Development of tunnel diode devices and models for circuit design and characterization

David Pawlik

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Development of Tunnel Diode Devices and Models for Circuit Design and Characterization

By

David J. Pawlik

A Thesis Submitted

in Partial Fulfillment

of the Requirements for the Degree of

Master of Science

in

Microelectronic Engineering

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COLLEGE OF ENGINEERING

ROCHESTER INSTITUTE OF TECHNOLOGY

ROCHESTER, NEW YORK

November 2007
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By

David J. Pawlik

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___________________ ____________________  
Name Date
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Abstract

Historically, the microelectronics industry has scaled down CMOS transistor dimensions in order to increase operating speeds, decrease cost per transistor, and free up on-chip real estate for additional chip functions. There are numerous challenges involved with scaling transistors down to the near term 32 nm node, and beyond. These challenges include short gate lengths, very thin gate oxides, short channel effects, quantum effects, band-to-band tunneling from source to drain, Gate Induced Drain Leakage, Fowler-Nordheim tunneling, and increasing dopant concentrations.

Field effect transistor circuits augmented with tunnel diodes lead to decreased circuit footprints, decreased device count, improved operating speeds, and lower power consumption without the need to solve current CMOS scaling challenges. Recently, N-on-P Si/SiGe resonant interband tunnel diodes (RITD) have been monolithically integrated with CMOS transistors. To further improve the benefits of RITD augmented circuits, P-on-N RITDS and all-Si RITDs were developed. Reported maximum peak-to-valley current ratios (PVCR), a key quantitative parameter of TDs, of 1.32 and 3.02 were measured, respectively.

Since integrated circuits operate at elevated temperatures, the I-V characteristics of various TDs were measured at temperatures ranging from room temperature up to 200°C. Three figures of merit were extracted; (i) peak current density ($J_P$), (ii) valley current density ($J_V$), and (iii) PVCR. Normalizing over their respective values at room temperature allowed for direct comparison between the various TD structures. This method allowed the author to determine that all devices show a similar $J_P$ response. However, the Si/SiGe RITD structure was overall least sensitive to temperature variations.

Furthermore, to design and optimize TD augmented circuits, a SPICE compatible model was developed. Past models have discontinuities, kinks in their slopes, difficult parameters to extract, unknown parameters, no closed form solutions, and/or poor fits to measured data. For this work a modified version of the S. M. Sze model with a superior match to experimental data, for Si based Esaki tunnel diodes (ETD) was developed. Using the developed model, several circuits were simulated, which were broken up into two groups. The first group of circuits is comprised of one TD and one of the following; (i) resistor, (ii) NMOS transistor, or (iii) TD. Finally, the behaviors learned from the simple circuits were used to simulate several TD augmented circuits such as (i) ADC comparator, (ii) TSRAM, (iii) and four basic logic gates.
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CHAPTER 1

Introduction and Motivation

Historically, the microelectronics industry has scaled down CMOS transistor dimensions in order to increase operating speeds, decrease cost per transistor, and free up on-chip real estate for additional chip functions. There are numerous challenges involved with scaling transistors down to the 32 nm node, and beyond. Due to large channel doping, short gate lengths, and very thin gate oxides – transistors are becoming dominated by short channel and quantum effects. Specifically, band-to-band tunneling from source to drain, Gate Induced Drain Leakage (GIDL), and Fowler-Nordheim tunneling (FN-tunneling) and direct tunneling of carriers between the gate and channel will dominate transistor characteristics without implementing new materials and device structures. Additionally, shrinking gate lengths and increasing dopant concentrations will make the transistors much more sensitive to varying numbers of dopant atoms in the channel region [1-4].

There are additional challenges related to DRAM and SRAM memory technologies. For DRAM, maintaining adequate storage capacitance and small transistor current leakages is becoming very difficult. Additionally, new materials with small sheet resistances for the word and bitlines will be needed in order to maintain desired operating speeds. SRAM is mainly having difficulties with maintaining adequate noise margins, minimizing soft errors, and there are significant lithography & etch issues to overcome [1].
Tunnel Diodes (TD) are being investigated as a CMOS augmentation technology. Integrating TDs leads to several advantages over an all-CMOS circuit design, at the same technology node. First, many common circuits can be simplified by significantly reducing device counts (some reductions exceed 80%) [5-9,11,19]. This directly results in a smaller on-chip footprint, freeing up space for other functions. Also, with a reduced device count, fewer contact cuts and metal lines are needed. This has several benefits such as smaller parasitic resistances and capacitances.

Historically, the power supply for FET driven circuits has been reduced as part of an effort to reduce power dissipation per transistor. Tunnel diode (TD) augmented circuits continue this trend by operating with even smaller voltage supplies and lower leakage currents, reducing the static power dissipation further [26, 27]. Finally, tunnel diodes have been shown to exhibit fast switching speeds, thereby increasing the operating frequency that circuits may be operated at.

Tunnel diodes discussed in this thesis are vertical devices. Currently, much of the work in Si-based systems has gone into developing resonant interband tunnel diodes (RITD) with the n-type layer on top of the p-type layer, referred to as an N-on-P RITD [10-28]. Further space savings can be made by developing an RITD structure with the p-type layer on top of the n-type layer, referred to as a P-on-N RITD. Such an RITD structure could be placed directly on top of the source/drain region of an NFET. Currently, the N-on-P RITD must be placed within the p-select region of an n-well [22, 26]. One goal of this study is to develop a P-on-N RITD structure for use in augmented circuits.
In order to design circuits for use on commercial products, quantitative models need to be developed. There are several extant physics and empirical based models. However, they have many difficulties including, but not limited to, (i) convergence issues, (ii) discontinuities, (iii) unknown parameters, and (iv) complex equations without closed form solutions. Additionally, circuits often operate at elevated temperatures, sometimes as high as 100°C, or greater. SPICE models that effectively model TDs, including at elevated temperatures, are needed by circuit designers in order to effectively design, characterize, and implement TD augmented circuits.

1.1. Organization of the Thesis

Chapter 2 of this thesis will discuss basic theory and physics related to the structure and operation of TDs. This theory and structure will be expanded upon in Chapter 3, which will discuss the development of two types of RITDs. The first half of the chapter will discuss the development of P-on-N Si/SiGe RITDs, then the development of a Si RITD, and the effect of anneal time on device characteristics.

High temperature measurements (0°C up to 200°C) on optimal N-on-P Si/SiGe RITD structure and proximity diffused ETDs are presented in Chapter 4. The results are then used in Chapter 5 to explore the viability of TD models developed by others. The chapter will then proceed with the development of a new model, which contains temperature variability and is Verilog-based SPICE compatible.

Finally, Chapters 6 and 7 utilize the models developed for this thesis to simulate simple and complex circuits, respectively. Load line analysis techniques will be used to qualitatively verify the simulation results of the simple circuits. The simple circuit results
are then used to verify the results of the complex circuits. The complex circuits simulated include analogue-to-digital converter comparators, tunneling SRAM cell, and basic logic gates. All simulations are performed using SIMUCAD’s Gateway (version 2.6.4.R) circuit simulation suite.

References for Chapter 1


CHAPTER 2

Tunnel Diodes

This chapter discusses basic quantum mechanical tunneling theory and its application towards TDs. The operation of three types of TDs is presented; (i) Esaki tunnel diodes (ETD), (ii) resonant tunnel diodes (RTD), and (iii) resonant interband tunnel diodes (RITD). Of particular interest for this thesis are ETDs and RITDs, both of which are the subjects of research in this thesis.

2.1. Tunnel Diode Benchmarks

A tunnel diode is a two terminal device that may be bipolar or unipolar in its current composition (referring to electrons or holes). At large biases, current flow follows thermal diffusion current characteristics similar to that of traditional diodes. However, there are several large deviations in current flow at small and reverse biases.

![Generic I-V characteristic for TDs. Peak and valley characteristic parameters are labeled.](image)

Fig. 2.1. Generic I-V characteristic for TDs. Peak and valley characteristic parameters are labeled.
The reverse bias breakdown is 0 V. Increasing bias slightly above 0 V results in a sharp increase in tunneling current. Further increasing bias causes the current to decrease, forming a region of negative differential resistance (NDR). A typical, generic, I-V characteristics curve may be seen in Error! Reference source not found..

\[ J_P = \frac{I_P}{A} \]  

(1)

\[ J_V = \frac{I_V}{A} \]  

(2)

There are three basic parameters used to characterize TD characteristics; (i) the peak, (ii) the valley, and (iii) the peak-to-valley current ratio (PVCR). The peak and valley voltages are referred as \( V_P \) and \( V_V \), respectively. The peak and valley currents (\( I_P \) and \( I_V \)) are often divided by the cross-sectional area (\( A \)) to obtain the effective current density of the devices, Eqs. (1) and (2). Ideally, \( J_P \) and \( J_V \) are independent of device geometries.

\[ PVCR = \frac{I_P}{I_V} = \frac{J_P}{J_V} \]  

(3)

The PVCR of a TD can be calculated using Eq. (3). The PVCR of a TD that exhibits NDR must be greater than 1. PVCR is often used as the primary characteristic of TDs.

2.2. Quantum Mechanical Tunneling

In classical mechanics, in order for a particle to overcome a barrier, it must be infused with a quantity of energy that is greater than the energy of the barrier. Otherwise, the particle will hit the barrier, and bounce backwards off of it. However, in quantum
mechanics particles must obey Schrödinger’s Wave Equation, Eq. (4a), which is a partial
differential equation involving a time derivative and Hamiltonian operator ($\hat{H}$), Eq. (4b).

$$i\hbar \frac{\partial \Psi}{\partial t} = \hat{H}\Psi$$  \hspace{1cm} (4a)

$$\hat{H} = -\frac{\hbar^2}{2m} \nabla^2 + V$$  \hspace{1cm} (4b)

This equation ties together the wave-like and particle-like nature of mass and
energy where $\hbar$ is Plank’s constant by $2\pi$, $t$ is time, $\Psi$ is the wave function, $m$ is the mass
of the particle, and $V$ is a potential of the barriers and/or wells. The 1-dimensional Time
Independent Schrödinger Equation (TISE) can be generated by assuming time (i) and
space (i) variables are separable, Eq. (5).

$$\Psi(x,t) = \psi(x)f(t)$$  \hspace{1cm} (5)

Applying Eq. (5) into Eq. (4a), and separating the variables,

$$\hat{H}\psi(x) = E\psi(x)$$  \hspace{1cm} (6)

When the mass of a small particle approaches a finite barrier whose energy is
greater than the particle, the wave function describing the particle’s motion will penetrate
the barrier. If the barrier is thin enough, the particle may “tunnel” through it, and end up
on the other side. As shown in Fig. 2.2, a particle with energy $E$, has an associated wave
function. When the wave function “hits” the potential barrier, of height $V_0$, the wave
function decays exponentially and then exits the barrier on the other side. Recall that
$\psi^*\psi$ is equal to the probability of finding the particle in any particular position at time
“$t$”. The extension of the wave function into and beyond the barrier indicates that there is
a statistical probability related to the particle tunneling through the barrier.
Fig. 2.2. Schematic diagram of a quantum particle and its corresponding wave function. The particle approaches a potential barrier, and has a probability of tunneling through it. Adopted from McKelvey [4].

An analytical solution can be found using the TISE differential equation. First, independent solutions to each of the three labeled regions are assumed to be linear combinations of complex exponentials, Eq. (7a-c).

Region I:  \[ \psi_I(x) = A \exp(ik_I x) + B \exp(-ik_I x); \quad k_I = \frac{2m\sqrt{E}}{\hbar} \]  

Region II:  \[ \psi_{II}(x) = C \exp(k_{II} x) + D \exp(-k_{II} x); \quad k_{II} = \frac{2m\sqrt{V_0 - E}}{\hbar} \]  

Region III:  \[ \psi_{III}(x) = F \exp(ik_{III} x); \quad k_{III} = k_I = \frac{2m\sqrt{E}}{\hbar} \]

Where \( E \) is the energy of the particle, \( i \) is imaginary number, and \( A, B, C, D, F \) are constants. The following requirements are used as boundary conditions; (i) particle conservation requires continuity of \( \psi(x) \) and (ii) momentum conservation requires the continuity of the first derivative of \( \psi(x) \) [2,3]. Since there are only 4 equations with 5 unknowns, constants \( B, C, D, \) and \( F \) can only be solved with respect to \( A \) (the initial incoming particle). However, the tunneling probability \( \mathcal{T} \) is a function of \( F/A \), and
therefore can be analytically solved (Eq. 8). Where \( k_{\mu} \) is the wave number of the particle inside the barrier, and \( W \) is the width of the barrier.

\[
T = \left( \frac{F}{A} \right)^* \left( \frac{F}{A} \right) = \frac{1}{1 + \left( \frac{1}{4} \right) \frac{V_0^2}{E(V_0 - E)} \sinh^2 \left( k_{\mu} W \right)}
\]  

(8)

This property of quantum mechanical tunneling can be employed by diodes, or diode-like structures in order to achieve the characteristic “N” shape I-V curve. The potential barriers are formed from the forbidden bandgap of semiconductors. The three basic types of TDs are (i) Esaki Tunnel Diodes (ETD), (ii) Resonant Tunnel Diodes (RTD), and (iii) and Resonant Interband Tunnel Diodes (RITD).

2.3. Esaki Tunnel Diode

In the 1950’s, intensive investigation into the internal field emission of pn junctions in semiconductor materials was being performed. Of great interest was the relationship of the I-V characteristics and doping concentration of the p and n type regions. Chenoweth, and other research groups, systematically increased the doping concentration in pn junctions, looking at breakdown voltages. With large enough concentrations, the breakdown was shifted to below 1 V. These diodes would start to conduct a greater current density in reverse bias than in forward bias, earning them the name of Reverse Diodes. Once the doping levels became degenerate for both terminals, Esaki began to notice a breakdown of 0 V in reverse bias. The forward bias characteristic would initially rise to a \( I_P \), then exhibit NDR and fall to an \( I_V \), and than rise again in the traditional thermal current. This is typical “N” shape characteristic was the first direct

Fig. 2.3. (a) I-V characteristic, and schematic band diagram for (b) reverse bias, (c) equilibrium, (d) peak tunneling current, (e) minimum direct tunneling current, and (f) thermal current for a generic ETD.

Looking at the progression of the band structure for an ETD, the I-V characteristics become clear, Fig. 2.3a. Without any applied bias, Fig. 2.3c, the Fermi energy is flat and is above $E_C$ on the n-type side, and below $E_V$ on the p-type side. Qualitative carrier density versus energy curves are provided for electrons and holes. The pn junction has a very sharp bend. In reverse bias, Fig. 2.3b, Zener tunneling occurs immediately, allowing for large amounts of current to flow. With a small amount of forward bias, electrons occupying states below $E_F$ in the n-side can begin tunneling to unoccupied (holes) states above $E_F$ on the p-side, Fig. 2.3d. Eventually, $E_C$ on the n-side
is shifted above $E_V$ on the p-side, which stops direct tunneling, Fig. 2.3e. However, the current does not drop down to 0 A; instead, carriers tunnel via indirect paths resulting in an excess current (topic discussed in more detail in Chapter 5). Finally, after a large enough bias is applied, the pn junction starts to behave like a standard diode, and a thermal current begins to flow, Fig. 2.3f.

The doping profiles need to be very sharp so that the tunnel barrier, primarily the bending of the bands, is very sharp and on the order of 10 nm thick or less. This helps to promote a high probability of tunneling, and therefore a large $I_P$. Often, the tunnel barrier is approximated as triangular in shape. The tunneling probability through such a barrier is discussed in more detail in chapter 4. However, the procedure for calculating the tunneling probability is the same, except that the Wentzel-Kramers-Brillouin (WKB) approximation is used for the sloped portion of the potential.

Additional affects to the tunneling probability depends on whether the semiconductor is a direct or indirect bandgap. Indirect bandgap materials require the addition of a momentum shift, usually from phonon interactions, in order to tunnel from the conduction band to valence band. Phonon-assisted tunneling is statistically less probable, and therefore $J_P$ and consequently the PVCR is smaller than it would be for a direct bandgap material.

### 2.4 Resonant Tunnel Diode

Unlike the bipolar ETDs, RTDs utilize only electrons (most common) or holes. These devices are formed with a series of narrow/wide/narrow/wide/narrow bandgap semiconductors. The wide bandgap material forms two tunneling barriers, between
which a narrow bandgap material forms a quantum well. When the well is of an appropriate thickness, one or more discrete quantum states will be formed, Fig. 2.4a. When a bias is applied such that a quantum state lines up with occupied states in the conduction band, Fig. 2.4b, a large amount of current will flow. A slightly larger bias will cause the occupied states to no longer be aligned with a quantum state in the quantum well, resulting in a decrease in current, Fig. 2.4c. With a larger bias, electrons will just flow right over the top of the tunnel barrier, creating a diode-like I-V characteristic.

![Band diagrams and IV characteristic of a generic RTD](image)

**Fig. 2.4.** Schematic band diagrams (a-b) and IV characteristic (d) of a generic RTD. Band diagram at (a) equilibrium, (b) $I_P$, and (c) $I_V$ are shown. Figure adopted from McKelvey [4].

As can be seen, this device is symmetric. Therefore, the forward and reverse bias I-V characteristics are equal in magnitude. In order for tunneling to occur, the tunnel barriers must be on the order of 3 nm to 10 nm thick. The heterojunction must be extremely sharp, on the order of less than 2.5 nm. The most common method of fabrication for RTDs uses molecular beam epitaxy (MBE), which can achieve these vary
sharp junctions and grow high quality crystals. Since at least two semiconductor systems are needed, III-V systems that are lattice matched are typically used.

2.5 Resonant Interband Tunnel Diode

RITDs are a mix of ETDs and RTDs. They are bipolar devices, with quantum wells in both the n and p sides. Like RTDs, the quantum states in the wells must be aligned in order for current to flow. When the states are misaligned, a minimum in current will occur. However, like ETDs, a large enough bias will cause a thermal current to flow like a normal diode. Additionally, this device is asymmetric, and therefore the reverse current does not match forward characteristics. The quantum wells can be formed in two main ways. Using multiple semiconductors, a quantum well in the n and p type regions can be formed, similarly to RTDs, Fig. 2.5.

Another method utilizes δ-doping planes, Fig. 2.6. Like a normal ETD, the n-type and p-type terminals are heavily doped. However, in the middle there would be an intrinsic layer (i-layer), that ultimately forms the tunnel barrier. On either end of the i-layer, a theoretically perfect plane of dopant atoms (n-type for the cathode side, and p-type for the anode side) is placed. This causes triangular wells to form, Fig. 2.6, on both sides of the i-layer.
Fig. 2.6. (a) Schematic band diagram of a generic RITD device, via $\delta$-doping planes as proposed by Sweeny and Xu [5]. The quantum wells are triangular in shape. (b) The discrete energy levels and corresponding wave functions for a triangular well, adopted from Gossman [6].

All of the RITDs discussed in this thesis are Si-based and use $\delta$-doping planes to form the quantum wells. This device was first developed in Si by Rommel, et al. [1], and further developed by Jin, et al. [7].

References for Chapter 2

CHAPTER 3

Development of Si/SiGe P-on-N RITDs and Si RITDs

This chapter discusses the development of RITDs. First, a brief overview of the historical development of Si and Si/SiGe RITDs is discussed, starting with the first device fabricated by Rommel, et al. [2] in 1998. Then the work performed for developing P-on-N Si/SiGe RITDs is presented. This study includes a look at the effect of the tunnel barrier composition, and the P δ-doping concentration, used to form the electron quantum well. Finally, development work on Si RITDs, including the effect of anneal time will be presented. Key parameters of interest are $J_P$ and PVCR.

3.1. Historical Development

In 1998, Rommel et al., fabricated the first Si/SiGe RITD [2]. Low-Temperature Molecular Beam Epitaxy (LT-MBE) was used to grow the RITD, using B as the p-type dopant and Sb as the n-type dopant. A PVCR of 1.5 was achieved. Reducing substrate temperatures during growth, and modifying dopant concentrations, layer thicknesses, and switching to P for the n-type dopant improved device characteristics.

Only B has been used for p-type doping, whereas Sb and P have been used for the n-type doping. The dopant species used are limited by processing considerations, and not electrical properties. Injector (cladding) dopant concentration and thickness are engineered to minimize parasitic resistances, and should not interfere with the δ-doping plane and tunnel barrier. Typically, concentrations have ranged from $2 \times 10^{19}$ cm$^{-3}$ to greater than $10^{20}$ cm$^{-3}$. The thicknesses have been varied between 100 nm and 250 nm.
The δ-doping planes need a large area concentration, with a very narrow full width half maximum (FWHM). Literature has reported concentrations ranging from $5 \times 10^{13}$ cm$^{-2}$ to $3 \times 10^{14}$ cm$^{-2}$, with FWHM of 3 nm to 5 nm. The tunnel barrier may incorporate Ge, typically 0% to 50%, with thicknesses of 2 nm to 16 nm. It is critical that the tunnel barrier region has very low defect densities and doping concentrations.

Table 3.1. Published reports of RITD Structures. For a complete description of the devices, review reference [2,3-5,6] starting from the left.

<table>
<thead>
<tr>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>N-type Dopant</td>
<td>Sb</td>
<td>Sb</td>
<td>Sb</td>
<td>Sb</td>
<td>P</td>
<td>P</td>
</tr>
<tr>
<td>P-type Dopant</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
</tr>
<tr>
<td>Injector Conc. (10$^{19}$ cm$^{-3}$)</td>
<td>Sb = 4.0, B = 2.0</td>
<td>Sb = 2.0, B = 4.0</td>
<td>Sb &gt; 10.0</td>
<td>3*10$^{14}$ cm$^{-2}$</td>
<td>4.0</td>
<td>5.0</td>
</tr>
<tr>
<td>Injector Thickness</td>
<td>100 nm</td>
<td>100 nm</td>
<td>100 nm</td>
<td>100 nm</td>
<td>100 nm</td>
<td>100 nm</td>
</tr>
<tr>
<td>δ-doping Conc. (10$^{14}$ cm$^{-2}$)</td>
<td>Sb = 3.0, B = 0.7</td>
<td>Sb = 3.0, B = 0.7</td>
<td>Sb = 3.0, B = 3.0</td>
<td>Intrinsic w/cap 10$^{20}$ cm$^{-3}$</td>
<td>P = 0.5, B = 1.0</td>
<td>P = 1.0, B = 1.0</td>
</tr>
<tr>
<td>δ-doping FWHM (nm)</td>
<td>3-5</td>
<td>3-5</td>
<td>3-5</td>
<td>3-5</td>
<td>5</td>
<td>3</td>
</tr>
<tr>
<td>Tunnel Barrier Thickness (nm)</td>
<td>4 &amp; 6</td>
<td>2 &amp; 4</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Tunnel Barrier Ge Conc.</td>
<td>50%</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
<td>0%, 30%, 50%</td>
<td>40%</td>
</tr>
<tr>
<td>PVCR</td>
<td>1.54</td>
<td>1.42</td>
<td>2.05</td>
<td>1.7</td>
<td>4.2</td>
<td>3.8</td>
</tr>
</tbody>
</table>

The target parameters for the best Si/SiGe RITD structure to date are as follows, whose cross-section can be seen in Fig. 3.1. Both injector concentrations should be $5 \times 10^{19}$ cm$^{-3}$, with a thickness of 100 nm. A δ-doping concentration of $1 \times 10^{14}$ cm$^{-2}$ encloses an intrinsic layer (i-layer) that consists of 4 nm of SiGe and 2 nm of Si. The tunnel barrier is defined by the i-layer thickness which can be adjusted to tailor the $J_P$ [6]. These TDs are similar to those reported by Jin, et al. [6], first fabricated by Rommel, et al. [1], with the composite i-layer tunnel spacer of SiGe (4 nm) and Si (2 nm).
After growth of the RITD structure, via LT-MBE, fabrication commences at RIT. Samples are annealed by rapid thermal anneal (RTA). The temperature is ramped at 100°C/sec up to the target temperature which is generally between 500°C and 800°C. Then, mesas are formed using an SF₆/CHF₃ reactive ion etch, with Al used as the etch mask, providing electrical isolation. The I-V characteristics were then measured using a Keithley 4200 Semiconductor Parameter Analyzer.

In 2003, Sudirgo was the first to integrate RITDs with CMOS transistors [7,8]. Recall that the RITD structure used has the p⁺ anode on the bottom. Therefore, integrating the two technologies required that the RITDs be grown within a LOCOS oxide opening on top an implanted p-select region. The RITD has a very low thermal budget. Therefore, the CMOS front-end processing was completed as normal, before any RITD processing or integration occurs. Oxide openings are formed, designating the location of the RITDS, and LT-MBE growth is done. After the RITDs are annealed and etched, back-end processing is completed. A schematic cross-section can be seen in Fig. 3.2.
Fig. 3.2. Cross-section schematic diagram of RITD integrated with NMOS. RITD is grown on top of p$^+$ well, with LOCOS isolation. A P-on-N RITD could be integrated directed on top of a source/drain region of an NMOS transistor. Diagram is not to scale.

3.2. P-on-N Si/SiGe RITD Development

Large space savings can be achieved by integrating the RITD directly on top of the source/drain (S/D) region of the NMOS transistor. Currently, the optimized structure is an N-on-P RITD structure, referring to the p-type terminal being located at the bottom of the device structure. Therefore, that particular RITD must be integrated on top of a p$^+$ well. With a P-on-N RITD structure, the n-type terminal would be on the bottom allowing for integration directly on top of an NMOS S/D region, Fig. 3.3.

The schematic device structure, Fig. 3.4, for the P-on-N RITD is the same as the traditional N-on-P version flipped upside down. As mentioned above, sharp doping profiles are needed for good I-V characteristics. Factors that affect doping profiles include (i) semiconductor material (Si vs. Si$_x$Ge$_{1-x}$), (ii) target doping concentration, (iii) doping species, and (iv) substrate temperature during growth. The substrate temperature was kept at the lowest value for which a low defect crystal can be grown. This minimizes surface segregation, which broadens doping profiles upwards towards the semiconductor.
surface [10,11]. Dopant species have differing surface segregation. Boron and Phosphorous have the smallest surface segregation for p-type and n-type dopants, respectively.

Fig. 3.3. Schematic diagram of P-on-N RITD integrated directly on top of NMOS S/D region. Diagram is not to scale.

Fig. 3.4. Circuit symbol (left) and device structure schematic (right) of P-on-N RITD. Various thicknesses for undoped SiGe (X nm) and Si (Y nm) were grown. Several target P δ-doping plane concentrations were also grown.
Two experiments were performed by varying the (i) thicknesses of the undoped Si and SiGe layers, and (ii) the area concentration of the P δ-doping plane. In the first experiment, the undoped SiGe (labeled as X nm) layer was grown to thicknesses of 4 nm, 2 nm, and 3 nm. The undoped Si layer was grown to thicknesses of 2 nm, 4 nm, and 3 nm, respectively. The target P δ-doping area concentration was $1.00 \times 10^{14}$ cm$^{-2}$. For the second experiment, both undoped layers were held constant at 4 nm. The P δ-doping concentrations were changed to $1.00 \times 10^{14}$ cm$^{-2}$, $1.50 \times 10^{14}$ cm$^{-2}$, and $1.25 \times 10^{14}$ cm$^{-2}$. Table 3.2 displays the details of these 2 experiments. Rows 1 to 3 refer to experiment 1, and rows 4 to 6 refer to experiment 2.

Table 3.2. Targeted thicknesses and concentrations used for experiment 1 (rows 1 to 3) and experiment 2 (rows 4 to 6).

<table>
<thead>
<tr>
<th>Sample #</th>
<th>Undoped SiGe (X nm)</th>
<th>Undoped Si (Y nm)</th>
<th>P δ-doping ($10^{14}$ cm$^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4</td>
<td>2</td>
<td>1.00</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>4</td>
<td>1.00</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>3</td>
<td>1.00</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>4</td>
<td>1.00</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
<td>4</td>
<td>1.50</td>
</tr>
<tr>
<td>6</td>
<td>4</td>
<td>4</td>
<td>1.25</td>
</tr>
</tbody>
</table>

3.2.1 Undoped Si and SiGe layer Thicknesses Experiment

Each sample was broken into 4 pieces which were annealed at 650°C, 700°C, 750°C, and 800°C. After Al (with 1% Si) contacts were deposited, and mesas were etched (for electrical isolation), I-V measurements were made. I-V characteristic for sample #2, Fig. 3.5, is representative of the other two samples in this experiment. There is no discernible trend in the I-V characteristics with respect to the anneal temperature.
Fig. 3.5. I-V characteristics for Sample #2 annealed at 650°C, 700°C, 750°C, and 800°C, respectively. There is no discernible trend with anneal temperature.

Fig. 3.6. (a) PVCR, and (b) $J_P$ versus anneal temperature for samples #1, #2, and #3. There is a small downward trend in PVCR and $J_P$ with respect to increasing anneal temperature. Standard N-on-P RITD results included in $J_P$. 
The PVCR and $J_p$ exhibit a small downward trend with respect to anneal temperature, Fig. 3.6, for each P-on-N RITD in this study. This trend is very noisy. The PVCR for a standard N-on-P RITD (not shown) consistently increases with anneal temperature. This indicates that the structure is not properly optimized. There is a clear decreasing trend in $J_p$ and $J_V$ versus the thickness of undoped SiGe in the $i$-layer, Fig. 3.7, for the pieces annealed at 800°C. This indicated that larger undoped Si thicknesses in the $i$-layer improve device characteristics. It is well documented that the surface segregation of P increases rapidly as the Ge content increases. Therefore, moving the SiGe layer further away from the P $\delta$-doping layer will help to limit the amount of dopants to diffuse into the $i$-layer, keeping the doping profile very sharp. This led the researchers to hold the SiGe and Si $i$-layer thicknesses at 4 nm for the second experiment.

![Graph showing the trend of PVCR, $J_p$, and $J_V$ with undoped SiGe and Si thicknesses.](image)

**Fig. 3.7.** The maximum $I_{\text{Latch}}$ (right axis) and $V_{\text{DD}}$ (left axis) versus temperature. $I_{\text{Latch}}$ data points were fitted with a quadratic. $V_{\text{DD}}$ was fitted with a line.
3.2.2 P δ-doping Concentration Experiment

Similarly to the previous experiment, each sample was broken into 4 pieces which were annealed at 650°C, 700°C, 750°C, and 800°C. After Al (with 1% Si) contacts were deposited via sputtering. Mesas were etched (for electrical isolation), I-V measurements were made. I-V characteristic for sample #5, Fig. 3.8, is the best working device for this example. Increasing the anneal temperature decreased the current density and shifted the peak and valley to smaller biases. The inset graph shows PVCR versus anneal temperature, which exhibits no trend.

![Sample #5 I-V characteristics](image)

Fig. 3.8. I-V characteristics of Sample #5 for the anneal temperatures of 650°C, 700°C, 750°C, and 800°C. The inset shows the PVCR versus anneal temperature.

The $I_P$ and PVCR versus P δ-doping concentration can be seen in Fig. 3.9. Quadratic line fits are shown for both data sets. $I_P$ increased with concentration until the
PVCR started to increase. In conclusion, increasing the undoped Si layer thickness and the P δ-doping concentration improves the I-V characteristics.

![Graph showing IP and PVCR versus P δ-doping concentrations. Each data set was fitted with a quadratic line.]

Fig. 3.9. $I_P$ and PVCR versus P δ-doping concentrations. Each data set was fitted with a quadratic line.

### 3.3. Si RITD Development

To avoid the added complexities of utilizing SiGe layers, all Si RITDs were grown, Fig. 3.10a. However, those structures used Sb instead of P as the n-type dopant. This study also looks at the effect of anneal times up to 10 min.

The schematic device structure of the RITDs fabricated for this study is shown in Fig. 3.10a. Highly doped p-type substrates (<0.005 Ω-cm) were prepared with a surface clean, and immediately placed under vacuum within the MBE reactor. A 1 nm, undoped Si layer was grown with a substrate temperature of 650°C. The substrate was then cooled to 500°C during the subsequent growth of 250 nm of $p^+$ Si (1.00×10^{18} cm^{-3}). The silicon growth was stopped, and the B δ-doping plane was formed while dropping the substrate temperature to 320°C; where it remained for the rest of the growth. An undoped spacer
layer of 6 nm of Si was grown on top of the B δ-doping plane. The P δ-doping plane was grown, followed by 100 nm of n⁺ Si (1.00×10¹⁸ cm⁻³). Finally, three sets of P δ-doping planes and undoped Si layers were grown to form the cathode contact layers. Two devices were grown with different P δ-doping concentrations, Fig. 3.10b, of 0.75×10¹⁴ cm⁻² (TD1) and 1.00×10¹⁴ cm⁻² (TD2).

![Device Structure](image)

<table>
<thead>
<tr>
<th>Device</th>
<th>P-δ-doping (cm⁻²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TD1</td>
<td>0.75×10¹⁴</td>
</tr>
<tr>
<td>TD2</td>
<td>1.00×10¹⁴</td>
</tr>
</tbody>
</table>

Fig. 3.10. (a) Schematic device structure of the Si RITD grown. (b) P δ-doping concentrations used for TD1 and TD2.

Initial experimentation found that the optimal rapid thermal anneal (RTA) temperature is below 600°C. Further experimentation by Park at Ohio State University found that the optimal anneal temperature is 575°C. Two different RTA times of; (1) 5 min. at 575°C and (2) 10 min. at 575°C, were performed on TD1 and TD2. Un-annealed samples (as-grown) were processed for comparison. A lift-off photolithography process was used to form the Al cathode contacts. A reactive ion etch using CHF₃/SF₆ chemistry was used to etch mesas, thereby electrically isolating devices from each other. Al deposited on the backside of the sample was used as the anode contact.
Table 3.3b lists $J_P$ versus anneal time for TD1 and TD2. TD1 has a smaller $J_P$ than TD2. After 10 minutes of annealing, TD1 shows a large increase in $J_P$ (1.62 kA/cm$^2$). $J_P$ for TD2 increases linearly with anneal time, up to 2.91 kA/cm$^2$. Also provided in the table is the best device reported in Ref. [9], which is of the same order of magnitude as TD1 and TD2. The PVCR for both devices, Table 3.3b, increases with anneal time. The as-grown PVCRs for TD1 and TD2, 2.48 and 2.57 respectively, is larger than the best reported device in Ref. [9], with a PVCR of 2.08. The PVCR for TD1 and TD2 increases up to 2.75 and 3.02 for the 10 min. anneal times, respectively.
Table 3.3. (a) $J_P$ results for TD1 and TD2. Ref. [9] shows similar magnitude in current density. (b) PVCR results for TD1 and TD2. The as-grown PVCR is larger than Ref. [9], and increases with anneal time.

<table>
<thead>
<tr>
<th>Time (min.)</th>
<th>$J_P$ (kA/cm$^2$)</th>
<th>PVCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>TD1</td>
<td>TD2</td>
<td>Ref. [6]</td>
</tr>
<tr>
<td>As-grown</td>
<td>1.42</td>
<td>1.98</td>
</tr>
<tr>
<td>5</td>
<td>1.34</td>
<td>2.46</td>
</tr>
<tr>
<td>10</td>
<td>1.62</td>
<td>2.97</td>
</tr>
</tbody>
</table>

(a)

(b)

In conclusion, $J_P$ and PVCR increase when anneal time is increased from 5 min. to 10 min. After a 10 minute anneal, the maximum $J_P$ and PVCR values for TD1 and TD2 are 1.62 kA/cm$^2$, 2.91 kA/cm$^2$, 2.48, and 2.57, respectively. For TD2, $J_P$ increased linearly with anneal time. For TD1 and TD2, most of the improvements in PVCR occur within the first 5 minutes of annealing. PVCR continues to increase after 5 minutes of anneal, but at a slower rate.

3.4. Conclusion

P-on-N RITDs that exhibited NDR were fabricated. In general, increasing anneal temperature decreased $J_P$ and PVCR. Increasing the SiGe and decreasing the Si components of the $i$-layer decreased $J_P$. A maximum PVCR of 1.06 was achieved with SiGe/Si thicknesses of 3nm/3nm. The P $\delta$-doping concentration has an undetermined effect on $J_P$. However, PVCR increased up to 1.33 with a P $\delta$-doping concentration of $1.5\times10^{14}$ cm$^{-3}$.

For the Si RITDS, $J_P$ and PVCR increase when anneal time is increased from 5 min. to 10 min. After a 10 minute anneal, the maximum $J_P$ and PVCR values for TD1 and TD2 are 1.62 kA/cm$^2$, 2.91 kA/cm$^2$, 2.48, and 2.57, respectively. For TD2, $J_P$
increased linearly with anneal time. For TD1 and TD2, most of the improvements in PVCR occur within the first 5 minutes of annealing. PVCR continues to increase after 5 minutes of anneal, but at a slower rate.

References for Chapter 3

CHAPTER 4

High Temperature DC Characterization of Si/SiGe RITD and Proximity Diffused ETD

This chapter discusses the DC characteristics of Si/SiGe RITDs and proximity diffused ETDs at temperatures ranging from room temperature (298K) up to 200°C (473K). Key parameters under investigation are PVCR, $J_p$, and $J_V$ as a function of temperature. The normalized $J_p$ values will be compared with a physics-based model. The normalized $J_V$ of the devices measured for this study is also compared to ETDs and Si/SiGe RITDs fabricated at various other facilities. These results are used in Chapter 5, for the development of a SPICE simulator compatible model.

4.1. Theoretical Current vs. Temperature Response

![ETD band structure and energy barrier seen by an electron tunneling through the pn junction. Both structures are approximated as triangles.](image)

Fig. 4.1. (a) ETD band structure and (b) energy barrier seen by an electron tunneling through the pn junction. Both structures are approximated as triangles.

As the temperature of the TD is increased, the magnitude of the current will also increase. To understand this effect on the tunneling current, the peak tunneling
probability (associated with $J_P$) will be analyzed. The band structure near the pn-junction for both ETDs and RITDs, can be approximated as triangular, as well as the tunnel barrier as shown in Fig. 4.1. The tunneling current equation developed by Kane [1,2] in Eq. 4.1a, assumes that the TD is formed from a direct bandgap semiconductor.

$$J_t = \frac{q^2 E}{36\pi h^2} \sqrt{\frac{2m_m^*}{E_g}} \times D \times T_t$$

(4.1a)

$$T_t = \exp \left( -\frac{4\sqrt{2m_m^* E_g^{3/2}}}{3qhE} \right)$$

(4.1b)

where $T_t$ is the tunneling probability, $E$ is the average electric field in the depletion region as given by Eq. 4.2, $m_m^*$ is the average effective mass of electrons and holes given by Eq. 4.3, $D$ is an integral incorporating the Fermi-Dirac distribution functions ($F_C$ and $F_V$) shown in Eq. 4.4, and $E_g$ is the bandgap.

$$E = \sqrt{\frac{q(\Psi_{bi} - V_P)N_{A,D}}{4\varepsilon_s}}$$

(4.2)

where $\Psi_{bi}$ is the built-in potential of a pn-junction, $V_P$ is the peak voltage of a TD, and $\varepsilon_s$ is the permittivity of the semiconductor in use.

$$m_m^* = 2 \left( \frac{1}{m_e^*} + \frac{1}{m_h^*} \right)^{-1}$$

(4.3)

$$D \equiv \int \left[ F_C(E) - F_V(E) \right] \left[ 1 - \exp \left( -\frac{2E_S}{E} \right) \right] dE$$

(4.4)

where $E_S$ is the energy of an electron in the conduction band minus the conduction band energy level.

With high doping levels the exponential, which is the approximate tunneling probability, will dominate any changes in $J_t$ with respect to temperature. Recall that the
bandgap of a semiconductor decreases as temperature increases. As the bandgap decreases, $T$ will become larger. The net result is an increase in $J_P$.

At about 500K $n_i = 3 \times 10^{14} \text{ cm}^{-3}$, which is much less than the doping levels of these TDs. Therefore $n = N_d$ in the n-type electrode and $p = N_a$ in the p-type electrode. In other words, as the temperature increases the bandgap decreases. The bandgap forms the tunnel barrier. Since the tunneling probability is exponentially related to the inverse barrier thickness, significant increases in $J_P$ are expected as the temperature increases.

The $V_P$ can be calculated from Eq. 4.5 [3], where $V_n'$ and $V_p'$ are defined by Eq. 4.6 [4].

$$V_P = \frac{V_n' + V_p'}{3}$$

$$V_n' = \frac{E_{f_n} - E_C}{q} = \frac{kT}{q} \left[ \ln \left( \frac{n}{N_C} \right) + 2^{3/2} \left( \frac{n}{N_C} \right) \right]$$

$$V_p' = \frac{E_f - E_f^p}{q} = \frac{kT}{q} \left[ \ln \left( \frac{p}{N_V} \right) + 2^{3/2} \left( \frac{p}{N_V} \right) \right]$$

Where $E_{f_n}$ and $E_{f_p}$ are the Fermi levels of the n-type and p-type electrodes, respectively. $N_C$ and $N_V$ are the effective density of states for the conduction and valence band, respectively. The density of states increases more rapidly than $kT/q$ with respect to temperature. Therefore, $V_n'$ and $V_p'$ get smaller as temperature increases, driving $V_P$ to lower voltages.

The $J_V$ is mainly dependent upon the excess current and diffusion current. The excess current utilizes deep level traps within the forbidden bandgap, formed via defects, in order to increase the tunneling probability. It is therefore reasonable to expect an increase in excess current with an increase in temperature. Furthermore, the diffusion
current, discussed below, may also be significant in determining $J_V$. The diffusion current also increases with temperature. Therefore, $J_V$ will also increase with temperature, possibly faster than $J_P$.

The post-valley current is dominated by the standard diffusion current, Eq. 4.7 and 4.8, associated with non-degenerately doped pn-junctions.

$$J_{\text{diffusion}} \approx J_0 \exp\left(\frac{qV}{kT}\right) \quad (4.7)$$

$$J_0 = qn_i^2 \left(\frac{D_p}{N_d L_p} + \frac{D_n}{N_a L_n}\right) \quad (4.8)$$

For a given applied bias, the saturation current density, $J_0$, increases at a faster rate than the exponential. The increase in $J_0$ results from the exponential growth in $n_i$, increase in $D_{n,p}$, and a decrease in $L_{n,p}$. This increase dominates $J_{\text{diffusion}}$, thereby increasing the post-valley current. It is expected that the diffusion current increases more rapidly than the excess current, thereby shifting $V_V$ to smaller values.

With a high enough temperature, $n_i$ becomes comparable to, and eventually dominates the carrier concentrations. This causes the device to look more and more like intrinsic silicon. At 500K, $n_i$ is approximately $3 \times 10^{14}$ cm$^{-3}$, which is much less than the doping in the TDs being measured. Measurements were not made above 480K, keeping carrier concentrations dominated by doping concentrations.

4.2. Devices Structures and Experimental Setup

The RITDs, Fig. 4.2, consist of degenerately doped p$^+$ and n$^+$ Si injector regions with B and P concentrations of $5 \times 10^{19}$ cm$^{-3}$, respectively. The active region is inserted between the injectors and incorporates p and n δ-doping regions surrounding an intrinsic
Si-based tunneling spacer layer. The tunnel barrier thickness is fundamentally defined by this $i$-layer. These TDs are similar to those reported by Jin, et al. [6,7], first fabricated by Rommel, et al. [5], with the composite $i$-layer tunnel spacer of $\text{Si} (X \text{ nm})$ and $\text{SiGe} (Y \text{ nm})$ varied to study their influence on temperature effects, as shown in Table 4.1. Three different $X \text{ nm}/Y \text{ nm}$ composite thicknesses were grown using LT-MBE: $1 \text{ nm}/3 \text{ nm}$ (TD4), $2 \text{ nm}/4 \text{ nm}$ (TD6), and $4 \text{ nm}/4 \text{ nm}$ (TD8).

Table 4.1. Composition and thicknesses of $i$-layers used for the RITDs in this study.

<table>
<thead>
<tr>
<th>Device</th>
<th>$i$-Si ($X \text{ nm}$)</th>
<th>$i$-SiGe ($Y \text{ nm}$)</th>
<th>$i$-layer (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TD4</td>
<td>1</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>TD6</td>
<td>2</td>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td>TD8</td>
<td>4</td>
<td>4</td>
<td>8</td>
</tr>
</tbody>
</table>

The ETDs were fabricated by Krom [8] using a proximity spin-on glass diffusion technique used by Wang, et al. [9]. The dopant sources employed used Emulsitone’s Phosphorosilicafilm (n-type) and Borofilm (p-type) spin-on glass dopants. The process commences by saturating the Si surface with P using a proximity diffusion technique.
Fig. 4.3. ETD fabricated by rapid thermal proximity diffusion.

A Si wafer coated with the spin-on glass dopant is separated by a ~400 µm air gap from the device wafer. The composite is then rapid thermal annealed by ramping up at 30°C/sec to 850°C for 1 sec. This was followed by an additional drive-in at 850°C for 90 seconds. The B dopant was then introduced using the same technique, excluding the drive-in step. The overall device structure is shown in Fig. 4.3. The peak dopant concentrations are expected to be of the order of 1×10²⁰ cm⁻³ with a junction depth of ~10 nm. Degenerately doped ETDs with abrupt junctions have depletion widths less than 10 nm. Therefore, the ETD is still approximately a long base.

Fabrication of the RITD and ETD devices commenced by forming mesas for electrical isolation using an SF₆/CHF₃ reactive ion etch, with Shipley 1813 photoresist as the etch mask. Aluminum with 1% Si was used for contact formation; deposited via sputtering or thermal evaporation for the RITDs or ETDs, respectively. The I-V characteristics were then measured using a Keithley 4200 Semiconductor Parameter Analyzer. The temperature of the heat chuck was controlled by an ΩE Omega CSC32-J bench top controller. A thermocouple was mounted in direct contact with the wafer for all measurements.

Initial measurements were taken at room temperature and used as reference points, with subsequent readings in 10K increments from 303K to 473K. The room temperature \( J_P \) was measured as 2.2 kA/cm², 3.1 kA/cm², 0.30 kA/cm², and 1.0 A/cm² for
TD4, TD6, TD8, and ETD, respectively. Room temperature PVCR values of 2.3, 3.0, 3.3, and 1.8 were determined for TD4, TD6, TD8, and ETD, respectively. The values of each parameter were normalized with respect to their respective values at room temperature. This normalization technique allows for direct comparison of key parameters, which vary as much as three orders of magnitude, between all devices.

4.3. Measured TD characteristics vs. Temperature

Fig. 4.4 shows that the current density of the four devices studied varies over three orders of magnitude. Thinner $i$-layer thicknesses result in higher current densities. This trend reverses when the $i$-layer becomes too small and is discussed in more detail by Jin, et al. [7]. The ETDs have lower current densities than all of the RITDs. The PVCR of the devices ranges from 1.8 up to 3.3. This wide range of device characteristics will lead to the extrapolation of general trends regarding the behavior of proximity diffused Si ETDs and MBE grown Si/SiGe RITDs.

![I-V characteristics of RITDs and ETD used in this study.](image)
4.3.1. I-V Characteristics of TDs vs. Temperature

The I-V characteristics of TD8 and ETD are shown Fig. 4.5. The current density increases with temperature over the entire bias range. The $J_V$ increases at a faster rate than $J_P$, causing the PVCR to decrease with respect to temperature. Even though NDR is present for all devices over the entire temperature range, it may disappear if the temperature becomes high enough. The $V_P$ and $V_V$ voltages decrease with increasing temperature. These qualitative observations agree with the predictions made above. Additionally, the results do not depend upon the direction of temperature change, or the length of time spent at that temperature.

![Graphs showing I-V characteristics](image)

Fig. 4.5. I-V characteristics for TD8 (a), and ETD (b). For both devices the current density for all biases increases. $V_P$ and $V_V$ shift to lower voltages. $J_V$ increases at a faster rate than $J_P$, therefore the PVCR must decrease with temperature.
4.3.2. PVCR vs. Temperature

Fig. 4.6. Decreasing PVCRs with increasing temperature for all four TDs.

Fig. 4.7. PVCR normalized over their respective values at 313K versus temperature. The RITDs decrease at the same rate. The ETD device decreases faster than the RITDs.
The variation in PVCR as a function of temperature is illustrated in Fig. 4.6. The PVCR of TD4, TD6, TD8, and the ETD devices at 373K (typical high end operating temperature of many integrated circuits) are 2.0, 2.6, 2.9, and 1.4 respectively. As seen in Fig. 4.6, extrapolating over the given temperature range indicates there is a critical temperature \( T_{\text{critical}} \) at which the PVCR will equal 1. The \( T_{\text{critical}} \) for each device is above 473K, and increases linearly with larger initial (room temperature) PVCRs. The PVCR normalized at 313K are shown in Fig. 4.7. The PVCR for the RITD structures all decrease at the same rate. The PVCR for the ETD device decreases at a faster rate.

4.3.3. Normalized \( J_P \) vs. Temperature

![Normalized J_P vs. Temperature](image)

Fig. 4.8. \( J_P \) normalized at 313K. The rate of increase is approximately the same for all TDs measured. The solid line is calculated from the tunneling probability portion of Eq 4.1, including a fitting coefficient of \( \frac{1}{4} \) within the exponential. The model starts to break down at ~400K.

Fig. 4.8 displays \( J_P \) normalized at 313K for all TDs. All of the normalized \( J_P \) curves overlay each other, showing a universal temperature response. The small
deviation of the ETD curve is expected to be a result of parasitics from the test setup, and probe contacts. The solid line was calculated from the tunneling probability, Eq 4.1a. The equation was modified slightly with an empirical fitting coefficient of $\frac{1}{4}$ within the exponential. This coefficient helps to account for the reduction in tunneling probability associated with phonon assisted indirect tunneling in silicon. The model fits the data well up to about 400K. Above this temperature the model significantly overestimates the measured results. The effective mass of holes and electrons become heavier with temperature, but were held constant for the calculations made above. Larger effective masses reduce tunneling probabilities, correcting some of the error seen in the curve.

### 4.3.4. Normalized $J_V$ vs. Temperature

The normalized $J_V$ results in Fig. 4.9 show that $J_V$ increase more quickly than the normalized $J_P$, which results in the drop in PVCR seen in Fig. 4.6 and Fig. 4.7. The RITD normalized $J_V$ curves change at the same rate, whereas the ETD structure increases more rapidly. This explains why the normalized PVCR for ETD devices decreases more rapidly than the RITDs. Fig. 4.10 overlays normalized $J_V$ values for TDC and ETD as well as data from other published studies. This data includes (i) another rapid thermal proximity diffused ETD [10], (ii) an MBE grown ETD [11], and (iii) another Si/SiGe RITD ($i$-layer of 3 nm) [10]. The ETD fabricated by Wang, et al. [9] exhibits the strongest temperature dependence compared to all other devices studied. The ETDs studied by Wernersson, et al. [11], and fabricated for this study display a temperature sensitivity that is slightly stronger than the RITD structures. Si/SiGe RITD normalized $J_V$ exhibits the weakest temperature dependence compared to all other TDs in this study.
Fig. 4.9. $J_v$ normalized at 313K. The rate of increase is the same for all RITDs, which is smaller than that of the ETD.

Fig. 4.10. Normalized $J_v$ at 295K of 2 devices from this study, and 3 TDs fabricated elsewhere. The proximity diffused ETDs have a stronger temperature dependence with respect to the RITD structures (including the device fabricated by Jin [10].
4.4. Conclusion

In conclusion, the RITD structures are less sensitive to temperature variations, and maintain larger PVCRs, making these structures the best qualified for memory and digital logic applications through integration with Si FETs. Normalizing key parameters allowed for direct comparison of various TD structures with current densities ranging over three orders of magnitude. This technique exposed a universal behavior in normalized tunneling current ($J_V$) versus temperature, which can be used as the basis of an experimentally based model. $J_V$ for RITDs and ETD showed well behaved trends that can also be employed in an empirically based model. Normalized $J_V$ results clearly show that RITDs are the least sensitive to temperature variations. The modified normalized tunneling probability model agrees with the data up to ~400K, at which point it begins to overestimate the measured results.

References for Chapter 4

7. N. Jin, S-Y Chung, R. Yu, R. Heyns, P. Berger, P. Thompson, “The Effect of Spacer Thicknesses on Si-Based Resonant Interband Tunneling Diode Performance and
CHAPTER 5
Empirical Tunnel Diode Model Developed For SPICE DC Simulations

This chapter discusses large signal DC interband tunnel diode models for use with PSPICE simulation tools. There are two basic types of models: (1) physics-based [1-6], and (2) empirical fits [7-13]. This chapter will give an overview of the physics-based and empirical fit models developed by others. Then, a modified version of the S.M. Sze model [11] created by the author will be discussed in detail. The modified model will be applied to the proximity diffusion ETD discussed in Chapter 4. Temperature effects will also be included in the final model. The following chapters (Chapters 6 and 7) will utilize this model for circuit simulations.

5.1. Introduction

The physics-based models are mathematically intensive to calculate and require parameters that are not easily measured, extracted, or calculated. Integrals that are a function of bias voltage, temperature, bandgap, density of states, and quasi-Fermi energy levels are unavoidable. The integrals have no closed form solutions and require numerical solutions at every bias point along an I-V curve.

The direct tunneling model for ETDs discussed in Section 4.1., was developed by Kane [1]. Recall that the tunnel barrier is approximated as triangular, with a tunneling probability given by Eq. 5.1b, which does not include phonon assisted tunneling in indirect bandgap semiconductors. The full tunneling current is given by Eq. 5.1a, where $D$ is calculated numerically from Eq. 5.2.
The above equations were used to calculate \( J_P \) of Ge ETDs over a range of doping levels by Demmassa, \textit{et al.} [3], and Meyerhofer, \textit{et al.} [4]. The results agreed very well with measured data, as seen in Fig. 5.1. To enable Eq. 5.1a use with indirect bandgaps, \( T_t \) must be modified to include the assistance of phonon energy \( (E_P) \). This is accomplished by changing \( E_g \) to \((E_G + E_P)\), in \( T_t \).

\[
J_t = \frac{q^3 E}{36\pi h^2} \sqrt{\frac{2m^*}{E_g}} \times D \times T_t \tag{5.1a}
\]

\[
T_t = \exp \left( -\frac{4\sqrt{2m^* E_g^{3/2}}}{3qhE} \right) \tag{5.1b}
\]

\[
D \equiv \int \left[ F_C(E) - F_V(E) \right] \left[ 1 - \exp \left( -\frac{2E_g}{E} \right) \right] dE \tag{5.2}
\]

Fig. 5.1. \( J_P \) for Ge ETDs vs. doping concentration. Theoretical results were calculated using Eq. 5.1a. Figure was obtained from [11], page 426.
The excess current is more difficult to model. The same difficulties as with the tunneling current exist, with the addition of several factors. Since the excess current occurs while the conduction band on the n-side is above the valence band on the p-side, there is no direct tunneling path. Therefore, carriers must tunnel to an intermediate state within the forbidden band gap, above the valence band. Then, they must recombine, giving off their energy as a photon or phonon. Several possible tunneling paths are depicted in Fig. 5.2.

![Diagram of tunneling via available states within the forbidden bandgap.](image)

**Fig. 5.2.** Tunneling via available states within the forbidden bandgap. These tunneling patterns give rise to the excess current. The magnitude of current is largely dependent upon the density of states within the bandgap.

The excess tunneling current was first modeled by Chenoweth [5], using paths A and B shown in Fig. 5.2. The form of the excess current is similar to Eq. 5.1a, where the density of states used is the density of states within the bandgap, which arise from impurities (such as metals) within the semiconductor and crystalline defects. Since these defects are process induced, it is extremely difficult to measure and predict their density. Therefore, a defect density must be chosen to fit the measured data.

A recent study by Rivas, *et al.* [6] suggests that direct tunneling (even for indirect bandgap semiconductors) and the inclusion of gap states in the contact regions result in
the best fits. There are many other assumed parameters in the model, leading to discrepancies between calculated results and measured.

In the end, the complexity of the models makes them impractical for use in circuit simulations. This leads many researchers to use empirical fits. The simplest is a list of measured data points from a TD, where linear approximations are used for interpolations [7]. This method inherently will not be perfectly smooth. This issue, along with inherent difficulties with simulating NDR characteristics can lead to simulation stability issues.

More complex fits have been proposed; such as (1) the use of multiple discrete devices (diodes, switches, current sources, resistors, and capacitors) [8,9], and (2) complex polynomial and trigonometric functions [11,12]. Although the use of discrete devices is simple for simulation via SPICE, it is difficult to determine all of the parameters needed. Polynomial functions are easy to work with; however, high order polynomials (six orders or higher) are needed for good fits [10]. The I-V characteristics are also divided into multiple sections, leading to kinks or even discontinuities in the simulated curve. Additionally, the fits cannot be trusted at all beyond the fitting range. There is no difficulty obtaining the coefficients needed for best fits using this method, but there is no relationship to physical properties or structure.

Trigonometric and exponential functions help reduce discontinuities, and smooth out the curve fits. These functions re-introduce some physical parameters, such as $J_P$, $J_V$, $V_P$, and $V_V$. Some parameters may be difficult to obtain. The functions are more limited in their ability to model various I-V shapes. Two such models, one reported by S. M. Sze [11] and the other by Yan [12], will be discussed in more detail in sections 5.2 and 5.3,
respectively. A modified version of the S. M. Sze model was developed by the author, and compared to the other models in sections 5.4.

5.2. S.M. Sze Empirical Model

The S.M. Sze model [11], Eq. 5.3, is the sum of three terms, the terms representing the tunneling (Eq. 5.4a), excess (Eq. 5.4b), or diffusion (Eq. 5.4c) current. The excess current requires a fitted parameter, \( B_2 \), which can be easily obtained from the post-valley slope of the I-V curve on a semi-log plot. The diffusion current is the standard ideal diode equation, where \( k \) is Boltzmann’s constant, \( T \) is the temperature, and \( J_0 \) is the saturation current.

\[
J_{Total} = J_{Tunnel} + J_{Excess} + J_{Diffusion}
\]

\[
J_{Tunnel} = \left( \frac{J_p}{V_p} \right) \times V \times \exp \left[ -\left( \frac{1}{V_p} \right) (V - V_p) \right]
\]

(5.4a)

\[
J_{Excess} = J_V \times \exp \left[ B_2 \left( V - V_r \right) \right]
\]

(5.4b)

\[
J_{Diffusion} = J_0 \times \exp \left[ qV_a / kT \right]
\]

(5.4c)

These model equations have several benefits over a polynomial or list fit. First, all three current components \( (I_{Tunnel}, I_{Excess}, I_{Diffusion}) \) are summed together in order to achieve the final results \( (I_{Total}) \). \( I_{Total} \) is a well-behaved and smooth function since each term is itself well-behaved and smooth. Simulations performed with this model are stable. Second, all of the parameters used for the model are easily obtained from measured I-V characteristics, or calculated from basic principles and ideal diode equations.
Fig. 5.3. Measured proximity diffused ETD, modeled $I_{\text{Tunnel}}$, $I_{\text{Excess}}$, $I_{\text{Diffusion}}$, and $I_{\text{Total}}$. The table (inset) includes the model parameters used for $I_{\text{Total}}$. $I_{\text{Total}}$ (S.M. Sze Model) overestimates $I_{\text{Measured}}$ over the entire bias range.

The S.M. Sze model was applied to a proximity diffusion ETD, Fig. 5.3. $I_{\text{Total}}$ overestimates the current for the entire bias range, and does not match the shape of the measured device in some regions. In reverse bias, the modeled current is dominated by $I_{\text{Tunnel}}$, which drastically overestimates the current. The measured data has a significant bend, reducing the current flow through the device. Alone, $I_{\text{Tunnel}}$ models the forward bias tunneling current very well. However, $I_{\text{Excess}}$ adds a significant magnitude to $I_{\text{Tunnel}}$ resulting in an overestimation of $I_{\text{Total}}$ in that region. Due to the fitted $B_2$ parameter, the excess current has the correct slope. However, the excess current does not dominate until significantly after $V_V$, therefore $I_V$ is too large and shifted to the left. Finally, $I_{\text{Diffusion}}$ does not match the measured data at all. Instead of an increase in slope, the slope of the measured curve begins to decrease, similarly to the reverse current. The values used for the model parameters are displayed in the table in the inset of Fig. 5.3.
Fig. 5.4. Measured Si/SiGe RITD, modeled $I_{\text{Tunnel}}$, $I_{\text{Excess}}$, $I_{\text{Diffusion}}$, and $I_{\text{Total}}$. The table (inset) includes the model parameters used for $I_{\text{Total}}$. $I_{\text{Total}}$ (S.M. Sze Model) overestimates $I_{\text{measured}}$ over the entire bias range. $I_{\text{Tunnel}}$ does not model the shape of the tunneling current accurately.

Similar to the ETD device, the S.M. Sze model overestimates the current of a Si/SiGe RITD, shown in Fig. 5.4. The modeled tunneling current rises faster then expected. Stays relatively flat around the peak and valley regions. This is in opposition to the measured characteristic which rises more slowly, peaks sharply, and then falls off more quickly. The model equation for $J_{\text{Tunnel}}$ does not work well for a $V_P$ greater than $\sim 0.1$ V.

5.3. Yan Empirical Model

Yan, et al. [12] developed a model that utilizes Gaussian curves in order to address some of the issues seen in the S.M. Sze model. The Yan model, Eq. 5.5, is composed of three terms, Eq. 5.6, 5.7, and 5.8. The rise in tunneling current, positive differential resistance (PDR), uses the left side of a Gaussian. The NDR region is
modeled with a separate right-sided Gaussian or an exponential. The post-valley current is modeled with an exponential similar to the ideal diode equation. $I_{PDR}$ and $I_{NDR}$ use a characteristic standard deviation in order to determine the shape of the Gaussian curves, which are independent of each other. The parameter “$a$” is a large constant ($a \gg 1$), and can be used to smooth out the curve in the region of $V_p$.

$$I_{Total} = I_{PDR} \cdot [1 - H(V_p)] + I_{NDR} \cdot H(V_p) + I_{Diode} \quad (5.5)$$

$$I_{PDR} = (1/2) \cdot I_P \cdot \exp \left[ \frac{-(V - V_p)^2}{\sigma_{PDR}^2} \right] \cdot [1 - \tanh(a(V - V_p))] \quad (5.6)$$

$$I_{NDR} = (1/2) \cdot I_P \cdot \exp \left[ \frac{-(V - V_p)^2}{\sigma_{NDR}^2} \right] \cdot [1 - \tanh(a(V - V_p))] \quad (5.7a)$$

$$I_{NDR} = (1/2) \cdot I_P \cdot \exp \left[ \frac{-(V - V_p)}{\sigma_{NDR}} \right] \cdot [1 - \tanh(a(V - V_p))] \quad (5.7b)$$

$$I_{Diode} = B \cdot \exp(D \cdot V) \quad (5.8)$$

Constants $B$ and $D$, as part of $I_{Diode}$, are fitted to the post-valley I-V characteristic, instead of calculated from the ideal diode equations. $I_{Total}$ utilizes two Heaviside step functions, so that $I_{PDR}$ is only used from a bias of 0 V up to $V_p$. Then, $I_{NDR}$ takes over and dominates until $I_{Diode}$ becomes large enough. Using piecewise equations tends to make simulations unstable. However, Yan, et al. [12] and Prost, et al. [13], report that non-convergence errors rarely occur.
The Yan model has been applied to a Si/SiGe RITD, as seen in Fig. 5.5. For a sharper valley, Fig. 5.5a, a Gaussian curve is used for $I_{\text{NDR}}$, Eq. 5.7a. For the RITDs, there is a significant difference between the measured valley current, and the modeled current, Fig. 5.5a. However, using an exponential for $I_{\text{NDR}}$ (Eq. 5.7b), allows for a broad valley that accurately models the measured results. The $J_P$ is overestimated by a small amount. Larger PVCRs will result in $I_{\text{Diode}}$ contributing a fractionally smaller magnitude to $J_P$. The tunneling current models the measured characteristic very well, except at less than 0.05 V. The modeled current is much greater than 0 A at a bias of 0 V, which can result in significant simulation errors. This discrepancy will become smaller with larger
$V_p$ values, due to the Gaussian “bell curve” nature of the model. Additionally, the model does not work in reverse bias, requiring another piecewise term.

5.4. Modified S.M. Sze Model

The S.M. Sze model (discussed in section 5.2) has been improved with several simple modifications by the author. First, $J_{Total}$ (Eq. 5.6) is the sum of two terms, $J_{Tunnel}$ and $J_{Excess}$. The term $J_{Diffusion}$ is not used. In order to model the decrease in slope in reverse bias, a denominator is added to $J_{Tunnel}$ (Eq. 5.7a), where $V_A$ and $A_3$ manipulates when the denominator begins to decrease the slope. $A_4$ is subtracted from $V_p^{-1}$ in the numerator to determine the slope. The measured $J_p^*$ is calculated by Eq. 5.8. The correction factor is calculated from the effect of the denominator used in $J_{Tunnel}$, and the value of $J_{Excess}$ (Eq. 5.7b) evaluated at $V_p$.

\[
\begin{align*}
J_{Total} &= J_{Tunnel} + J_{Excess} \\
J_{Tunnel} &= \frac{\left(\frac{J_p^*}{V_p}\right) V \exp\left[-\left(\frac{1}{V_p}\right)(V - V_p)\right]}{1 - A_3 \cdot V \exp[-A_4 (V - V_A)]} \\
J_{Excess} &= \frac{(J_V/2) \exp[B_3 (V - V_v)]}{1 + B_3 \cdot \exp[B_4 (V - V_B)]} \\
J_p^* &= \left[J_p \cdot J_{Excess}(V_p)\right] \frac{[J_p / J_{Tunnel}(V_p)]]}{}}
\end{align*}
\]

Similar to $J_{Tunnel}$, an exponential was placed in the denominator of Eq. 5.7b, for $J_{Excess}$. Three additional parameters were added, $B_3$, $B_4$, and $V_B$, which serve similar functions as their counterparts in Eq. 5.7a. Many of the parameters, $J_p$, $J_V$, $V_p$, $V_v$, $V_A$ and $V_B$ are easily extracted from the I-V characteristics. The rest of the parameters are fitted to give the best fit possible.
Fig. 5.6. Measured proximity diffused ETD, modeled using modified S.M. Sze model (Eq. 5.6 & 5.7). The table (inset) includes the model parameters used for $I_{\text{Total}}$. $I_{\text{Total}}$ shows an extremely close fit to the measured data.

The device in Fig. 5.3, was remodeled with the modifications shown in Eq. 5.7 and 5.8. The modeled I-V characteristic closely matches the measured results, seen in Fig. 5.6. The modifications made to the model corrected the deficiencies of the of the S.M. Sze model. The modeled $J_P$, $J_V$, and PVCR are within 0.7% of measured, and $V_P$, $V_V$ are within 7.0% of measured, shown in Table 5.1.

Table 5.1. Measured versus modeled peak and valley characteristics. The percent change is included, and indicates that the model is very close to the measured results.

<table>
<thead>
<tr>
<th>Measured</th>
<th>Model</th>
<th>% Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>$J_P$</td>
<td>56.4 µA</td>
<td>56.6 µA</td>
</tr>
<tr>
<td>$V_P$</td>
<td>75 mV</td>
<td>80 mV</td>
</tr>
<tr>
<td>$J_V$</td>
<td>31.3 µA</td>
<td>31.2 µA</td>
</tr>
<tr>
<td>$V_V$</td>
<td>250 mV</td>
<td>265 mV</td>
</tr>
<tr>
<td>PVCR</td>
<td>1.80</td>
<td>1.81</td>
</tr>
</tbody>
</table>
The modified model is perfectly smooth, and therefore convergence problems during simulations are rare. Parameters are easily extracted from and fitted to measured data. The equations are easy to work with, and SPICE compatible. Modeled current is not significantly overestimated at any bias. The shape of the modeled curve closely fits the measured data.

5.5. Adding Temperature Variability to the Modified Model

The temperature results for the proximity diffused ETDs discussed in Chapter 4 have been modeled in Fig. 5.7. Only five temperatures - 296K, 333K, 373K, 413K, and 473K.

Fig. 5.7. Modified model applied to the proximity diffusion ETD at multiple temperatures. (a) The Modeled I-V characteristics fit the measured data in forward and reverse bias for all temperatures. (b) Close up of the peak and valley characteristics.
473K – have been modeled. The forward and reverse bias characteristics, Fig. 5.7a, fit the characteristics well over the entire bias range.

A close-up of the peak and valley, Fig. 5.7b, shows only small differences between measured and modeled. In Table 5.2 the difference between measured and modeled $V_P$ and $V_V$, with a maximum percent change of 7%, are listed. The same comparison is made for $I_P$ and $I_V$ in Table 5.3. All differences are within 3%.

Table 5.2. Measured versus modeled $V_P$ and $V_V$ characteristics. The difference between and percent change between measured and modeled are small, indicating that the model is a good fit.

<table>
<thead>
<tr>
<th>Temperature (K)</th>
<th>$V_P$ (V) Meas.-Model %Change</th>
<th>$V_V$ (V) Meas.-Model %Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>296</td>
<td>-0.005 6.67</td>
<td>-0.015 6.00</td>
</tr>
<tr>
<td>333</td>
<td>-0.005 6.67</td>
<td>-0.010 4.26</td>
</tr>
<tr>
<td>373</td>
<td>-0.005 6.67</td>
<td>-0.005 2.33</td>
</tr>
<tr>
<td>413</td>
<td>-0.005 6.67</td>
<td>-0.005 2.56</td>
</tr>
<tr>
<td>473</td>
<td>0.000 0.00</td>
<td>-0.010 6.45</td>
</tr>
</tbody>
</table>

Table 5.3. Measured versus modeled $I_P$ and $I_V$ characteristics. The difference between and percent change between measured and modeled are small, indicating that the model is a good fit.

<table>
<thead>
<tr>
<th>Temperature (K)</th>
<th>$I_P$ (mA) Meas.-Model %Change</th>
<th>$I_V$ (mA) Meas.-Model %Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>296</td>
<td>-0.161 0.29</td>
<td>0.055 0.18</td>
</tr>
<tr>
<td>333</td>
<td>-0.167 0.29</td>
<td>0.031 0.09</td>
</tr>
<tr>
<td>373</td>
<td>-0.153 0.25</td>
<td>-0.089 0.21</td>
</tr>
<tr>
<td>413</td>
<td>-0.178 0.29</td>
<td>1.463 2.98</td>
</tr>
<tr>
<td>473</td>
<td>0.000 0.00</td>
<td>1.190 1.97</td>
</tr>
</tbody>
</table>

5.5.1. Modeling Parameters vs. Temperature

The model parameters used in Fig. 5.7 were manually fitted for each temperature. Several parameters, $V_P$, $V_a$, $A_d$, $V_b$ were held constant at 0.075V, 0.2V, 10V$^{-1}$, 0.81V, respectively. Appropriate function fits for the other parameters were found, as a function of temperature.
Fig. 5.8. Model parameters $A_3$ and $(1/2)J_V$ versus temperature. Curve fits (solid lines and equations) are provided in the figure.

A plot of $A_3$ and $\frac{1}{2}J_V$ versus temperature is shown in Fig. 5.8. $J_V$ was modeled with a simple exponential function. A simple exponential was used for $\frac{1}{2}J_V$. However, due to the more complex nature of $A_3$, a fraction with exponentials in the numerator and denominator was needed. Similarly, exponential fits for $V_V$ and $J_P$ versus temperature can be found in Fig. 5.9. Included in the figure are the resulting $J_P^*$ values, which do not follow a simple exponential relationship. The change in coefficients $B_2$, $B_3$, and $B_4$ versus temperature, Fig. 5.10, use natural logarithm, line, and exponential fits, respectively.
Fig. 5.9. Model parameters $V_V$ and $J_P$ versus temperature. Curve fits (solid lines and equations) are provided in the figure. Calculated $J_P^*$ does not follow a simple exponential fit.

\[ V_V = C_0 + C_1 \times \exp(R_2 \times T) \]
\[ C_0 = 300 \text{ (mV)} \quad C_1 = -14.0 \text{ (mV)} \]
\[ R_2 = 4.32 \times 10^{-3} \text{ (K)} \]

\[ J_P = J_{P0} \times A \times \left[ 1 - \exp\left( B_1 \times (18.7 + T) \right) \right] \]
\[ J_{P0} = 56.4 \text{ (µA)} \quad A = 1.27 \]
\[ B_1 = -4.92 \times 10^{-3} \text{ (K)} \]

Fig. 5.10. Model parameters $B_2$, $B_3$, and $B_4$ versus temperature. Curve fits (solid lines and equations) are provided in the figure.

\[ B_2 = a \times \ln(T) + b \]
\[ a = 14.1 \text{ (1/V)} \quad b = -72.4 \text{ (1/V)} \]

\[ B_3 = A + B \times T \]
\[ A = -0.254 \text{ (1/V)} \quad B = 0.0238 \text{ (1/VK)} \]

\[ B_4 = a \times \exp(b \times T) \]
\[ a = 1.05 \times 10^{-3} \quad b = 20.2 \times 10^{-3} \]
5.5.2. Model with Temperature Variability

Using the functions developed above, the I-V characteristics of the ETD can be simulated accurately within the design space (298K up to 473K). The forward and reverse bias simulated characteristics, Fig. 5.11a, fit very well. There is greater deviation at larger biases. However, the fit close to \( V_P \) and \( V_I \), Fig. 5.11b, is of greater importance.

![Graphs showing I-V characteristics for multiple temperatures](image)

Fig. 5.11. Modified model, using temperature variability, applied to the proximity diffusion ETD at multiple temperatures. (a) The Modeled I-V characteristics fit the measured data in forward and reverse bias for all temperatures. (b) Close up of the peak and valley characteristics.

In Table 5.4 the differences between measured and simulated \( V_P \) and \( V_I \), with a maximum percent change of 6.67%, are listed. The same comparison is made for \( I_P \) and \( I_V \) in Table 5.5. All percent changes are within 3%. The changes for \( V_P \) and \( V_I \) are the same as the manually fitted characteristics summarized in Table 5.2 and Table 5.3. The average difference and percent change in \( I_P \) and \( I_V \) increased by approximately 1%.
However, the range (maximum minus minimum) was reduced by about $\frac{1}{2}$. The close fit of the simulated characteristic to the measured shows that this model can be used for accurate simulation of TD augmented circuits, which will be discussed in Chapters 6 and 7.

Table 5.4. Measured versus simulated $V_P$ and $V_V$ characteristics. The difference between and percent change between measured and modeled are small, indicating that the model is a good fit.

<table>
<thead>
<tr>
<th>Temperature (K)</th>
<th>$V_P$ (V)</th>
<th>Meas.-Sim.</th>
<th>%Change</th>
<th>$V_V$ (V)</th>
<th>Meas.-Sim.</th>
<th>%Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>296.00</td>
<td>-0.005</td>
<td>6.67</td>
<td></td>
<td>-0.015</td>
<td>6.00</td>
<td></td>
</tr>
<tr>
<td>333.00</td>
<td>-0.005</td>
<td>6.67</td>
<td></td>
<td>-0.010</td>
<td>4.26</td>
<td></td>
</tr>
<tr>
<td>373.00</td>
<td>-0.005</td>
<td>6.67</td>
<td></td>
<td>-0.010</td>
<td>4.65</td>
<td></td>
</tr>
<tr>
<td>413.00</td>
<td>-0.005</td>
<td>6.67</td>
<td></td>
<td>-0.005</td>
<td>2.56</td>
<td></td>
</tr>
<tr>
<td>473.00</td>
<td>0.000</td>
<td>0.00</td>
<td></td>
<td>-0.010</td>
<td>6.45</td>
<td></td>
</tr>
</tbody>
</table>

Table 5.5. Measured versus simulated $I_P$ and $I_V$ characteristics. The difference between and percent change between measured and modeled are small, indicating that the model is a good fit.

<table>
<thead>
<tr>
<th>Temperature (K)</th>
<th>$I_P$ (mA)</th>
<th>Meas.-Sim.</th>
<th>%Change</th>
<th>$I_V$ (mA)</th>
<th>Meas.-Sim.</th>
<th>%Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>296.00</td>
<td>-0.161</td>
<td>0.29</td>
<td></td>
<td>-0.026</td>
<td>0.08</td>
<td></td>
</tr>
<tr>
<td>333.00</td>
<td>-0.903</td>
<td>1.55</td>
<td></td>
<td>-0.289</td>
<td>0.80</td>
<td></td>
</tr>
<tr>
<td>373.00</td>
<td>-0.985</td>
<td>1.63</td>
<td></td>
<td>-0.334</td>
<td>0.80</td>
<td></td>
</tr>
<tr>
<td>413.00</td>
<td>-1.190</td>
<td>1.92</td>
<td></td>
<td>0.435</td>
<td>0.89</td>
<td></td>
</tr>
<tr>
<td>473.00</td>
<td>-1.190</td>
<td>1.85</td>
<td></td>
<td>0.866</td>
<td>1.44</td>
<td></td>
</tr>
</tbody>
</table>

5.6. Conclusion

In conclusion, a modified version of S. M. Sze’s model was developed to accurately simulate TDs with low $V_P$. The model uses parameters extracted from empirical data. Temperature variability has been added to the model for additional functionality. The model is perfectly smooth, and has been fitted to a proximity diffused ETD. The model has been shown to fit the data very well, and has been employed in a SPICE circuit simulator.
References for Chapter 5

CHAPTER 6

Simulation of Simple Circuits with Bistability

This chapter discusses the simulation of three simple circuits that exhibit a bistable region. Bistability refers to a situation where an applied voltage causes the circuit to latch onto one of two stable sense node voltages ($V_{SN}$). Previous biasing conditions determine which stable state $V_{SN}$ latches onto, and therefore the circuit can be used as a memory cell. Three simple circuits, exhibiting bistability, consisting of a TD serially connected to a resistor (section 5.1), NFET (section 5.2), or TD (section 5.3) as the load are discussed below. All simulations utilize the modified Sze model discussed in Chapter 5, and were completed with SIMUCAD’s Gateway (version 2.6.4.R) circuit simulation suite.

6.1. TD and Resistor in Series

The first circuit to be discussed is a resistor (load) in series with a TD (driver), seen in the inset of Fig. 6.1. A load line analysis for $V_{SN}$, Fig. 6.1, clearly shows why bistability occurs. When the resistor is too small, for example 3.7 kΩ, the load line intersects the TD curve (Driver) only at 1 point, indicating the value of $V_{SN}$. Once the resistor becomes large enough, 7.4 kΩ, the load line intersects the driver line at 3 points; (1) near the peak, (2) in the NDR region, and (3) near the valley. The NDR region is relatively unstable. Therefore there exist two stable $V_{SN}$ latching points, resulting in a bistable circuit. Increasing the resistor more causes the difference between high and low
$V_{SN}$ to increase. More importantly, the range of $V_{DD}$ that results in bistability increases a lot. Therefore, $V_{DD}$ can fluctuate more and have a minimal effect on the output.

![Load line analysis of Resistor (Load) in series with a TD (Driver). Three different resistances are shown; (1) 3.7 kΩ, (2) 7.4 kΩ, and (3) 11.1 kΩ. As resistance decreases, the region of bistability decreases until it disappears. The inset to the figure shows the circuit schematic.](image)

The I-V characteristic curves, Fig. 6.2, show that $V_P$ and $V_Y$ shift to the right. Since the magnitude of $I_P$ is larger than $I_Y$, $V_P$ moves faster than $V_Y$. Eventually $V_P$ moves past $V_Y$ ($V_P > V_Y$), creating a region of bistability. The critical resistance ($R_{crit}$), minimum resistance needed for bistability, may be obtained from Eq. (1) [1]. The TD-only measured values of $V_P$, $V_Y$, $I_P$, and $I_Y$ are used. The calculated $R_{crit}$ for the tunnel diode used in these simulations is 7.35 kΩ.

$$R_{crit} = \frac{V_Y - V_P}{I_P - I_Y} \quad (5.1)$$
In Fig. 6.2, the solid line represents a $V_{DD}$ being swept from low to high, and the dashed line represents a reverse sweep. Over most of the I-V curve, the forward and reverse sweeps overlap each other indicating only one stable latching point for $V_{SN}$. For the 7.4 kΩ, 11.1 kΩ, and 14.8 kΩ resistors, the forward and reverse sweep curves separate for a region, indicating bistability. As the resistor increases, the range of $V_{DD}$ that results in bistability also increases. Note that $I_P$ and $I_V$ do not change.

![Figure 6.2](image)

Fig. 6.2. I-V characteristic for a resistor and TD in series. Forward and reverse $V_{DD}$ sweeps shown in order to highlight bistable regions. As the resistor increases, $V_P$ and $V_V$ also increase. Bistability occurs with at least 7.4 kΩ resistance. The region of bistability increases as the resistor increases.

Recall that increasing temperature significantly (1) increases $I_P$ and $I_V$, (2) shifts $V_V$ to the left, and (3) has a minimal effect on $V_P$. This causes the bistable region to shift to the right (large $V_{DD}$) and shrink in size. If the resistor is small enough, the bistability region may even disappear, Fig. 6.3. For clarity, only three temperatures are shown; (1) 23°C, (2) 100°C, and (3) 200°C.
Fig. 6.3. I-V characteristics for 7.4 kΩ resistor in series with a TD at 23°C, 100°C, and 200°C. The bistable region shifts to the right, and decreases in size as temperature increases. The Bistable region disappears for the 200°C measurement.

Similar analysis can be performed on $V_{SN}$, Fig. 6.4 and Fig. 6.5. First, just looking at changes in resistance, Fig. 6.4, bistability does not occur until a 7.4 kΩ resistor is used. As the resistance increases the region of bistability increases, and the difference between the high ($V_H$) and low ($V_L$) voltages increase. These observations agree with the predictions made from the load line analysis, Fig. 6.1, and the I-V characteristics, Fig. 6.2. $V_{SN}$ for the 0 kΩ curve follows $V_{DD}$ exactly, since there is no voltage drop across the resistor. Using the 0 kΩ line as a reference, none of the $V_H$ values are close to $V_{DD}$, indicating a very low gain (< 0.5) for this circuit.

Temperature has a similar effect on $V_{SN}$, Fig. 6.5. The bistable region decreases in size and shifts to the right as the temperature increases. At 200°C the bistability vanishes.
Fig. 6.4. $V_{SN}$ for multiple resistors at 23°C. As the resistance increases, the bistable region increases in size and shifts to the right.

Fig. 6.5. $V_{SN}$ with 7.4 kΩ resistor in series with a TD at 23°C, 100°C, and 200°C. The bistable region shifts to the right, and decreases in size as temperature increases. The bistable region disappears for the 200°C measurement.
The effects discussed here have been briefly discussed with actual measurements elsewhere [1]. The results qualitatively agree with each other. There exists a minimum resistance needed for bistability to occur. Increasing the resistance will increase the bistable region, which can be seen in the I-V characteristics curves, and a plot of $V_{SN}$ vs. $V_{DD}$. Factoring in temperature, first time such an analysis has been completed, shows that increasing temperature will decrease bistability, and possibly even makes it disappear. In the end, this shows that the circuit is highly sensitive to both of these factors. This would not be an appropriate circuit for digital logic and memory applications due to the sensitivity to resistance, temperature, and low gain. However, it may be useful for on chip temperature measurements.

### 6.2. TD and NMOS in Series

For this circuit, inset of Fig. 6.6, there are two voltages to apply; (1) gate voltage ($V_g$) and (2) drain voltage ($V_{DD}$). Therefore, bistability can be achieved by holding the $V_g$ constant and sweeping $V_{DD}$, or sweeping $V_g$ and holding $V_{DD}$ constant.

The load line analysis for sweeping $V_g$ can be seen in Fig. 6.6a. When $V_g$ is too small or too large (2.5 V and 3.5 V, respectively), there is only one allowable $V_{SN}$ state. For a range of $V_g$, there exist two stable latching points and one relatively unstable latching point in the NDR region. Note that in this case, $V_{SN}$ is bistable but the currents for both states are equal to each other.

The load line analysis for sweeping $V_{DD}$ can be seen in Fig. 6.6b. When $V_{DD}$ is too small or large (0.75 or 1.75, respectively), there is only one stable latching point for
For a range of $V_{DD}$, the circuit is bistable. Both the current through the circuit and $V_{SN}$ are bistable for this case.

Fig. 6.6. Load line analysis of NFET in series with TD. (a) Sweeping $V_g$ and holding $V_{DD}$ constant. (b) Sweeping $V_{DD}$ and holding $V_g$ constant.

Results for sweeping the gate can be seen in Fig. 6.7. When $V_{DD}$ is too small, $V_{SN}$ stays low. Once $V_{DD}$ becomes large enough, a large bistable region forms. As $V_{DD}$ increases from this point, the bistability decreases and shifts a small amount to the left (smaller biases). Smaller $V_g$ biases can be achieved by using FET models with larger gain, larger gate widths, and/or smaller gate lengths.

Case 2, sweeping $V_{DD}$ can be seen in Fig. 6.8. $V_{SN}$ does not initial show bistability, for $V_g$ of 2.75 V. Once $V_g$ gets large enough, a large bistability region occurs. The bistable region decreases in size as $V_g$ continues to increase, and it shifts significantly to the left. One can see similar results for the I-V characteristics, Fig. 6.8b.
Fig. 6.7. Simulation results for the sense node ($V_{SN}$). The $V_{DD}$ was held constant while $V_g$ was swept in both forward and reverse. No bistability occurs (0.75 V) until a large enough $V_{DD}$ is applied. Then, increasing $V_{DD}$ decreases the region of bistability.

Fig. 6.8. Simulation results for the (a)$V_{SN}$ and (b)current. The $V_g$ was held constant while $V_{DD}$ was swept in both forward and reverse. No bistability occurs (2.75 V) until a large enough $V_g$ is applied. Then, increasing $V_g$ decreases the region of bistability and shifts it to the left.

6.3. Two TDs in Series

The load line analysis for TDs in series can be seen in Fig. 6.9. Similar to the previous circuits, if $V_{DD}$ is to small or large there is only one stable latching point. For
the remaining biases, $V_{SN}$ will be bistable, however the current is not. The I-V characteristics, Fig. 6.10, exhibit two peaks and valleys. Increasing temperature increases both peaks and valleys, and shifts them to the left. This follows the effect of temperature on one TD.

![Graph showing current vs. VDD for two TDs in series](image)

**Fig. 6.9.** Load line analysis of 2 TDs in series.

$V_{sn}$ as a function of $V_{DD}$ for multiple temperatures, Fig. 6.11, clearly shows the bistable region. The bistable region starts at about the first peak ($V_{P1}$) in the I-V characteristic, and ends after the second valley ($V_{V2}$). The bistable region decreases in size, both horizontally and vertically, as temperature increases. This agrees with decreasing $V_{V2}-V_{P1}$ and decreasing PVCRs with increasing temperature. This circuit has the best gain, $(V_H - V_L)/V_{DD}$, upwards of 90%. This circuit is the best candidate for use in a TSRAM cell, and will be discussed in Chapter 7.
Fig. 6.10. I-V characteristic of two TDs in series. Even though $V_{SN}$ is bistable for some $V_{DD}$ biases, the current is not. The current flow for $V_H$ and $V_L$ are equal to each other.

Fig. 6.11. $V_{SN}$ for two TD in series. The bistable region, or “eye”, decreases horizontally and vertically with increasing temperature.
6.4. Conclusion

The model developed in Chapter 5 was used in SIMUCAD’s Gateway SPICE circuit simulator to simulate three simple circuits; (i) a resistor and TD in series, (ii) an NFET and TD in series, and (iii) two TDs in series. These circuits were initially analyzed using Load Line analysis techniques, whose quantitative and qualitative results were compared with the simulated results. Each circuit simulated operated as predicted, for various biasing conditions, temperatures, and voltage sweeping directions. Each circuit exhibited bistability for certain ranges of bias conditions and temperatures. Some of these circuits will be used in more complex circuits, discussed in Chapter 7.

References for Chapter 6

CHAPTER 7

Simulation of Tunneling Analogue to Digital Converter, TSRAM cell, and Tunneling Logic Gates

This chapter discusses the simulation of (1) tunneling analog to digital converter (ADC) comparator, (2) tunneling SRAM (TSRAM) cell, and (3) logic gates using the model developed in Chapter 5. Advantages of TD augmented circuits will be discussed. As in the previous chapter, simulations were performed using SIMUCAD’s Gateway (version 2.6.4.R) circuit simulation suite.

7.1. ADC Comparator

ADC comparators are used to digitize analogue signals. Ideally, a sinusoidal input is transformed into a perfect square wave as the output, Fig. 7.1. The tripping voltage ($V_{\text{ref}}$) at which the output switches from high to low ($T_{\text{HL}}$) or low to high ($T_{\text{LH}}$) should be the same. The switch should occur instantaneously, with an infinite gain in the output. A typical ADC using traditional devices [1] utilizes twelve transistors and six Schottky diodes, Fig. 7.2a. However, the TD augmented comparator uses only one transistor and two TDs, Fig. 7.2b. Additionally, the TDs can be integrated directly on top of the source/drain regions of the MOSFET, saving a large amount of area.

A primary ADC comparator can be fed into the input of a secondary comparator in order further digitize the output signal, as seen in Fig. 7.2b. Simulations were performed for such an arrangement. The output of the primary ($V_{\text{out1}}$) and secondary ($V_{\text{out2}}$) comparators are measured for easy comparison. In the following simulations the secondary ADC used TDs of fixed areas equal to $\frac{1}{2}$ arbitrary units (AU) and 1 AU for the
load and drive TDs respectively. The primary drive TD used 1 AU, whereas the load was varied between (1) \( \frac{1}{2} \) AU, (2) 1 AU, and (3) 1.5 AU.

Fig. 7.1. Input (top) and output (bottom) of an ideal ADC comparator. \( V_{\text{trip}} \) corresponds to the input voltage at which the output switches from high to low \( (T_{\text{HL}}) \) or low to high \( (T_{\text{LH}}) \). The output is an ideal square wave.

Fig. 7.2. ADC comparator using (a) traditional devices [1], and (b) TDs. The traditional comparator uses 12 transistors and 6 Shotky diodes. Areas (in AU) are given as the subscripts of \( \frac{1}{2}, 1, \) and X.
Fig. 7.3. (a) $V_{out1}$ and (b) $V_{out2}$ for all three sizes of the primary load TD. (a) $V_{out1}$ exhibit many kinks, or relatively low gains. (b) $V_{out2}$ is more digitized for all cases. Notice that $V_{ref}$ increases as $X$ (area) increases.

The simulated output of $V_{out1}$ and $V_{out2}$ can be seen in Fig. 7.3a and Fig. 7.3b. The output versus input biases for the primary comparator, Fig. 7.3a, are not ideal. There are undesired kinks and bends. The secondary output is more ideal, with very sharp $T_{HL}$ and $T_{LH}$, Fig. 7.3b. However, a hysteresis effect occurs because $V_{ref}$ for $T_{HL}$ does not equal $V_{ref}$ for $T_{LH}$; this is an undesired characteristic, which can be minimized through design of the FET and TD I-V characteristics. The three different cases, with primary load TD areas of 0.5 AU, 1 AU, and 1.5 AU, have varying amounts of hysteresis ($X = 1.0$ AU being the smallest). Also note that $V_{ref}$ shifts to high biases as $X$ increases. This is an expected result [1] which may be used to design comparators for specific reference voltages.
Using a sinusoidal input for $V_{in}$, $V_{out1}$, and $V_{out2}$ were simulated, Fig. 7.4. $V_{out1}$ has many kinks, and a $V_{low}$ that is not flat (significant dependence on $V_{in}$). Also, $V_{low}$ increases with area ($X$), similarly to the increase in $V_{ref}$. $V_{out2}$ is almost a perfect square wave. $V_{high}$ and $V_{low}$ are the same values for all three areas. However, $V_{ref}$ shows the same dependence on area. A single ADC comparator works well for digitizing an analog signal; however, adding a secondary comparator improves the output substantially. Since one comparator is very small in device count and on chip footprint, adding a second comparator will still be much smaller than the traditional comparator, shown in Fig. 7.2.
7.2. **TSRAM cell**

The TSRAM cell consists of two TDs in series (See Chapter 6.3) with current source connected to the sense node ($V_{SN}$), Fig. 7.5a. During operation, $V_{DD}$ would be held constant, a memory state would be changed through current injection into $V_{SN}$, and the memory state would be read directly from $V_{SN}$. Injecting a large enough positive current causes $V_{SN}$ to go high ($V_H$), and injecting a large enough negative current causes $V_{SN}$ to go low ($V_L$). In these simulations, both the load and drive TDs are exactly the same. Therefore the current magnitude needed to latch ($I_{Latch}$) high or low is exactly the same.

Constant current sources are complex circuits, and therefore an NFET is more appropriate, Fig. 7.5b. This version of the TSRAM is very compact, using only one FET and two TDs, versus the six FETs needed for traditional SRAM cells. Recall that TDs may be integrated directly on top of MOSFET source/drain regions, therefore reducing the size of TSRAM cells to approximately 1/5 of SRAM cells. Additionally, the Gate and Source terminals may be used as the word line and bit line, respectively. This allows for addressing of individual cells within a memory array. However, using a constant current source allows for characterization of certain TSRAM parameters.

Using circuit in Fig. 7.5b, $V_{SN}$ versus $I_{in}$ was simulated at multiple temperatures and $V_{DD}$ biases, Fig. 7.7. Recall from Chapter 6.3, the bistability curve generated from two TDs in series, Fig. 7.6. Recall that the region bistability decrease, in height and width, as temperature increases. This is a result of the PVCR for the TDs decreasing, and $V_Y$ moving closer to $V_P$. Similar results were found for $V_{SN}$ versus $I_{in}$, Fig. 7.7.

The vertical lines in Fig. 7.6 indicate the $V_{DD}$ biases for the simulation results in Fig. 7.7 are found. At $V_{DD}$ equal to 0.18 V, Fig. 7.7a, the bistability is very narrow, with
little variation with respect to temperature. For a $V_{DD}$ of 0.3 V, Fig. 7.7b, the bistable region is very large. However its size is noticeably reduced with increasing temperature, but does not disappear. For $V_{DD}$ equal to 0.4 V, the bistable region is still large, but a little smaller over all. At the highest temperature (180°C), the bistability totally vanishes.

Fig. 7.5. TSRAM cell using a (a)current source or (b) NFET as the current injector. The NFET version is more practical for use in a memory array.

Fig. 7.6. Bistability curve of two TDs in series. The bistable region decreases in size with increasing temperature. Several vertical lines are provided for easy reference to the $V_{DD}$ values used in later simulations.
$I_{\text{Latch}}$ is the current at which $V_{SN}$ makes a large jump from low to high (write high) or high to low (write low). This is the minimum current needed for a write operation. Notice that for each case, the current need to latch high is equal to the magnitude needed to switch low. Therefore, an input current of 0 A is at the center of the bistable region. To write $V_H$ or $V_L$, a “+” or “-” $I_{\text{Latch}}$ current is injected into $V_{SN}$, respectively. When a bit is being stored in the TSRAM cell, no current is injected into the memory cell, and $V_{SN}$ will maintain its previous $V_H$ or $V_L$ state.

![Graphs showing $V_{SN}$ versus $I_{in}$ for different $V_{DD}$ biases.](image)

Fig. 7.7. $V_{SN}$ versus $I_{in}$. $V_{DD}$ biases of (a) 0.18 V, (b) 0.3 V, and (c) 0.4 V. Increasing temperature decreases the region of bistability. There exists a $V_{DD}$ that results in a maximum bistable region for a particular temperature.
Using the $I_{\text{Latch}}$ values obtained from the simulation curves in Fig. 7.7, and those not shown here, $I_{\text{Latch}}$ versus $V_{DD}$ curves can be extracted, Fig. 7.8. The dashed curves are quadratic fits to the simulated data points. For $V_{DD}$ biases that do not exhibit bistability, $I_{\text{Latch}}$ is given a value of 0 A. Notice that the initial rise in $I_{\text{Latch}}$ starts at approximately 0.18 V for all temperatures. However, the high end $I_{\text{Latch}}$ cutoff decreases with increasing temperature, agreeing with Fig. 7.6 and Fig. 7.7. For each temperature there is a $V_{DD}$ that results in a maximum $I_{\text{Latch}}$. This maximum $I_{\text{Latch}}$ value decreases and shifts to smaller biases with increasing temperature.

![Graph showing $I_{\text{Latch}}$ versus $V_{DD}$ for different temperatures.](image)

**Fig. 7.8.** The $I_{\text{Latch}}$ current needed to latch to $V_H$ or $V_L$. The dashed lines are quadratic fits. Simulated data points are designated by symbols.

The maximum $I_{\text{Latch}}$ versus temperature, Fig. 7.9 (right axis), follows a quadratic. However, the corresponding $V_{DD}$ follows a linear relationship with temperature, Fig. 7.9 (Left axis). A $V_{DD}$ of 0.3 V was chosen for a temperature of 100°C, a common high end operating temperature. The chosen $V_{DD}$ was used the following simulations, where the current source is an NFET, Fig. 7.5b.
Fig. 7.9. The maximum $I_{\text{Latch}}$ (right axis) and $V_{\text{DD}}$ (left axis) versus temperature. $I_{\text{Latch}}$ data points were fitted with a quadratic. $V_{\text{DD}}$ was fitted with a line.

Fig. 7.10. The maximum $I_{\text{Latch}}$ (right axis) and $V_{\text{DD}}$ (left axis) versus temperature. $I_{\text{Latch}}$ data points were fitted with a quadratic. $V_{\text{DD}}$ was fitted with a line.

Holding the word line ($V_{\text{Word}}$) at 1.75 V, $V_{\text{DD}}$ at 0.3 V, and sweeping the bit line (Fig. 7.10) results in a curve similar to that shown in Fig. 7.7b. For temperatures rising up to 100°C (the optimum temperature for the $V_{\text{DD}}$ used), the bistability increases in
width a small amount. Temperatures increasing past 100°C result in larger decreases in the bistability region.

![Timing diagram of TSRAM using an NFET](image)

**Fig. 7.11.** The maximum $I_{\text{Latch}}$ (right axis) and $V_{DD}$ (left axis) versus temperature. $I_{\text{Latch}}$ data points were fitted with a quadratic. $V_{DD}$ was fitted with a line.

A timing diagram of the TSRAM using an NFET can be seen in Fig. 7.11. When the TSRAM cell is being written to, 1.5 V is applied to the wordline (the gate of the NFET). To write a $V_L$ the bit line is held low, and to write $V_H$ the bit line is brought to a high bias (0.3 V in this case). During storage or read periods, the word line is kept low, thereby turning the NFET off, preventing any current injection. Notice that as temperature increases $V_H$ decreases, and $V_L$ increases. Further simulations and analysis can be performed using the TD model discussed in Chapter 5, which does not include capacitance, inductance, or frequency response. Basic analysis of the TSRAM operation has been reported elsewhere [2-5].
7.3. Basic Logic Gates

Four different basic logic gates were simulated; (1) OR, (2) NOR, (3) AND, and (4) NAND. All circuits used two NFETs connected in series or parallel, and two serially connected TDs. The load TD would have an area of 1 AU or 0.5 AU, whereas the drive TD would be 0.5 AU or 1 AU. This would cause $V_{SN}$ to automatically latch high or low without any current injection into $V_{SN}$. For example, when the load TD is 0.5 AU and the drive TD is 1 AU, $V_{SN}$ will latch low as shown in the load line analysis in Fig. 7.12. Once a large enough positive current is injected into the center node, $V_{SN}$ will latch high. To latch low again, the input simply needs to be removed. It is important that the large to small area ratio of the TDs is greater than the PVCR of the TD’s I-V characteristics.

![Load line analysis of two TDs in series](image)

**Fig. 7.12.** Load line analysis of two TDs in series, where the load is 0.4 AU, and the drive is 1 AU. $V_{SN}$ (the intersection of the two curves) latches low until a large enough positive current is injected into $V_{SN}$.

When the load TD has an area of 1 AU, and the drive TD has an area of 0.5 AU, $V_{SN}$ will normally latch high. A large enough negative current injection will latch $V_{SN}$ to...
a low value. This case is the same as that shown in Fig. 7.12, mirrored around a vertical line at $V_{in} = 0.175 \text{ V}$.

![Circuit Schematics](image)

Fig. 7.13. Circuit schematics of (a) OR gate, (b) NOR gate, (c) AND gate, and (d) NAND gate. All circuits use only two NFETs and two TDs.

The four logic gate circuit schematics can be seen in Fig. 7.13. The substrate or body contacts (not shown in the figures) are connected to ground. Therefore, a high bias on the NFET gates will cause the transistor to turn on. In Fig. 7.13, logic gates in the same column have the load and drive TD areas, and the NFETs are connected to power (column 1) or ground (column 2). Rows use the same NFET configuration of parallel (row 1) or series (row 2). In this fashion, the circuit configurations follow a simple order.
that is in part similar to traditional CMOS logic gates. A simple set of rules may in the future be used to develop more complicated circuits without the need to always use basic logic gates. However, that is beyond the scope of this thesis.

![Timing diagram of the four basic logic gates](image)

**Fig. 7.14.** Timing diagram of the four basic logic gates (a) OR, (b) NOR, (c) AND, and (d) NAND. The output of each gate is correct, and drives nearly to full rails of $V_{dd}$ (0.3 V).

The voltage transfer characteristics ($V_{SN}$ vs. $V_{in}$), Fig. 7.15, all show a hysteresis of varying sizes. Only input “A” was swept in forward and reverse biases. Input “B”
was held constant at low for OR and NOR gates, and high for the AND and NAND gates. 
$V_{SN}$ drives nearly to full high rail (0.3 V) for the NOR and NAND gate, and pretty close 
to full low rail. The OR and AND gate drives to full low rail (0 V); however, when high, 
there is a significant dependence on $V_A$. These circuits were not optimized for 
performance.

![Graphs of voltage transfer characteristics](image)

Fig. 7.15. Voltage transfer characteristics of (a) OR gate, (b) NOR gate, (c) AND gate, 
(d) NAND gate.
7.4. Conclusion

The model developed in Chapter 5, and knowledge gained from the simulation of the simple circuits discussed in Chapter 6 was used to simulate (i) ADC comparators, (ii) TSRAM cell, and (iii) four basic logic gates. The TD-augmented ADC comparator successfully digitized sinusoidal inputs. The simulations performed show the viability of TD augmented comparators, which use 1/6 the transistors and 2/3 as many diodes, resulting in a large space savings on chip.

The TSRAM simulations agreed with prediction, and indicate that such memory cells can operate well above room temperature. Simulations and work by Sudirgo, et al. [3-5], indicate the viability of implementing TSRAM cells on chip. TSRAM can save upwards of 80% on chip area, with vertical integration of the TDs directly on top of MOSFET S/D regions.

Simulations of basic logic gates – (i) OR, (ii) NOR, (iii) AND, and (iv) NAND – showed correct logic. Output voltages do not get high enough to drive the NFET transistors used in the simulations. Therefore, chains of logic gates cannot be simulated as is. More advanced transistor models may be employed in the future to investigate this issue further.

References for Chapter 7


CHAPTER 8

Conclusion

Recently, N-on-P Si/SiGe RITDs have been integrated with NMOS transistors [1-6]. That study shows the viability of TD-augmented circuits. Large increases in space savings can be achieved with the integration of P-on-N RITDs, which has only had limited development in the past [7]. This thesis looked at the effect of $i$-layer composition and P $\delta$-doping concentration. SiGe/Si thicknesses were varied from (i) 2 nm/4 nm, (ii) 3 nm/3 nm, and (iii) 4 nm/2 nm. The effect of $i$-layer composition on PVCR and $J_P$ indicates that maximizing both SiGe and Si thicknesses to 3 nm each is the best configuration. A maximum PVCR of 1.06 was achieved, which is well below a targeted PVCR of 2.0.

For the second experiment, P $\delta$-doping concentrations of (i) $1.00 \times 10^{14}$ cm$^{-3}$, (ii) $1.25 \times 10^{14}$ cm$^{-3}$, (iii) $1.50 \times 10^{14}$ cm$^{-3}$, were used. The SiGe/Si $i$-layer thicknesses were held constant at 4 nm/4 nm. The PVCR increased substantially with increases in the $\delta$-doping concentration. A concentration of $1.5 \times 10^{14}$ cm$^{-3}$ resulted in a maximum PVCR of 1.33. Further development and study could improve RITD significantly improve characteristics, and become suitable for TD-augmented circuits.

There has been large success with N-on-P Si/SiGe RITDs [8,9]. However, the SiGe layer drastically reduces the thermal stability of the TD, and complicates the device growth. Therefore RITDs that are only comprised of Si were also developed. The Si RITD structure is the same as the optimal Si/SiGe developed by Jin, et al. [9], except that all SiGe layer were grown as Si. P $\delta$-doping concentrations of $0.75 \times 10^{14}$ cm$^{-3}$ (TD1) and
1.00×10^{14} \text{ cm}^3 \text{ (TD2) were used. Previous studies have shown that the optimal anneal temperature is 575^0\text{C}. Increasing the anneal time to 10 min. resulted in maximum } J_P \text{ and PVCR values for TD1 and TD2 are 1.62 kA/cm}^2, 2.91 \text{ kA/cm}^2, 2.48, \text{ and 2.57, respectively. The largest portion of PVCR increase occurred in the first 5 minutes of annealing time. These devices have characteristics that are well above the requirements needed for TD-augmented circuits.}

CMOS circuits often operate at temperatures up to 100^0\text{C}, or even higher. It is therefore important to understand the effects of these elevated temperatures on TD characteristics. The IV characteristics of Si/SiGe RITDs and proximity diffused Si ETDs were measured at multiple temperatures from room temperatures up to 200^0\text{C}. The current density of the TDs increased with temperatures. However, } J_V \text{ increased more rapidly than } J_P, \text{ resulting in an over-all decrease in PVCR with increasing temperature. The PVCR for the RITD device decreased at a slower rate than for the ETD devices.}

To compare the rate in change of } J_P, \text{ a plot of } J_P \text{ normalized over } J_P(@ \text{ room temperature}) \text{ versus temperature was made. A similar plot was done for } J_V. \text{ It was found that } J_P \text{ increased with temperature at the same rate for all devices looked at. However, } J_V \text{ increased at a faster rate for the ETD devices, than for the RITD devices. The rate of change for both } J_P \text{ and } J_V \text{ is well-behaved, and exponential in nature. These results agree with the PVCR observations previously discussed.}

The temperature results obtained were used to develop a SPICE compatible model that can be used to analyze the operation of TD-augmented circuits. Initially, piece-wise, physics-based, and trigonometric empirical models were investigated. The trigonometry-based model developed by Yan, et al. [11], provided an over-all good fit. However, the
model was poor in reverse bias, and close to a bias of 0 V. Additionally, the function could lead to discontinuities and kinks in the slope. The model discussed by S. M. Sze, [10] was then looked into. This model is perfectly smooth, and simpler. However, it overestimates the magnitude of current over the entire bias range.

To overcome the deficiencies of the above models, the Sze model was modified to fit with measured results. Modifications include; (i) removal of diffusion current term, (ii) addition of current limiting denominators, (iii) simple modifications to the values used in place of \( J_P \) and \( J_V \). With the modifications made, very high accuracy fits were made with proximity diffused ETDs.

The model was further modified to include temperature effects. To achieve this, the model was fit to the I-V characteristics at multiple temperatures. Then, fits to the model constants, including \( J_P \) and \( J_V \), versus temperature were made. Each time the temperature is changed, the model calculates new model coefficients and \( J_P \) and \( J_V \), which are then used in the model to calculate the appropriate I-V characteristic. The latest version of the model fits the proximity diffused ETD device at temperatures ranging from room temperature (23\(^0\)C) up to 200\(^0\)C. Key parameters extracted from the output of the model were within 7\% of measured values. Furthermore, the parameters were usually within 5\%.

The model developed was then implemented into SIMUCAD’s Gateway (version 2.6.4.R) circuit simulation suite. Initially, three simple circuits were simulated; (i) a resistor and TD in series, (ii) an NFET and TD in series, and (iii) two TDs in series. The circuits were first analyzed using load line analysis techniques. The qualitative and
quantitative results obtained were used to verify the simulated results for accuracy. Each circuit simulated behaved as expected for various biasing conditions and temperatures.

Each circuit exhibited regions of bistability. Bistability can be used to simplify traditional CMOS circuits including ADC comparators, digital logic circuits, and memory cells. Bistability is highly dependent on biasing conditions, temperature, resistance, NFET characteristics, and TD characteristics. In general, the region of bistability decreases with increasing temperature. In other words, the performance of these simple circuits degrades measurably with increasing temperature. Over-all, the two TDs in series exhibited the best bistability characteristics, followed by the NFET in series with a TD.

The knowledge gained from the simple circuits was used to simulate complex circuits augmented with TDs: (i) ADC comparators, (ii) TSRAM cell, and (iii) basic logic gates. The ADC comparator uses the information learned from an NFET in series with a TD. A single comparator does digitize an analogue signal, but the output is not very ideal. Connecting a second comparator to the output of the first causes the output to form into a nearly perfect rectangular waveform. Changing the effective area, and therefore the current magnitude of each TD significantly affects $V_{\text{trip}}$ of the comparator.

Knowledge gained from simulating two TDs in series was used for the TSRAM simulations. Bistability is critical for proper operation of the TSRAM cell. $V_{DD}$, $I_{\text{inj}}$, and temperature sweeps shows how the bistability region changes. There is an optimum $V_{DD}$ for each temperature where $V_H - V_L$ and $I_{\text{Latch}}$ are maximized. Correctly operating TSRAM cells were simulated at multiple temperatures. The memory cell was written to when the wordline with high, and the logic state was stored when the wordline was low.

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A $V_{DD}$ of 0.3 V was used, which is the optimum bias for a temperature of 140°C. However, it is important to note that, $V_H - V_L$ consistently decreases with increasing temperature.

Finally, (i) OR, (ii) NOR, (iii) AND, and (iv) NAND gates were simulated. Each logic gate gave the correct output. The swing in $V_{out}$ is not large enough to drive other logic gates. This limits the current usefulness of the logic gates designed. However, further optimization of the gates, and the use of more advanced deep sub-micron NFET gate models would improve the voltage swing of $V_{out}$.

Each complex circuit simulated uses far less devices than their traditional CMOS counterparts. The TD-augmented comparator used only one NMOS and two TDs, whereas traditionally twelve FETs and six Schottky diodes are used. The TSRAM uses two TDs and one NMOS, instead of six MOSFETs. All of the logic gates used various arrangements of two TDs and two NMOS, instead of four MOSFETs. Also, recall that TDs may be integrated on top of the S/D regions of MOSFETs, dramatically decreasing on-chip footprint.

8.1. Further Development and Application of Work Completed

Further development of the P-on-N Si/SiGe RITDs can lead to P-on-N Si RITDs. Integrating these devices on top of NMOS transistors would be a huge advancement towards TD-augmented circuits. Such technology could be used to greatly reduce on-chip footprint of various circuits, simplify the layout of those circuits, and lead to reduced power consumption and high operating frequencies.
Improvements on the model developed can be made to remove limitations on $V_p$. Additionally, adding inductance and capacitance components could lead to simulation of high frequency effects. This would further verify the usefulness of TD-augmented circuits. Such a model would allow circuit designers to completely design and simulate TD-augmented circuits. This is necessary in order to fabricate TD-augmented circuits for commercial products.

The developed model can additionally be adopted for use on advanced CMOS transistors. Doping concentrations for S/D and body regions are approaching degenerate levels of doping [12]. In other words, S/D junctions are looking more and more like backward diodes. Eventually, they may look like ETDs. It is therefore very important for circuit designers, and SPICE models to account for this behavior. The model developed here, along with the enhancements mentioned above, could be adjusted and implemented into the MOSFET models.

References for Chapter 8


