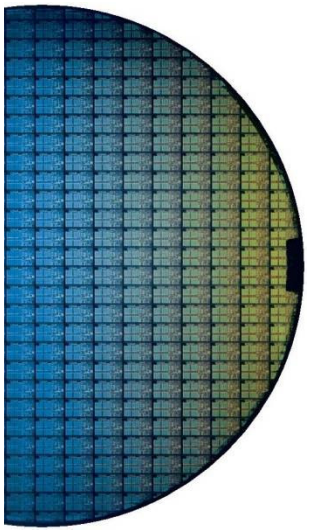

Design and Simulation of Dual channel MOSFET's

A performance evaluation for Strained Si/Strained SiGe channel

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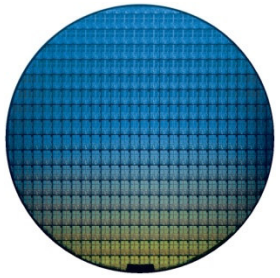
Master's Thesis Defense

Puneet Goyal [a]

Research Advisor : Dr James E. Moon [a]

[a] Department of Electrical Engineering,
Rochester Institute of Technology, NY



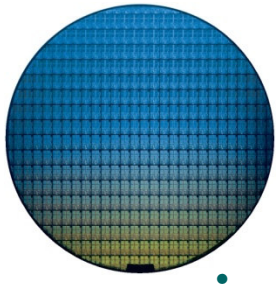
Key Messages

- Process induced strain is the most significant innovation in submicron MOS transistor technology , but scalability is a major bottleneck in driving performance for sub 65 nm technologies.

- Compound semiconductor material such as SiGe a promising solution for foreseeable future of MOS transistor technology.

- Dual channel CMOS transistor technology with a biaxial tensile strained Si and biaxial compressive strained SiGe channel is a promising solution to sustain the scaling challenges.

- Challenges with SiGe devices: leakage issues, surface roughness and cross hatching, higher cost and process complexivity with substrate development.



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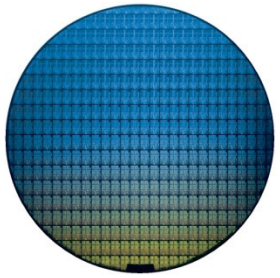
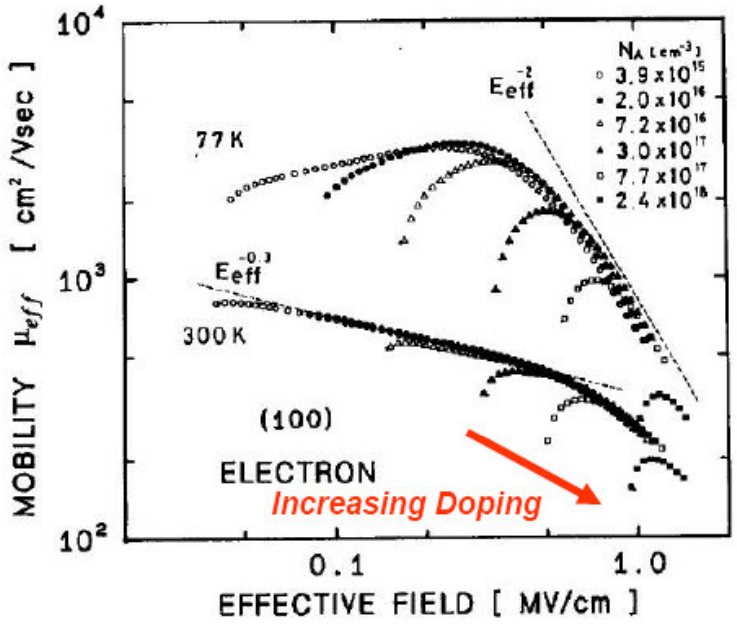


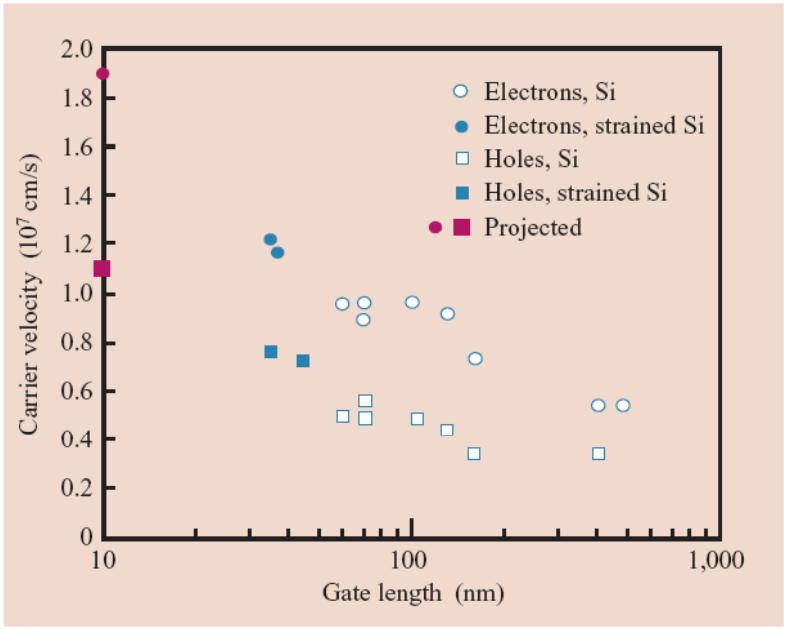
Objective

- To design, optimize and evaluate the performance of strain Si/Strain SiGe dual channel heterostructure MOS transistor for sub 65 nm technology.

- Formulation of unified modeling scheme based on different physics-based model in order to design, simulate and predict device behavior.

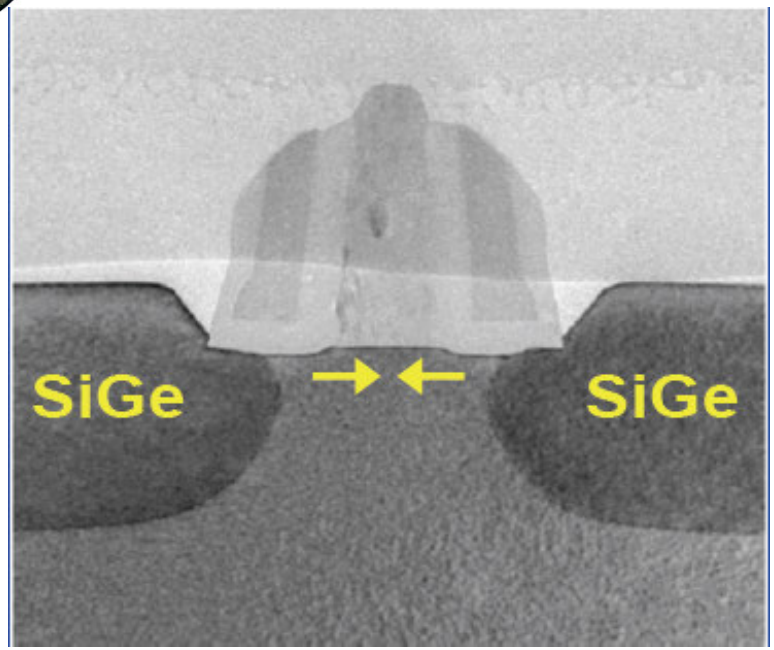
Scaling Trends and Challenges

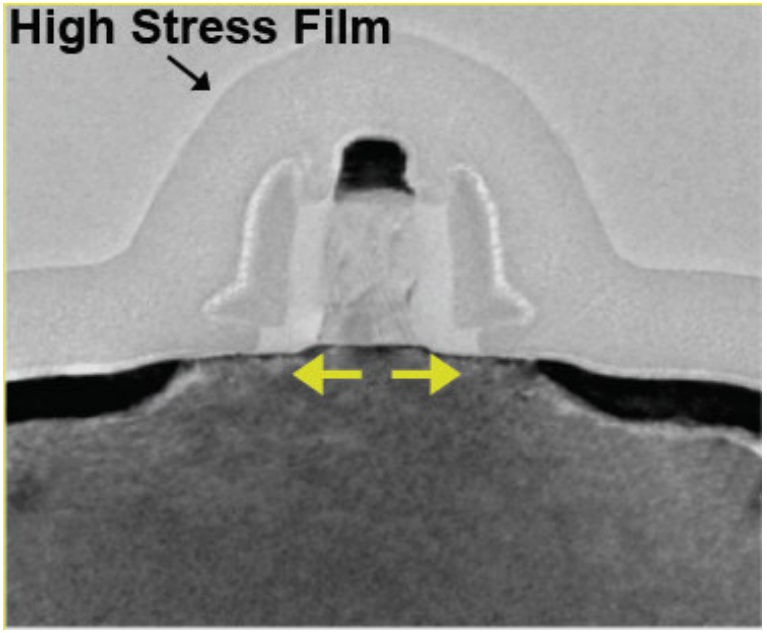




- Scaling enables more transistor and increased performance.
- Challenges with Scaling
  - SCE becomes more and more dominant coupled with increase scattering, and leakage.
  - Approaching fundamental, scientific and engineering limits with conventional CMOS

Strain as a Solution

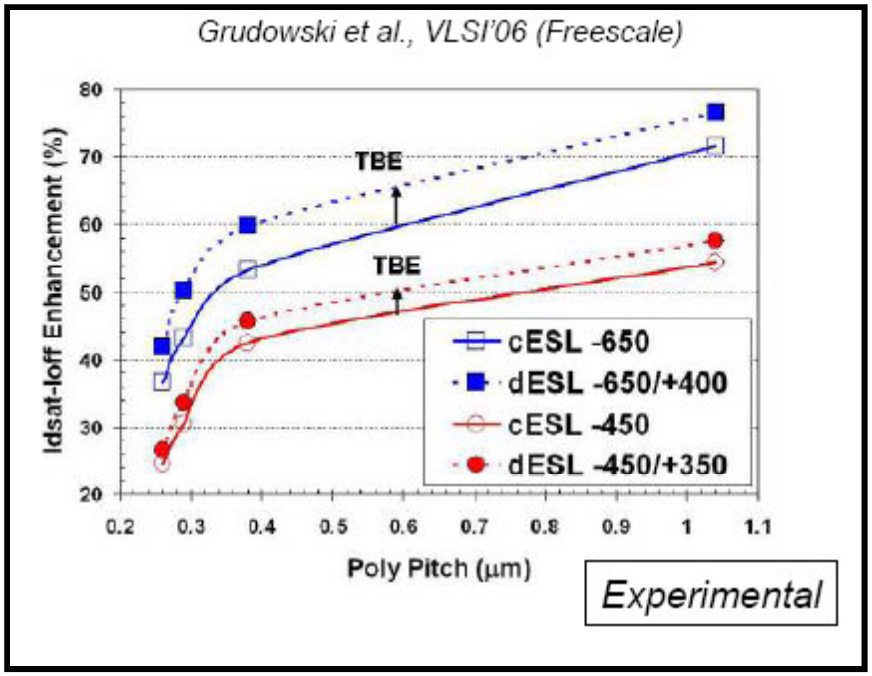


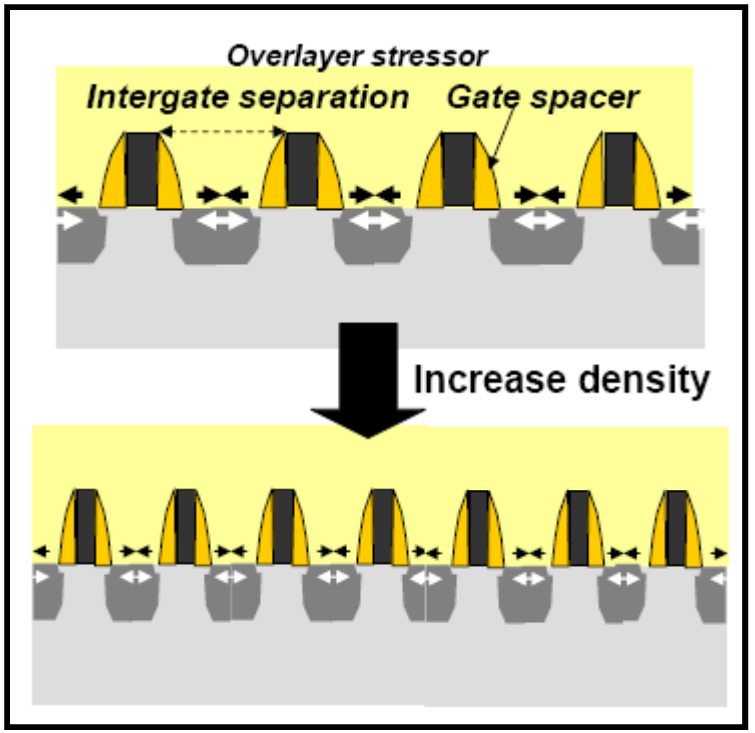


- Strain in Si as a performance booster.
- High electron and hole mobility , more performance per watt.
- Next generation strain : SMT, SPT, strain with hybrid orientation technique, SSOI, e-SiC

Ref : Jan *et al. IEDM Tech* , Oct 2005, Courtesy (Intel Corp)

Performance Vs Scalability of Strain Silicon

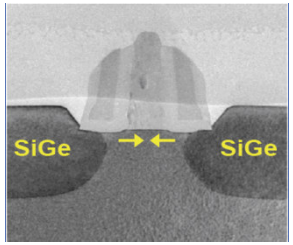




- Density hurts strain, resulting in low and saturated performance.
- Source/Drain proximity issues, higher defect densities, process integration challenges and higher manufacturing cost with scaling.

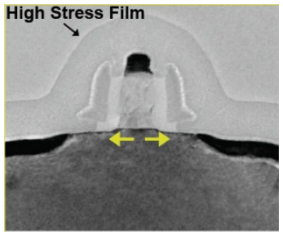
Courtesy : Semiconductor International : Ref Aaron Thean Freescale, Strain Si Update , March 07

Innovation Enable Technology Pipeline as a solution to Scaling

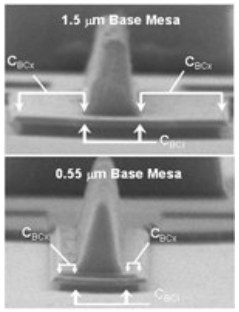


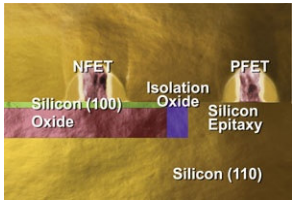
90 nm

Process Induced Strain stress liners (tESL/dESL)+ e-SiGe



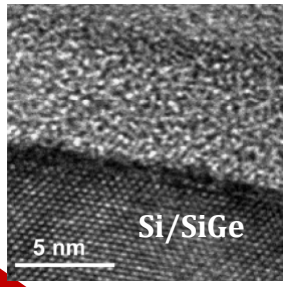
Process + Substrate Induced Stress (SPT, HOT)

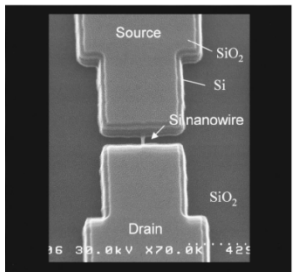




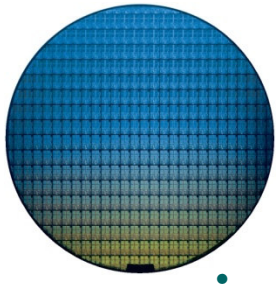
65 nm beyond

New Material SiGe , III-V's, SiC, CNT





- **New channel material such as SiGe and hetero-structure devices as potential candidate for sub -65 nm technology.**



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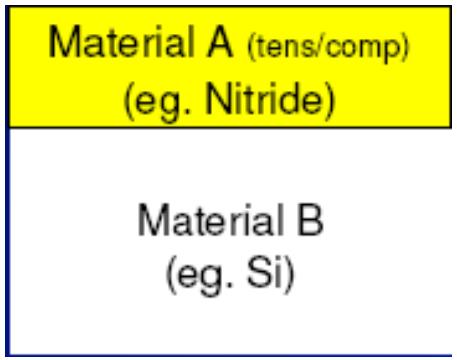
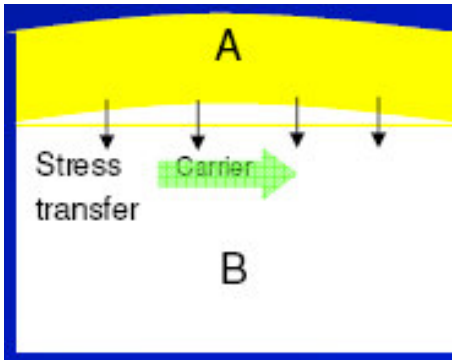
Mechanics of Strain



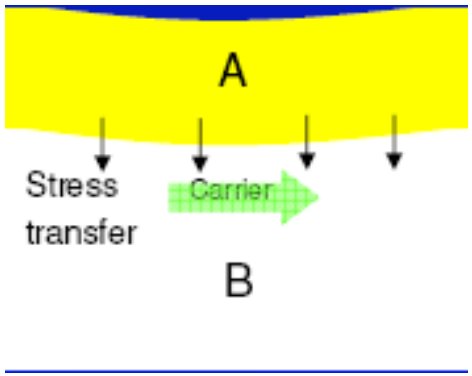
Due to material mismatch of A & B, arising from material composition, lattice size, different thermal expansion rate.
A will introduce mechanical stress on B



Strain in Silicon

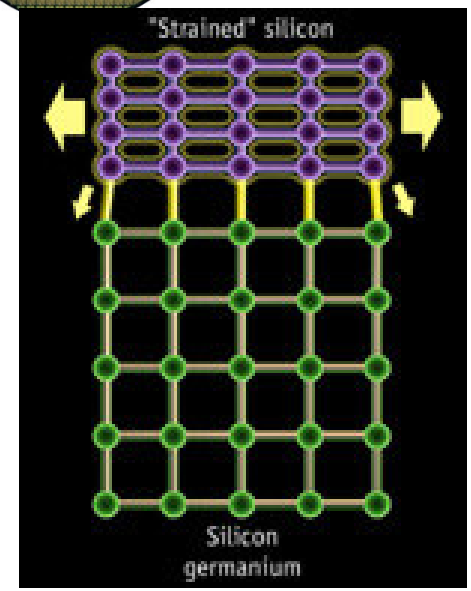
Strain (ε) =($a_{silicon*}$ - $a_{silicon}$)/ $a_{silicon}$

- If $a_{silicon*} > a_{silicon}$, Tensile Strain.
- If $a_{silicon*} < a_{silicon}$, Compressive Strain

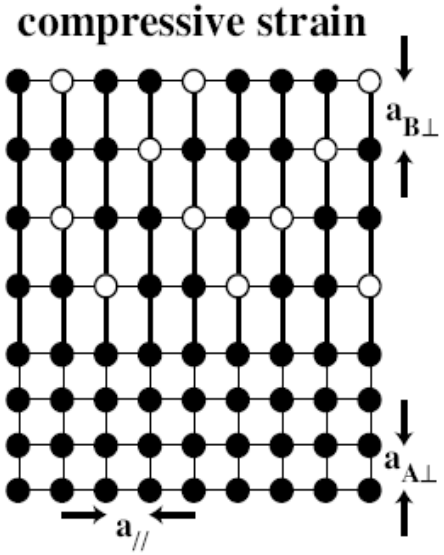


Ref : Victor Chan IBM SRDC, Hope well Junction , Jan 2007

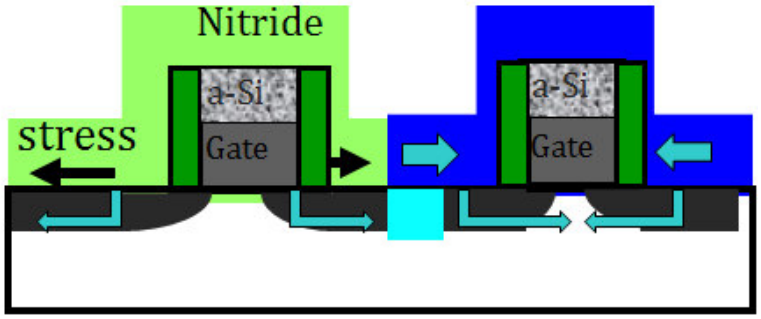
Stress Induction



$a_{silicon} < a_{SiGe}$
Biaxial Tensile Stress



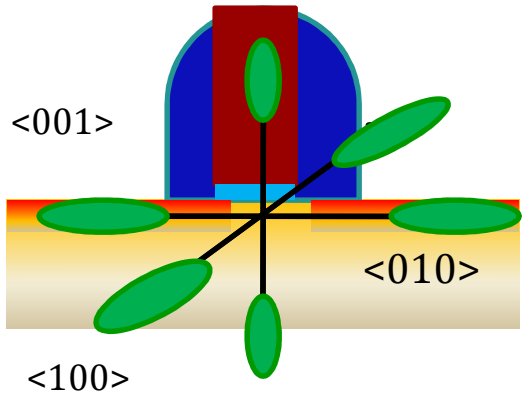
$a_{SiGe(y)} < a_{Si/SiGe(x)}$
Biaxial Compressive Stress

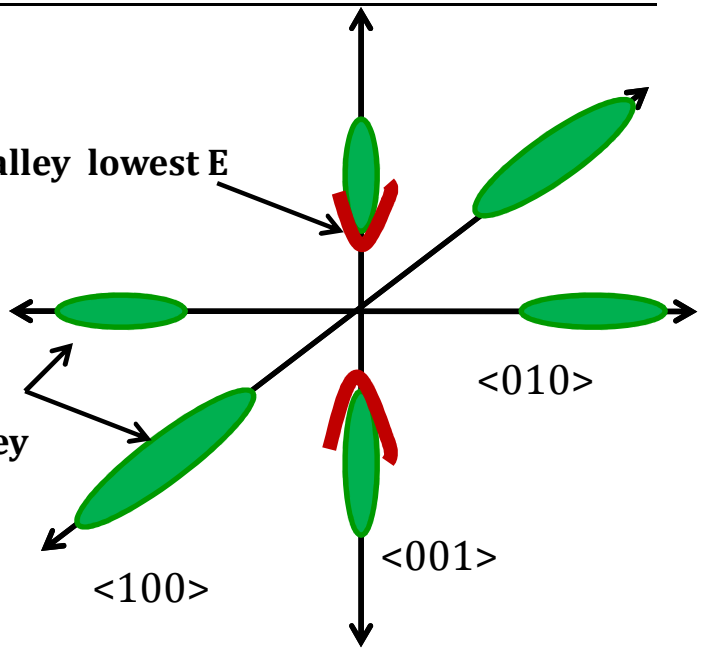


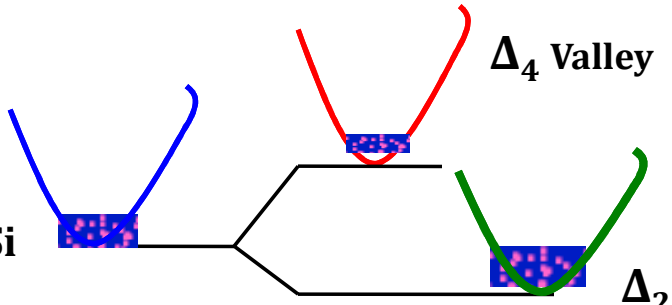
dual etch stop Stress Liner – Process Induced Strain

- Substrate Induced Strain – strain in *x-y* plane.
  - Biaxial Tensile Stress – Tensile component in *x-y* plane and compressive stress in z plane
  - Biaxial Compressive Stress – Compressive Stress in *x-y* plane and tensile stress in z plane.
- Uniaxial Process Induced Strain – Strain in *x* plane.
  - Common stress configuration – e-SiGe, Stress Liners and SMT

Electron Mobility in Strained Silicon

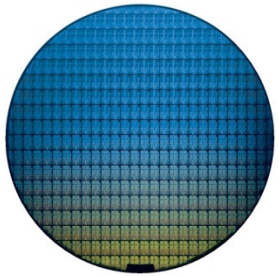




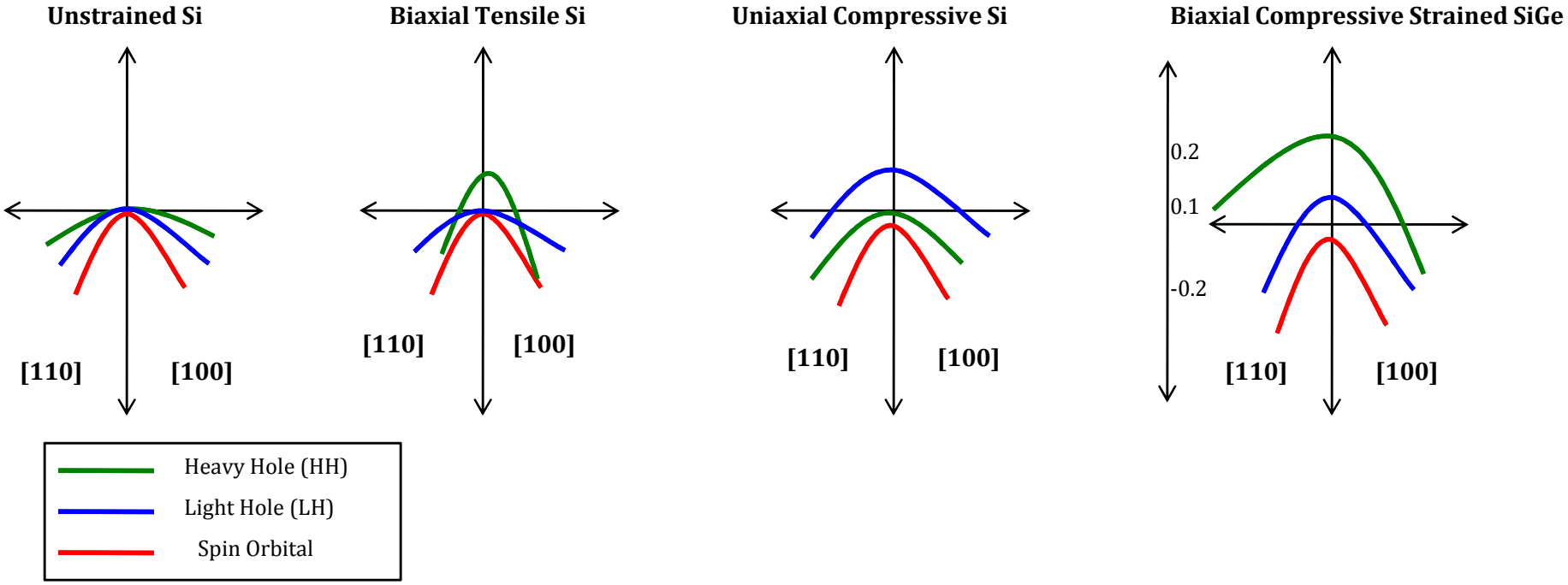


$\mu = e\tau / m^*$

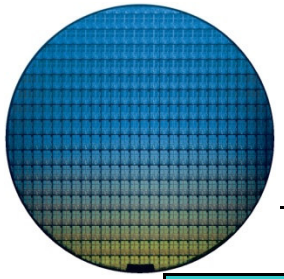
- Strain splits the conduction valley into four in-plane conduction Δ_4 valleys and two out-of plane conduction Δ_2 valleys (lower energy).
- Preferential population of electron in Δ_2 valleys . Lower effective mass, high mobility



Hole Mobility

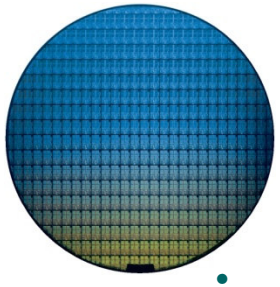


- Strain causes mixing of bands thus making HH and LH degenerate.
- Degeneracy cause band wrapping and repopulation of holes in top-most layer, thus increasing hole mobility.
- $\mu_{H\ unstrained} < \mu_{H\ biaxial\ tensile} < \mu_{H\ uniaxial\ compressive} < \mu_{H\ biaxial\ compressive}$



Strain Comparison

Strain	NMOS	PMOS	Scalability and Performance
Biaxial Tensile	☺	☹	Scalable, high performance for NMOS High process cost, process challenges – defect free epi layers
Biaxial Compressive	☹	☺	Scalable , high performance for PMOS, High process cost, process challenges – defect free epi layer
Uniaxial Compressive	☹	☺	Scalability Issues with all configuration except e-SiGe, high performance, process challenges with scalability , high cost , and defect free epi S/D .
Uniaxial Tensile	☺	☹	Scalability Issues with all configuration, high performance, process challenges with scalability , high cost.



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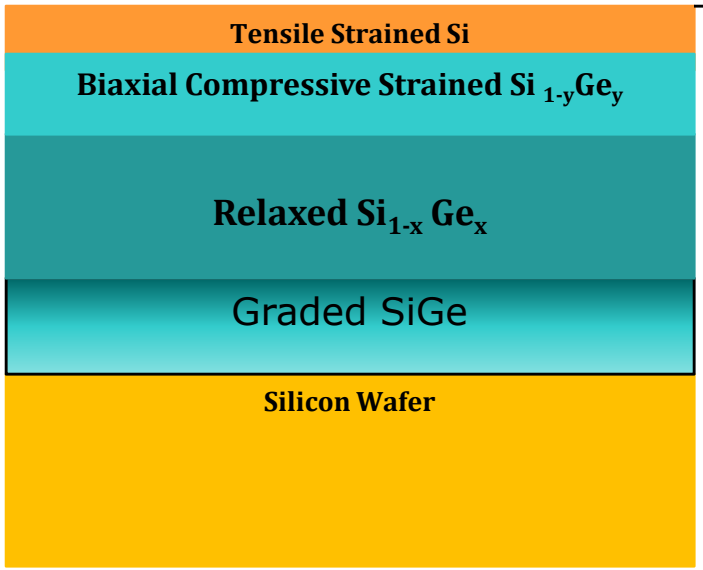
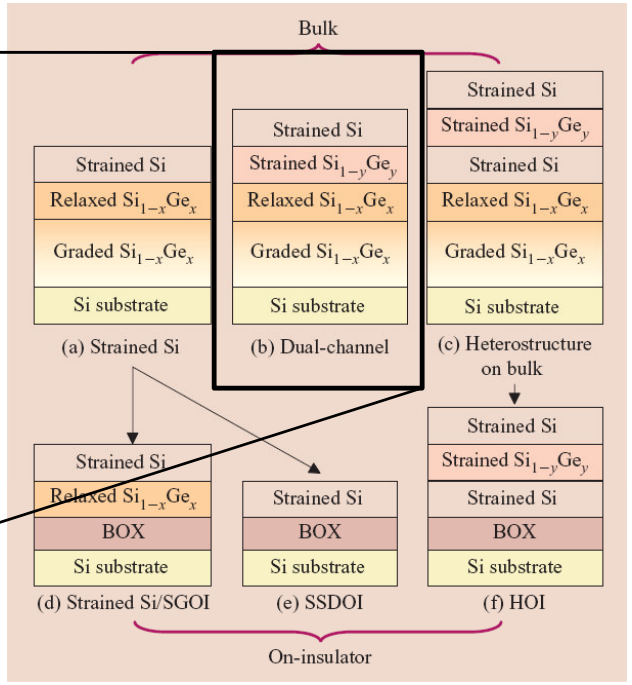
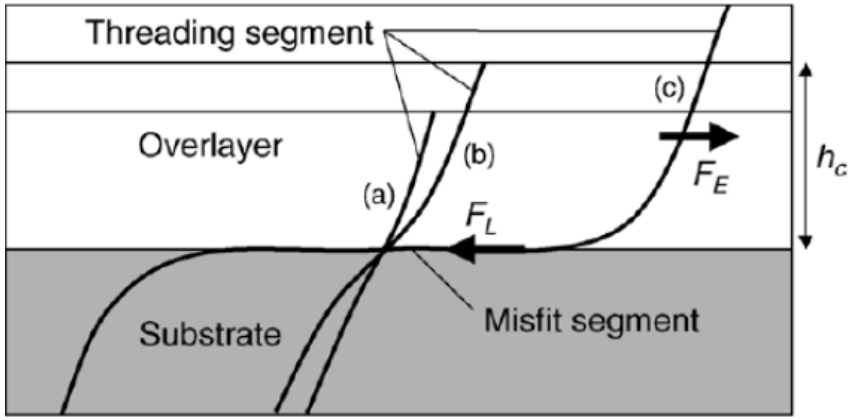
Dual Channel (DCH) Architecture





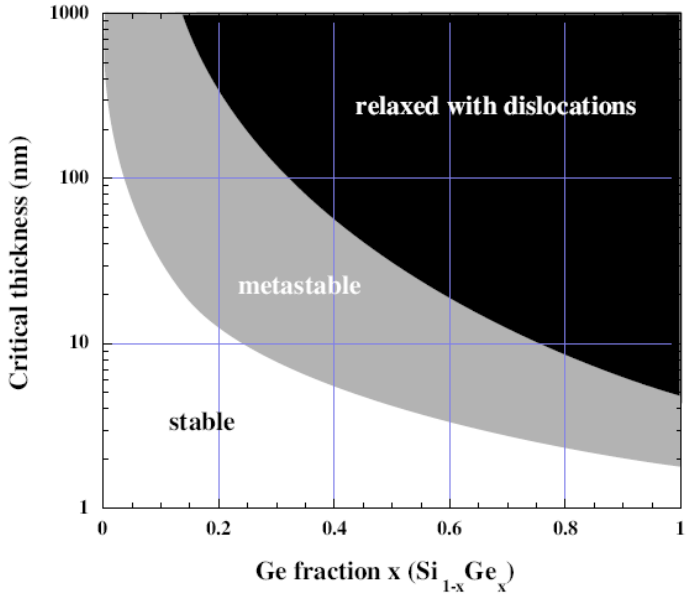
- Dual channel MOS comprises of tensile strained Si/compressively strained SiGe *pseudomorphically* grown on virtual substrate.
- For PMOS , both Si and SiGe (strained) acts as channel layers.
- For NMOS, channel remains confined to Strain Silicon layer.

Critical Thickness & Strain Relaxation



Strain Relaxation and critical thickness based on Matthew & Blakslee[1]

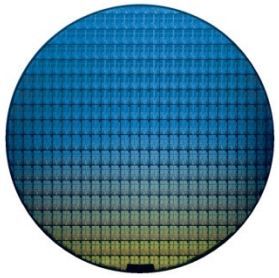
$$h_c = \frac{b(1-\nu\cos^2\alpha)}{8\pi(1+\nu)f\cos\theta}\left[1+\ln\left(\frac{h_c}{b}\right)\right]$$



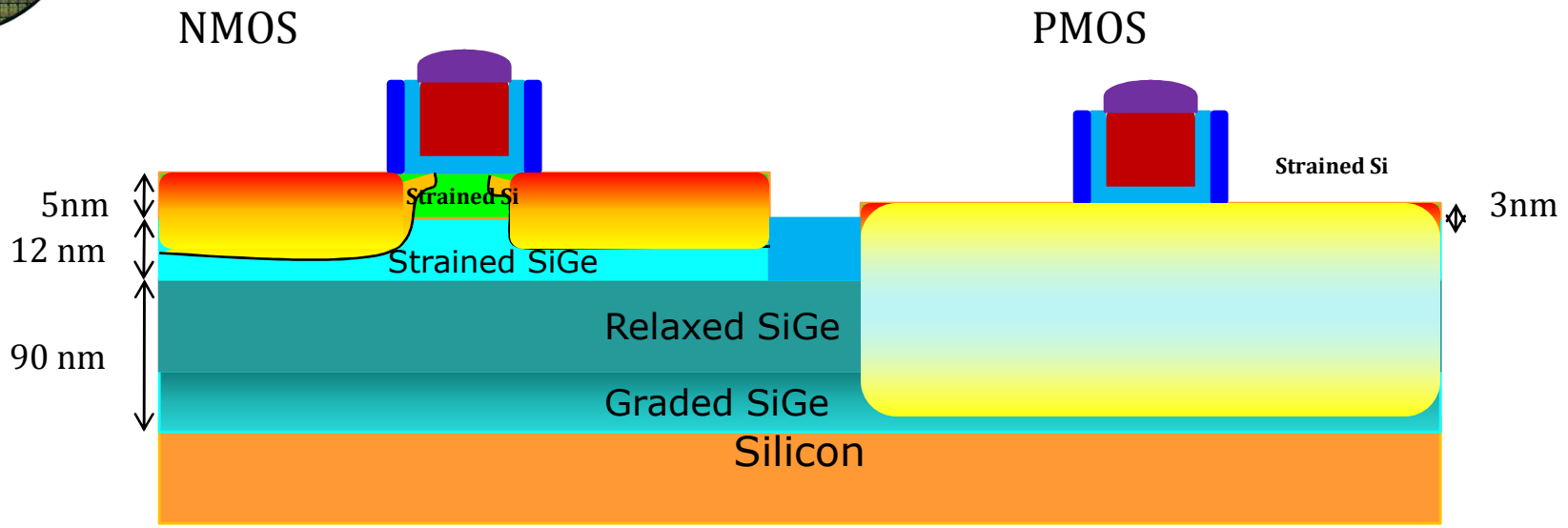
Critical thickness as variance of Ge mole fraction for growth at 550C [2]

- Critical Thickness defined as minimum value of the film thickness, above which the strain in the film relaxes due to misfit dislocation, elastic and plastic deformation and half loop nucleation.
- Approaches to reduce defect :
  - LPCVD
  - Graded Buffer
  - Wafer Bonding

[1]Yasuhiro Shiraki *et al.*, Surface Science Report , 2006
[2] Douglas J Paul. Review Article, *Semicond Science Tech*. University of Cambridge UK

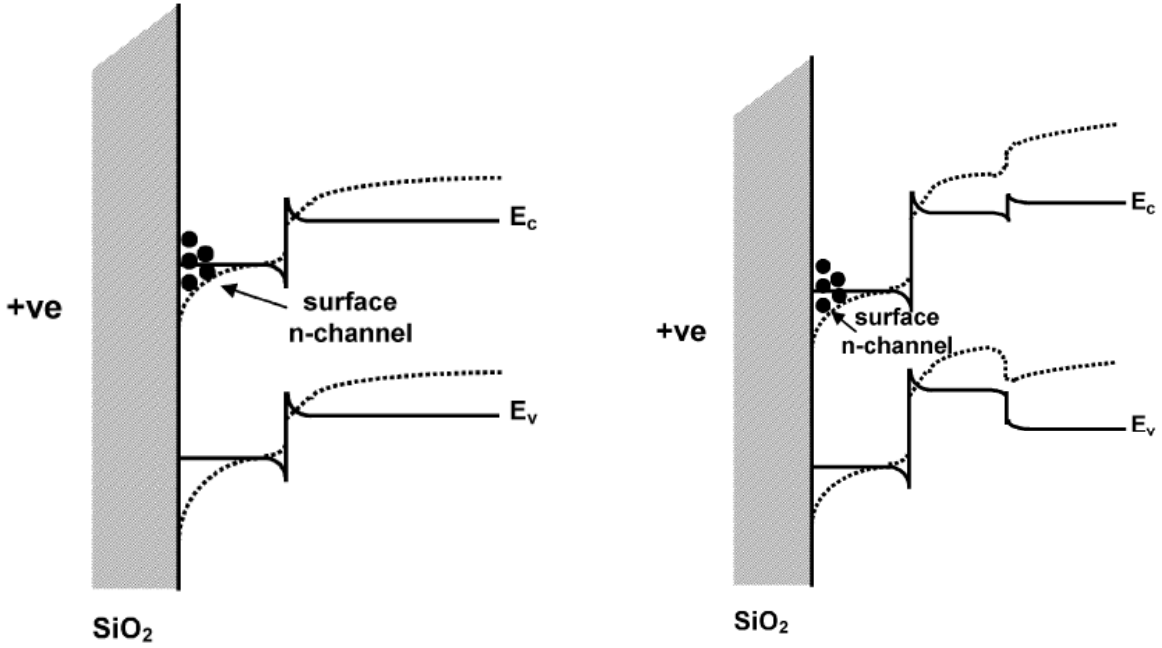


CMOS Integration of DCH MOS



- Different strained silicon cap layer for NMOS and PMOS.
- Size of NMOS strain Si cap layer ≥ 5 nm.
- Size of PMOS strain Si cap layer < 3 nm.
- The virtual substrate thickness is optimized to 90 nm (20 nm + 70 nm).

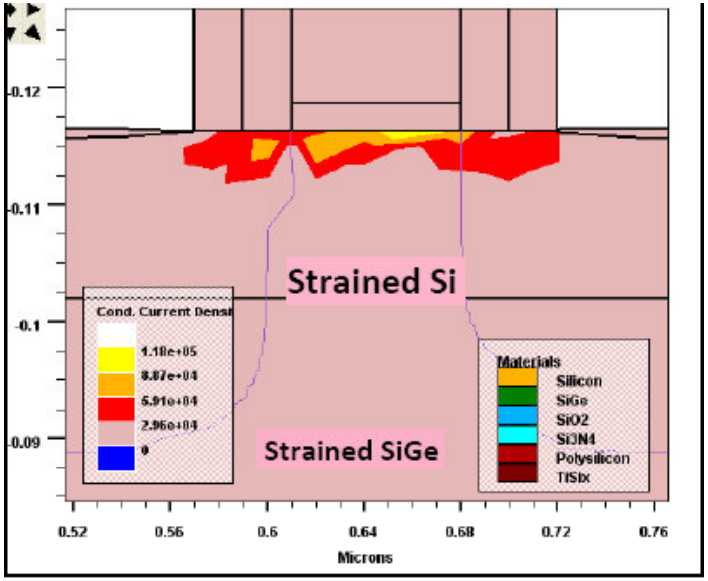
Device Theory – Band Diagram , NMOS



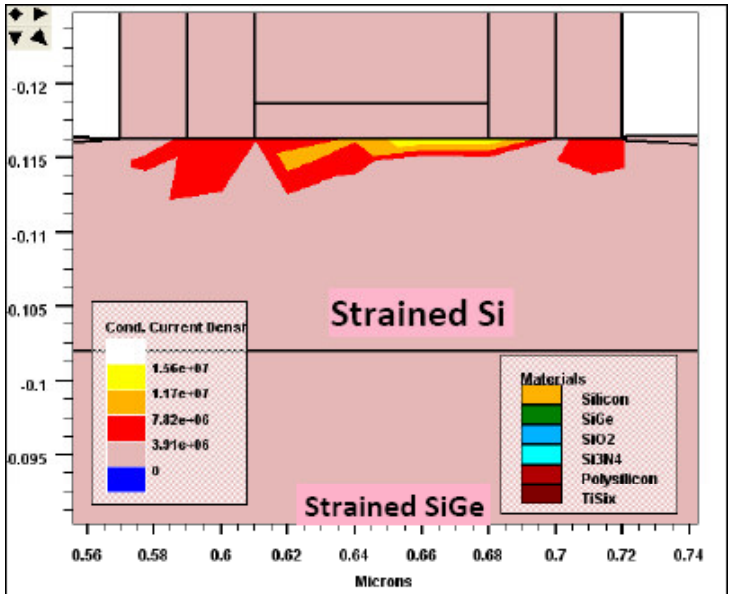
Comparison of single channel (left) and double channel (right) band structure under positive bias.

- The band offset between strained Si and compressive strained SiGe leads to a sufficient discontinuity in conduction band.
- Electrons remain confined to strained Si layer in Δ_2 conduction valley.

NMOS Operation



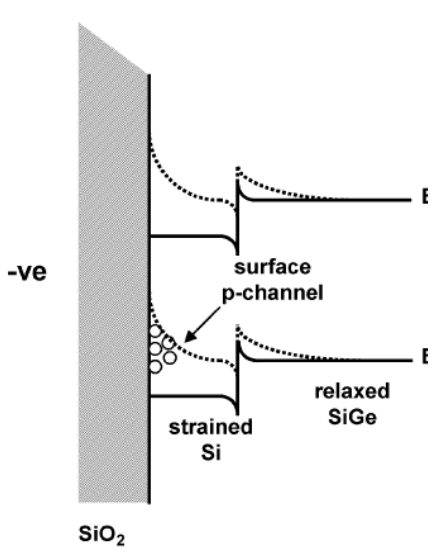
At $V_g = V_{TSN}$



At $V_g > V_{TSN}$

- The depletion regions is formed in strained Si cap layer.
- At $V_g = V_{TSN}$ the inversion occurs in strained Si Layer.
- Due to band alignment , inversion charge due to electron remains in strained Si, even at strong inversion).

Device Theory – Band Diagram PMOS



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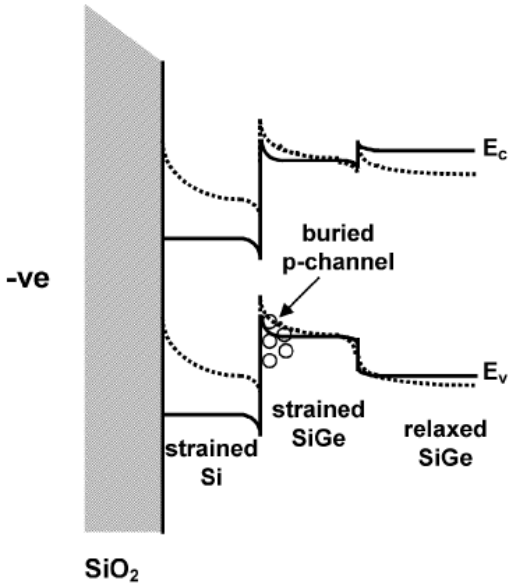


Comparison of single channel (left) and double channel (right) band structure negative bias.

$\Delta E_V = 0.238x\text{-}0.03x^2$

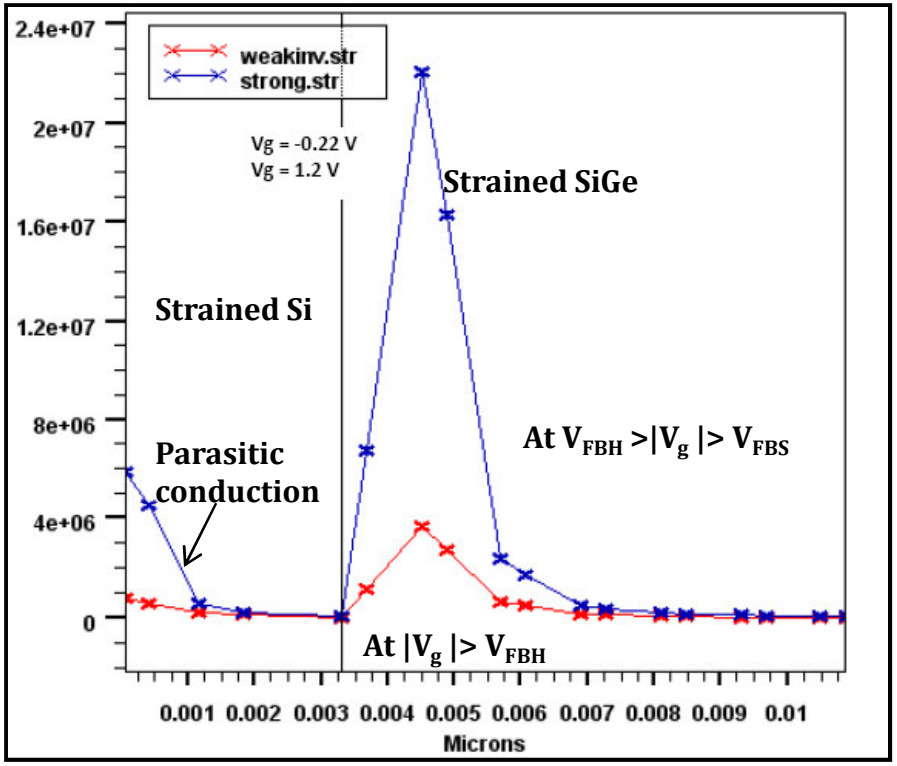
For x = 0.3 , $\Delta E_V = 0.0687$

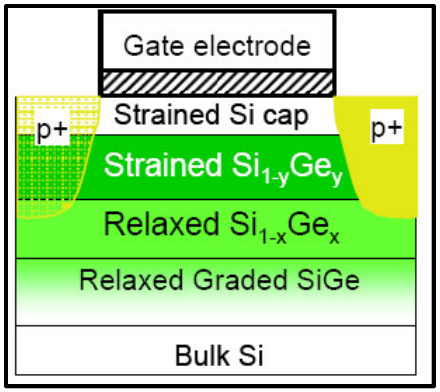
$\Delta E_V \sim 0.74x$

For x = 0.3 , $\Delta E_V = 0.222$

- Valence band offset of compressively stressed layer lower in energy than both underlying strained Si and relaxed SiGe .
- High valence band discontinuity for strained Si/strained SiGe compared to strained Si/SiGe.

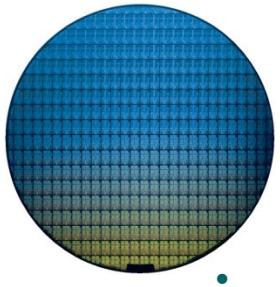
PMOS Operation





Conduction current density as a function of sheet hole concentration in PMOS

- Accumulation region ($V_G \geq V_{FBS}$).
- Depletion region ($V_{THS} > |V_G| > V_{FBH}$), the strained SiGe channel starts getting depleted first.
- Inversion ($V_{THS} \geq V_G$) layer is formed in strained SiGe; ($V_{TS} \geq V_G$) a small parasitic channel forms in strained Si cap layer.



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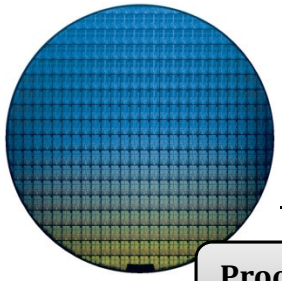
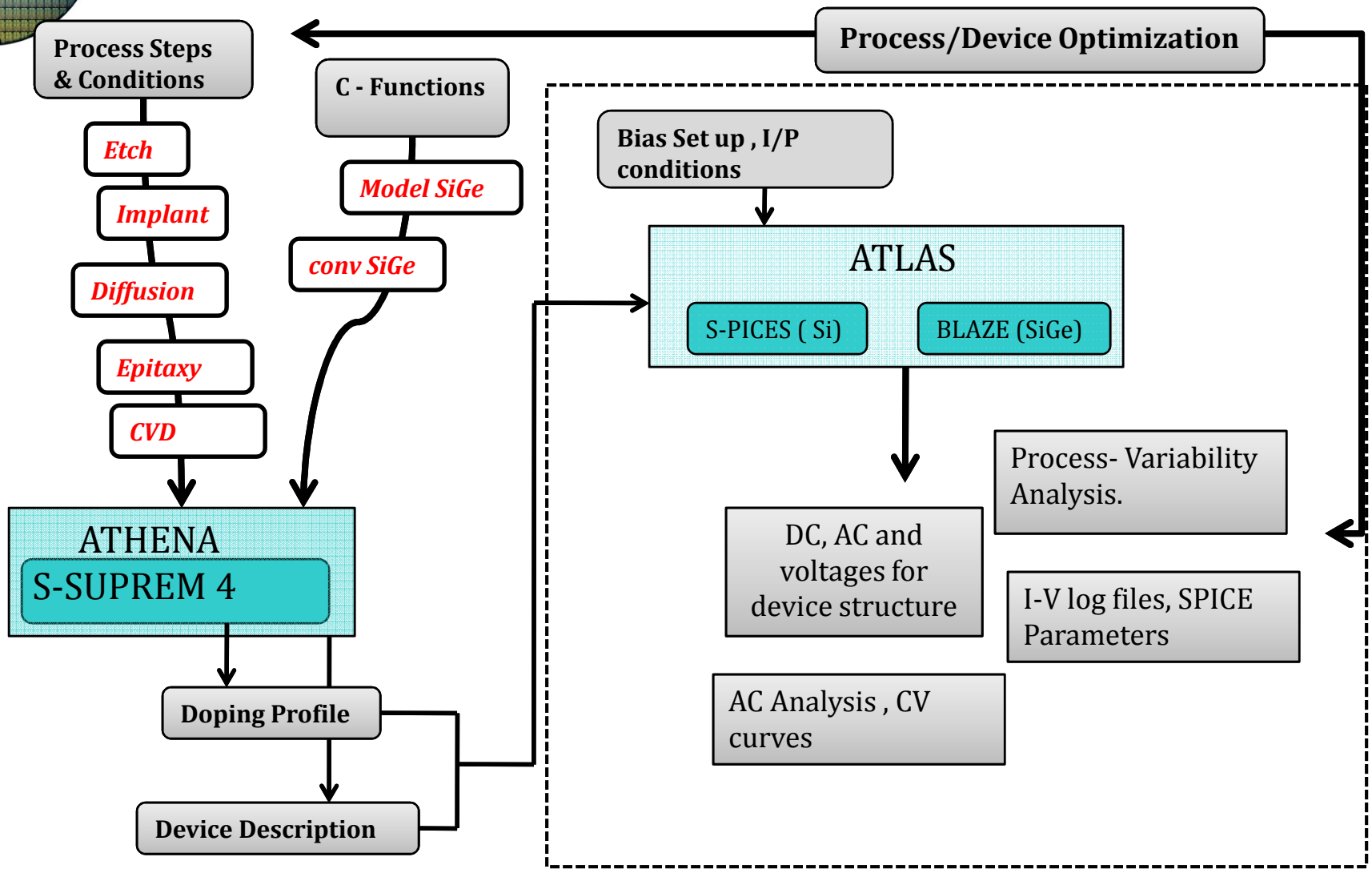
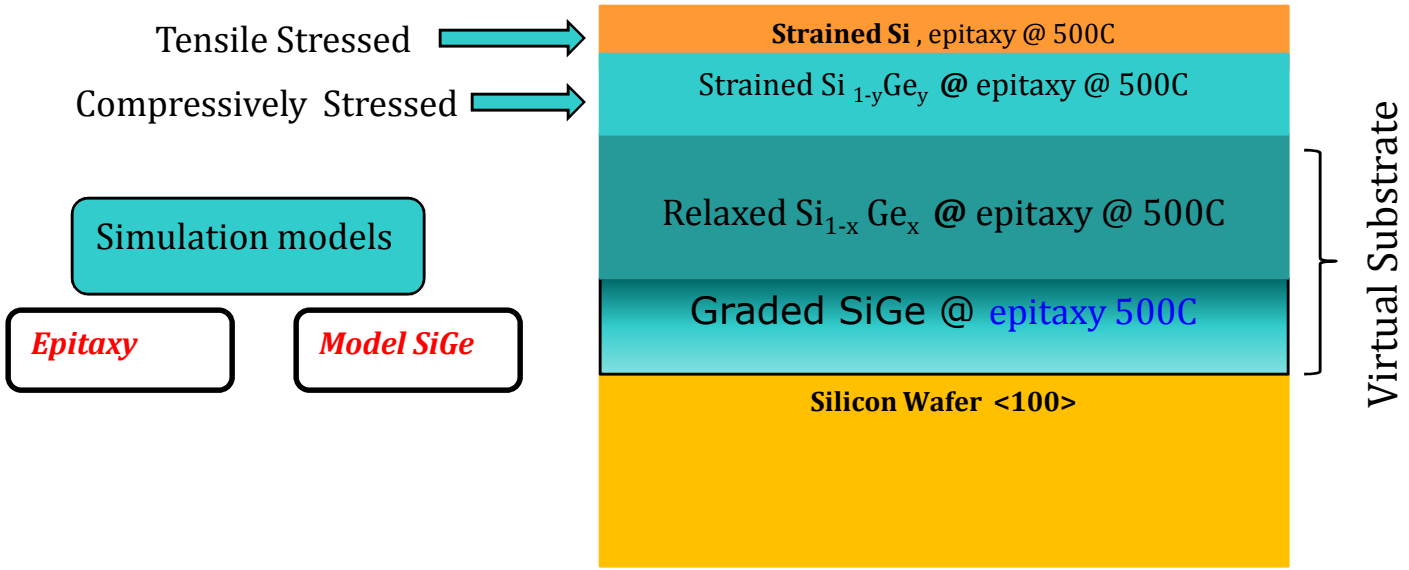
Modeling and Simulation Flowchart



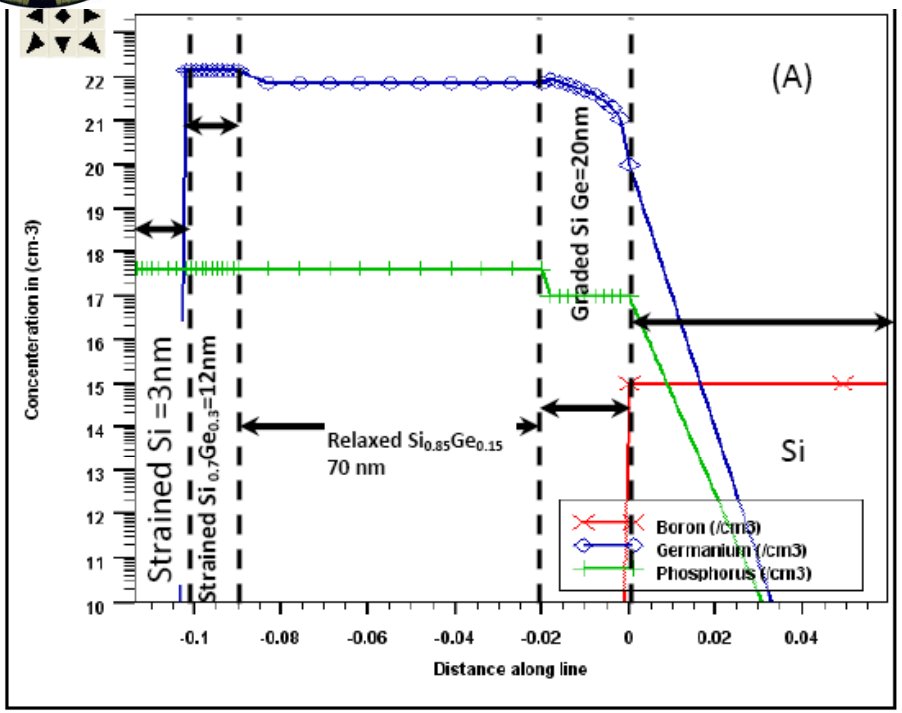


DCH Substrate Development

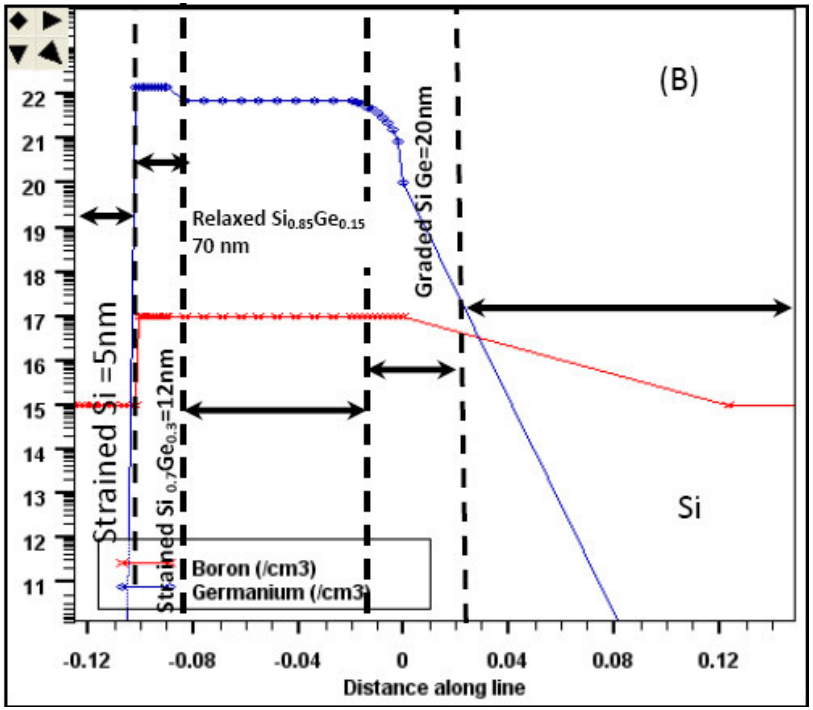


- Epitaxial deposition of all layer @ 500 C , *in-situ* doped.
- Low temperature growth → low surface roughness, better film conformality.
- Graded SiGe (step growth of 0.1).
- Relaxed SiGe , 15 % Ge.
- Strained SiGe , 30 % Ge , compressive stress.

Substrate Doping Profile

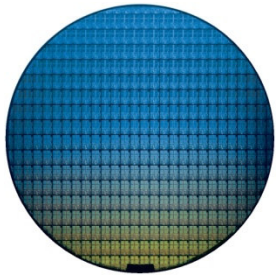


PMOS Substrate



NMOS Substrate

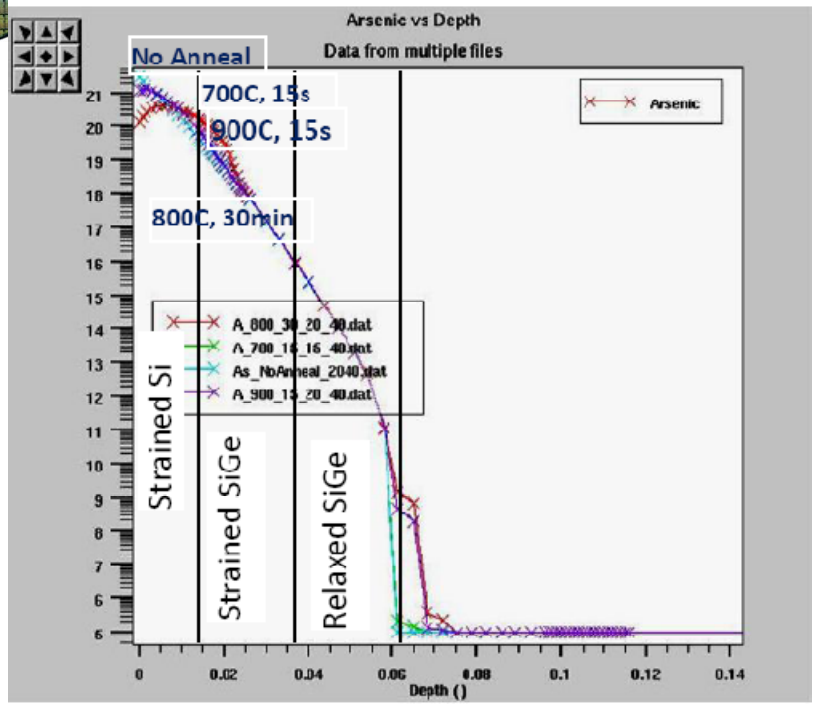
- Germanium out diffusion at Si/SiGe interface.

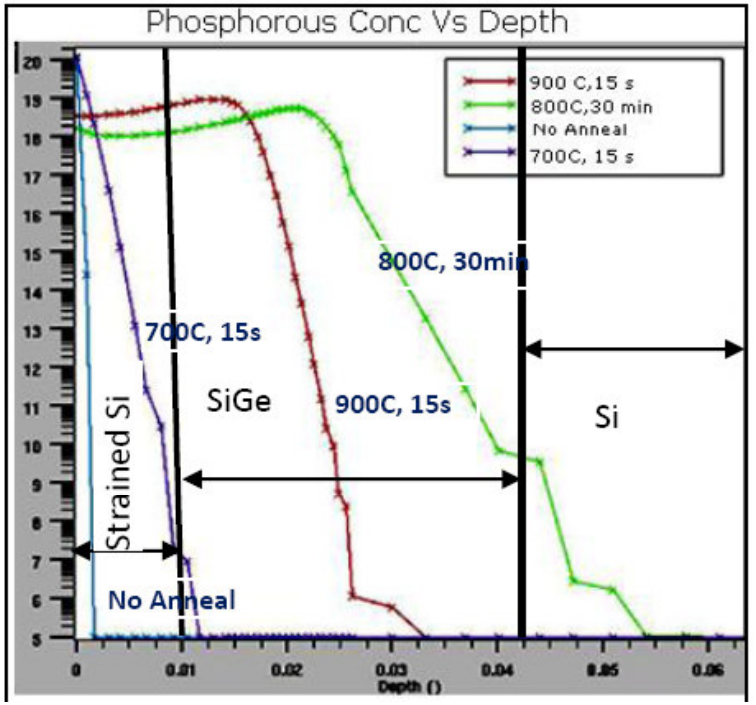


Process Flow

- Nitride Deposition and Oxide Growth. Controlled removal of Si from PMOS
- STI Development , 0.312 µ Trench
- Deposit Sacrificial Oxide. PMOS and NMOS VT adjustment
- 1.7 nm LPCVD, Oxynitride Deposition
- 1300 Å of Polysilicon deposition
- Gate stack Pattern, define CD ~ 65 nm
- LPCVD Spacer I (Oxide),
- S/D Implant I .
- Pattern Spacer I Gate Oxide
- LPCVD Nitride (SPACER II)
- S/D Implant II.
- Spacer II Pattern
- RTA , 900 C, 15 sec
- Silicidation 450 C @ 10 Sec

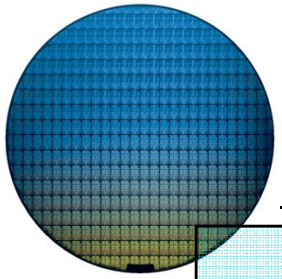
Thermal Effects on Dopant Diffusion





- Phosphorous tends to diffuse more in SiGe as compared to As.
- Compared to As , P shows more sensitivity to anneal time and temperature.
- High anneal time/temperature and low anneal temperature /high anneal time are worst cases and shows degraded device performance.

Device Modeling

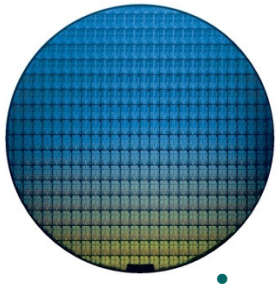


ATLAS

S-PICES (Si)

BLAZE (Si/SiGe)

Energy Balance Transport Model	Drift –Diffusion , Boltzmann transport, velocity overshoot and velocity saturation
Band Gap Narrowing Model	Band Gap Narrowing due to SiGe and Si , Density of states and effective mass.
Carrier –Carrier Scattering Model	Carrier Scattering, lattice scattering, dopant fluctuation, ionized impurity scattering
Conc. SRH Model	Phonon transition, auger transition, surface recombination, impact ionization and tunneling
Density Gradient Quantum Model	Quantum correction to carrier temperature, conduction and potential profile based on Wigner function and Schrodinger-Poisson Equation
Field Based Mobility	Field Based Mobility dependence, velocity saturation.



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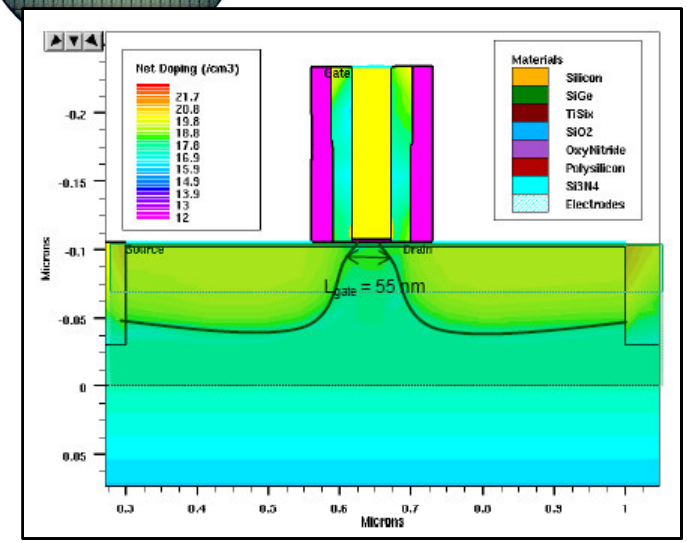
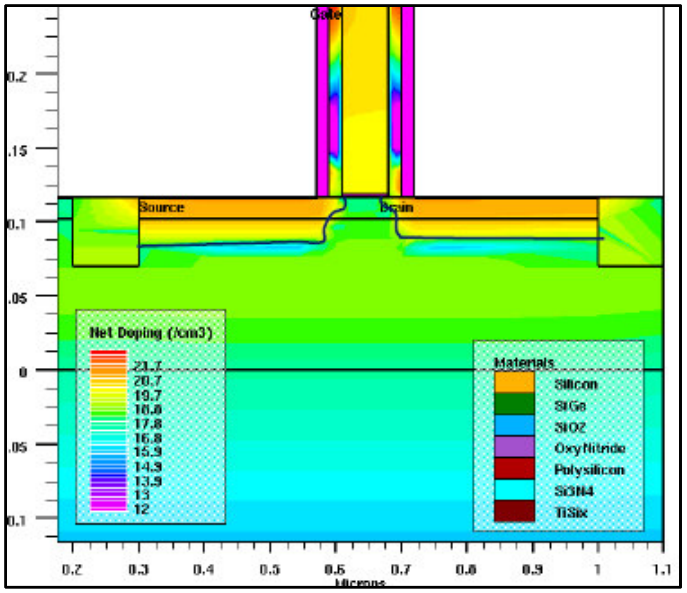
Drain Current Model

Ref B. Bindu *et al*. *IEEE* TED, 06, 2006



PMOS

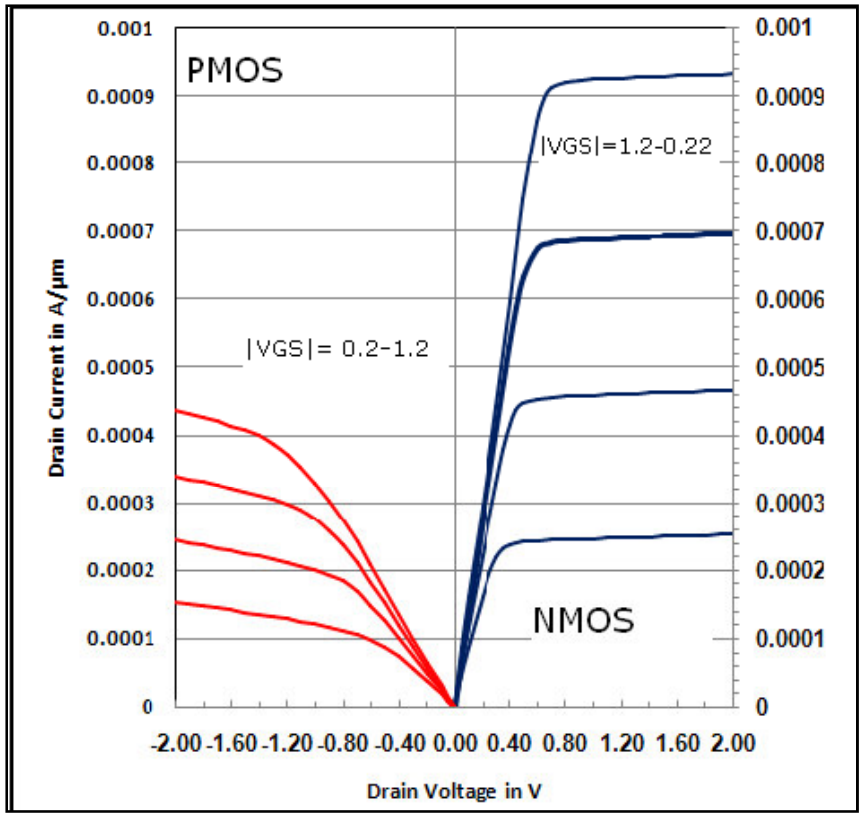
$$I_D = \begin{cases} I_{Dsub}^{H} = \dfrac{-W\mu_p^{SiGe} v_t^{\,2} C_{Dp}}{L}\left[\exp\left(\dfrac{|V_G - V_{THP}|}{m_p v_t}\right)\right]\left[1-\exp\left(\dfrac{|-V_D|}{v_t}\right)\right] & |V_G| < |V_{THP}| \\ I_D^H = \dfrac{-W\mu_p^{SiGe} C}{L\left(1-V_D \big/ 2V_{Lp}^{SiGe}\right)\left(1-\theta_p^H (V_G - V_{THP})\right)} \times \left[V_G - V_{THP} - \dfrac{\alpha_p^H V_D}{2}\right] V_D & |V_D| < |V^{\,H}{}_{Dsat}| \\ I_D^H = I_{Dsat}^H \left\{1+\lambda_p |V_D - V_{Dsat}^H|\right\} & |V_{THP}| \le |V_G| < |V_{TSP}| \\ I_D^H |_{V_G = V_{TSP}} + I_{Dsatp}^S \left\{1+\lambda_p |V_D - V_{Dsatp}^s|\right\} & |V_G| \ge |V_{TSP}| \end{cases}$$



NMOS

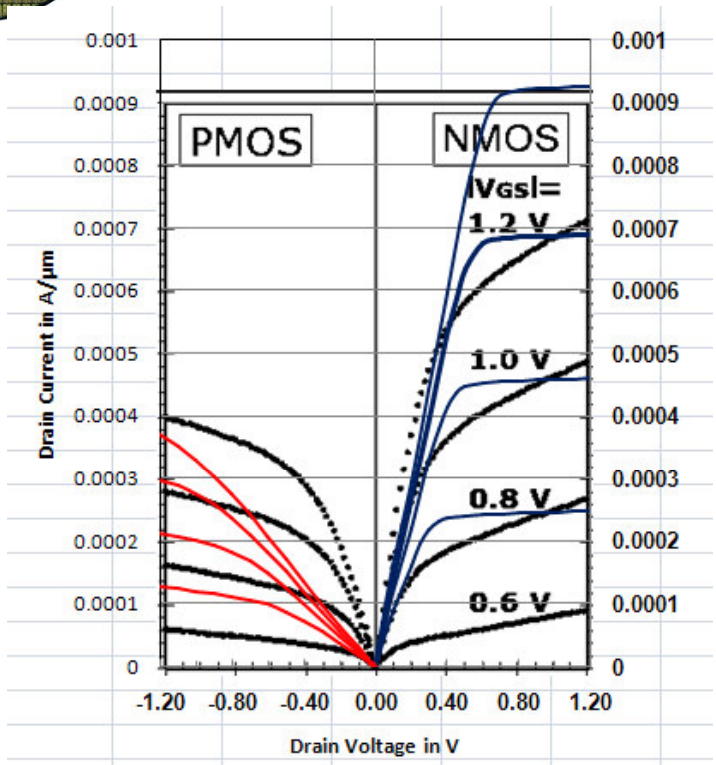
$$I_D = \begin{cases} I_{Dsub}^{s} = \dfrac{-W\mu_n^{Si} v_t^{\,2} C_{Dn}}{L}\left[\exp\left(\dfrac{|V_G - V_{Tsn}|}{mnv_t}\right)\right]\left[1-\exp\left(\dfrac{|-V_D|}{v_t}\right)\right] & |V_G| > |V_{Tsn}| \\ I_{Dlin}^{s} = \dfrac{-W\mu_{n\max}^{Si} C_{ox}}{L\left(1+\dfrac{V_D}{2V_{Ln}^{s}}\right)\left[1+\theta_n^s (V_G - V_{Tsn})\right]}\left[V_G - V_{Tsn} - \dfrac{\alpha_n^s V_D}{2}\right] V_D & |V_D| < |V_{Dsatn}^{s}| \\ I_{Dn}^{s} = I_{Dsatn}^{S}\left\{1+\lambda_p |V_D - V_{Dsatn}^s|\right\} & |V_D| \ge |V_{Dsatn}^{s}| \end{cases}$$

I_D-V_{DS} Curves

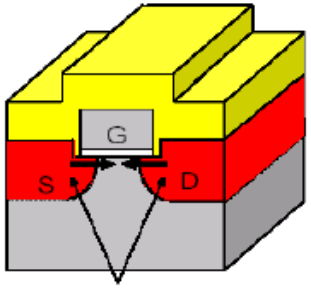


- High drive current for NMOS and PMOS
- NMOS - 0.94 mA/µm and PMOS - 0.45 mA/µm at V_{GS} = 1.2 V .

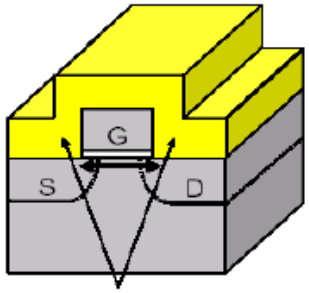
I_D-V_{DS} Comparison with Intel's 65 nm ULP MOS



Compared with Jan *et al., IEDM , 08, 2005*

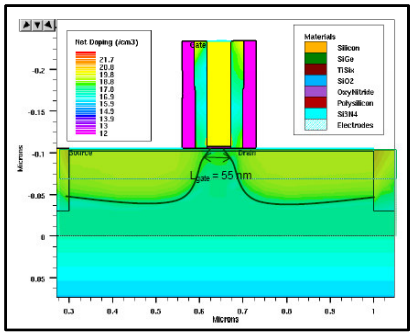


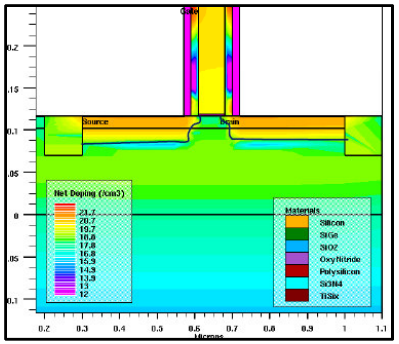
Selective SiGe S-D



Tensile Si_3N_4 Cap

Intel Work (L_g = 54 nm, T_{ox} = 1.7 nm)

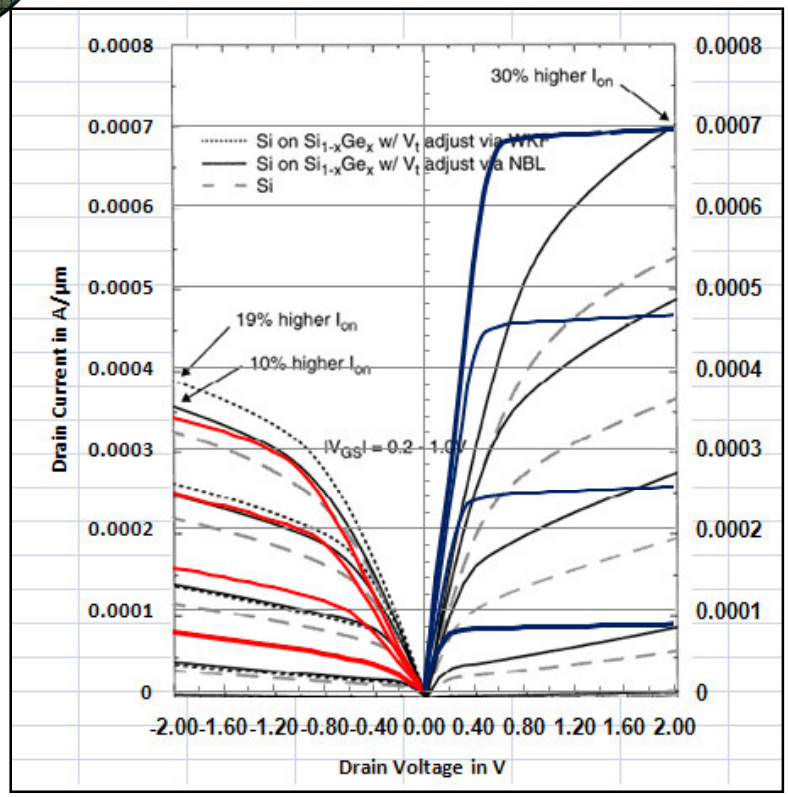




This work (L_g = 55 nm, T_{ox} = 1.7 nm)

- Well matched I-V curves
- Simulated results shows improved performance of ~ 16 % at V_{GS} = 1 V

I_D-V_{DS} DCH Vs. Biaxial Tensile MOS

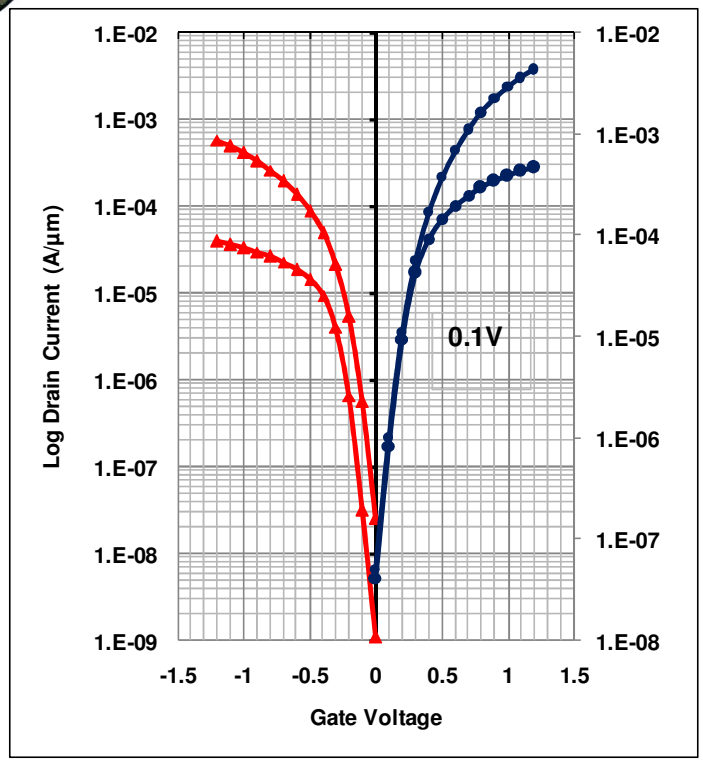


SPECS	This Work	Comparison Work
T_{ox}	1.7 nm	1.3 nm
L_{eff}	55 nm	50 nm
Technology	Biaxial Tensile & Compressive	Biaxial Tensile

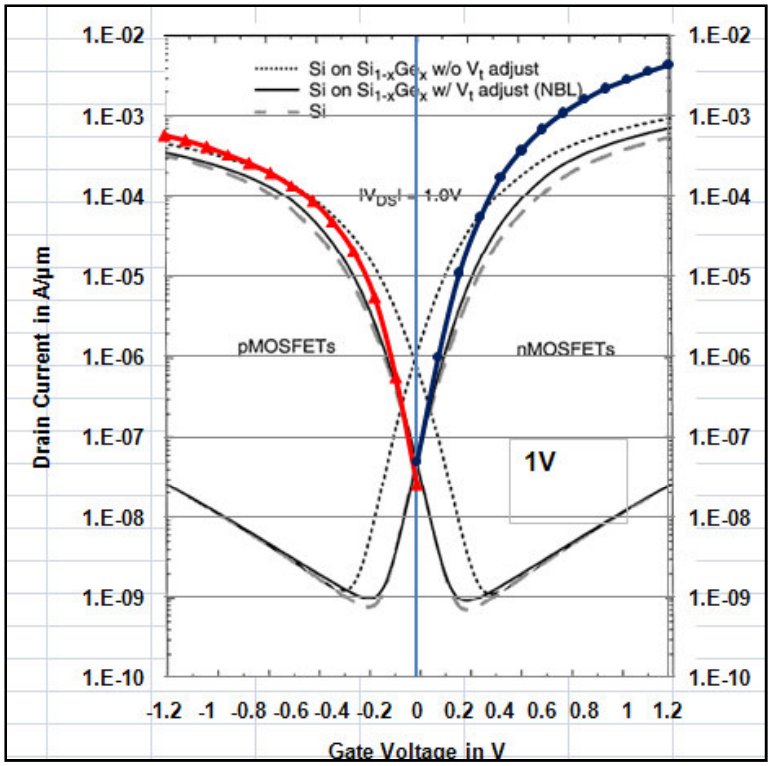
Compared with Jerry G. Fossum *et al., IEEE TED , 04, 2003*

- Improved PMOS and NMOS drive currents by ~ 20 %.
- At higher Vg the PMOS drive current is comparable to comparison work.

Threshold Voltage



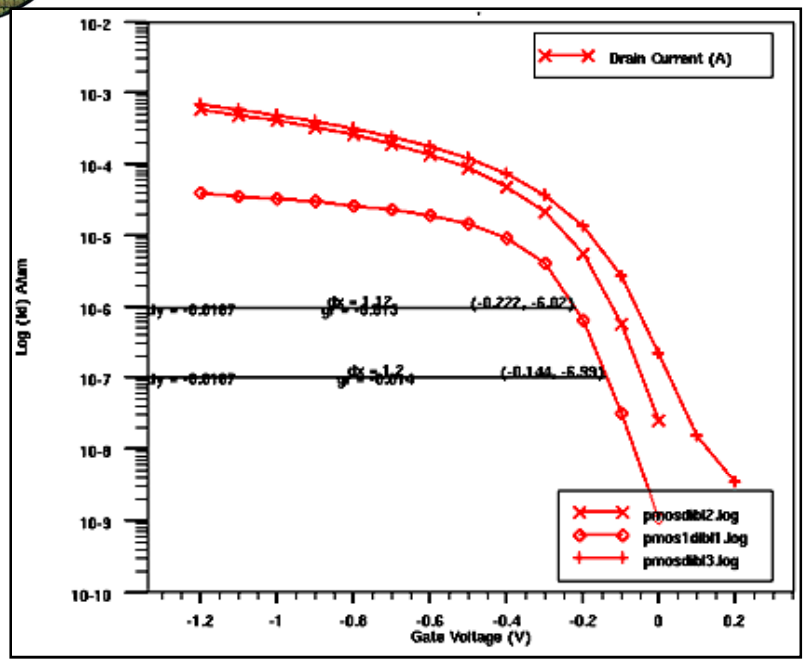
This Work



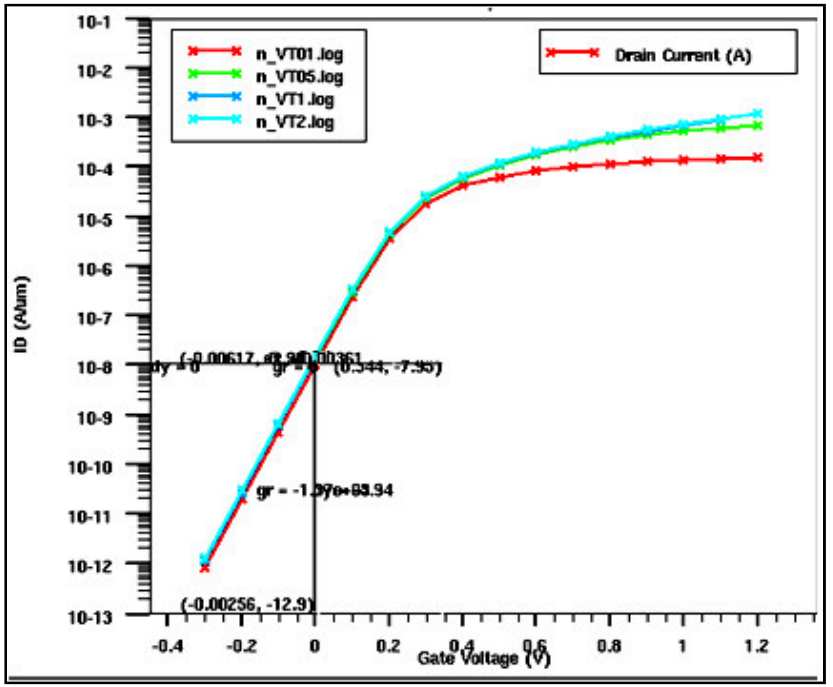
Compared with Jerry G. Fossum *et al., IEEE TED , 04, 2003*

- Threshold voltage of 0.22 and -0.22 for NMOS and PMOS at Vds = 0.1 V.
- Dual channel exhibits lower threshold value than single channel device

Subthreshold & DIBL



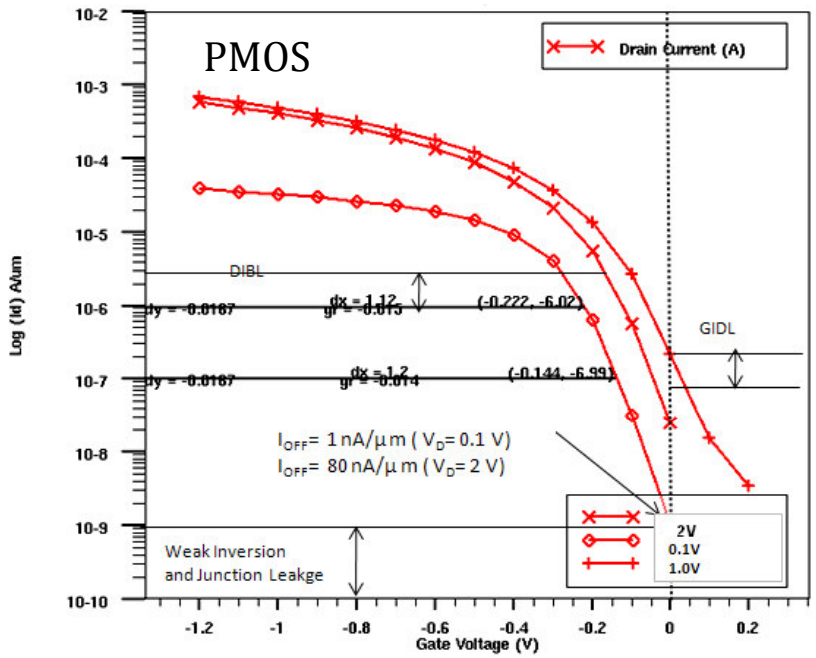
PMOS

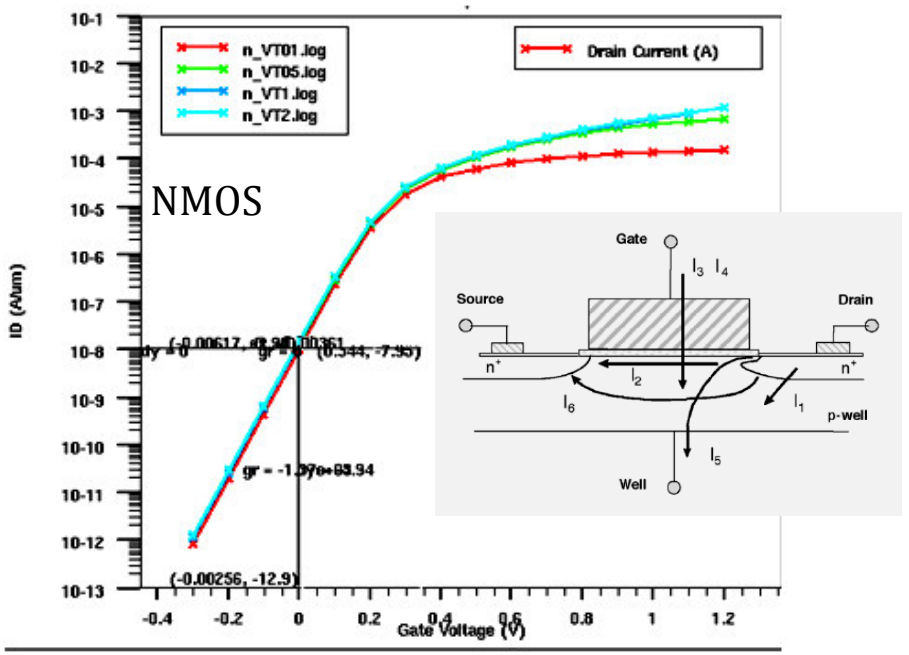


NMOS

- Subthreshold swing of 88 mv/decade and 78 mV/decade for PMOS and NMOS.
- DIBL of 26mV/V and 12 mV/V for PMOS and NMOS.

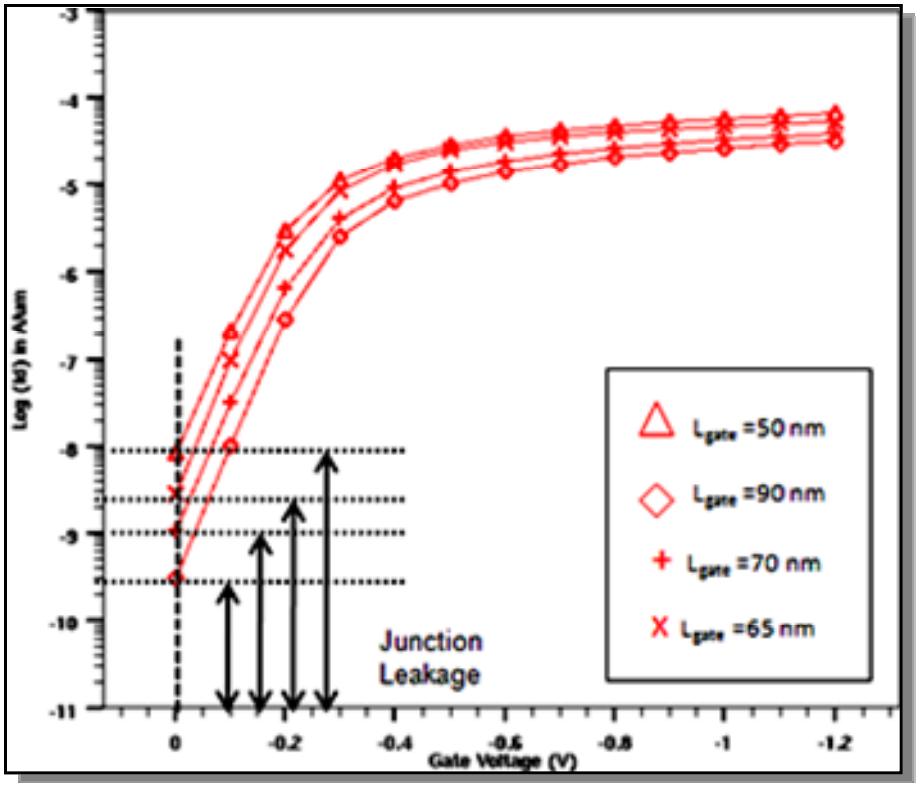
Leakage





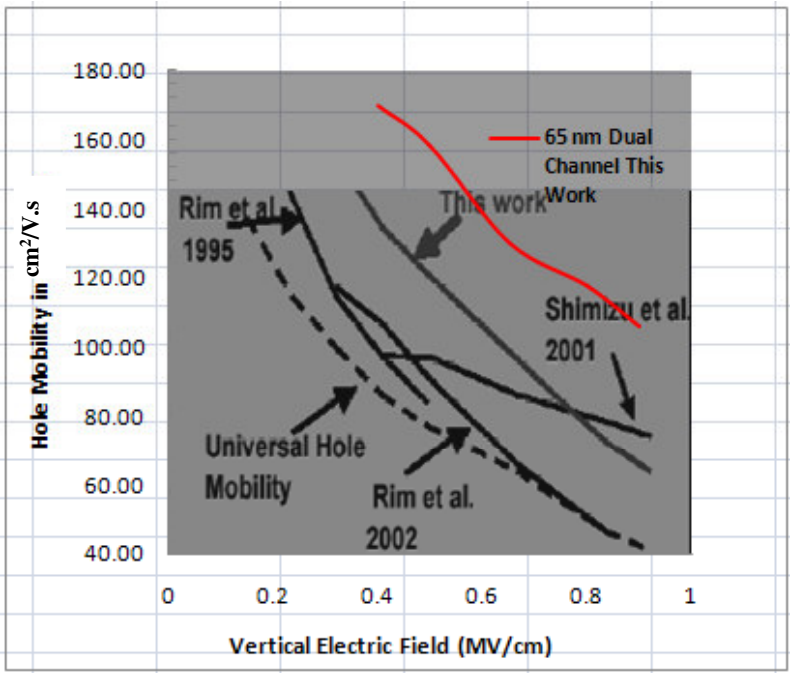
- Off state leakage current of ~ 10 nA/µm and 80 nA/µm for NMOS and PMOS (@ $|V_{DS}|$= 1V).
- Ion/Ioff exceeds 10 orders of magnitude.

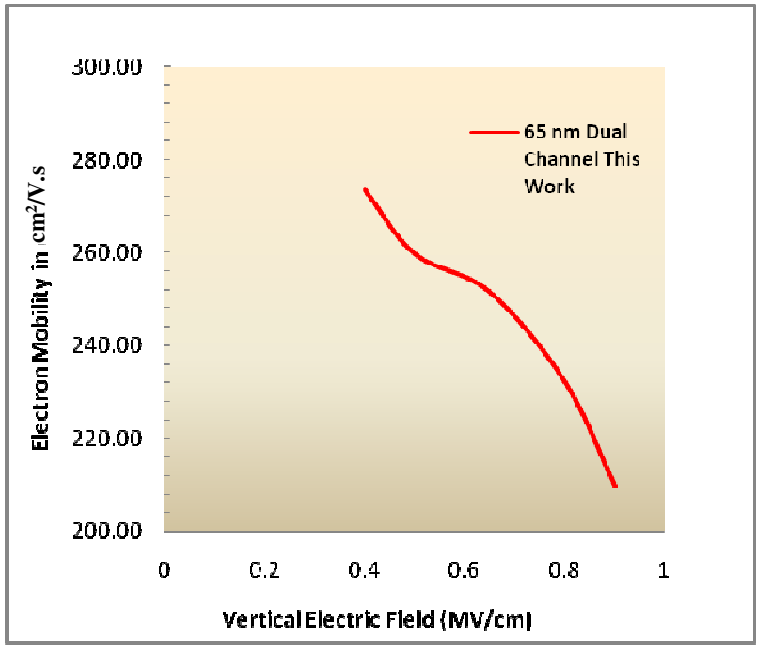
PMOS Leakage Vs Gate Length



- Off-state leakage increases with decrease in gate length.
- Performance degrades almost by 100 x.

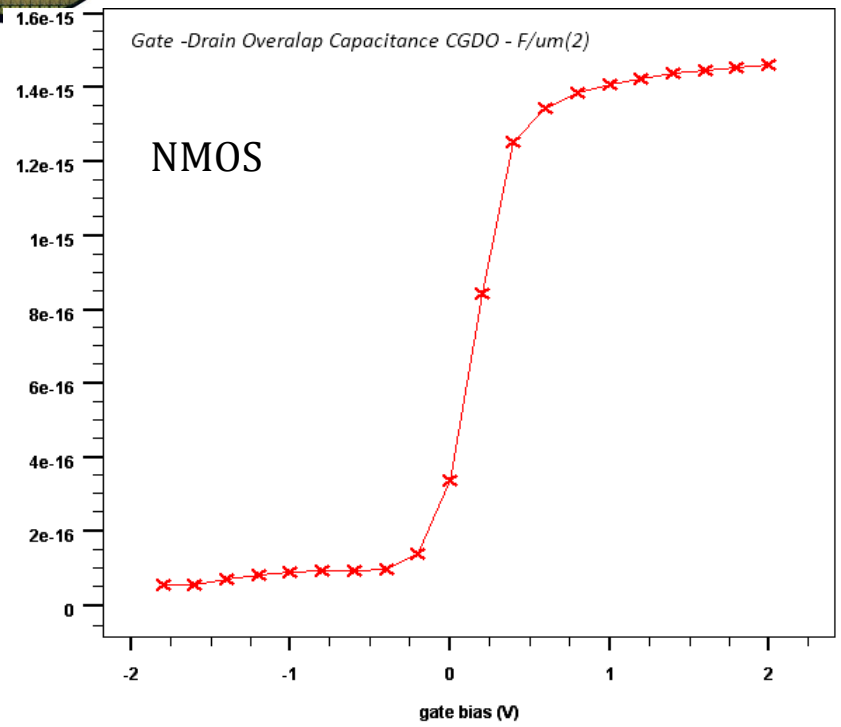
Mobility in Strained Si/Strained SiGe Channel

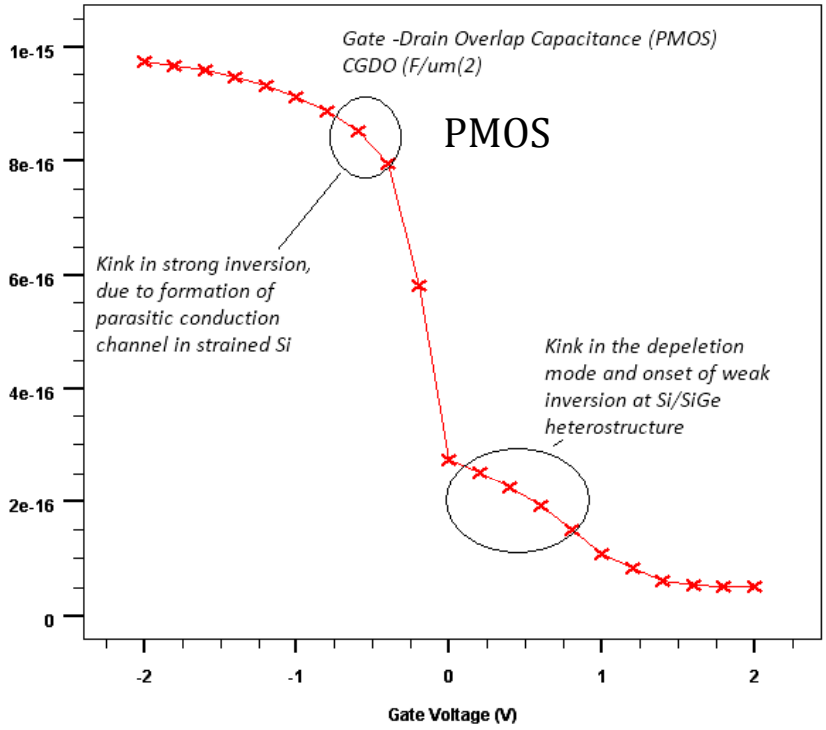




- PMOS mobility improves by 12 % over uniaxial stressed e-SiGe PMOS.
- Peak NMOS mobility of 278 $cm^2/V.s$, no available published data for NMOS mobility at 65 nm.

Overlap Capacitance

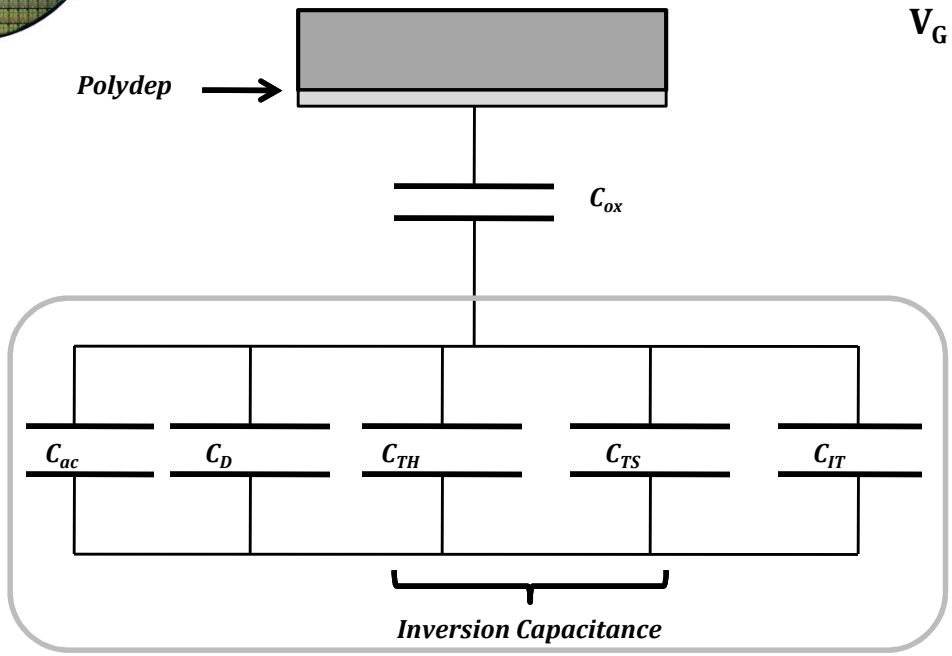




- $C_{GS} = C_{gsd} + C_f$
- Overlap capacitance of 9.73E-09 and 1.63E-09 F/m^2 for NMOS and PMOS, respectively.

Capacitance Model

Capacitance Model : Ref B. Bindu *et al*. *IEEE* TED, 08, 2007



$V_G > V_{FBS}$ Accumulation

$$C_A = \frac{dQ_s}{d\psi_s} = C_{LD}\left[1 + \frac{\psi_s}{2v_t}\right]$$

$$C_{LD} = \varepsilon_s / \sqrt{\varepsilon_s v_t / qN_{D/A}}$$

$C_g = C_{ox}$ in series with C_A

$V_{THS} < V_G < V_{FBS}$ Depletion

$$C_D = \frac{1}{C_{ox}}\left[\sqrt{1 + \frac{\left(2C^2_{ox}(V_G - V_{FBS})\right)}{q\varepsilon_{si}N_{a/d}}} - 1\right]$$

$C_g = C_D$ series with C_{ox}
For highly doped case, $C_g = C_{LD}$ in series with C_{ox}

$V_G > V_{TH}$ Inversion

$$C_{TH} = -q(d\rho_s^H / d\psi_s)$$

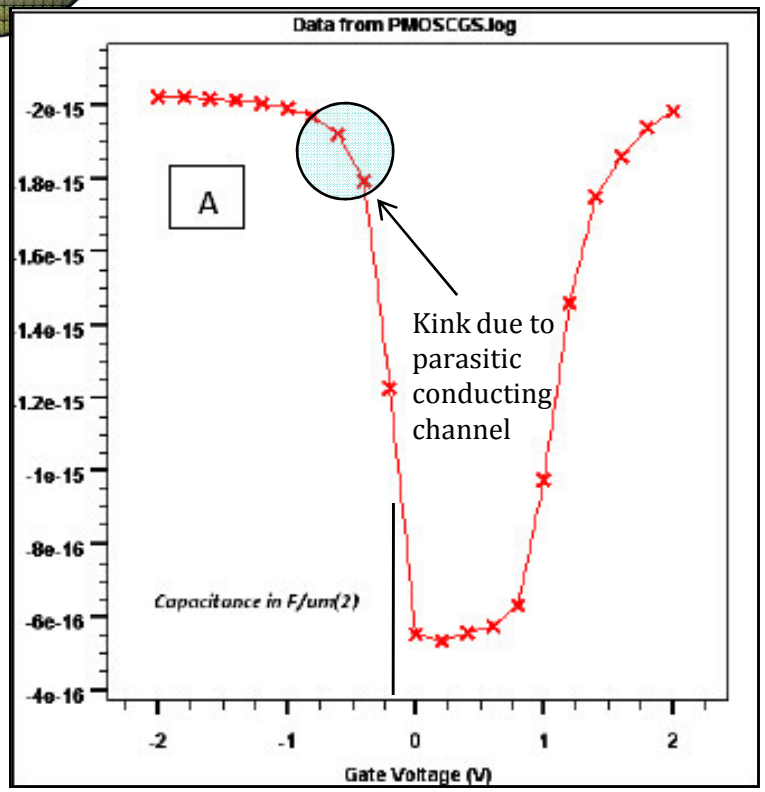
$C_g = C_{ox}$ in series C_{TH}

$V_{TS} \geq V_G$. Strong Inversion

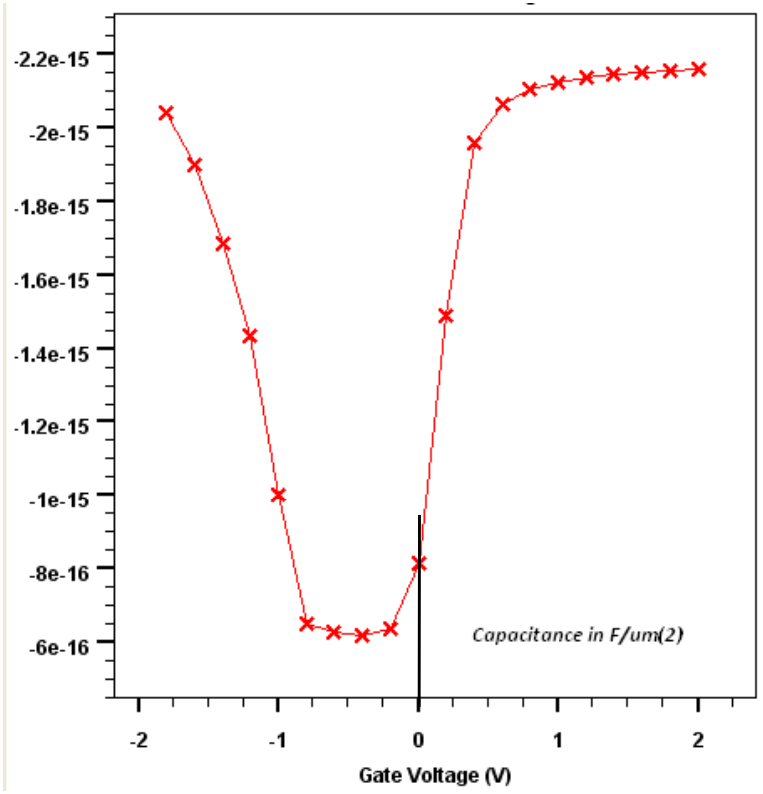
$$C_{TS} = -q(d\rho_s^S / d\psi_s) = -q(d\rho_s^S / dV_G)(dV_G / d\psi_s)$$

$C_g = C_{ox}$

Total Gate Capacitance

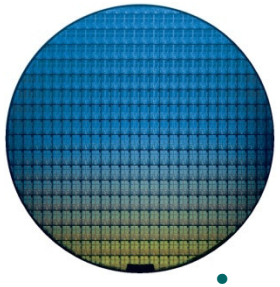


PMOS Total Gate Cap



NMOS Total Gate Cap

$$C_G = \frac{1}{C_{ox}} + \frac{1}{C_D + C_I}$$



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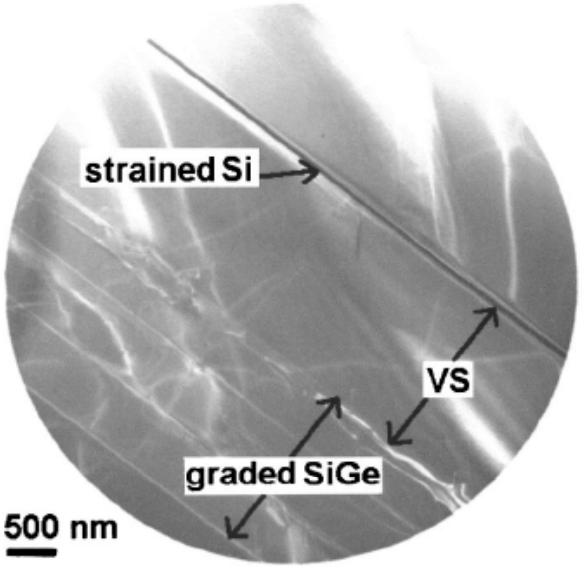
Challenges

Cross hatching in Strained Si/SiGe wafer

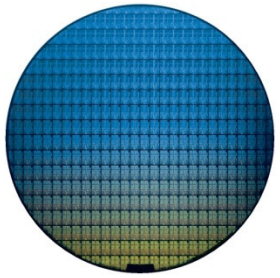
Ref S. H. Olsen *et al . , IEEE TED ,2003*



Surface Roughness in Strained Si/SiGe wafer

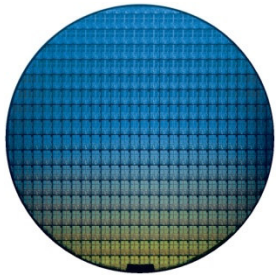
Ref S. H. Olsen *et al . , IEEE TED ,2003*

- Surface roughness and cross hatching.
- Germanium out diffusion and strain relaxation.
- High Leakage
- Process challenges in CMOS integration and high cost



Future Work

- Modeling
  - Models for effectively calculating strain in layers.
  - Strain dependence of mobility and effective density of state calculation.
  - More robust diffusion profiles and models for SiGe.
  - Compact Models development for Strained Si technology.
- Device Optimization
  - Using Strained SiGe without Si cap for PMOS, for improved device behavior.
  - High –k dielectric for integrating gate dielectric with SiGe layer.
  - Metal Gate Integration.
  - Developing a low cost process method with lower defect and dislocations by optimizing LPCVD method.



Key Messages

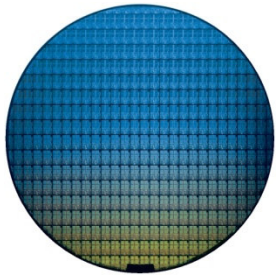
- Process induced strain is the most significant innovation in submicron MOS transistor technology , but scalability a major bottleneck in driving performance for sub 65 nm technologies.

- Compound semiconductor material such as SiGe, III-V's, a promising solution for foreseeable future of MOS transistor technology.

- Dual channel CMOS transistor technology with biaxial tensile strained Si and biaxial compressive strained SiGe channel a promising solution to sustain scaling challenges

- Higher drive currents and comparable performance with process induced strain.

- Challenges with SiGe channel: leakage issues, surface roughness and cross hatching, higher cost and process complexivity with substrate development



Acknowledgement

Thesis Advisor , Chair

- Dr James E. Moon

Thesis Committee Members

- Dr . Santosh Kurinec
- Dr. P.R. Mukund

AMD Process Development Team

- Karol Finfando
- Dr. Edward Ehrichs
- Dr. Belinda Hannon
- Ashwin Chincoli
- Amado Ramirez

Silvaco Corporation CA

EE. Staff

- Ken Snyder
- James Stefano
- Patti Vicari

Friends

- Srinivas Pandharpure(RIT Alum , IBM SRDC, India)
- Gaurav Thareja (PhD Student, Stanford Univ.)
- Kunal Rohilla (RIT Alum, Kla –Tencor)

RIT Library

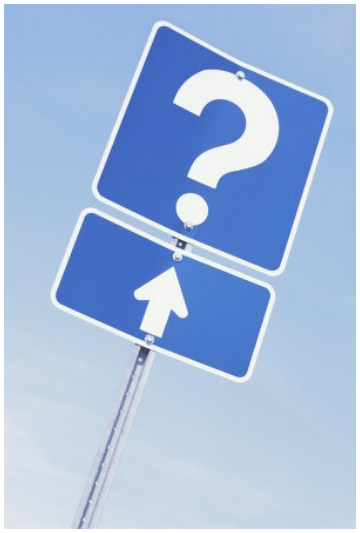
In addition to above people I would like to thank,

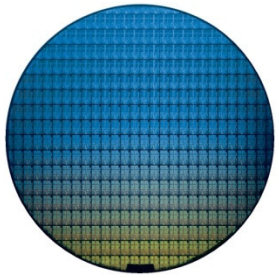
- Intel's Reliability Team.
- Dr. Joesph Watts. (IBM SRDC)
- Dr. William Tonti (IBM SRDC)
- Dr. Scott Springer (IBM SRDC)
- Dr. Syed Islam

- This work was partly funded by NSF through Grant Number #EEC-0530575

THANK YOU!!

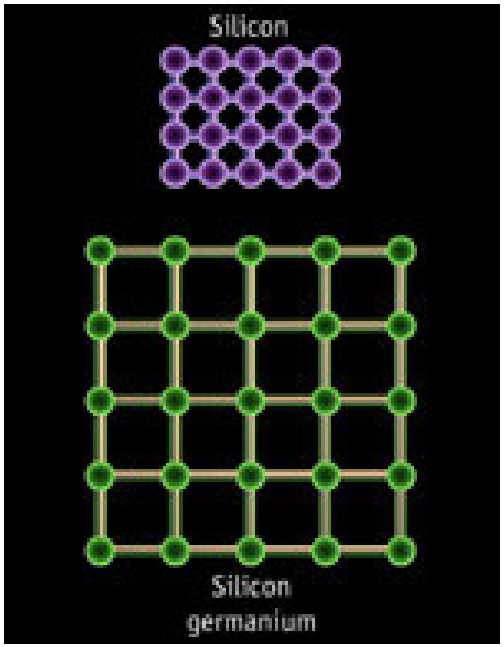
QUESTIONS

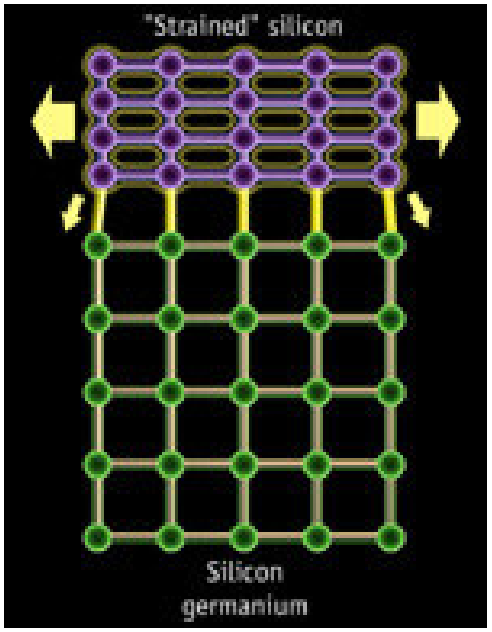


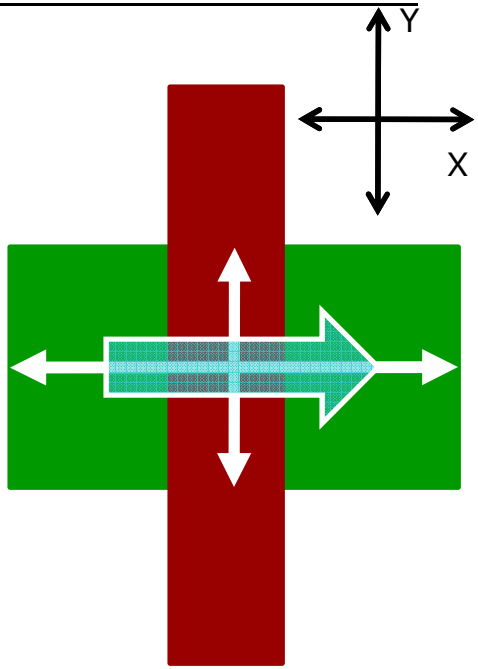


BACKUP SLIDES

Substrate Induced: Biaxial Tensile Strain





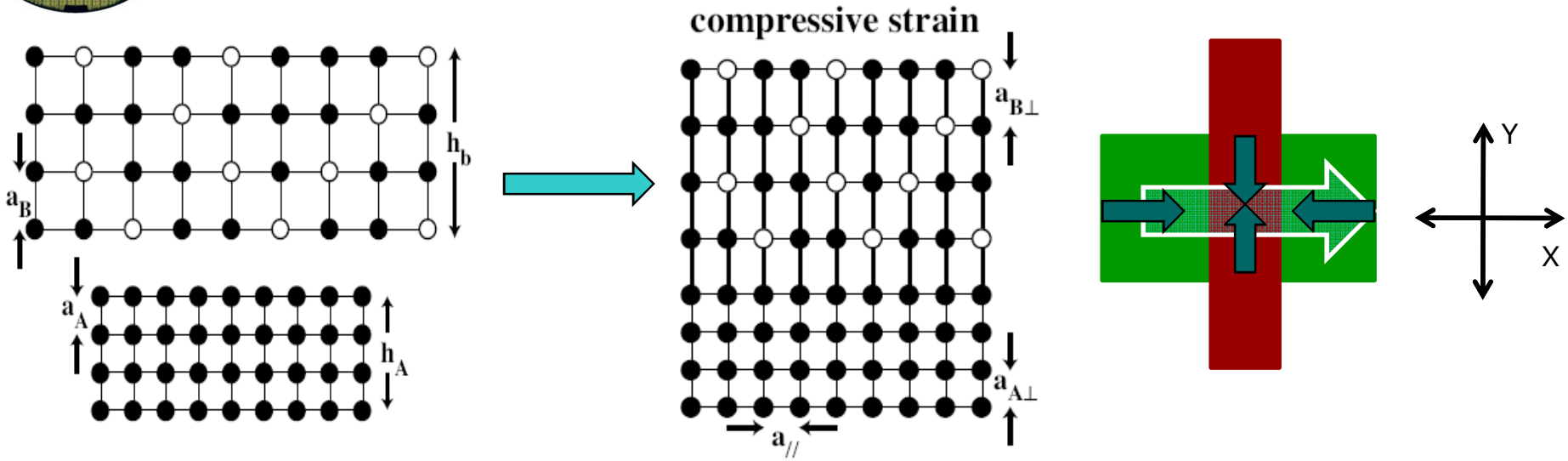


Biaxial Tensile Stress

- Pseudomorphic growth of epi layer either by MBE or LPCVD.
- Silicon under Biaxial tensile stress ($a_{silicon} < a_{SiGe}$ (x)).
- Stress induction in *x y* plane.

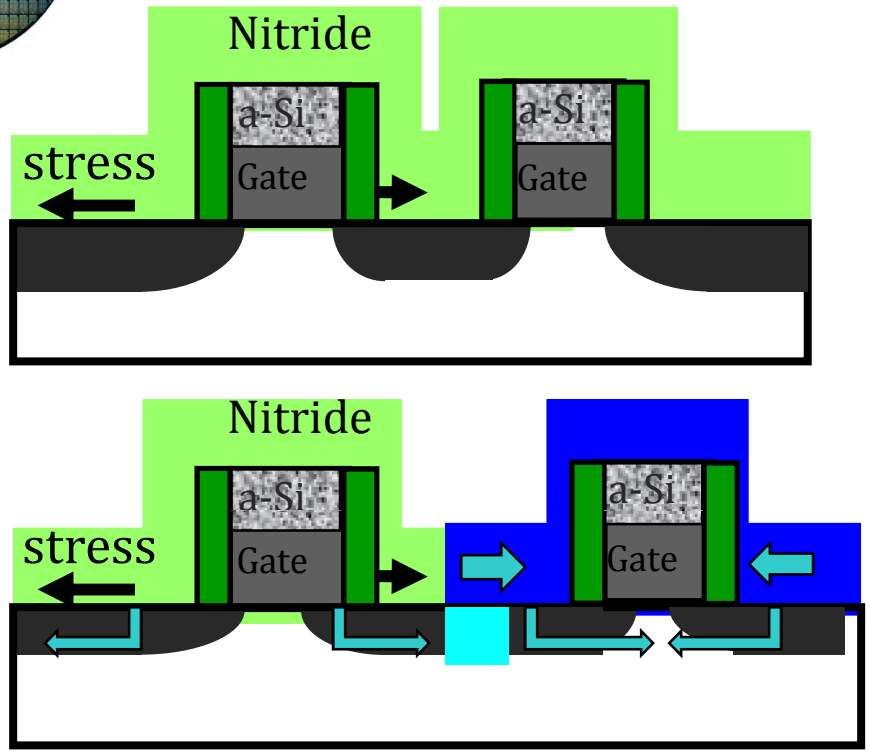
Ref : Victor Chan IBM SRDC, Hope well Junction , Jan 2007

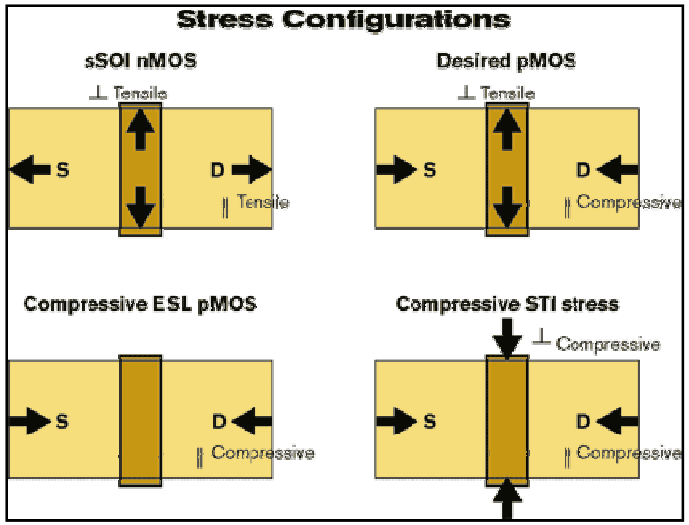
Substrate Induced: Biaxial Compressive Strain



- $Si_{1-y}\,Ge_y$ film deposited over $Si_{1-x}Ge_x$ (y >x)
- $Si_{1-y}\,Ge_y$ film under biaxial longitudinal and transverse compressive stress, with an out of plane tensile component.

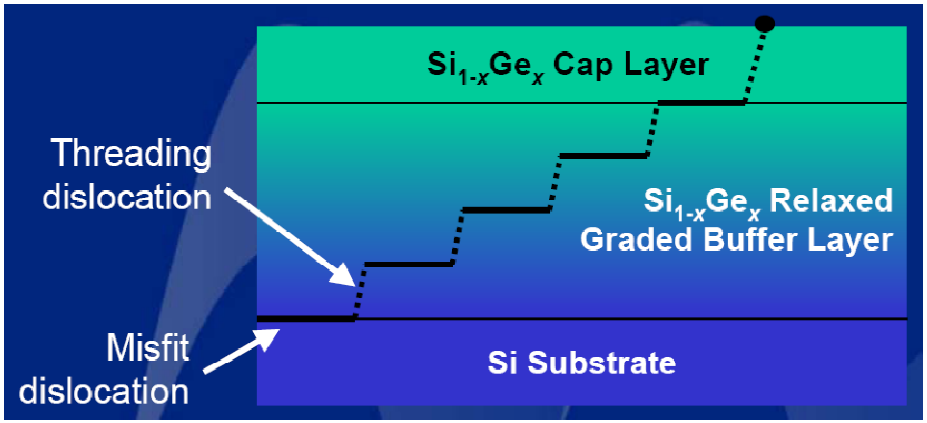
Process Induced stress: Uniaxial Strain

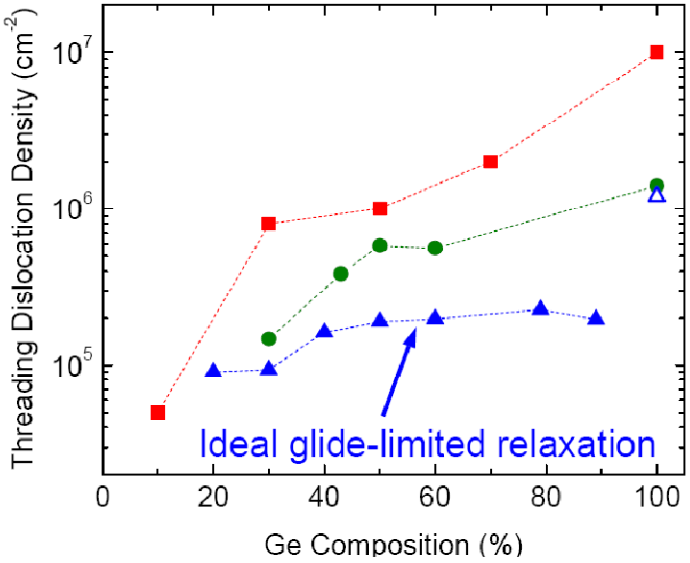




- Process induced strain , strain in *x* (110) direction.
- Common stress techniques, plasma enhanced nitride layer deposition, stress memorization technique, and e-SiGe in S/D region.
- Present in current 90 nm and 65 nm technology.

MISFIT DISLOCATION

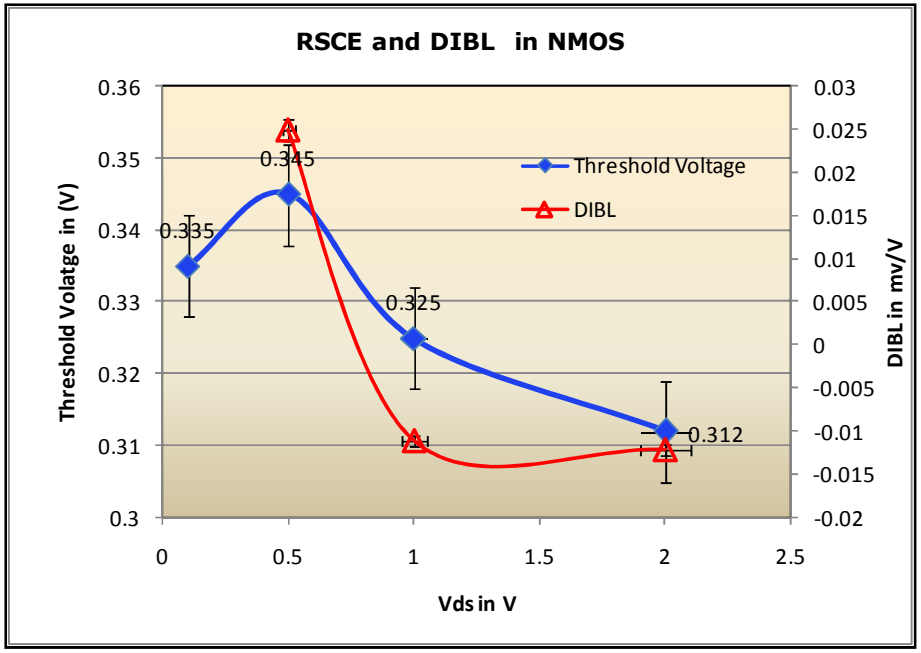


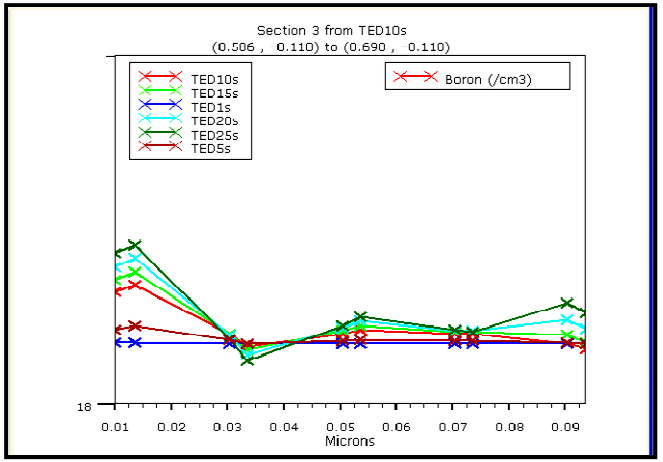


- Above critical thickness , film relaxes due to
  - elastic deformation,
  - plastic deformation
  - Dislocation or half loop nucleation
- Approaches to reduce defect
  - LPCVD or Epitaxy between 500 ~ 800 C followed by CMP.
  - Graded Buffer
  - SiGe Free Strained Si/ SOI integration

Ref : Matthew Erdmann, 204th Meeting *ECS*, October 2003. (courtesy : Amber wave)

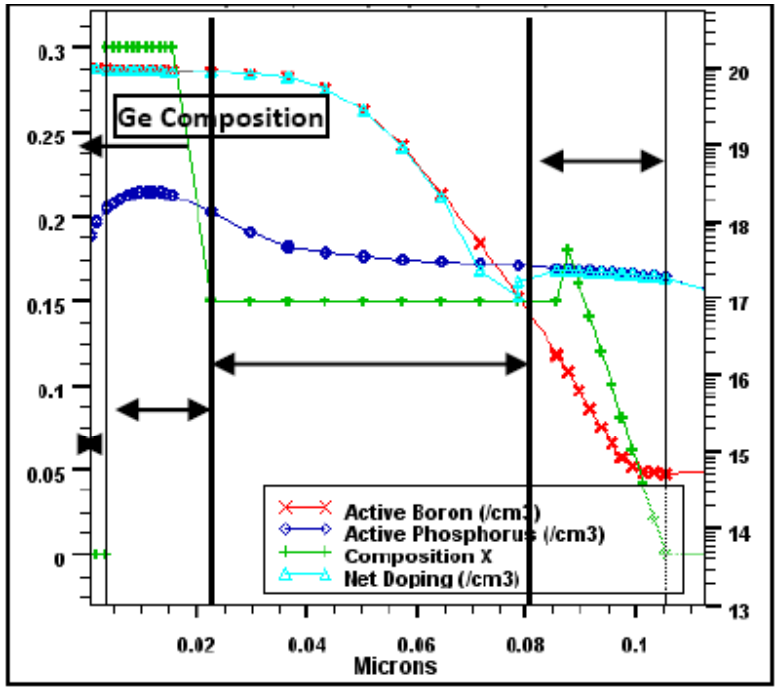
RSCE in N-MOS



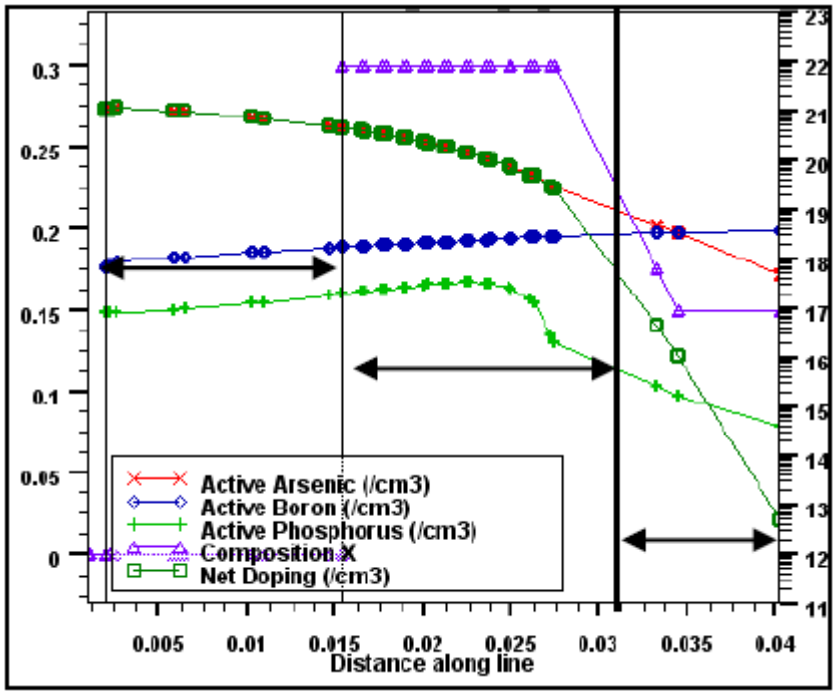


- NMOS devices shows reverse short channel effect, initial increase in threshold voltage with increase in VDS.
- Boron pile up due to transient enhanced diffusion seems to be the cause.

Doping Profile after Silicidation



PMOS



NMOS

- Junction Depth calculated from SIMS profile ~ 78 nm for PMOS and 35 nm.
- S/D doping of order ~ 1E21 cm^{-3} .