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Performance Evaluation of III-V Hetero/Homojunction Esaki Tunnel Diodes on Si and Lattice Matched Substrates

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by

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A dissertation submitted in partial fulfillment of the requirements

for the degree of Doctorate of Philosophy in Microsystems Engineering

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Committee Approval:

We, the undersigned committee members, certify that we have advised and/or supervised the candidate on the work described in this dissertation. We further certify that we have reviewed the dissertation manuscript and approve it in partial fulfillment of the requirements of the degree of Doctorate of Philosophy in Microsystems Engineering.

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Abstract

Understanding of quantum tunneling phenomenon in semiconductor systems is increasingly important as CMOS replacement technologies are investigated. This dissertation studies a variety of heterojunction materials and types to increase tunnel currents to CMOS competitive levels and to understand how integration onto Si substrates affects performance. Esaki tunnel diodes were grown by Molecular Beam Epitaxy (MBE) on Si substrates via a graded buffer and control Esaki tunnel diodes grown on lattice matched substrates for this work. Peak current density for each diode is extracted and benchmarked to build an empirical data set for predicting diode performance. Additionally, statistics are used as tool to show peak to valley ratio for the III-V on Si sample and the control perform similarly below a threshold area. This work has applications beyond logic, as multijunction solar cell, heterojunction bipolar transistor, and light emitting diode designs all benefit from better tunnel contact design.

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This work is dedicated to my family, the source of my greatest strength.

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List of Symbols and Abbreviations

Term	Description	Units/Value
A	Area	cm^2
A_C	Corrected Area	cm^2
a	Measured undercut in X direction	nm
b	Measured undercut in Y direction	nm
C'_D	Depletion region capacitance per unit area	F/cm^2
C'_{ox}	Oxide capacitance per unit area	F/cm^2
D	Overlap integral	eV
D_n	Electron diffusion coefficient	cm^2/s
D_p	Hole diffusion coefficient	cm^2/s
$\mathcal{E}$	Electric field	V/cm
E_C	Energy at the conduction band edge	eV
ΔE_C	Change in energy at the conduction band edge	eV
E_F	Fermi level	eV
E_G	Band gap energy	eV
E_{Geff}	Effective band gap energy	eV
E_V	Energy at the valence band edge	eV
ΔE_V	Change in energy at the valence band edge	eV
E_x, E_y	Electric field normal and parallel to the gate	V/cm
$\hbar$	Reduced Planck constant	6.582×10^{-16} eV·s
I	Current	A
I_T	Band to band tunneling current	A
I_P	Peak current	A

Term	Description	Units/Value
I_V	Valley current	A
I_D	Diffusion current	A
I_E	Excess current	A
I_{Esaki}	Esaki diode current	A
J_D	Diffusion current density	A/cm^2
J_E	Excess current density	A/cm^2
J_{Esaki}	Esaki diode current density	A/cm^2
J_n	Electron current density	A/cm^2
J_p	Hole current density	A/cm^2
J_P	Peak current density	A/cm^2
J_S	Reverse saturation current density	A/cm^2
J_T	Band to band tunneling current density	A/cm^2
J_V	Valley current density	A/cm^2
k	Boltzmann's constant	8.617×10^{-5} eV/K
L_n	Electron Debye length	nm
L_p	Hole Debye length	nm
m^*	Carrier effective mass	kg
N_A	Acceptor concentration	cm^{-3}
N_D	Donor concentration	cm^{-3}
N^*	Effective doping density	cm^{-3}
N_c	Effective density of states in the conduction band	cm^{-3}
N_v	Effective density of states in the valence band	cm^{-3}
n_i	Intrinsic carrier concentration	cm^{-3}
PVCR	Peak to valley current ratio	
q	Elementary charge	1.602×10^{-19} C

Term	Description	Units/Value
R_S	Series Resistance	Ω
RMS	Root Mean Squared (roughness measurement)	nm
SS	Subthreshold swing	V/dec
T	Temperature	K
V_a	Applied voltage	V
V_P	Peak voltage	V
V_V	Valley voltage	V
V_{FB}	Flatband voltage	V
V_G	Gate voltage	V
W_D	Depletion Width	nm
ϵ_s	Permittivity of a semiconductor	F/cm
μ_n, μ_p	Mobility of electrons and holes respectively	cm/V·s
Ψ_s	Surface potential	eV
ψ_{bi}	Built in potential	eV
χ	Electron affinity	eV

Chapter 1

Introduction

Pressure to improve device performance is a constant companion to semiconductor research. The path from Braun (development of metal-semiconductor contacts) to Shockley, Bardeen, and Brattain's transistor through the present state of the art has been fraught with challenge's, whether it was oxide interface or material, progress has relied on aggressive engineering solutions [1–3]. One such drive has been towards the replacement of Si as the channel material for complementary metal oxide semiconductor (CMOS) technology. Thus, III-V materials such as $In_{0.53}Ga_{0.47}As$ and InAs are being studied in earnest as replacement materials and, as such, much needs to be investigated with regard to dopants and defects. With the potential change in channel also comes a fundamentally different device, tunneling field effect transistors (TFETs) are being investigated as a device with superior power consumption capabilities when compared to standard CMOS [4, 5]. Due to the tunneling nature of carrier transport for TFETs, transconductance, or substhreshold slope (SS), can be below the thermal limit of $\approx$ 60 mV/dec. at 300° K which will allow for more aggresive voltage scaling with the associated reduction in power requirements [6, 7]. This work aims to answer some of the fundamental materials questions for how different designs might affect the tunneling performance.

Most TFET designs involve a p-i-n diode structure consisting of a III-V [8, 9] or group IV semiconductor. Current is modulated by applying a gate bias across an

intrinsic region which causes an accumulation of carriers. The increase in carriers causes an overlap of the conduction and valence bands, thereby enabling tunneling across the band gap of the device. Most TFET research has involved building devices based on model predictions [10]. However, there is very little empirical data available for calibrating those models [11]. This work will focus on *the material and current transport properties of heterojunction Esaki diodes on lattice matched and Si substrates* so that the understanding for TFETs and III-V devices as a whole may be improved.

Diode characteristics will be measured electrically to measure tunneling characteristics and push towards a 10 MA/cm^2 current density target. Raman, Hall, and SIMS will be utilized to confirm dopant concentration within the samples. XRD, AFM, and TEMs will be utilized to confirm crystal quality as well as hints to any changes in crystal composition. Combining the aforementioned techniques will provide prime empirical material for model calibration at high carrier concentrations across several non-Silicon heterojunction systems. Proper execution of this project requires multiple epitaxial growths of which a significant number have been or will be obtained through collaboration with Texas State University (TSU) and SEMATECH.

Much of the research of tunneling phenomenon in homo and heterojunction Esaki diodes has involved low to moderately degenerately doped junctions. Investigators have focused more on designing high electron mobility transistors (HEMTs) [12], heterojunction bipolar transistors (HBTs)[13–15] , multijunction solar cells (MJSCs) [16], superlattices (SLs) [17, 18], and short of a small number of researchers, very few have investigated band to band tunneling phenomenon, and far fewer reports exist on tunneling near the limits of dopant solubility. A renewed interest in tunneling phenomenon has arisen with the placement of tunneling field effect transistors (TFETS) [5, 8, 19], and many groups have tried to force CMOS techniques and models to fit the TFET characteristic with varying levels of success [10, 20–25]. Few references

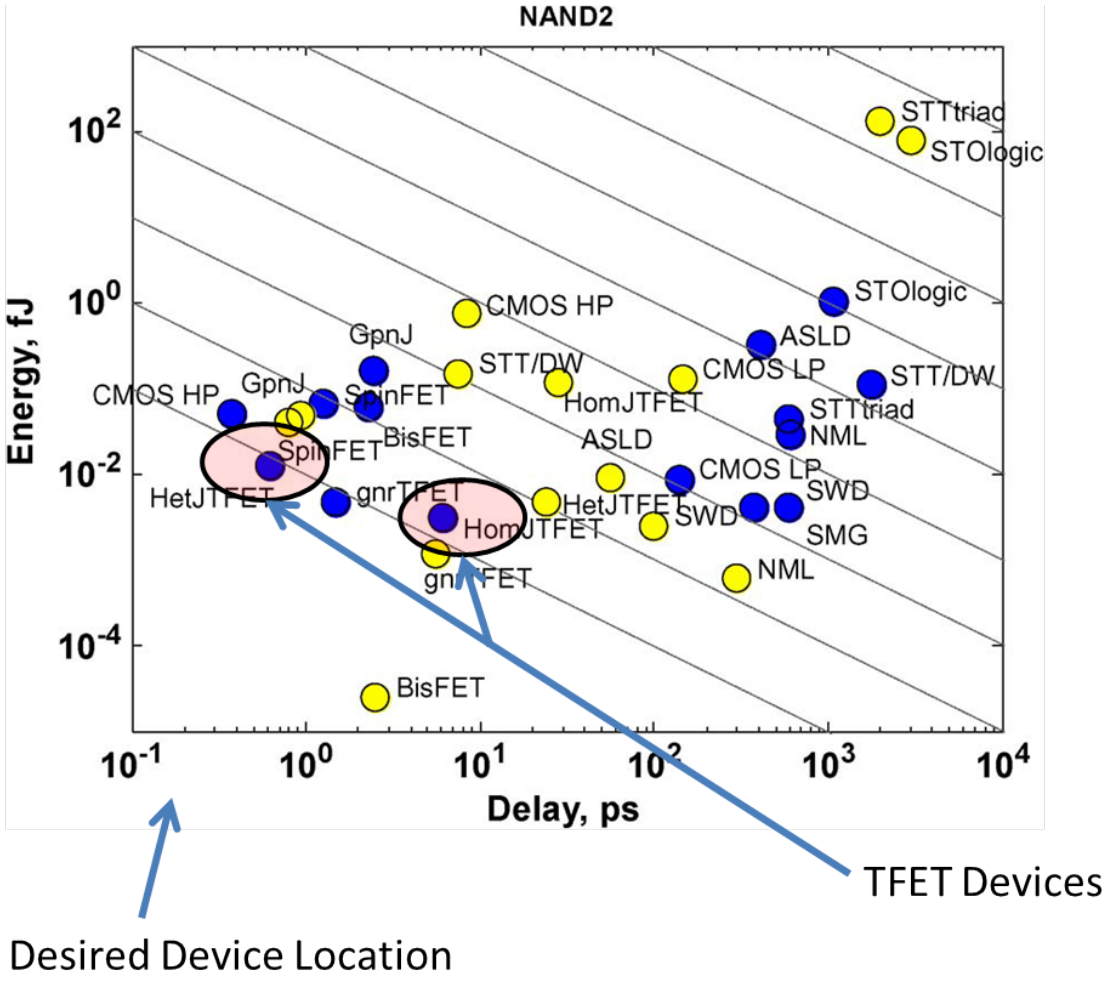


Figure 1.1: Comparing many potential low power logic technologies to each other was done by Nikonov and Young [5] to show if any candidates could compete with advanced CMOS.[1]

for devices characteristics exist that are appropriate for building adequate tunneling models for TFET operation. This work attempts to alleviate this issue by exploring the maximum current density that can be expected of homo and heterojunction tunnel diodes which can, in turn, be applied to TFETs under the most ideal of conditions.

One notable barrier to past research was the limited volume of data on submicron tunneling devices. As current density increases, the device area must be reduced

[1]Reprinted with permission from D. E. Nikonov and I. A. Young, "Overview of Beyond-CMOS Devices and a Uniform Methodology for Their Benchmarking," *Proc. IEEE*, vol. 101, no. 12, pp. 2498–2533, Copyright © 2013, IEEE.

or series resistance will skew the measured data due to a tunnel diode's inherent latching property [26]. Most studies only measured devices in the 100 μm $\times$ 100 μm range, largely due to the ease in probing. Collectively the research group at RIT has managed to implement contact techniques utilized in CMOS to test devices in the sub 100 nm range [27–29].

Esaki diodes are the closest proxy for TFETs relative to how carriers tunnel through the bandgap of two oppositely charged regions [25]. Prior to this work, the record peak current density for any Esaki diode was 975 kA/cm^2 for an $In_{0.53}Ga_{0.47}As$ Esaki diode [28]. This work will demonstrate 3.2 MA/cm^2 for a heterojunction Esaki diode at a lower total doping density. Fig. 1.2 displays the possibility of increased current density for narrow bandgap and heterojunction Esaki diodes as it can be inferred from Day et al. [30] that narrower barriers will exhibit higher J_P. With appropriate levels of dopant, it may be possible to reach 10 MA/cm^2 or greater current density with heterojunction tunnel diodes. However, large doping densities in InAs and InSb homojunctions would likely not yield usable results because their narrow bandgaps, 340 meV and 180 meV respectively [31], are easily overcome by traps and thermal currents thereby creating very large excess currents that swamp out the desired tunneling mechanisms [32]. The nature of broken and staggered gap homojunctions is such that many of the problems of the narrow gap semiconductors may be mitigated or circumvented to create useable devices.

Large differences between on and off current are also important for developing better TFET devices. Presently, most groups have focused on pushing on current; however, little will be gained if the devices built require nearly as much current when in an off state [34]. Knoch and Appenzeller proposed the $Al_{1-x}Ga_xSb/InAs_{1-x}Sb_x$ system as a possibility due to the ability to engineer the band gap without significant impact on lattice constant [35]. Achieving two to three orders of magnitude between the on and off currents would be requisite for a replacement logic device for CMOS.

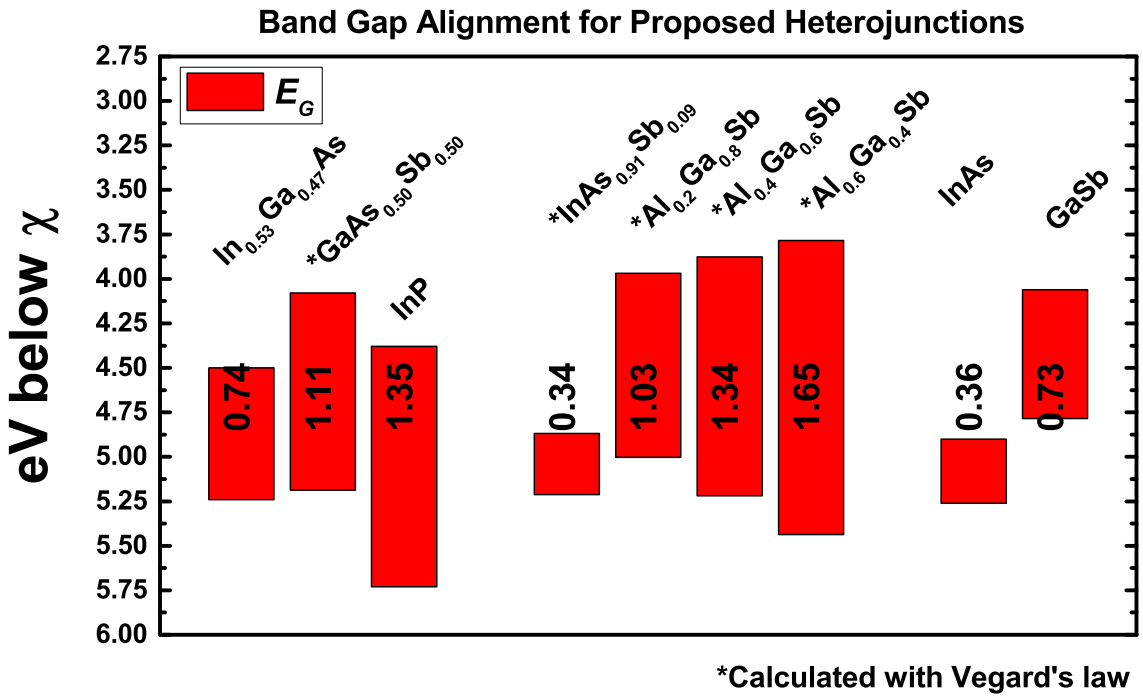


Figure 1.2: Band gap line up for several binary and ternary semiconductors to be used in this work. Ternary compound band gaps were calculated using Vegards rule, and are approximate. A more accurate set of band alignments could be extracted from the band information in Figs. A.1 and A.2 from Vurgaftman et al. [33]

Barriers to III-V device use include the cost and brittleness of the substrates. Direct growth on lattice mismatched substrates offer a solution, but can lead to undesirably large defect densities when done poorly [34]. Virtual substrates will aide in the proliferation of III-V based devices, by decreasing cost and defect density. Presently, a number of devices have been built on GaAs based virtual substrates [36, 37], but fewer are grown on Si based virtual substrates due to defect propagation [38–40]. Aspect Ratio Trapping may provide a convenient avenue for reducing the complexity of III-V on Si growth while also reducing total defect density [41, 42]. Prior ART based devices have performed the same or better than devices grown on native substrates [43–45], but higher mobility devices based on InAs or InP will need to be proven to show the true utility of this epitaxy process.

Electron tunneling in the GaAs/InAs ternary system has been reasonably well defined through the efforts of Kane [46] and confirmed by those of Pawlik et al. [28]

and Romanczyk et al. [27]. However, the tunneling in those systems is solely based on a homojunction model, and, as the InAs data shows, with narrower band gaps come greater excess currents which are ignored by most simple models. Heterojunction tunneling is not well modeled to date, owing to scarce data on staggered and broken (type II and type III) heterojunction data for Esaki type diodes. A fair amount of knowledge is available on heterojunction bipolar transistors (HBTs), super lattice (SL), and Resonant Tunneling Diodes (RTDs), but the characteristics of tunnel and diffusion currents differ in those systems from a simple heterojunction. Techniques such as Raman spectroscopy, X-ray Diffraction (XRD), and low temp (LT) measurements will elucidate the differences between homo and heterojunction Esaki diodes, but much of the data does not exist in the degenerately doped heterojunction space.

Improving current density for tunneling devices has generally been left to just increasing the doping levels. Generally the limit for dopant solubility hovers in the low 10^{20} cm^{-3} range for both n and p dopants across the range of semiconductors covered by this proposal [44, 47]. Dopant activation is an issue near the highest values, which may inhibit the ability of the devices to reach the 10 MA/cm^2 J_P target. Fortunately, other avenues exist for either increasing the dopant density or modifying the epi layers that may push the J_P even further [48, 49]. Work by Collins et al. [50] showed that changes in i-layer design and/or an additional tunnel barrier can increase the throughput current by two to four times the amount exhibited by an abrupt two region diode.

Prior to this dissertation much was unknown about the performance of highly doped Esaki diodes in the heterojunction systems reported. Fig. 1.3 shows the state of the art prior to this work. This figure of merit (FOM) plot will recur throughout this dissertation to show the population of the J_P *vs.* N^* devices.

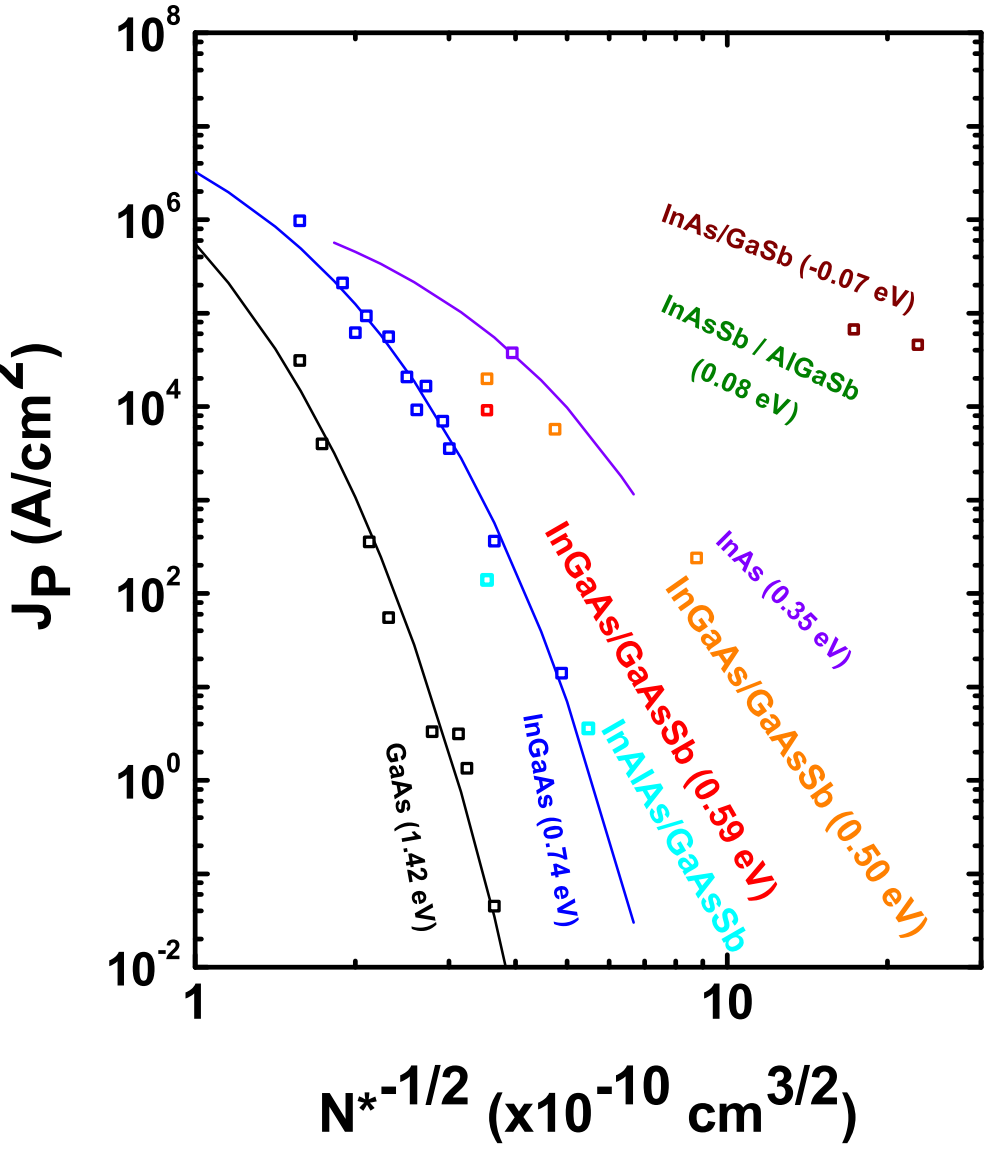


Figure 1.3: The state of the art prior to the work in this dissertation did not include many examples of broken or staggered gap tunnel diodes. Lack of electrical data compounds the difficulties in developing potential TFET systems.

Chapter 2

Esaki Diodes: Characteristics and Applications

2.1 Introduction

Diodes form the very basis of how modern electronics function. Without understanding how the fields of differently charged regions within a material behave, none of computers, phones, televisions, and other modern devices would be possible. This dissertation focuses heavily on a very specific form of diode, the Esaki diode.

This section is intended to aid the reader in how to best interpret the electrical results that are shown in following sections of this dissertation. Sections 2.2 and 2.3 discuss homo and heterojunction diodes as a basis for understanding the materials that will comprise the diodes discussed throughout the dissertation. Section 2 discusses the key theories behind Esaki diode operation. This chapter concludes with section 2.5 which gets to real applications for Esaki tunnel diodes.

2.2 Homojunction Diodes

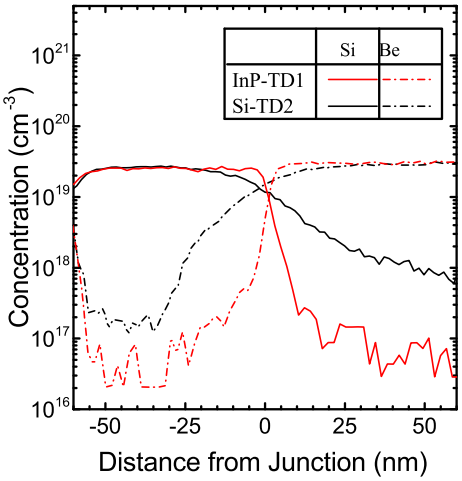
Diode theory is well covered in a number of device physics text books [1, 3, 51, 52], but a brief coverage the of the material is deserved to address the origins of the current during electrical measurements made in this dissertation.

Homojunction diodes consist of p (positive) and n (negative) doped regions of the

same host material, *i.e.* Si, Ge, GaAs, $In_{0.53}Ga_{0.47}As$, etc. For group IV elements, group III and lower elements would dope p-type and group VI and higher would dope n-type. Compound semiconductors are a bit more complicated due to the amphoteric nature of group IV elements exhibiting both p and n-type characteristics, in addition to group II and VI elements. Often, p-n diodes are shown as two distinct blocks of material as per Fig. 2.1(a) with perfectly abrupt junctions. In reality, both dopants diffuse during growth to create the broader junction regions shown in Fig. 2.1(b) where profiles under 5 nm/dec. are considered fairly abrupt.

$In_{0.53}Ga_{0.47}As$: Si (n-type)	$In_{0.53}Ga_{0.47}As$: Be (p-type)

(a) Homojunction Diode representation



(b) $In_{0.53}Ga_{0.47}As$ Homojunction SIMS on InP and on Si

Figure 2.1: (a) Schematic of a diode, generally it is assumed that the profiles are perfectly abrupt. (b) SIMS from an actual "abrupt" diode shows that diffusion of dopants will happen regardless.

Generally, the diodes in this dissertation have abrupt profiles so assumptions for depletion widths are assumed valid. Charge in one region seeks to balance out the charge in the neighboring region causing a region that is depleted of carriers between them. This depletion region, W_D, overlaps both the p and n regions such that the charges are balanced is shown in Eq. 2.1; where N_A is the acceptor doping density, N_D is the donor acceptor density, ϕ_{bi} is the built in potential between n and p regions, q is fundamental charge, and ϵ_S is semiconductor permittivity. For non-degenerate

doped diodes these depletion widths can be near 1 μm, however the material covered in this dissertation is below 10 nm.

$$W_D = \sqrt{\frac{2 \cdot \epsilon_S \cdot \psi_{bi}}{q} \cdot \frac{N_A + N_D}{N_A \cdot N_D}} \tag{2.1}$$

The diffusion current through the diode can be characterized as eq. 2.2. Where J_D is the output current density, J_S is the reverse saturation current density, k is Boltzman's constant, T is temperature in °K, and V_a is the applied voltage.

$$J_D = J_S \cdot exp\left(\frac{q \cdot V_a}{k \cdot T} - 1\right) \tag{2.2}$$

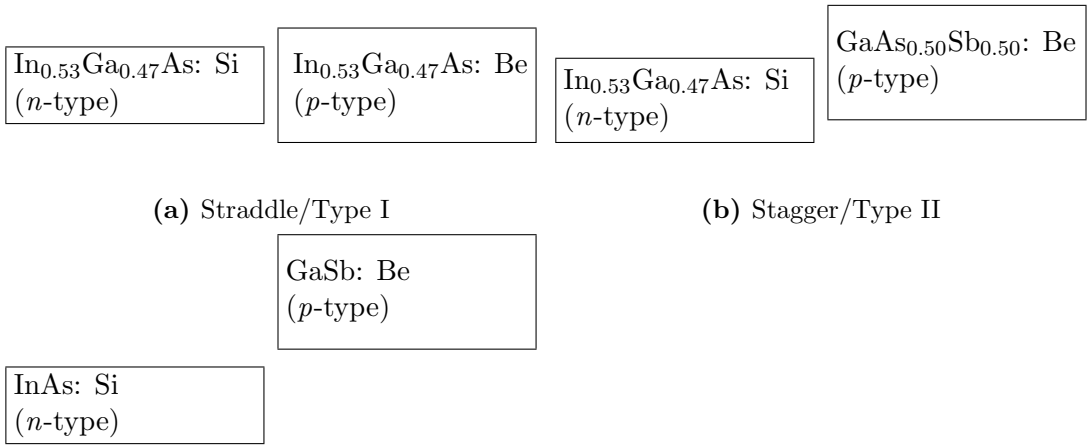
While the above equations work for homojunction diodes, the devices in this dissertation consist of degenerately doped heterojunction diodes and the equations above require adaption to apply in that space. Characteristics for the homojunction diodes are largely static; E_G changes with temperature [53] but exists as a barrier to carrier transport. However, sandwiching different materials together can result in changes to E_G and affects many characteristics of diode function.

2.3 Heterojunction Types and Diodes

Much of this dissertation involves heterojunctions. Basic characteristics of heterojunctions are often described in device phyics texts, *i.e.* Neamen [1], Sze [3, 52], and Streetman [51]. Specifically, a semiconductor heterojunction is the adjoinment of two separate semiconductors such as Si and Ge. The same physical processes that apply to homojunctions also apply in heterojunctions, but additional care is required in the book keeping to calculate W_D and J_D.

First, the differences in E_G, E_C, and E_V must be addressed. Heterojunctions will have an offset between the valence and conduction bands of the constituent

materials. There are three types of band offsets which are shown conceptually in Fig. 2.2. Type I, or straddled, offsets occur when both the valence and conduction bands for one material fall in between those of the neighboring material, *e.g.* the Si/Ge and GaAs/InGaAs systems [52]. Type II, or staggered, offsets are aligned such that there only one band from each material falls between the valence and conduction bands of the other. A number of type II systems have been reported, combinations of $In_{0.53}Ga_{0.47}As/GaAs_{0.50}Sb_{0.50}$ [54] and $Al_{0.40}Ga_{0.60}Sb/InAs_{0.91}Sb_{0.09}$ [55, 56] have been reported. Whereas type III, or broken, offsets have no overlap of E_G for either material. The InAs/GaSb system is probably the most well documented type III junction [57].



(a) Straddle/Type I

(b) Stagger/Type II

(c) Broken Gap/Type III

Figure 2.2: Conceptual diagrams of heterojunction diodes without taking into account junction effects are shown above. (a) In straddled/type I heterojunctions both the valence and conduction bands of one adjoining material fall between those of the other material, *e.g.* the Si-Ge heterojunction system. (b) In stagger gap/Type II heterojunctions only one of the bands for the adjoining materials falls between those of the other, *e.g.* $In_{0.53}Ga_{0.47}As/GaAs_{0.50}Sb_{0.50}$. (c) Broken gap/Type III heterojunctions have no overlap of adjoining materials' bands, *e.g.* InAs/GaSb.

The electron affinity rule is an acceptable approximation for conduction band alignments utilizing the electron affinitiy, χ, of both materials. Assuming that the

vacuum level for all electrons is the same across all semiconductors. In many cases the electron affinity rule is invalid [58], but for the purposes of describing heterojunction interactions it proves to be adequate.

Considering a type I heterojunction, Fig. 2.3 shows how to treat the changes in E_G due to the different materials. W_{D1} and W_{D2} consist of the depletion region on either side of the junction and are represented by Eq.2.3 and Eq. 2.4 are modifications of Eq. 2.1. In this case the subscripts 1 and 2 indicate which semiconductor parameter to use.

$$W_{D1} = \sqrt{\frac{2N_{A2}\epsilon_{S1}\epsilon_{S2}(\psi_{bi} - V_a)}{qN_{D1}(\epsilon_{S1}N_{D1} + \epsilon_{S2}N_{A2})}} \tag{2.3}$$

$$W_{D2} = \sqrt{\frac{2N_{D1}\epsilon_{S1}\epsilon_{S2}(\psi_{bi} - V_a)}{qN_{A2}(\epsilon_{S1}N_{D1} + \epsilon_{S2}N_{A2})}} \tag{2.4}$$

From Sze [3], this type I heterojunction J_D can then be modeled similarly to the homojunction diode by combining J_n and J_p, where L_x and D_x represent the Debye length and carrier diffusion coefficients for their respective material as shown in Eq. 2.5:

$$J_D = J_n + J_p = \left(\frac{qD_{n2}n_{i2}2}{L_{n2}N_{A2}} + \frac{qD_{p1}n_{i1}2}{L_{p1}N_{D1}}\right)\left(\exp\frac{qV_a}{kT} - 1\right) \tag{2.5}$$

Notably, ΔE_C and ΔE_V are not present in Eq. 2.5. Assumptions were made with respect to junction abruptness to simplify the quantum well seen by holes as mentioned in Sze [3]. For type II and type III heterojunctions a similar simplification may not be necessary since the nature of band overlaps is such that it tends to minimize barriers to conduction.

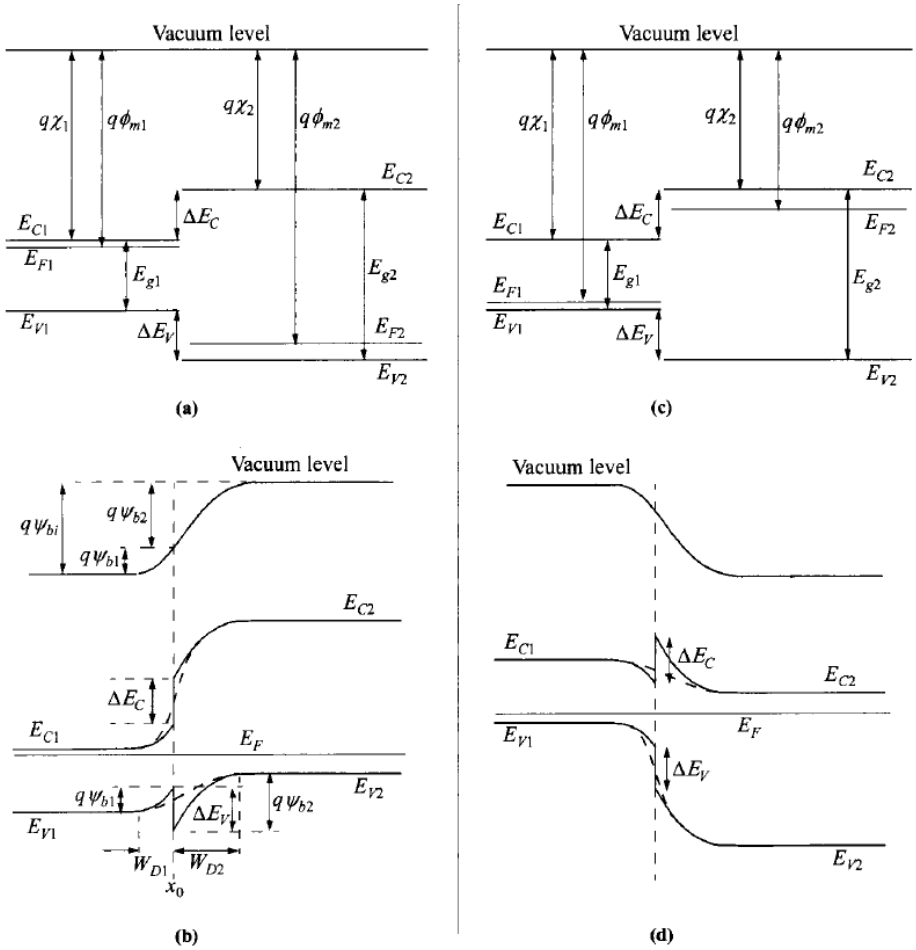


Figure 2.3: This figure, adopted from Sze [52], shows many of the aspects that must be considered in a heterojunction.

2.4 Esaki Diodes

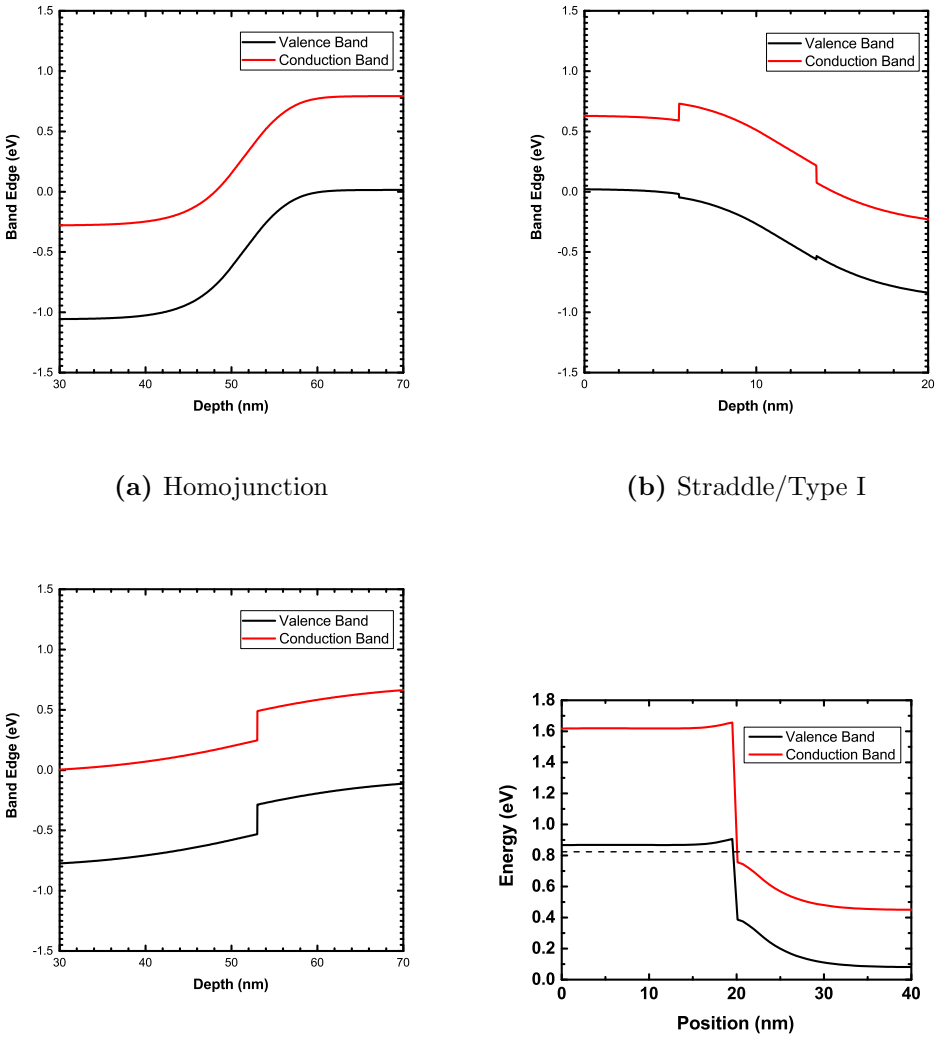
When a diode is heavily doped such that both the n and p sides are degenerate, a special case emerges where quantum mechanical tunneling can occur across the band gap due to an overlap of the valence and conduction band Fermi positions. This case is called the Esaki diode, named after Leo Esaki who first discovered them in 1958 [59]. Esaki tunnel diodes (ETDs) are known to have zero breakdown voltage as well as a region of negative differential resistance (NDR) between the peak current, I_P, and valley current, I_V.

Much of the recent interest in Esaki diodes has focused on applications to tunneling field effect transistors (TFETs) [6, 8, 9, 22, 28, 60–62]. However, Esaki diodes have a number of applications in photovoltaics (PVs)[54, 63], light emitting devices (LEDs), and in heterojunction bipolar transistors (BJTs)[64–67]. Esaki diodes were heavily reasearched in the late 50's and 60's, but were built utilizing alloying techniques.

2.4.1 Theory

The degenerately doped junctions for Esaki diodes cause an overlap of E_C and E_V as seen in the representations in Fig. 2.4 of each junction type. Because the potential barrier has a width below 10 nm quantum mechanical tunneling can occur across E_G for holes and electrons. This tunnel current causes a rapid increase in I that greatly exceeds the contribution from diffusion. This dissertation measures the tunneling characteristics of Esaki diodes consisting of each of the arrangements shown in Fig. 2.4. Relative to a homojunction Esaki diode, Fig. 2.4(a), type II and type III Esaki diodes, Figs. 2.4(c) and 2.4(d), are expected to have a higher J_P for a given N^*. Type I Esaki diodes can create large effective tunnel barriers which will lower J_P relative to a homojunction Esaki.

Fig 2.5 from Fig. 3 in Sze [52] depicts the various operation modes of an Esaki



(a) Homojunction

(b) Straddle/Type I

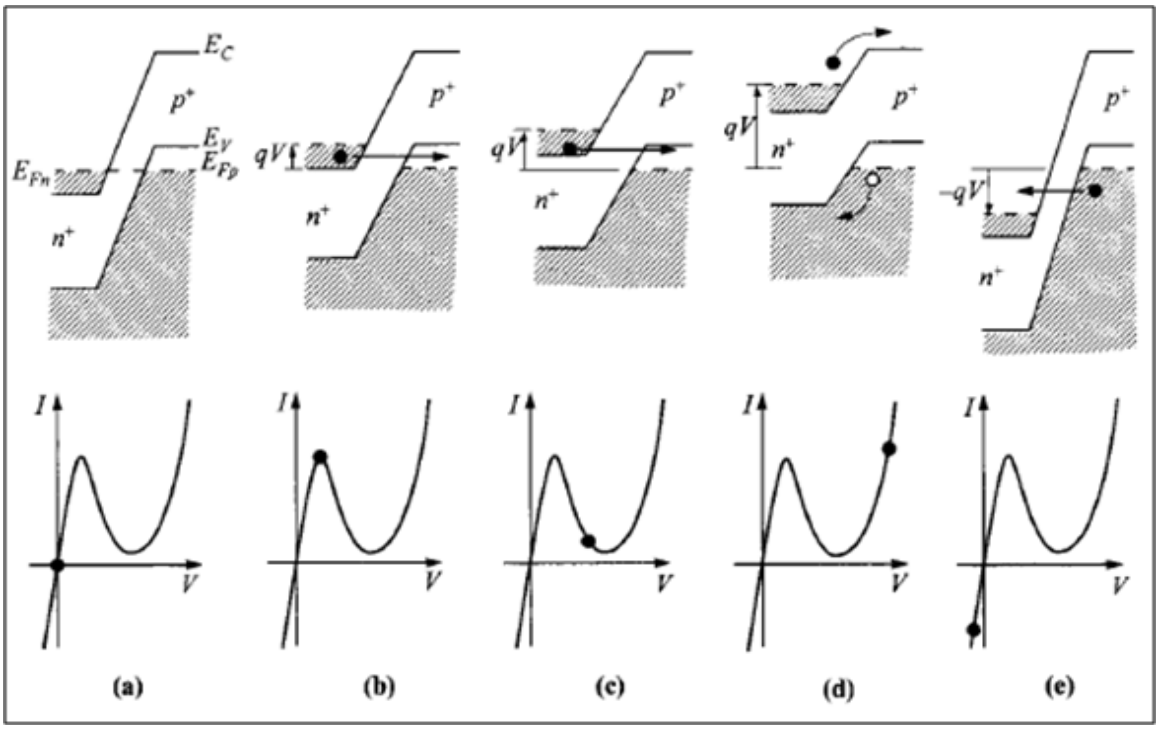
(c) Stagger/Type II

(d) Broken/Type III

Figure 2.4: (a) Band bending for an $In_{0.53}Ga_{0.47}As$ Esaki diode showing the overlap of the valence and conduction bands.(b) Many heterojunctions fall into the straddled/type I category. Esaki diodes made from this system can exhibit reduced J_P due to an effective widening of the tunnel barrier. (c) Staggered gap diodes would provide for a narrower tunnel barrier, which should increase J_P for a given N^*. (d) The broken gap should create the thinnest barrier to tunneling and allow for very high J_P.

diode. Similar to the representations in Fig. 2.5(a), at 0 V bias the diode is in thermal equilibrium and the electrons and holes tunnel back an forth freely. However, once a small bias has been applied electrons will tunnel into the valence band until a peak is reached at the maximum overlap of the valence and conduction band Fermi

levels as seen in Fig. 2.5(b). Beyond this peak, the overlap is further separated at increasing bias until the tunnel current is quenched at the minimum called the valley in Fig. 2.5(c). After the valley, thermal diffusion currents dominate and the *I-V* plot follows more closely to an ideal diode in Fig. 2.5(d). Under the reverse bias scenario, the bands are forced farther apart and Zener tunneling occurs in Fig. 2.5(e). The Zener direction is the area of interest for TFET operation [8, 9, 61].



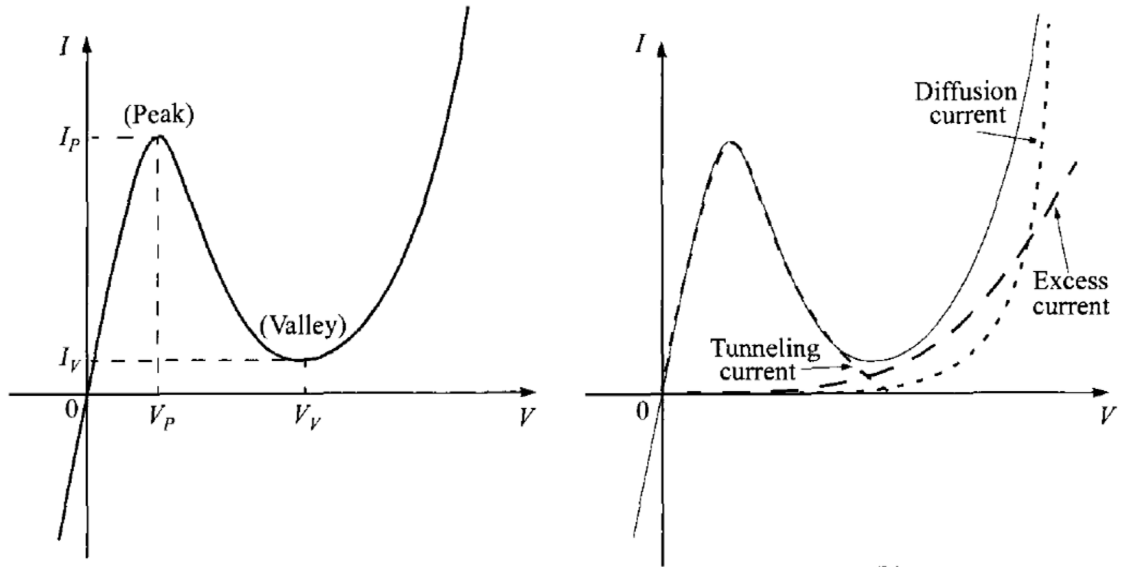
From K. K. Ng and S. M. Sze, *Physics of Semiconductor Devices (3rd Edition)*. Copyright © 2006 by John Wiley & Sons, Inc. Reprinted with permission of John Wiley & Sons, Inc.

Figure 2.5: Sze [52] described the operational modes of an Esaki diode at (a) zero bias, (b) peak, (c) valley, (d) diffusion, and (e) reverse bias conditions.

Esaki diodes have a very distinct *I-V* characteristic curve. Current in these diodes is actually a combination of several current sources as seen in Fig. 2.6(b). Tunnel current/current density is due to tunneling of conduction band electrons into valence band sites. The distinct peak in the *I-V* curve occurs when the greatest overlap of the valence and conduction band occurs. As the diode is biased further the band overlap lessens and the tunneling current begins to diminish. The confluence of excess

current, I_E, and tunneling current, I_T, is called the valley current, I_V, after this point I_E dominates the contribution to overall current. I_E is the combination of all sources of current which are not diffusion or tunnel current. There can be multiple sources of I_E, *e.g.* traps, crystalline defects [68], and surface effects. Without I_E, the I_V would occur when diffusion current, I_D, overtakes I_T as the larger current source. I_D becomes the dominate current contributer once the turn on voltage for that diode material is reached. Considering current over area, Eq. 2.6 describes the contributions of the different current sources to the overall current density of the diode. J_{Esaki} represents the total current density, J_T is the tunnel current contribution, J_E is the excess current contribution, and J_D is the diffusion current density. J_{Esaki} will be discussed further in section 2.4.3. J_E can often be broken down into smaller units with low temperature I-V measurements as seen with the "hump" currents discussed by Chynoweth et al. [69] and Holonyak and Lesk [70].

$$J_{Esaki} = J_T + J_E + J_D \tag{2.6}$$



(a) **(b)**

Figure 2.6: Sze [52] described (a) the two primary I-V characteristics of an Esaki diode, I_V and I_P, and (b) the contribution of tunnel, excess, and diffusion current to the characteristic curve of an Esaki diode.

2.4.2 Data Extraction from Esaki Diodes

Esaki diodes have some very characteristic behavior. Fig. 2.7 illustrates several of the key concepts to understand when measuring Esaki diodes. First there are typical I-V curves, as seen in Fig. 2.7(a). On an I-V plot there are several regions to consider. First, there is the Zener tunnel region in the reverse current direction. Zener tunneling is utilized by TFETs and can be shown to have an emprical relationship to I_P. In the forward current direction, there are the peak and valley current and voltage (I_P, I_V, V_P, V_V) shown in Fig. 2.7(a). The peak to valley ratio is taken from I_P and I_V as seen in Eq. 2.7. For a given device, J_P will be constant regardless of the R_S between the diode and the ground contact. V_P will shift lower with reduced R_S as seen in Fig. 2.7(b); however, the locations of V_P and V_V will shift closer and higher with increased R_S. At high enough R_S values a latching effect can be observed between V_P and V_V as discussed by Hao and Seabaugh [6] and Sudirgo [26] for use in tunneling SRAM devices.

$$PVCR = \frac{I_P}{I_V} = \frac{J_P}{J_V} \tag{2.7}$$

This dissertation focuses on maximizing peak tunnel current density, J_P, as it is the single most important factor for a TFET to compete with low power CMOS[71]. Most studies have relied on the mask defined area to calculate J_P, which is adequate for devices over 400 μm^2 due to the relatively small reduction in area during mesa formation. However, for submicron devices a different scheme becomes necessary as the ratio between metal and mesa can be nearly 9:1 as seen in Fig. 2.7(c). Such differences between mask size and device area necessitate an area correction to provide appropriate J_P estimates. Several different methods have been utilized to increase the precision of the area used for J_P calculations, *e.g.* planar fit [28], mean area [72], and adjusted mean [27]. Mean area requires the least amount of time but also has

the greatest device variation, whereas the planar fit method requires significant time investment whilst providing minimal device variation.

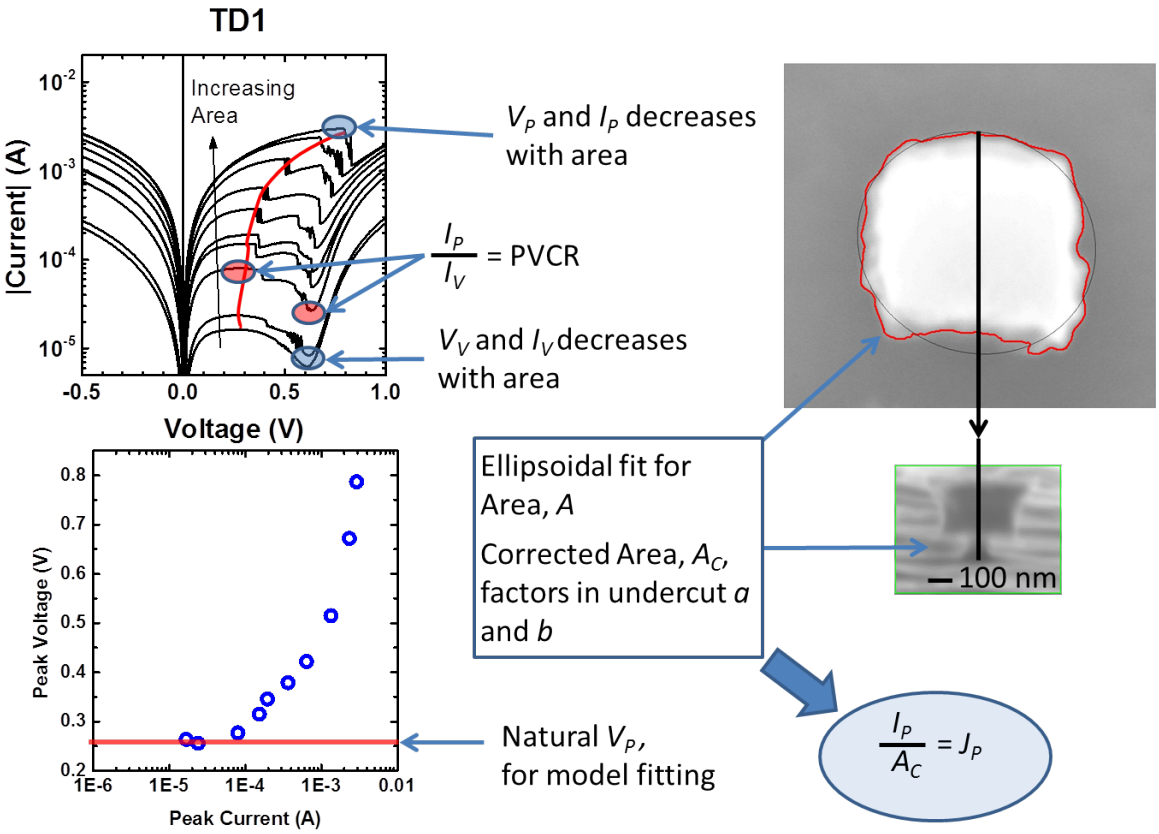


Figure 2.7: Utilizing sample SSG-TD1 an example, keys concepts for understanding Esaki diodes are shown above. a. I-V characteristics for SSG-TD1 as devices are scaled down with area, I_P, I_V, V_P, and V_V, are all every apparent for each discrete device. R_S influence is reduced with area, and eventually V_P will reach a minimum value. J_P is calculated from the corrected device area and I_P. PVCR is calculated from I_P and I_V

Also of importance for this work, is the knowing the doping density for a given device. Drift in the growth pattern can affect device performance despite utilizing the same growth parameters. A few such instances will be exhibited later in this work. Therefore, to more accurately determine the performance of material system, the total doping density must be measured. As seen in Fig 2.8, a technique known as secondary ion mass spectroscopy (SIMS) can be utilized to measure the total dopants in the target material. From which, N^* can be calculated by taking half the harmonic average of the dopants per equation 2.8:

$$N^* = \frac{N_D N_A}{N_D + N_A} \tag{2.8}$$

While there are some limitations to the technique, this measurement provides valuable data on doping density which can then be combined with the measure J_P and plotted against other tunneling devices as shown in Fig. 2.8. In addition to N^*, the abruptness of the junction can be measured with SIMS. Because Esaki tunneling between the bands has a field component, a broader dopant profile between regions results in a lower built-in field strength. Lower field strength causes a lower J_P than would otherwise be expected for a diode at a given N^*.

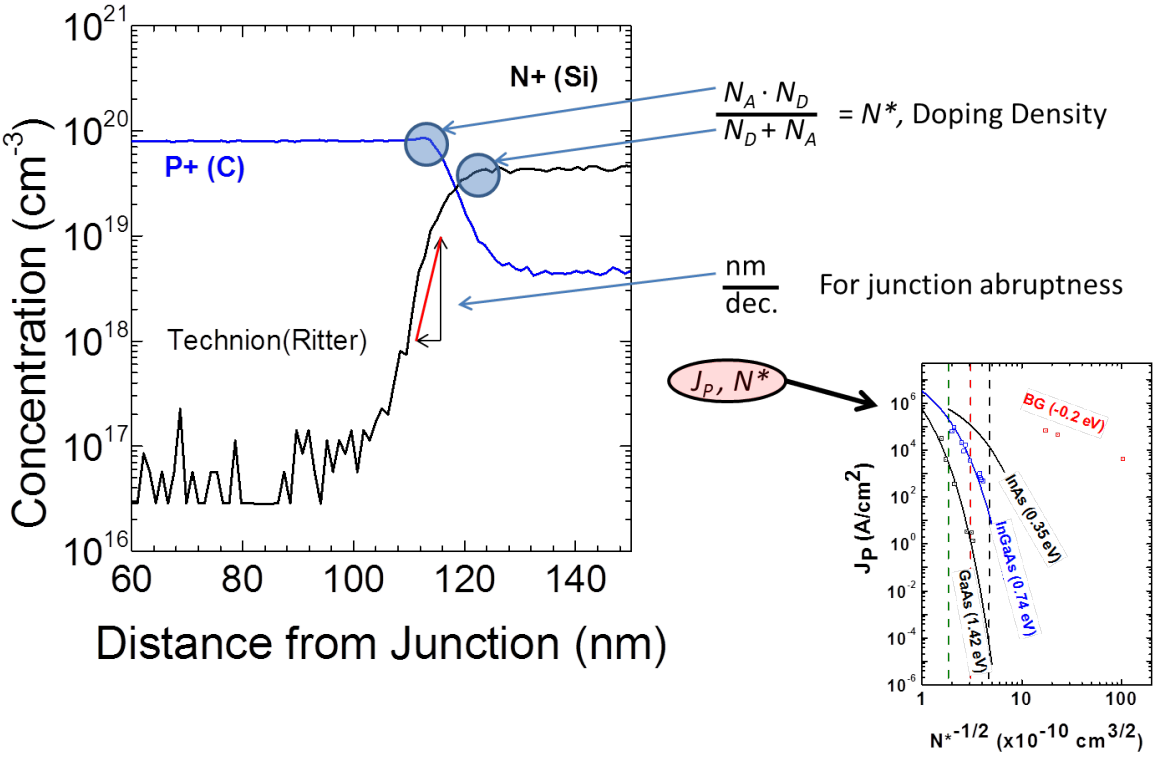


Figure 2.8: Utilizing a homojunction Esaki diode an example, keys concepts for understanding the diodes are shown above. a. SIMS provides data on the actual doping levels contained within the sample. These concentrations are utilized in the calculation of N^* in Eq. 2.8. Additionally, the abruptness of the junction can be measured to explain variations from expected performance. b. Taking the doping density and plotting it *vs.* J_P provides a means for comparing devices of different materials.

For the purposes of this dissertation, J_P, J_V, PVCR, V_P, and N^* will be the primary characteristics used to compare devices. J_P and N^* are necessary to determine if devices based on the tunnel junctions presented in this work can meet the current requirements proposed by industry [4, 5].

2.4.3 Tunnel Models

Models such as Kane [46, 73, 74] and Schenk [75] can be used to predict tunneling current in homojunction Esaki diodes with fairly excellent accuracy [62]. However, in the case of heterojunction Esaki diodes this is a more complicated combination to model, but the Kane model [46] in Eq. 2.9 is useful for explaining the tunneling mechanisms at play. Material differences in the adjoining material systems such as dielectric constant, density of states (DOS), band gap alignment, the interface terminations of the two regions, and many more considerations need to be made for modeling. While Bastard [76], Bastard et al. [77] has had some success in modeling heterojunction Esaki diodes by treating the overlap integrals separately, the modeled current characteristics are approximate at best. In addition to differences in carrier effective mass, there are hybrid bands, susceptibility, strain, atomistic simulations such as NEMO or OMEN could possibly perform this task [11].

$$J_T = \left(\frac{q^2}{36\pi\hbar^2}\right) \cdot \sqrt{\frac{2m^*}{E_G}} \cdot D \cdot E \cdot \exp -\frac{\pi\sqrt{m^*}E_G^{\frac{3}{2}}}{2\sqrt{2}\hbar} \cdot \frac{1}{E} \tag{2.9}$$

While the Kane model is limited to two parabolic bands in a homojunction and deriving a relation for J_T in heterojunctions is beyond the scope of this dissertation, this model is sufficient for discussing where improvements may be made to increase J_T. In Eq. 2.9 [46, 62] m^* is the reduced effective mass of both carriers, E is the electric field between n and p regions, D is the overlap integral of the valence and conduction bands, and the remaining components retain standard values. Immediately, it becomes apparent that reducing E_G will greatly affect tunneling and that m^* will play a role to a lesser extent. Prior work had shown the validity of this hypothesis [62] for homojunction systems. Heterojunctions will require a different mathematical treatment, but the reduced E_G due to type II and type III heterojunctions implies that significant gains in J_T may be made with the correct combination of materials.

2.5 Applicable Fields

2.5.1 Tunneling Field Effect Transistors (TFETs)

Much of the recent interest in Esaki tunneling has been related to building better TFETs [6]. While Si CMOS has the benefit of 50+ years of research in understanding how to build devices, TFETs have a much shorter history [6]. Understanding the maximum tunnel currents for a majority of the device systems is largely unknown. This dissertation analyzes how the effective band gap for $In_{0.53}Ga_{0.47}As/GaAs_{0.50}Sb_{0.50}$, $InAs_{0.91}Sb_{0.09}/Al_{0.40}Ga_{0.60}Sb$, and InAs/GaSb material systems affects the J_P *vs.* N^* relationship discussed in Pawlik [62]. This work also examines how tunneling devices are affected by defects by placing them onto lattice mismatched substrates.

TFETS are *p*-*i*-*n* diodes that have gated the *i*-layer to make the device operate like an Esaki diode. Typical designs have been vertical structures like that of Dewey et al. [8], Romanczyk [9], Bijesh et al. [61] in Fig. 2.9. To design the parameters for these devices an Esaki can be viewed as the device in the on state whereas the *p*-*i*-*n* can be considered the offstate for the the device. There are several design issues associated with this approach related to the gate placement. Gating sidewalls for the devices and isolating the source or drain have proven to be challenge [9, 78], as gate overlap can impact the tunneling characteristics. However, as with the implementation of finFETs, solving the gating solution will be a matter of time [6, 8, 61].

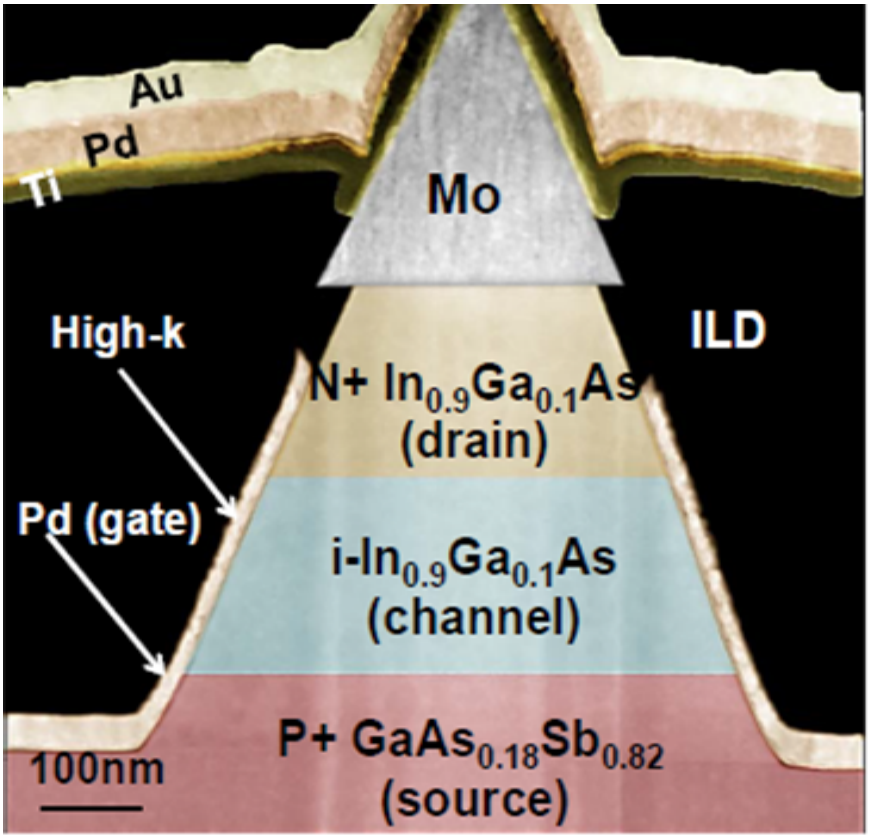


Figure 2.9: A TEM micrograph of a BG TFET presented by Bijesh et al. [61] presents the typical approach to TFETs, a vertical p-i-n structure with gated sidewalls.

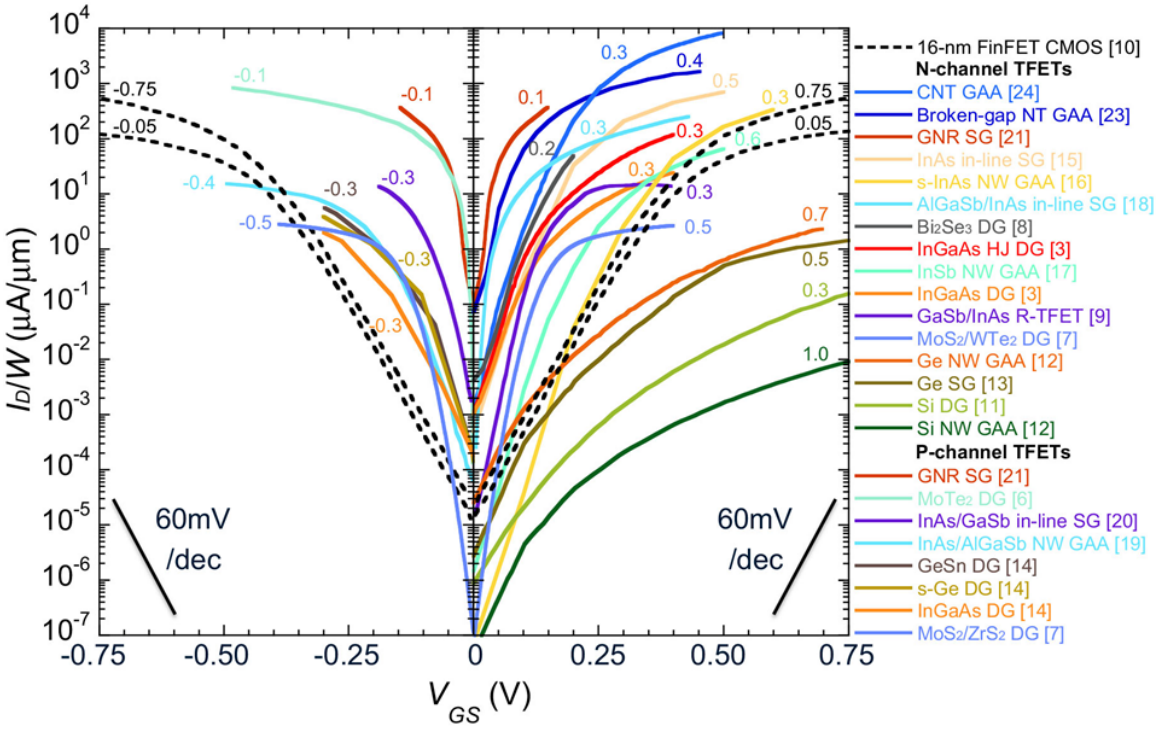


Figure 2.10: From Hao and Seabaugh [6], State of the Art for TFETs as of 2014. Often devices will beat SS, but be low in I or vice versa.

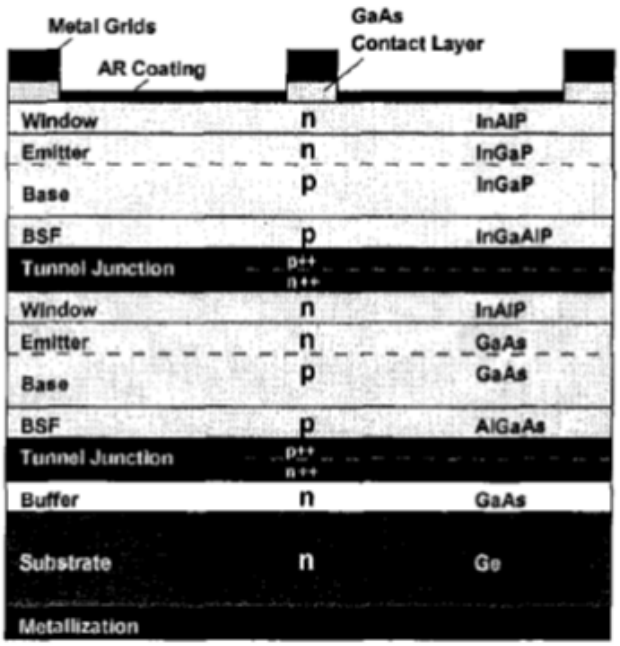


Figure 2.11: Example of tunnel junctions as contacts in multijunction solar cells from Miller et al. [92].[1]

2.5.2 Photovoltaics (PVs)

Solar cells, also commonly referred to as photovoltaics (PVs), often rely on highly doped contact regions in multijunction solar cells (MJSC) [16, 30, 54, 63, 79–92]. These cells look to use lattice matched materials with successively narrower band gaps to capture the AM1.5 spectrum [93]. Tunnel junctions provide the low resistance contact between the junctions that comprise the solar cell as seen in Fig. 2.11. This work may benefit the community by providing empirical data for determining how the heterojunction current characteristics will behave with doping.

[1] Reprinted with permission from D. L. Miller, S. W. Zehr, and J. S. Harris Jr, "GaAs-AlGaAs TUNNEL JUNCTIONS FOR MULTIGAP CASCADE SOLAR CELLS," *Journal of Applied Physics*, vol. 53, no. 1, pp. 744–748, 1982. Copyright © 1982 by American Institute of Physics

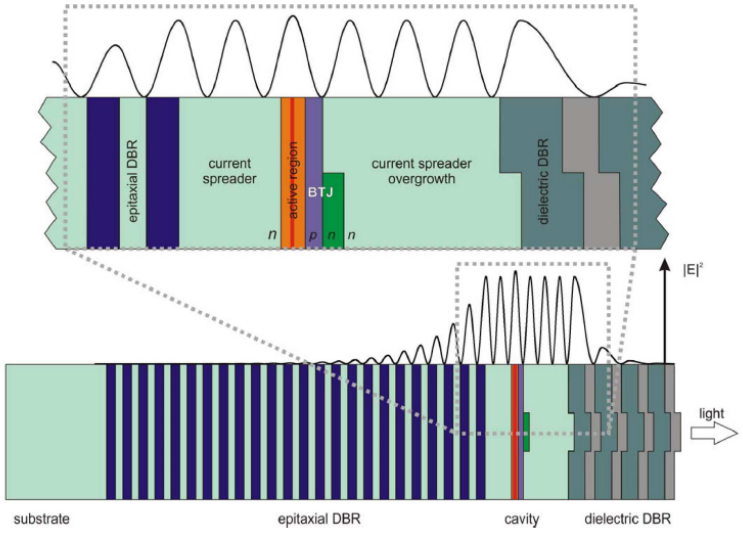


Figure 2.12: Example of tunnel junctions in a VCSEL [97]

2.5.3 Lasers/Light Emitting Diodes (LEDs)

Similar to PVs, Lasers and LEDs utilize degenerately doped contacts to reduce resistance in the system. Optimal design of the contact allows for improved light emission and quantum efficiency of the devices. A number of GaAs-based [94], InP-based [45, 95, 96], and GaSb-based [97, 98] Vertical cavity surface emitting laser (VCSEL) designs rely on Esaki tunnel junctions to contact the active device region. Understanding the output current at a various effective doping levels may prove helpful for improved VCSEL designs. Similarly, multiple LED based on GaN [99–102], GaAs [103–106], GaSb [107–109], and BeTe/ZnSe [110] rely on Esaki tunnel junctions for improved efficiency and performance characteristics.

2.5.4 Heterojunction Bipolar Transistors (HBTs)

Series resist ance in the collector of Heterojunction Bipolar Transistors (HBTs) can significantly reduce the gain. A number of groups have utilized Esaki diodes as a means of mitigating these effects [64, 66, 67, 111–113]. In these devices the HBT performance had limits related to the J_P of the included Esaki diode. This work has

applicable benefits for device designers, in that there will now be information, across a range of effective doping densities, for multiple heterojunction systems.

2.6 Esaki Diode Applications and Characteristics Conclusion

This chapter discussed the basics of homojunction and heterojunction diodes and how they apply to Esaki diodes. Additionally, the basic principles of Esaki diode operation were discussed with an emphasis on J_T, which is the primary parameter studied in this dissertation. Applications for Esaki diodes were then discussed to emphasize the broad impact that this work may have across multiple research topics.

Chapter 3 will explore the various electrical and materials analysis techniques to be used in this dissertation. And the following chapters will then explore the implications of stagger and broken gap heterojunctions on J_T as well the impact of defect density on tunneling performance.

Chapter 3

Growth and Materials Analysis Techniques

This chapter is designed to cover the various material growth and characterization techniques that are used to build and evaluate the devices presented in this dissertation. Sections 3.1.1 and 3.2 cover the growth methods and considerations necessary to fabricate the Esaki diodes studied in this work. The remaining sections cover the analysis techniques utilized in this work, *e.g.* SEM, TEM, XRD, AFM, *I-V*, and device fabrication and characterization. The purpose of this chapter is to outline how the devices are to be evaluated and identify sources for deviations from expected results.

3.1 Growth Methods

3.1.1 Molecular Beam Epitaxy (MBE)

This dissertation relies heavily upon molecular beam epitaxy (MBE) to build device layers on a variety of substrates. Fig. 3.1 from Pohl [114] provides a representative schematic of a MBE system. These chambers require ultra high vacuum (UHV) pressure levels $\approx 10^{-9}$ torr to produce high quality epitaxial films. Typically there will be a load lock to maintain system pressure and to reduce contamination when a sample is loaded for growth. Effusion cells are heated and deposition rates are controlled by temperature and a shutter, for example two different cell temperatures would provide

a higher level of doping for the warmer setting. Often the growth is monitored by reflection high energy electron diffraction (RHEED) ensure proper crystal structures are formed. Depending on the material grown, the doping concentrations and crystal structure can be confirmed through Hall measurements and/or XRD.

Many of the devices in this work are grown in the reactors at Texas State University. Because of the varied nature of the heterojunctions and limited effusion cell space per chamber, several different chambers will be utilized.

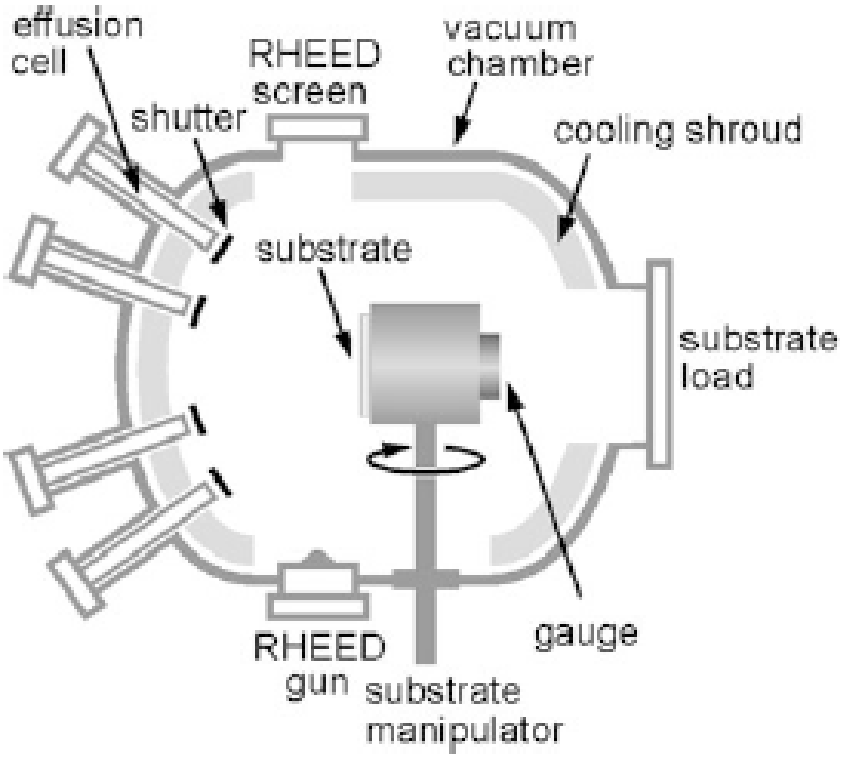


Figure 3.1: This schematic from Pohl [114] represents a standard MBE system. Substrates are located such that the deposition rates from the effusion cells can be calibrated to reach target composition and doping levels in the grown film.[1]

3.1.2 Other growth methods

Devices in this dissertation will be grown by MBE; however a number of other techniques exist for growing tunnel junctions, each with benefits and drawbacks. His-

[1] *Epitaxy of semiconductors: introduction to physical principles*, 2013, p. 301, Molecular Beam Epitaxy, U. W. Pohl, Fig. 7.21, © 2013. With permission from Springer Science+Business Media.

torically, alloy junction growths were used to form tunnel junctions. This technique utilizes a contact containing high concentrations of a dopant. Subsequently, temperature is increased to the Eutectic point forming a degenerately doped alloy junction with the substrate. The very first Esaki diodes were all grown via alloyed junctions [59, 69, 70, 115]. Alloy junction formation is a form of liquid phase epitaxy (LPE). LPE which relies on a furnace to heat the constituent materials to melting where they can then be grown on the substrate surface such as with the sliding boat system [114]. Finally, there is metal organic chemical vapor phase epitaxy (MOVPE), or metal organic chemical vapor deposition (MOCVD) depending on the author, which forms epitaxial layers through surface reactions of precursor gases on the substrate. MOVPE can operate at higher pressures than MBE, but also requires slightly higher growth temperatures which can lead to slightly broader junction profiles and may also require an anneal to remove residual H and other gases that may have been trapped during growth [44, 116, 117]. While a number of other tunnel diodes have been grown using the aforementioned techniques, this work focuses on growths by MBE.

3.2 Heterointegration

3.2.1 Lattice Mismatch

Due to the nature of atoms within crystalline materials, there are a variety of lattice types and sizes that result. Generally group IV and III-V crystals form face centered cubic (FCC) lattices, though other hexagonal and tetragonal lattices may form when atom sizes are small or paired with partners that are significantly larger.

$$t_c = b\frac{(1-\nu\cos^2\alpha)}{8\pi|f_0|(1-\nu)\sin\alpha\cos\beta}ln\left(\frac{\rho\cdot t_c}{b}\right) \tag{3.1}$$

These size differences between crystals cause a strain on the lattice that must be relieved beyond a critical thickness, represented in 3.1 from Pohl [114]. Where t_c

represents the critical thickness for the grown material, b is the absolute value of the Burgers vector $\mathbf{b}$, ν is the Poisson ratio, α is the angle between the Burgers vector and the dislocation line vector, β is the angle between the interface glide plane of the dislocation, f_0 is the natural misfit, and ρ is the strain energy of the dislocation.

Such thicknesses become problematic for mismatches much over 1%, beyond that many materials will relieve stress quickly and cause a highly defected region of material. Screw, dislocation, and threading defects are commonly caused by differences in the lattice constant of crystals [114, 118].

A few techniques have evolved to address issues related to pairing lattice mismatched materials. Perhaps the simplest in concept is the use of a buffer layer, where a thick sacrificial layer is grown of either the target material or a material graded to match both the host and target crystals [12, 36]. Buffer grown materials will constitute the majority of the work covered in this document are more detailed in next section. Aspect ratio trapping (ART) is a technique that was recently developed to reduce defect density in lattice mismatched films [41, 119]. ART utilizes deep dielectric trenches and selective growth to terminate defects prior to reaching a coalesced region that is grown above the trench walls. Some devices in this work will utilize ART. One additional method worth noting is delamination and reapplication to another substrate, this process has been successfully been used to integrated InP based HBTs and other devices onto a Si substrate.

3.2.2 Metamorphic Buffer

An approach utilized to reduce growth and lattice mismatch related defects has been to create a large buffer region of metamorphic material to join the device region to the host substrate. Total defect density is related to the overall thickness of the buffer region, but there are diminishing returns much beyond 1 μm of grown material.

Reasonably high quality devices have been built on substrates utiizing such buffer

layers. Hill et al. [120] and Lau et al. [12] have built transistors utilizing a buffer to demonstrate the potential for integration on Si. From Fig. 3.2 it can be seen how defects could affect device performance. Some systems are largely vertical in the current transport, but any that would need to cross defect boundaries can be expected to suffer.

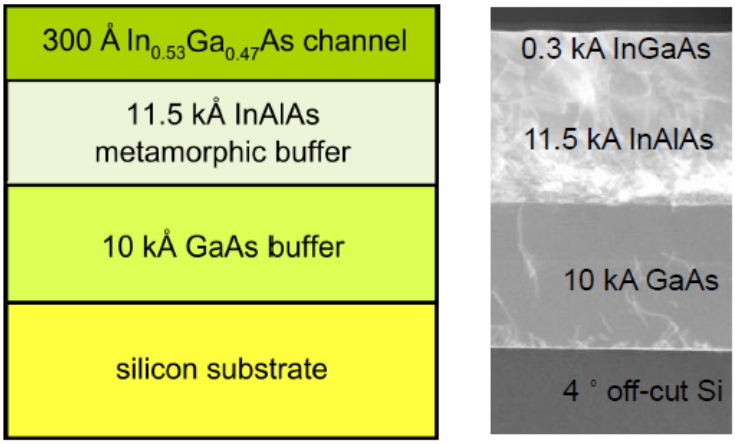


Figure 3.2: Much research has focused on reducing the total number of defects that reach the surface and active regions [120]. The TEM above exhibits defect reduction towards the active region at the substrate surface.

3.2.3 Aspect Ratio Trapping (ART)

Aspect ratio trapping was developed by Li et al. [121], and has been successfully applied to Ge [41, 42, 122, 123], GaAs [43, 119, 121], and InP [124] based systems. Most other methods of heterointegration suffer from defects that propagate upwards through the grown regions. ART allows for a reduction of such defects by trapping many of them against dielectric trench walls which are several times the critical thickness in height.

<100> Si substrates are utilized to produce ART. An oxide is grown on the Si surface to form the trench wall material, though other dielectrics have also been proposed. Threading dislocations originate near the interface of the Si and virtual

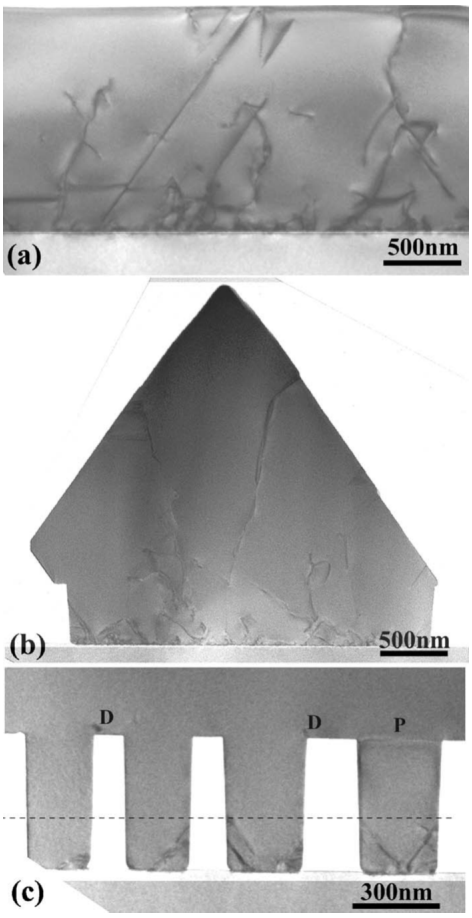


Figure 3.3: (a) GaAs on Si, (b) GaAs in, shallow, 0.2 aspect ratio (AR) trenches, and (c) GaAs in 1.0 AR trenches. **D** represents dislocation defects and **P** represents planar defects along the virtual substrate/trench interface. ART reduces the total defect density near the device region of the semiconductor by eliminating a majority of the <311> defects that propagate upwards from interface between the host substrate and virtual substrate as demonstrated by Bai et al. [125] and Li et al. [121].[2]

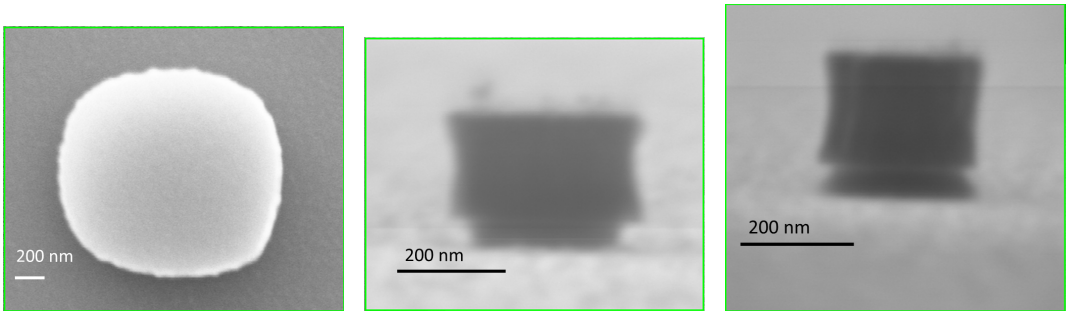
substrate material and propagate along the <311> direction towards the trench walls. Unlike direct growth on a substrate, ART trenches eliminate the majority of the dislocation defects at or near the trench wall leaving a <100> virtual substrate of the desired material as seen in Fig. 3.3. Defect density utilizing ART approaches that of lattice matched substrates and electrical performance has been shown to be similar between ART and literature lattice matched samples [43, 44].

[2] Reprinted with permission from J. Z. Li, J. Bai, J. S. Park, B. Adekore, K. Fox, M. Carroll, A. Lochtefeld, and Z. Shellenbarger, "Defect reduction of GaAs epitaxy on Si (001) using selective aspect ratio trapping," *Applied Physics Letters*, vol. 91, 2007. Copyright © 2007 by American Institute of Physics

3.3 Materials Analysis Techniques

3.3.1 Scaning Electron Microscopy (SEM)

Scanning electron microscopy (SEM) will be vital to this dissertation. Not only will the LEO EVO 50 system be used to measure metal contact area and etch undercut, it is also the main lithography system used for this work.



(a) Top down measurement of a metal contact

(b) Undercut measurement of a metal contact

(c) Undercut measurement of a metal contact

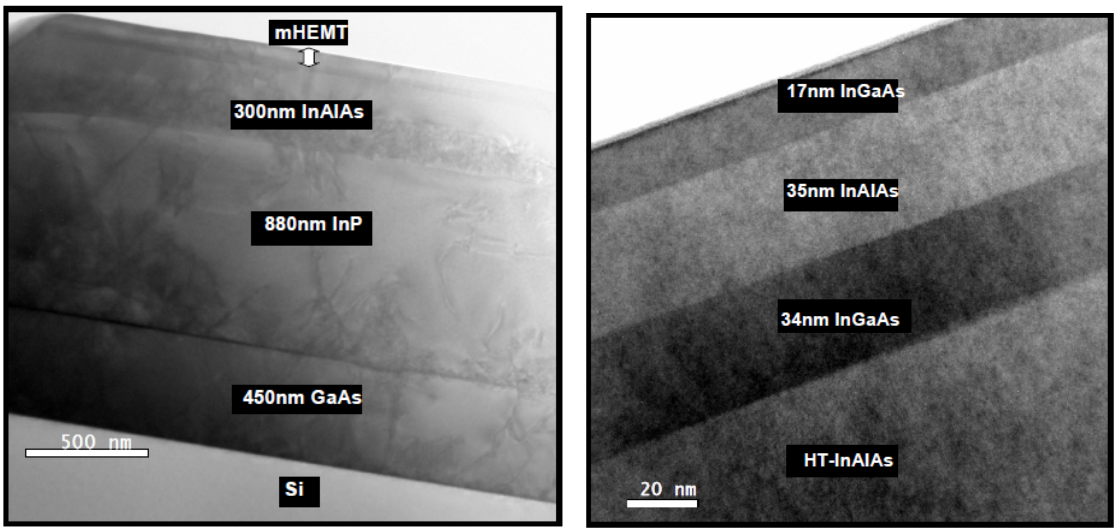
Figure 3.4: (a) Mesa areas are measured with a top down image capture and extracted by a Matlab^{TM}script which provides a best fit for the area. (b) Undercut of the metal contact is measured from two perpendicular angles to capture the anisotropy of the wet etch for inclusion in area correction calculations.

SEM measurements are the primary method by which contact areas and undercut are measured in this dissertation. Prior reports by Pawlik et al. [29, 126] have demonstrated the measurement of undercuts and metal area per Fig. 3.4. Distortion of the features defined by ebeam lithography requires that measuring contact metal area be performed to ensure an accurate extraction of the J_P from electrical measurements. Several top down images are captured across a number of die, ≈80 devices or four per mask defined size, to determine a median area per size set. Using Matlab^{TM}, the images are processed to extract areas based on the number pixels that represent the metal contact. During area analysis, the sample is rotated to a high tilt angle to observe undercut from the etch. The samples are then rotated 90° to measured because of differences in etch rate for the various crystal planes as seen in Fig. 3.4(b)

and 3.4(c).

3.3.2 Transmission Electron Microscopy (TEM)

Transmission electron microscopy (TEM) will be utilized on select samples to determine a variety of characteristics about the state of the designed heterojunctions. Lattice strain can be extracted from the brightness of the ordered region. Defect types can also be determined with TEM analysis as seen in Fig. 3.5(a) and 3.5(b). When used in conjunction with X-ray Photo Spectroscopy (XPS) [127, 128] and Electron Energy Loss Spectroscopy (EELS) [128–131], species intermixing and band alignment can be determined near the junction interface. Due to the cost and sample preparation required by this technique, only select samples will require this analysis. XPS can be utilized to measure valence band edges for materials, but the 10 nm penetration depth is not optimal for determining band edge alignments for heterojunctions.



(a) Cross-secional TEM of mHEMT device showing substrate and buffer

(b) Cross-secional TEM of mHEMT device

Figure 3.5: (a) TEM is capable of imaging lattice defects throughout the device structure (b) This mHEMT sample presented by Lau et al. [12] exhibits excellent crystal quality in the active device region.

3.3.3 Secondary Ion Mass Spectroscopy (SIMS)

Secondary Ion Mass Spectroscopy (SIMS) has proven to be a very useful tool in determining the concentration of impurities within a crystal lattice. While there are drawbacks to this technique, such as the destructive nature of the process and the need for reference samples, few methods can determine constituent lattice atoms as well as SIMS. In most instances only the n and p-type dopants will necessitate determination. Though, if questions regarding the make-up of ternary film stacks should arise, the crystal mole fractions can also be extracted. The metallurgical junction for homojunctions will be considered as the point where n and p-type dopant concentrations are equal. In heterojunction systems, this determination is simply the region where both materials abut. Dopant information, along with corrected J_P, will determine where designed devices belong on a figure of merit chart.

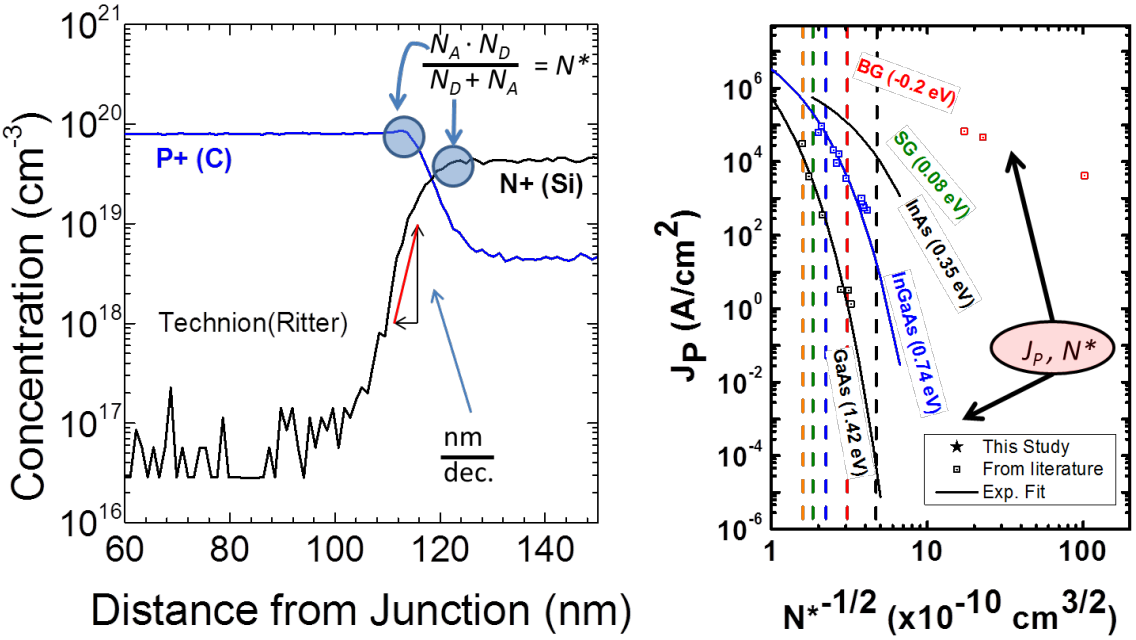


Figure 3.6: SIMS plot of a 200 kA/cm^2 J_P device showing the dopant species and level on either side of the junction. (a) The inlays detail the methods for calculating the junction abruptness as well as N^*. (b) Figure of merit plot showing where J_P and N^* will be applied to compare devices [50, 57, 132].

Samples for SIMS will be taken from the pieces that can not be utilized for device processing. Typical samples would originate near the edge or from pieces impractical for use with lithography. SIMS can give absolute numbers for dopant density and, depending on system capability, has about a 3 nm precision. However, SIMS counts all atoms in the lattice including interstitial and inactive dopant species, which may result in an overestimate of active doping levels. This limitation does not reduce the utility of SIMS as a technique to determine the dopant profile and junction abruptness. Extracting doping levels is straightforward; a calibrated counts value corresponds to specific concentrations of dopant. Generally, the maximum value in the region proximal to the junction will be utilized as the doping level. Once both n and p dopant levels have been determined, half of the harmonic average value will be used in conjunction with the device current density to place the sample on the figure of merit plot shown in Fig. 7.4 below.

3.3.4 High Resolution X-Ray Difraction (HRXRD)

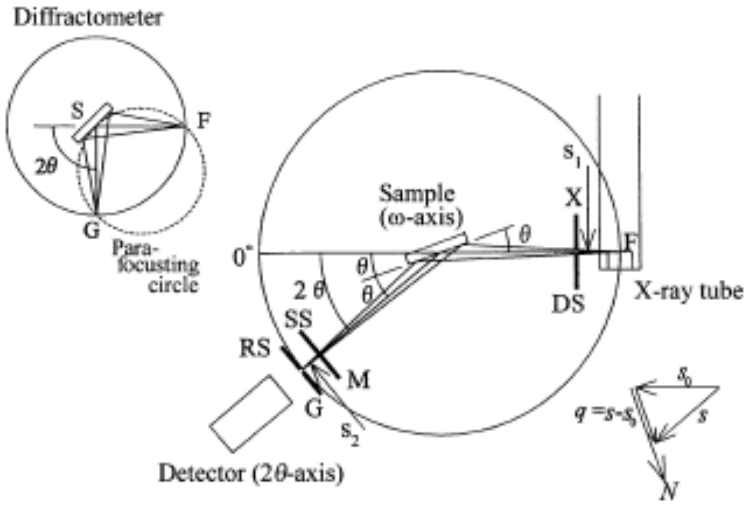


Figure 3.7: A typical HRXRD measurement set up shown by Shinoda et al. [133].[3]

[3] *X-Ray Diffraction Crystallography: Introduction, Examples and Solved Problems*, 2011, p. 108, Diffraction from Polycrystalline Samples and Determination of Crystal Structure, K. Shinoda, Fig. 4.1, © 2011. With permission from Springer Science+Business Media.

X-ray Diffraction will be utilized as a nondestructive technique to confirm material composition is as desired. A fairly typical HRXRD arrangement can be seen in Fig. 3.7, where a sample is loaded onto an adjustable stage with a detector that can be moved independently. By examining the peak width and location, lattice constants for the layers within the film stack can be determined with great precision. The sensitivity of this technique is such that differences in lattice constant be determined down to the $\frac{1}{1000}$ of an Angstrom. Strain effects and defect density can also be extracted using XRD [118] when necessitated by large lattice mismatch layer design or hetero-integration.

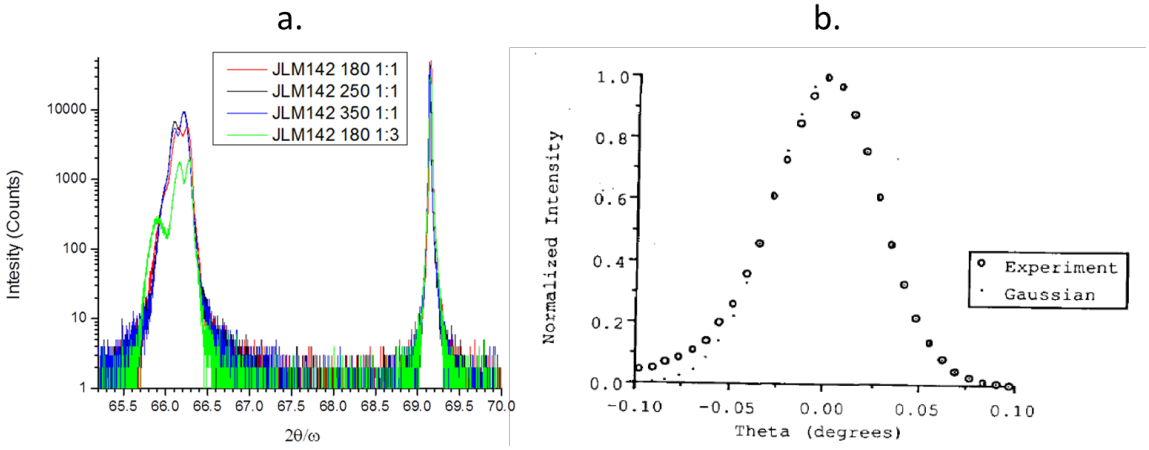


Figure 3.8: (a) Differences in lattice constant and defect density can be detected through XRD techniques. Typical measurements are performed around the (400) wurtzite peak, where fringe spacing and peak width can be utilized to determine film thickness and relaxation. These measurements were taken from a GaAs on Ge Aspect Ratio Trapping sample, compliance with the GaAs lattice reduces with wider spacing. (b) Example of a GaAs peak rocking curve on Si used to determine threading dislocation density by Ayers [118].[4]

When possible, HRXRD measurements will be taken from samples upon arrival from the crystal grower. Measurements along the (400) peak can give indication of the thickness of films, ensuring that layers are near designed parameters. Additionally, Full Width Half Maximum (FWHM) measurements of the ω (rocking) curve will

[4] Reprinted from *Journal of Crystal Growth*, vol. 135, J. E. Ayers, "Measurement of threading dislocation densities in semiconductor crystals by X-ray diffraction," pp. 71–77, Copyright © 1994 with permission from Elsevier

indicate, to a reasonable approximation, the relaxation of layers for a given sample [118]. For example, the peak representing GaAs in Fig. 3.8(a) could have a rocking curve performed as seen in Fig. 3.8(b), allowing for an extraction of the defect density from the FWHM. When multiple rocking curves are taken at high, low, and an additional incidence angle, the defect density due to dislocations, screw defects, and other defect sites can be extracted [118]. Knowledge of defect density and layer thicknesses will be advantageous to processing (for etch depths) as well as current density calculations for defect related tunneling (excess current) [68]. When resources allow, a reciprocal space map (RSM) can provide great insight into the behavior of the source material, indicating varying levels of strain or interface related defects as shown by Penn State in InGaAs on GaAsSb TFET research in Fig. 3.9 [34, 127].

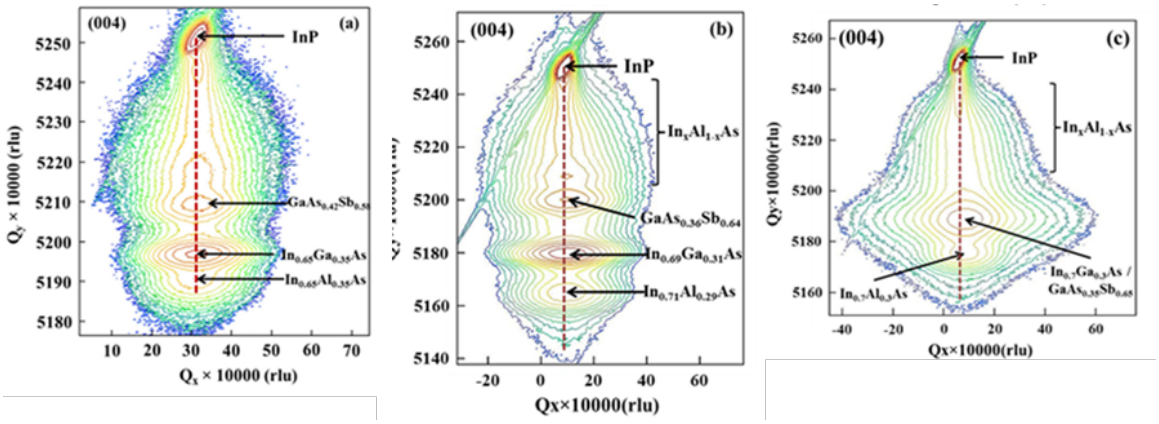


Figure 3.9: RSM of InGaSb/GaAsSb device, the lack of a sharp peak region indicates a highly defected $In_{0.70}Ga_{0.30}As/GaAs_{0.35}Sb_{0.65}$ region as well as significant relaxation of the lattice [34].[5]

Techniques utilizing a combination of low and high incidence angles combined with the (400) peak measurement should allow for the best determination of defect density within a sample. Such measurements will be of great interest when used in conjunction

[5] Reprinted with permission from Y. Zhu, N. Jain, S. Vijayaraghavan, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, W. K. Liu, N. Monsegue, and M. K. Hudait, "Role of InAs and GaAs terminated heterointerfaces at source/channel on the mixed As-Sb staggered gap tunnel field effect transistor structures grown by molecular beam epitaxy," *Journal of Applied Physics*, vol. 112, p. 024306 (16 pp.), 2012. Copyright © 2012 by American Institute of Physics

with large lattice constant differences, such as those originating from InP and GaSb thin films grown on Si substrates. Large defect densities may prove prohibitive to device performance, thus defect density should be extracted when possible.

3.3.5 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a very versatile technique. There are a variety of measurements that can be made, including conductivity and surface roughness. AFM utilizes a probe tip which is scanned across the surface of the sample, through direct or indirect contact and can provide high resolution of the surface conditions. Fig. 3.10 below from [134] displays a typical AFM setup. A laser is reflected off of the top of the tip, and the minute changes in the beam vibration and height are measured and translated into a height. Additional information on the various operational modes available for AFM analysis may be found in Haugstad [135] or Voigtländer [134].

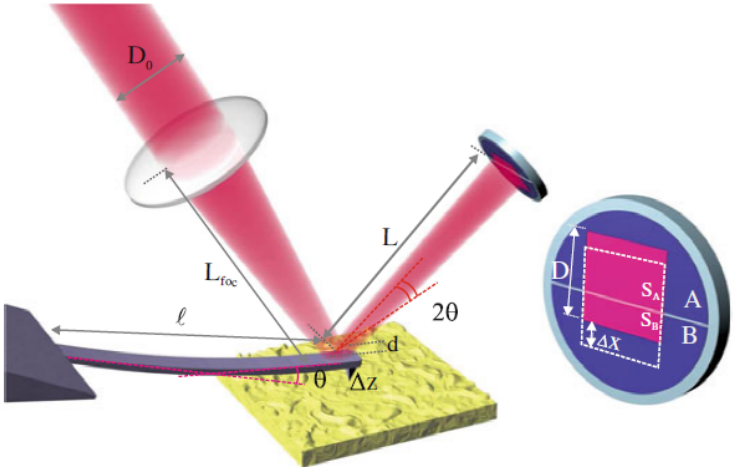


Figure 3.10: A schematic drawing from Voigtländer [134] exhibiting probe deflection characteristics for determining sensitivity during AFM measurements.[6]

In this dissertation AFM will be used to measure surface roughness in terms of absolute height and root mean square (RMS) roughness. However, RMS roughness can be a misleading value without careful selection of the scan window and analysis region. Additionally, RMS roughness values are known to correlate with total defects in the sample [136] and may be used as an alternate means for qualitatively estimating electrical performance.

[6] *Scanning Probe Microscopy : Atomic Force Microscopy and Scanning Tunneling Microscopy*, 2015, p. 161, Technical Aspects of Atomic Force Microscopy (AFM), B. Voigtländer, Fig. 12.3, © 2015. With permission from Springer Science+Business Media.

3.4 Device Fabrication

Generally, devices in this dissertation are grown by MBE. Several different substrates are used in this work: GaAs, GaSb, InP, and Si. Material is chosen based whether it has an appropriate lattice constant for the device material. However, the fabrication process for the tunnel diodes in this dissertation all follow the same general process flow which has evolved as new metals, resists, or processes were introduced. This section describes the metal first process developed in conjunction with my colleagues and published in Applied Physics Letters [27] and the 2012 IEDM Tech. Digest [28]. Table A.2 summarizes the subtle differences between process flows.

First, devices are cleaned in a 1:10 HCl:H_2O solution which removes native oxide and other surface contaminants. Proper adhesion of the metal to the substrate surface is vital and clean surfaces allow for better adhesion by removing native oxides and other material that may have found its way onto the sample surface. Following the clean, samples are promptly mounted onto a carrier substrate with capton tape and loaded into a deposition tool for the metal 1 (M1) contact layer.

Multiple metals may be utilized for the first level contact, typically Mo is used because of the excellent contact made to n-type compound semiconductors [137]. While Ta and W have made reasonably good contacts as well, Mo has provided consistent contact and etch rates. Both e-beam evaporation and sputtering may used, each with different benefits. E-beam provides a lower base pressure and ion damage which can improve electrical results but has been inconsistent during the deposition due to the high melt temperature of the pellets held in the crucible. Sputtering introduces some ion damage but generally adheres well to the cleaned surface. However, it can be adversely affected by prior processes and creates a MoO_x surface layer if the base pressure is too high. Following the Mo recipe in Table 3.1, results in about 200 nm of metal film. Following M1 deposition, samples are carefully removed from the carrier

wafer and moved onto the next step, Lithography level 1 (L1).

Table 3.1: CVC601 metal deposition processes

Metal	Power (W)	Pressure (mTorr)	Ar (sccm)	Time (s)	Thickness (nm)
Mo†	200	2.2	17	420	200
W	200	2.2	17	750	200
Ta	50	2.2	17	300	200

† Typically performed after an overnight pump down and a base pressure below 5×10^{-6} Torr.

Following metal deposition, samples are prepared for L1. A quick deionized water (DI) rinse is performed to remove particulates that may have gathered on the surface after deposition. The sample is then baked on a hot plate at the softbake temperature to remove residual H_2O from the surface. A primer such as AP3000 may be applied following this rinse to encourage complete coverage by the negative tone resist. Early iterations of this process utilized MaN2401 as the negative resist, but moved to a 1:1 (by weight) diluted mixture of AZ nLoF and PMGEA, adapted from Herth et al. [138], due to the superior etch resistance and exposure requirements. Using the recipe listed in Table 3.2 a photoresist thickness of 500 nm is targeted to provide sufficient masking of the metal during etch. Rough alignment marks are scratched into the edges of the resist for focusing and to allow for stage tilt correction during ebeam lithography. Following the post application bake (PAB) samples are loaded into the LEO EVO 50 SEM and alignment of a corner (typically bottom right corner) to the column is performed to create a consistent starting point. After the beam has stabilized, the samples are typically written at 300 nA beam current which represents a crossover of write time and minimum feature size. A pattern consisting of a 10×10 grid is written for each die with a minimum area of 10^{-2} μm^2 or 2.5×10^{-1} μm^2, and a maximum area of 4×10^{2} μm^2. Defined areas often differed greatly from target values due, in large part, to the large writing size field and how the beam was rastered across the surface. Typically device areas were smaller than mask defined sizes, with the greatest variation around the edges of the die area. Changes to the pattern file

could include moving smaller devices towards the center to improve yield. Following L1, the samples must undergo a post exposure bake (PEB), otherwise the chemically enhanced resist will not fully expose and will not develop properly. Samples were typically developed in CD-26, rinsed, and readied for dry etch.

Table 3.2: nLoF level 1 process

Step	Process	Time
1	DI rinse and blow dry	10 s - 30 s
2	Dehydration Bake	60 s or greater
3	500 RPM ramp	2 s
4	500 RPM	5 s
5	3000 RPM ramp	2 s
6	3000 RPM	45 s
7	Post Application Bake at 110°	60 s
8	e-beam lithography	
9	Post Exposure Bake at 110°	180 s
10	Develop in CD-26	30 s
11	DI rinse and blow dry	30 s or greater

Samples are then transferred into a dry etch chamber to remove the exposed metal. Three different systems have been utilized to perform this etch: a LAM490 plasma etcher, a DryTek Quad reactive ion etcher (RIE), and a TRION RIE. Results from the LAM490 tend to be isotropic and adversely affect small devices by reducing metal 2 contact area. Whereas the TRION etched samples unevenly when on a carrier wafer, leading to undesirable results. Utilizing the DryTek Quad provided the most stable output as well as anisotropic etching of the contact metal. Utilizing the etch recipes listed in Table 3.3 either Mo or W could be etched with similar output. With Mo, the photoresist etched at a higher rate than the metal necessitating a thicknesses roughly double that of the metal. This etch rate provided an additional reason to not use MaN2401 which only coats films 100 nm thick. Following the RIE, samples were then subject to a quick O_2 clean to remove residual photoresist. However, the O_2 plasma clean may cause a metal oxide to form, which may interfere with contact to the metal

2 (M2) layer. Additionally, this oxide was the cause of memristor-like device output, especially with the Ta contact metal.

Table 3.3: DryTek Quad metal etch processes for chamber 2

Metal	Power (W)	Pressure (mTorr)	SF_6	O_2	CHF_3 (sccm)	Temperature (C°)	Time (s)
Mo	150	125	125	-	-	50	135
W	150	125	125	-	-	50	75
Ta	150	125	125	-	-	50	135

Once mesa contacts had been defined by RIE, the Esaki junctions had to be isolated. While a Cl_2 or H_2/CH_4 based etch could be used to create anisotropic structures [139–141], wet etch was the preferable formation method due to the lower cost and lack of ion damage that could affect junction performance. A 20:1 solution of $C_6H_8O_8$:H_2O_2 was used to etch InAs, $InAs_{0.91}Sb_{0.09}$, and $In_{0.53}Ga_{0.47}As$. For $Al_{0.40}Ga_{0.60}Sb$ and GaSb an additional solution of 4:1 NH_4OH:H_2O_2 was utilized to further etch into the p-regions. Etch times were on the order of 60 s to 75 s for InAs and $In_{0.53}Ga_{0.47}As$ to etch through the n-region and into or to the p-region. Etch rates were on the order of 1 nm-s^{-1} which lead to undercutting of the device contacts which necessitated measurements to provide accurate device areas for calculating J_P and J_V. Due to the anisotropic nature of the wet etch, high tilt SEM images were utilized to determine the total undercut and actual device size from selected devices across the written region.

Following mesa etch samples are placed into the SEM to determine both the undercut and metal mask/contact area. First, top down measurements are made across multiple die for each size of device. This creates an average area that can then be used for each device instead of the mask defined area. Precision of this measurement can be increased by measuring every size on a die and then sampling single devices across several die to do a planar fit. However, in practice both methods provide roughly the same extracted current density so the average is used in most cases

for this dissertation. Measuring the undercut of the devices is equally as important as the finding the metal area, since it can mean up to a 9× difference in area. Samples are rotated to a steep angle, $> 84°$, to measure the undercut of the metal in one direction and then the stage is rotated 90° to measure undercut in that direction the importance of this step is seen in Fig. 3.4(c). M1 area is then extracted from the SEM micrographs using a Matlab^{TM}script and an average area per device size is determined. The undercut is then subtracted from this area using rectangle parameters that fit the extracted area. This area per device will be used later for J_P and J_V calculations. Following metrology, samples are then moved to planarization.

To facilitate good contact to 100 nm mesas with 2.4 μm diameter probe tips, an additional contact layer must be created. First, viscous interlayer dielectric (ILD) material, bis-benzocyclobutene (BCB) is used to encapsulate the mesas. BCB is then baked and at 140 °C for 5-10 minutes and promptly cured at 250 °C in a N_2 ambient, as exposure to atmosphere at high temperatures creates a brittle and oxidized surface that fails to passivate devices below. The coating process for BCB in Table 3.4 results in approximately 1200 nm of film, which must be etched back to between the metal and mesa surfaces. Utilizing a SF_6/O_2 based plasma, per the BCB etch recipe in Table 3.5, the sample is etched until the metal is exposed. Large area devices and the outer die edges tend to clear fastest, which is likely due to how the die couples to the plasma. This difference in etch can be as large as the metal thickness, leading to both shorting and open circuits on the same die. Following the BCB etch back samples can be observed by SEM to see if the metal has cleared the BCB surface because at high tilt angles charging makes the metal appear especially bright relative to the surrounding BCB. Once metal has cleared the BCB surface, the samples are ready for level 2(L2) lithography.

L2 consists of creating the 20 μm diameter contacts and has undergone several changes to reduce shorting. Originally, a positive resist 950K poly methylmethacry-

Table 3.4: nLoF level 2 process

Step	Process	Time
1	DI rinse and blow dry	10 s - 30 s
2	Dehydration Bake	60 s or greater
2	Apply LOR5A	
4	500 RPM ramp	2 s
5	500 RPM	5 s
6	3000 RPM ramp	2 s
7	3000 RPM	45 s
8	Apply dilute nLoF	
9	500 RPM ramp	2 s
10	500 RPM	5 s
11	3000 RPM ramp	2 s
12	3000 RPM	45 s
13	Post Application Bake at 110°	60 s
14	e-beam lithography	
15	Post Exposure Bake at 110°	180 s
16	Develop in CD-26	30 s
17	DI rinse and blow dry	30 s or greater
18	Deposit M2	300 s or greater
19	Lift-off in remover PG	30 min or greater

late (950K PMMA) was used but required longer exposure times and additional develop steps relative to later iterations. Then a negative L2 layout was created using AZnLoF, but this method would leave metal bits between the ground and contact during incomplete lift-off. A final incarnation utilized ARCH8250, a chemically amplified resist, that exposed quickly and readily dissolved for lift-off. Using this last process, only the contacts need defining. Following the process listed in Table A.1, samples were mounted onto a carrier wafer and loaded for metal deposition. The same Mo recipe in Table 3.1 is used to deposit M2, allowing coprocessing of samples for M1 deposition. After M2 is deposited the samples are then placed in a lift-off solution per the recipe in Table 3.6 and are ready to test once the field area of the samples has been cleared of deposited metal and photoresist. Through the processes listed above devices as small as 10^4 nm^2 are able to be probed and measured. Fig. 3.11 summarizes

Table 3.5: LAM 490 etch processes

Material	Power (W)	Pressure (mTorr)	SF_6	O_2	CHF_3	He (sccm)	Electrode spacing (cm)	Time (s)
Mo	150	125	125	-	-		50	135
BCB	25	300	20	80	-	100	1.65	75
resist	150	125	125	-		-	50	135

Table 3.6: ARCH 8250 level 2 process

Step	Process	Time
1	DI rinse and blow dry	10 s - 30 s
2	Dehydration Bake	60 s or greater
3	500 RPM ramp	2 s
4	500 RPM	5 s
5	3000 RPM ramp	2 s
6	3000 RPM	45 s
7	Post Application Bake at 110°	60 s
8	e-beam lithography	
9	Post Exposure Bake at 110°	180 s
10	Develop in CD-26	30 s
11	DI rinse and blow dry	30 s or greater

previously listed steps in a conceptual schematic going from bare substrate to final encapsulated mesa. Device yield is of incredible importance to this work to ensure proper extraction of J_P and J_V values as shown in later sections.

3.5 Device Characterization and Methodology

The previous sections described the general fabrication process for the diodes in this dissertation. This section describes how the area and electrical characterizations listed previously are performed as well as how to interpret the electrical results.

Samples are to be tested on a Keithley 4200 Semiconductor Parameter analyzer. Utilizing the grid defined in Chapter 3.4 as a ground contact allows the difference in device R between the ground and test devices to current limit to the smaller

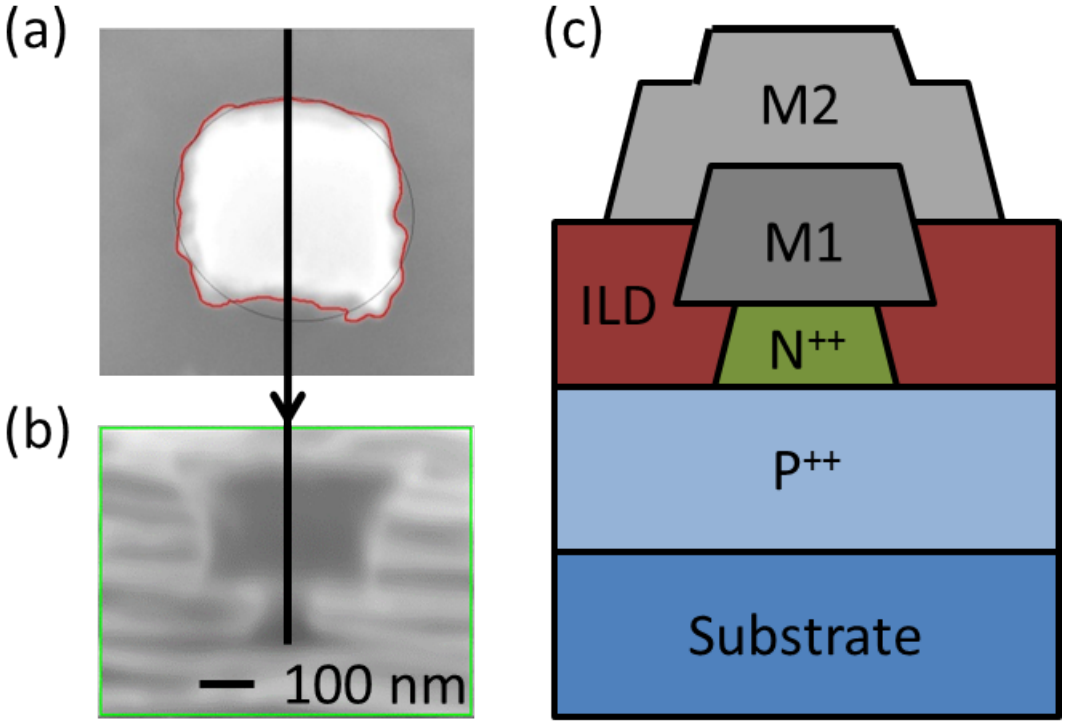


Figure 3.11: (a) Device areas are taken across several die to attain a representative contact area to increase the precision of the J_P and J_V data. (b) The sample is then rotated to a steep angle, often 84°, or higher, to measure the undercut in two perpendicular planes to account for etch anisotropy. (c) A second level metal and ILD must be used with these mesas to contact devices below 2 μm widths
.

device. Fig. 3.11(c) provides an example of how devices are probed, showing the ground contact to the grid as well as the measured device. Since R_S affects the location of V_P, it is possible that high J_P devices will current limit prior to exhibiting V_P. As such, progressively smaller devices must be tested as J_P begins to exceed 100 kA/cm^2. For each device, J_P, J_V, V_P, V_V, and PVCR are recorded from the I-V measurements. PIVET was developed [62] to greatly reduce the analysis time when measuring multiple devices, by allowing graphical selection of the peak and valley locations recording the values automatically.

Once data has been collected, it must be sorted and bad data points removed. This is easily accomplished by removing any data which has a PVCR near or at 1,

since tunnel devices are likely to have PVCR greater than 1.01. Once bad points are removed, the devices are sorted by area and assigned a corrected area as detailed in Chapter 3.4. At this point, statistical analysis of the data proceeds with extractions of J_P, PVCR, and J_V from a Gaussian peak fit to the histogram of the data. Obtaining these extracted values comprises the bulk of the work in this dissertation.

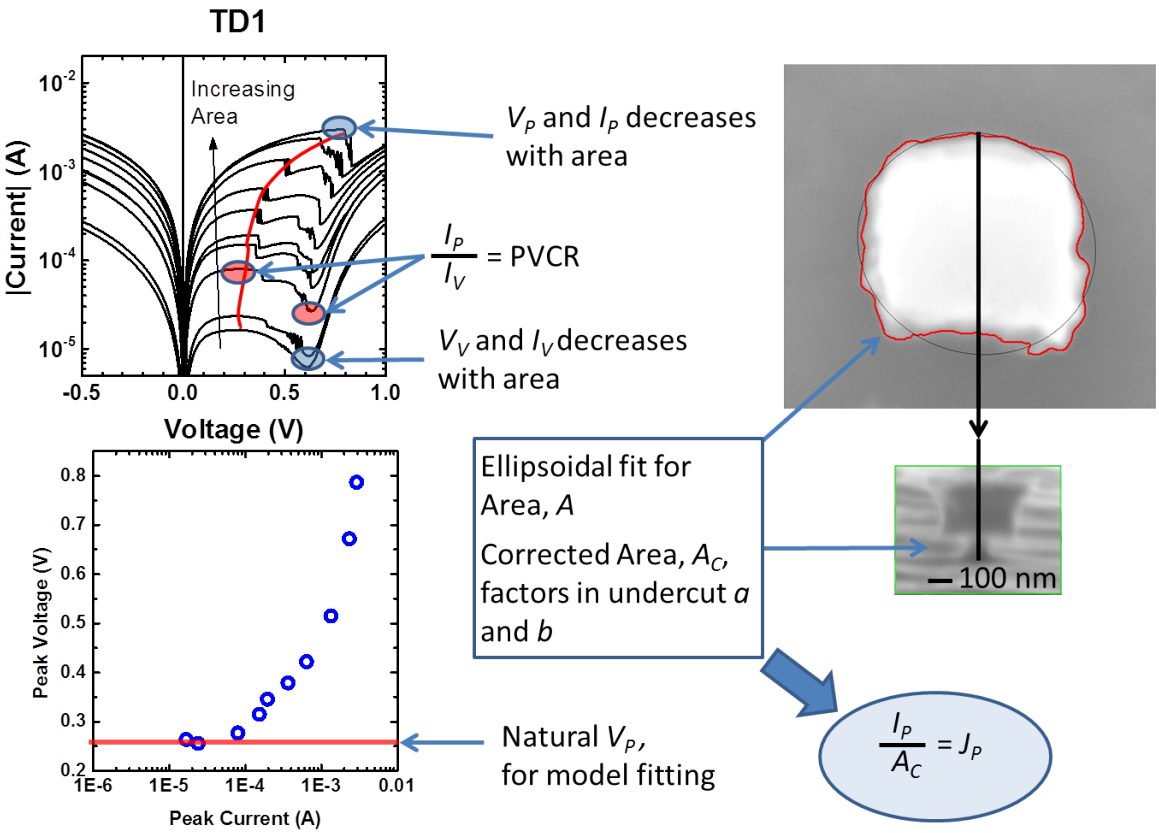


Figure 3.12: Utilizing sample SSG-TD1 an example, keys concepts for understanding Esaki diodes are shown above. a. I-V characteristics for SSG-TD1 as devices are scaled down with area, I_P, I_V, V_P, and V_V, are all every apparent for each discrete device. R_S influence is reduced with area, and eventually V_P will reach a minimum value. J_P is calculated by dividing I_P by the corrected device area. PVCR is calculated from I_P and I_V

3.6 Growth and Characterization Conclusions

Chapters 2 and 3 describe what Esaki tunnel diodes are and how to fabricate and examine them. The previous sections discuss which analysis techniques are utilized

and why they are useful for understanding the behavior of the devices measured in this dissertation.

Building upon the prior sections, the following chapters will discuss the various tunnel diodes studied in this dissertation. Chapter 4 will cover small stagger gap devices, aiming to show how reducing the effective E_G can increase J_P. Chapter 5 further examines the reduction in effective E_G by examining large staggered gap devices. Chapter 6 explores a completely broken gap system in an attempt to reach a 10 MA/cm^2 J_P target. The remaining Chapters 7 and 8 attempt to analyze the impact of heterointegration onto Si substrates has on tunneling characteristics.

Chapter 4

Small Staggered Gap/Type II Heterojunctions

4.1 Introduction

This chapter explores the impact of effective bandgap on tunneling characteristics. $In_{0.53}Ga_{0.47}As$ Esaki diode behavior is well known [28] and can be modeled [62], but to reach a target of 10 MA/cm^2 doping densities would have to exceed what $In_{0.53}Ga_{0.47}As$ can contain. However, an Esaki diode with lower E_G will produce higher J_P at equivalent doping density of an $In_{0.53}Ga_{0.47}As$ device. This chapter will explore small staggered gap (SSG) and large staggered gap devices (LSG) and compare the results back to those of $In_{0.53}Ga_{0.47}As$ based systems.

First, a SSG family of devices will be fabricated and tested. This group consists of $In_{0.53}Ga_{0.47}As/GaAs_{0.50}Sb_{0.50}$ heterojunctions, which should provide small (<0.2 eV) reductions to the effective E_G. Such a change would be expected to produce J_P values somewhere between those of $In_{0.53}Ga_{0.47}As$ and InAs. Second, strained SSG devices will be built and tested. Strained SSG devices affect carrier mobility which applies directly to tunneling probability. As such, these systems are expected to deviate from the J_P that would otherwise be exhibited.

4.2 Small Stagger Gap Esaki Diodes (SSG)

Two samples for the $In_{0.53}Ga_{0.47}As/GaAs_{0.50}Sb_{0.50}$ system were built in the preliminary set, with slightly differing layer schemes as shown in Fig. 4.1. InGaAs layers were n-type doped using Si, while GaAsSb layers are p-type doped with C. Table 4.1 summarizes the doping scheme and typical electrical characteristics for these devices. Typical materials and electrical results for the small stagger $In_{0.53}Ga_{0.47}As/GaAs_{0.50}Sb_{0.50}$ devices will also be shown.

Data for the small stagger system is very promising, exhibiting J_P values exceeding 90 kA/cm^2. It appears that for equivalent N^* values, a larger band overlap will lead to an increase in the tunnel current relative to the $In_{0.53}Ga_{0.47}As$homojunction as seen in Fig.2.4(b). Excess current does not appear to be problematic for this lattice matched system, likely due to low defect density and good growth quality. While this heterojunction does mark an improvement over the $In_{0.53}Ga_{0.47}As$ homojunctions system, it does not appear to be capable of meeting the 10 MA/cm^2 target for peak current density.

4.2.1 Small Stagger Gap Series 1

SSG-TD1 was designed to have similar doping to previously reported $In_{0.53}Ga_{0.47}As$ devices to provide for a good comparison between effective E_G for the two material systems. Fig. 4.1(a) gives a representative schematic for the SSG-TD1 film stack. This system was acquired from a commercial vendor(Intelliepi), and represents the maximum doping levels for which the system had been calibrated. Other groups have had a tendency to create a very thin, but highly doped region just prior to the tunnel junction [142]. This technique is supposed to provide increased doping levels at the junction without the risk of increased defect density due to the high doping levels. Fig. 1.3displays where doping density and J_P fall relative to other Esaki tunnel

diodes. SSG-TD1 exhibits J_P between $In_{0.53}Ga_{0.47}As$ and InAs as hypothesized.

60 nm	$In_{0.53}Ga_{0.47}As$: Si	4.5×10^{19} cm^{-3}
3 nm	$In_{0.53}Ga_{0.47}As$	uid
10 nm	$GaAs_{0.50}Sb_{0.50}$: C	2×10^{19} cm^{-3}
300 nm	$GaAs_{0.50}Sb_{0.50}$: C	1×10^{19} cm^{-3}
300 nm	$In_{0.52}Al_{0.48}As$: C buffer	1-5×10^{19} cm^{-3}
Substrate	InP:Fe	P+

(a) SSG-TD1

60 nm	$In_{0.53}Ga_{0.47}As$: Si	1×10^{20} cm^{-3}
3 nm	$In_{0.53}Ga_{0.47}As$	uid
300 nm	$GaAs_{0.50}Sb_{0.50}$: C	5×10^{19} cm^{-3}
300 nm	$In_{0.52}Al_{0.48}As$: C buffer	1×10^{19} cm^{-3}
Substrate nm	InP:Fe	P+

(b) SSG-TD2

Figure 4.1: (a) Schematic of the film stack for samples SSG-TD1. Doping levels are targeted to be very high to produce large J_P between that of $In_{0.53}Ga_{0.47}As$ and InAs. A 10 nm highly doped region was utilized as an attempt to further increase doping levels. (b) Schematic of the film stack for samples SSG-TD2. The 10 nm highly doped region has been replaced with one of uniform doping to reduce parallel resistor issues associated with the two level doping scheme.

Material analysis for sample SSG-TD1 and SSG-TD2 were limited to SIMS as shown in Fig. 4.2. Doping densities for SSG-TD1 were lower than targeted, probably to preserve the quality of the sample over attaining target doping levels. Dopant concentration was found to be 9×10^{19} cm^{-3} for Si and 1.7×10^{19} cm^{-3} for C, which leads to an N^* value of 1.43×10^{19} cm^{-3} for SSG-TD1. Doping profiles for Si and C, show 10.2 and 4.89 nm/dec., respectively. A lower J_P than designed was expected of SSG-TD1 due to lower doping concentrations at the junction. Doping densities for SSG-TD2 were near targeted values, though N^* will slightly higher than targeted due to slight differences in doping from the specified targets. Dopant concentration was found to be 1.2×10^{20} cm^{-3} for Si and 5.5×10^{19} cm^{-3} for C, which leads to an N^* value of 3.77×10^{19} cm^{-3} for SSG-TD2. Doping profiles for Si and C, show 10.6 and 7.94 nm/dec., respectively, which is marginally broader than SSG-TD1. A J_P greater than SSG-TD1 should be expected.

Over 300 devices were measured for both SSG-TD1 and SSG-TD2 to build a statistical data set for extracting J_P, J_V, and PVCR. NDR without series resistance related latching was readily apparent for numerous devices, indicating J_P values will

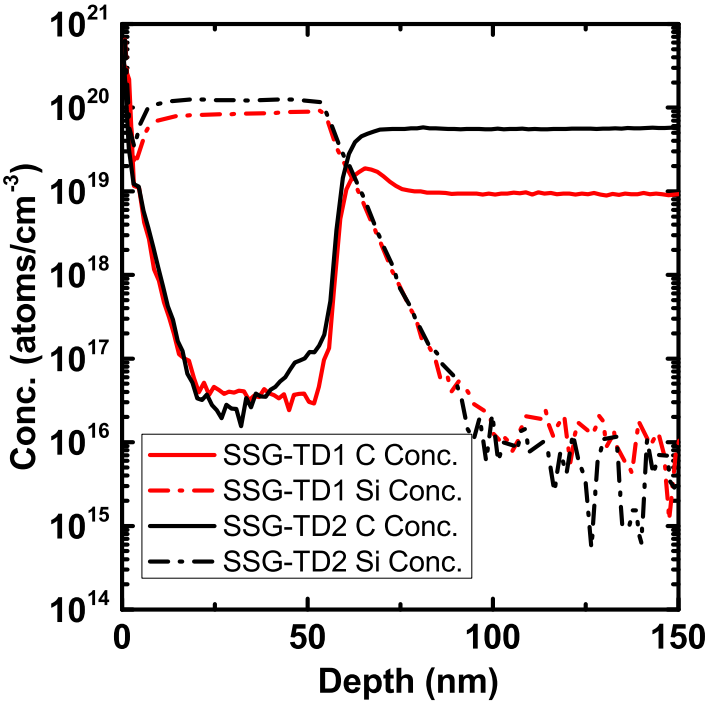
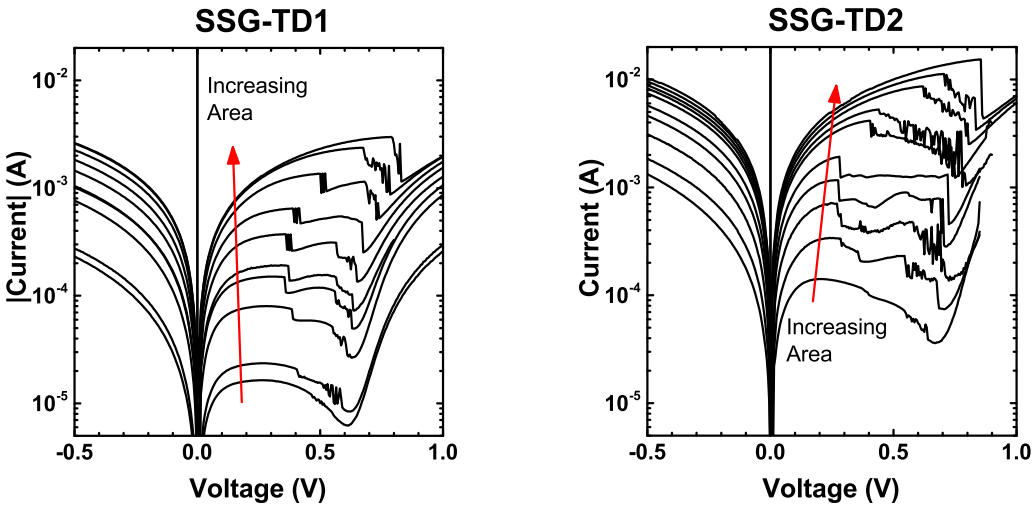


Figure 4.2: SIMS for SSG-TD1 (red) from which peak doping levels of 9×10^{19} cm^{-3} for Si and 1.7×10^{19} for C were extracted. For SSG-TD2 (black) doping levels of 1.2×10^{20} cm^{-3} for Si and 5.5×10^{19} cm^{-3} for C were extracted. Junction abruptness for this sample is reasonable for MBE, and should not reduce device performance. Si was found to be 10.2 nm/dec. and C was found to be 4.89 nm/dec. at the metalurgical junction for SSG-TD1. 10.6 nm/dec. for Si and 7.94 nm/dec. for C were extracted for SSG-TD2.

be under 100 kA/cm^2 for SSG-TD1. Measured devices typically exhibited I-V curves like those in Fig. 4.3(a) showing excellent current scaling with reductions in area. Sample SSG-TD2 was shown to exhibit higher J_P than SSG-TD1 due to higher I for the equivalent sized devices. Fig. 4.3(b) represents typical I-V characteristics for a given die. As with SSG-TD1, V_P quickly moves to lower values with reduced area as R_S related latching is reduced.

J_V, J_P, and PVCR values were extracted using the procedures in sections 3.4 and 3. PVCR for samples SSG-TD1 and SSG-TD2 were extracted from a Gaussian fit to a histogram of the data values. SSG-TD1 exhibited a mean PVCR of 2.75 with a maximum of 6.55, while SSG-TD2 showed a mean of 3.11 and maximum of 5.45 as seen in Fig. 4.4. Due to the limited volume of literature values for PVCR [54], it can not



(a) Family of *I-V* Curves for SSG-TD1 **(b)** Family of *I-V* Curves for SSG-TD2

Figure 4.3: Family of *I-V* curves for SSG-TD1 and SSG-TD2 showing current scaling with reduced area devices. Interestingly, there appears to be a longer distance between V_V and V_P relative to a homojunction $In_{0.53}Ga_{0.47}As$ Esaki diode which may be due to a greater overlap of conduction and valence bands for the heterojunction *vs.* a homojunction.

be determined if a peak PVCR region exists between or below the effective doping levels for this sample set. From Fig. 4.5 it can be seen that SSG-TD1 exhibits a J_P of 91.3 kA/cm^2 and SSG-TD2 has a J_P of 572 kA/cm^2. From Fig. 4.6 it can be seen that SSG-TD1 exhibits a J_V of 33.3 kA/cm^{2}and SSG-TD2 has a J_V of 179 kA/cm^2. At 572 kA/cm^2 and N^* at 3.77×10^{19}, the $In_{0.53}Ga_{0.47}As/GaAs_{0.50}Sb_{0.50}$ heterojunction system may not reach 10 MA/cm^2. Table 4.1 summarizes the results for SSG-TD1 and SSG-TD2. With N^* at 3.77×10^{19} cm^{-3} for a 572 kA/cm^2 J_P, it does not appear that this system will reach 10 MA/cm^2 before reaching doping limits above the 5×10^{19} cm^{-3} N^* range. However, from Fig. 4.7(a), with an effective E_G of roughly 0.50 eV, the SSG samples exhibit J_P between $In_{0.53}Ga_{0.47}As$ (0.74 eV) [31] and InAs (0.34 eV) [31, 58].

Table 4.1: Summary of device information and extracted values

Device	C $\times 10^{19}$ (cm^{-3})	Si $\times 10^{19}$ (cm^{-3})	N^* $\times 10^{19}$ (cm^{-3})	$N^{*-0.5}$ $\times 10^{-10}$ (cm^{-3})	J_P (kA/cm^2) mean	σ	J_V (kA/cm^2) mean	σ	PVCR mean	max	σ
SSG-TD1‡	1.7	9	1.43	2.64	91.3	7.3	33.3	6.6	2.75	6.56	0.25
SSG-TD2‡	5.5	12.0	3.77	1.63	572	80	179	43.5	3.11	5.45	0.85

‡ InP substrate

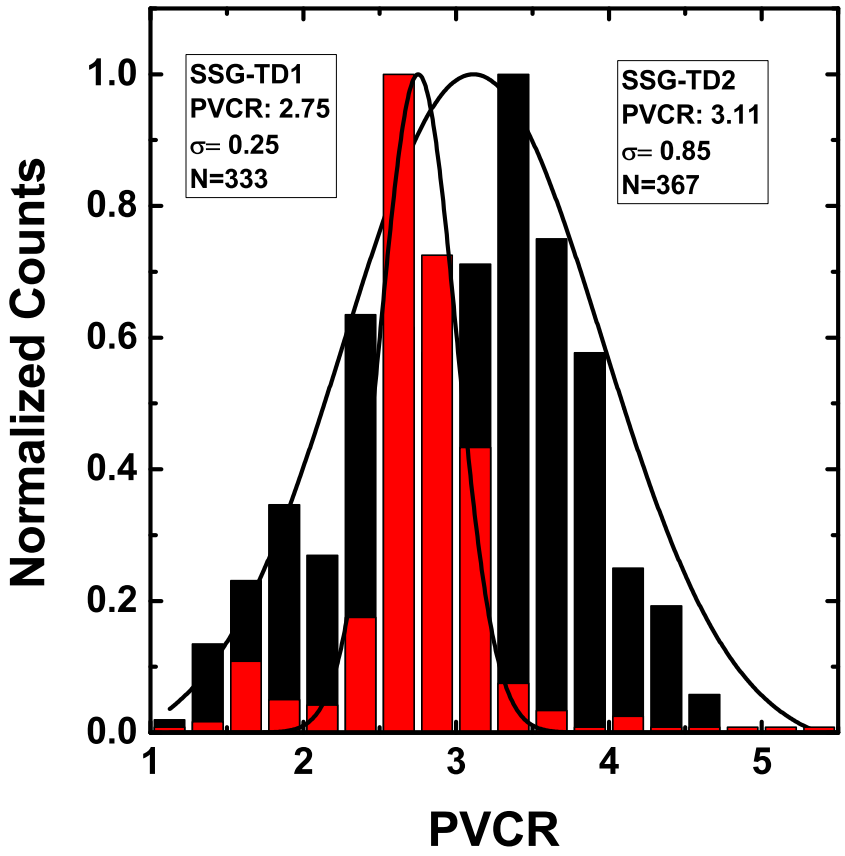


Figure 4.4: PVCR histogram for SSG-TD1 and SSG-TD2 showing extracted PVCR values to be 2.75 and 3.11, respectively. The distribution of values for SSG-TD1 is fairly tight, which indicates uniform performance across the wafer and few defects that would cause major changes in excess current. The broader profile of SSG-TD2 was likely process related since XRD analysis appears to show good crystallinity.

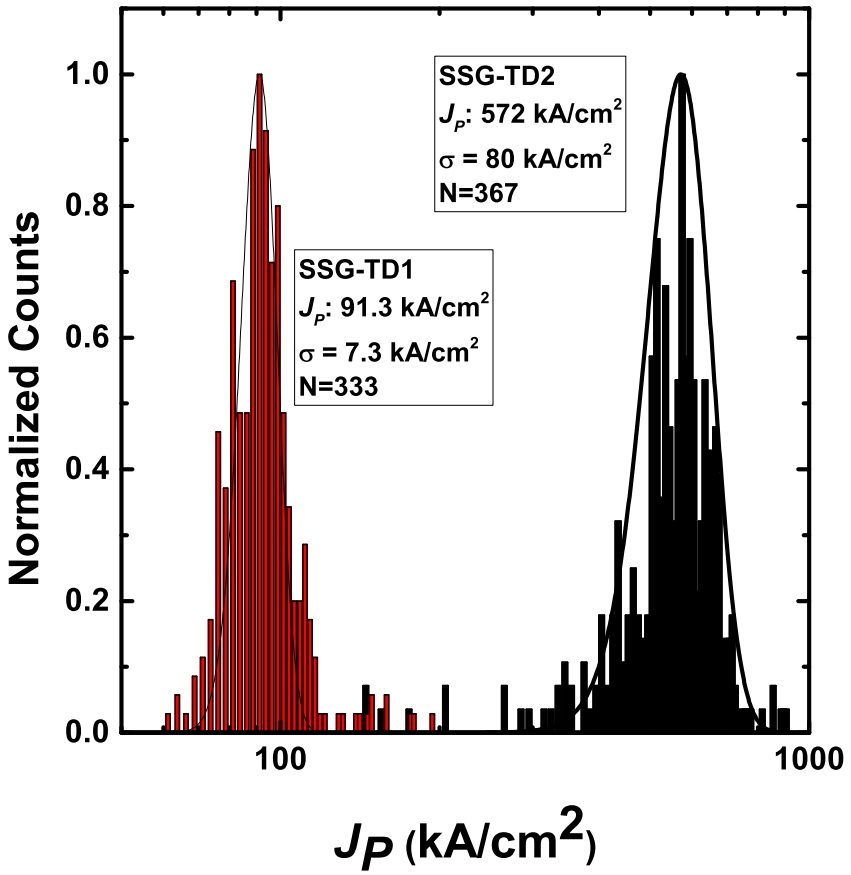


Figure 4.5: J_P histogram for SSG-TD1 and SSG-TD2 showing extracted values to be 91.3 kA/cm^2 and 572 kA/cm^2, respectively. σ values are between 5% and 15%, indicating that area variation between devices is likely higher than the fitted value on SSG-TD2. Though doping levels may be pushed higher, it is unlikely that exceeding 1×10^{20} cm^{-3} for both dopants could reach a 10 MA/cm^2 J_P target.

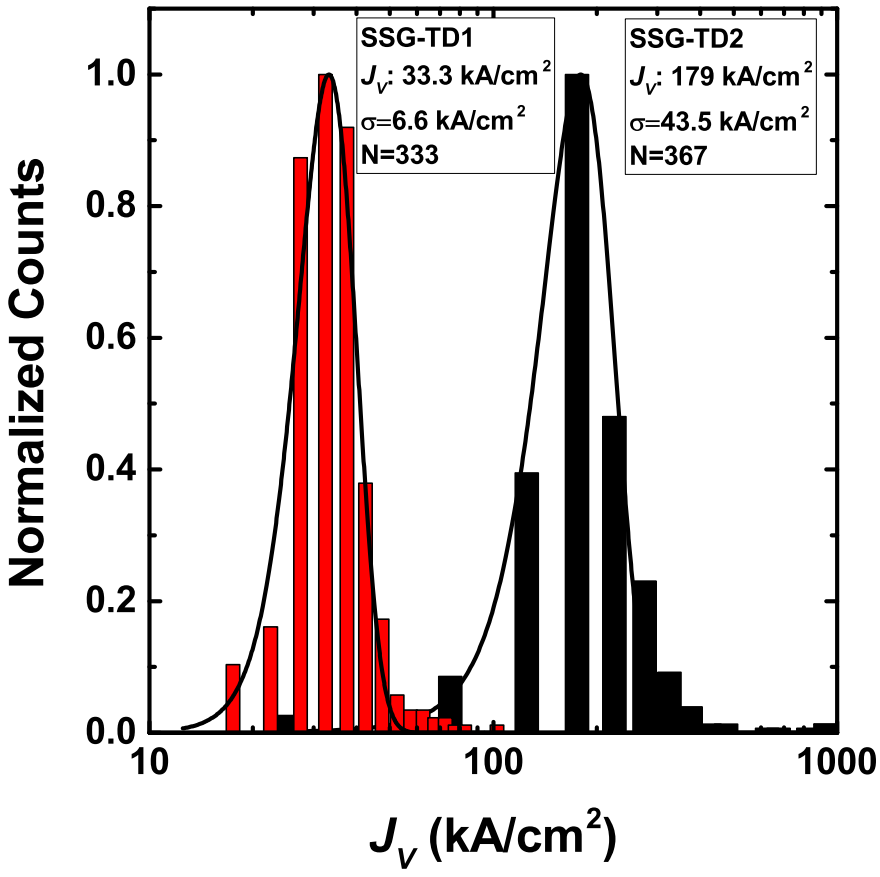
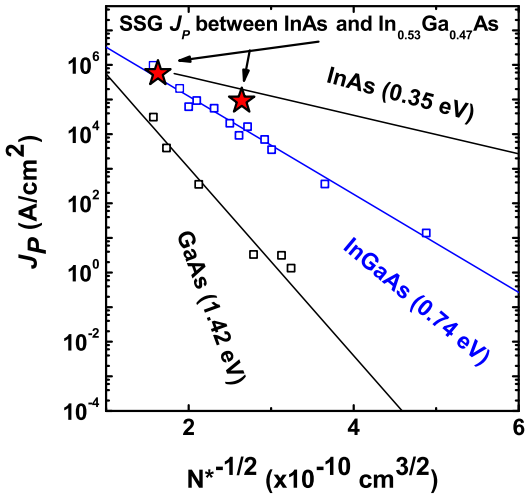
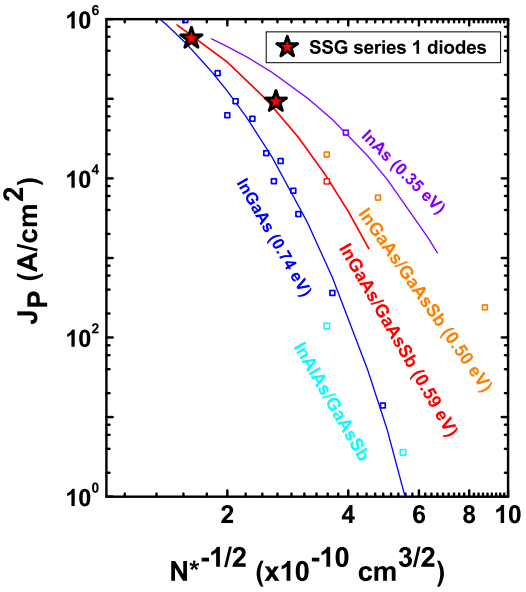


Figure 4.6: J_V histogram for SSG-TD1 and SSG-TD2 showing extracted values to be 33.3 kA/cm^2 and 179 kA/cm^2, respectively. σ values are between 20% and 25%, indicating that area variation between devices is likely higher than the fitted value.



(a) Figure of Merit Plot (FOM)



(b) Figure of Merit Plot (FOM) adapted from Romanczyk et al. [27]

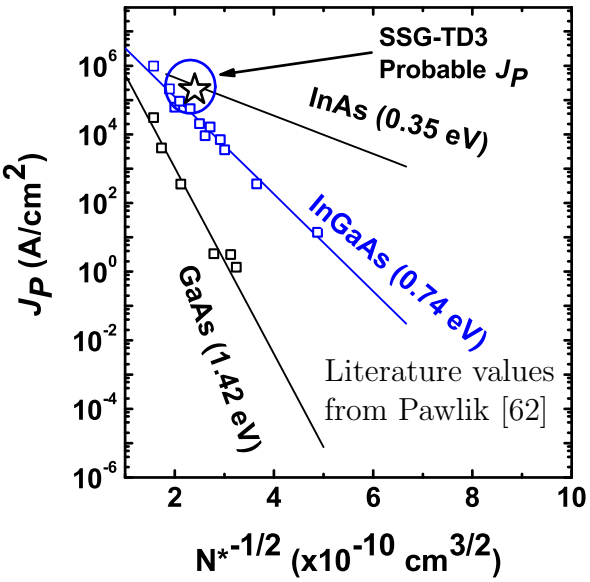
Figure 4.7: (a) PVCR *vs.* N^* FOM plot for SSG-TD1 and SSG-TD2. The small stagger gap (≈0.5 eV) provides J_P values between equivalently doped InAs and $In_{0.53}Ga_{0.47}As$ doped samples. (b) Figure of merit (FOM) plot comparing published values of J_P against systems with E_G below that of InAs

4.2.2 SSG-TD3

It follows from samples SSG-TD1 and SSG-TD2 that creating a smaller effective E_G will increase J_P for the same N^* value with respect to Esaki diodes from higher E_G material. As such, SSG-TD3 was designed to have a small to moderate stagger by combining $In_{0.7}Ga_{0.3}As$ with $GaAs_{0.35}Sb_{0.65}$ for an effective E_G similar to that of InAs and below that of the $InAs_{0.91}Sb_{0.09}/GaAs_{0.50}Sb_{0.50}$ system. Fig. 4.8(a) shows the designed film stack for this device. By utilizing the high In content InGaAs combined with the high Sb content GaAsSb device performance is expected to be along the line indicated in Fig. 4.8(b). However, it will be shown that no NDR related values were able to be extracted due to high defect density.

60 nm	$In_{0.7}Ga_{0.3}As$: Si	(5-10)×10^{19} cm^{-3}
3 nm	$In_{0.7}Ga_{0.3}As$	uid
10 nm	$GaAs_{0.35}Sb_{0.65}$: C	(5-10)×10^{19} cm^{-3}
300 nm	$GaAs_{0.35}Sb_{0.65}$: C	(1-5)×10^{19} cm^{-3}
1000 nm	$In_{0.7}Al_{0.3}As$: C buffer	(1-5)×10^{19} cm^{-3}
Substrate	InP:Fe	S.I.

(a) SSG-TD3



(b) Figure of Merit Plot (FOM)

Figure 4.8: (a) Schematic of the film stack for samples SSG-TD3. Doping levels are targeted to be very high to produce large J_P. (b) Figure of merit (FOM) plot comparing published values of J_P against the projected SSG-TD3 J_P value.

For SSG-TD3, doping was Si on the n side of the junction, and C on the p side of the junction. High doping density values of 5×10^{19} cm^{-3}, or greater, were targeted for both Si and C doping. A 1 μm thick $In_{0.7}Al_{0.3}As$ buffer was used to match the $In_{0.7}Ga_{0.3}As$ lattice constant. Surface analysis in the SEM during area correction

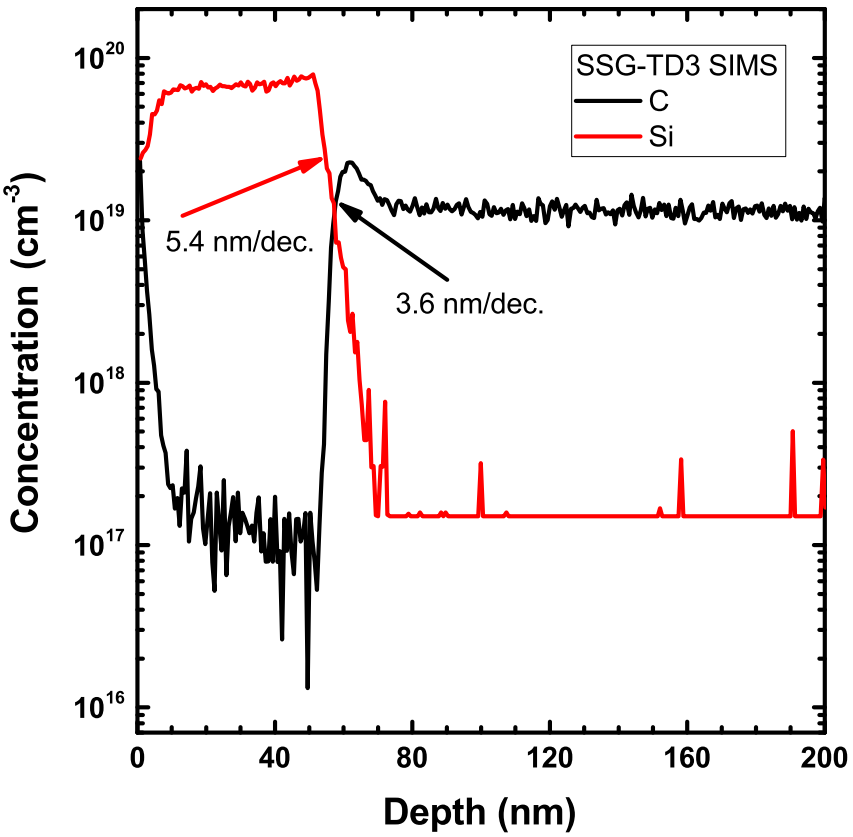


Figure 4.9: SIMS for SSG-TD3 exhibits steep dopant slopes of 5.4 nm/dec. for Si and 3.6 nm/dec. for C.

indicates that there are many defects that propagated through the epilayers. Images from a TEM would help determine the density of the defects per layer similar to the work of Zhu et al. [34, 127].

SEM, SIMS, and XRD were utilized to analyze SSG-TD3. From SIMS it can be seen that the doping levels were nearly an order of magnitude lower than the target of 1×10^{20} cm^{-3} for both Si and C dopants. Attaining levels of Si and C above 2×10^{20} cm^{-3} has been shown to be difficult for $In_{0.53}Ga_{0.47}As$ and $GaAs_{0.50}Sb_{0.50}$ as well as for InAs and GaSb [47, 143, 144], the ternary combinations between them should be expected to be slightly more difficult owing to less calibrated growth and available literature information. From Fig. 4.9 dopant levels for Si were shown to be 7.5×10^{19} cm^{-3} and 2.25×10^{19} cm^{-3} for C. Resultant junction abruptness yielded 5.4 nm/dec. for Si and 3.6 nm/dec. for C, which are within range of the best reported

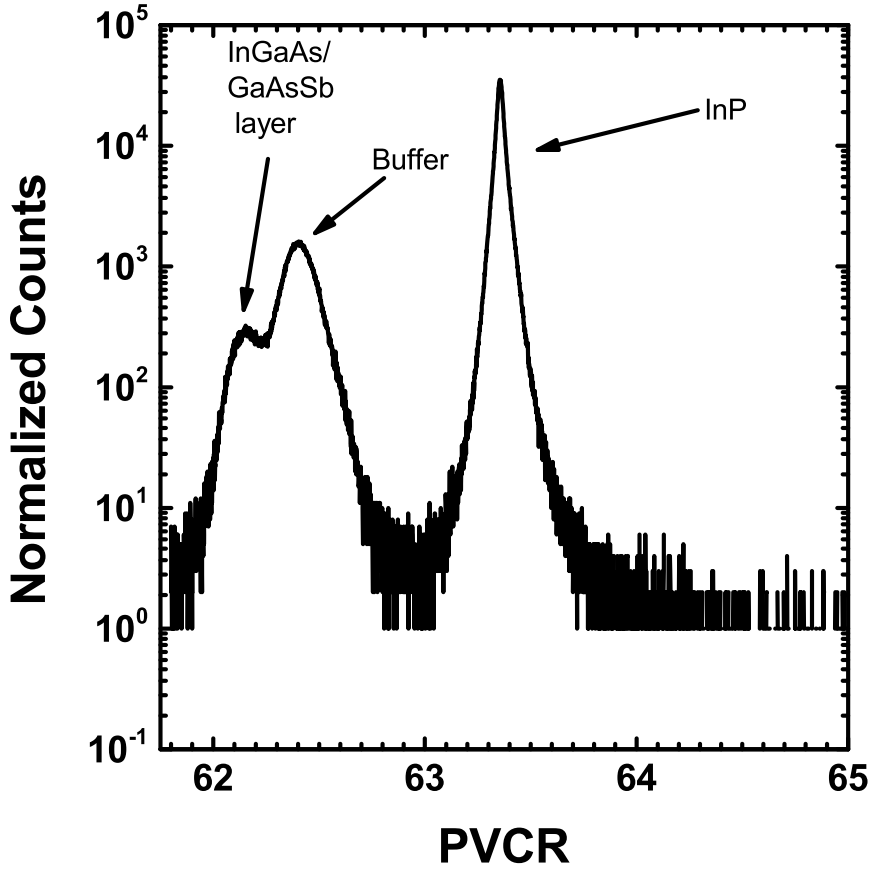


Figure 4.10: HRXRD for SSG-TD3 shows a fairly broad InGaAs/GaAsSb layer indicating the presence of relaxing which will adversely affect tunneling performance.

doping profiles for those dopants by MBE. From Fig. 4.10 there appears to be some relaxation of the $In_{0.53}Ga_{0.47}As/GaAs_{0.50}Sb_{0.50}$ layer, which will negatively impact J_V and PVCR.

SSG-TD3 I-V characteristics show kinks that can be associated with tunneling currents, however from Fig 4.11 is apparent that a large excess current swamps the system. Sources for the excess current are likely to be defects within the device layer that have propagated up from the buffer. Viewing Fig. 4.12, it becomes apparent that surface variation may be affecting the device performance. While this device should have exhibited J_P values similar to those seen in InAs, only I-V curves showing very

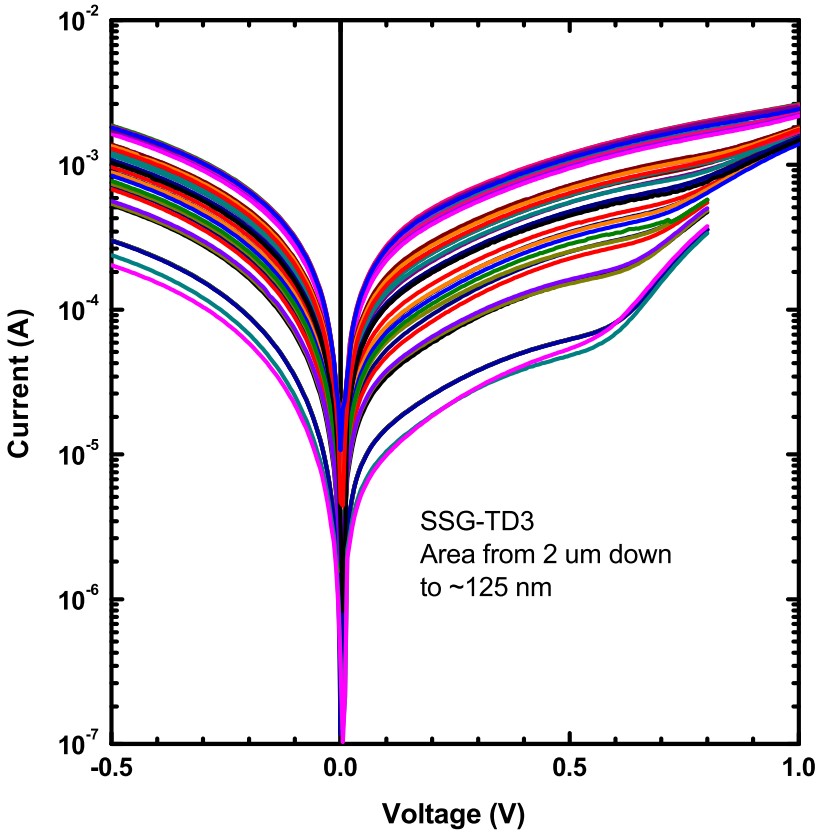


Figure 4.11: Typical I-V characteristics for SSG-TD3. This device was designed to be closer to InAs in effective E_G, however high defect density affected the devices to the point that excess current completely masks the tunnel region of the I-V curves.

large excess current were able to be extracted. This combination of I-V data and materials analysis indicates that further study of SSG-TD3 would not yield usable results at room temperature. Low temperature measurements have proven successful for other groups when this type of behavior occurs, however other devices in this dissertation were viewed as having greater potential to exceed the 10 MA/cm^2 J_P target, and as such further study of SSG-TD3 was deemed unnecessary.

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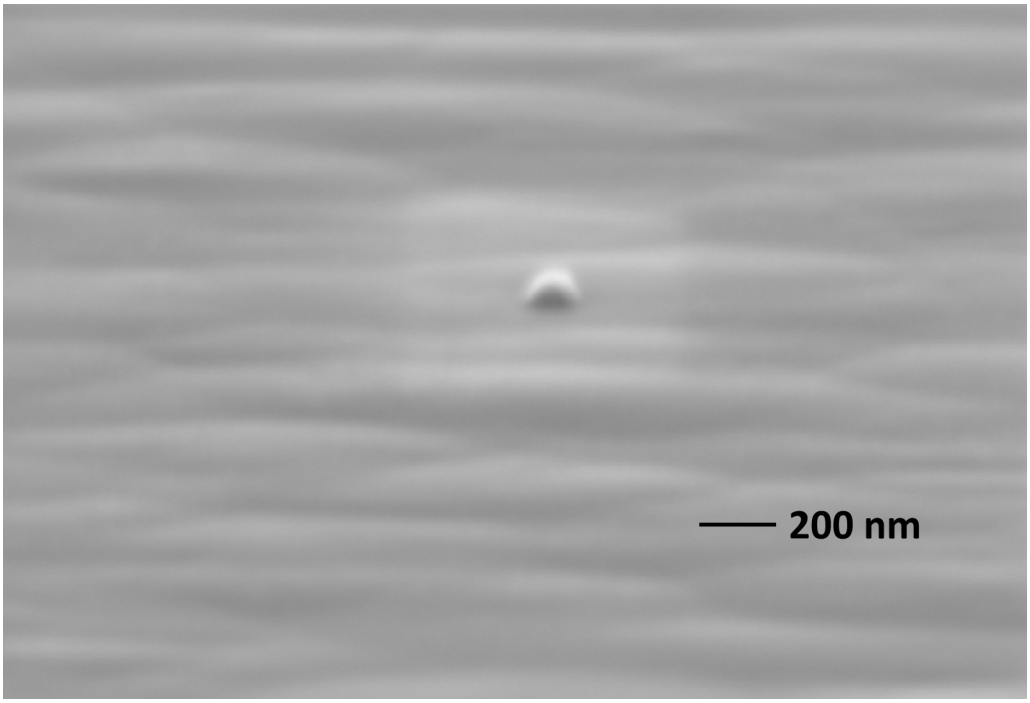


Figure 4.12: Surface roughness is very apparent for sample SSG-TD3 from SEM micrographs, indicating probable large defect densities and a relaxed layer.

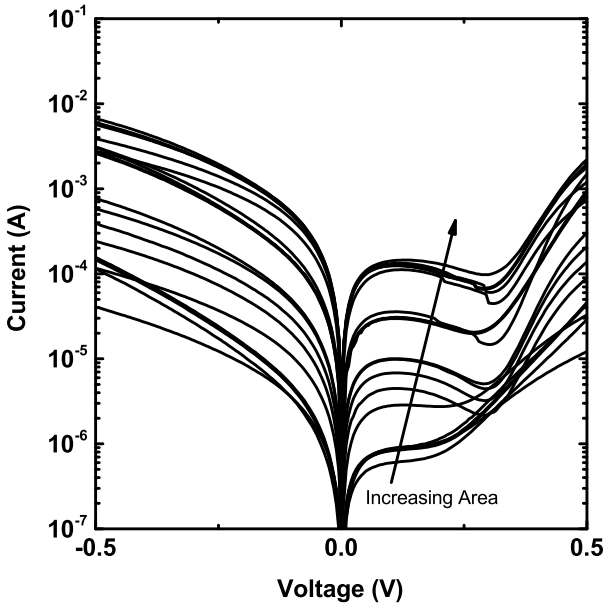
4.3 Small Stagger Strained Heterojunctions

Strain is known to affect carrier mobility for both p and n type carriers. How the sample is strained may reduce mobilities and quickly referencing [46, 52, 62] makes apparent how this could lead to lower tunnel current. For Si and Ge devices, devices can be strained by warping the substrate through applied pressure. III-V semiconductors are not nearly as compliant with the tools used to strain Si devices and break under low stress conditions. As such, little data can be extracted due to their inherently lower mechanical strength. To test this hypothesis, strain was induced through lattice mismatch between the tunneling region and the surrounding material. Three samples were created for this purpose and are described in Figs. 4.13(a), 4.14(a), and 4.15(a). Fully relaxed $In_{0.70}Ga_{0.30}As$ was grown on an InP substrate to provide tensile strain across the tunnel region and a capping layer of $In_{0.70}Ga_{0.30}As$ acted to reinforce lattice compliance. This design was similar to that of Day et al. [30] in that

the band gap was varied in a 3 nm region between $In_{0.53}Ga_{0.47}As$ n and p regions, but different in that these layers also incorporated strain. The design of this sample set was adjusted by partners at SEMATECH and intended to include a control and compressed tunnel region data point. However, these samples would not meet the J_P targets and did not warrant further resource expenditures. Additionally, further research was abandoned when high priority broken gap samples arrived.

5.5 nm	$In_{0.70}Ga_{0.30}As$: Be	1×10^{19} cm^{-3}
5 nm	$In_{0.53}Ga_{0.47}As$: Be	1×10^{19} cm^{-3}
3 nm	$In_{0.53}Ga_{0.47}As$	uid
300 nm	$In_{0.70}Ga_{0.30}As$: Si	1×10^{19} cm^{-3}
Substrate	InP	

(a) SSG-TD4



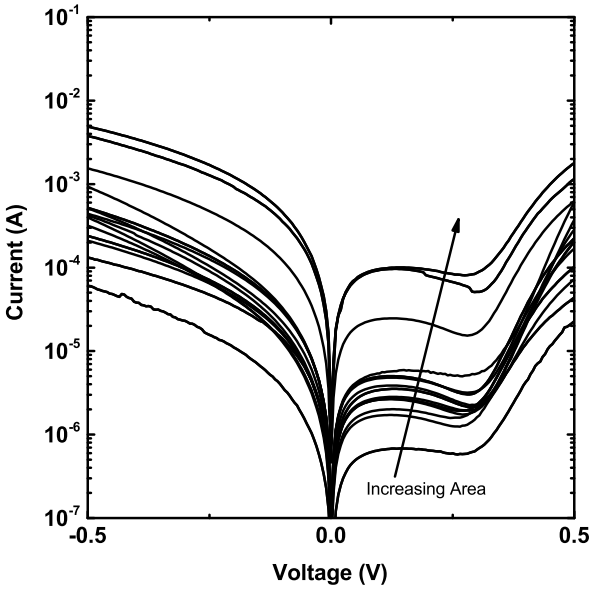
(b) SSG-TD4 Family of I-V Curves

Figure 4.13: (a) Schematic of the film stack for the strained staggered gap Esaki diode SSG-TD4 with an $In_{0.53}Ga_{0.47}As$ tunnel region. (b) I-V curves for SSG-TD4 show scaling with area reduction. Additionally, low PVCR values are consistent with higher defect density.

However, in can be noted that with increased strain that the devices exhibit lower current, with the caveat of an increased bandgap which also decreases J_P as seen in Figs. 4.13(b), 4.14(b), and 4.15(b). This experiment hints at J_P reductions with increased tensile strain but is confounded with an increased E_G at the tunnel junction. Likely, the J_P is more affected by the change in E_G as well as strain and/or reduced defect inclusion as the mole fractions approach parity with the capping and base layers. From Fig. 4.16(a) it can be seen that J_P is extracted as 29.2 A/cm^2,

5.5 nm	$In_{0.70}Ga_{0.30}As$: Be	1×10^{19} cm^{-3}
5 nm	$In_{0.40}Ga_{0.60}As$: Be	1×10^{19} cm^{-3}
3 nm	$In_{0.40}Ga_{0.60}As$	uid
300 nm	$In_{0.70}Ga_{0.30}As$: Si	1×10^{19} cm^{-3}
Substrate	InP	

(a) SSG-TD5



(b) SSG-TD5 family of I-V curves

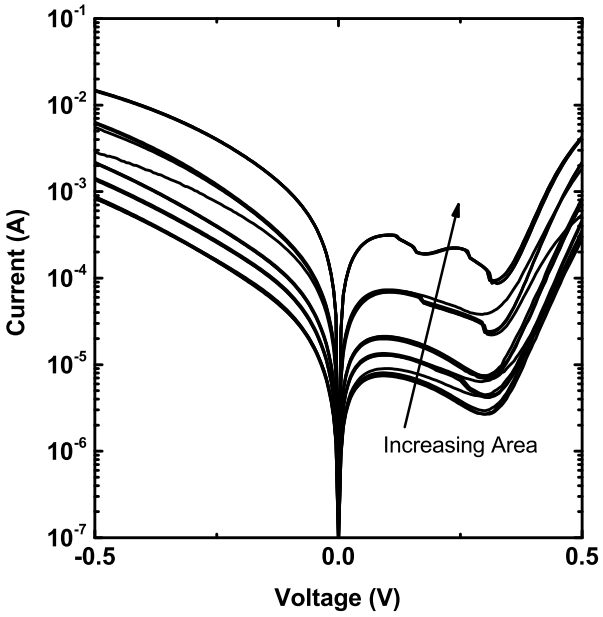
Figure 4.14: (a) Schematic of the film stack for the strained staggered gap Esaki diode SSG-TD5 with an $In_{0.40}Ga_{0.60}As$ tunnel region. (b) I-V curves for SSG-TD5 show scaling with area reduction. Additionally, lower J_P and PVCR values relative to SSG-TD4 and SSG-TD6 are seen.

22.7 A/cm^2, and 79.4 A/cm^2 for SSG-TD4, SSG-TD5, and SSG-TD6 respectively. From this data set it is difficult to discern if the differences are due to strain, defects, or E_G in the tunnel region. However, as the mole fraction approaches parity with the cap and base layers it does exhibit improved J_P. PVCR for the samples was extracted in Fig. 4.16(b), and median values were found to be 1.1, 1.7, and 3.1 for SSG-TD4, SSG-TD5, and SSG-TD6. It is expected that the values should follow the strain relative to the capping and base layers, but SSG-TD4 and SSG-TD5 appear out of order in this respect. The maximum PVCR values, however, do follow the expected trend at 2.53, 1.98, and 3.75, respectively. This difference may be due to yield differences between the samples, as the SSG-TD4 sample set of 59 devices is low relative to many of the other systems reported in this work.

Overall, the strained SSG sample study data wasn't very compelling. J_P values generally tracked with expectations, as did PVCR. When compared to $In_{0.53}Ga_{0.47}As$,

5.5 nm	$In_{0.70}Ga_{0.30}As$: Be	1×10^{19} cm^{-3}
5 nm	$In_{0.60}Ga_{0.40}As$: Be	1×10^{19} cm^{-3}
3 nm	$In_{0.60}Ga_{0.40}As$	uid
300 nm	$In_{0.70}Ga_{0.30}As$: Si	1×10^{19} cm^{-3}
Substrate	InP	

(a) SSG-TD6



(b) SSG-TD6 Family of Curves

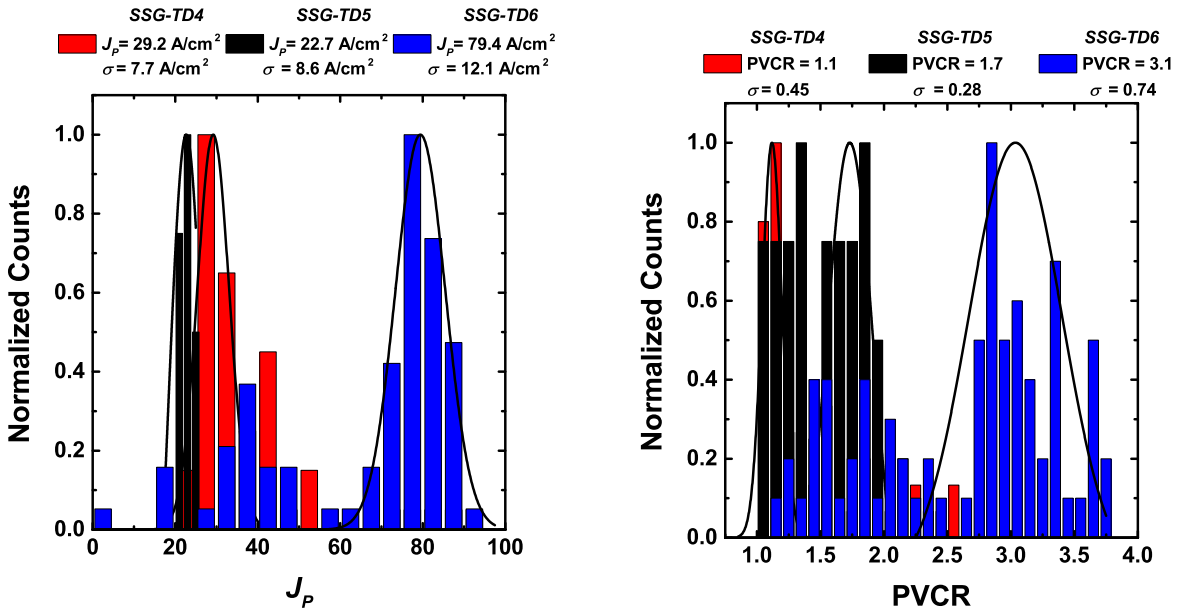
Figure 4.15: (a) Schematic of the film stack for the strained staggered gap Esaki diode SSG-TD6 with an $In_{0.60}Ga_{0.40}As$ tunnel region. (b) *I-V* curves for SSG-TD6 show scaling with area reduction. SSG-TD6 appears to exhibit the highest PVCR and J_P values, likely due to the closer lattice match to the straining layers.

Table 4.2: Summary of device information and extracted values

Device	Be $\times10^{19}$ (cm^{-3})	Si $\times10^{19}$ (cm^{-3})	N^* $\times10^{19}$ cm^{-3}	$N^{*-0.5}$ $\times10^{-10}$ cm^{-3}	J_P (A/cm^2) mean	J_P (A/cm^2) σ	J_V (A/cm^2) mean	J_V (A/cm^2) σ	PVCR mean	PVCR max	PVCR σ
SSG-TD4‡	1	1	0.5	4.47	29.2	7.7	23.3	12.9	1.1	2.53	0.45
SSG-TD5‡	1	1	0.5	4.47	22.7	8.6	13.5	4.6	1.7	1.98	0.28
SSG-TD6‡	1	1	0.5	4.47	79.4	12.1	23.9	12.8	3.1	3.75	0.74

‡ InP Substrate

the data shows a relation to mole fraction and E_G but doesn't vary much from expected J_P values for a 5×10^{18} cm^{-3} N^* effective doping level as seen in Fig. 4.17. Table 4.2 summarizes the results for the strained SSG samples. A possible alternative approach to straining the samples may be though ILD deposition similar to the oxide/nitride interaction for CMOS [2].



(a) Strained SSG J_P

(b) Strained SSG PVCR

Figure 4.16: J_P and PVCR histograms for strained SSG samples. (a) J_P values decreased with tensile strain which may indicate an unfavorable change in m^*. However, the strain samples are also likely affected by the increased E_G seen at the tunneling interface [30]. (b) PVCR are, on average low, indicating a number of defects are increasing excess current and masking strain effects on PVCR.

4.4 Small Stagger Gap Conclusions

This chapter demonstrated the implementation of SSG $In_{0.53}Ga_{0.47}As/GaAs_{0.50}Sb_{0.50}$ heterojunctions on InP substrates and how their performance compares to $In_{0.53}Ga_{0.47}As$. Utilizing band offsets provided an effective E_G of 0.59 eV, between $In_{0.53}Ga_{0.47}As$ and InAs, which performed in the expected regime as seen in Fig. 4.17. Pushing doping density in SSG-TD2 exhibited a max J_P near 570 kA/cm^2, well below 10 MA/cm^2. SSG-TD3 yielded a null result due to high excess currents caused by high defect density. Were it not for the defects, this sample would have likely performed similarly to InAs. Strained sample performance was similar to $In_{0.53}Ga_{0.47}As$ at equivalent doping levels. Results for the SSG devices are summarized in Table 4.3

Table 4.3: Summary of SSG device information and extracted values

Device	C $\times 10^{19}$ (cm^{-3})	Si $\times 10^{19}$ (cm^{-3})	N^* $\times 10^{19}$ cm^{-3}	$N^{*-0.5}$ $\times 10^{-10}$ cm^{-3}	J_P (kA/cm^2)		J_V (kA/cm^2)		PVCR		
					mean	σ	mean	σ	mean	max	σ
SSG-TD1‡	1.7	9	1.43	2.64	91.3	7.3	33.3	6.6	2.75	16.4	0.25
SSG-TD2‡	5.5	12.0	3.77	1.63	572	80	179	43.5	3.11	12.9	0.85
SSG-TD3‡	2.45	3.0	1.35	2.72	–	–	–	–	–	–	–
SSG-TD4‡	1	1	0.5	4.47	29.2	7.7	23.3	12.9	1.1	2.53	0.45
SSG-TD5‡	1	1	0.5	4.47	22.7	8.6	13.5	4.6	1.7	1.98	0.28
SSG-TD6‡	1	1	0.5	4.47	79.4	12.1	23.9	12.8	3.1	3.75	0.74

‡ on InP Substrates

Over 700 devices were tested between SSG-TD1 and SSG-TD2 samples. This volume of testing created a large dataset from which values of J_P, J_V, and PVCR were extracted and contrasted. SSG-TD2 exhibited high PVCR and J_P performance, indicating further improvements may be possible. Strained sample results indicate that may have negative implications for device performance if not considered. This information exhibits how slight changes in gap stagger can have somewhat profound results. This chapter demonstrates that a small stagger increases J_P for an equivalent homojunction doping density. Further enhancements to J_P can be made through larger staggers as seen in Chapter 5.

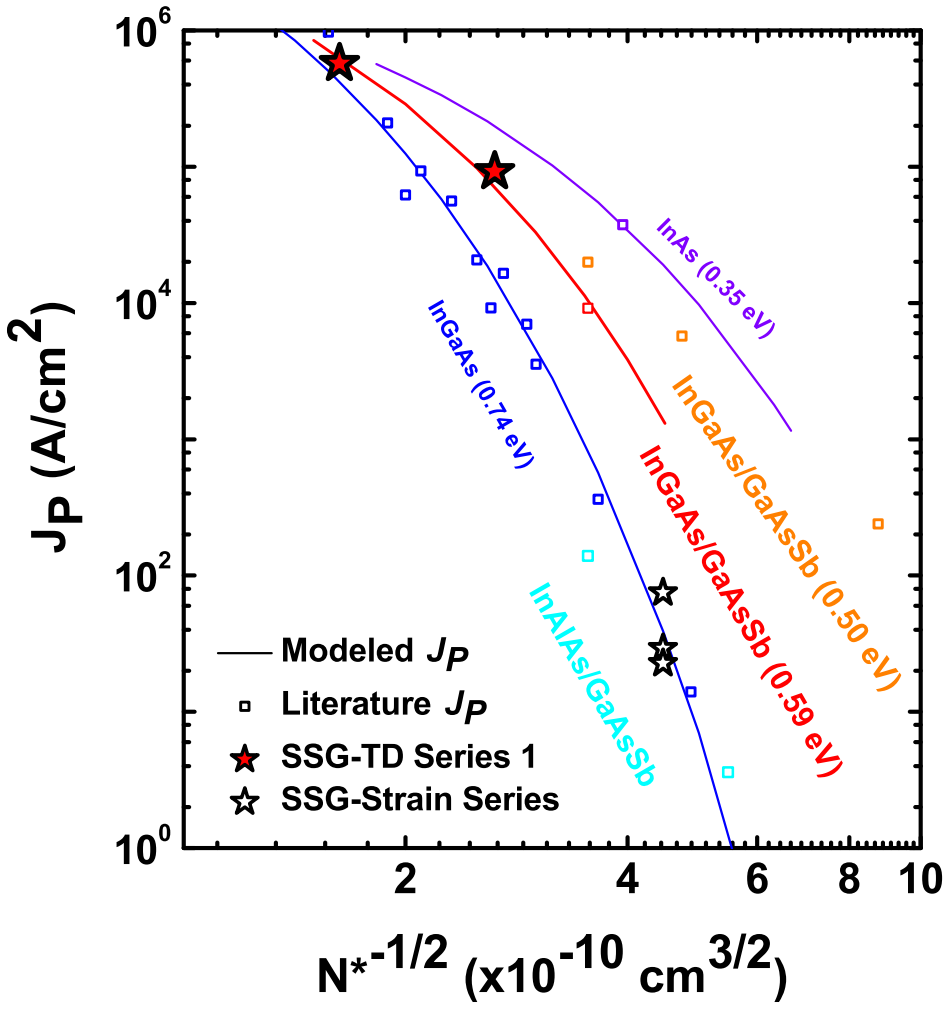


Figure 4.17: Figure of merit plot for the SSG series samples *vs.* other material systems [27, 54, 62] with an exponential fit showing that a 10 MA/cm^2 J_P for this material system may not be possible before dopant activation becomes a serious concern.

Chapter 5

Large Stagger Gap/Type II Heterojunctions

5.1 Introduction

Chapter 4 presented the results from small stagger gap (SSG) Esaki diodes fabricated by molecular beam epitaxy (MBE). Samples exhibited negative differential resistance, confirming tunneling behavior. Relative to homojunction $In_{0.53}Ga_{0.47}As$ Esaki diodes, the SSG samples produced higher current density (J_P) values for equivalent doping density. Increased J_P, coupled with a reduced effective band gap (E_G), confirms the hypothesis that a heterojunction with a smaller effective gap will exhibit superior performance. This chapter builds upon the previous study, presenting several large stagger gap (LSG) devices, and further confirms the improvements to tunnel current through band gap engineering.

LSG samples in this chapter are varied in two ways: (i) % Al content is varied from 20% to 60%, and (ii) doping density for the 40% Al content sample is varied from 9.8×10^{17} cm^{-3} to 2.5×10^{19} cm^{-3}. Large stagger is confirmed to improve J_P for the same doping density and increased Al content decreased J_P.

5.2 Large Staggered Gap Esaki Diodes (LSG)

Four samples are in the preliminary $InAs_{0.91}Sb_{0.09}/Al_{0.40}Ga_{0.60}Sb$ set, LSG-1 through LSG-4, which were sourced through two different epitaxial growers, IQE and Intelliepi. This experiment determined the relationship between doping and current density in heterojunction diodes with an $Al_{0.40}Ga_{0.60}Sb$ p type region. Sample LSG-1 was provided by SEMATECH through Intelliepi and targeted $> 5{\times}10^{19}$ cm^{-3} Si doping in the $InAs_{0.91}Sb_{0.09}$ layer and $5{\times}10^{19}$ cm^{-3} C doping in the $Al_{0.40}Ga_{0.60}Sb$ region. Remaining samples were procured through IQE and targeted $> 5{\times}10^{19}$ cm^{-3} Si doping in the $InAs_{0.91}Sb_{0.09}$ layer and varied from $1{\times}10^{18}$ cm^{-3} to $1{\times}10^{19}$ cm^{-3} Be doping in the $Al_{0.40}Ga_{0.60}Sb$ region. Knoch and Appenzeller [35] have proposed TFETs based on varying Al composition to address the issues that may be associated with the off-state [35]. Results from these designs would hint that this system may approach the 10 MA/cm^2 target, but will likely be a little short of the target.

5.2.1 Experimental Setup

The LSG series is designed to have a more aggressive stagger than those in the SSG series. Where SSG samples had an E_{Geff} of 0.59 eV,$\approx$ 0.2 eV ΔE_G from their constituent materials, the LSG series E_{Geff} is significantly smaller, $\approx$ 0.08 eV E_{Geff}; smaller than either $Al_{0.40}Ga_{0.60}Sb$ or $InAs_{0.91}Sb_{0.09}$. From Fig. 5.1 the difference in stagger is very apparent and should increase J_P commensurately.

As with the samples in the previous chapter, LSG-1 through LSG-4 were grown via MBE. However, changes were made to accommodate the difference in material systems. LSG-1 was grown on a 0.35° misscut towards <111> <100> GaSb wafer. All other samples were grown on <100> GaSb wafers, as confirmed by a 0.35° offset in substrate peak in XRD measurements. Devices consisted of a degenerately Si doped n-type $InAs_{0.91}Sb_{0.09}$ layer, a small $InAs_{0.91}Sb_{0.09}$ intrinsic region, followed by

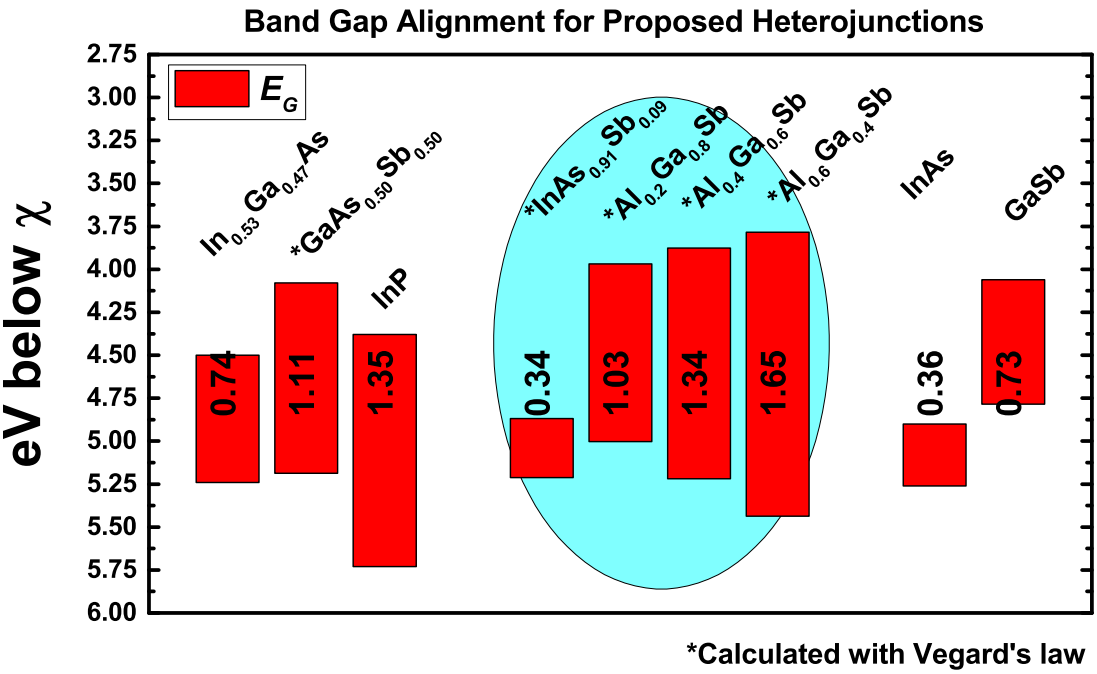


Figure 5.1: A relatively small decrease in the effective tunnel barrier for the SSG series resulted in significant gains in J_P, greater gains in J_P are expected for the LSG series which has a much smaller effective band gap.

a degenerately C, or Be, doped p-type $Al_{0.40}Ga_{0.60}Sb$ layer grown directly on the substrate. Schematics for the specific device designs are shown in Fig. 5.2

Fabrication for the LSG sample set largely follows those used for the SSG set. However, slight variations to etch time due to a faster etch rate for $InAs_{0.91}Sb_{0.09}$ *vs.* $In_{0.53}Ga_{0.47}As$ were required. Additionally, citric acid is highly selective [145, 146]to $InAs_{0.91}Sb_{0.09}$ over $Al_{0.40}Ga_{0.60}Sb$ so overetching beyond the p-type region is not an issue.

5.2.2 Results

Diodes from the LSG series required small contact areas to consistently show NDR behavior, in contrast to the SSG series which could often be probed following mesa etch. Additional development of the contact was also necessary, as the n-type contacts to III-V's didn't work well with liftoff processes as seen in Fig 5.3 a move to a metal first process became necessary. Initial samples tested Ta as a contact metal because

60 nm	$InAs_{0.91}Sb_{0.09}$: Si	$>4\times10^{19}$ cm^{-3}
3 nm	$InAs_{0.91}Sb_{0.09}$	uid
300 nm	$Al_{0.40}Ga_{0.60}Sb$: Be	5-10$\times10^{19}$ cm^{-3}
Buffer	$Al_{0.40}Ga_{0.60}Sb$: Be	
Substrate	GaSb	

(a) LSG-TD1

60 nm	$InAs_{0.91}Sb_{0.09}$: Si	$>5\times10^{19}$ cm^{-3}
3 nm	$InAs_{0.91}Sb_{0.09}$	uid
30 nm	$Al_{0.40}Ga_{0.60}Sb$: Be	1×10^{19} cm^{-3}
Substrate	GaSb	

(c) LSG-TD3

60 nm	$InAs_{0.91}Sb_{0.09}$: Si	$>5\times10^{19}$ cm^{-3}
3 nm	$InAs_{0.91}Sb_{0.09}$	uid
30 nm	$Al_{0.40}Ga_{0.60}Sb$: Be	5×10^{18} cm^{-3}
Substrate	GaSb	

(b) LSG-TD2

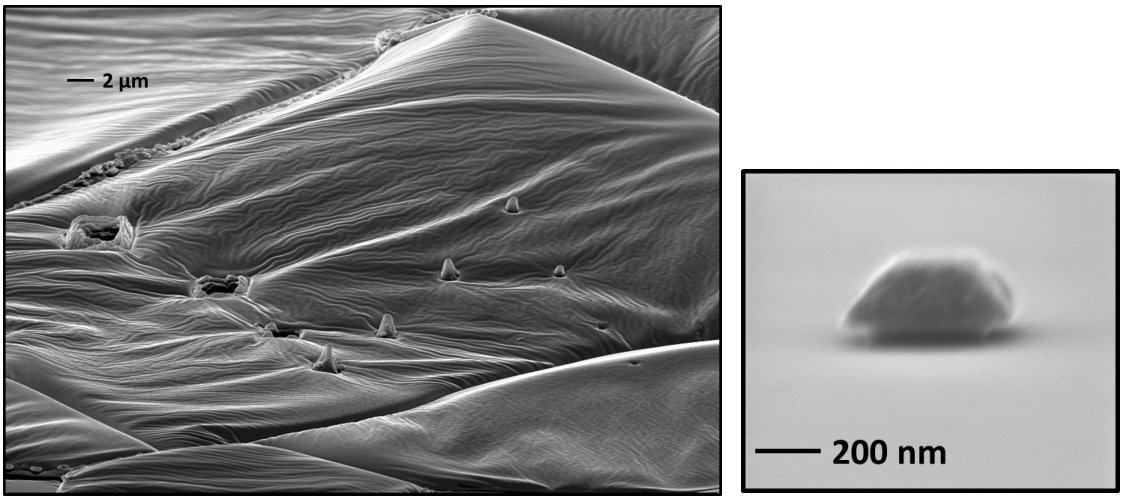
60 nm	$InAs_{0.91}Sb_{0.09}$: Si	$>5\times10^{19}$ cm^{-3}
3 nm	$InAs_{0.91}Sb_{0.09}$	uid
30 nm	$Al_{0.40}Ga_{0.60}Sb$: Be	1×10^{18} cm^{-3}
Substrate	GaSb	

(d) LSG-TD4

Figure 5.2: Schematic of the film stacks for samples LSG-1 through LSG-4. Doping levels are varied so as to extract the relationship between N^* and J_P. LSG-TD2 through LSG-TD4 have a very narrow p-type region which may cause issues related to spreading resistance.

it was easy to image in the SEM and had a work function compatible with n-type $InAs_{0.91}Sb_{0.09}$, this would provide additional benefit as a fiducial for L2 alignment. However, between BCB and level 2 metallization, the contact properties changed to be very resistive. This material was thought to be Ta_2O_5, which can be difficult to remove and is resistive. Highly resistant contacts would then require biases that exceeded the carrying capacity of the small diodes and would yield null results. A such, contacts were changed to Mo resulting in a more robust contact at the expense of poorer contrast for L2 alignment.

After reaching L2, devices as small as 4.9×10^{-10} cm^2 were measured and exhibited tunneling characteristics. LSG-TD1 through LSG-TD3 behaved as expected, but LSG-TD4 did not exhibit NDR as seen in Fig. 5.4. Thus the minimum p-type doping lies somewhere between 1×10^{18} cm^{-3} and 5×10^{18} cm^{-3}, though lower doping in the $InAs_{0.91}Sb_{0.09}$ could still be expected to provide tunneling characteristics so long as the doping density does not fall much below 8×10^{18} cm^{-3}. Though LSG-TD4 failed to



(a) Ta Contact to LSG Samples **(b)** Mo Contact to LSG Samples

Figure 5.3: (a) Initial attempts to utilize liftoff processes for refractory metal contacts to the LSG samples required a major shift in procedure. (b) Changing from lift-off to a metal first and etch back process eliminated issues with sidewall metal coating *and* had the benefit of producing smaller L1 contacts. Processes for both Mo and W were developed for L1 contacts, but the limited availability of W lead to Mo utilization as the contact for most devices.

show NDR, it does show promise as a possible TFET material as had been suggested by Knoch and Appenzeller [35]. LSG-TD1, TD2, and TD3 show increasing J_P with doping density, but may fall short of being able to deliver 10 MA/cm^2.

Over 200 devices were measured for each sample to create a good statistical data set for J_P, J_V, and PVCR extraction. From Fig. 5.5(a) it can be seen that I-V scales with area and there do not appear to be any surface leakage effects reducing device performance. Outliers are most likely due uncertainty related to area approximation, since there were significant variations in device area as devices were written farther from the die center. Smaller devices were more adversely affected by the variation, as it was often in one direction and lead to areas far smaller than targeted.

Comparing the V_P for each device, there are some drastic differences between LSG-TD1 and the rest of the sample set in Fig. 5.5(b). V_P is affected by a number of factors: doping, band overlap (for heterojunctions), and series resistance. However, V_P for LSG-TD1 is close to 0.2 V below that of LSG-TD2. A difference greater than

the 10's of mV which is typical for differently doped devices of the same material system. Additionally the band overlap for the 40% Al LSG series samples can be considered the same, excluding the differences due to doping. Only R_S remains as an explanation for the significantly higher V_P values for LSG-TD2 and LSG-TD3. PVCR and J_V are affected by the V_P shift in that PVCR will be significantly lower and J_V analysis will be uninteresting. As such, LSG-TD2 and LSG-TD3 will only be analyzed through histogram data because very little information can be extracted from their J_V and I_V/I_P/PVCR *vs.* area plots.

J_P for samples that showed PVCR were extracted from a Gaussian fit to a histogram of J_P data from Fig. 5.6. Distribution tails for the devices trended towards the high side due to overestimated areas. LSG-TD1 was found to have a J_P of 874 kA/cm^2, followed by 521 kA/cm^2 and 356 kA/cm^2 for LSG-TD2 and LSG-TD3, respectively. LSG-TD4 exhibited diffusion current characteristics, but could be expected to show tunneling with a modest Voltage application. The highest J_P was still lower than the record $In_{0.53}Ga_{0.47}As$ J_P of 972 kA/cm^2 [28], but at a much lower N^*.

PVCR for the LSG series was extracted from histograms of all the PVCR data. From Fig. 5.7 LSG-TD1 gives the highest median value of 1.48, whereas LSG-TD3 and LSG-TD2 followed at 1.03 and 1.01, respectively. However, the maximum PVCR is often the number reported by literature; as such, the values were found to be 3.05, 1.15, and 1.19 for LSG-TD1, LSG-TD2, and LSG-TD3. Low PVCR may be attributed to a number of factors. Generally, large excess current will severely limit PVCR. However, the very narrow p-region likely leads to increased spreading resistance which can also have the effect of reducing PVCR. Additionally, the epitaxy benefits of a miss cut may be offset by increased excess currents despite a reduced defect density and other mechanisms which suppress excess current.

Fig. 5.8 represents the typical *I-V* characteristics of LSG-TD1 devices with mask defined areas from 0.25 μm^2 to 400 μm^2. NDR is very clearly observed for many

devices, especially when compared against the other LSG samples. Excellent current scaling is represented as devices reach smaller sizes. V_P appears to rest between 0.3 V and 0.4 V as seen in Fig. 5.5(b) and hinted in Fig. 5.8. As in the SSG, an extended NDR region with a broader peak seems to be exhibited by LSG-TD1. This NDR region broadening may be due to additional tunneling paths that exist in heterojunctions that do not appear in their homojunction counterparts. These paths may have different cutoff voltages for tunneling, resulting in the more gradual slopes seen in the staggered gap systems.

Fig. 5.9 plots I_V, I_P, and PVCR against device area for LSG-TD1 and indicates scaling with area and variation between samples appears largely related to I_V. I_V and I_P scaling is fairly typical for well fabricated devices. Interestingly, the peak in PVCR appears near device areas close to 1 μm^2. Typically, PVCR maximums appear with the smallest devices since the range increases due to larger differences in the inclusion of defects/excess current paths between devices. Reduced PVCR at smaller device sizes indicates there may be some surface or processing effects that are affecting an increase in excess current.

HRXRD can indicate the presence of defects between samples and if there are differences in the substrates. From Fig. 5.10 a few characteristics can be inferred about the samples. First, the GaSb peak is shifted between the two samples. The slight shift is near 0.35° and a commonly used GaSb substrate for growth is miss cut in 0.35° in the <111> direction. In addition to the differences in how sample LSG-TD1 cleaved relative the rest of the set, it would appear that LSG-TD1 was grown on an intentionally miscut wafer. Peaks for $Al_{0.40}Ga_{0.60}Sb$ and $InAs_{0.91}Sb_{0.09}$ appear to be in the same general locations, but with some masking of $InAs_{0.91}Sb_{0.09}$ on LSG-TD1 due to an over lap with the substrate peak. Second, from peak heights, it can be seen that the $Al_{0.40}Ga_{0.60}Sb$ layer is thicker for LSG-TD1. Thus, it is very likely that differences in the PVCR between LSG-TD1 and the rest of the sample

set are related more to the thickness of the $Al_{0.40}Ga_{0.60}Sb$ region and R_S than defect originated excess currents.

SIMS was performed on LSG-TD1, and shows very high C doping in Fig. 5.12. However, this measurement was made using GaAs as a calibration sample and had greater than 50% uncertainty in the doping levels. Additional SIMS of LSG-TD2 through LSG-TD4 were not taken, due to cost and the volume of samples.

Table 5.1: Large Staggered Gap Tunnel Diodes

Device	p $\times 10^{19}$ (cm^{-3})	n $\times 10^{19}$ (cm^{-3})	N^* $\times 10^{19}$ (cm^{-3})	$N^{*-0.5}$ $\times 10^{-10}$ (cm^{-3})	J_P (kA/cm^2)		J_V (kA/cm^2)		PVCR		
					mean	σ	mean	σ	mean	max	σ
LSG-TD1†	4 C	5 Si	2.2	2.1	874	126	594	139	1.48	3.05	0.19
LSG-TD2‡	5 Be	1 Si	0.83	3.5	552	54	498	62	1.01	1.15	0.01
LSG-TD3‡	5 Be	0.5 Si	0.45	4.7	356	76	349	69	1.03	1.19	0.03
LSG-TD4‡	5 Be	0.1 Si	0.10	0.1	N/A		N/A			N/A	

† 0.35deg offcut to < 111 > GaSb Substrate
‡ < 100 > GaSb substrates

5.2.3 Large Stagger Gap Doping Study Conclusion

LSG samples containing 40% Al follow the hypothesis that reducing the tunnel barrier through band gap engineering is effective for increasing J_P for equivalent doping density. LSG-TD1, LSG-TD2, and LSG-TD3 were shown to have J_P values of 874 kA/cm^2, 552 kA/cm^2, and 356 kA/cm^2. LSG-TD4 exhibits J_P values significantly lower than LSG-TD3, indicating the candidacy of this system for TFETs. J_P for the LSG trends upwards with doping density, as expected. However, based on Fig. 5.11, it does not appear that the LSG series will quite meet the neccessary 10 MA/cm^2 value needed to make TFETs competitive with CMOS [4, 148]. Doping for both $Al_{0.40}Ga_{0.60}Sb$ and $InAs_{0.91}Sb_{0.09}$ would need to exceed 1×10^{20} cm^{-3} and the trendline indicates this system may not reach 2 MA/cm^2. In addition, there may be dopant activation and compensation issues once concentrations exceed 5×10^{19} cm^{-3}. Table 5.1 summarizes the results from the LSG 40% samples.

An issue seems to arise from a combination of excess current and spreading resistance in the IQE samples possibly due to substrate choice; most devices bigger

than 500 nm do not appear to exhibit NDR before a 1 V bias and devices under 300 nm rarely survive processing. Chidley et al. [149] has demonstrated a precipitous decrease in hole mobility with increased Al content in the AlGaSb system, this reduction in mobility leads to a problematic increase in resistance. One solution was to etch through the high resistance AlGaSb region and to use the GaSb to conduct current. However, the doping levels in the GaSb layer are too low for this process to work, and the calculated resistances of the $Al_{0.40}Ga_{0.60}Sb$ and GaSb happen to be fairly close in this instance. Any future iterations of this device family must be grown on more optimal surfaces so as to suppress excess current. Additionally, the resistance issues might be abated through a couple methods. First, utilizing a thicker $Al_{0.40}Ga_{0.60}Sb$ would reduce the resistance seen by the system as current travels to ground. Secondly, a degenerately doped buffer of GaSb could be grown on the substrate. This approach minimizes additional process development and utilizes the lower resistance of GaSb thereby reducing spreading resistance. Alternatively, devices could be built in reverse order but a suitable p-type contact would need to be utilized. Ni is a likely candidate due to the proximity of the work function to the valence band edge of AlGaSb, which addresses the issue of n-type regions through a high resistance p-region.

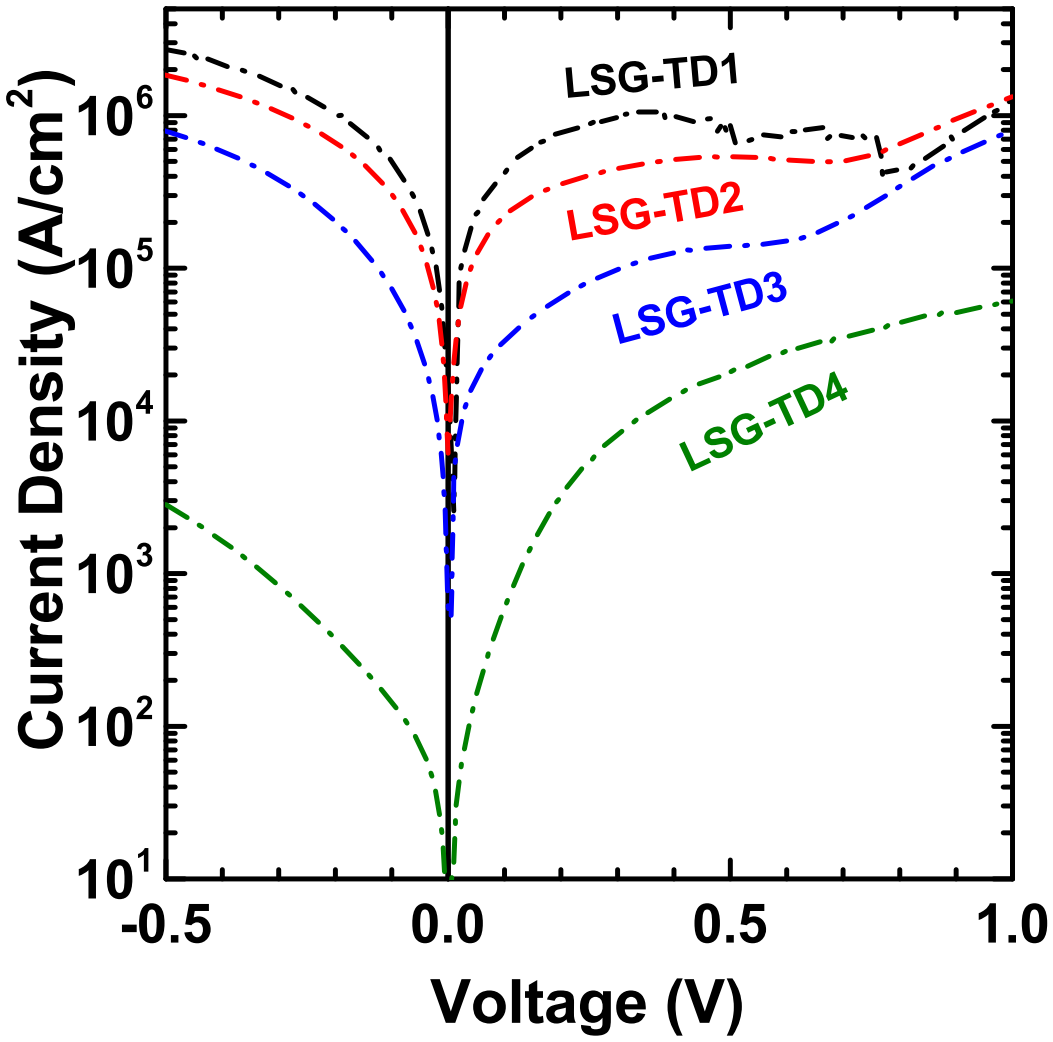
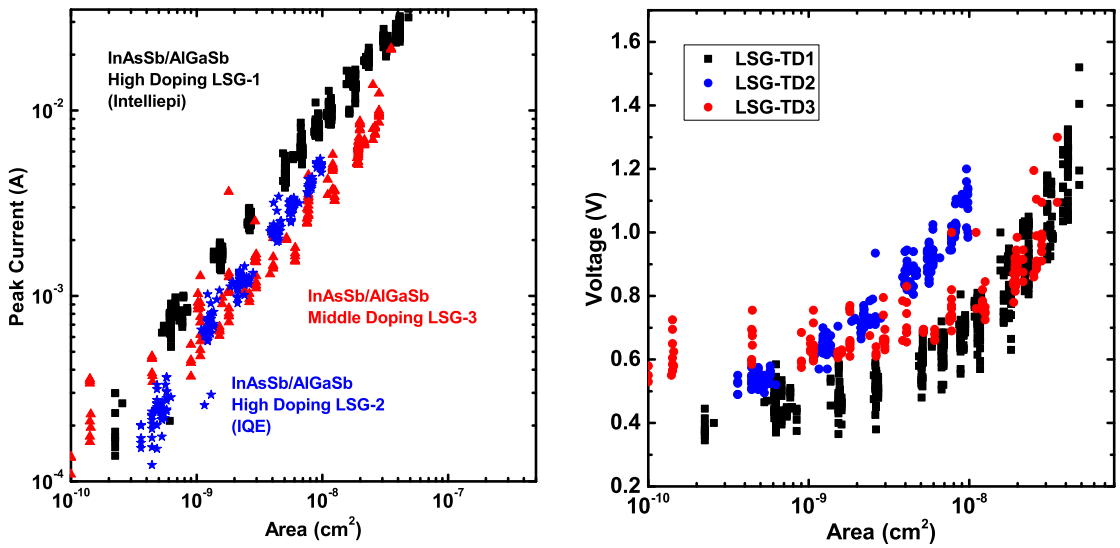


Figure 5.4: Family of J-V curves for similarly sized devices in the LSG series. LSG-1 exhibits the best J_P and PVCR, at 872 kA/cm^2 and 3.05, respectively. LSG-2 and LSG-3 show modest PVCR and J_P commensurate with their doping density, at 521 kA/cm^2 and 356 kA/cm^2. LSG-4 presents an interesting case, as no NDR is observed, but the doping is only 1/5 that of LSG-3 indicating a promising candidate material system for a TFET.



(a) I_P *vs.* area for LSG samples

(b) V_P *vs.* area for LSG samples

Figure 5.5: (a) Peak current scales with area for the 40% Al content LSG series. LSG-TD3 shows variation with reduced area which is likely due to an underestimated area for the shown devices.(b) V_P decreases with area as expected, however LSG-TD2 and LSG-TD3 show significantly higher V_P relative to similarly sized LSG-TD1 devices. While V_P variation is expected, LSG-TD1 should have the lowest because it is the highest doped, the large difference between the samples indicates there is likely a significant R_S in LSG-TD2 and LSG-TD3.

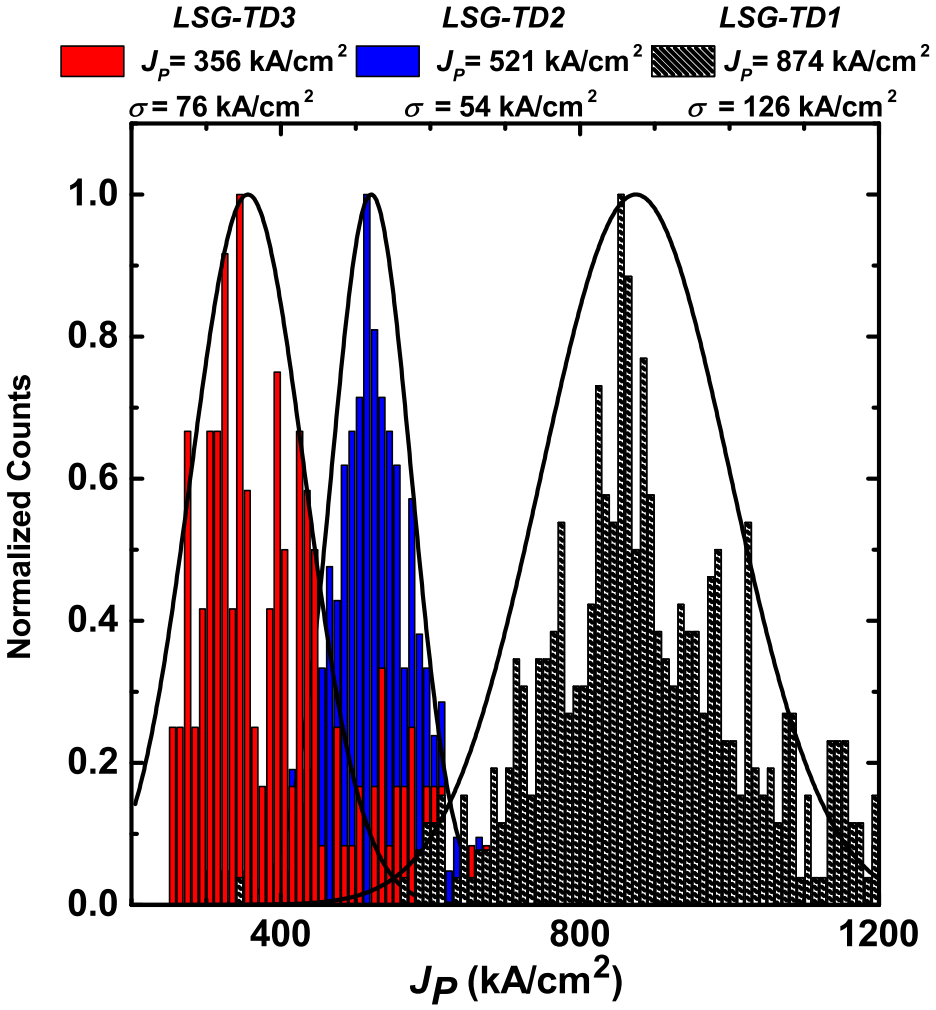


Figure 5.6: J_P of 874 kA/cm^2 was extracted from sample LSG-TD1, which was the highest reported J_P value for the $InAs_{0.91}Sb_{0.09}/Al_{0.40}Ga_{0.60}Sb$ system reported [147]. Dopant levels for both p and n-type may be pushed higher, but reaching a 10 MA/cm^2 target is questionable.

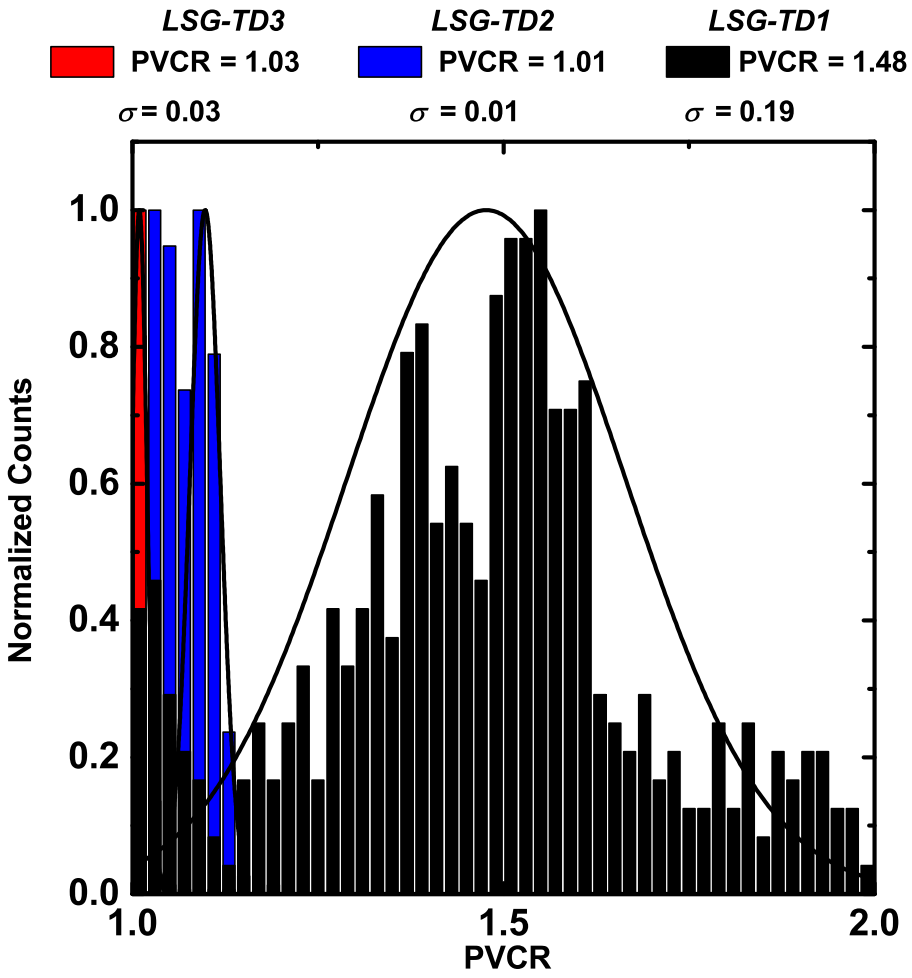


Figure 5.7: PVCR values of 1.48 (LSG-TD1), 1.01 (LSG-TD2), and 1.03 (LSG-TD3) were extracted from Gaussian fits to the histogram data. LSG-1 appears to exhibit the best PVCR performance, which may be related to the different substrate.

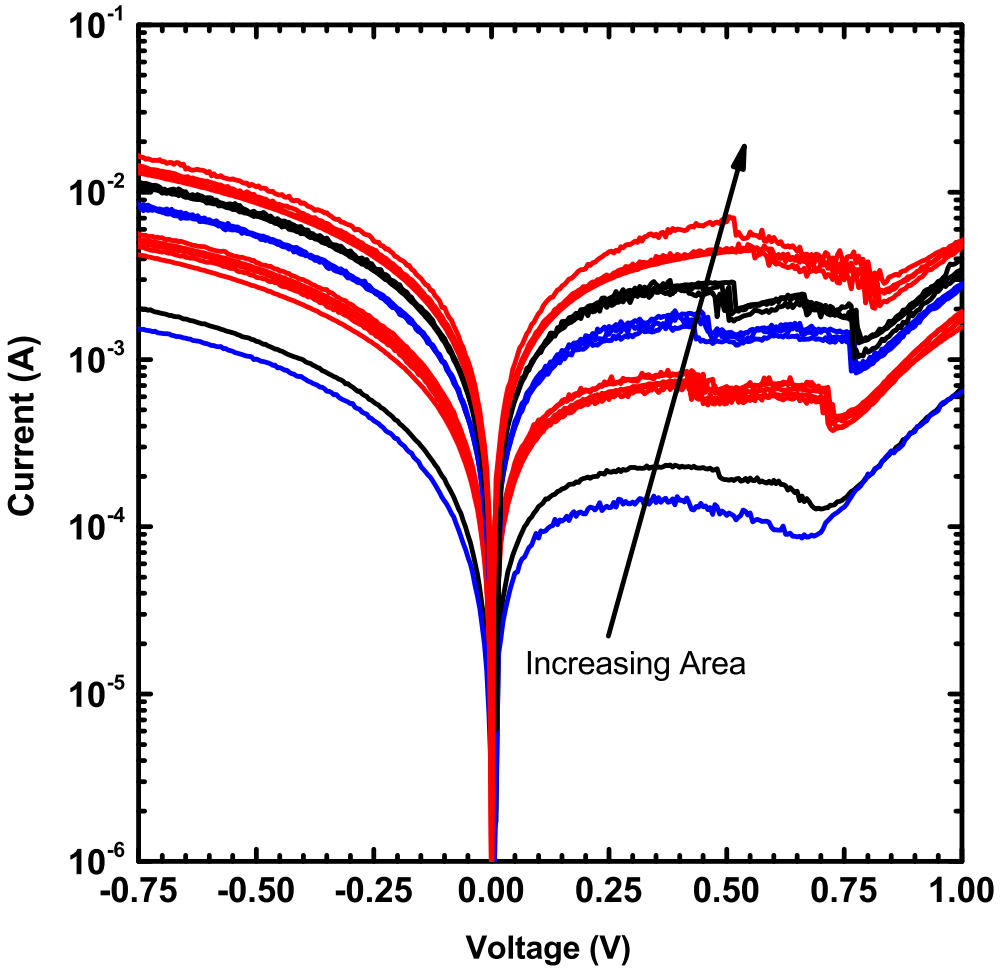


Figure 5.8: Family of I-V curves for LSG-TD1 show excellent current scaling area is reduced.

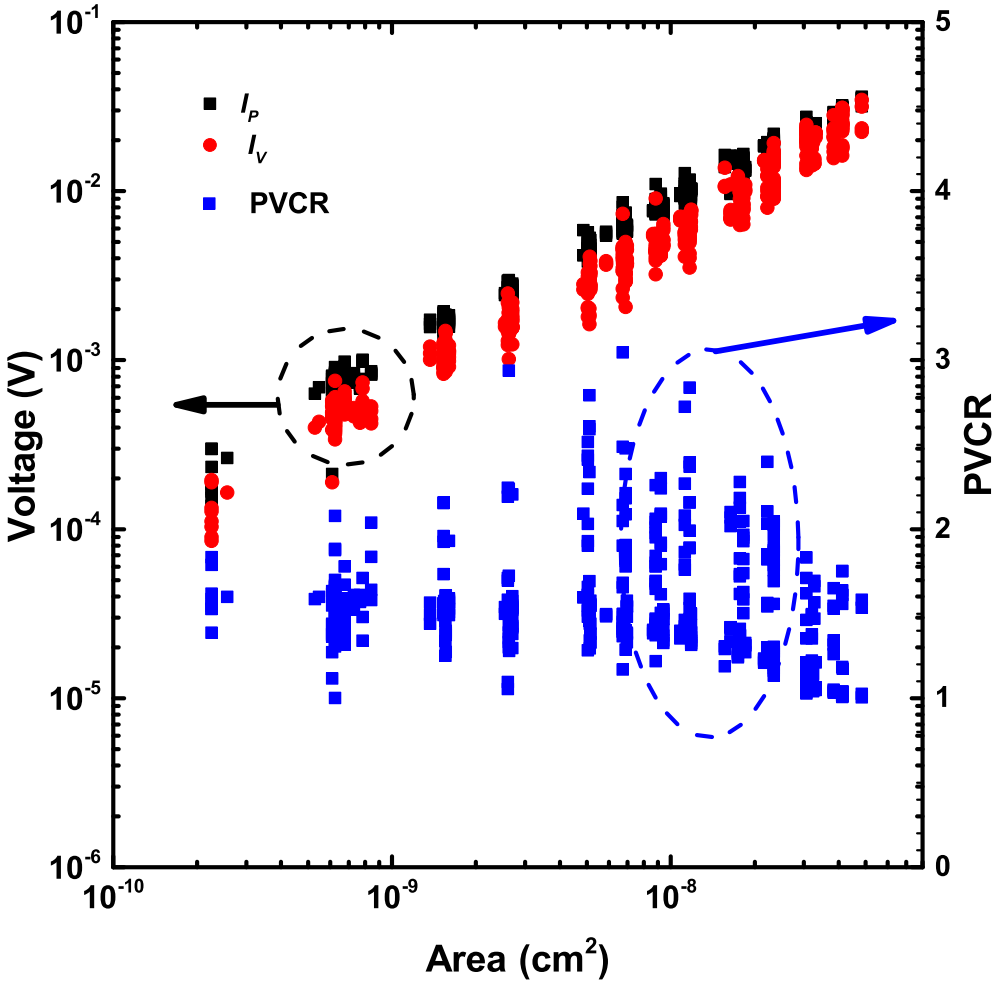


Figure 5.9: Current *vs.* area plot for LSG-TD1 which shows excellent scaling with area. PVCR is also plotted *vs.* area, and appears to have a peak which may be due to a number of leakage paths.

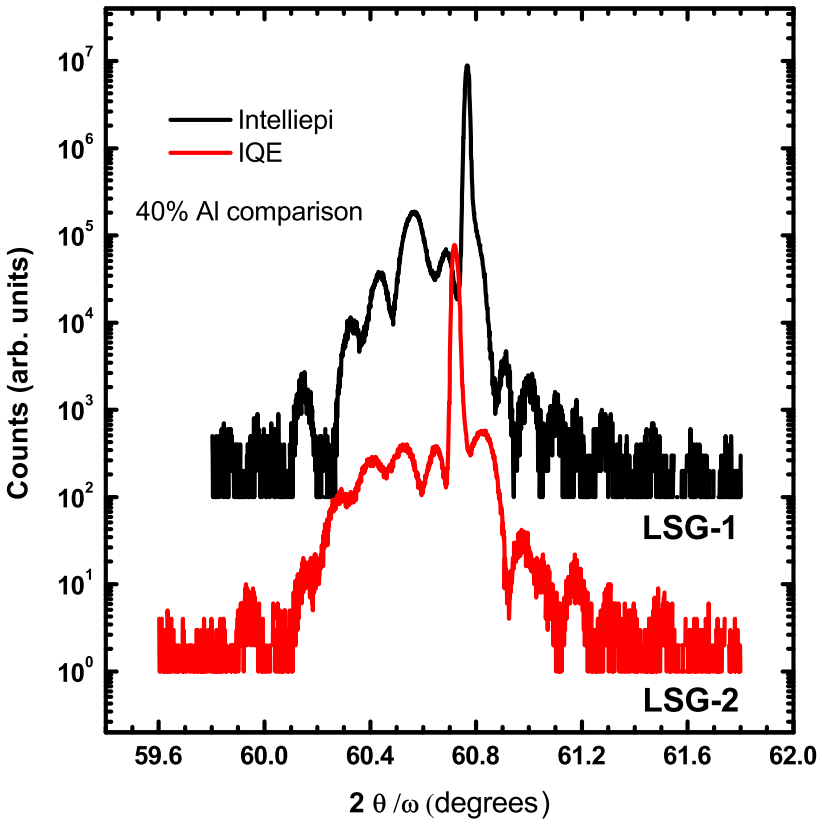


Figure 5.10: Comparing the $2\theta/\omega$ profiles for LSG-1 and LSG-2, one can see some differences. Notably the substrate peak is shifted from the (400) peak location due to the 0.35° miss cut. LSG-1 also exhibits sharper peaks for $InAs_{0.91}Sb_{0.09}$, as well as more pronounced fringes, and may have a slightly lower Al content than LSG-2 due to the shoulder instead of a peak to the right of the GaSb peak.

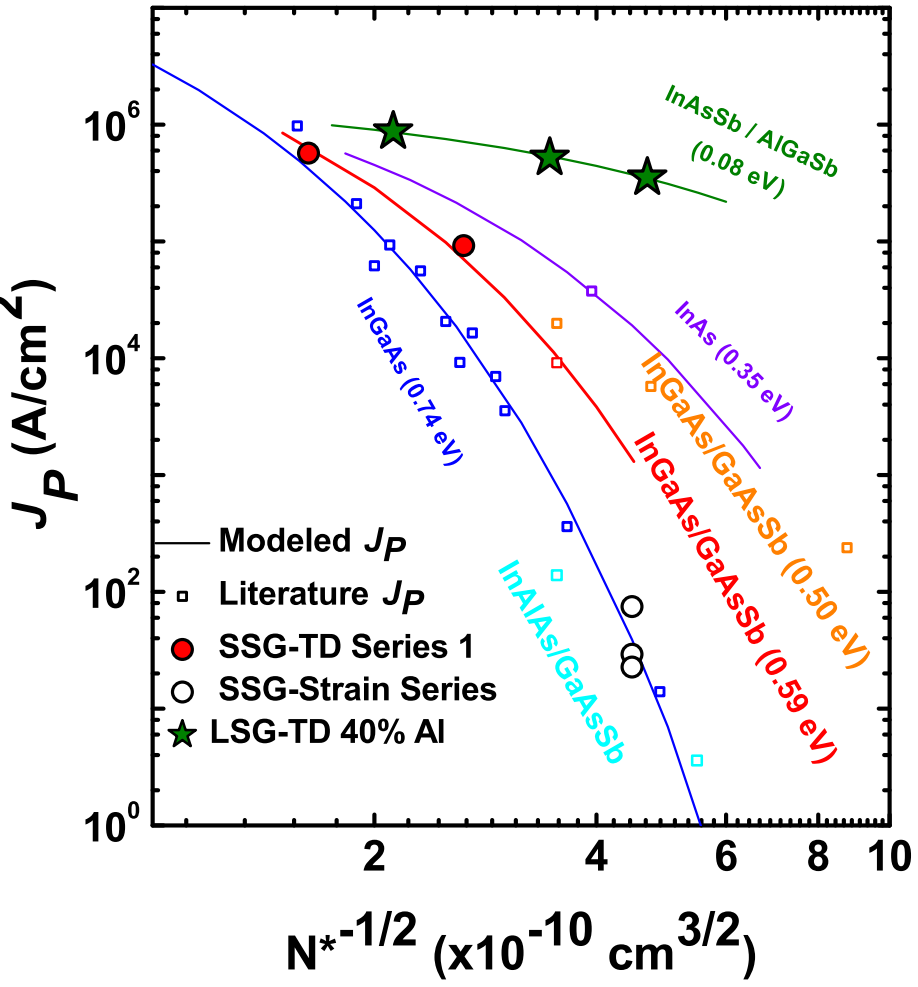


Figure 5.11: Figure of merit plot for the 40% Al LSG series samples with an exponential fit showing that a 10 MA/cm^2 J_P for this material system may not be possible.

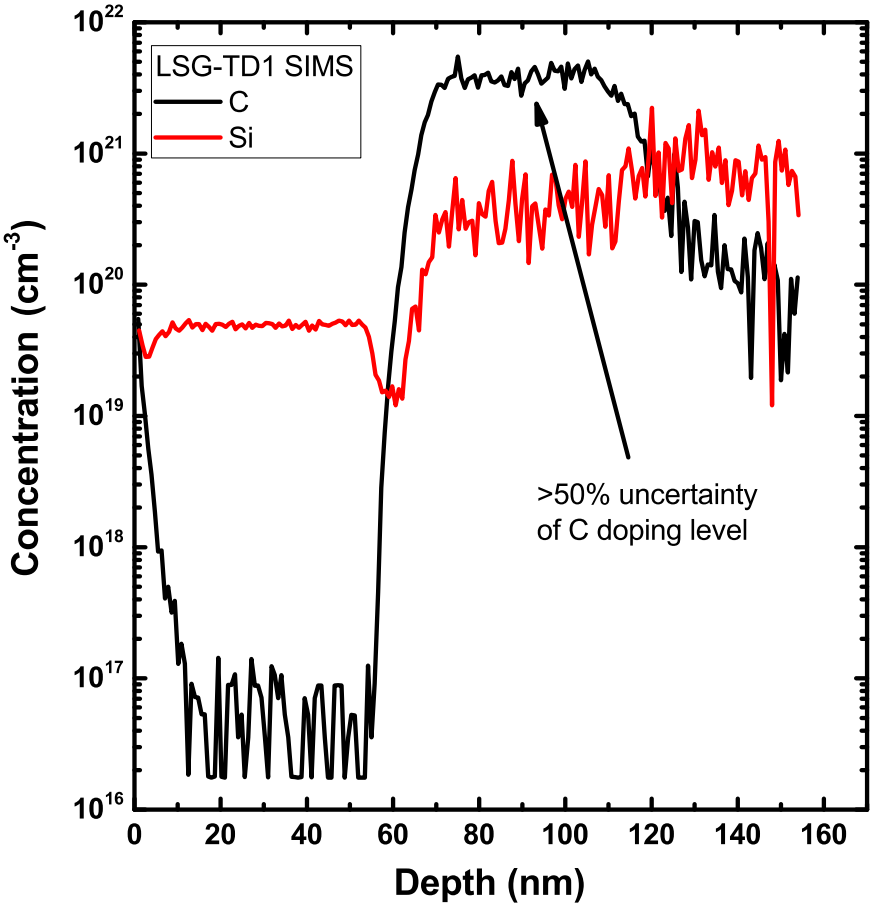


Figure 5.12: This SIMS plot for LSG-TD1, shows exceptionally high C levels while hitting the Si doping target. This shows an excellent junction profile, despite the uncertainty in the doping measurement.

5.3 Other Al content samples

Samples in this section are inspired by the modeling work of Knoch and Appenzellar [35] to show how an AlGaSb based system could prove useful for both p and n-type TFETs. LSG-TD5 and LSG-TD6 were designed to have the same N^* as LSG-TD3, but would vary Al content to 20% and 60% from the 40%. Utilizing the lowest doping levels should create a wider spread between devices to make any effects due to band gap more apparent.

5.3.1 20% Al content sample

In theory, reducing the Al content of the LSG series didoes will bring the system closer to a broken gap (BG) arrangement and will result in increased J_P relative to the trends shown in prior sections. Fig. 5.13 shows a schematic of LSG-TD5, where the $Al_{0.40}Ga_{0.60}Sb$ region has been replaced with a 20% Al content region. However, in this instance increasing the Ga content appeared to reduce the J_P for the sample.

60 nm	$InAs_{0.91}Sb_{0.09}$: Si	5×10^{19} cm^{-3}
3 nm	$InAs_{0.91}Sb_{0.09}$	uid
30 nm	$Al_{0.20}Ga_{0.80}Sb$: Be	5×10^{18} cm^{-3}
Substrate	GaSb	

Figure 5.13: Schematic of the film stack for LSG-TD5.

From Fig. 5.14 it can be seen that LSG-TD5 I-V scales with area. Also evident is that PVCR does not venture far from 1.01, this may be due leakage paths in (100) crystals that are mitigated by small miscuts as shown by the differences between LSG-TD1 and the remaining samples of this set. PVCR does increase with reduced area, but due to the issues affecting V_P , it does not stray far from 1.0. Spreading resistance is likely high due to the 30 nm $Al_{0.20}Ga_{0.80}Sb$, and is causing the reduced PVCR performance. Considering the very large V_P values shown in Fig. 5.15, the reduced PVCR for LSG-TD5 is likely due to R_S.

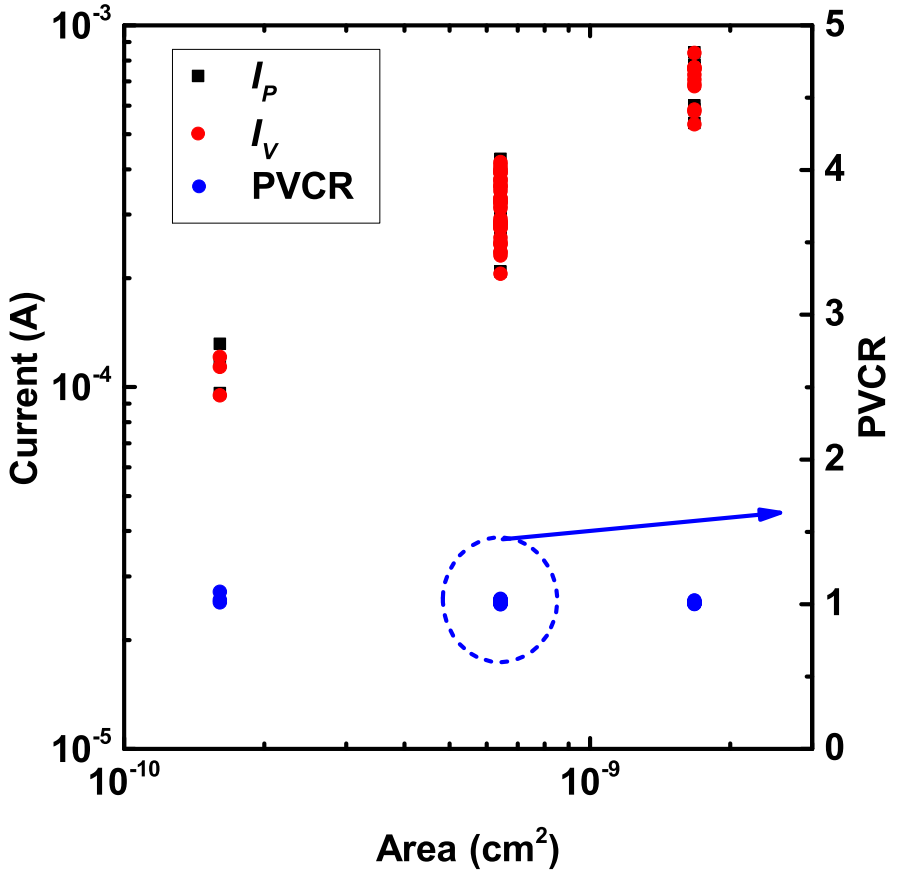


Figure 5.14: LSG-5 displays scaling with area, however due to undercut during wet etch most devices were etched away.

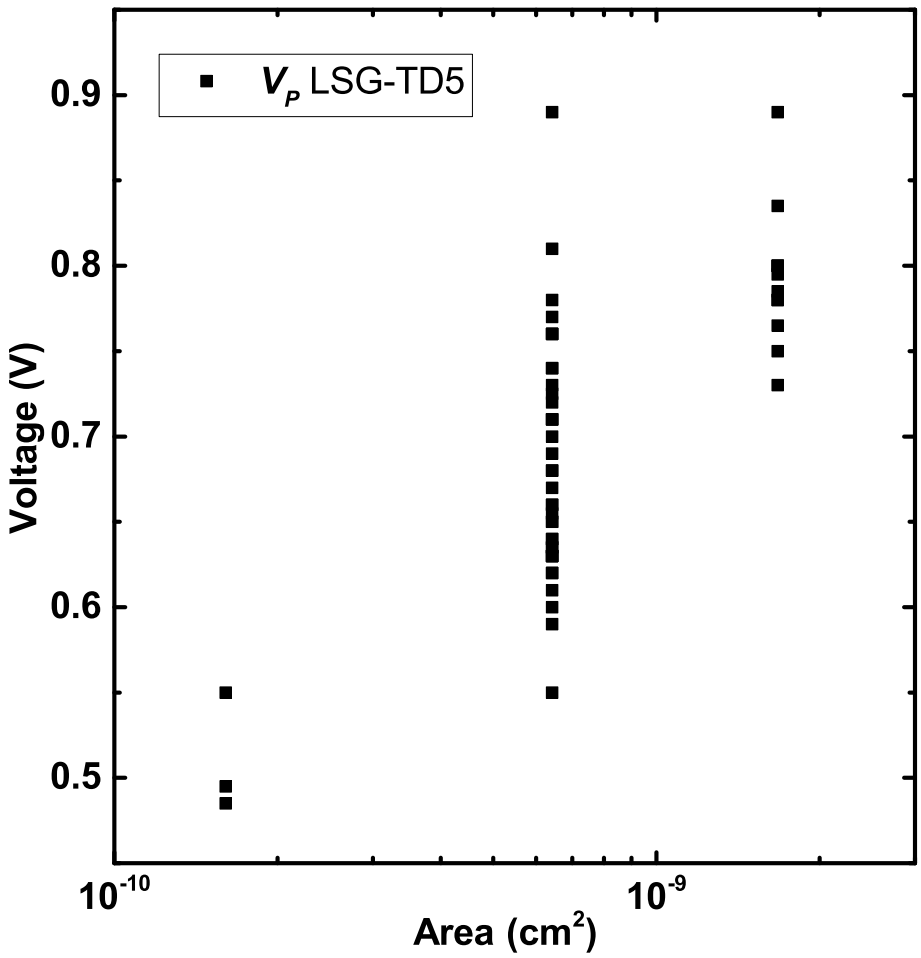
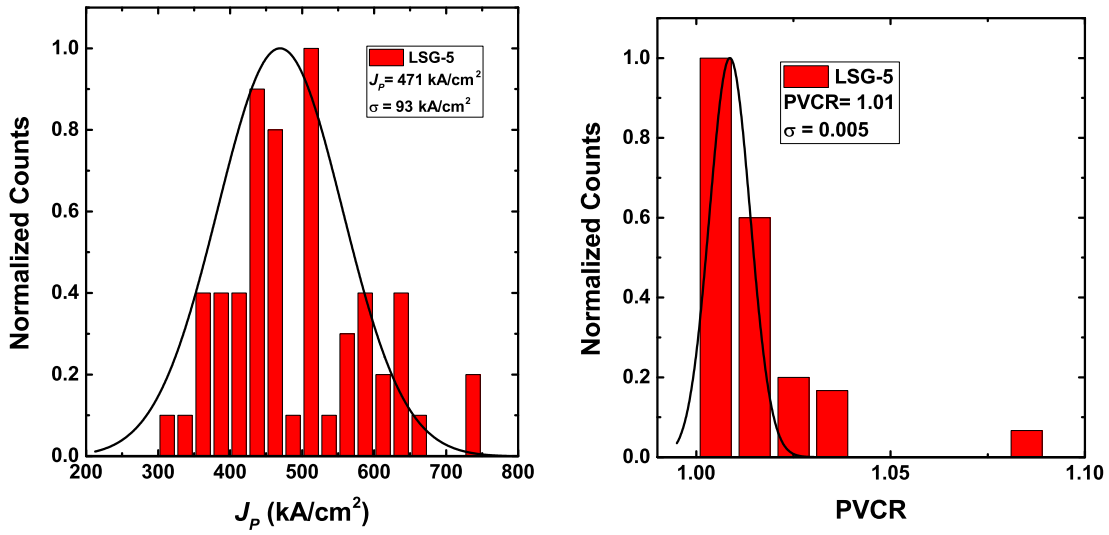


Figure 5.15: LSG-TD5 V_P values are very large, indicating the presence of large resistance values *vs.* excess current being the source of the small PVCR values.

Data from the 20% Al content InAsSb/AlGaSb samples indicate a reasonable large J_P, but large series resistance as evidenced by large V_P in Fig. 5.15. A respectable J_P of 471 kA/cm^2 was extracted for LSG-TD5 from the histogram in Fig. 5.16(a), a value less than LSG-TD2 the equivalent 40% Al content sample. This result is counterintuitive as the system should be nearly a broken gap diode at 20% Al, however considering the how few experiments have utilized this combination it is not surprising. Likely there are doping activation and optimization issues at play for this sample. J_V extraction for LSG-TD5 was considered uneccesary, as the PVCR values hovered near 1.0 and are therefore uninteresting. A median PVCR of 1.01 was extracted from



(a) LSG-5 J_P Histogram **(b)** LSG-TD5 PVCR Histogram

Figure 5.16: (a) A J_P of 471 kA/cm^2 was extracted from sample LSG-5, which is lower than anticipated and may be due to calibration differences between 20% and 40% Al content epitaxy at the grower. (b) A median PVCR of 1.01 was extracted from sample LSG-5, indicating significant excess currents.

Fig. 5.16(b), with a meager maximum of 1.10. Low PVCR values indicate that the sample has a very large excess current, or, more likely, a combination of spreading and series resistance. LSG-TD5 is compared to the rest of the sample set in Table 5.2, and shows the lower J_P relative to LSG-TD2.

Table 5.2: LSG summary table with 20% Al sample

Device	p $\times 10^{19}$ (cm^{-3})	n $\times 10^{19}$ (cm^{-3})	N^* $\times 10^{19}$ (cm^{-3})	$N^{*-0.5}$ $\times 10^{-10}$ (cm^{-3})	J_P (kA/cm^2) mean	σ	J_V (kA/cm^2) mean	σ	PVCR mean	max	σ
LSG-TD1†	4 C	5 Si	2.2	2.1	874	126	594	139	1.48	3.05	0.19
LSG-TD2‡	5 Be	1 Si	0.83	3.5	552	54	498	62	1.01	1.15	0.01
LSG-TD3‡	5 Be	0.5 Si	0.45	4.7	356	76	349	69	1.03	1.19	0.03
LSG-TD4‡	5 Be	0.1 Si	0.10	0.1	N/A		N/A			N/A	
LSG-TD5‡	5 Be	0.5 Si	0.83	3.5	471	93			1.01	1.10	0.005

† 0.35° offcut to < 111 > GaSb Substrate
‡ < 100 > GaSb substrates

5.3.2 60% Al content sample

Sample LSG-TD6 was to show the impact of decreasing the band overlap in the InAsSb/AlGaSb system. Fig. 5.17 shows a change in Al content while maintaining target doping levels. However, minimal data was retrieved from the sample. 200+

60 nm	$InAs_{0.91}Sb_{0.09}$: Si	$>5\times10^{19}$ cm^{-3}
3 nm	$InAs_{0.91}Sb_{0.09}$	uid
30 nm	$Al_{0.60}Ga_{0.40}Sb$: Be	5×10^{18} cm^{-3}
Substrate	GaSb	

Figure 5.17: Schematic of the film stack LSG-TD6.

devices were measured for LSG-TD6, but only four demonstrated tunneling characteristics. Therefore, only minimal qualitative analysis for the sample was realistic. Data from the 60% Al containing InAsSb/AlGaSb sample indicates a lower J_P than that of LSG-TD3 and LSG-TD5, in the ball park of 284 kA/cm^2. Only devices in row three, 4.9×10^{-9} cm^2 mask designed area, exhibited NDR which indicates that J_P may be over estimated. Additionally, only one PVCR value exceeded 1.1. Table 5.3 summarizes the results from LSG-TD6 and constrasts the device with the rest of the LSG series. It can be seen that by increasing Al content, a reduction in J_P can be expected. From Fig. 5.18 some slight relaxtion may be occuring in the $InAs_{0.91}Sb_{0.09}$ region due to widening peak near that of the substrate and is likely not the source for low device yield. LSG-TD6 exhibits characteristics of a spreading resistance limited system, similar to other devices tested by the group. In those cases, the resistance of the transit region between devices was large enough to completely mask tunneling characteristics. This increased resistance was overlooked during device design, but is in line with the findings of Chidley et al. [149] who showed the precipitous decrease in hole mobility in AlGaSb with increasing Al content.

However, PVCR near 1.01 is generally considered questionable for reporting pur-

Table 5.3: Summary of LSG series results

Device	p $\times 10^{19}$ (cm^{-3})	n $\times 10^{19}$ (cm^{-3})	N^* $\times 10^{19}$ (cm^{-3})	$N^{*-0.5}$ $\times 10^{-10}$ (cm^{-3})	J_P (kA/cm^2)		J_V (kA/cm^2)		PVCR		
					mean	σ	mean	σ	mean	max	σ
LSG-TD1†	4 C	5 Si	2.2	2.1	874	126	594	139	1.48	3.05	0.19
LSG-TD2‡	5 Be	1 Si	0.83	3.5	552	54	498	62	1.01	1.15	0.01
LSG-TD3‡	5 Be	0.5 Si	0.45	4.7	356	76	349	69	1.03	1.19	0.03
LSG-TD4‡	5 Be	0.1 Si	0.10	0.1	N/A		N/A			N/A	
LSG-TD5‡	5 Be	0.5 Si	0.83	3.5	471	93	-	-	1.01	1.10	0.005
LSG-TD6‡	5 Be	0.5 Si	0.83	3.5	285	-	-	-	1.01	1.01	-

† 0.35° offcut to < 111 > GaSb Substrate
‡ < 100 > GaSb substrates

poses. It is very likely that the spreading resistance of the 60% Al sample is masking the results. Inspection of the data would indicate a large spreading resistance which may be able to be designed out of future growths. One method for improved results would be to grow a degenerately doped contact layer below the $Al_{1-x}Ga_xSb$, a rough calculation of the resistance indicates that the substrate and ptype epitaxy are of similar resistance, a highly doped contact region could mitigate problems associated with this resistance. Alternatively, the device could be grown upside down on an InAs starting substrate, creating a low resistance path to ground. A respectable J_P, 285 kA/cm^2, was estimated for this sample, though SIMS and additional data points are necessary to confirm this J_P and N^*.

5.3.3 %Al Content Conclusions

Comparing results from Table 5.3 it can be seen that LSG-TD2 exceeds the performance of both LSG-TD5 and LSG-TD6. LSG-TD5 and LSG-TD6 do follow the trend of increased stagger yielding greater J_P, however LSG-TD2 does not fit with this result. Because $Al_{0.40}Ga_{0.60}Sb$ is a much more common film, [35] it is probable that achieving target active doping levels is better known and that LSG-TD5 and LSG-TD6 have lower active levels resulting in lower J_P. In addition the V_P values were generally over 0.5 V, which indicates a high R_S affecting the devices.

HRXRD indicates the change in Al content between samples as well as the presence of the misscut in LSG-TD1 as seen in Fig. 5.18. Only LSG-TD6 appears to show any

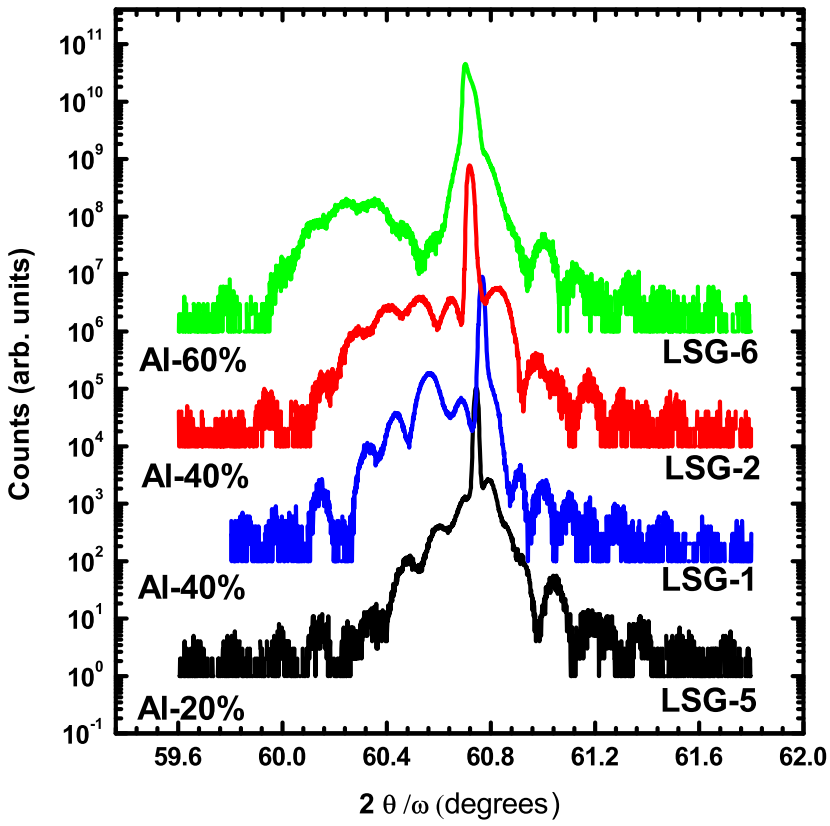


Figure 5.18: HRXRD of the LSG series samples. Peaks due to the Al content are shown to migrate to smaller angles commensurate with the larger lattice constant of AlSb compared to GaSb and InAs. LSG-TD6 appears to show some additional relaxation compared to the other samples, as evidenced by the broadness around the substrate peak.

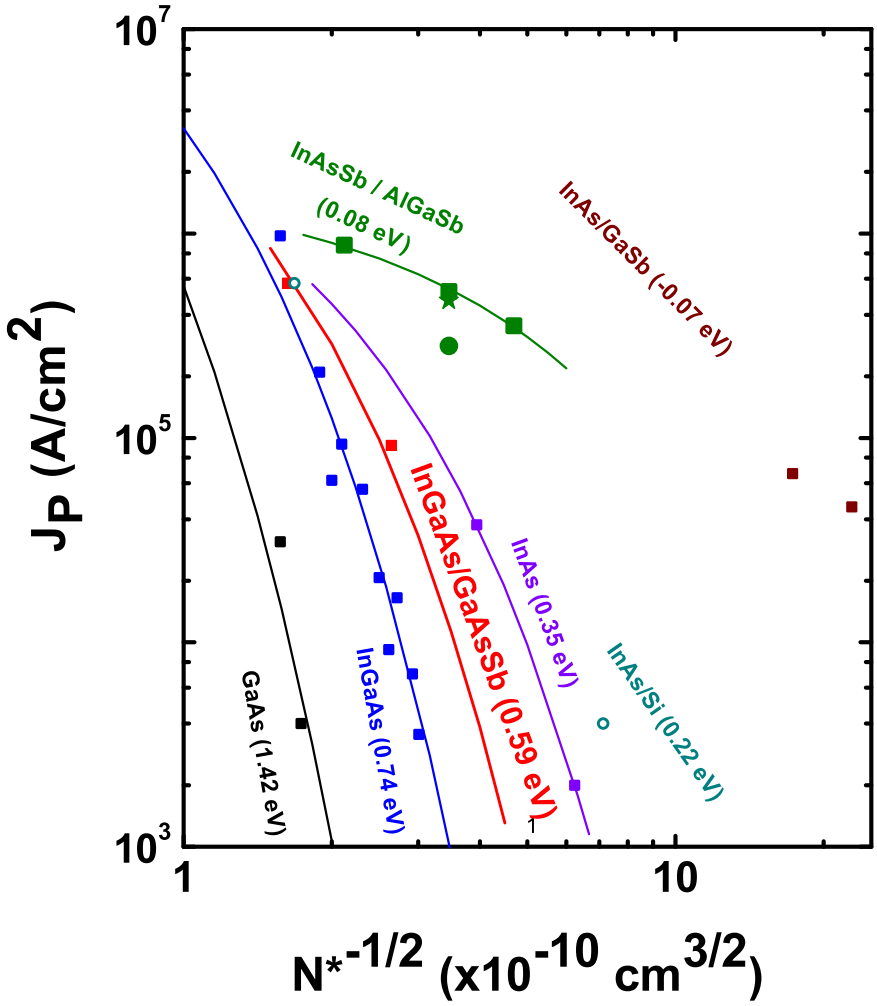


Figure 5.19: Figure of merit plot of the full LSG series. LSG series data exhibits a higher J_P than InAs for a given doping density which is further confirmation of the hypothesis that J_P can be increased through bandgap engineering. Notably, Al content also affected J_P indicating additional band gap engineering potential for this system.

signs of relaxation as seen by the broader shoulder for $InAs_{0.91}Sb_{0.09}$ near the substrate peak.

5.4 Large Stagger Gap Conclusions

This chapter has demonstrated doping density and band gap variations to those demonstrated by the SSG systems in prior sections. A larger stagger gap of ≈0.08 eV was introduced to further illustrate the relationship between J_P and N^*. Further-

more, the doping density of the structure was then varied from 1×10^{18} cm^{-3} to 2.2×10^{19} cm^{-3} to build a trend line that could be utilized to extrapolate device performance. The highest doped sample, LSG-TD1, was found to have a maximum PVCR of 3.05 and J_P of 874 kA/cm^2. It should be noted that this sample was grown on an miscut wafer and that the $Al_{0.40}Ga_{0.60}Sb$ region was 10× as thick as the remaining devices in the set. It is believed that this substrate and film combination lead to better overall device performance through reduced excess current and R_S. LSG-TD2 was found to have J_P of 552 kA/cm^2 and maximum PVCR of 1.15, the narrow $Al_{0.40}Ga_{0.60}Sb$ region likely contributed to the reduced PVCR. LSG-TD3 was found to have J_P of 356 kA/cm^2 and maximum PVCR of 1.19, likely this sample suffered from the same R_S issues as LSG-TD2. LSG-TD4 did not show tunneling characteristics, and illustrates the fine line between having a tunneling device and low breakdown voltage diode. LSG-TD4 shows how a lighter doped sample may be prove useful for future TFET applications as carrier concentration needs a relatively modest change to begin exhibiting tunneling behavior. As such the FOM plot Fig. 5.19 is expected to show a sharper drop past LSG-TD3.

Variations to the $Al_{0.40}Ga_{0.60}Sb$ layer were then presented. Al content was changed to 20% and 60% from 40% in the prior series. Fig. 5.18 shows that all the samples exhibit reasonably good crystallinity, with some slight relaxation likely for the 60% sample. It was found that there is a relation between the Al content and J_P, but the 40% sample exhibited the highest J_P. LSG-TD5 and LSG-TD6 were shown to exhibit J_P values of 471 kA/cm^2 and 285 kA/cm^2, respectively. This difference is very likely due to active doping levels, due to the growths being non-calibrated. Doping content is likely at the desired levels, but not as active as those in the 40% sample. Maximum PVCR was found to be 1.09 and 1.01 for LSG-TD5 and LSG-TD6, indicating excess current or R_S influence. Likely, the samples were mostly plagued by R_S due to the narrow AlGaSb region.

Samples from this chapter further illustrate the relationship between effective bandgap and J_P. From Fig. 5.19 it is apparent that LSG samples exhibit greater J_P at equivalent doping density when compared many of the other material systems known to have Esaki diodes. These results lead into Chapter 6 where the effective bandgap becomes negative due to broken nature of the band alignment. Results from the 20% and 60% samples were not quite in line with expectations, but that may be due to a doping activation and optimization issues resulting in lower effective doping for those samples than for the comparable 40% sample.

Results from the 40% Al content work has been cited by Desplanque et al. [147] to show additional large stagger diodes. Those samples have shown J_P in excess of 1 MA/cm^2, but no doping density was listed, nor are the contact areas for the mesas straight forward to consider. Future papers by the group may prove more informative and may push J_P further.

Chapter 6

Broken Gap Type III Heterojunctions

6.1 Introduction

Chapters 4 and 5 investigated the effects of increasing band gap stagger on the J_P for a given Esaki diode. Broken gap heterostructures are expected to provide the greatest J_P due to extended overlap of the valence and conduction bands as exaggerated in Fig. 6.1. This chapter studies how a broken gap/type III heterojunction affects J_P over an effective doping range greater than prior reports [57, 132, 150].

Prior to this work, few reports had investigated the tunnel properties of a single barrier tunnel junction. Collins et al. [57], Ganjipour et al. [132], and Luo et al. [150] investigated this junction. However Luo and Collins had only utilized low degenerate doping levels, with devices under 100 kA/cm^2. Whereas Ganjipour studied $InAs_{0.91}Sb_{0.09}$/GaSb nanowires, and N^* calculation is not straight forward in such cases nor are the devices quite the same as InAs/GaSb. This work greatly expands the knowledge for Broken Gap (BG) Esaki diodes.

This chapter investigates several factors affecting J_P in the InAs/GaSb Esaki diode system. First,the effect of N^* on J_P is explored from 9.1×10^{17} cm^{-3} to 6.7×10^{18} cm^{-3}, a range significantly higher than prior reports. Next δ-doping is investigated to determine if J_P can be pushed higher when a system is temperature limited. Following that work, a second series of BG devices was grown at an alternative grower to ensure

repeatability and to push doping density up to 2.3×10^{19} cm^{-3}. Lastly, the impact of i-layer design on J_P are tested through thickness and material changes.

BG Esaki diodes were found to exhibit higher J_P than previously tested devices, with the second series exceeding 3 MA/cm^2. Additionally, i-layer material and thickness were found to affect PVCR and J_P for measured systems, with the unsurprising result of increased PVCR and lower J_P as i-layer thickness is increased.

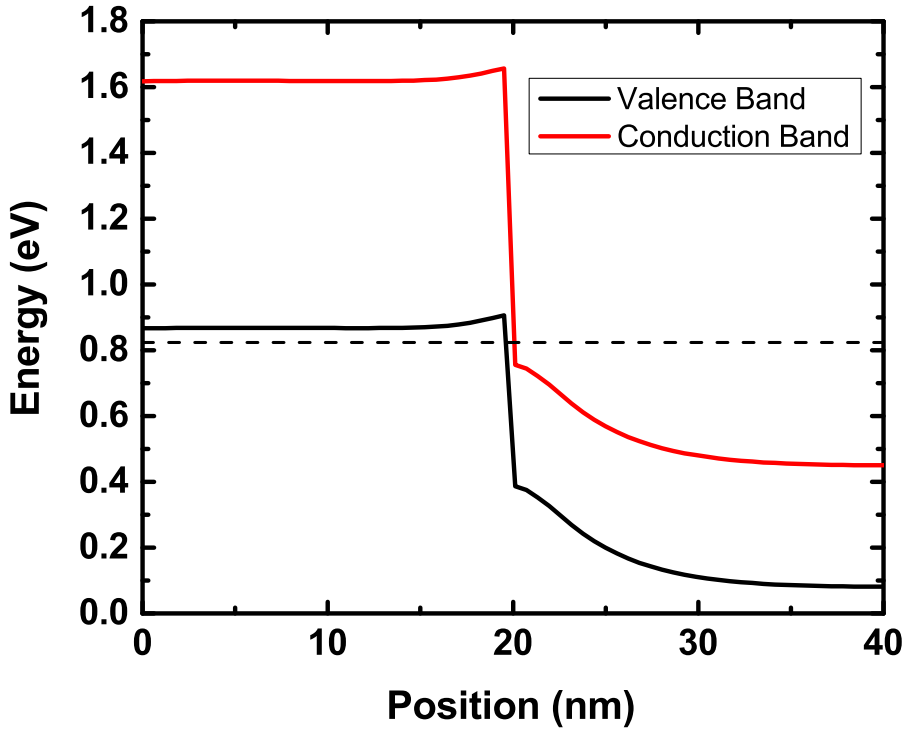


Figure 6.1: Band diagram courtesy of Mathieu Luisier. Type III/broken gap heterojunctions are thought to eliminate the barrier to tunneling. From above it can be seen that InAs and GaSb show a broken gap behavior, which will allow for greater tunneling currents.

6.2 Broken Gap Diodes: Series 1

6.2.1 BG Series 1 Design

The samples in this study were grown by molecular beam epitaxy atop $p+$ GaSb substrates. Fig. 6.2 illustrates the schematic diagram of the device layers, which consists of 300 nm of $p+$ GaSb (Be-doped, from 1×10^{18} cm^{-3} to 1×10^{19} cm^{-3}), a 3 nm thick

nominally intrinsic InAs layer, and a 50 nm $n+$ InAs (Si-doped, 3×10^{19} cm^{-3}). All growths were carried out in a DCA solid source molecular beam epitaxy (MBE) system using elemental Ga and In metals in standard effusion cells and Sb and As valved cracker sources set to produce dimeric group V species. Si and Be were used as n-and p-type dopants respectively which were calibrated using secondary ion mass spectroscopy (SIMS) technique. Epi ready p-type GaSb <100> substrates were mounted in In-free holders and introduced into the growth chamber after an initial outgas in the load lock at 150°C. Growth rates were determined using the RHEED oscillation technique on native substrates. Growth rates of 0.5 ML/s and 0.3 ML/s with V/III ratios of 5 and 7 were used for GaSb and InAs respectively. Substrate thermocouple temperatures were calibrated using a combination of pyrometer and KSA bandit system. Oxide desorption was monitored exclusively with RHEED. Oxide desorption from GaSb substrates was observed to occur at substrate temperatures of 530°C. GaSb layer growth occurred at 500°C while the InAs layers were grown at 480°C .

Device fabrication closely follows a process reported by Pawlik et al. [29] but with differences in contact metal and contact definition. 200 nm of Mo is blanket deposited, via DC magnetron sputtering, on the sample surface. A negative ebeam resist, nLOF, is diluted in PGMEA (≈1:1 by mass) and masks the mesa contact during a SF_6-based dry etch which to defines the Mo patterns ranging from 100 nm to 20 μm squares. Mesas are etched in a 20:1 citric acid: peroxide solution for 60 s. Both the contact area and undercut are measured over a variety of device sizes and locations to estimate the device area across the sample to increase the precision of J_P extracted values. This undercut is estimated to be approximately 100 nm. Samples are then coated with a bisbenzocyclobutane ILD which acts to passivate devices and support a large level 2 Mo contact pad.

Current-voltage characteristics (I-V) were obtained via a Keithley 4200 Semiconductor Parameter Analyzer. As in Romanczyk et al. [27], a large area Esaki diode

(>1000 × the measured junction area) is used as a virtual ground. The ground plane was designed to fully surround the devices to minimize any effects of current crowding; this is critical for measuring high current tunnel junctions as it minimizes unwanted resistive-based latching that obscures the negative differential resistance. Data was collected and processed to extract the J_P from a histogram. HRXRD of the samples was performed on a Bruker 8 system to confirm film stack. HRXRD profiles were compared against film stacks modeled in LEPTOS^{TM} software from Bruker which explained possible sources for variation from the design.

50 nm	InAs: Si	1×10^{19} cm^{-3}
3 nm	InAs	uid
300 nm	GaSb: Be	2×10^{19} cm^{-3}
Substrate	GaSb	

(a) BG-TD1

50 nm	InAs: Si	1×10^{19} cm^{-3}
3 nm	InAs	uid
300 nm	GaSb: Be	5×10^{18} cm^{-3}
Substrate	GaSb	

(b) BG-TD2

50 nm	InAs: Si	1×10^{19} cm^{-3}
3 nm	InAs	uid
300 nm	GaSb: Be	1×10^{18} cm^{-3}
Substrate	GaSb	

(c) BG-TD3

50 nm	InAs: Si	1×10^{19} cm^{-3}
3 nm	InAs	uid
300 nm	GaSb: Be	1×10^{18} cm^{-3}
Substrate	GaSb	

(d) BG-TD4

Figure 6.2: (a) Schematic for highest doped BG sample, BG-TD1. (b) Schematic for BG-TD2 with lower doping levels. (c) Schematic of the film stack for BG-TD3 which was designed to doped higher than previous InAs/GaSb reports [57, 132]. (d) A repeat growth of BG-TD3, after the former shattered prior to fabrication.

6.2.2 BG Series 1 Materials Analysis

HRXRD and SIMS measurements were taken from the BG series diodes. XRD provided an extra peak between GaSb and InAs, indicating the presence of an additional material. Using LEPTOS^{TM} modeling software, there was an indication as to the composition of the additional peak material. SIMS measurements indicated that Si

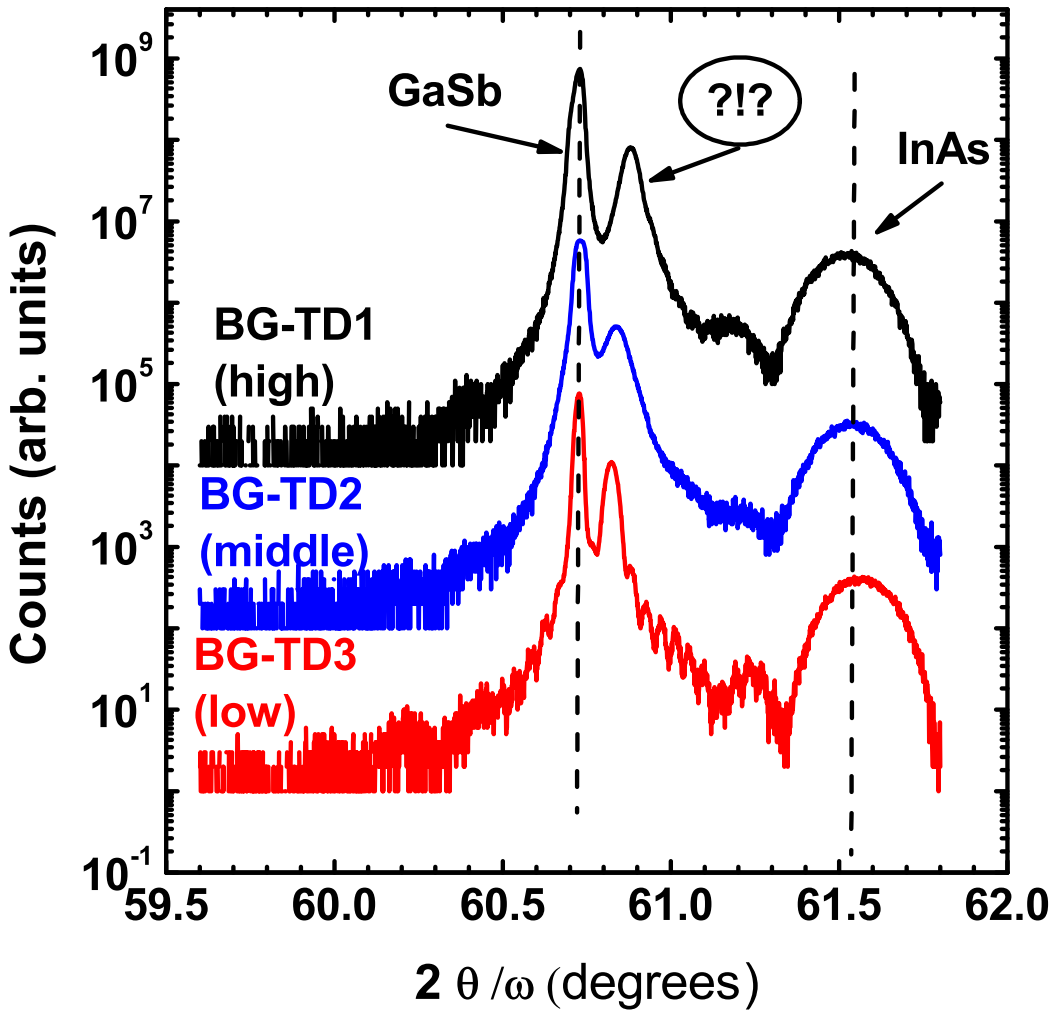


Figure 6.3: $\omega/2\theta$ curves for the InAs/GaSb tunnel diodes exhibit an additional sharp peak near the GaSb line. This peak may be indicative of a variation in film composition for the 300 nm GaSb region.

doping was, generally, higher than targeted.

Figure 6.3 exhibits secondary peaks near the GaSb substrate peak, indicating that the GaSb epitaxy layers lattice constant is smaller than designed (right shifted). Lacking a symmetric peak to the left of the GaSb peak would indicate that this feature is not a side lobe. Figure 6.4 displays the expected $\omega/2\theta$ scan for the designed film with an overlay of a film containing a small percentage of As incorporation consistent with the overpressure of As during growth. Remarkably, the inclusion of the As in the model fits quite closely with the measured data, hinting that the sample likely

includes As therefore shifting the band edge alignment at the junction. A quick linear interpolation would indicate that the bands now are near perfect alignment, increasing the band offset 80 meV to 0 eV. Each peak shifts with increased Be concentration, which behaves similarly to reports of Be in super lattice structures [18] at similar concentration levels. Thereby indicating that XRD could be used as a nondestructive means to determine dopant concentration in tunnel diode applications.

SIMS provided doping density values for BG-TD1, BG-TD2, and BG-TD3. From Fig. 6.5 it can be seen that the doping profile is reasonably abrupt for both Si and Be. Doping values for Si were found to be $\approx 3\times10^{19}$ cm^{-3} for all three samples. Be concentrations were shown to vary, roughly as designed at 2×10^{19} cm^{-3}, 5×10^{18} cm^{-3}, and 1×10^{18} cm^{-3} for BG-TD1, BG-TD2, and BG-TD3 respectively. These doping concentrations lead to extracted values of 6.67×10^{18} cm^{-3}, 3.33×10^{18} cm^{-3}, 9.09×10^{17} cm^{-3} for N^*. These doping levels are higher than previous reports [57, 132], and expected to exceed the J_P of equivalently doped LSG and SSG devices.

TEM analysis was also performed on BG-TD1. There were no detectable defects measured during analysis. HAADF scans showed an InSb-like interface between the InAs and GaSb regions which may have an effect of lowering V_P [151].

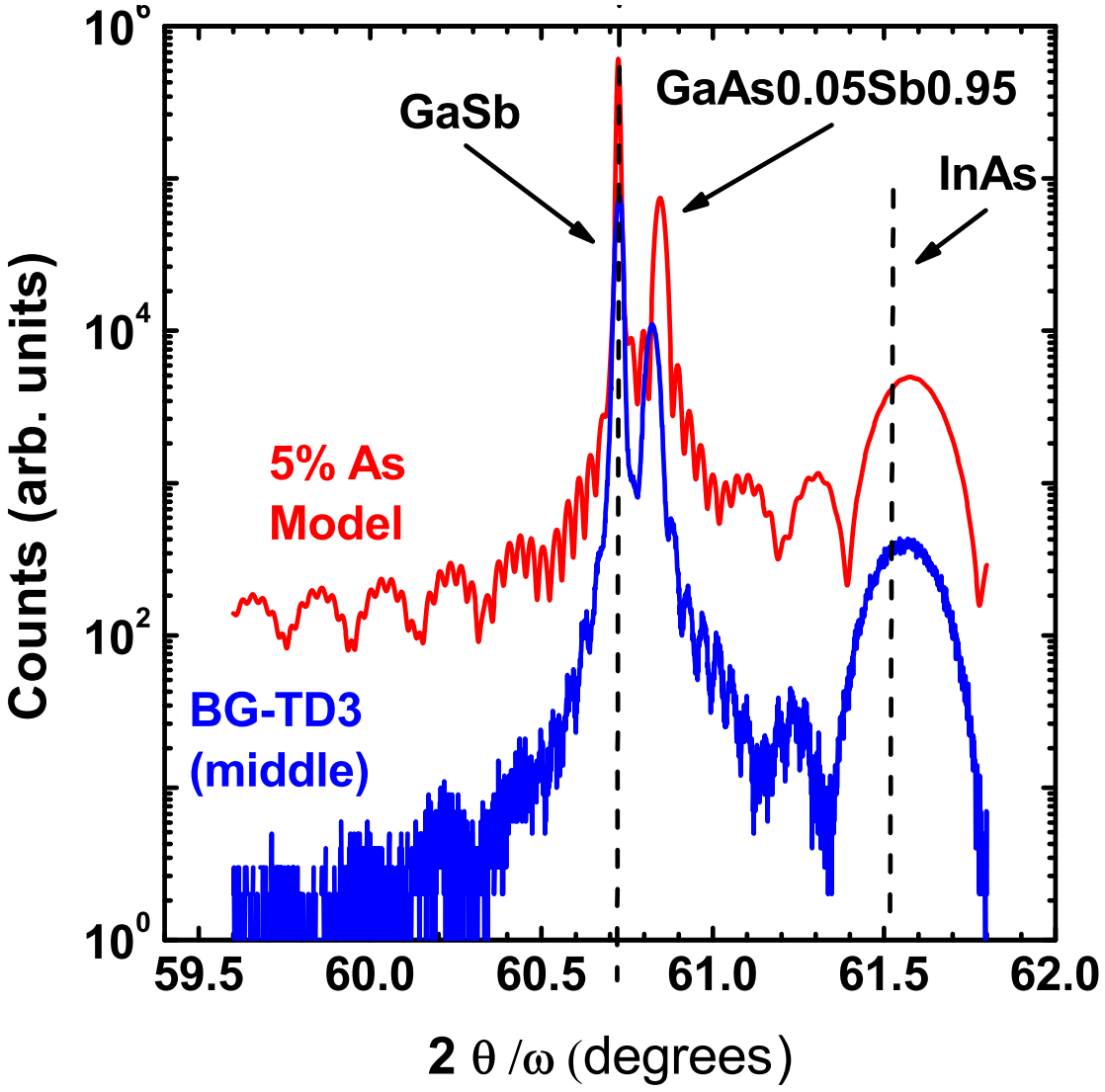


Figure 6.4: Assuming a 5% As incorporation into the GaSb film, LEPTOS was used to predict a $\omega/2\theta$ curve. Interestingly, the same peak appears in simulation as was exhibited by each sample. Implying that there was As incorporated into the film.

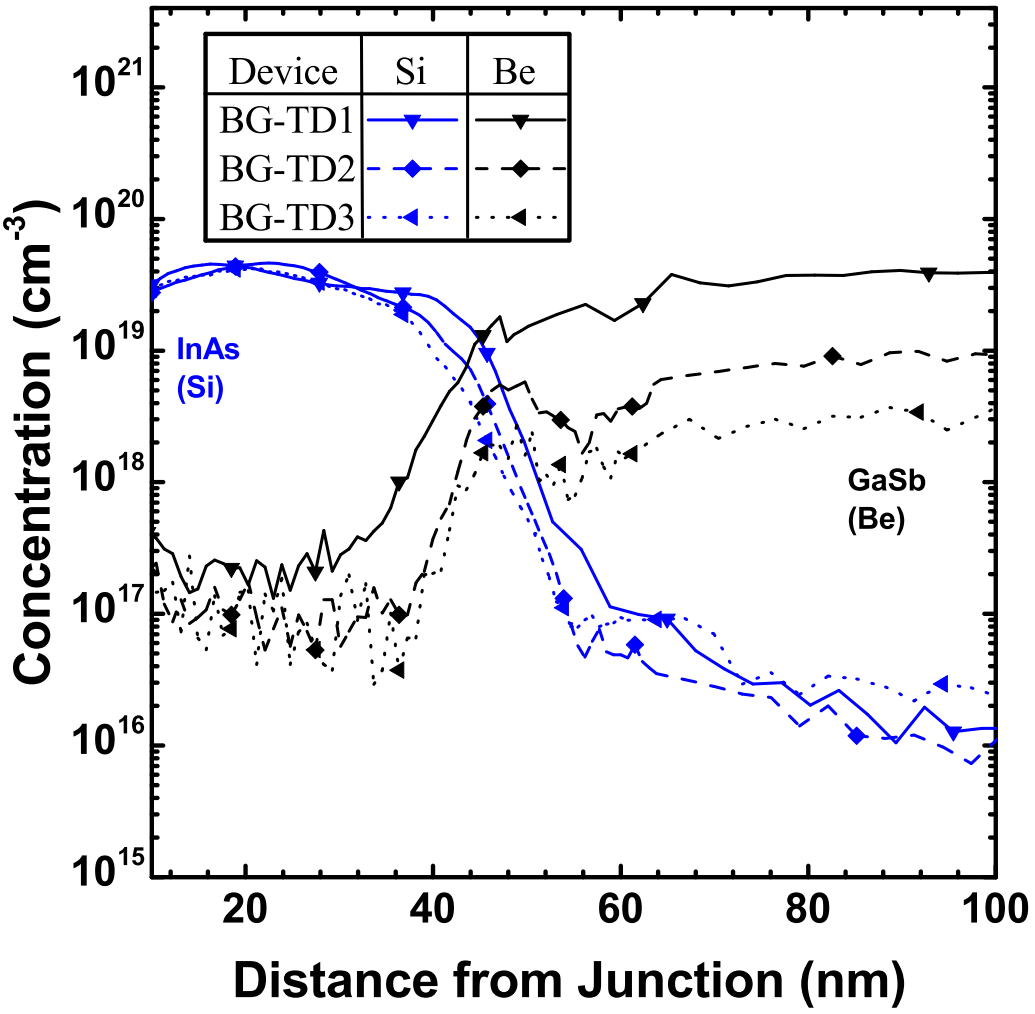


Figure 6.5: SIMS was performed on the samples to determine dopant levels present within the sample. BG-TD1, BG-TD2, and BG-TD3 were found to have Si and Be doping levels near the targeted values. Detectable levels of As were found to be within the GaSb film region.

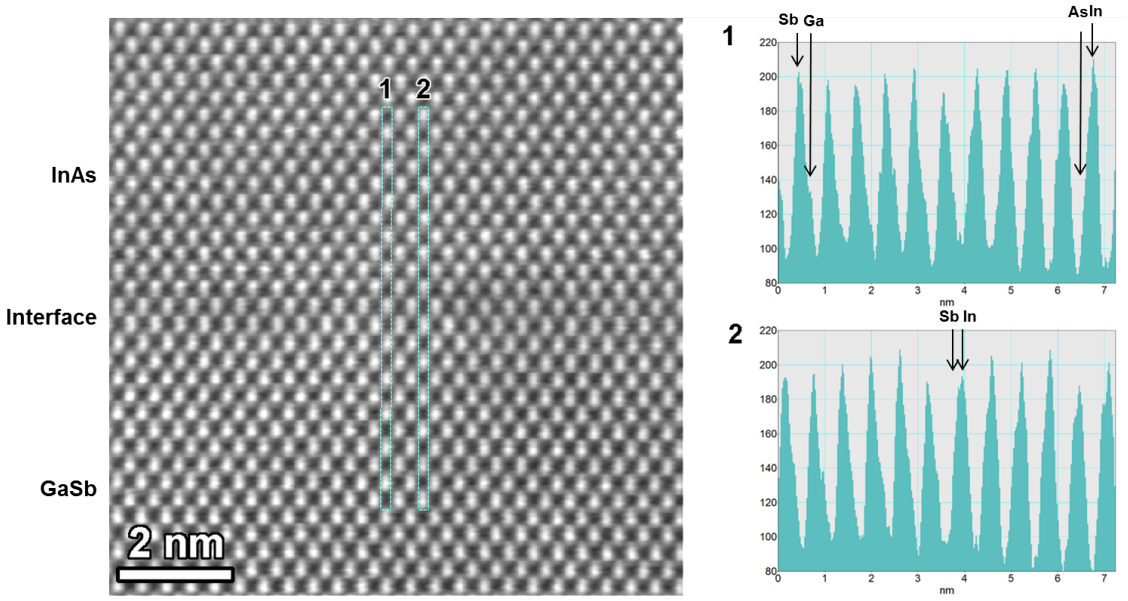


Figure 6.6: TEM analysis of the TD7A junction shows an InSb like interface and was found to be largely defect free.

6.2.3 Broken Gap Series 1 Electrical Analysis

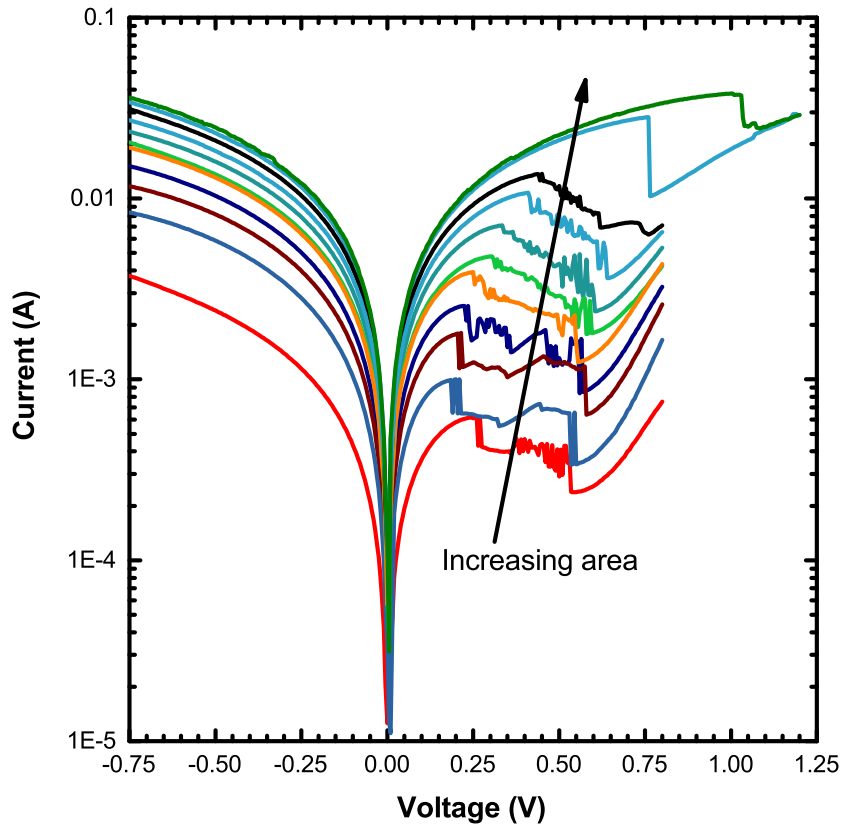


Figure 6.7: Family of I-V curves for BG-TD1 show current scaling and a very clear NDR region.

Many devices across each of the three samples were tested, generally 200 or more to provide a sufficient population for J_P extraction. Figure 6.7 shows the typical diode characteristics with scaling, with large device areas a latch characteristic is present indicating a significant contribution from series resistance. As devices scale, this resistance diminishes. The device size at which these effects become negligible is typically larger for lower current devices. The latching phenomenon created by large R_S, became less prominent as device area decreased below 1 μm^2. Characteristic

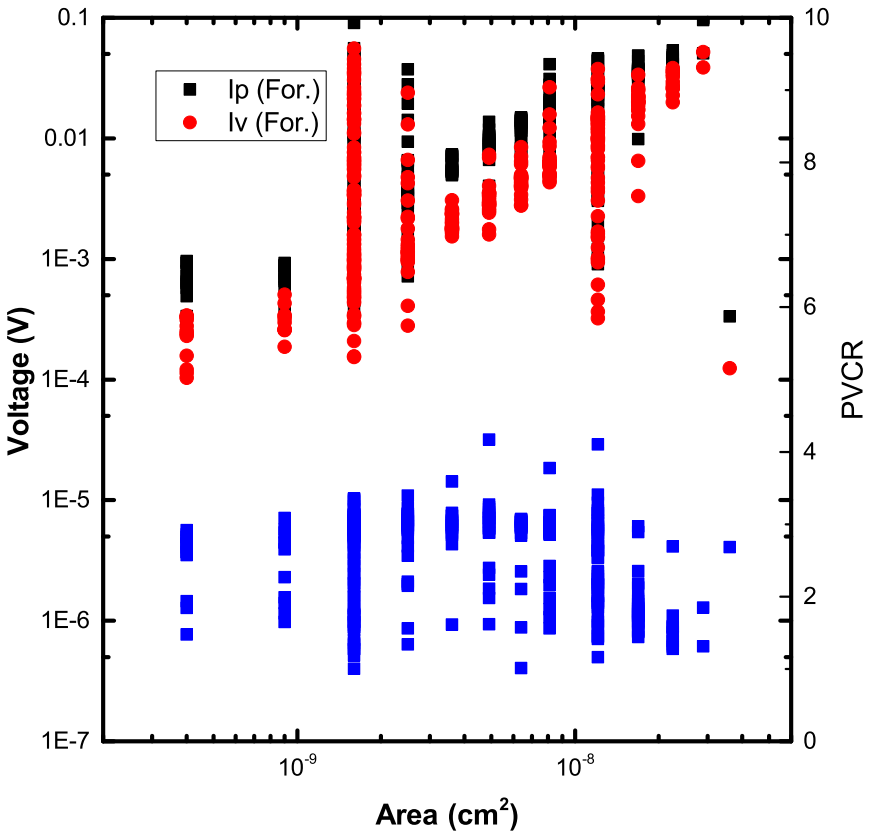


Figure 6.8: I_V, I_P, and PVCR *vs.* Area for BG-TD1 shows current scaling with area and the relatively stable range for PVCR across device sizes.

curves for the three BG samples in this study are exhibited in Fig. 6.9. As expected, J_P increased as the Be doping shifted from 10^{18} cm^{-3} to 10^{19} cm^{-3}. BG-1 exhibits a J_P of roughly 220 kA/cm^2 which is 5× greater than the numbers reported by Collins et al. [50] and Ganjipour et al. [132]. Increasing Be doping in GaSb to 5×10^{18} cm^{-3} results in a 2.5× improvement in J_P. Sample BG-3 exhibits the largest J_P, 2.2 MA/cm^2, of any reported tunnel diode [28]. It is interesting to note the increase in PVCR with increased doping, which is atypical of Esaki diodes with such large J_P values. Usually the PVCR value peaks at much lower level of doping, indicating that this structure could still see improvements to J_P with even greater doping levels. Over 200 devices

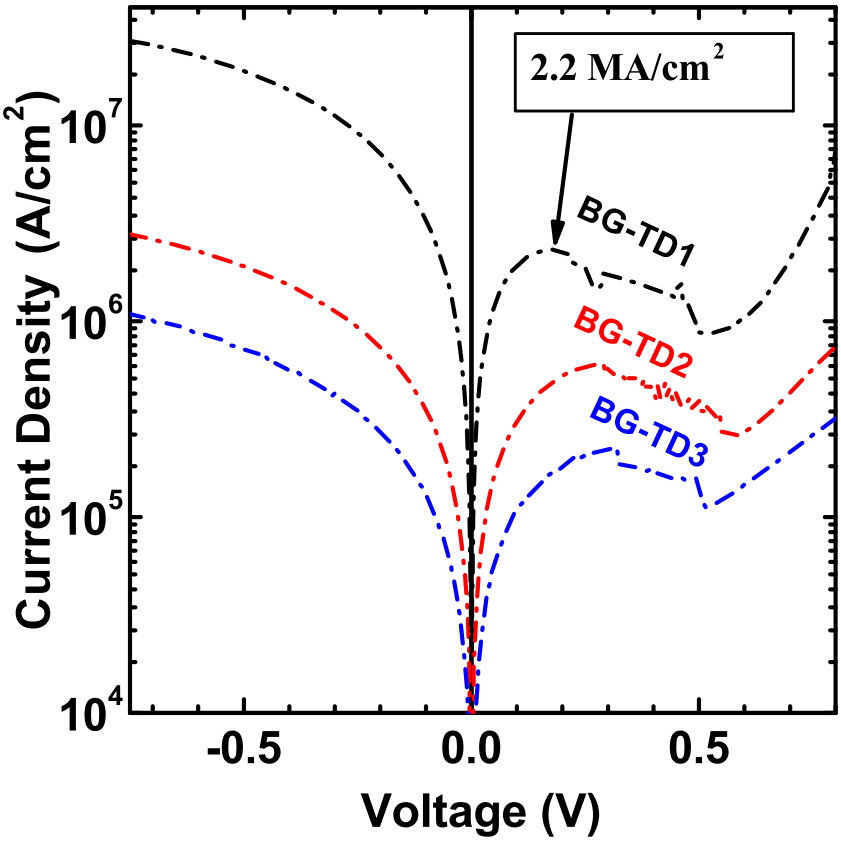


Figure 6.9: Representative *I-V* curves for similarly sized devices from the BG Series 1 diodes.

were tested per sample, allowing the authors to extract the J_P from the histograms shown in Fig. 6.10 as well as the median PVCR from Fig. 6.11. Table 6.1 summarizes the values extracted from the characteristic curves of the devices shown in Figure 6.9.

Relative to the $In_xGa_{1-x}As$ homojunction system, the InAs/GaSb BG system exhibits decreased sensitivity to doping for tunnel current, while maintaining significantly higher currents densities. A TFET might be able to attain an output current of 100 MA/cm^2 if performance translates from the $In_{0.53}Ga_{0.47}As$ TFET systems to date [8]. However, the slow decrease in current for the change in doping level may make the BG system a less ideal candidate for future TFET systems.

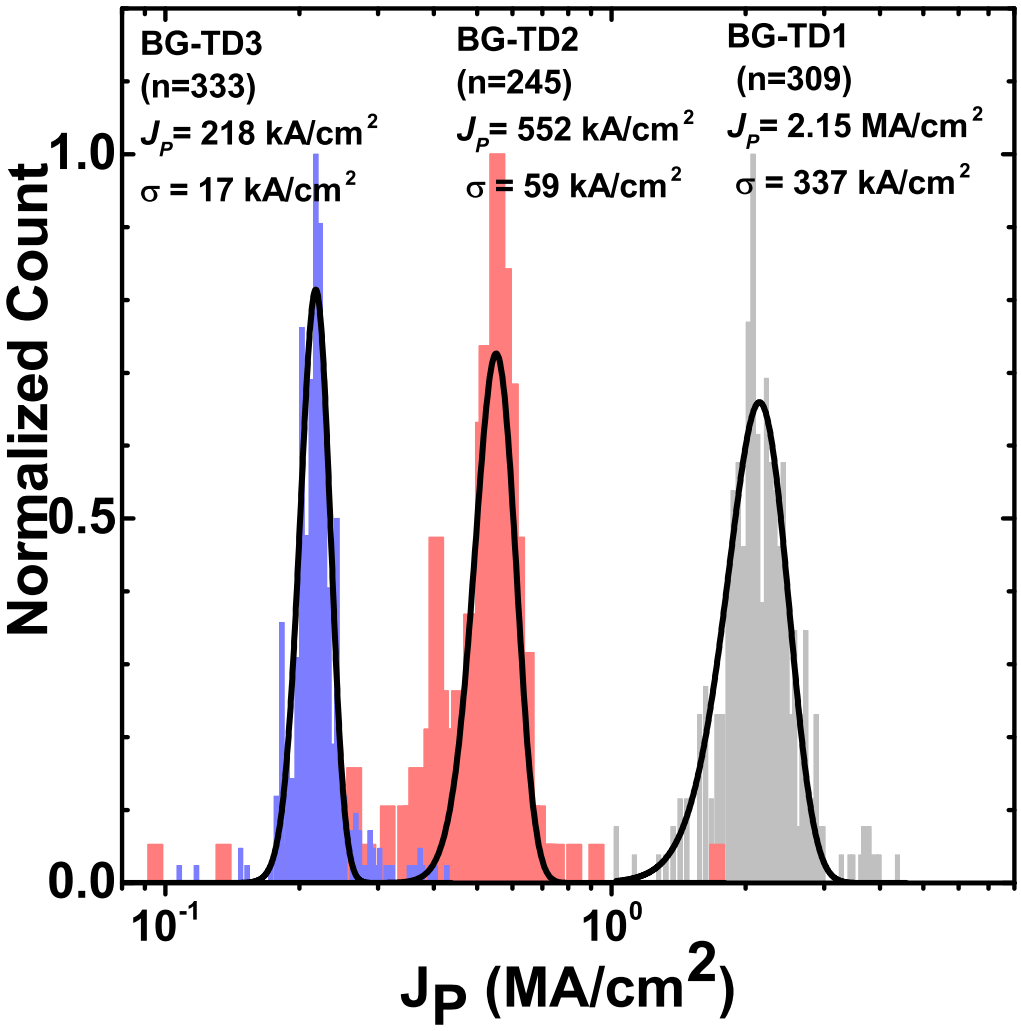


Figure 6.10: J_P histograms for BG series 1 diodes from which 2.2 MA/cm^2, 552 kA/cm^2, and 212 kA/cm^2 J_P values were extracted for BG-TD1, BG-TD2, and BG-TD3.

6.2.4 BG Series 1 Summary

The author has reported BG tunnel diodes with a record peak current density of 2.2 MA/cm^2. These diodes show the potential for the BG heterojunction systems to meet the requirements placed on TFETs to replace CMOS. At this point, it is unclear if As incorporation into the GaSb layer was detrimental to the final output current. Additional growths would be required to decouple this information on the FOM plot. One sample would utilize the same growth conditions but at doping levels similar to the Collins papers [50, 57], while the other would have to repeat the highest doped

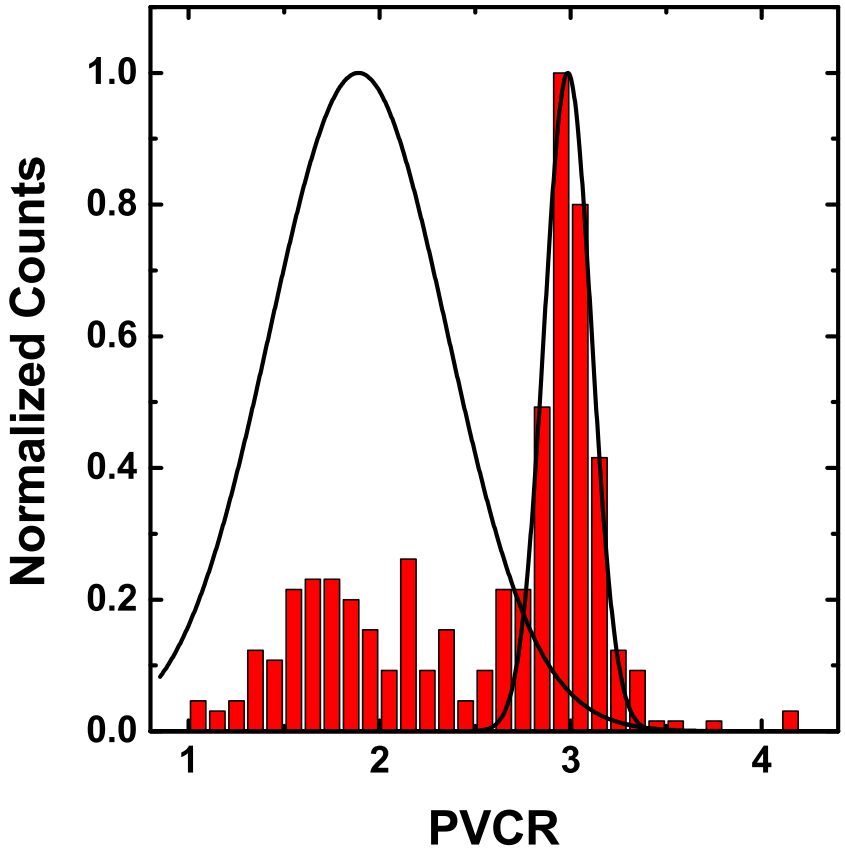


Figure 6.11: From the histogram of PVCR values, there appears to be a bimodal distribution of PVCR as shown by the two peak fits. It possible that there are processing factors in play that would cause such a characteristic to appear.

sample while excluding As from the GaSb lattice. It is the opinion of the author that the InAs/GaSb BG system can likely exhibit J_P near 10 MA/cm^2, since the both Si and Be dopants can exceed 10^{20} cm^{-3} within their respective layers [47, 144].

Table 6.1: Broken Gap Series 1 Summary

Device	p $\times 10^{19}$ (cm^{-3})	n $\times 10^{19}$ (cm^{-3})	N^* $\times 10^{19}$ (cm^{-3})	$N^{*-0.5}$ $\times 10^{-10}$ (cm^{-3})	J_P (kA/cm^2)		J_V (kA/cm^2)		PVCR		
					mean	σ	mean	σ	mean	max	σ
BG-TD1‡	2 Be	1 Si	0.67	3.87	2200	337	2200	139	1.48	3.95	0.19
BG-TD2‡	0.5 Be	1 Si	0.33	5.48	552	54	498	62	2.45	3.1	0.11
BG-TD3‡	0.3 Be	3 Si	0.27	6.06	212	12.3	136	28.8	1.71	1.83	0.06
BG-TD4‡	0.1 Be	1 Si	0.09	10.5	172	16.6	109	30.5	1.63	2.12	0.27

‡ $< 100 >$ GaSb substrates

6.3 *i*-layer Series 1

6.3.1 BG *i*-layer Series 1 Design

Following the results from the previous section, the importance of the i-layer was investigated. Collins et al. [57] had shown a twofold increase in J_P when doubling the width of the i-layer. This section investigates the changes in the InAs i-layer thickness. Fig. 6.12 displays the designed changes to InAs thickness in BG-TD5 and BG-TD6. By comparing 0 nm InAs to 6 nm InAs, a relation for J_P and PVCR is likely to emerge. Removing the i-layer may increase the J_P by increasing $\mathcal{E}$ while reducing PVCR through increased leakage paths.

50 nm	InAs: Si	1×10^{19} cm^{-3}
0 nm	InAs	uid
300 nm	GaSb: Be	1×10^{18} cm^{-3}
Substrate	GaSb	

(a) BG-TD5

50 nm	InAs: Si	1×10^{19} cm^{-3}
6 nm	InAs	uid
300 nm	GaSb: Be	1×10^{18} cm^{-3}
Substrate	GaSb	

(b) BG-TD6

Figure 6.12: (a) Schematic of the film stack for BG-TD1 which was designed to doped higher than previous InAs/GaSb reports [57, 132]. (b) Schematic for BG-TD2 with higher doping levels. (c) Schematic for highest doped BG sample, BG-TD3. (d) A repeat growth of BG-TD1, after the former shattered prior to fabrication.

6.3.2 BG *i*-layer Series 1 Materials Analysis

HRXRD $2\theta/\omega$ measurements were taken from samples BG-TD5 and BG-TD6 and compared to BG-TD3. Slight differences in the peak location for the grown GaSb film appear, and may create marginal differences between samples. From Fig. 6.13 BG-TD5 closely resembles BG-TD3, while BG-TD6 would appear to have less As present in the GaSb layer. Otherwise, the samples appear to exhibit excellent crystallinity which will minimize the impact of defects on excess current.

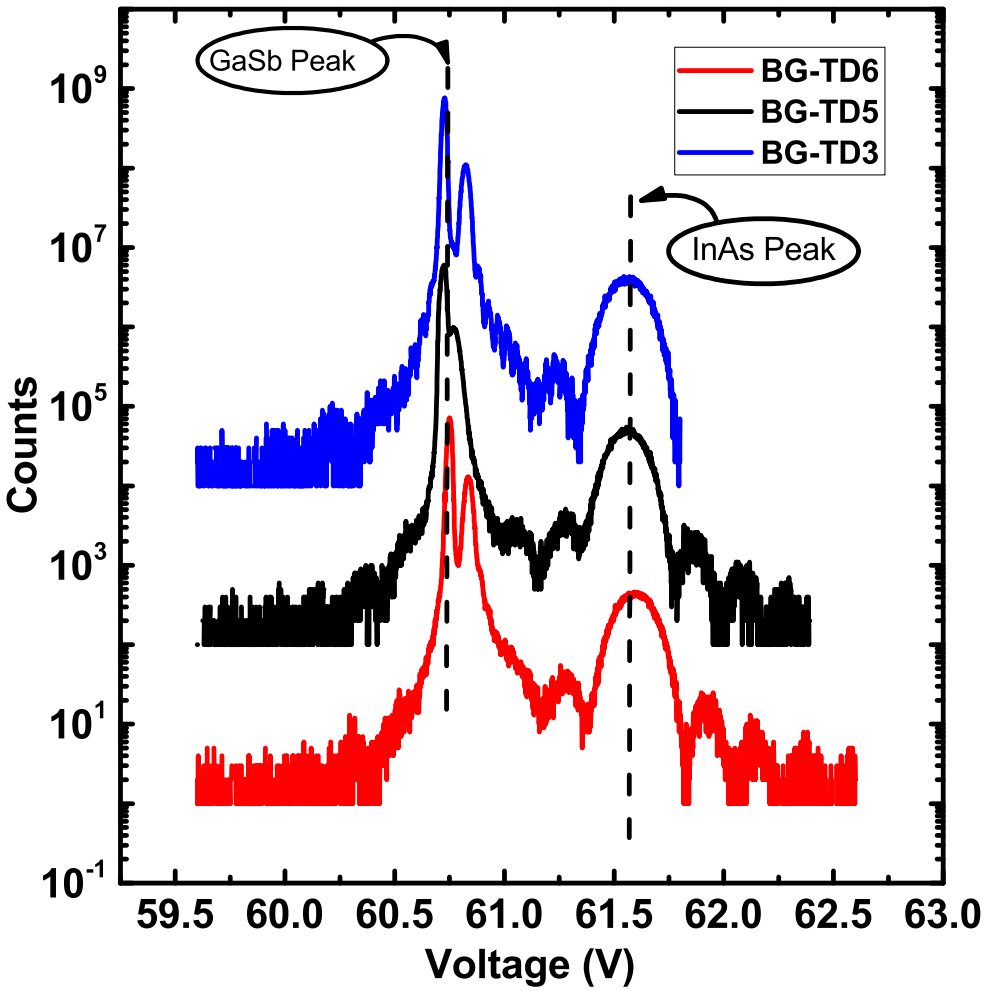


Figure 6.13: HRXRD of samples BG-TD5 and BG-TD6 compared against BG-TD3 show slight differences in the 300 nm film which are likely due to As remaining in the chamber following flux measurements.

Comparing SIMS results between BG-TD3, BG-TD5, and BG-TD6 shows that the origin for higher J_P in BG-TD3 is the higher than intended doping. SIMS was not performed on BG-TD4 because the material that survived shipping was dedicated to fabrication. The i-layer appears to be on target for 0 nm, 3 nm, and 6 nm per the designs shown in Fig. 6.12. From Fig. 6.14, N^* values of 2.7×10^{18} cm^{-3} and 7.5×10^{18} cm^{-3} were extracted for BG-TD3 and BG-TD5 and BG-TD6.

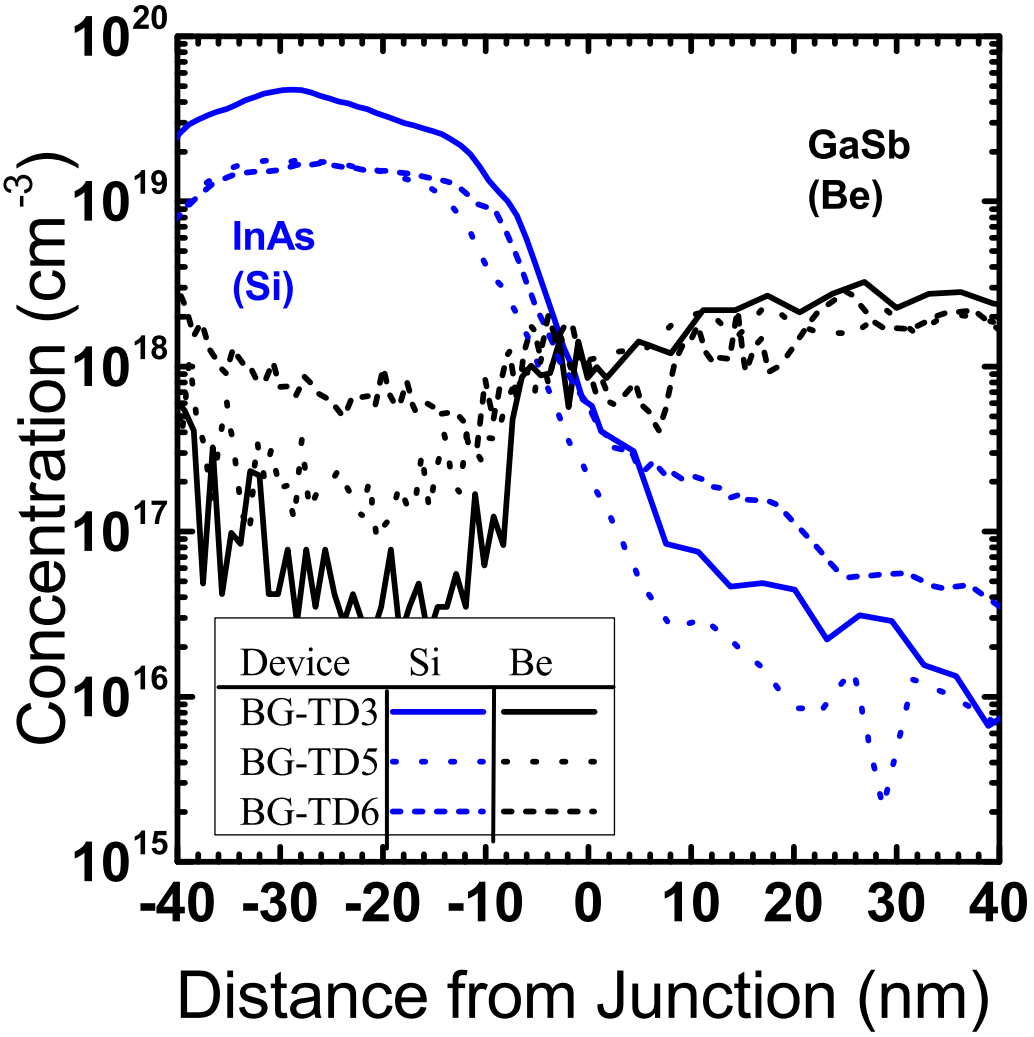


Figure 6.14: SIMS was performed on the samples to determine dopant levels and compare i-layer thickness. N^* values of 2.7×10^{18} cm^{-3} was extracted for BG-TD3 and 7.5×10^{18} cm^{-3} was extracted for BG-TD5 and BG-TD6.

6.3.3 BG i-layer Series 1 Electrical Analysis

Examining samples from BG-TD5 and BG-TD6 electrical performance is relatively similar, but with some expected differences in PVCR and J_P. From Fig. 6.15, it can be seen that similarly sized devices exhibit low R_S but BG-TD5 exhibits a slightly lower J_P and slightly higher PVCR than BG-TD6.

Current scaling in Fig. 6.16 further illustrates the differences between devices created by changing i-layer thickness. Generally, BG-TD5 shows lower I_P and I_V

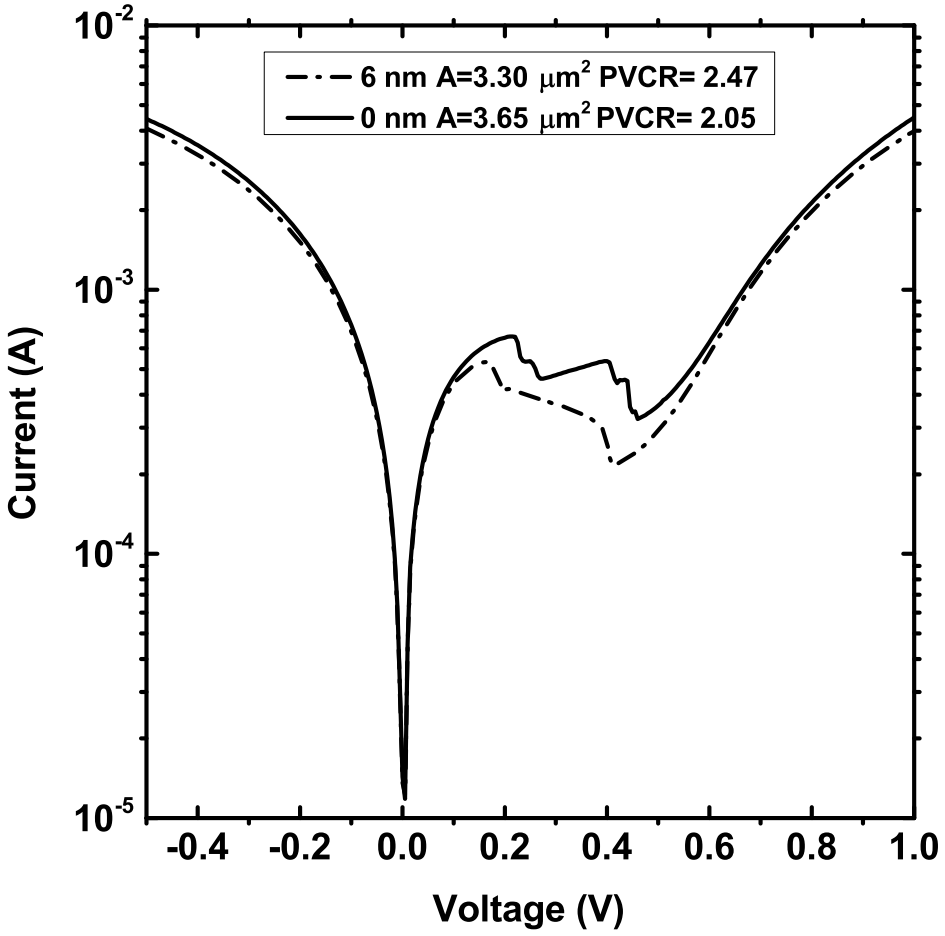


Figure 6.15: Normalized J_P histograms for InAs i-layer study showing the effect of InAs thickness on J_P. As expected, decreasing the i-layer thickness causes an increase in J_P. Confounding the results are the values from BG-TD3 and BG-TD4, which both have a 3 nm i-layer but is likely related to growth system drift.

while having higher PVCR than BG-TD6. Higher PVCR for BG-TD5 is likely due to a wider i-layer suppressing leakage paths. A wider i-layer also lowers the field between the n and p regions, thereby reducing J_P at value proportional to the i-layer width [46]. As summarized in Table 6.2, increasing i-layer thickness to 6 nm shows a 20% decrease to J_P while providing $\approx$ 10% improvement to PVCR relative to no i-layer. This result varies from those of Collins et al. [50], but may be due to an interaction that exists when the i-layer encompasses the heterojunction. However, depending on the design targets for tunneling devices, varying i-layer thickness for InAs could be used to balance between PVCR and J_P.

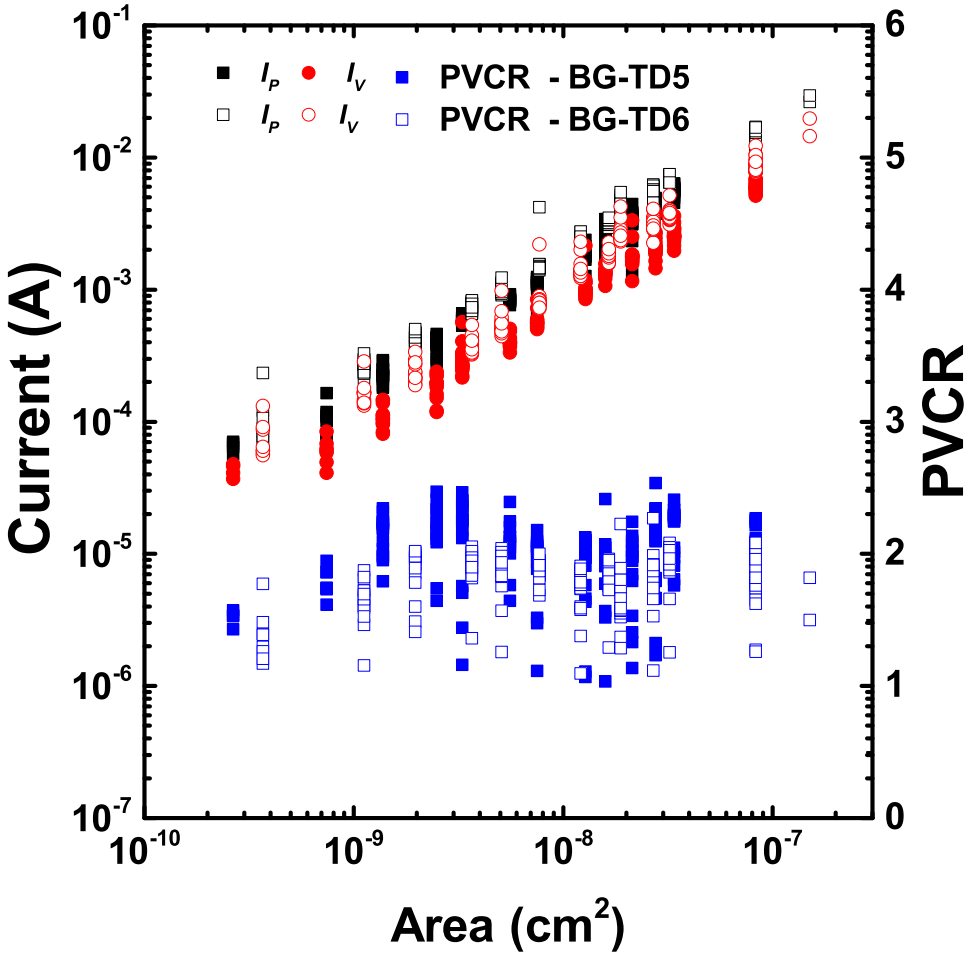


Figure 6.16: I_V and I_P *vs.* area for BG-TD5 and BG-TD6 show an increased J_P when reducing the i-layer thickness between the n and p regions, due to an increased electric field allowing increased carrier tunneling. Similarly, PVCR increases when the i-layer thickness is increased likely due to the increased screening that a wider tunnel region presents for excess currents.

Comparing V_P between BG-TD5 and BG-TD6 shows a slight increase for the 0 nm i-layer sample. V_P would be expected to be lower for the 0 nm i-layer sample, since the fields are higher and should peak at lower voltages. When compared to 3 nm i-layer, samples BG-TD3 and BG-TD4, BG-TD5 and BG-TD6 exhibit lower values but all converge within 0.1 V. Differences may be due to time between sample growths or any number of other process variations. However, the V_P data shows that R_S for these BG samples is exceedingly low, but also indicates the need for better process

control if fine control of J_P and PVCR is required for device design.

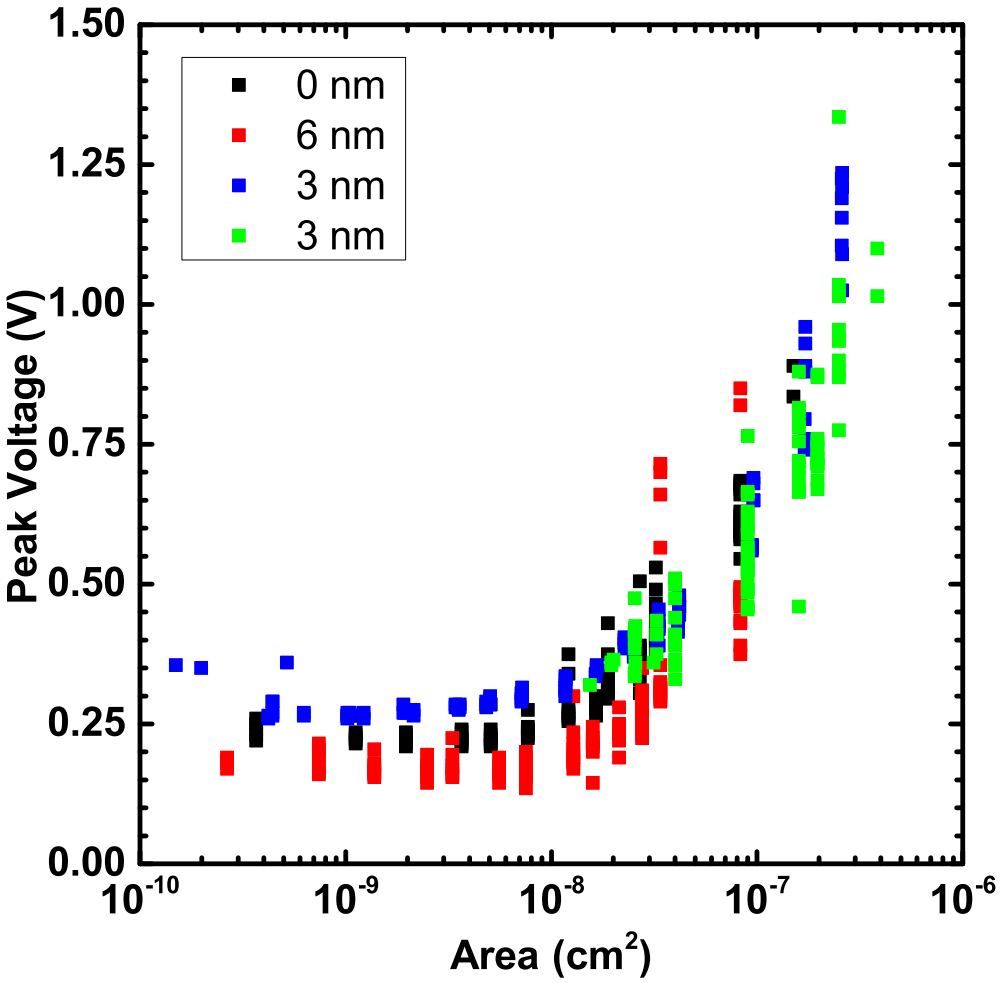


Figure 6.17: Typical minimum V_P values for the InAs i-layer devices appear to fall between 0.3 V and 0.2 V, indicating minimal influence from R_S.

Observing Fig. 6.18, it appears that variations between growths can contribute as much to differences in J_P as do changes to the i-layer. While BG-TD4 firmly falls between the 0 nm and 6 nm devices, J_P for BG-TD3 is greater than all the other devices. Unfortunately, the sample set for BG-TD4 was limited to a few small pieces due to a fall prior to shipping and could not be investigated further. Generally, a claim could be made that J_P tracks with i-layer thickness with $\approx$7 kA/cm^2 reduction in J_P for each nm of InAs added to the i-layer. However, variations in doping from target values can quickly exceed the benefits of i-layer thickness variation.

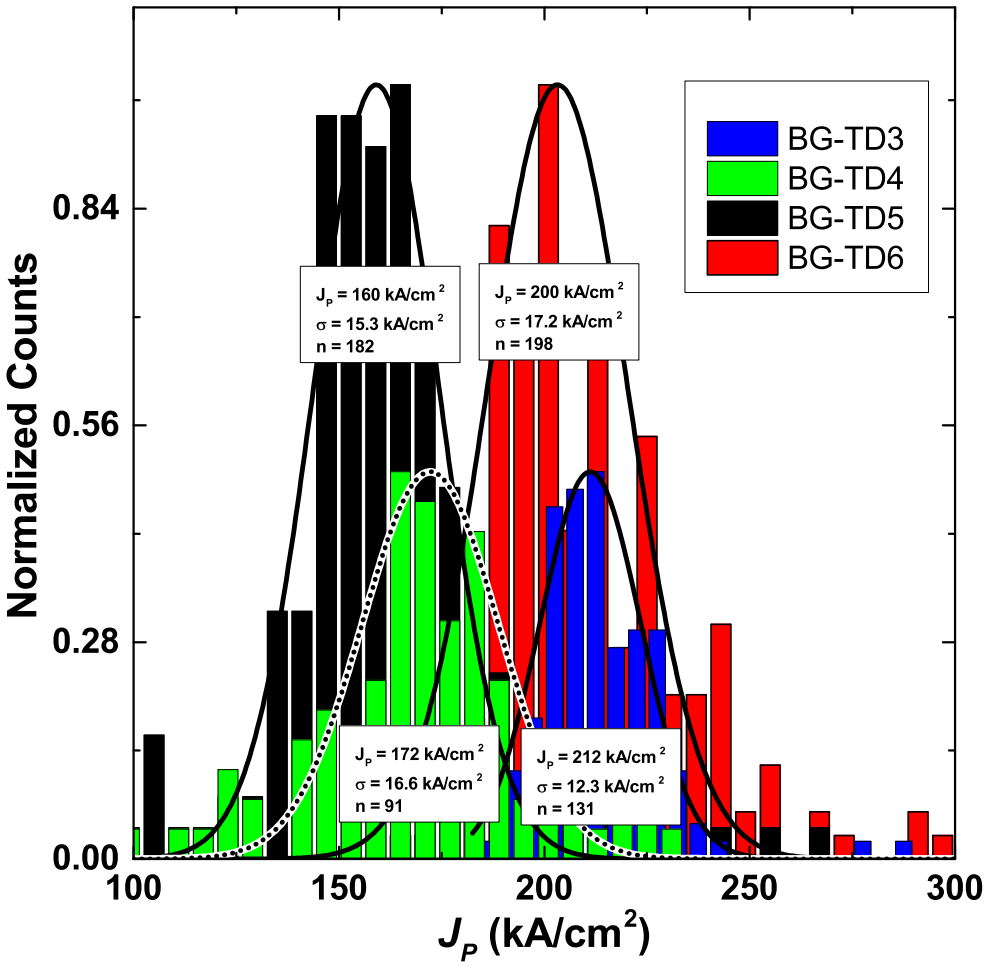
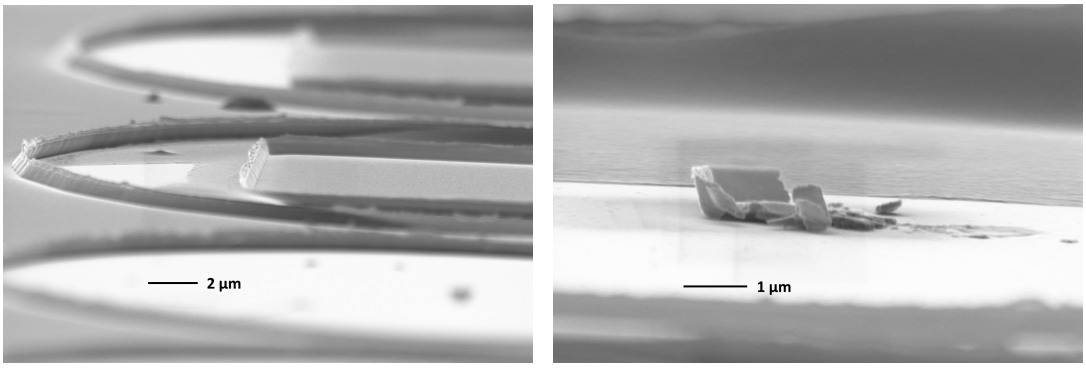


Figure 6.18: Normalized J_P histograms for InAs i-layer study showing the effect of InAs thickness on J_P. As expected, decreasing the i-layer thickness causes an increase in J_P. Confounding the results are the values from BG-TD3 and BG-TD5, which both have a 3 nm i-layer but is likely related to growth system drift.

Similar to the J_P results, PVCR for the 3 nm samples also deviated from the trend seen between the 0 nm and 6 nm i-layer samples. BG-TD3 and BG-TD4 both appear to have lower PVCR than BG-TD6 in Fig. 6.20 . Sources for lower PVCR for the 3 nm samples are not clear, but are likely process related as BG-TD3 and BG-TD4 were part of the initial sample set in which process parameters were still being defined and tuned. BG-TD4 low PVCR may be related to early iterations of the fabrication process which could leave small stringers of metal near the side wall after metal 1 was lifted off instead of the etch back process which was developed later

as seen in Fig. 6.19. Regardless, the differences in PVCR illustrate the challenges of targeting specific values as i-layer and doping both affect J_P and PVCR outcomes.



(a) Lift-off on BG-TD4 **(b)** Stringers on BG-TD4

Figure 6.19: Intitial lift off processes for L1 lead to stringers which would cause shorting between the contact and the mesa. This creates additional shunt paths which reduce PVCR.

6.3.4 BG *i*-layer Series 1 Summary

Modifying i-layer thickness to affect J_P and PVCR was found to be effective but with a few caveats. Table 6.2 summarizes the i-layer results and shows that for devices grown consecutively, i.e. under the same conditions, changing thickness between the n and p regions can create differences in the J_P and PVCR. However drift in system calibration can negate the effects as seen by the BG-TD3 falling outside of the trend that would have been created when looking at the results of the remaining samples. Additionally, a change in doping will likely exert a greater influence on J_P than slight changes to i-layer thickness.

Table 6.2: BG i-layer Series 1 Summary

Device	p $\times 10^{19}$ (cm^{-3})	n $\times 10^{19}$ (cm^{-3})	N^* $\times 10^{19}$ (cm^{-3})	$N^{*-0.5}$ $\times 10^{-10}$ (cm^{-3})	J_P (kA/cm^2)		J_V (kA/cm^2)		PVCR		
					mean	σ	mean	σ	mean	max	σ
BG-TD3‡	0.3 Be	3 Si	0.27	6.06	212	12.3	136	28.8	1.71	1.83	0.06
BG-TD4‡	0.1 Be	1 Si	0.09	10.5	172	16.6	109	30.5	1.63	2.12	0.27
BG-TD5‡	0.15 Be	1.5 Si	0.75	3.65	160	82	20.7	1.03	2.08	2.54	0.25
BG-TD6‡	0.15 Be	1.5 Si	0.75	3.65	200	123	84	1.10	1.87	2.27	0.14

‡ $< 100 >$ GaSb substrates

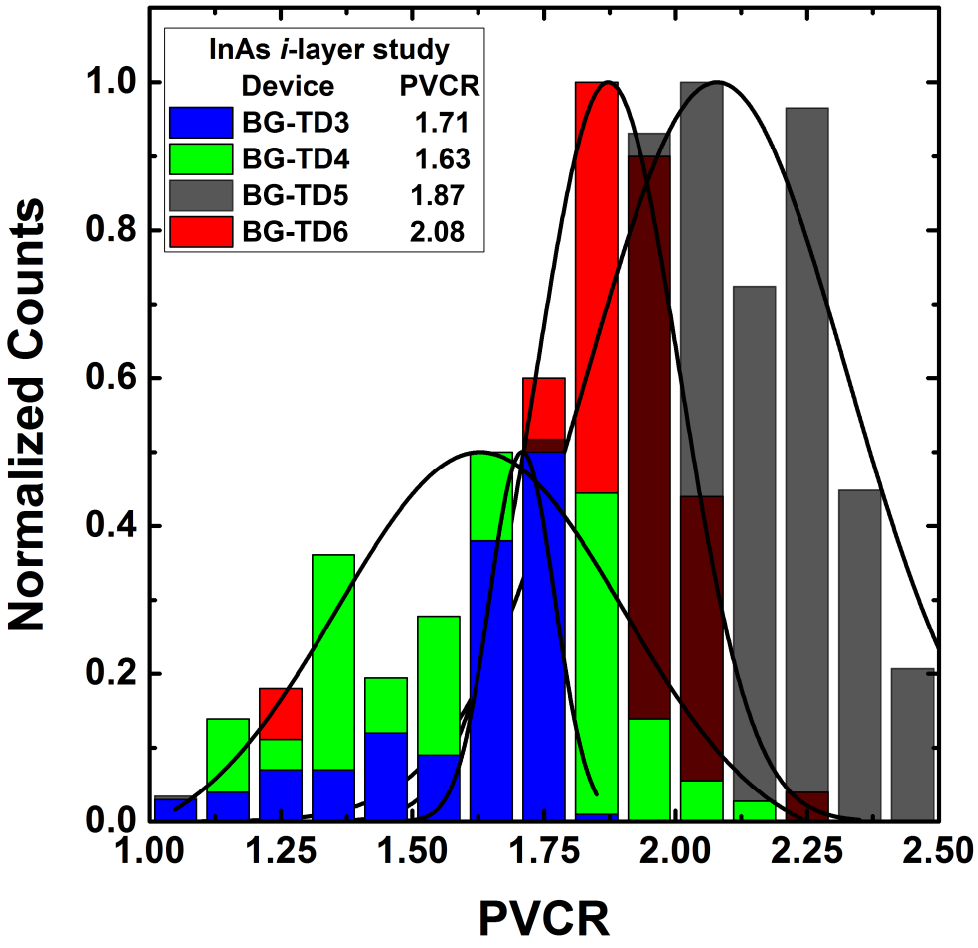


Figure 6.20: Normalized J_P histograms for InAs i-layer study showing the effect of InAs thickness on J_P. As expected, decreasing the i-layer thickness causes an increase in J_P. Confounding the results are the values from BG-TD3 and BG-TD5, which both have a 3 nm i-layer but is likely related to growth system drift.

6.4 Broken Gap δ-Doping Series

With BG-TD1 representing the maximum doping available from TSU, alternative doping methods were investigated. It is well known that δ-doping is an effective means for creating highly doped regions in a semiconductor [152, 153]. Under the premise that δ-doping could increase J_P, this series of BG devices investigates two different doping schemes. Fig. 6.21(a) and Fig. 6.21(b) show film schematics for the δ-doping series. BG-TD7 utilizes δ doping in the InAs region, only. Whereas BG-TD8 uses Si for δ-doping in both InAs and GaSb. Utilizing δ-doping in this manner should create high J_P BG Esaki diodes.

50 nm	InAs: Si	5×10^{18} cm^{-3}
3 nm	InAs	uid
300 nm	GaSb: Be	1×10^{19} cm^{-3}
Substrate	GaSb	

(a) Schematic of BG-TD7

50 nm	InAs: Si	5×10^{18} cm^{-3}
300 nm	GaSb: Be	1×10^{19} cm^{-3}
Substrate	GaSb	

(b) Schematic of BG-TD8

Figure 6.21: (a) Schematic of the film stacks for BG-TD7. This structure integrates δ-doping into the design to push N^* higher. (b) Schematic of the film stacks for BG-TD8. This structure integrates δ-doping into both the n and p regions to push N^* higher.

6.4.1 δ-doping Series Materials Analysis

Growth for samples BG-TD7 and BG-TD8 was based on growth rates established by the previous experiments. BG-TD7 had five δ-doping planes at 0 nm, 10 nm, 20 nm, 30 nm, and 40 nm from the InAs i-layer. Each layer was run at the growth rate established for the 3-4$\times10^{19}$ cm^{-3} Si doped InAs for 100 s. Similarly, BG-TD8 six

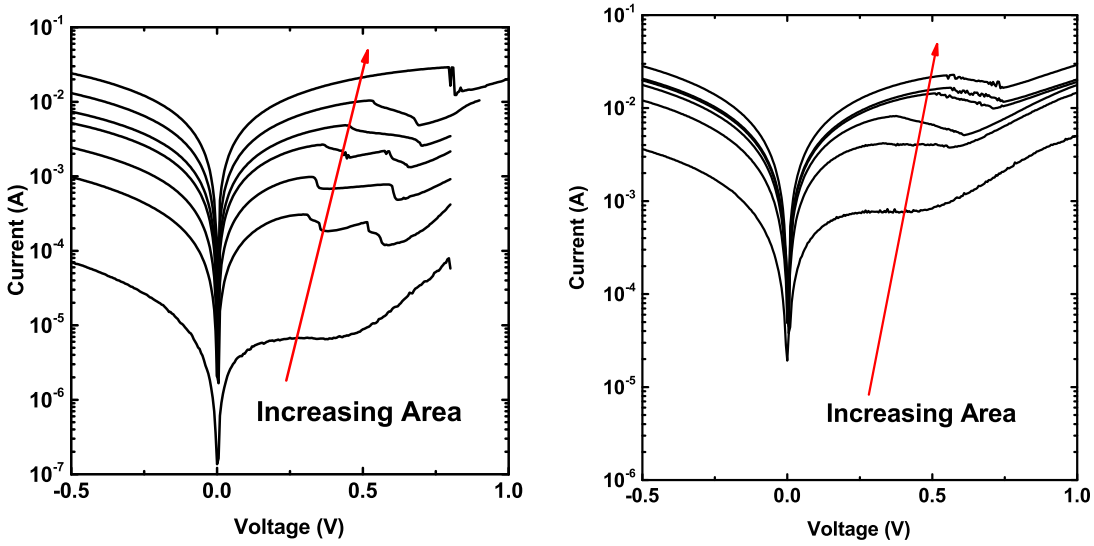
δ-doping planes at -10 nm, 0 nm, 10 nm, 20 nm, 30 nm, and 40 nm from the InAs interface at the previously mentioned growth rate. BG-TD8 utilized Si as a p-type dopant in GaSb, and the growth rated for GaSb was measured as being roughly twice that of InAs, so the δ-doped GaSb Si deposition rate is expected to be on the order of $1 \approx 2 \times 10^{19}$ cm^{-3}.

Samples BG-TD7 and BG-TD8 were fabricated using the techniques established in prior chapters. A blanket Mo layer was deposited on the surface and contacts were designated by negative e-beam resist. During area characterization it became apparent that determination of the exact J_P for these devices would be unlikely due to the odd undercutting of the contacts as shown in Fig. 6.27(a). While J_P may be much higher for these samples, the roughness across the device surface provides inaccurate area measurements.

6.4.2 δ-doping Series Electrical Analysis

Prior to level 2 metallization, samples BG-TD7 and BG-TD8 exhibited low resistance I-V curves which indicated that the samples are highly conductive and would have large J_P. Figs. 6.22(a) and 6.22(b) show representative I-V curves for BG-TD7 and BG-TD8. Both samples are highly conductive and BG-TD7 seems to show a very high J_P.

BG-TD7 and BG-TD8 both appear scale linearly with area, indicating that additional current paths do not dominate small area devices. BG-TD8 had wider variation than BG-TD7, but generally scaled with area and significant deviations are likely due to variation in exposure dose during lithography. In Fig. 6.23(a) the PVCR exhibits a peak at device areas around 6×10^{-9} cm^2, which indicates there may be a processing artifact creating leakage paths for small devices. Fig. 6.23(b) also shows a slight peak in PVCR between 8 and 9 $\times 10^{-8}$ cm^2, with causes similar to those for BG-TD7. Fig. 6.24 compares V_P *vs.* area for BG-TD7 and BG-TD8. V_P for BG-TD7

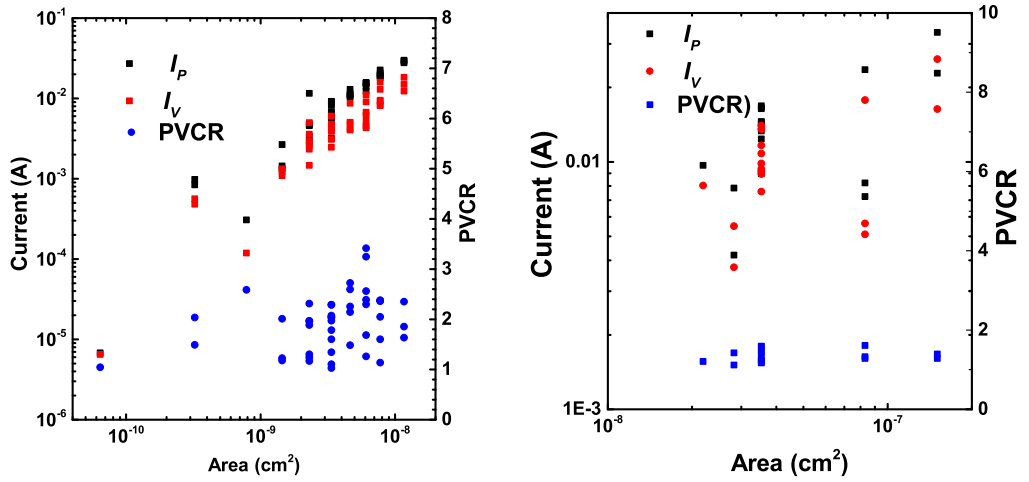


(a) Family of Curves for BG-TD7 **(b)** Family of Curves for BG-TD8

Figure 6.22: Family of I-V curves for δ-doped BG series. L2 metal was required to get samples to show NDR, indicating a current density over 100 kA/cm^2 for the δ-doped samples.

has a minimum near 0.25 V, indicating a low R_S for the device. V_P for BG-TD8 is less clear, additional sample measurements would probably have a result similar to BG-TD8 but due time constraints no further measurements were made.

As with previous sections PVCR and J_P were extracted from Gauss fits to the histogram data for BG-TD7 and BG-TD8. BG-TD7 exhibited a J_P of 2.49 MA/cm^2 and a maximum PVCR of 3.42, which is very competitive with the BG-TD1 for PVCR and J_P. However, inconsistent area under the contact and difficulty in calculating N^* with δ-doped regions makes placing the samples on the figure of merit plot difficult. However, based on equations 6.1 and 6.2 (1.2 and 1.3 from Schubert [153]), N^* may be considered to be $\approx$6.8$\times$ 10^{18} cm^{-3} for BG-TD7. Thus N^* could be calculated as 2.5$\times$ 10^{18} cm^{-3} for BG-TD8. For BG-TD8, 432 kA/cm^2 was extracted for J_P and a maximum PVCR was found to be 1.61. Lack of an intrinsic region combined with an unknown Si activation in GaSb probably resulted in the reduced PVCR and J_P for this sample. Additionally, since few devices were tested(46 and 17 each), more measurements would provide more accurate extracted values. δ-doping might provide



(a) I_V, I_P, and PVCR *vs.* area for BG-TD7 **(b)** I_V, I_P, and PVCR *vs.* area for BG-TD8

Figure 6.23: I_V,I_P, and PVCR *vs.* area for δ-doped BG series shows a general current scaling trend. PVCR for the samples seems to show a peak at larger device areas, which indicates there may be some process related increased to J_V.

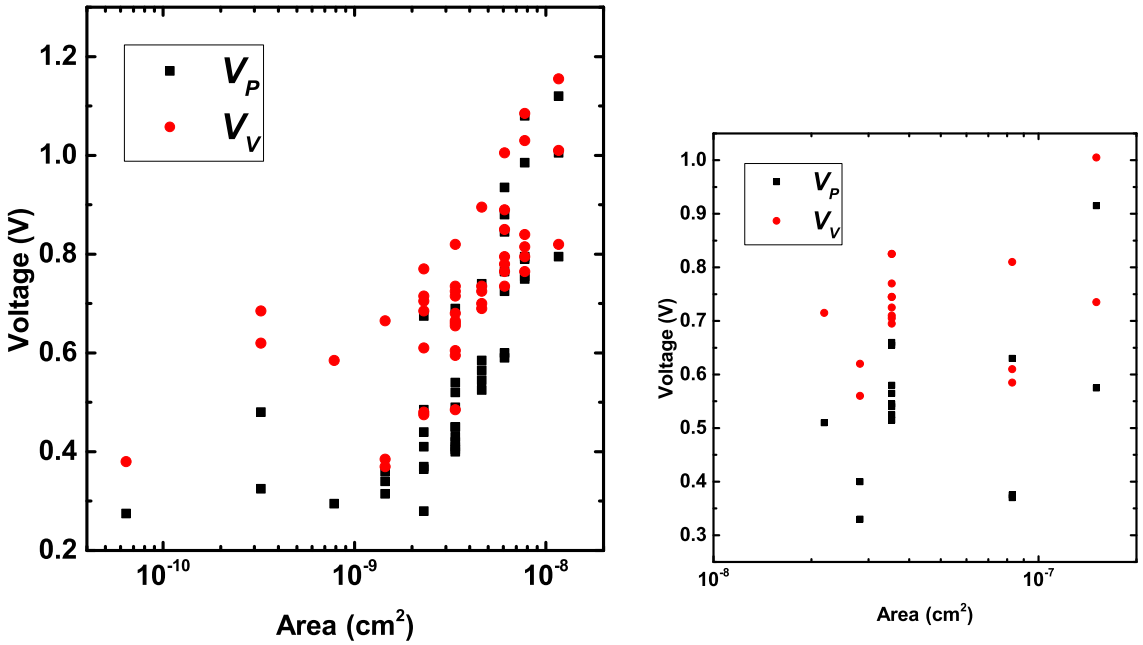
a path to exceeding 10 MA/cm^2 if processing issues can be overcome.

$$N^{2D} = N\nu_g t \tag{6.1}$$

$$N^{3D} = (N^{2D})^{\frac{3}{2}} \tag{6.2}$$

6.4.3 δ-doping Series Summary

In this section BG-TD7 and BG-TD8 were measured and found to exhibit J_P values of 2.49 MA/cm^2 and 432 kA/cm^2, as well as maximum PVCR values of 3.42 and 1.61. These results, summarized in Table 6.3, indicate δ-doping may be on the path to exceeding 10 MA/cm^2, but a few processing issues would need to be addressed. Si doping layers appear to have caused irregularities in etching as seen in Fig. 6.27, a physical component of a dry etch might be less prone to such effects. Further analysis of BG-TD8 would also beneficial in understanding if the reduced performance was related to either the doping change, lack of i-layer, or some combination thereof.



(a) V_P *vs.* area for BG-TD7

(b) V_P *vs.* area for BG-TD8

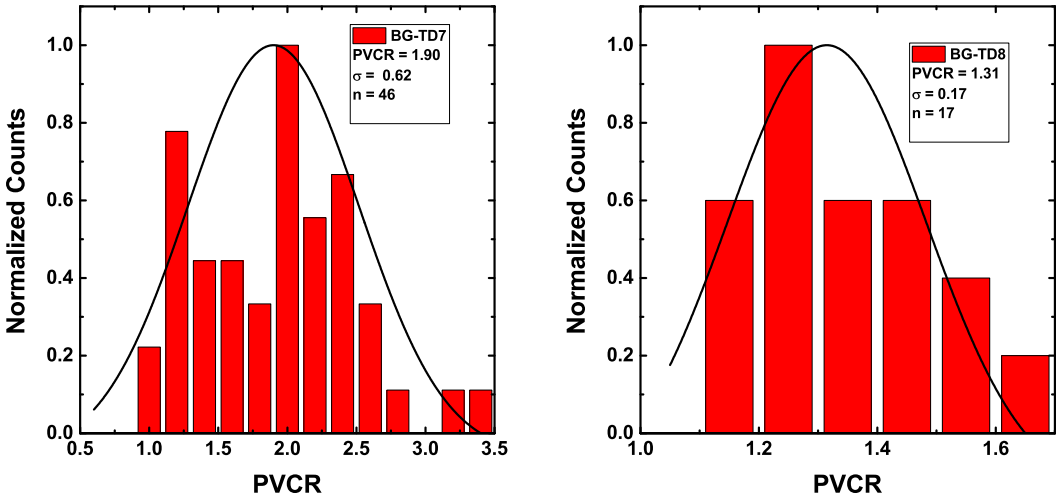
Figure 6.24: (a) V_P *vs.* area for BG-TD7 showing a V_P that should settle near 0.25 V. (b) V_P *vs.* area for BG-TD8 showing that is unclear where V_P should settle without additional data. V_P for both samples indicates that the samples are not limited by R_S

Despite the promise of δ-doping performance, the uncertainty of the device areas and doping lead to a need for the more consistent bulk doping schemes seen in later sections.

Table 6.3: δ-doped BG Diode Data Summary

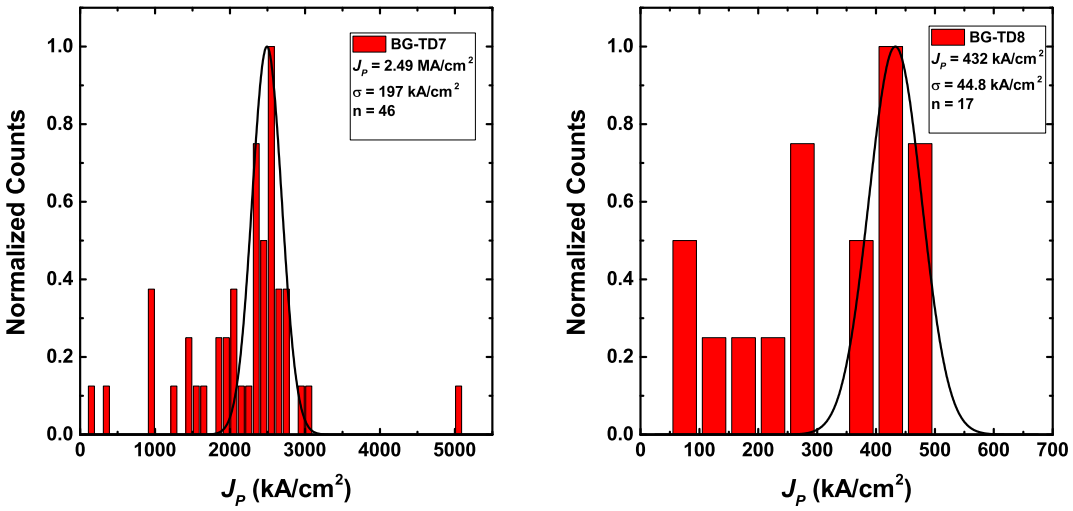
Device	p $\times 10^{19}$ (cm^{-3})	n $\times 10^{19}$ (cm^{-3})	N^* $\times 10^{19}$ (cm^{-3})	$N^{*-0.5}$ $\times 10^{-10}$ (cm^{-3})	J_P (kA/cm^2) mean	J_P (kA/cm^2) σ	J_V (kA/cm^2) mean	J_V (kA/cm^2) σ	PVCR mean	PVCR max	PVCR σ
BG-TD7‡	x Be	x Si	0.68	3.83	2490	197	1173	428	1.9	3.41	0.06
BG-TD8‡	x Si	x Si	0.25	6.32	432	44.8	236	104	1.31	1.61	0.17

‡ < 100 > GaSb substrates



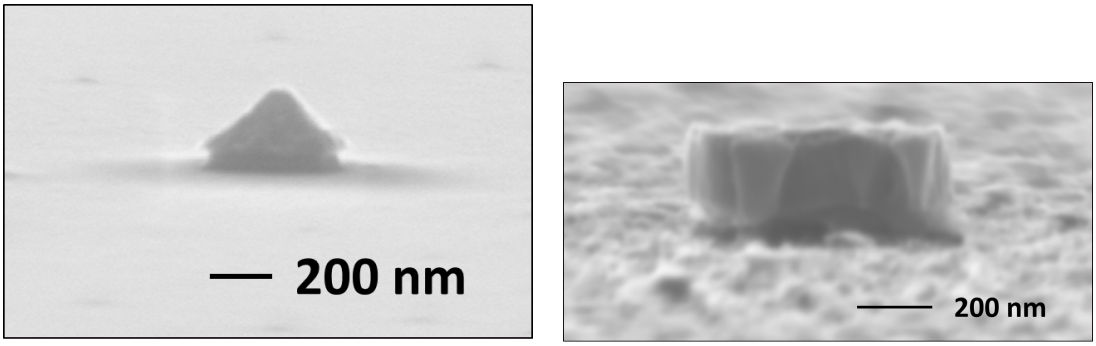
(a) PVCR Histogram for BG-TD7 **(b)** PVCR Histogram for BG-TD8

Figure 6.25: (a) PVCR exhibits a maximum of 3.42 and a mean of 1.9 which is consistent with high doped BG samples being greater than lower doped samples. (b) With a maxmimum PVCR of 1.61 and mean of 1.31, the δ-doping scheme used for BG-TD8 appears to be less effective or in need of optimization. PVCR for both samples was extracted from a Gauss fit to the histogram data, the small data set for BG-TD8 may skew the results.



(a) Histogram of J_P for BG-TD7 **(b)** Histogram of J_P for BG-TD8

Figure 6.26: Histogram of J_P for δ-doped BG series from J_P values were extracted from Gauss fits. BG-TD7 shows a J_P of 2.49 MA/cm^2 and BG-TD8 shows 432 kA/cm^2. Etch inconsistencies for the samples necessitated approximations for extracted values, development of alternative etch processes such as RIE may alleviate this issue.



(a) Micrograph of BG-TD7 **(b)** Micrograph of BG-TD8

Figure 6.27: As shown in the SEM micrographs (a) and (b), processing issues confound area analysis by leaving uneven contacts and possible shorts to the mesa.

6.5 Broken Gap Series 2

This section investigates samples grown by a commercial grower, IQE, in an attempt to push doping levels higher than what had been available at TSU. Samples were designed to be similar to BG series 1 devices, but with higher doping levels and on <100> GaSb wafers miss cut 0.35° to <111>. Film schematics for the devices in this section are shown in Fig. 6.28. Sample BG-TD9 from Fig. 6.28(a) is designed to match the performance of BG-TD1 to ensure that BG device performance is not growth system dependent. BG-TD10 and BG-TD11, Figs. 6.28(b) and 6.28(c), were designed to exceed the doping levels of BG-TD1 with the expectation that BG-TD11 might approach 10 MA/cm^2.

50 nm	InAs: Si	3×10^{19} cm^{-3}
3 nm	InAs	uid
20 nm	GaSb: Be	1×10^{19} cm^{-3}
280 nm	GaSb: Be	
Substrate	GaSb	

(a) BG-TD9

50 nm	InAs: Si	5×10^{19} cm^{-3}
3 nm	InAs	uid
20 nm	GaSb: Be	5×10^{19} cm^{-3}
280 nm	GaSb: Be	
Substrate	GaSb	

(b) BG-TD10

40 nm	InAs: Si	1×10^{20} cm^{-3}
10 nm	InAs: Si	uid
3 nm	InAs	5×10^{19} cm^{-3}
20 nm	GaSb: Be	
280 nm	GaSb: Be	
Substrate	GaSb	

(c) BG-TD11

Figure 6.28: (a) Schematic of the film stack for BG-TD9 which is supposed to match doping and performance levels of BG-TD1. (b) BG-TD10 film stack with target doping levels higher which should result in J_P over 2.2 MA/cm^2. (c) BG-TD11 film stack representing highest doping levels capable from IQE equipment, which should be close to 10 MA/cm^2, but is short of the N^* of 5×10^{19} cm^{-3} which should guarantee 10 MA/cm^2.

6.5.1 Broken Gap Series 2 Materials Analysis

BG series 2 materials analysis included HRXRD, SIMS, and Raman spectroscopy from which some interesting characteristics were notable. HRXRD $\omega/2\theta$ plots supplied by the vendor indicate excellent crystallinity for BG-TD9 and BG-TD10 as seen in Fig. 6.29. Deviations from target doping levels is apparent from SIMS for series 2 as seen in Fig. 6.30. Additionally, there appear to be slight material differences between series 1 and 2 that appear in both the HRXRD and SIMS profiles. Raman spectroscopy was also performed on the BG series 2 samples, and exhibited a trend that tracked with doping concentration.

HRXRD $\omega/2\theta$ plots supplied by the vendor indicate excellent crystallinity for BG-TD9 and BG-TD10 as seen in Fig. 6.29. HRXRD also showed there was significant relaxation in BG-TD11. As such, the resultant InAs film will likely exhibit high excess currents thereby masking any NDR behavior for BG-TD11. Notably, there does not appear to be a secondary peak near the substrate peak which indicates the IQE chamber is capable of removing residual As from flux measurements at a greater rate than chamber 7 at TSU.

SIMS was performed by EAG labs to confirm doping concentrations within the series 2 samples, a second sample from BG-TD1 was included to ensure that system drift could be ruled out. SIMS results for all the samples from series 2 are shown in Fig. 6.30 where it quickly becomes apparent that doping levels are not quite to targeted levels. BG-TD9 is close to target Si and Be levels, with Si being low and Be on the high side. BG-TD10 hits near 1×10^{20} cm^{-3} Si doping and 3×10^{19} cm^{-3} Be doping, which is twice the intended Si doping and half the Be target and provides a 10% lower N^* of 2.31×10^{19} cm^{-3}. BG-TD11 appears to exceed 2×10^{20} cm^{-3} Si, but the Be doping levels are nearly two orders of magnitude higher in the InAs region than they should be. If BG-TD11 can show NDR, it will not be without significant difficulty due to the broad doping profiles. However, BG-TD9 and BG-TD10 should

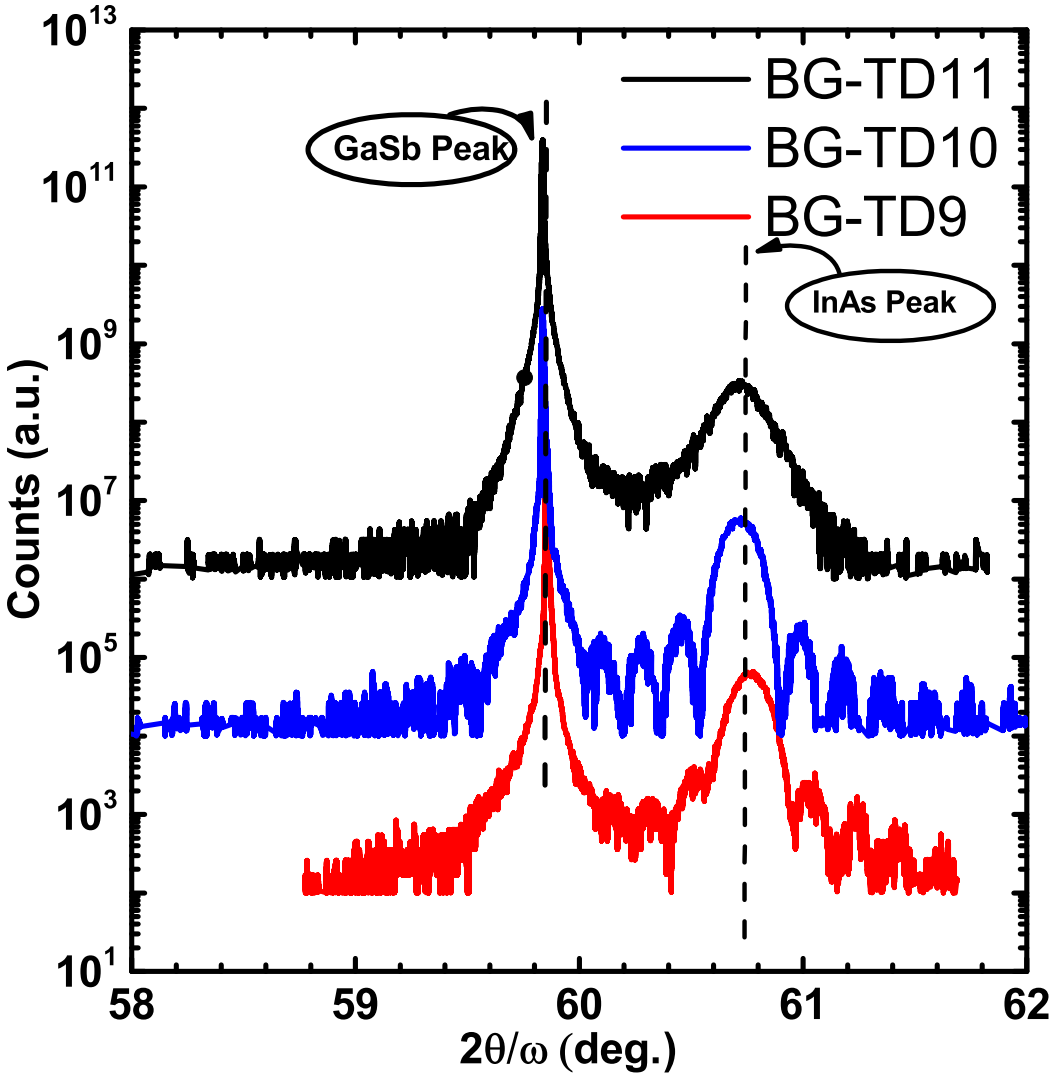


Figure 6.29: HRXRD information provided by the vendor show minimal relaxation for BG-TD9 and BGTD-10, while BG-TD11 appears to be fully relaxed. NDR should be expected to appear for samples BG-TD9 and BG-TD10, however the relaxation in BG-TD11 will be problematic for extracting tunneling characteristics. BG-TD11 will likely perform similarly to SSG-TD3, being highly conductive but failing to show NDR due to high defect density related excess current.

provide excellent electrical characteristics on either side of those of BG-TD1.

6.5.2 Broken Gap Series 2 Electrical Results

Samples for BG-series 2 were tested electrically and proved to be slightly more difficult to test than anticipated. BG-TD11 was highly conductive but did not show any instances of NDR as was to be expected from the materials analysis in the previ-

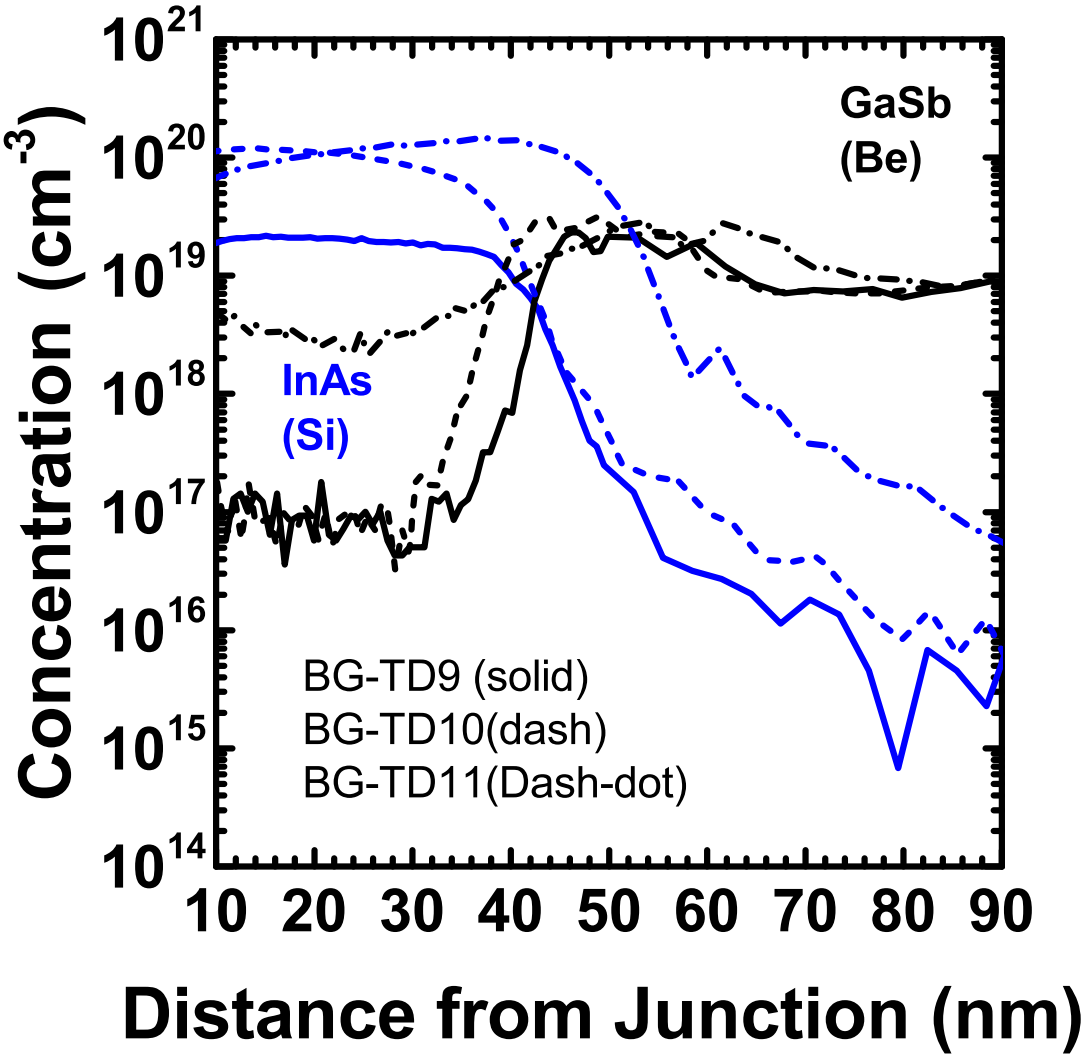
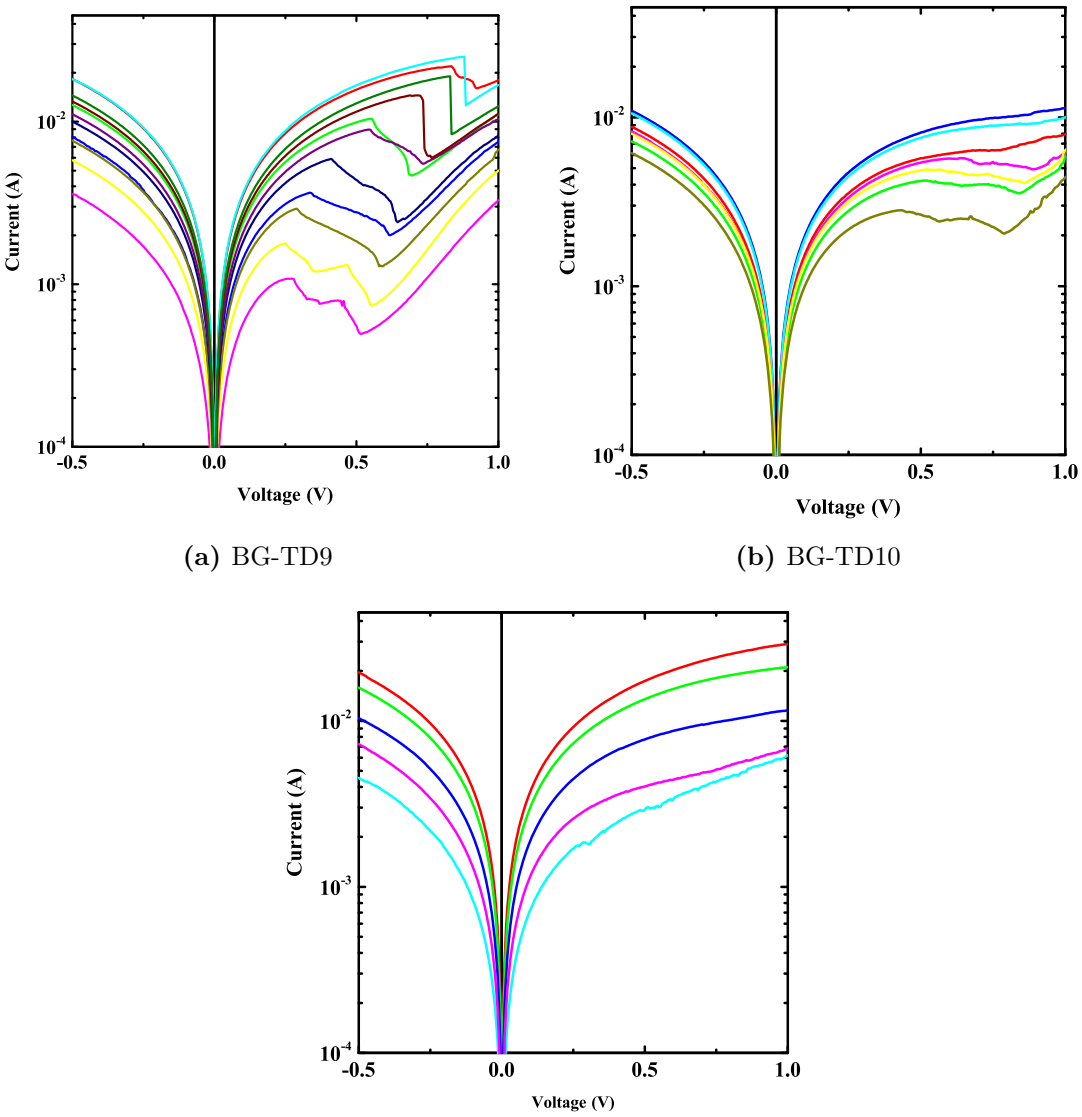


Figure 6.30: SIMS was performed on the samples to determine dopant levels present within the sample. BG-TD9, BG-TD10, and BG-TD11 were found to have Si and Be doping levels near the targeted values. As levels within the GaSb film region were near the detection limit, and should not produce a satellite peak in HRXRD measurements.

ous section. Fig. 6.31(c) exhibits the typical I-V performance for BG-TD11 devices which indicates that further investigation of the sample will be unlikely to yield usable results. Samples BG-TD9 and BG-TD10 benefited from a brief Ammonium Hydroxide etch(NH_4OH:H_2O at a 5:1 ratio) into the GaSb layer, the dual layer nature of the film may have caused some unintended measurement problems. BG-TD9 performance, shown in Fig. 6.31(a), was quite similar to that of BG-TD1 albeit with lower J_P due a lower N^* value. Initial measurements of BG-TD10 exhibited low PVCR

values, however post etch devices performed better as seen in Fig. 6.31(b).



(a) BG-TD9

(b) BG-TD10

(c) BG-TD11

Figure 6.31: (a) BG-TD9 performed similarly to BG-TD1, per its design, but exhibited lower PVCR. (b) BG-TD10 generally exhibited higher J_P, but was also more difficult to measure due to R_S effects combined with the high J_P. (c) BG-TD11 exhibited some kinks in the I-V characteristic, but did not show NDR at any device size. There were likely too many defects in this sample that masked the tunneling performance.

R_S appears to be problematic for the high J_P sample. V_P performance of BG-TD9 was very similar to BG-TD1. BG-TD10 appears to be affected by R_S in that it shows V_P values over 0.45 V down to the smallest measured devices.

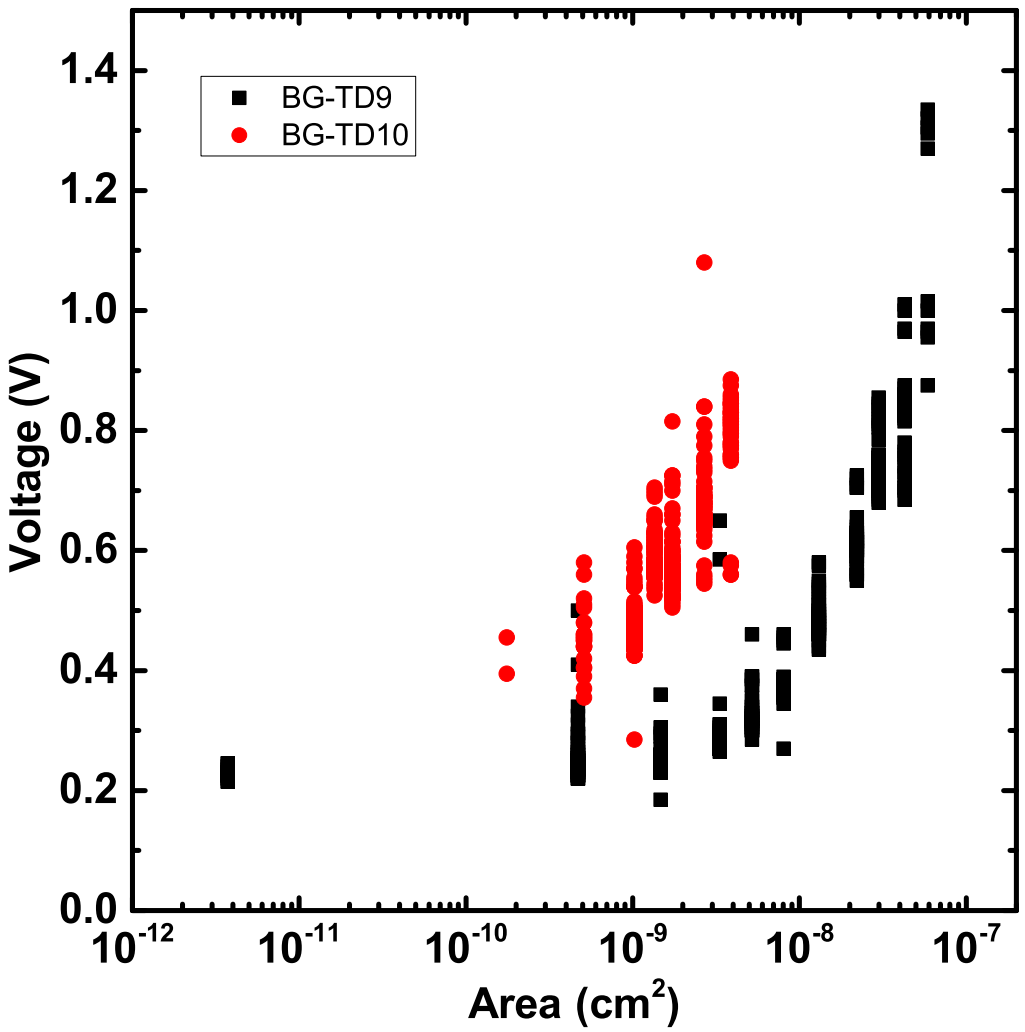


Figure 6.32: Typical minimum V_P values for series 2 devices appear to fall between 0.3 V and 0.2 V, with greater influence from R_S for BG-TD10 due to the higher J_P.

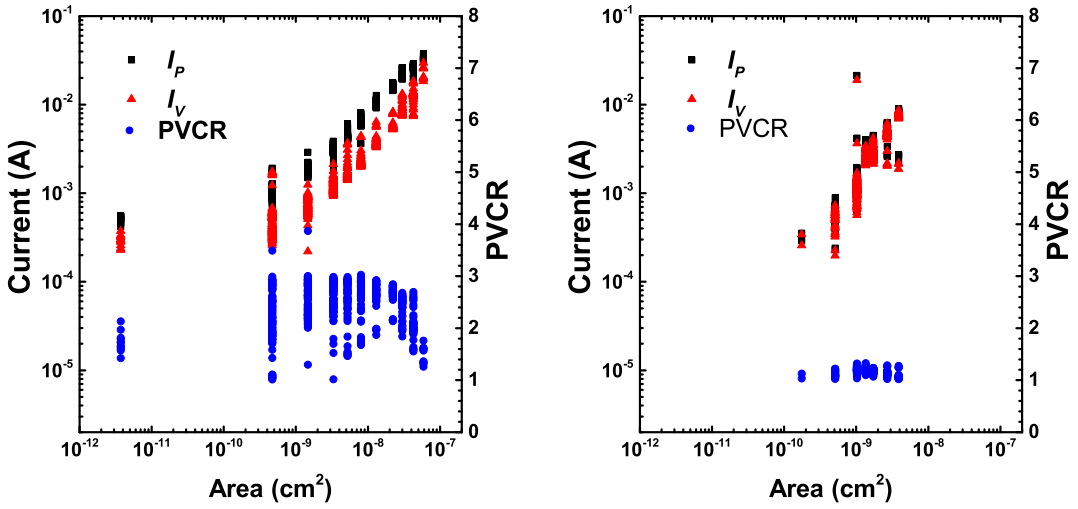
Table 6.4: Broken Gap Tunnel Diode Series 2 Summary

Device	p $\times 10^{19}$ (cm^{-3})	n $\times 10^{19}$ (cm^{-3})	N^* $\times 10^{19}$ (cm^{-3})	$N^{*-0.5}$ $\times 10^{-10}$ (cm^{-3})	J_P (kA/cm^2) mean	J_P (kA/cm^2) σ	J_V (kA/cm^2) mean	J_V (kA/cm^2) σ	PVCR mean	PVCR max	PVCR σ
BG-TD9†	3 Be	1.5 Si	1	3.16	1860	175	726	214	2.62	3.49	0.33
BG-TD10†	3 Be	8 Si	2.14	10.5	3212	302	2867	532	1.18	2.24	0.05
BG-TD11†	3 Be	15 Si	2.5	2	-	-	-	-	-	-	-

† < 100 > GaSb substrates miscut 0.35° <111>

6.5.3 Broken Gap Series 2 Summary

This section reported BG tunnel diodes with a J_P of 3.2 MA/cm^2. Notably, p-type doping can still be increased to reach the 10 MA/cm^2 target [47]. These diodes show



(a) BG-TD9 (b) BG-TD10

Figure 6.33: Current was shown to scale for both BG-TD9 and BG-TD10 with area.

the potential for the BG heterojunction systems to meet the requirements placed on TFETs to replace CMOS and the results are summarized in Table 6.4. As incorporation into the GaSb layer does not appear to be detrimental to the final output current. However, the change from <100> substrates to miscut substrates does appear to lower PVCR, and will be examined further in Section 6.6. Additionally, BG-TD9 exhibited a J_P of 1.8 MA/cm^2 which is close to the target of 2.2 MA/cm^2 based on the BG-TD1 sample. While BG-TD11 did not produce measurable tunnel characteristics, the InAs/GaSb BG system can likely exhibit J_P near 10 MA/cm^2 since the both Si and Be dopants can exceed 10^{20} cm^{-3} within their respective layers [47, 144].

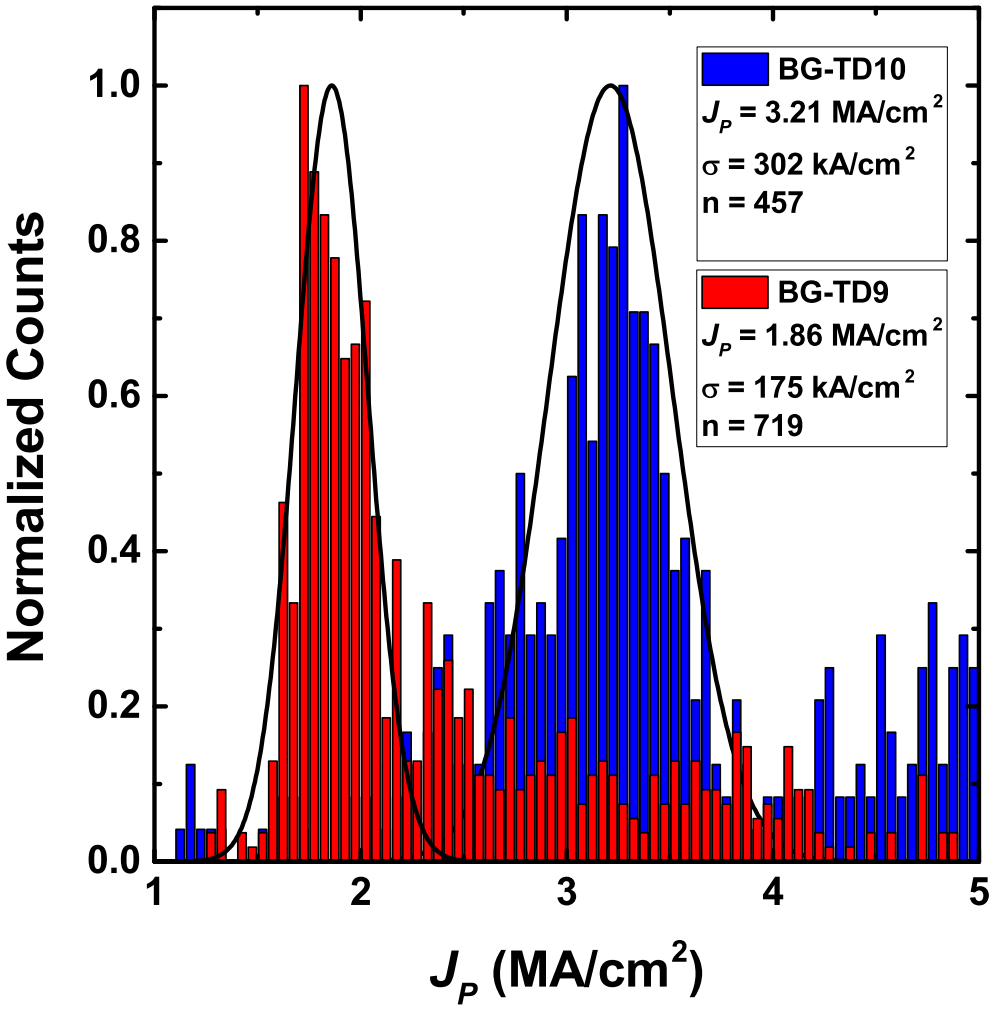


Figure 6.34: Normalized J_P histograms for series 2 study showing 1.82 MA/cm^2 and 3.21 MA/cm^2 J_P for BG-TD9 and BG-TD10. Based on the SIMS data, J_P may be pushed higher if both dopants can exceed 1×10^{20} cm^{-3}.

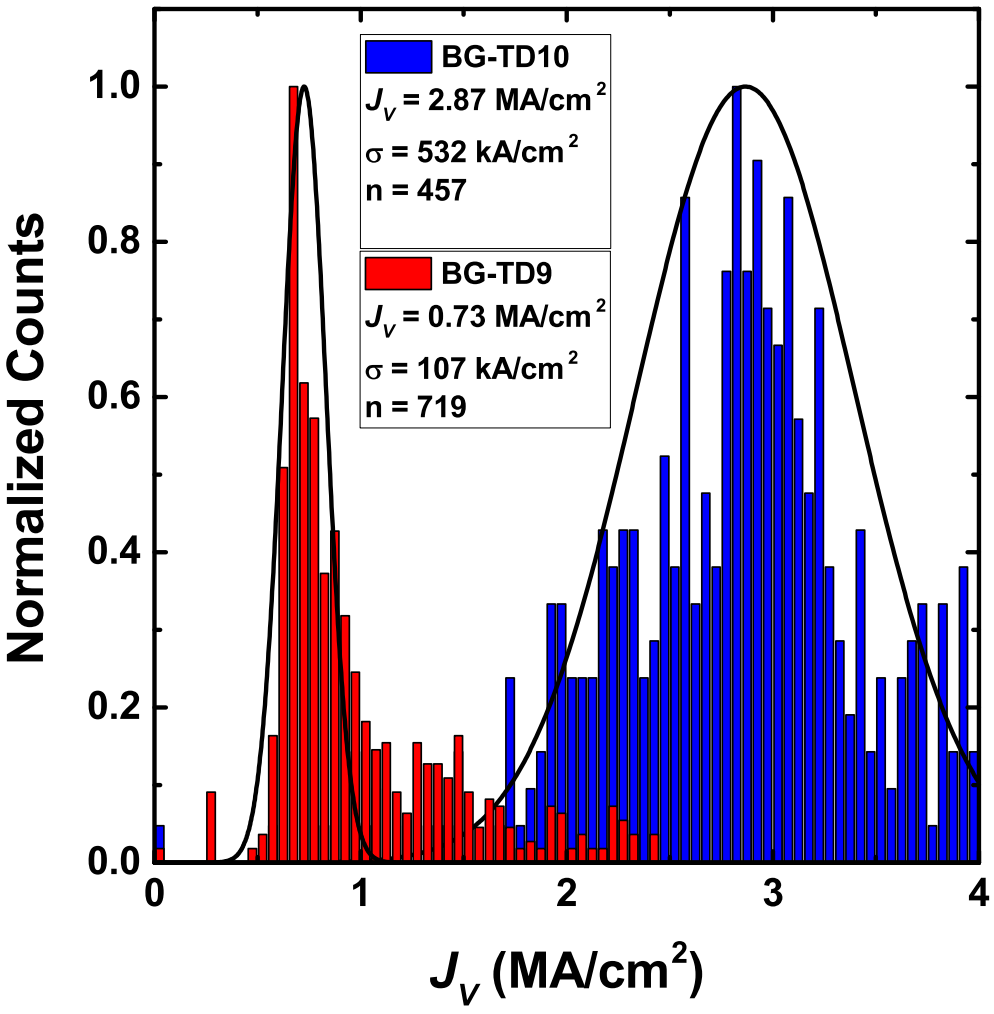


Figure 6.35: Normalized J_V histograms for series 2 study. BG-TD10 shows wider variation likely due to the additional processing requirements to etch into the GaSb layer.

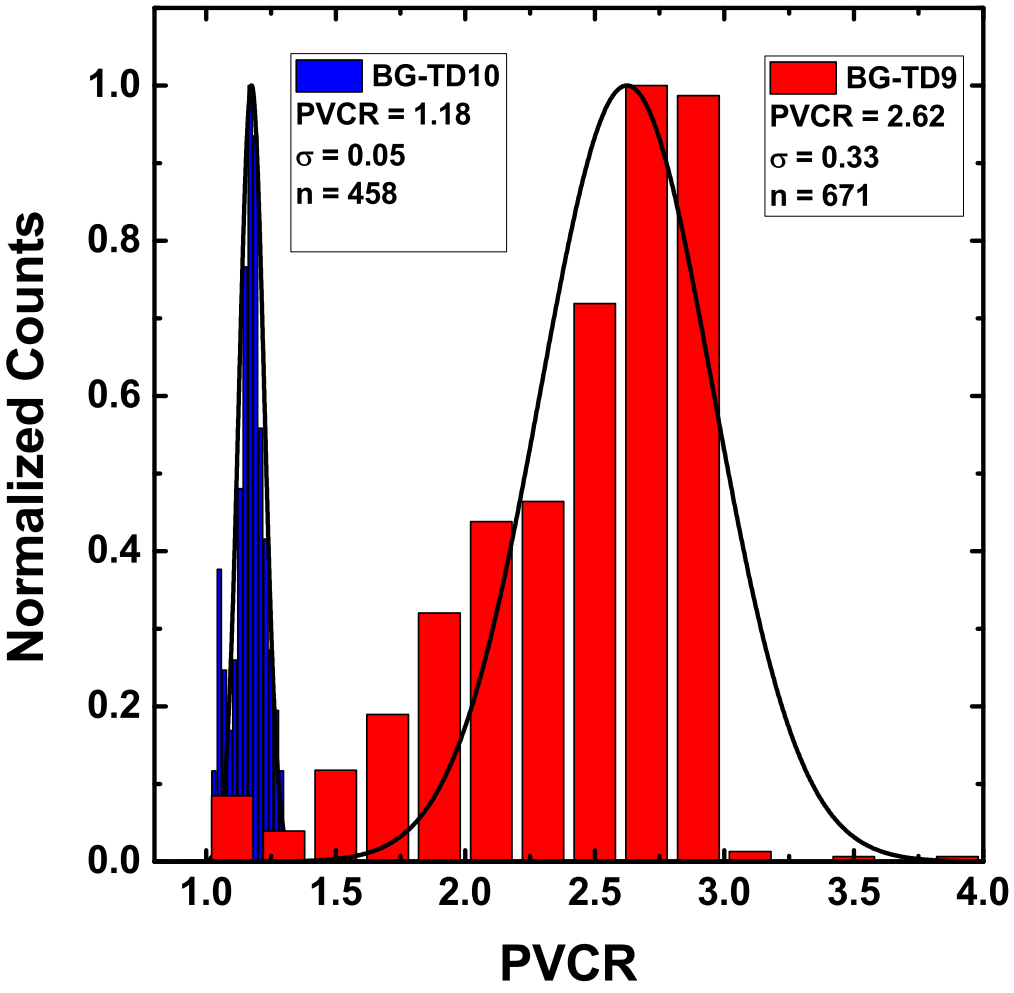


Figure 6.36: Normalized PVCR histograms for series 2 study showing that, after a peak value, PVCR is reduced with increased doping as has been shown in multiple other material systems.

6.6 Series 1 to Series 2 Comparison

Broken Gap series 1 and series 2 were designed to push J_P towards 10 MA/cm^2, but they also present an opportunity to compare growers. Because the samples were grown in different reactors by different growers, a comparable device needed to be built at both sites. BG-TD1 and BG-TD9 are the comparable devices between TSU and IQE. From Fig. 6.37, current scaling is not an issue for any of the grown devices. Further comparing the J_P peaks in Fig. 6.38 reveals that both BG-TD1 and BG-TD9 are very similar and have overlapping σ.

HRXRD of both BG-TD1 and BG-TD9 were performed, as can be seen in Fig. 6.39. Because of the miscut of 0.35° towards <111> on BG-TD9, the XRD plots were aligned to the GaSb (400) peak to provide an easier comparison between the two samples. It becomes immediately apparent that BG-TD9 lacks the satellite peak that exists in the prior samples. A discussion with Prof. Droopad determined that this peak was likely As incorporation due to As remaining following As flux measurements. The excess As signal in Fig. 6.40 also confirms this theory.

Determining the origins for the performance difference between the two samples warranted TEM analysis. Both samples were exceptionally defect free as seen in Fig. 6.41(a) and Fig. 6.41(b). However, BG-TD1 was found to have an InSb like interface between InAs and GaSb in Fig. 6.42, while BG-TD9 was found to have a GaAs-like interface in Fig. 6.43. Studies by Khan-Cheema et al. [154] had shown a that there can be a influence on V_P and J_P due to the heterointerface.

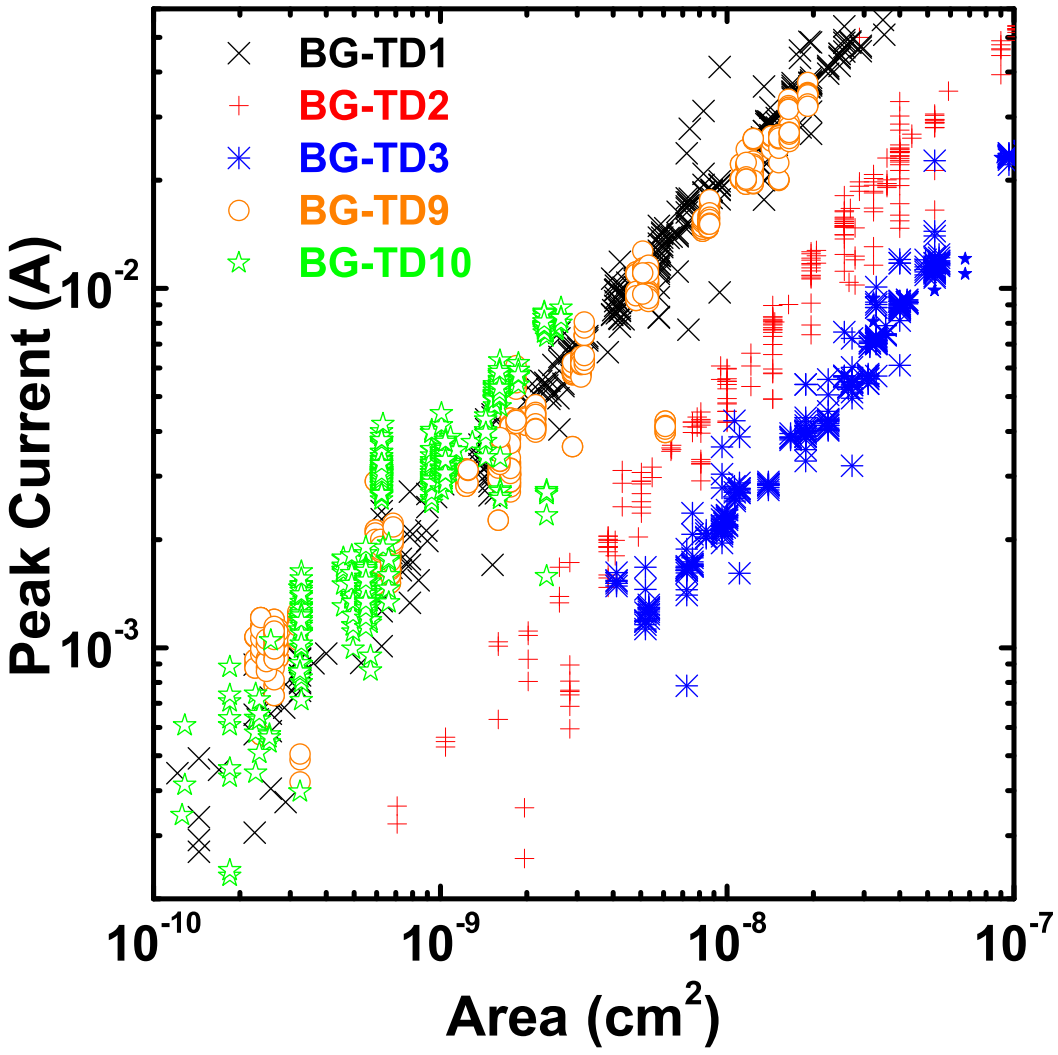


Figure 6.37: I_P scaled with area for the BG series 1 and series 2 diodes. The wider spread in I_P for BG-TD10 is due to the increased area variability from a two-step mesa etch process.

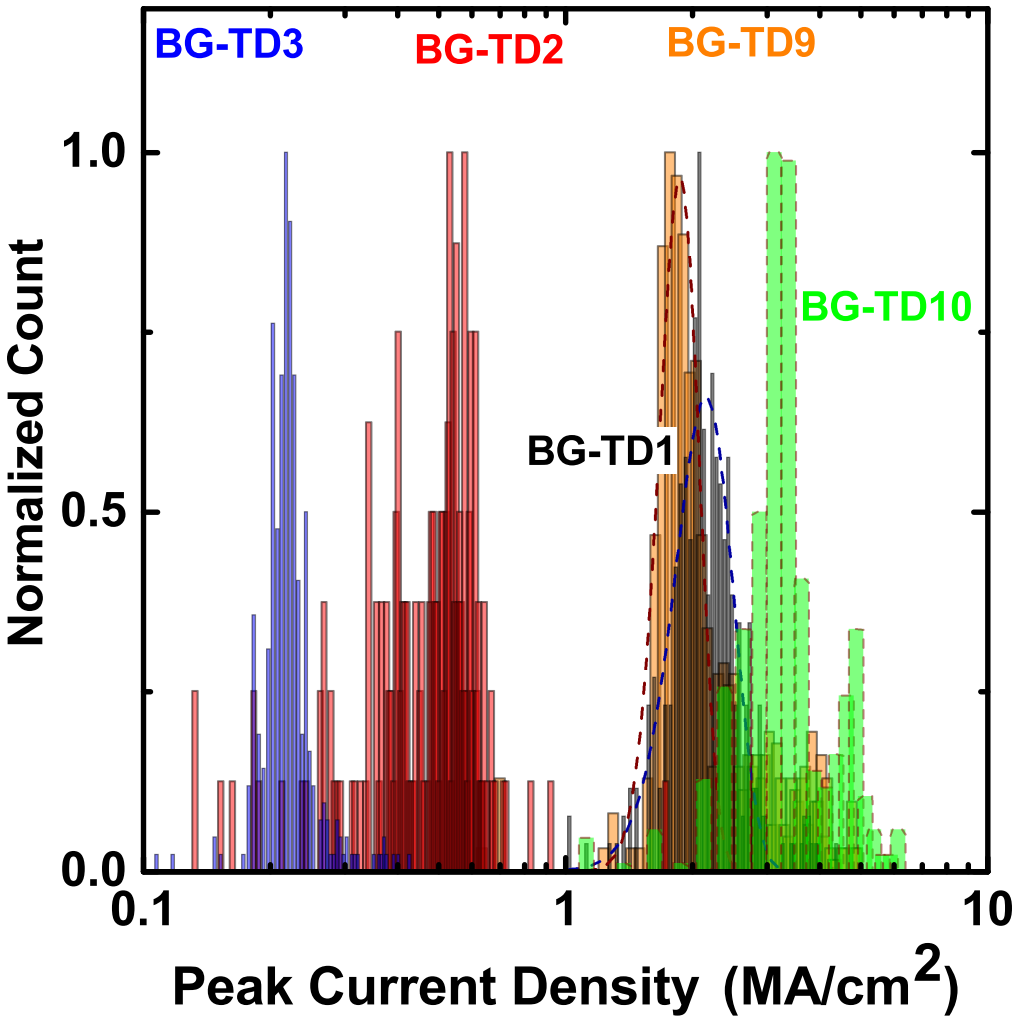


Figure 6.38: J_P histograms for the Series 1 and Series 2 BG diodes. BG-TD1 and BG-TD9 were nearly identical and BG-TD10 exhibits J_P greater than 3 MA/cm^2.

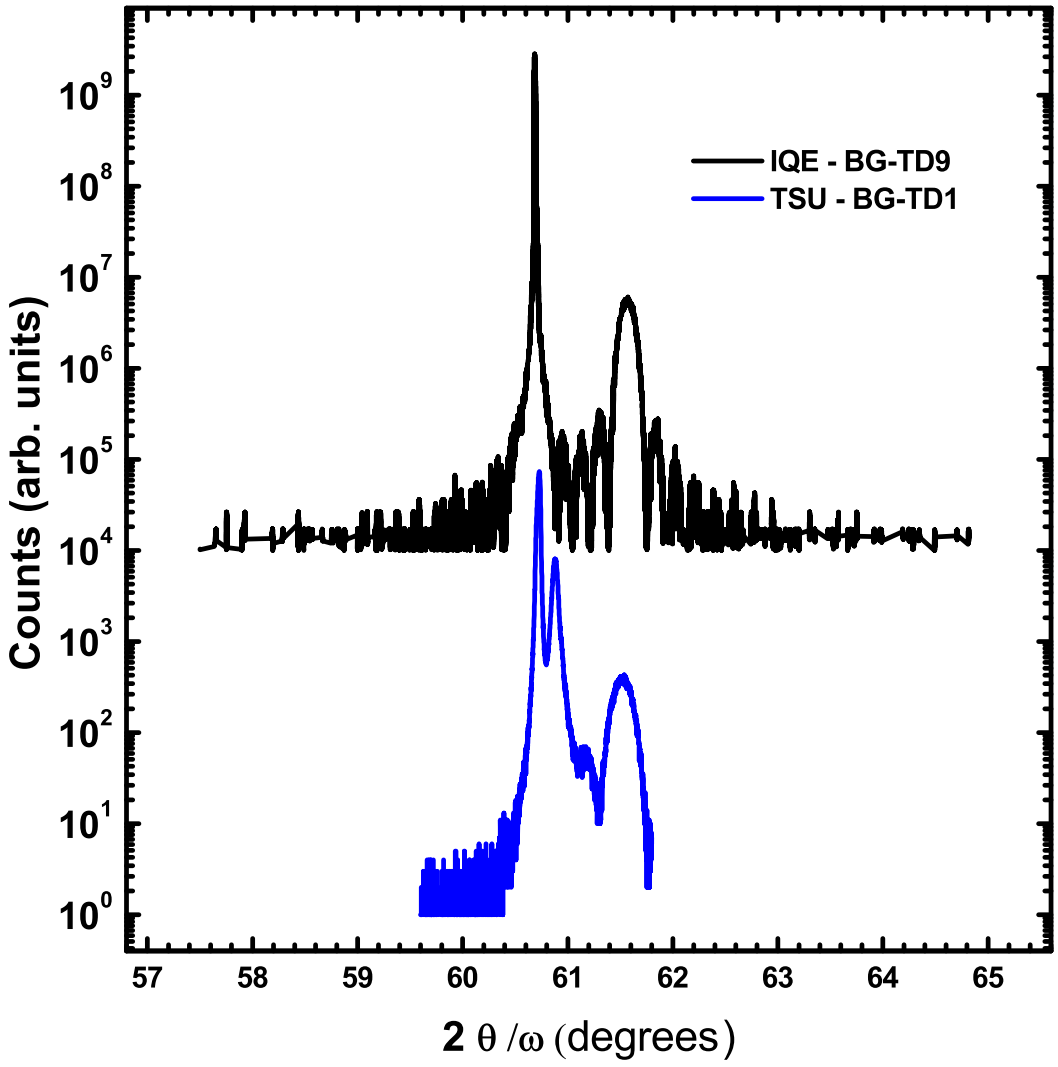


Figure 6.39: HRXRD of BG-TD1 and BG-TD9 samples indicates the presence of an offcut as well as the lack of a secondary peak near the GaSb substrate peak for BG-TD9, a correction of 0.7° was inclduded to align the GaSb peaks. The excellent crystal structure of both samples would indicate that dislocation defects should have minimal impact on device performance.

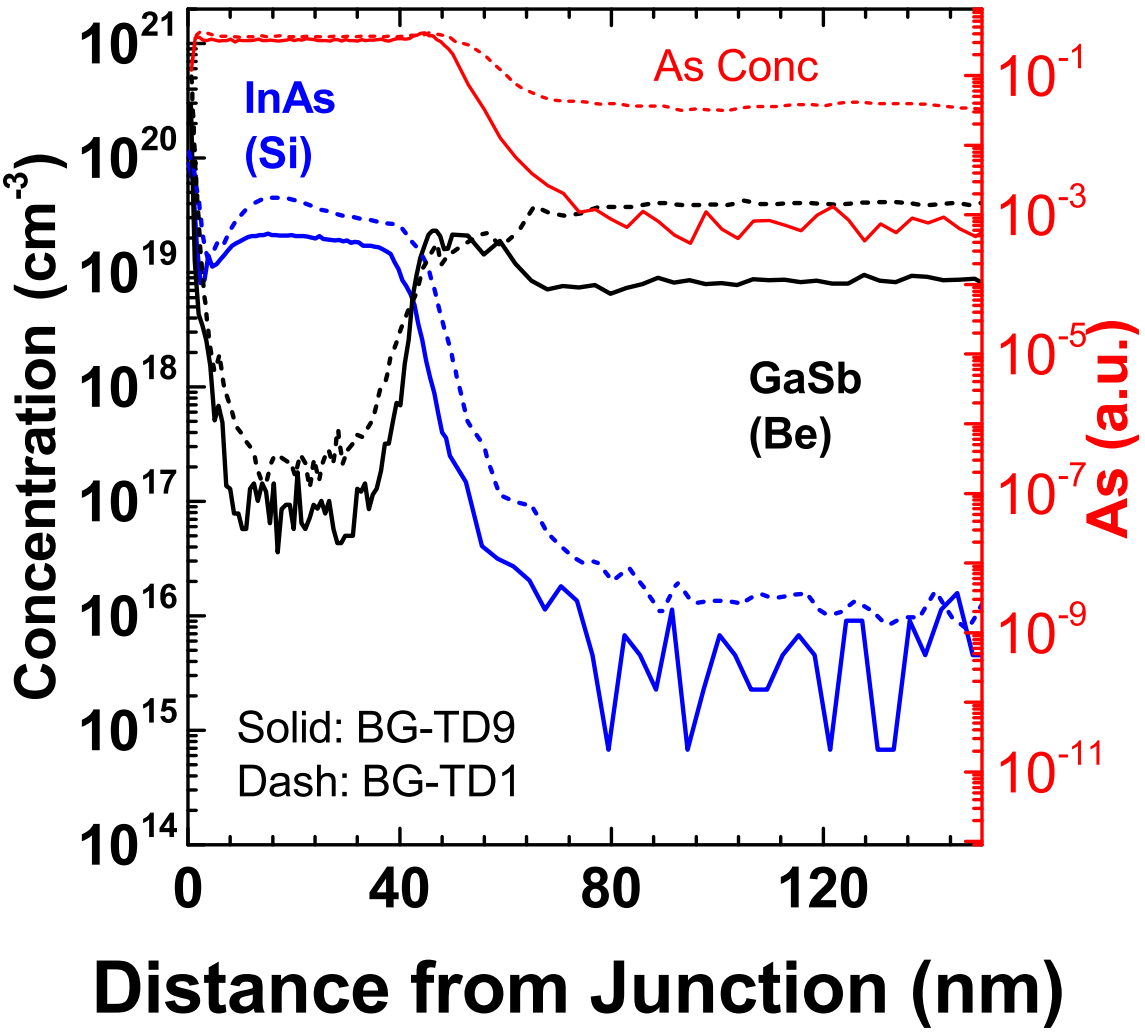
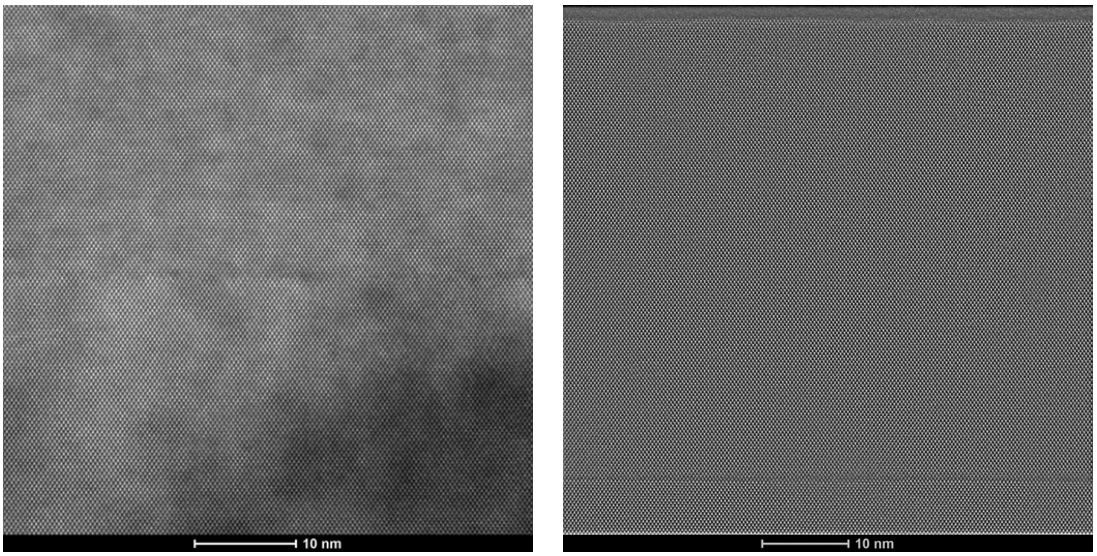


Figure 6.40: SIMS of BG-TD1 and BG-TD9 samples indicates the presence of an As in BG-TD1. Doping for BG-TD9 was slightly lower than that of BG-TD1



(a) BG-TD1 TEM of heterointerface **(b)** BG-TD9 TEM of heterointerface

Figure 6.41: TEM micrographs of the heterointerfaces for both BG-TD1 and BG-TD9 exhibit no visible defects, indicating excellent crystal quality for both samples.

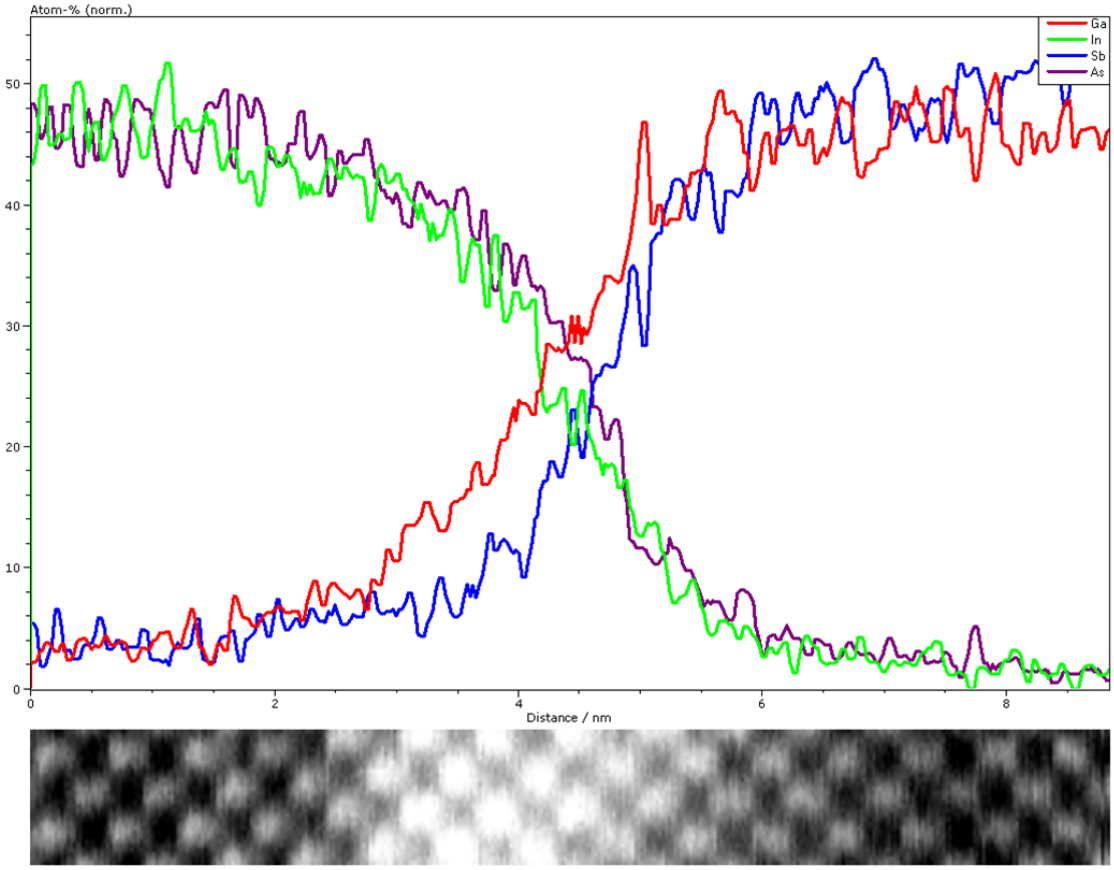


Figure 6.42: XPS during TEM analysis of the BG-TD1 junction shows an InSb like interface and was found to be largely defect free.

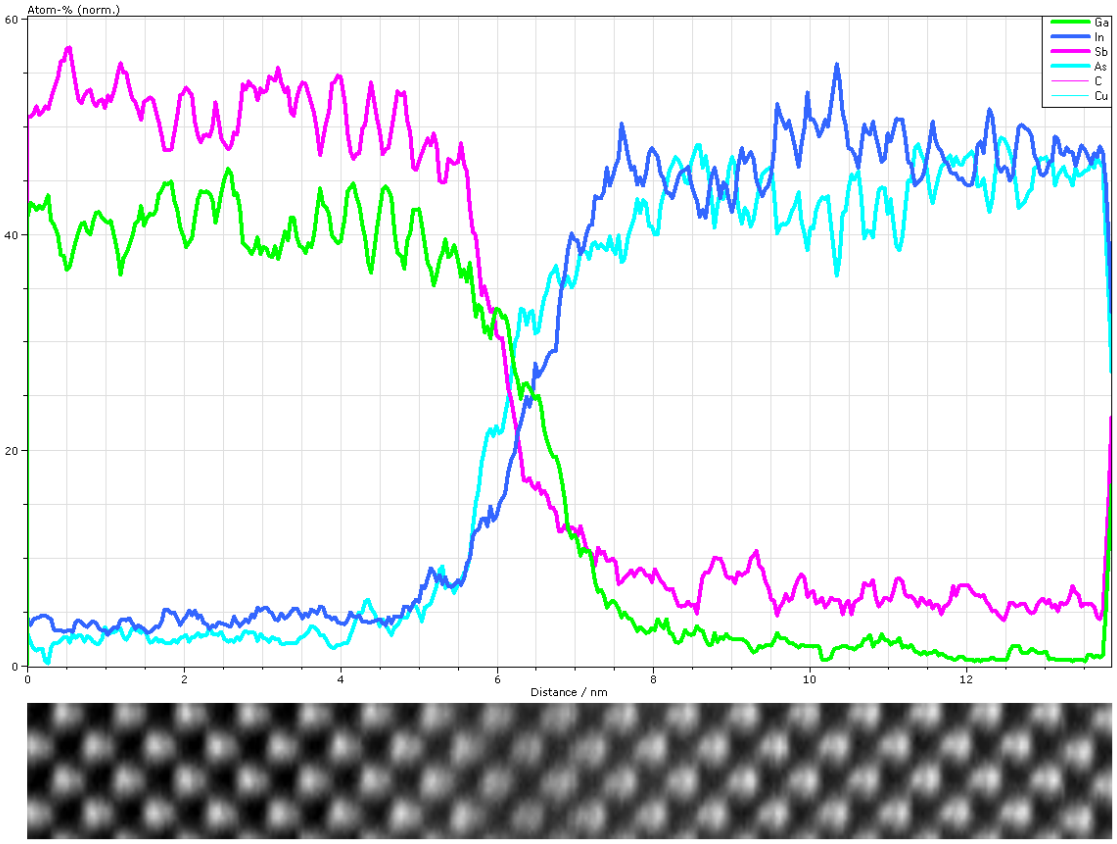


Figure 6.43: XPS during TEM analysis of the BG-TD9 junction shows an GaAs like interface and was found to be largely defect free.

6.7 GaSb *i*-layer study

Previous reports have indicated some sensitivity to i-layer design for Esaki diode performance in the BG diode systems [50]. This section investigates the substitution of the i-layer from InAs to GaSb. Fig. 6.44 shows schematics representing the devices tested in this series. Changes with respect to BG-TD2 include: Te substituted for Si as the n-type dopant, substrates are now on miss cut wafers, InAs thickness has been slightly reduced, and the i-layer consists of GaSb. Te does not have the same counterdoping problems as Si, but the dopings levels are not so high as to expect dopant species to be much of an issue. Changing to miss cut wafers is theorized to be better for epitaxy, but prior results from this study do not appear to exhibit any impact due to this change. Thinner InAs should reduce the likelihood of problems associated with critical thickness from appearing. Changing to GaSb from InAs in the i-layer may affect performance due to the more extreme bending seen in GaSb, but the tunnel region for the BG diodes is larger than the i-layer and may show little or no impact on J_P and J_V.

50 nm	InAs: Si	1×10^{19} cm^{-3}
3 nm	InAs	uid
300 nm	GaSb: Be	5×10^{18} cm^{-3}
Substrate	GaSb	

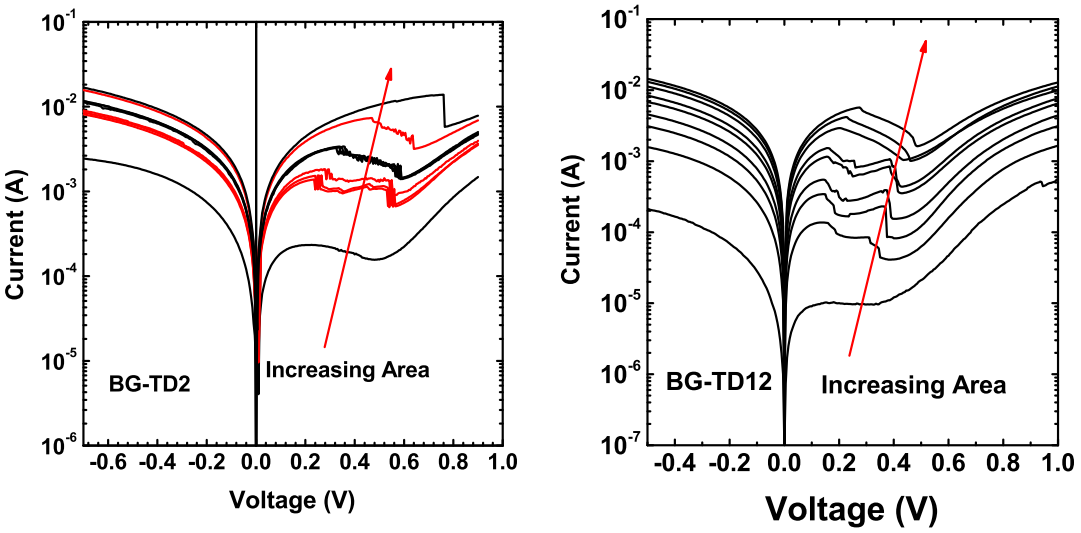
(a) BG-TD2

25 nm	InAs: Te	1×10^{19} cm^{-3}
3 nm	GaSb	uid
300 nm	GaSb: Be	5×10^{18} cm^{-3}
Substrate	GaSb	

(b) BG-TD12

Figure 6.44: (a) and (b) Schematic of the film stacks for samples BG-TD2 and BG-TD12 compared in this study. Doping levels are targeted around an N^* value of 1.5×10^{19} dopants per cm^3 which allows for the highest PVCR for a given diode J_P.

At first glance current scaling in Fig. 6.45 illustrates that InAs and GaSb i-layer devices perform similarly. However, further analysis will show some subtle but important differences when changing i-layer material. PVCR and V_P appear to be affected by the change in i-layer, with both characteristics showing improvement. PVCR for the GaSb i-layer tends to be greater and V_P tends to be lower.

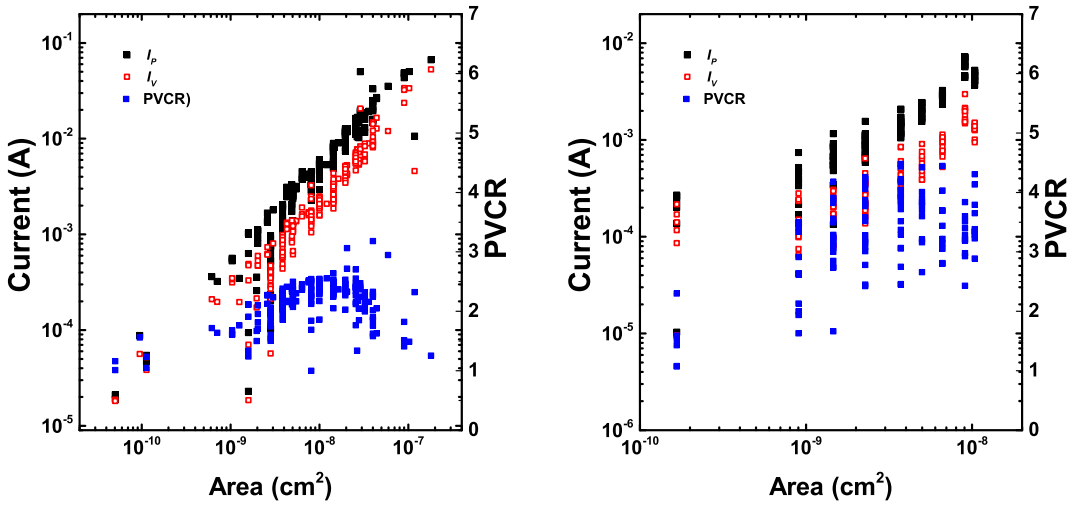


(a) Family of I-V Curves for BG-TD2 **(b)** Family of I-V Curves for BG-TD12

Figure 6.45: BG-TD2 and BG-TD12 show excellent I-V scaling characteristics as seen above for device areas from $2.5\times\ 10^{-9}$ cm^2 to $4\times\ 10^{-8}$ cm^2. Typical PVCR values for BG-TD12 are greater than those for BG-TD2, while J_P is lower. V_P also appears to be lower with the GaSb i-layer.

Examining I_P, I_V, and PVCR for BG-TD2 and BG-TD12 show excellent current scaling in Fig. 6.46, with the exception of the smallest devices. The leftmost data points are all from the 500 nm die, which must have been overexposed due to the current exceeding that of much larger mask defined devices. Generally, PVCR appears to increase as device sizes decrease for both samples until reaching the edges of the process control window. Fig. 6.47 shows that both BG-TD2 and BG-TD12 exhibit low V_P values near 0.2 V, though BG-TD12 appears to have a lower V_P floor than BG-TD2. It is possible that the change in i-layer to GaSb was enough to cause a slight shift in the electrostatics resulting in the lower V_P value.

Observing Fig. 6.48, it appears that changing i-layer material can result in J_P changes as much as 40%, going from 552 kA/cm^2 to 336 kA/cm^2. Conversely, observing Fig. 6.49 indicates a roughly 40% increase in PVCR when changing to GaSb, going from 2.31 to 3.49. Such a large difference was unexpected since the tunnel region is effectively the same for both samples. J_P, PVCR, and J_V findings for this



(a) I_P, I_V, and PVCR *vs.* area for BG-TD2 **(b)** I_P, I_V, and PVCR *vs.* area for BG-TD12

Figure 6.46: I_V and I_P *vs.* area for BG-TD2 and BG-TD12 show excellent scaling characteristics with area. Additionally, the influence of GaSb as an i-layer can be seen above.

section are summarized in Table 6.5. One additional growth integrating an i-layer with both InAs and GaSb could provide interesting results.

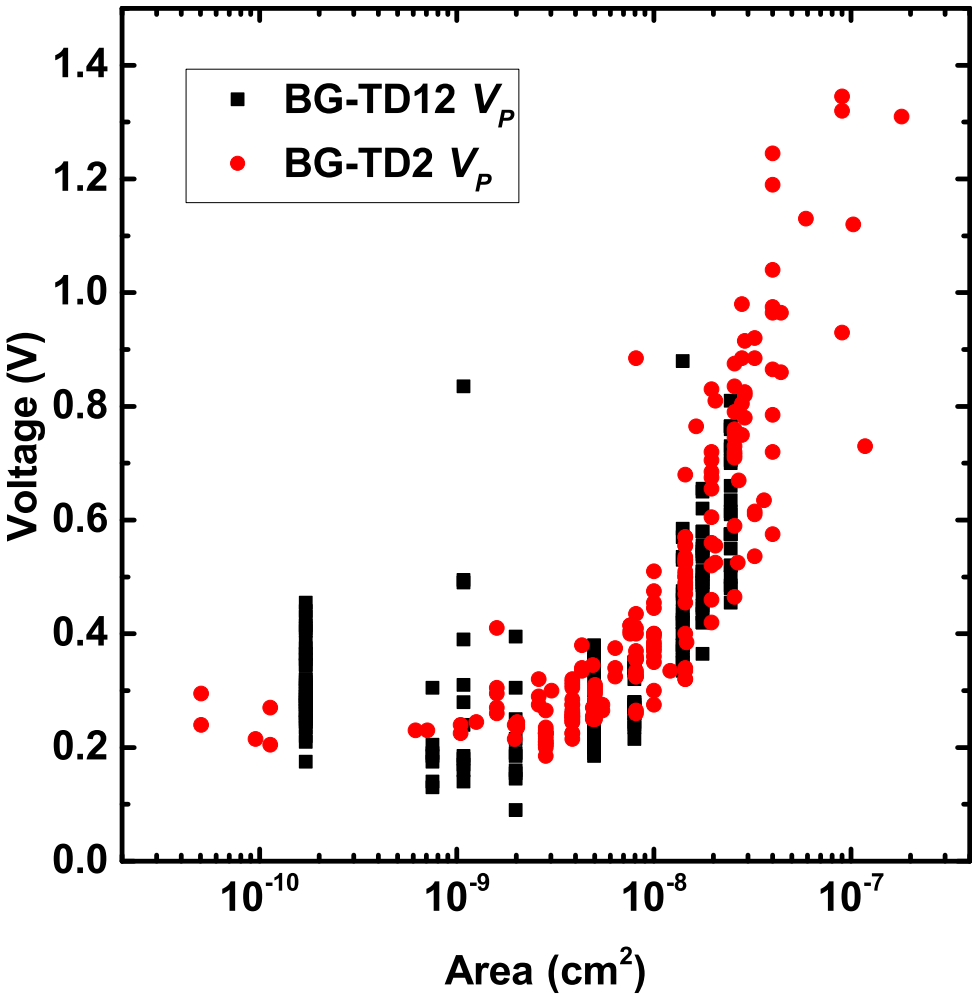


Figure 6.47: Typical minimum V_P values for the series 2 i-layer devices appear to fall between 0.3 V and 0.2 V, indicating minimal influence from R_S.

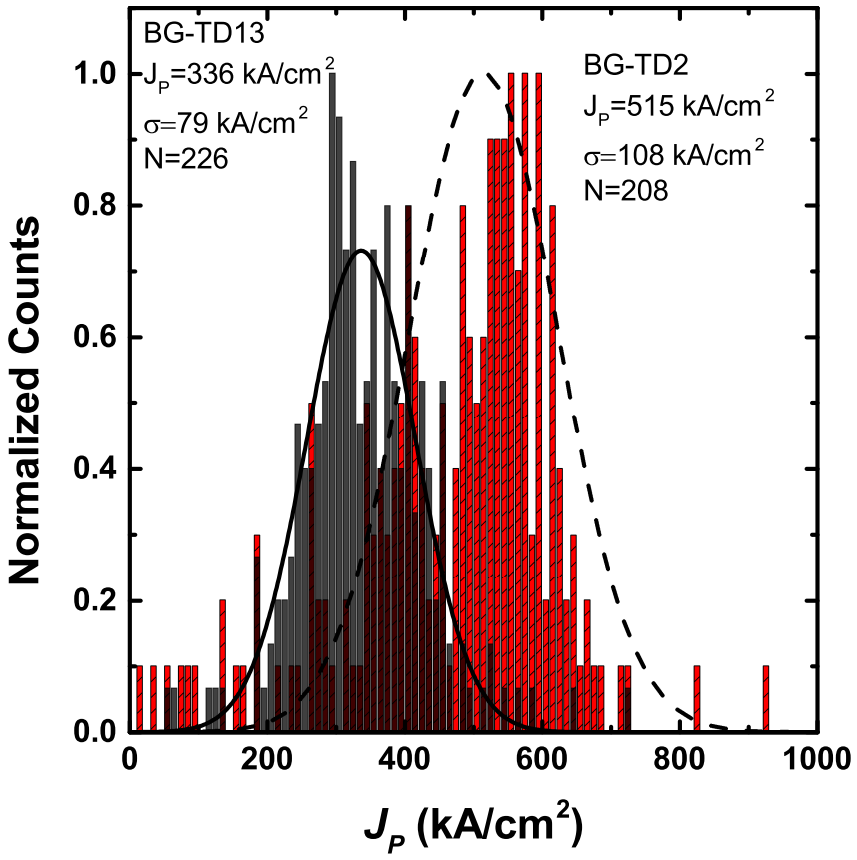


Figure 6.48: Normalized J_P histograms for BG i-layer series 2 study showing the effect of InAs and GaSb i-layer content on J_P. Such a large change in J_P was unexpected, as the devices are essentially the same for modeling purposes.

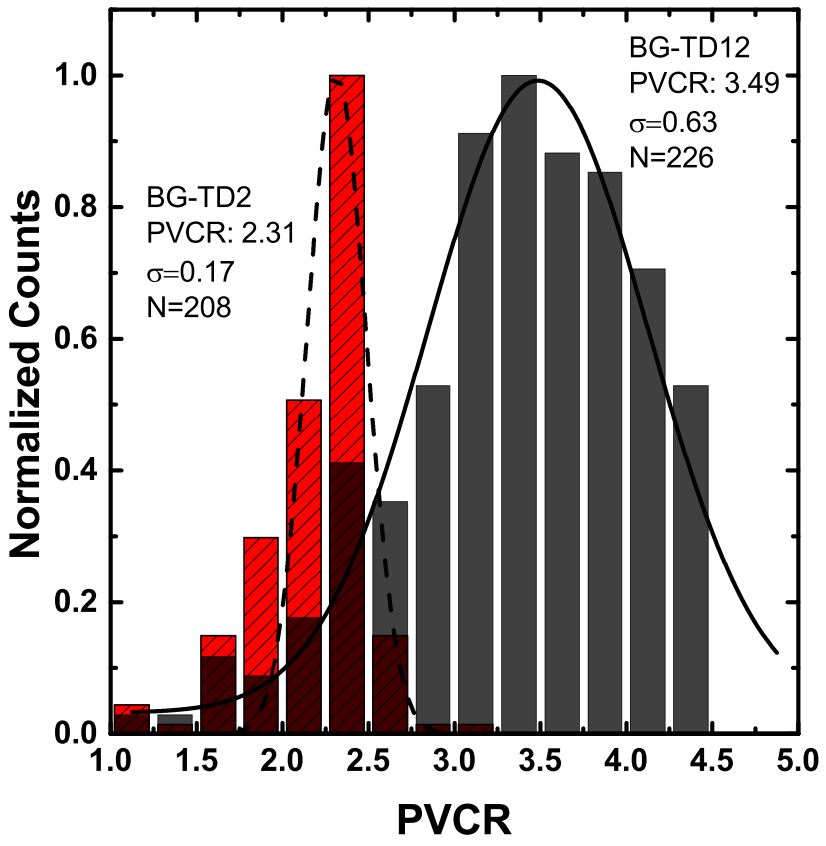


Figure 6.49: Normalized PVCR histograms for BG *i*-layer series 2 study showing the effect of InAs and GaSb *i*-layer content on PVCR. PVCR was expected to increase slightly, since the wider gap GaSb was expected to suppress excess current. However an increase of nearly 50% was much greater than anticipated.

6.8 Broken Gap Esaki Diode Conclusions

This chapter demonstrated the implementation of BG InAs/GaSb heterojunctions on GaSb substrates and compares their performance. Pushing doping density in BG-TD10 exhibited a max J_P near 3.2 MA/cm^2, well below 10 MA/cm^2 but not out of range. Results for the BG devices are summarized in Table 6.5

All samples in this chapter were designed to map changes in J_P and PVCR with respect to N^* with the goal of approaching a 10 MA/cm^2 J_P. Fig. 6.50 plots the change in J_P *vs.* N^* against prior reports and other material systems. Reaching 10 MA/cm^2 is a real possibility if maximum doping levels are tested for this system [47, 144].

Table 6.5: Broken Gap Tunnel Diode Summary

Device	p $\times 10^{19}$ (cm^{-3})	n $\times 10^{19}$ (cm^{-3})	N^* $\times 10^{19}$ (cm^{-3})	$N^{*-0.5}$ $\times 10^{-10}$ (cm^{-3})	J_P (kA/cm^2)		J_V (kA/cm^2)		PVCR		
					mean	σ	mean	σ	mean	max	σ
BG-TD1‡	2 Be	1 Si	0.67	3.87	2200	337	2200	139	1.48	3.95	0.19
BG-TD2‡	0.5 Be	1 Si	0.33	5.48	552	54	498	62	2.45	3.1	0.11
BG-TD3‡	0.3 Be	3 Si	0.27	6.06	212	12.3	136	28.8	1.71	1.83	0.06
BG-TD4‡	0.1 Be	1 Si	0.09	10.5	172	16.6	109	30.5	1.63	2.12	0.27
BG-TD5‡	0.15 Be	1.5 Si	0.75	3.65	160	82	20.7	1.03	2.08	2.54	0.25
BG-TD6‡	0.15 Be	1.5 Si	0.75	3.65	200	123	84	1.10	1.87	2.27	0.14
BG-TD7‡	x Be	x Si	0.68	3.83	2490	197	1173	428	1.9	3.41	0.06
BG-TD8‡	x Si	x Si	0.25	6.32	432	44.8	236	104	1.31	1.61	0.17
BG-TD9†	3 Be	1.5 Si	1	3.16	1860	175	726	214	2.62	3.49	0.33
BG-TD10†	3 Be	8 Si	2.14	10.5	3212	302	2867	532	1.18	2.24	0.05
BG-TD11†	3 Be	15 Si	2.5	2	-	-	-	-	-	-	-
BG-TD12†	0.5	1.0	0.33	5.48	336	79	117	44.7	3.43	4.47	0.63

‡<100> GaSb
†<100> GaSb 0.35° offcut to <111>

Over 2000 devices were tested between BG-TD1 through BG-TD12 samples. This volume of testing created a large dataset from which values of J_P, J_V, and PVCR were extracted and contrasted. This work demonstrates that broken gaps increase J_P for an equivalent doping density. Further enhancements to J_P will have to be made with larger broken gaps or higher doping. The remaining chapters will investigate the performance of III-V Esaki diodes that have been integrated onto a Si platform to demonstrate the viability of III-V devices integrated on Si in general, and III-V

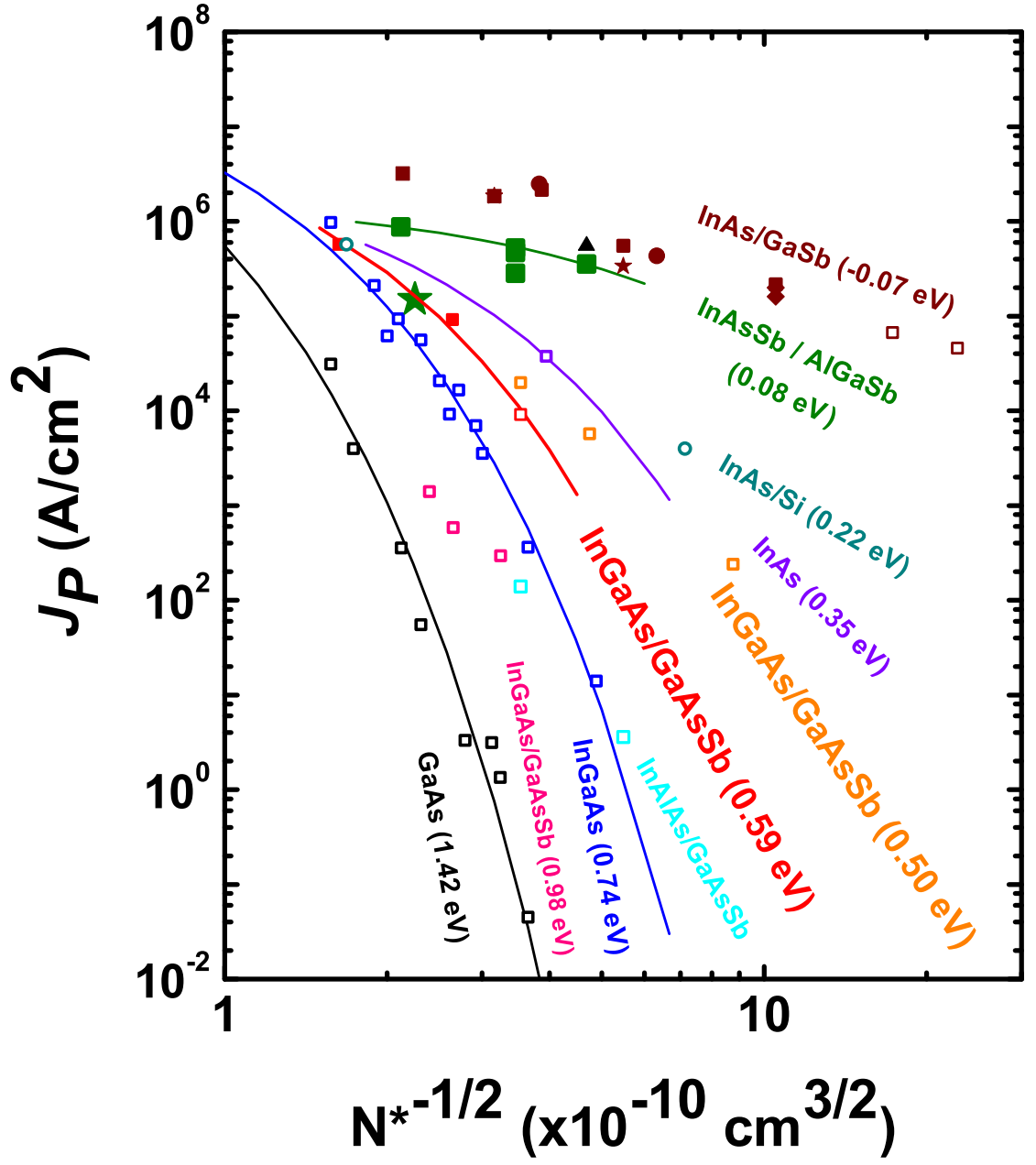


Figure 6.50: Figure of merit plot with data from all BG samples in this dissertation overlayed with other reported tunnel diodes.

tunnel devices integrated on Si in particular.

Chapter 7

Homojunction III-V Esaki Diodes on Si Substrates

7.1 Introduction

[1] Tunneling devices are of renewed interest due to increased research of tunneling field effect transistors (TFETs), a potential low power CMOS replacement technology. Prior work by the authors [28, 126] has investigated the application of Esaki diode properties to improve TFET design. Most reports around the $In_{0.53}Ga_{0.47}As$ tunnel devices focused on applications related to bipolar junction transistors (BJTs) [64–66, 155] and photovoltaics (PVs) [63, 156, 157] and were typically grown by Molecular Beam Epitaxy (MBE) on lattice matched InP substrates. Often, these devices are over 20 μm in diameter, designed to maximize peak current density (J_P), and only present a few representative devices. As such, it can be difficult to predict the performance range for a group of parallel processed tunnel diodes.

Concurrent to the investigation of low power devices, III-V on Si platforms are widely reported for $In_{0.53}Ga_{0.47}As$ on Si transistors as demonstrated by Lau et al. [12] and Hill et al. [120]. While there are reports of $In_{0.53}Ga_{0.47}As$ and other material systems grown on a GaAs substrate, to the author's knowledge, very few reports

[1] Significant portions of sections 7.1,7.2, and 7.3 have been reprinted with permission from P. Thomas, M. Filmer, A. Gaur, E. Marini, D. Pawlik, B. Romanczyk, S. L. Rommel, K. Majumdar, W. Loh, M. Wong, C. Hobbs, K. Bhatnagar, R. Contreras-Guerrero, and R. Droopad, "Performance Evaluation of $In_{0.53}Ga_{0.47}As$ Esaki Tunnel Diodes on Silicon and InP substrates," *IEEE – Transactions on Electron Devices*,

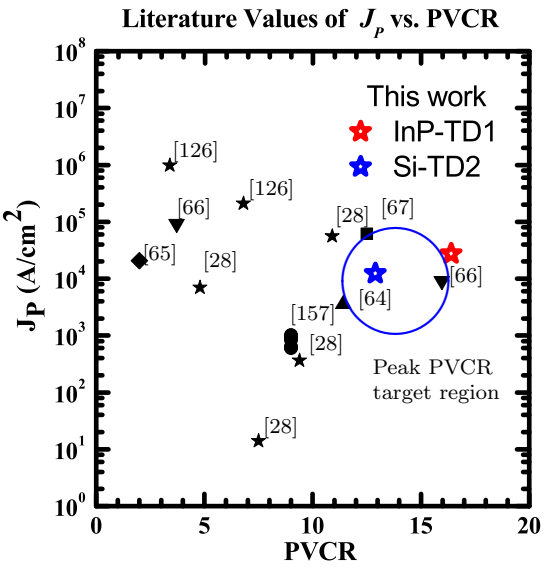
exist on the integration of $In_{0.53}Ga_{0.47}As$ tunnel diodes on a Si substrate. Low In% content InGaAs Esaki tunnel diodes have been integrated on virtual Ge aspect ratio trapping (ART) substrates [43], but other reports of III-V on Si Esaki diodes are quite rare [156–158]. This work provides an extensive set of data directly comparing an $In_{0.53}Ga_{0.47}As$ control to one heterointegrated on a Si substrate.

Prior studies have pushed to maximize J_P [28, 64–67, 126, 157], which is relatively robust with regard defect assisted current mechanisms. However, valley current density (J_V) is sensitive to defect density [68], and can vary widely between devices. Therefore to compare performance across different substrates the peak to valley current ratio (PVCR) is a more appropriate metric as it captures both characteristics. Per Fig. 7.1(a), the maximum PVCR correlates to a mid range J_P between 10 and 90 kA/cm^2, and device doping levels in this study were targeted accordingly. Thus, utilizing changes in J_V due to heterointegration on Si, this work measures relative performance of $In_{0.53}Ga_{0.47}As$ on Si to a control sample on InP and shows that, below 8.7×10^{-10} cm^2, PVCR for both systems can be considered equivalent.

7.2 Experimental Procedure

Tunnel diodes for this experiment were designed to maximize PVCR to highlight differences due to epitaxy on different substrates. Devices were designed to maximize PVCR, which, for $In_{0.53}Ga_{0.47}As$, appears between 3.5 kA/cm^2 and 62 kA/cm^2 per literature values in Fig. 7.1(a).[64, 66, 67] Doping levels for the devices were determined using prior experimental and modeling work to map J_P for $In_{0.53}Ga_{0.47}As$ systems [28, 62]. An effective doping, N^*, value near 1.5×10^{19} cm^{-3}($\approx 3 \times 10^{19}$ cm^{-3} of both n and p dopants) was selected, which would target a J_P of 30 kA/cm^2. Where N^* is defined by Eq (7.1):

$$N^* = \frac{N_D N_A}{N_D + N_A} \tag{7.1}$$



(a) Figure of Merit Plot (FOM)

60 nm	$In_{0.53}Ga_{0.47}As$: Si	3×10^{19} cm^{-3}
3 nm	$In_{0.53}Ga_{0.47}As$	uid
300 nm	$In_{0.53}Ga_{0.47}As$: Be	3×10^{19} cm^{-3}
Substrate	InP	

(b) InP-TD1

60 nm	$In_{0.53}Ga_{0.47}As$: Si	3×10^{19} cm^{-3}
3 nm	$In_{0.53}Ga_{0.47}As$	uid
300 nm	$In_{0.53}Ga_{0.47}As$: Be	3×10^{19} cm^{-3}
200 nm	$In_{0.52}Al_{0.48}As$	uid
1000 nm	InAlAs buffer	uid
500 nm	GaAs	uid
100 nm	Low Temp GaAs	uid
Substrate	Si	

(c) Si-TD2

Figure 7.1: (b) Schematic of the film stacks for samples InP-TD1 and Si-TD2. Doping levels are targeted around an N^* value of 1.5×10^{19} cm^{-3} dopants which allows for the highest PVCR for a given diode J_P. (a) Figure of merit (FOM) plot comparing published values of J_P against the PVCR reported or extracted for the $In_{0.53}Ga_{0.47}As$ system. This study targets J_P values near 30 kA/cm^2(circled),within range of the maximum PVCR values expected for $In_{0.53}Ga_{0.47}As$ devices. High defect density samples reduce PVCR through an increase in the measured J_V values.

In this regime, PVCR is generally high and the impact of growth defects between the two samples should be pronounced. J_P may see a slight increase due to excess current, but the sample is not expected to respond strongly to an increased defect density. However J_V and PVCR are expected to show a strong response with defect density, as this region is dominated by excess current. High defect densities create additional current paths, which will cause increased J_V with respect to a sample with lower defect density. [64–68, 126]

The samples in this study were grown by molecular beam epitaxy atop either $p+$ (001) InP or 4° to <110> miscut (001) Si substrates. Figs. 7.1(b) and 7.1(c) illustrate the schematic diagram of the device layers, which consists of 300 nm of $p+$ $In_{0.53}Ga_{0.47}As$:Be (2.4×10^{19} cm^{-3}), a 3 nm thick unintentionally doped region

(uid) $In_{0.53}Ga_{0.47}As$ layer, and a 60 nm n+ $In_{0.53}Ga_{0.47}As$:Si (2.4×10^{19} cm^{-3}). The growths on Si substrates include buffer layers that consists of GaAs, graded InAlAs, and $In_{0.52}Al_{0.48}As$ to achieve the lattice constant of InP. All growths were carried out in a DCA solid source molecular beam epitaxy (MBE) system using elemental Ga and In in standard effusion cells and As valved cracker sources set to produce dimeric species. Si and Be were used as n-and p-type dopants, respectively, which were calibrated using electrochemical C-V and Hall measurements. Epiready substrates were mounted in In-free holders and introduced into the growth chamber after an initial outgas in the load lock at 150°C. Growth rates and alloy compositions were calibrated using the RHEED oscillation technique and measured using x-ray diffraction. The substrate temperature used for $In_{0.53}Ga_{0.47}As$ active region growth on InP was 490°C as determined using an optical pyrometer. For growth on the Si substrate, a metamorphic buffer [120] is used to reduce defect density in the top $In_{0.53}Ga_{0.47}As$ active layers. This is achieved by using various layers to grade the lattice constant along the growth direction allowing lattice matched growth of the top active layers. The metamorphic buffer also helps to relieve the lattice mismatch generated strain through defect formation and defect filtering [159, 160].

High resolution x-ray diffraction (HRXRD) measurements were performed on a Bruker 8 system to confirm the film stack and to qualitatively measure differences in film quality. A relation exists between full width half maximum (FWHM) and threading dislocation defect density (TDD) for GaAs and GaAs on Si films [118]. In principle, a similar relationship should apply for an $In_{0.53}Ga_{0.47}As$ on InP (control) and $In_{0.53}Ga_{0.47}As$ on Si and would appear as differing peak widths. In addition to XRD, atomic force microscopy (AFM) was utilized to measure the surfaces of InP-TD1 and Si-TD2, as surface roughness can have a large impact on electrical characteristics.

Accurate J_P determination requires known doping levels within the device. Secondary ion mass spectroscopy (SIMS) was performed to determine n and p doping

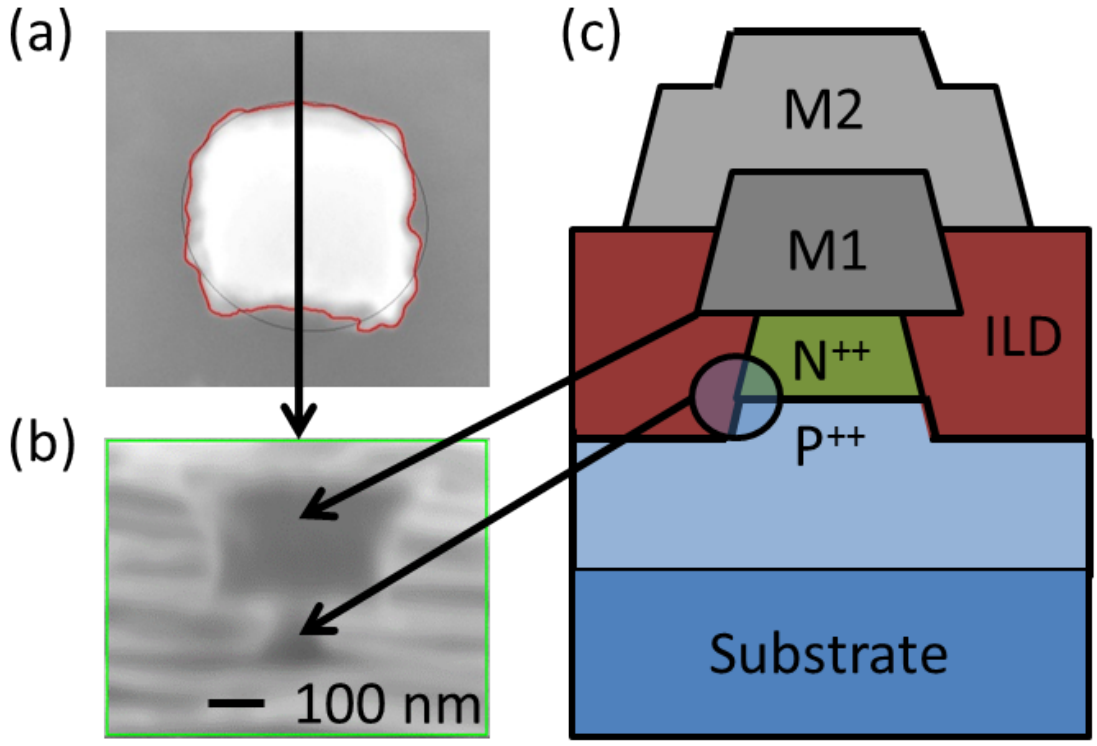


Figure 7.2: (a) Device areas are taken across several die to attain a representative contact area to increase the precision of the J_P and J_V data. (b) The sample is then rotated to a steep angle, often 84°, or higher, to measure the undercut in two perpendicular planes to account for etch anisotropy. (c) To prevent the probe from shorting the contact to the mesa wall, a second level metal and ILD must be used with these mesas to contact devices below 2 μm widths.

densities within the sample. Carrier levels measured by SIMS in this study should be sufficiently below solubility limits and are assumed fully active. Additionally, the two samples were fabricated concurrently to ensure the greatest precision between measurements.

Device fabrication generally follows the approach used in prior work [27–29, 68]. First, the sample surfaces are cleaned in a 10:1 H_2O:HCl solution for 10 s. Then, a 200 nm thick layer of Mo is sputtered onto the sample. nLOF, diluted in PGMEA (≈1:1) [138], and e-beam lithography in a Nabity driven LEO EVO 50 SEM define the mesa and ground contacts. SF_6-based reactive ion etching (RIE) removes the exposed

Mo and leaves devices ranging from 1×10^{-2} μm^2 to 4×10^{2} μm^2 mask defined areas. A brief O_2 surface clean is used to remove residual photoresist. A 20:1 citric acid: hydrogen peroxide solution etches the sample for 75 s to form Esaki diode mesas. Following mesa etch, contact area and undercut are measured by SEM for each size on several die to give a mean device area per Figs. 7.2(a) and 7.2(b). Variability for J_P and J_V values originate from differences in device area from the mean. Bis-benzocyclobutane (BCB) is used as an inter layer dielectric (ILD) and planarization layer as detailed by Pawlik et al. [29]. Level 2 contacts are then defined by e-beam lithography and a lift-off process producing devices depicted in Fig. 7.2(c) so devices as small as 1×10^{-2} μm^2 can be manually probed.

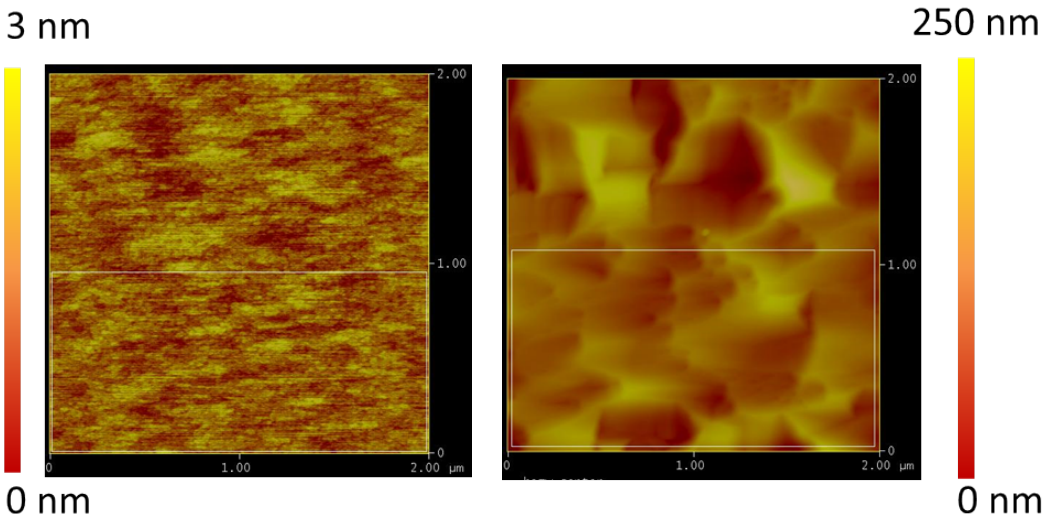
Current-voltage characteristics (I-V) are obtained via a Keithley 4200 Semiconductor Parameter Analyzer. As in the work by Pawlik et al. [28, 29], a large area Esaki diode ($> 1000\times$ the measured junction area) is used as a virtual ground. The ground plane was designed to fully surround the devices to minimize any effect from current crowding; this is critical for measuring high current tunnel junctions as it minimizes unwanted resistive-based latching that obscures the negative differential resistance. To ensure an accurate statistical set, data was collected from over 1000 devices on InP-TD1 and Si-TD2. PVCR, J_P, and J_V were extracted and corrected based on the aforementioned area analysis. Statistical values were then extracted from the sample set to determine the J_P for the device.

7.3 Results

Device yield for both the control and the III-V on Si sample was high without any notable differences between samples. Device sizes varied from mask definition across die and between die by more than 5%, which will likely increase the variability of the J_V and J_P extracted values. Most of the data presented represents mask defined areas ranging from 0.25 μm^2 to 400 μm^2. Electrical measurements determined that InP-

TD1 exhibited higher J_P and PVCR characteristics than Si-TD2, a finding similar to those of Freundlich *et al.* [157].

7.3.1 III-V on Si Materials Analysis



(a) Control sample **(b)** III-V on Si

Figure 7.3: AFM measurements were taken from both InP-TD1 and Si-TD2. (a) InP-TD1 provided an expected smooth surface with RMS of 0.24 nm over the 4 μm^2 area. (b) Si-TD2 had regions of varying haziness, so roughness values were expected to vary across the surface, and a RMS of 14.8 was measured over the haziest region.

AFM measurements revealed a substantially rougher surface for Si-TD2 relative to InP-TD1. InP-TD1, shown in Fig. 7.3(a), has a root mean sqaure (RMS) of 0.24 nm. Measurements on Si-TD2 revealed wide surface variation. RMS values ranging from 8.2 nm to 14.5 nm, per Fig. 7.3(b), corresponded to the observed haziness of the sampled regions. RMS roughness values have been shown to correlate well with threading dislocation density (TDD) [136, 161], which will cause increased J_V [68] for Si-TD2. Additionally, surface roughness affects sample processing, *e.g.* irregular mesa etch patterns and metal flakes that can short to the side of the mesa. These manifest electrically as lower PVCR (short related) and J_P (area related) measurements. As

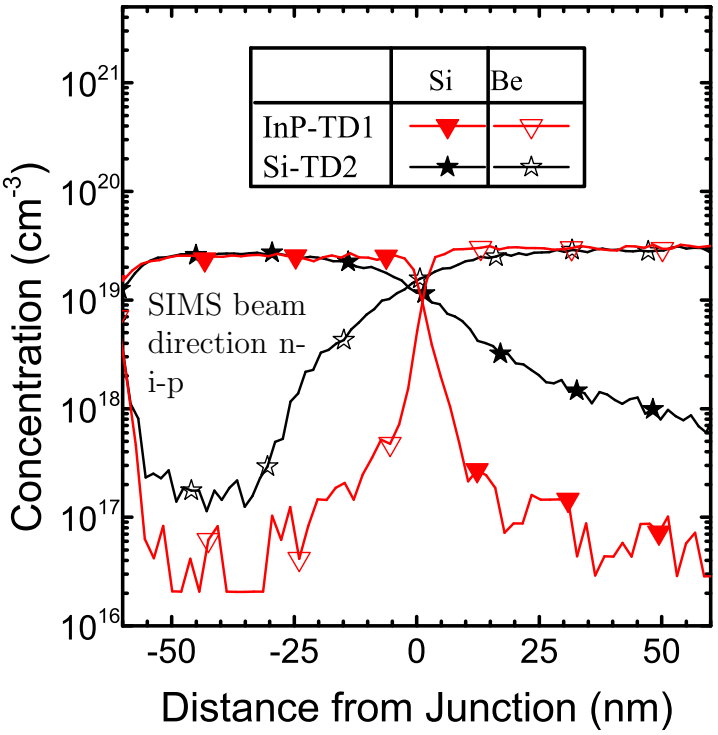


Figure 7.4: InP-TD1 and Si-TD2 appear to have similar doping levels. The broader slope of dopants for Si-TD2 are, presumptively, related to knock-on effects due to the roughness of the sample

such, the author's expect Si-TD2 to exhibit greater variability from device to device.

SIMS analysis revealed that total doping between samples was roughly equivalent, but would seem to reveal some differences in the doping profile. Fig. 7.4 shows that doping levels were nearly equivalent for both devices on either side of the junction. Si-TD2 appeared to have a broad junction profile; however, due to the surface roughness, the authors believe that knock on effects and the measurement angle caused the relaxed dopant concentration profiles. However, if the junction profile is truly more broad for Si-TD2 the authors would expect a reduced J_P due to the lower electric field between the n and p regions. Peak dopant values indicated concentrations of 2.5×10^{19} cm^{-3}, Be, and 3.0×10^{19} cm^{-3}, Si, for InP-TD1, and 2.4×10^{19} cm^{-3}, Be, and 3.0×10^{19}

cm^{-3}, Si, for Si-TD2. N^* was calculated to be 1.36×10^{19} cm^{-3} and 1.30×10^{19} cm^{-3} for InP-TD1 and Si-TD2, respectively. As such, Si-TD2 was expected to exhibit similar, but lower, J_P to InP-TD1.

HRXRD scans in Fig. 7.5 exhibit excellent crystallinity for InP-TD1, and the possibility of some relaxation in Si-TD2 per the broader $In_{0.53}Ga_{0.47}As$ peak. Total threading dislocation density was reported to be $\approx7.6\times10^{9}$ cm^{-2} for Si-TD2 [68], corresponding to higher defect assisted tunneling. Relaxation in the $In_{0.53}Ga_{0.47}As$ for Si-TD2 increases J_V due to higher defect assisted tunneling contributing to the total excess current. Mean PVCR values for Si-TD2 should approach that of InP-TD1 as device area is reduced and fewer defects contribute to the total excess current.

7.3.2 III-V on Si Electrical Results

Over 1000 diodes have been measured per sample to build a good statistical dataset for extracting J_P and J_V. Fig. 7.6 and Fig. 7.7 present select I-V characteristics for diodes on Si-TD2 ranging from 0.25 μm^2 to 100 μm^2 areas as mask defined. Negative differential resistance (NDR) was clearly present at room temperature, and the oscillations seen in the curves are a common artifact of the measuring equipment commonly seen in other reports [27, 28, 43, 66]. The extent to which the samples have been tested can be seen in Fig. 7.8 and Fig. 7.9, from which a few trends can be observed. First, devices tested on InP-TD1 exhibit less variation than those on Si-TD2, which indicates that fewer defects are present. Second, electrical data for both samples shows excellent scaling with area. Any surface or other leakage paths do not appear to affect J_V as devices are scaled down, as neither system appears to show a change in slope with smaller device areas. Third, InP-TD1 generally exhibits a higher PVCR than Si-TD2 as seen in Fig. 7.10. InP-TD1 typically has a higher PVCR around 10.6, whereas Si-TD2 is generally somewhere near 8.6 for PVCR, a result similar to those of Freundlich et al. [157] and consistent with the modeling work

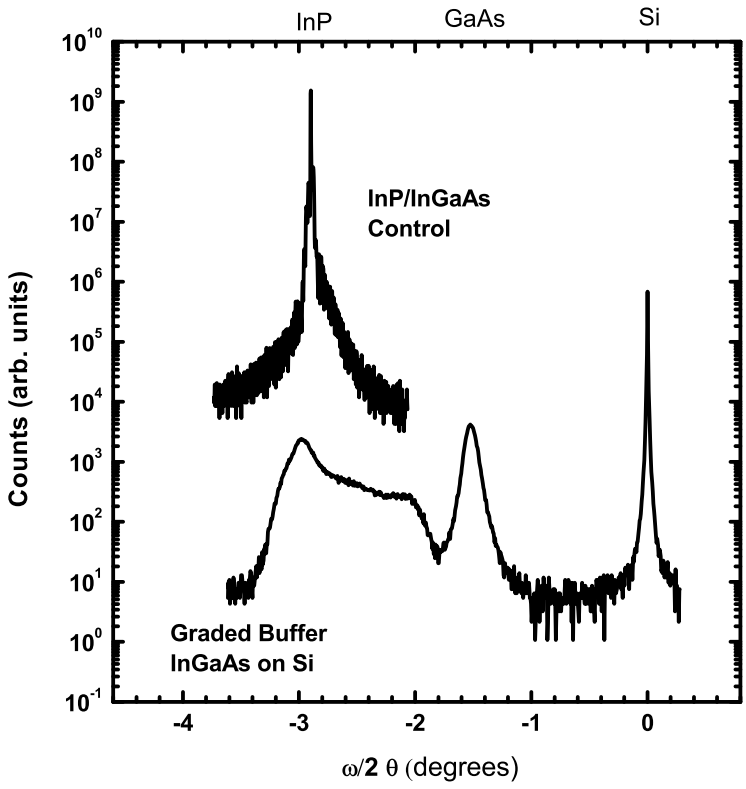


Figure 7.5: $\omega/2\theta$ scan of InP-TD1 and Si-TD2, comparing the difference in peaks. Si-TD2 exhibits a broader $In_{0.53}Ga_{0.47}As$ peak, indicating the existence of a higher defect density in the film.

by Majumdar et al. [68]. Interestingly, devices with mesa areas below 3×10^{-9} cm^2 begin to show an increased overlap of the PVCR range. This may be due to devices approaching a critical size under which defects play a diminished role in J_V.

The authors surmise that the origins of the differences in J_P between the samples may be related to a few possibilities. First, the junction profile for Si-TD2 may be broader than InP-TD1 , but the SIMS data is inconclusive due to the surface topology. However, a shallower dopant profile effectively increases the tunnel barrier thereby reducing current density for, otherwise, equivalent diodes. Second, a combination of surface topology and the amphoteric nature of Si [152] may create an environment

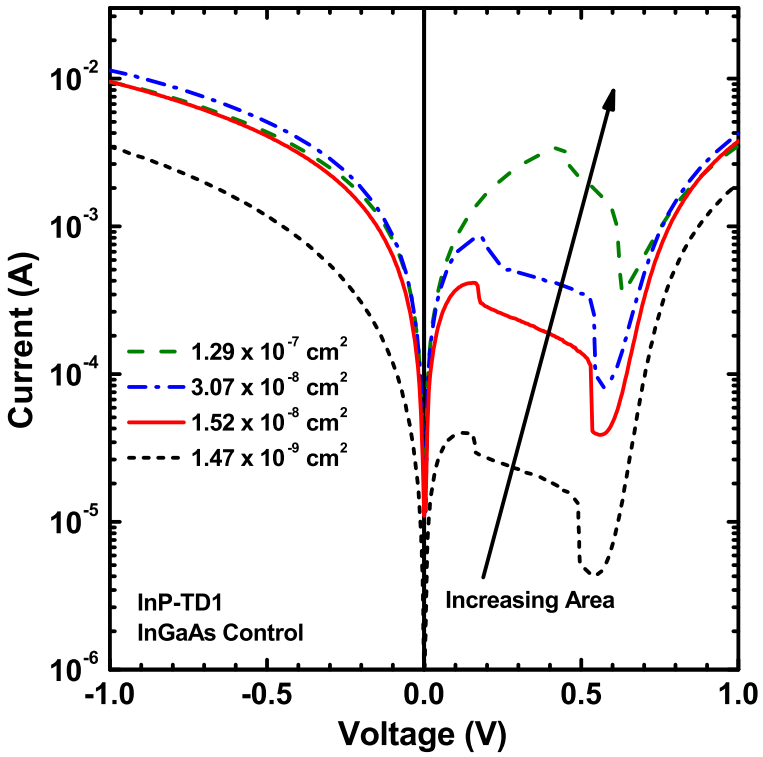


Figure 7.6: Representative *I-V* characteristics for InP-TD1 device areas ranging from 0.25 μm^2 to 100 μm^2. NDR was present at room temperature, indicating the presence of good tunnel junctions.

with lower effective n-type doping due to counterdoping. Third, due to the different thermal properties of Si and InP, it may be possible that dopants diffused or incorporated differently between the samples. Generally, lower doping or broader dopant profiles would create differences in J_P without adversely affecting the PVCR.

A Gaussian fit to the data was made following exhaustive electrical testing, roughly 1000 per sample, and area analysis. The extracted means for InP-TD1 and Si-TD2 PVCR are 10.6 and 8.6. Maximum PVCR of 16.4 and 12.9 for the samples are amongst the highest reported in the $In_{0.53}Ga_{0.47}As$ system [66, 67]. InP-TD1 and Si-TD2 were determined to exhibit J_P values of 27.2 kA/cm^2 and 12.2 kA/cm^2, respectively. Extracted J_V values were found to be 2.6 kA/cm^2 and 1.5 kA/cm^2,

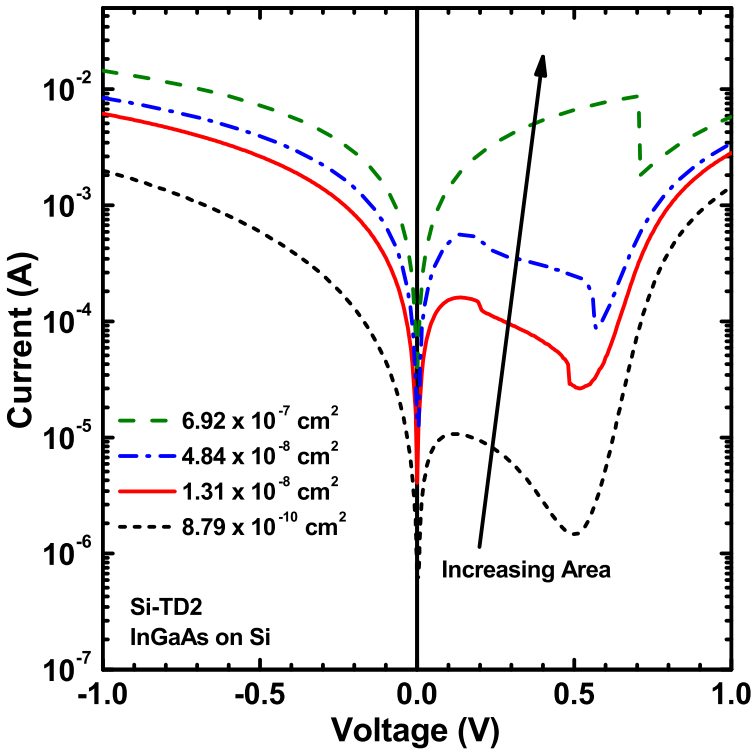


Figure 7.7: Representative *I-V* characteristics for Si-TD2 device areas ranging from 0.25 μm^2 to 100 μm^2. NDR was present at room temperature, indicating the presence of good tunnel junctions.

for InP-TD1 and Si-TD2. As expected, Si-TD2 (the III-V on Si), exhibited greater variability between devices. However, it is important to note that InP-TD1 and Si-TD2 PVCR means and range show significant overlap at reduced areas per Fig. 7.10. Following procedures for performing a t-test [162], devices below 8.7 $\times$ 10^{-10} cm^2 exhibit the same PVCR with a 1% risk of being different. Results from both devices are summarized in Table 7.1. Due to the interest in integrating non-native crystals on Si, this is an important data point proving that certain applications may see acceptable performance despite the defect density.

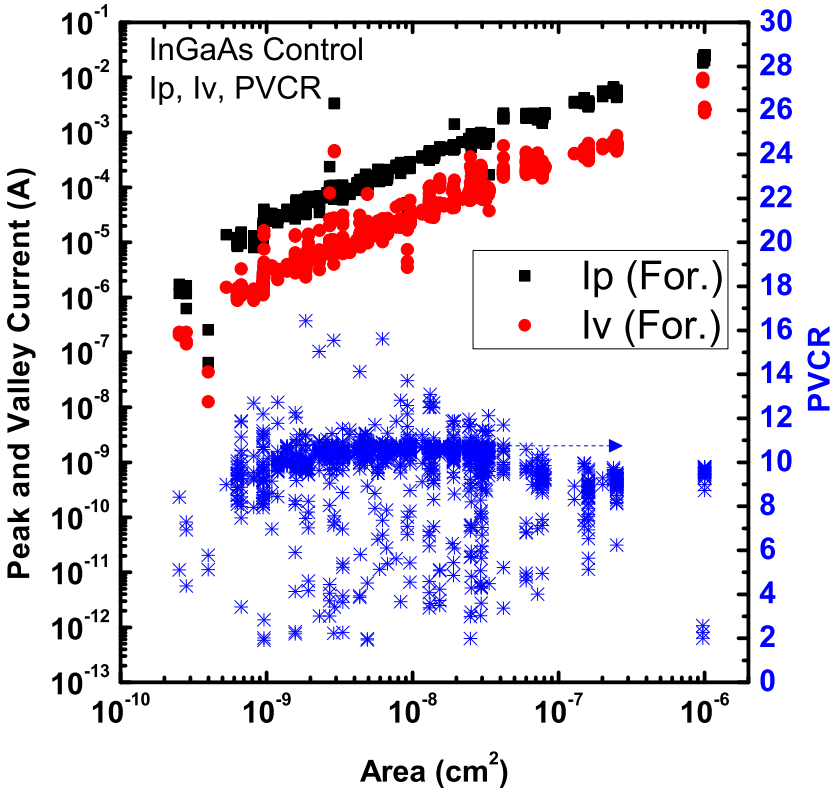


Figure 7.8: J_V, J_P, and PVCR values for InP-TD1 are plotted against device area. Current scales with area and 10.6 is the approximate value of PVCR. Low PVCR values indicate a rise in J_V which are associated with defects and yield issues.

Table 7.1: Summary of device information and extracted values

Device	p $\times 10^{19}$ (cm^{-3})	n $\times 10^{19}$ (cm^{-3})	N^* $\times 10^{19}$ (cm^{-3})	$N^{*-0.5}$ $\times 10^{-10}$ (cm^{-3})	J_P (kA/cm^2) mean	σ	J_V (kA/cm^2) mean	σ	PVCR mean	max	σ
InP-TD1†	2.45 Be	3.0 Si	1.35	2.72	27.2	3.3	2.6	0.3	10.6	16.4	0.16
Si-TD2‡	2.34 Be	3.0 Si	1.31	2.76	12.2	2.7	1.5	0.45	8.6	12.9	0.64

† InP
† <100> miscut 4° to <110>

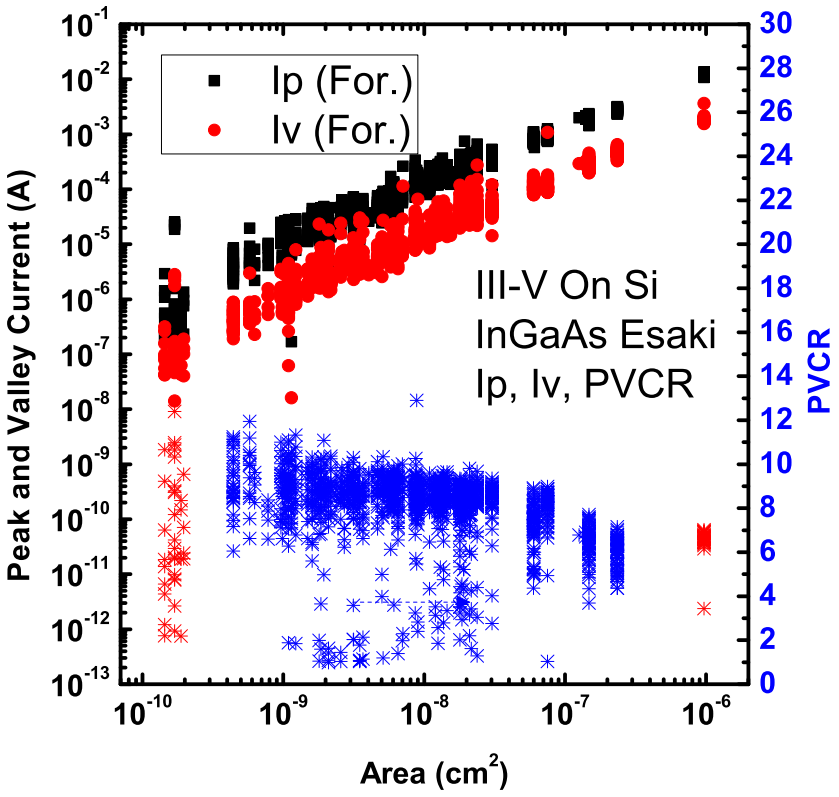


Figure 7.9: J_V, J_P, and PVCR values for Si-TD2 are plotted against device area. Generally, there is a wider spread in the data with respect to InP-TD1. A PVCR around 8.6 exhibits greater variability due to a greater defect density leading to higher J_V values.

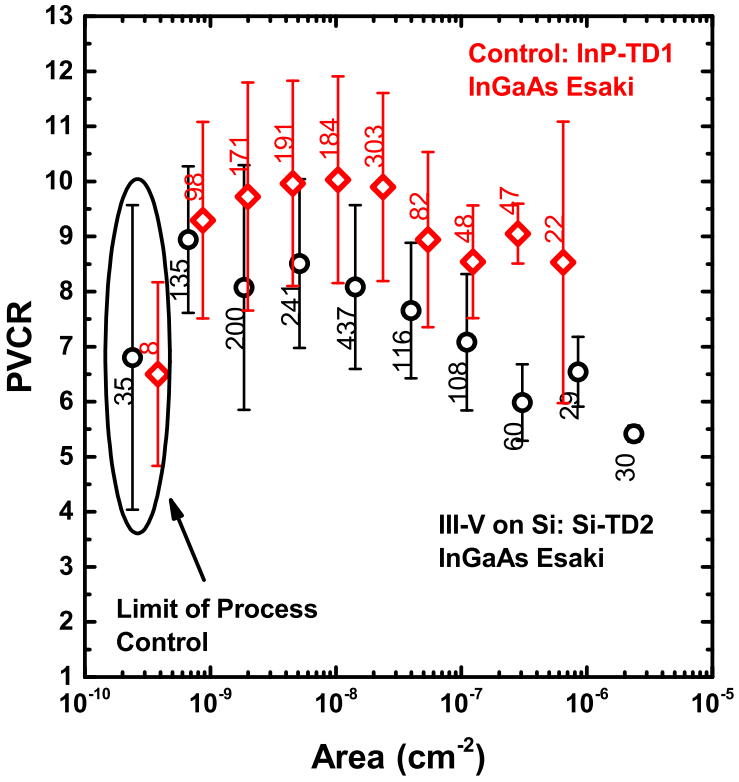
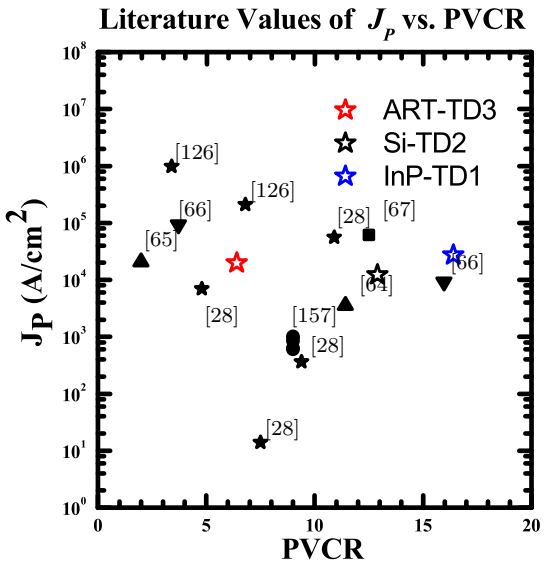


Figure 7.10: Devices are sorted by area and display the mean, range, and population. Using the nearest neighbor area to compare between InP-TD1 and Si-TD2 it can be seen that sample variation overlaps and that the means begin to converge. Below 8.7 $\times 10^{-10}$ cm^2, t-tests confirm that there is at most 1% error in assuming equivalent PVCR.

7.4 $In_{0.53}Ga_{0.47}As$ on Aspect Ratio Trapping substrates

60 nm	$In_{0.53}Ga_{0.47}As$: Si	3×10^{19} cm^{-3}
3 nm	$In_{0.53}Ga_{0.47}As$	uid
300 nm	$In_{0.53}Ga_{0.47}As$: Be	3×10^{19} cm^{-3}
	Coalesced InP	uid
	InP ART	uid
Substrate	Si	

(a) ART-TD3



(b) Figure of Merit Plot (FOM)

Figure 7.11: (a) Schematic of the film stack ART-TD3. Doping levels are targeted around an N^* value of 1.5×10^{19} cm^{-3} dopants which allows for the highest PVCR for a given diode J_P. (b) Figure of merit (FOM) plot comparing published values of J_P against the PVCR reported or extracted for the $In_{0.53}Ga_{0.47}As$ system. This study targets J_P values near 30 kA/cm^2, within range of the maximum PVCR values expected for $In_{0.53}Ga_{0.47}As$ devices. High defect density samples reduce PVCR through an increase in the measured J_V values.

One growth was performed on a non-epitaxy ready surface of a sample of InP ART. This sample was grown in the same reactor as the InP control, and was targeted to have the same levels of doping. The resultant epitaxy was not optimal, however some devices did show NDR.

Upon visual inspection, the sample surface was very hazy, even more so, than the $In_{0.53}Ga_{0.47}As$ on Si sample. Normally, devices grown on an ART surface would be expected to exhibit far better material and electrical characteristics [43, 124], however that was not the case. The double grooved trenches in Fig. 7.12 gives some explanation as to why. ART should exhibit a single V-groove interface between the Si substrate and the III-V, the double groove indicates an incomplete groove etch due

Figure 7.12: Sample ART-TD3 was cleaved to view the seed location in each trench. Normal samples should show a single V-groove due to the selective Si etch, these samples have a double groove indicating an incomplete groove etch which likely contributed to the epitaxy issues for the sample.

to oxide masking the Si which is used in Germanium on Nothing processing, GON [163, 164]. The abnormal trench lead to abnormal growth conditions for the InP, which affected the coalesced InP and $In_{0.53}Ga_{0.47}As$ that had been grown on top.

AFM measurements of the ART-TD3 surface revealed a surface roughness RMS value of 25.7 nm, high quality epitaxy on optimal conditions is often under 1 nm. 25.7 nm corresponds to step heights of over 250 nm. Considering the device on the film stack is approximately 63 nm tall and variation across the surface can be as much as 3× the device height. Such variability across the surface will make device processing difficult and area characterization near impossible, a significantly reduced yield is to be expected for this sample.

Electrical characterization of over 800 devices was performed, however the rough

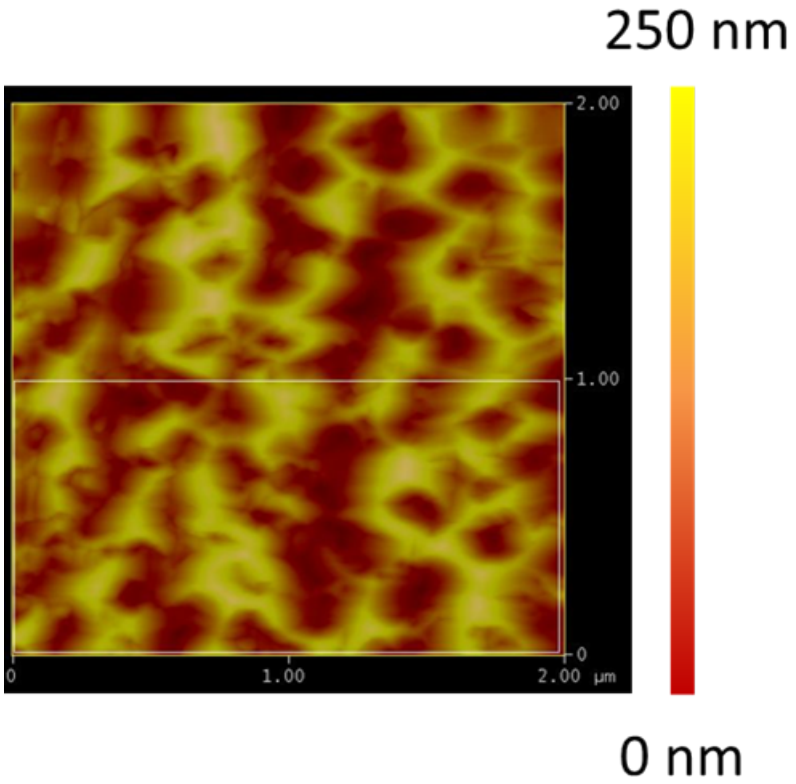


Figure 7.13: AFM of Si-TD3 showing an exceedingly rough surface with RMS values of 25.7 nm. This sample was not on an epi-ready ART wafer, as such, this roughness should not be considered typical for future samples that may be grown on ART, considering that lasers have been built using this technology [43, 45, 124].

nature of the sample surface limited the number of viable diodes to 134. Many devices yielded low PVCR values and J_P with respect to their control sample counterparts, though some were as high as 6.7. Fig. 7.14 exhibits the typical I-V characteristics for $In_{0.53}Ga_{0.47}As$ devices on the ART substrate. Reduction in PVCR appears consistent with the effects of defect density presented by Majumdar et al. [68].

Extracted values for J_P appear to have a bimodal distribution of 4.4 kA/cm^2 and 19.8 kA/cm^2, respectively, and are shown in Fig. 7.15. However, closer inspection of the data reveals that the distribution is largely dependent on area. Therefore, it is quite likely that the estimated area for the smallest devices is an overestimate and is artificially reducing the calculated J_P values. This discrepancy is due to the

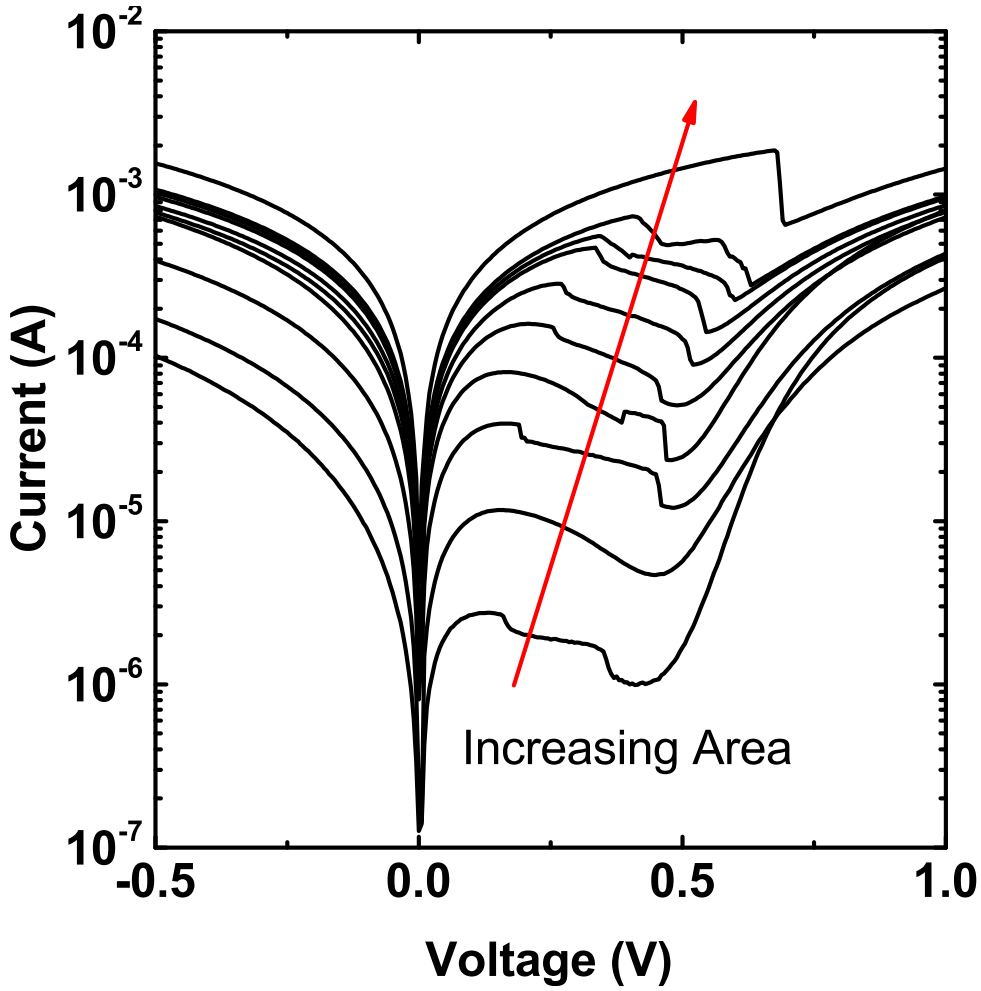
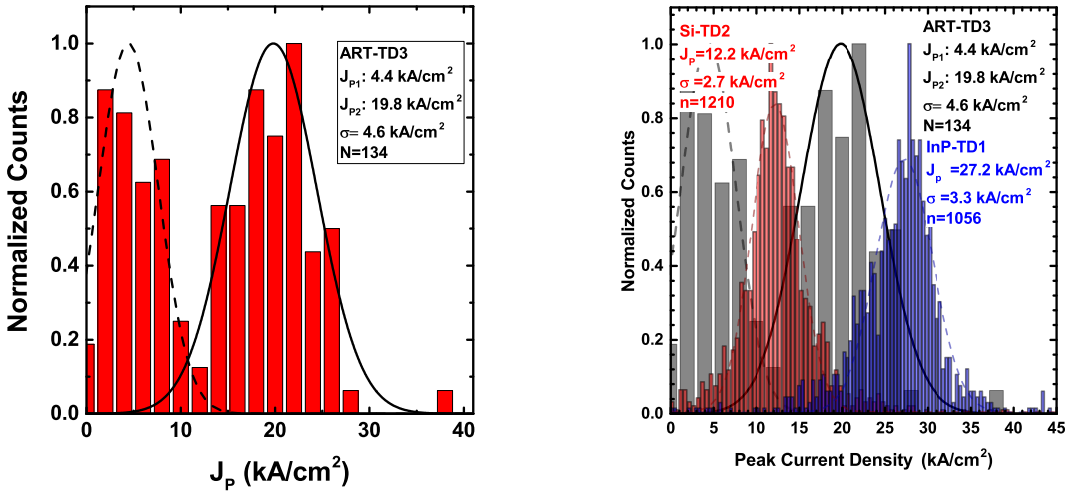


Figure 7.14: Sample ART-TD3 exhibits a reduced NDR region, this is very likely due to the roughness of sample surface. Because the sample is more rough than Si-TD2, it displays poorer PVCR characteristics which are commensurate with the level of defects within the film.

combination of surface morphology with mesa fabrication, leading to oddly shaped and smaller than designed device areas. Based on J_P, but without SIMS confirmation, it would appear that ART-TD3 has a doping density between InP-TD1 and Si-TD2. A N^* value of 1.33×10^{19} cm^{-3} was calculated for ART-TD3 based on empirical fit data derived from prior experiments [28, 62]. Variation in the doping level could be expected due to the MBE system not being calibrated for the combined thermal properties of an ART substrate. Confirmation of doping density by SIMS would likely be unsuccessful for ART-TD3. Significant variation across the surface would likely

lead to knock-on effects which would skew the dopant measurements. Additionally, the doping profiles would show lower slope than is present due to surface roughness leading to multiple surfaces being measured. The lower surface variability of Si-TD2 allowed for a good comparison between it and InP-TD1, but such a comparison would likely be futile in this case. PVCR extracted from Fig. 7.17 was shown to be 2.84,



(a) ART-TD3 J_P Histogram

(b) $In_{0.53}Ga_{0.47}As$ on Si J_P histograms

Figure 7.15: (a) A bimodal distribution of J_P caused by large area defects required a two peak extraction. (b)Histogram of J_P for ART-TD3, which shows the J_P value as compared to the control and buffer layer samples.

only a single peak is present because PVCR is independent of area. This finding is in line with those presented by Majumdar et al. [68], seeing as the PVCR decreased with increased defect density allowing greater excess current culminating in J_P values greater than both InP-TD1 and Si-TD2. The increased defect level has clearly affected the PVCR, as typical values are near 2.8 instead of 10 for the control sample.

Fig. 7.16 shows the performance of J_V for ART-TD3. Similar to the J_P values, there is a bimodal distribution due to the variety of device sizes. J_V was found to be $\approx$ 6.6 kA/cm^2 and $\approx$ 1.4 kA/cm^2. Devices with 1.4 kA/cm^2 are likely smaller than assumed, thus the actual J_V for ART-TD3 should be considered 6.6 kA/cm^2. When

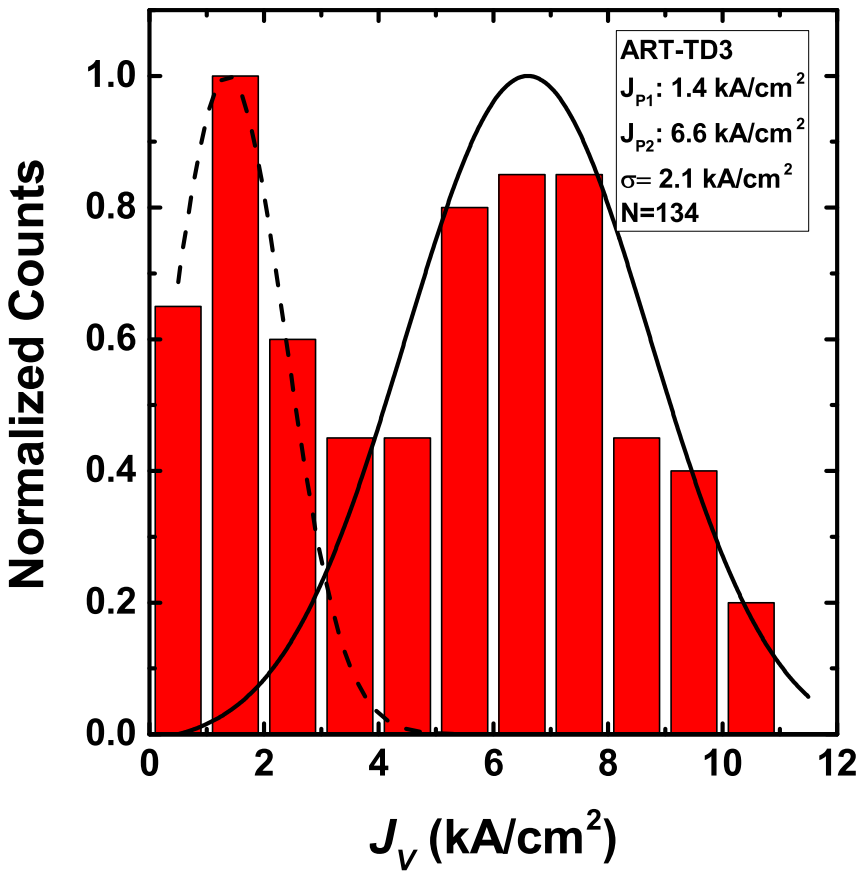


Figure 7.16: Histogram of J_V for ART-TD3, which shows a higher J_V value as compared to the control and buffer layer samples due to the higher defect density.

compared to Si-TD2 and InP-TD1, ART-TD3 has significantly higher J_V due to a greater defect density. However, this sample should not be considered typical for the technology considering that low In content Esaki diodes on ART currently hold the record for PVCR [43].

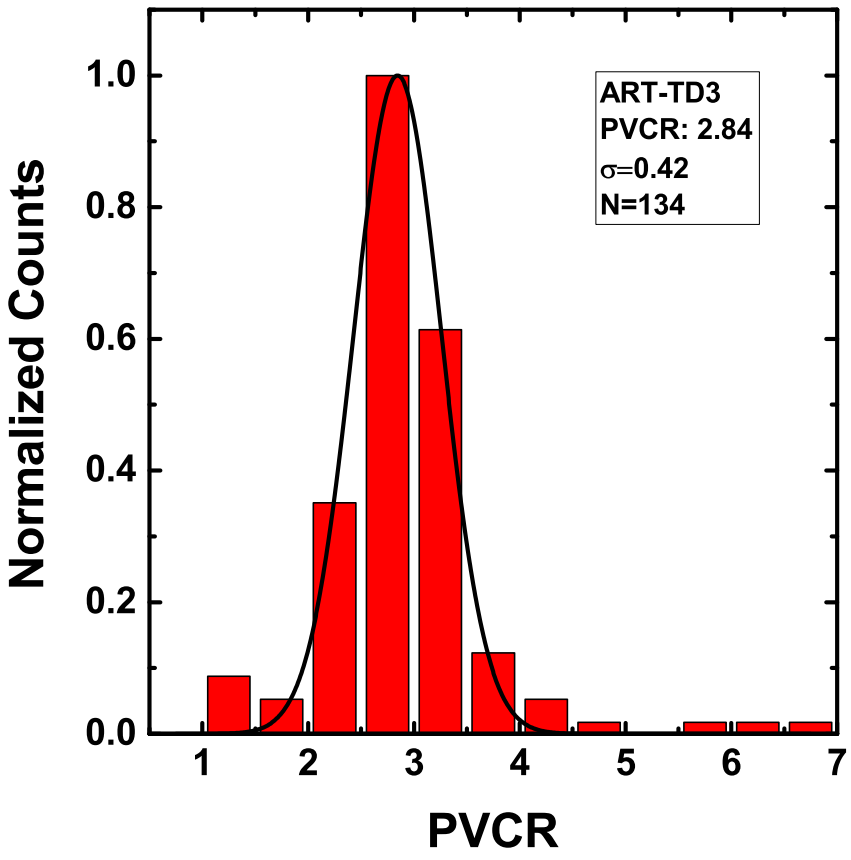


Figure 7.17: Histogram of PVCR from which a value of 2.84 was extracted from a Gaussian fit.

Table 7.2: Summary of device information and extracted values

Device	p $\times 10^{19}$ (cm^{-3})	n $\times 10^{19}$ (cm^{-3})	N^* $\times 10^{19}$ (cm^{-3})	$N^{*-0.5}$ $\times 10^{-10}$ (cm^{-3})	J_P (kA/cm^2)		J_V (kA/cm^2)		PVCR		
					mean	σ	mean	σ	mean	max	σ
InP-TD1[†]	2.45 Be	3.0 Si	1.35	2.72	27.2	3.3	2.6	0.3	10.6	16.4	0.16
Si-TD2[‡]	2.34 Be	3.0 Si	1.31	2.76	12.2	2.7	1.5	0.45	8.6	12.9	0.64
ART-TD3[a]	*2.39* Be	*3.0* Si	*1.31*	*2.73*	19.8	4.6	6.6	2.1	2.84	6.4	0.42

[†] InP
[†] <100> miscut 4° to <110>
[a] ART Virtual InP Substrate on Si

7.5 $In_{0.53}Ga_{0.47}As$ on Si Conclusion

This chapter demonstrated the integration of $In_{0.53}Ga_{0.47}As$ homojunctions on Si substrates and how their performance compared to a control sample on InP. All samples in this chapter were designed to have high PVCR values to assess how defects due to the substrate impact performance. The device layer was designed to be the same across all three samples: control, GaAs buffer on Si, and ART. J_P was highest in InP-TD1 (27.2 kA/cm^2) followed by ART-TD3 (19.2 kA/cm^2) and Si-TD2 (12.2kA/cm^2). PVCR was also highest in InP-TD1 (10.6) followed by Si-TD2 (8.6) and ART-TD3 (2.8). Table 7.2 summarizes the results taken from these samples.

Over 1000 devices were tested for the InP-TD1 and Si-TD2 samples, and over 130 were tested for ART-TD3. This volume of testing created a large dataset from which values of J_P, J_V, and PVCR were extracted and contrasted. Si-TD2 exhibited performance within several standard deviations of the control performance. The ART-TD3 results should be considered atypical of devices grown on an ART platform, as there are several exemplary reports showing parity with lattice matched devices [43, 124]. This information exhibits the excellent potential for integrating III-V tunnel junctions onto a Si platform.

This work demonstrates that $In_{0.53}Ga_{0.47}As$ Esaki diodes can be integrated directly onto a Si platform, with performance very near a control sample. Further enhancements can be made through growth control and buffer design, such that future devices may exhibit minimal degradation. Further, Chapter 8 will show that large lattice mis-

matched systems such as $In_{0.53}Ga_{0.47}As/GaAs_{0.50}Sb_{0.50}$ [27] or InAs/GaSb[28] can be integrated onto a Si platform with similar performance outcomes compared to control samples.

Chapter 8

Broken Gap Esaki Diodes on Si Substrates

8.1 Introduction

Chapter 6 and Chaptger 7 demonstrated broken gap tunnel junctions on GaSb that approach 10 MA/cm^2 J_P and demonstrated integrating large lattice mismatched $In_{0.53}Ga_{0.47}As$ devices on Si. To date, few groups have attempted to integrate GaSb onto Si substrates due to the large lattice mismatch and accompanying defects. This section tests BG tunnel diodes grown on Si to a control GaSb substrate to demonstrate the possibility of integrating InAs/GaSb devices onto a Si platform. A number of modern devices rely heavily on InAs/GaSb tunnel junctions as THz emitters and NIR detectors, moving such devices to a more forgiving substrate such as Si may reduce costs to the point where they are ubiquitous on personal electronics.

8.2 Device design

Devices for this section are based on the BG-12 GaSb i-layer design. Represented in Fig. 8.1(a), GaSb-TD1 was the control sample grown on GaSb and designed to be similar to BG-TD2 in doping and BG-TD12 in layer structure. This allowed a larger range of PVCR values, over which to compare the four samples. Shown in Fig. 8.1(b), AlSb-TD2 is a BG diode grown on a Si substrate with an AlSb buffer. In Fig. 8.1(c)

GaAs-TD3 was grown on GaAs, which is a common lattice mismatched substrate for this material system. Much of the work by Collins et al. [50, 57] was grown on GaAs substrates. Fig. 8.1(d) exhibits STO-TD4, a novel buffer approach to incorporating lattice mismatched III-V's onto Si. STO-TD4 should exhibit electical qualities that are superior to AlSb-TD2.

25 nm	InAs: Te	1×10^{19} cm^{-3}
3 nm	GaSb	uid
300 nm	GaSb: Be	5×10^{18} cm^{-3}
Substrate	GaSb	

(a) GaSb-TD1

25 nm	InAs: Te	1×10^{19} cm^{-3}
3 nm	GaSb	uid
300 nm	GaSb: Be	5×10^{18} cm^{-3}
50 nm	GaSb: Be	uid
500 nm	AlGaSb	uid
Substrate	Si	

(b) AlSb-TD2

25 nm	InAs: Te	1×10^{19} cm^{-3}
3 nm	GaSb	uid
300 nm	GaSb: Be	5×10^{18} cm^{-3}
50 nm	GaSb: Be	uid
500 nm	GaAs Buffer	uid
Substrate	GaAs	

(c) GaAs-TD3

25 nm	InAs: Te	1×10^{19}
3 nm	GaSb	uid
300 nm	GaSb: Be	5×10^{18} cm^{-3}
500 nm	GaSb: Be	uid
500 nm	GaAs	uid
10 nm	$SrTiO_3$ buffer	
Substrate	Si(001)	$4^\circ < 110 >$

(d) STO-TD4

Figure 8.1: Film stacks for the four devices in the BG on Si series. (a) GaSb-TD1 represents the control sample grown on GaSb and designed to be similar to BG-TD2. (b) AlSb-TD2 is a BG diode grown on a Si substrate with an AlSb buffer. (c) GaAs-TD3 was grown on GaAs, which is a common lattice mismatched substrate for this material system. (d) STO-TD4 represents a novel buffer approach to incorportating lattice mismatched III-V's onto Si.

8.3 Broken Gap Esaki Diodes on Si Materials Analysis

XRD analysis for this sample set reveals the expected pattern for device quality. From Fig. 8.2 it can be seen that GaSb-TD1 > GaAs-TD3 > STO-TD4 > AlSb-TD2 in terms of GaSb sharpness. From this, the defect density (Threading Dislocation Density, TDD) for the diodes was found to be 1.47×10^{7} cm^{-2}, 3.89×10^{8} cm^{-2}, 2.27×10^{9} cm^{-2}, and 5.77×10^{9} cm^{-2}, respectively. As seen in Chapter 7, this will have an appreciable effect on PVCR. SIMS was not performed on these systems due to time and

resource constraints, but prior growths have been well within %50 of designed doping levels and those levels will be used for calculating N^*.

In addition to XRD, AFM measurements were taken for the BG on Si series samples. The level of surface roughness can be seen in Fig. 8.3 for each of the four samples. GaSb-TD1 exhibited the lowest RMS of 0.11 nm. while AlSb-TD2 had the highest at 5.73 nm. GaAs-TD3 and STO-TD4, had measured values of 1.23 nm and 2.32 nm respectively. While the height differential for AlSb-TD2 and STO-TD4 are on the order of the InAs thickness, fabricating measurable devices will likely only see real impact for area analysis and undercut measurements.

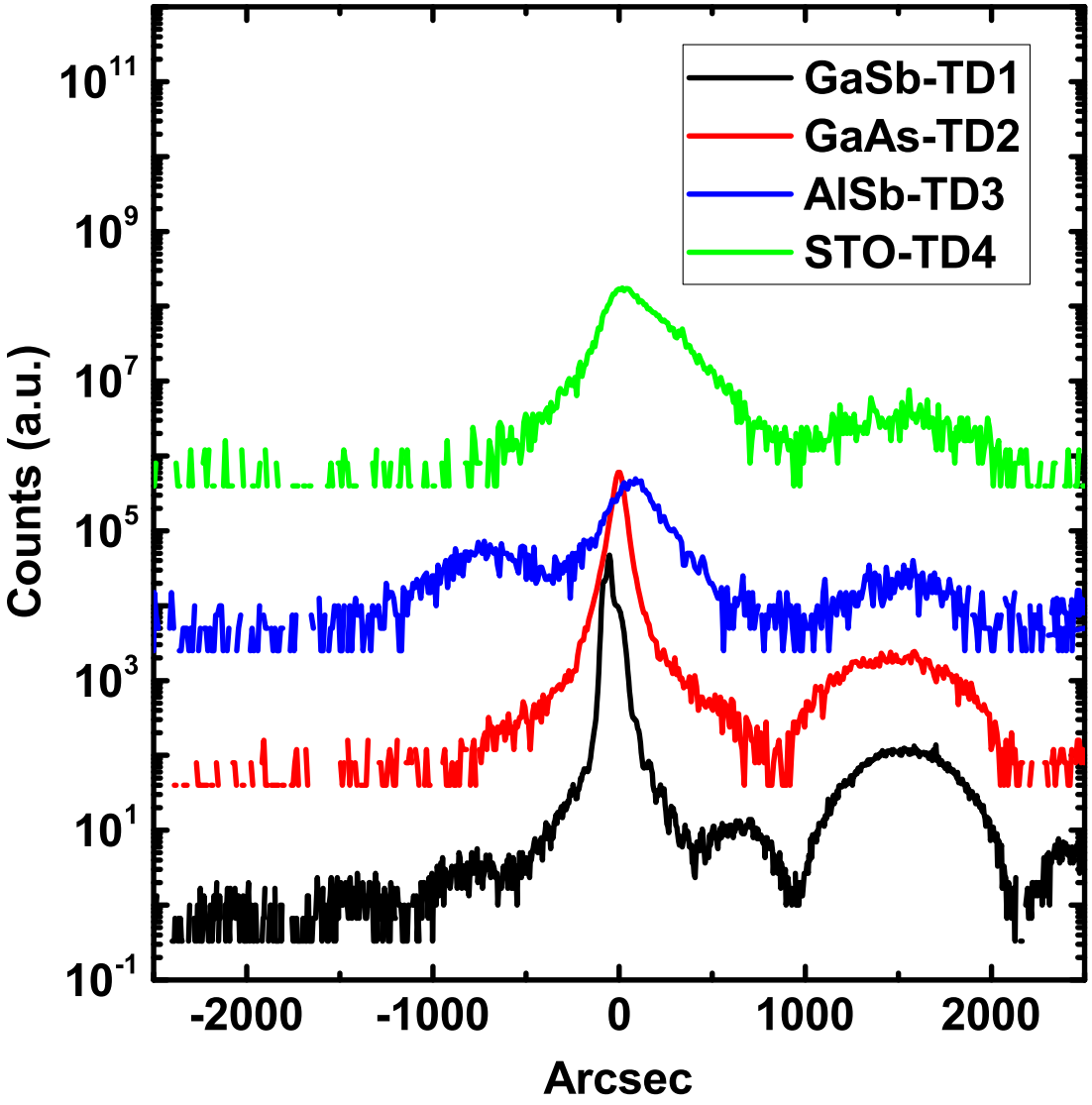
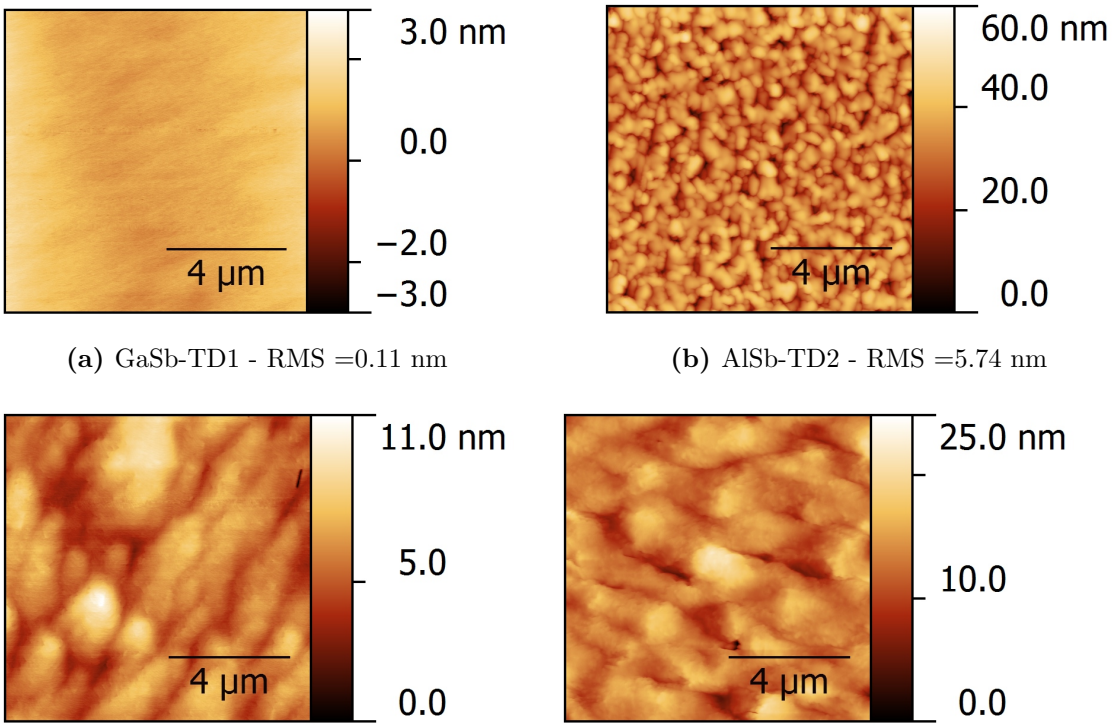


Figure 8.2: HRXRD of BG on Si series samples which have been aligned to the GaSb peak. Differences between the on buffer samples and control appear similar to those presented in Chapter 7, and will likely show decreased PVCR and J_P relative to the control.



(a) GaSb-TD1 - RMS =0.11 nm

(b) AlSb-TD2 - RMS =5.74 nm

(c) GaAs-TD3 - RMS =1.23 nm

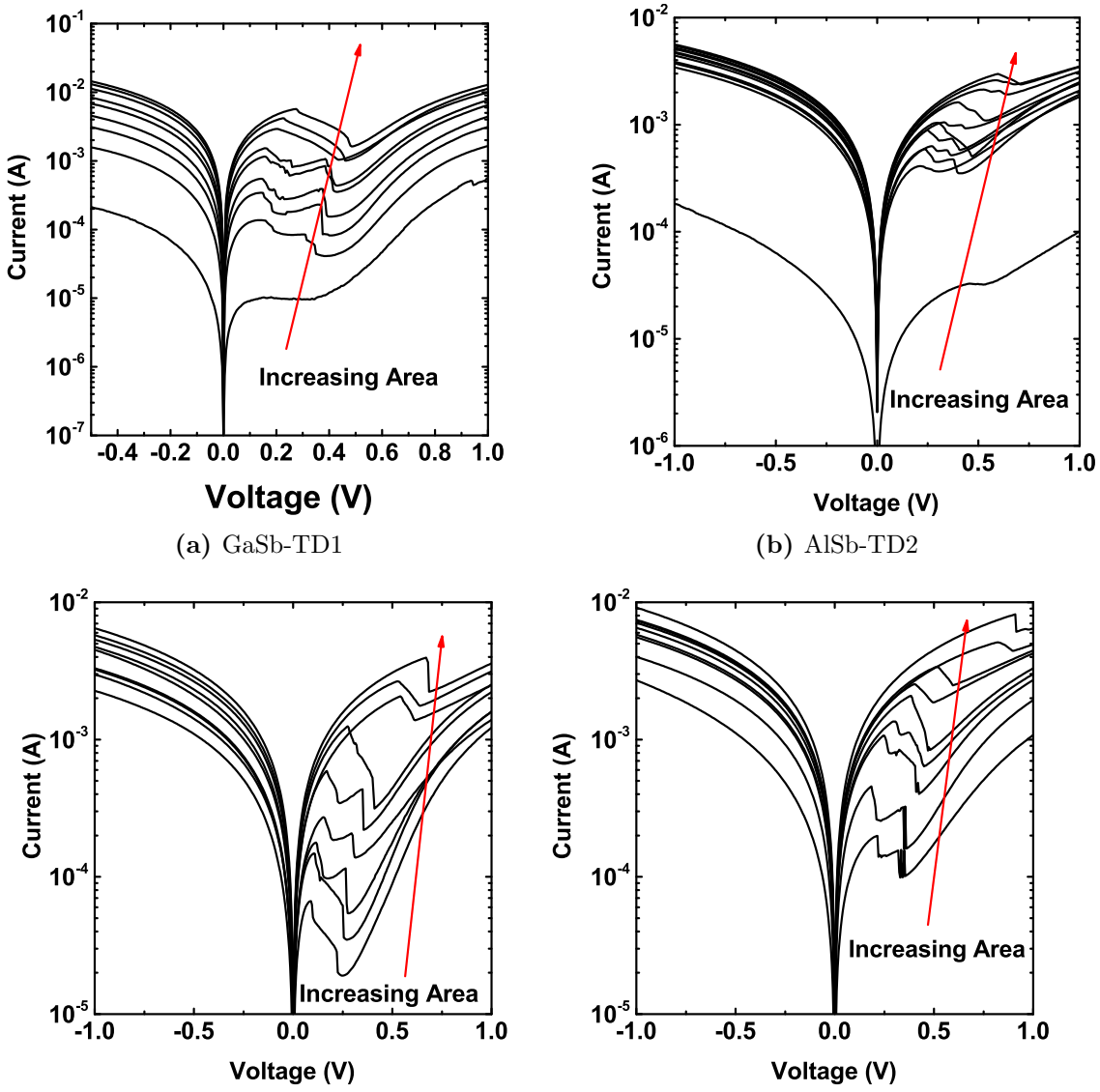
(d) STO-TD4 - RMS =2.32 nm

Figure 8.3: AFM measurements were taken at TSU for each of the BG on Si series samples, GaSb-TD1, AlSb-TD2, GaAs-TD3, and STO-TD4. (a) GaSb-TD1 provided an expected smooth surface with RMS of 0.11 nm over the 100 μm^2 area. (b) AlSb-TD2 exhibited the roughest surface due to the largest mismatch in lattice constant from Si, and had a RMS of 5.74 nm. (c) GaAs-TD3 exhibited lower RMS roughness (1.23 nm) than AlSb-TD2 but higher than GaSb-T1, as expected. (d) exhibited RMS values of 2.32 nm and was expected to perform between the AlSb and GaAs TD samples.

8.4 Broken Gap Esaki Diode on Si Electrical Analysis

Over 100 diodes have been measured per sample to build a reasonable dataset for extracting J_P and PVCR. Fig. 8.4 presents select *I-V* characteristics for BG on Si series diodes ranging from 0.25 μm^2 to 4 μm^2 areas as mask defined. Negative differential resistance (NDR) was clearly present at room temperature, and the oscillations seen in the curves are a common artifact of the measuring equipment commonly seen in other reports [27, 28, 43, 66]. Mean PVCR for each system was extracted from histograms is summarized in Table 8.1. Surprisingly, AlSb-TD2 had the highest mean PVCR of all the on buffer devices. Similar to Chapter 7, as device areas shrink PVCR range overlaps more as seen in Fig. 8.6. Interestingly, GaAs-TD3 exhibits a larger PVCR maximum value than GaSb-TD1, at 4.95 and 4.47 respectively. STO-TD4 held a maximum PVCR of 3.25, while AlSb-TD2 provided a maxmimum of 2.89. Maximum PVCR values are generally in line with defect density, though at $\approx 4\times10^8$ cm^{-2} most GaAs-TD3 devices are below the critical device area for matching control diode performance.

J_P was extracted from the histograms shown in Fig. 8.7, and was shown to follow along with defect density. Differences in J_P between the samples may be related to a few possibilities. Without SIMS to confirm doping levels, the different thermal properties of Si, GaAs, and GaSb may have had dopants diffuse or incorporate differently. Generally, the same issues affecting $In_{0.53}Ga_{0.47}As$ performance on Si will affect GaSb on Si devices. J_V values were also extracted and are summarized in Table 8.1 along with J_P.



(a) GaSb-TD1

(b) AlSb-TD2

(c) GaAs-TD3

(d) STO-TD4

Figure 8.4: Representative *I-V* characteristics for BG on Si devices with areas ranging from 0.25 μm^2 to 4 μm^2. NDR was present at room temperature, indicating the presence of good tunnel junctions for each sample.

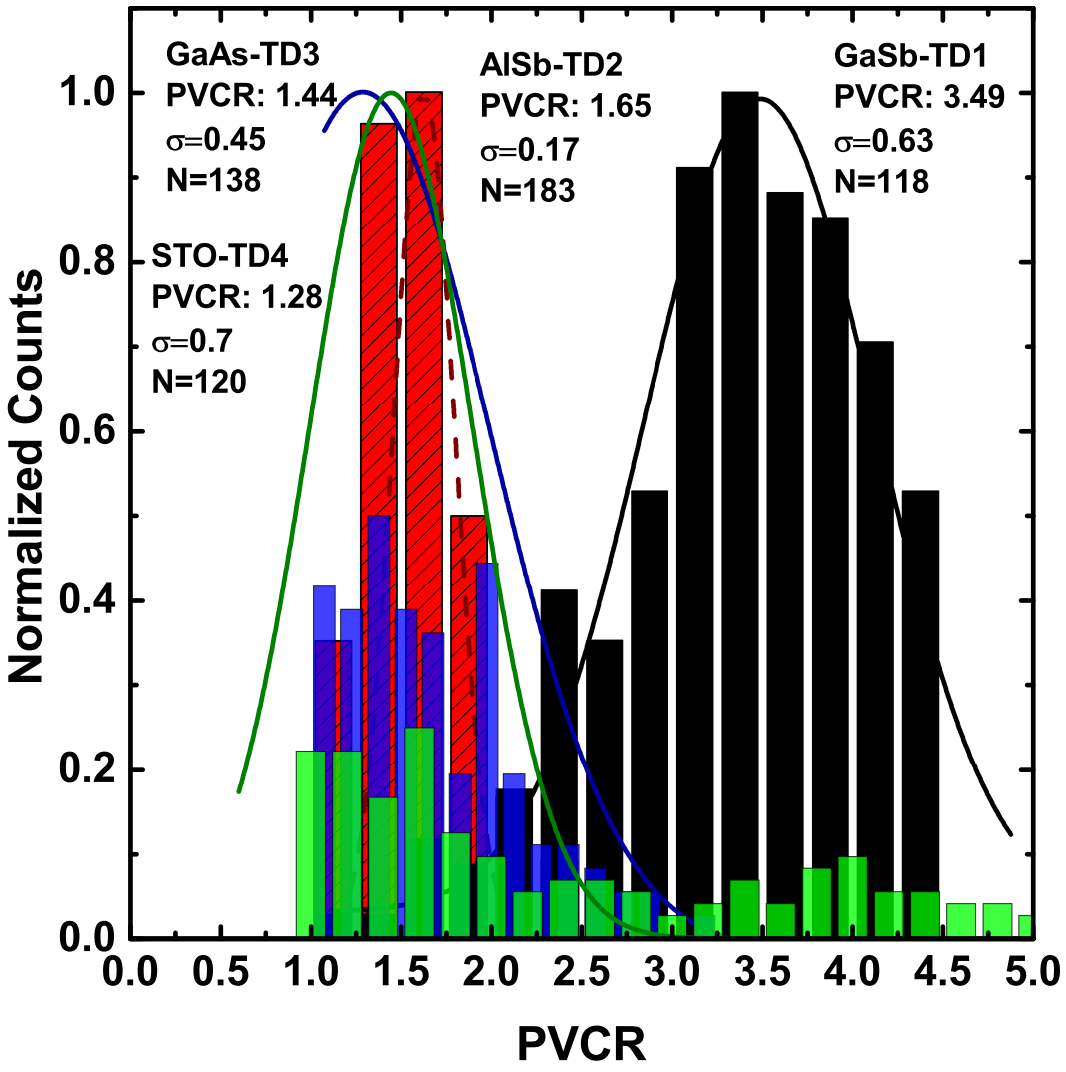


Figure 8.5: Normalized PVCR histograms for BG on Si study, with GaAs-TD3 and STO-TD4 scaled for visibility, showing that median values for PVCR are quite similar across devices on a buffer. However, samples with the smallest defect density show significantly higher PVCR range.

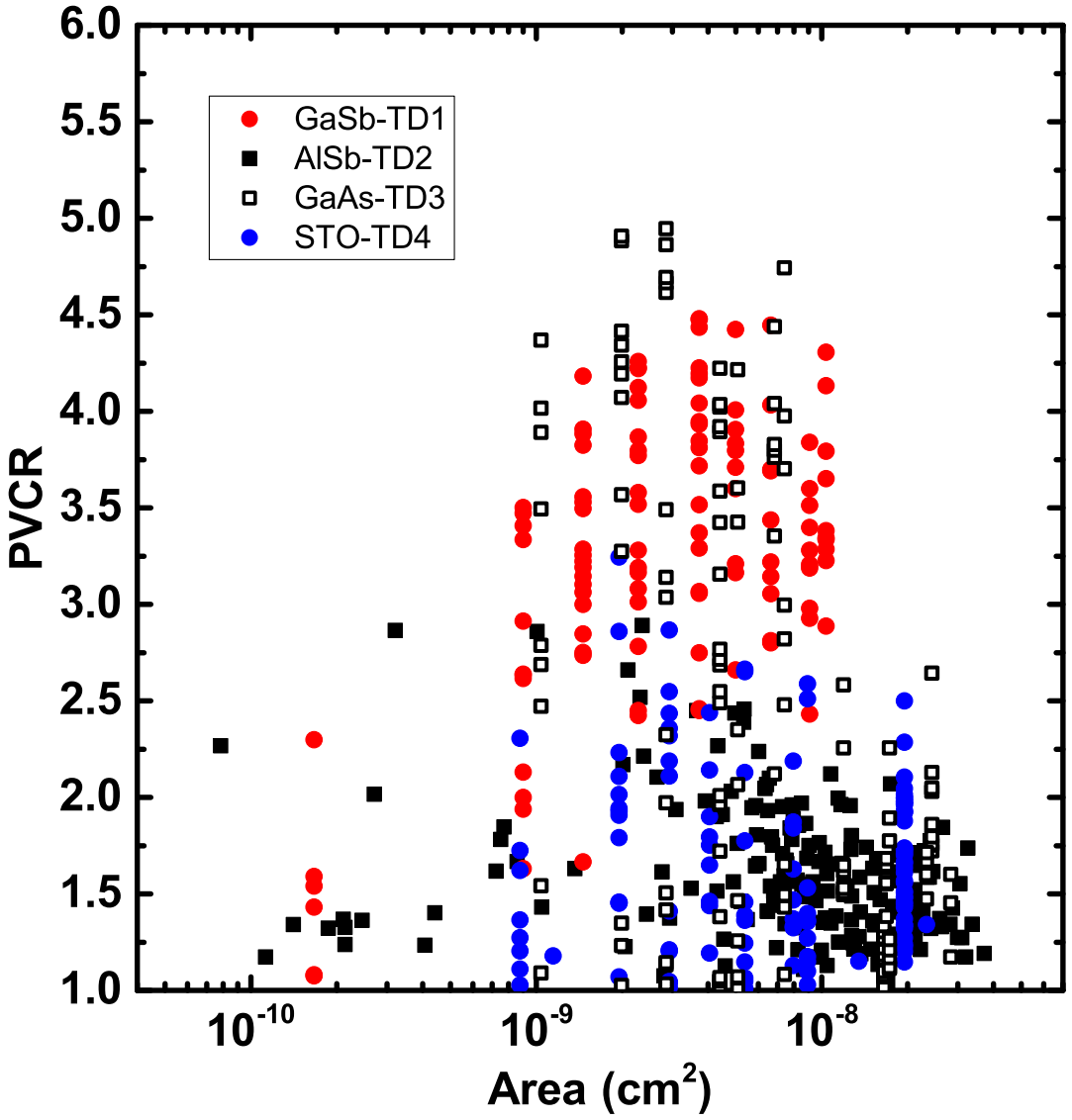


Figure 8.6: Devices are plotted by PVCR *vs.* area showing that PVCR tends to show maximum values prior to reaching the limits of the process control window. Both GaAs-TD3 and GaSb-TD1 show maximum PVCR around 4×10^{-9} cm^2.

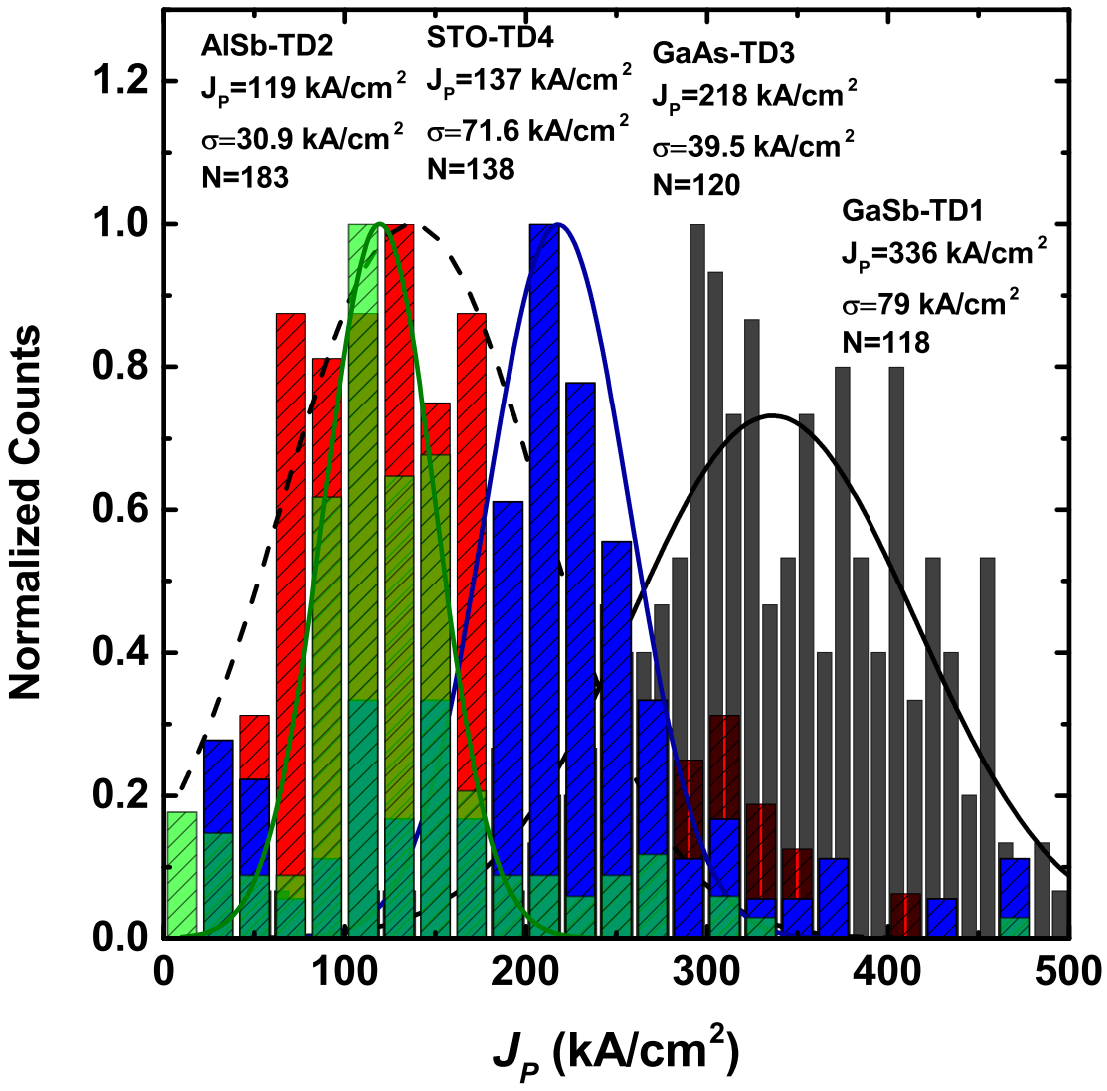


Figure 8.7: Normalized J_P histograms for BG on Si series showing the effect of various buffers on J_P. Varying results for J_P between the four samples may be due to the difference in thermal properties as STO-TD4 and AlSb-TD2 appear to have similar J_P, while GaSb-TD1 and GaAs-TD3 are more than double the J_P of the on Si samples.

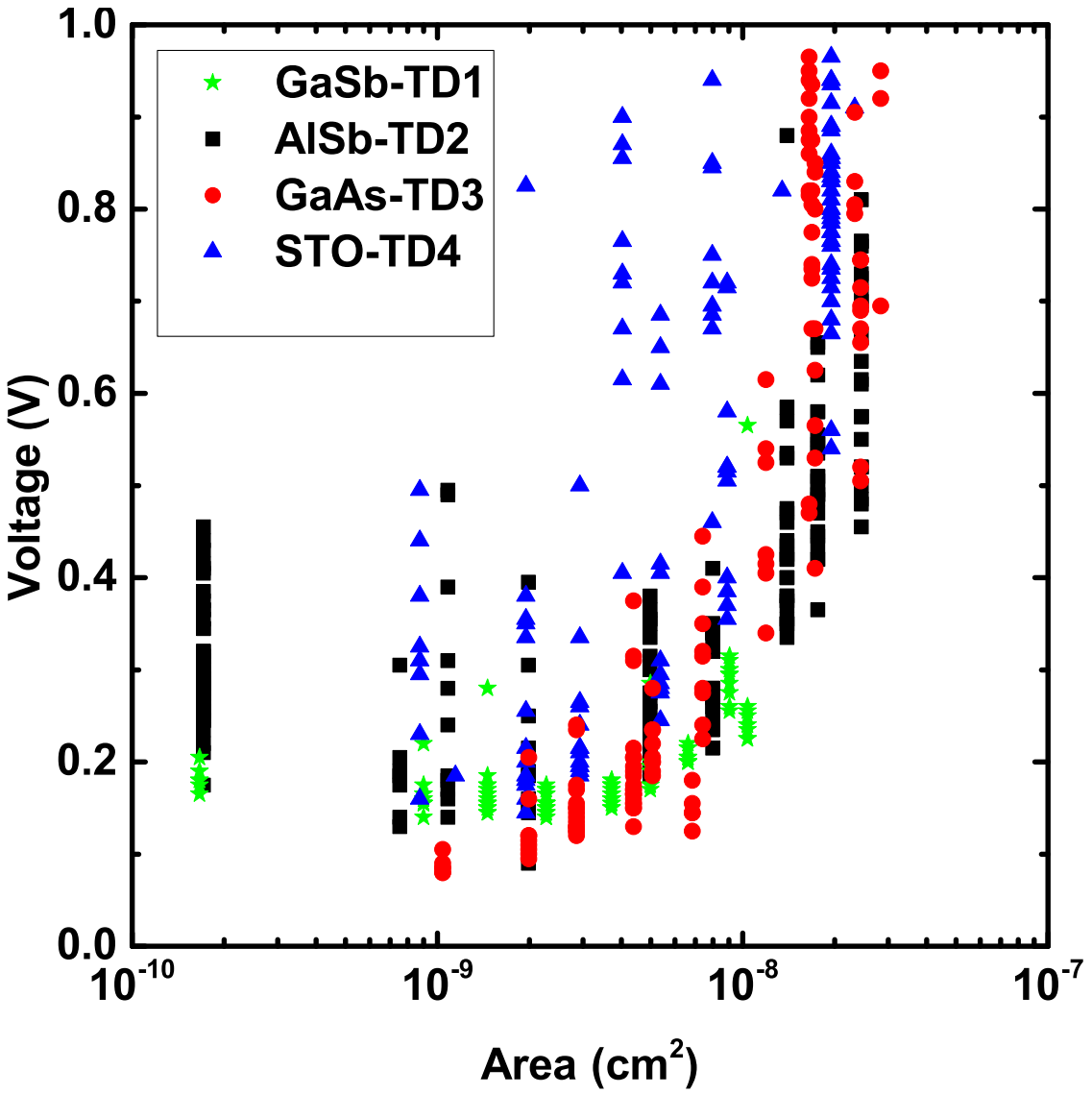


Figure 8.8: Typical minimum V_P values for the BG on Si devices appear to fall between 0.2 V and 0.3 V, indicating minimal influence from R_S. STO-TD4 appears to have higher V_P, likely due to variations in etch back of BCB affecting device measurements.

Table 8.1: Summary Broken Gap on Si Device Data

Device	p $\times 10^{19}$ (cm^{-3})	n $\times 10^{19}$ (cm^{-3})	N^* $\times 10^{19}$ (cm^{-3})	$N^{*-0.5}$ $\times 10^{-10}$ (cm^{-3})	J_P (kA/cm^2)		J_V (kA/cm^2)		PVCR		
					mean	σ	mean	σ	mean	max	σ
GaSb-TD1[†]	0.5	1.0	0.33	5.48	336	79	117	44.7	3.43	4.47	0.63
AlSb-TD2[‡]	0.5	1.0	0.33	5.48	119	30.9	93.6	26.1	1.65	2.89	0.36
GaAs-TD3[a]	0.5	1.0	0.33	5.48	137	71.6	68.0	65.3	1.44	4.95	0.45
STO-TD4[b]	0.5	1.0	0.33	5.48	218	39.5	114	72.4	1.29	3.25	0.7

[†] GaSb <100>
[‡] AlSb Buffer on 4° miscut <110> Si<100> substrate
[a] GaAs <100>
[b] $SrTiO_3$ buffer on 4° miscut <110> Si<100> substrate

8.5 Broken Gap Esaki Diodes on Si Conclusion

This chapter demonstrated the integration of InAs/GaSb heterojunctions on Si and GaAs substrates and compared their performance to a control sample on GaSb. All samples in this chapter were designed to have high PVCR values to assess how defects due to the substrate impact performance. The device layer was designed to be the same across all four samples: control, on GaAs , on AlSb buffer, and on a $SrTiO_x$ buffer. J_P was highest in GaSb-TD1 (336 kA/cm^2) followed by GaSb-TD3 (218 kA/cm^2), STO-TD4 (137 kA/cm^2), and AlSb-TD2 (119kA/cm^2). PVCR was highest in GaAs-TD3 (4.95) followed by GaSb-TD1 (4.47), STO-TD4 (3.25), and AlSb-TD2 (2.89). Table 8.1 summarizes the results taken from these samples.

Over 100 devices were tested for each device. This volume of testing created a dataset from which values of J_P and PVCR were extracted and contrasted. Additional test volume would allow for the extraction of the critical device sizes for AlSb-TD2 and STO-TD4 for similar performance *vs.* the control sample. This information exhibits the potential for integrating broken gap tunnel junctions onto a Si platform.

This work demonstrates that InAs/GaSb Esaki diodes can be integrated directly onto a Si platform, with performance approaching a control sample. Further enhancements can be made through growth control and buffer optimization, such that future devices may exhibit minimal degradation.

Chapter 9

Conclusions and Recommendations

This dissertation demonstrated a relationship between effective band gap and doping density that had not been shown. By reducing the effective bandgap significant gains can be made to tunnel currents for the same doping density. Thirty three (33) different samples were grown, and thousands of devices tested for this dissertation. This dissertation demonstrates the highest J_P for any tunneling system, 3.2 MA/cm^2, as well as one of the highest J_P for any tunnel diode on a Si platform, 137 kA/cm^2. This work mapped the relationship between J_P and N^* for multiple heterojunction systems showing that reduced effective bandgap results in higher J_P for a given doping density. Furthermore, this dissertation demonstrates that below a critical area devices can between a control and one grown on Si can not be differentiated.

9.1 Impact of Work

This dissertation mapped the performance of multiple (≈ 25) tunnel diode systems with varying band gaps to show that ultra high current densities may be possible for broken gap tunneling systems as seen in Fig.9.1. When combined with other literature values, an excellent chart for determining J_P based on N^* has been expanded to include the heterojunction systems of InAs/GaSb, $In_{0.53}Ga_{0.47}As/GaAs_{0.50}Sb_{0.50}$, and $InAs_{0.91}Sb_{0.09}$/AlGaSb. From Fig. 9.1, it appears that the InAs/GaSb hetero-

junction system could possibly reach the 10 MA/cm^2 if effective doping can exceed 2×10^{20} cm^{-3}.

Some of this effort has been cited by other authors in their work and some can be shown to fit along the figure of merit plot in Fig. 9.2 [11, 94, 147, 165–172]. Interest in LSG devices for TFETs current was studied by Desplanque et al. [147][173] and have shown some improvement in the case of $InAs_{0.91}Sb_{0.09}/Al_{0.40}Ga_{0.60}Sb$, pushing 1.3 MA/cm^2 for the $InAs/Al_{0.40}Ga_{0.60}Sb$ system. Investigation of this concept by other groups implies that this work will have impact on future tunneling devices.

Other groups have begun to use this work for modeling tunneling junctions. Luisier [11] and Agarwal and Yablonovitch [170] have used this work to model electrical transport in tunnel junctions and to predict substhreshold slope for TFETs. Chun-Hsing and Nguyen Dang [168] investigated low E_G heterojunctions for TFET applications, and cited the J_P for the BG diodes for design and modeling of TFET performance.

Outside of TFETs and associated tunneling models, PV investigators have also utilized this work for comparing MJSC's. Garca et al. [94] showed J_P values tracked for heterojunctions Esaki diodes that have E_G between $In_{0.53}Ga_{0.47}As$ and GaAs. This data is further validation for J_P tuning with heterojunctions and effective E_G.

Additionally, this work has improved upon the information available for heterointegration onto Si substrates. This dissertation reports both the highest $In_{0.53}Ga_{0.47}As$ and InAs/GaSb J_P reported on Si. This work shows that similarly designed devices can perform nearly identically on Si and lattice matched substrates. It may be possible to integrate III-V based sensors, lasers, and other devices onto inexpensive Si substrates if defect density is reduced to levels that allow for acceptable device to device variation.

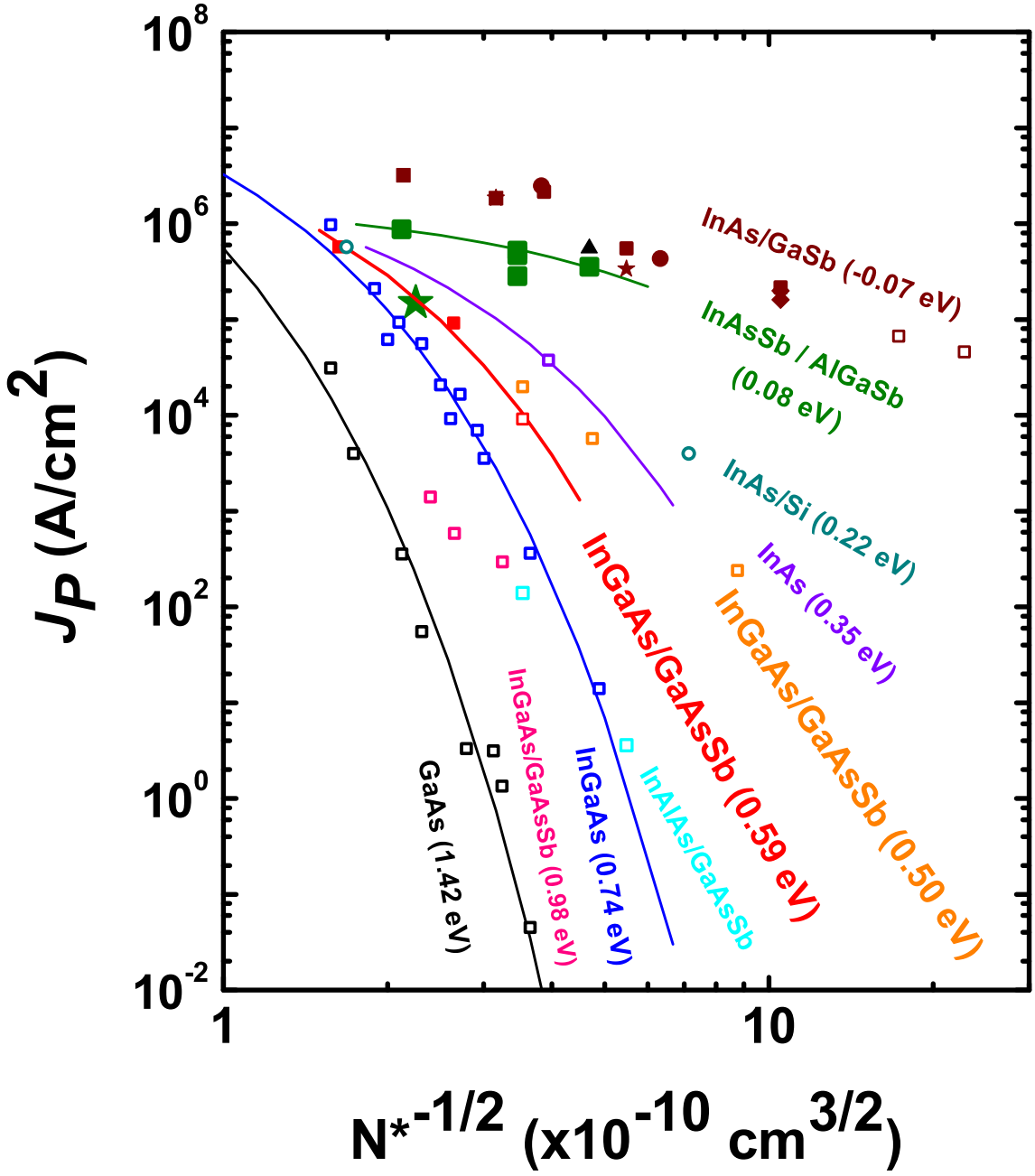


Figure 9.1: Final figure of merit plot with data from all samples in this dissertation overlayed with other reported tunnel diodes.

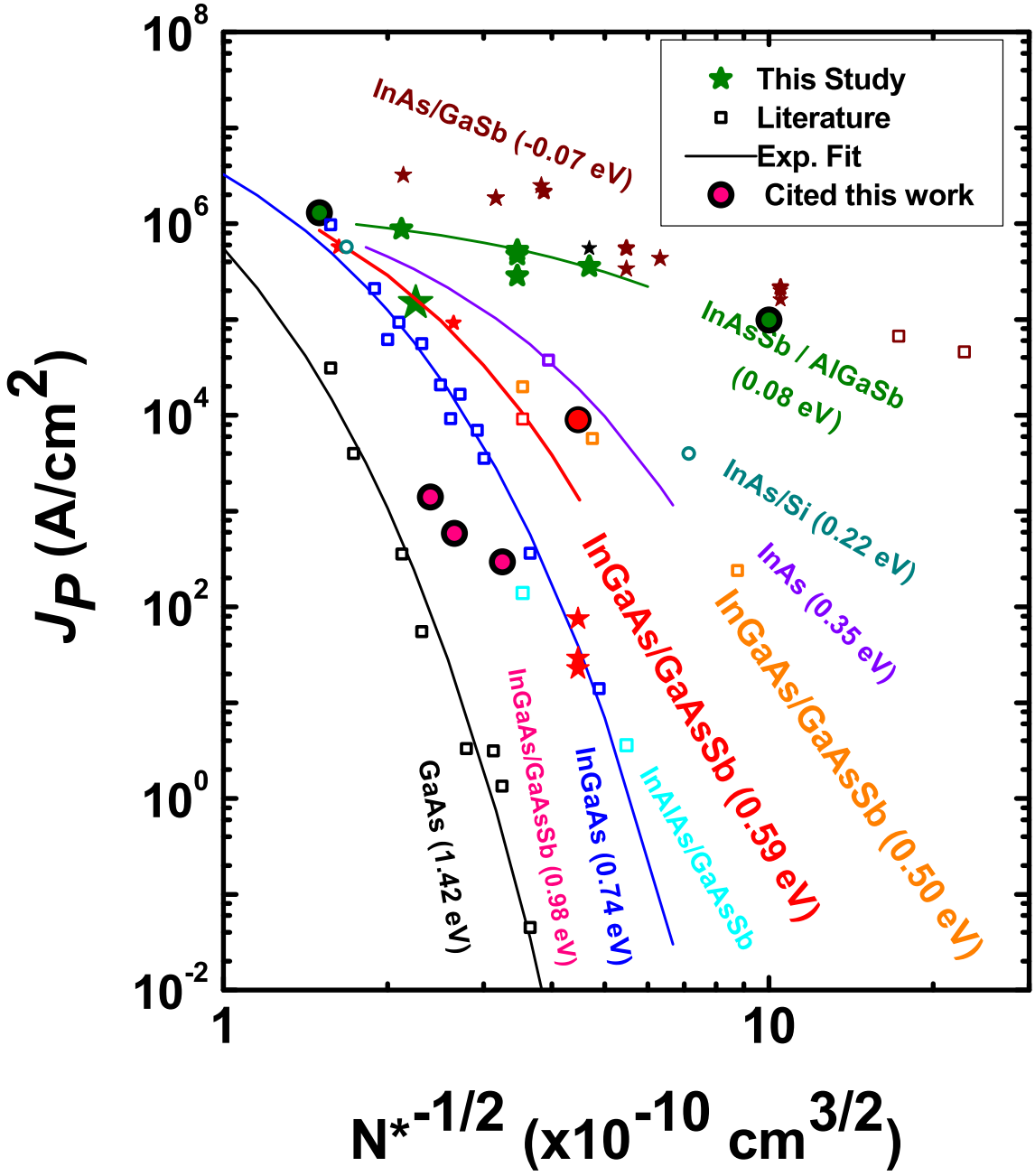


Figure 9.2: Figure of merit plot with data from reports that have cited this work[94, 147, 174].

9.2 Final Recommendations

This work did not meet the 10 MA/cm^2 J_P specified in previous sections. Future work could show that increased doping density in the InAs/GaSb system is capable of reaching this target. In addition, much more research could be applied to the $InAs_{0.91}Sb_{0.09}/Al_{0.40}Ga_{0.60}Sb$ system. As a potential TFET candidate this system has excellent off characteristics, but additional work similar to that of Desplanque et al. [147] is needed to approach higher current levels.

Near the end of this work it was noticed that odd speckling became visible on InAs/GaSb samples that had the GaSb exposed to atmosphere for long periods. This may indicate that there is an oxidation mechanism at play, which may have detrimental effects on device performance. It should also be noted that samples which incorporated As into the GaSb layer did not show this effect. This may prove important if these devices are to become common place.

Future studies should investigate the impact of i-layer design on the total tunneling current, as there may be something to the design by Collins et al. [57] where there may be an ideal device length. Additionally the impact of the terminations at the heterointerface warrant further study as the InSb-like GaAs-like interfaces have been shown to have an impact on RTDs [154] and may impact Esaki diodes and TFETs as well. Raman spectroscopic study of the systems in this work may also prove interesting, as initial work showed an odd coupling between the InAs and GaSb doped regions that would not normally be expected.

Prior to this work a comprehensive map of device performance, J_P, with respect to effective doping, N^* did not exist. Additionally, integration of tunnel diodes on Si had been limited to sub-kA/cm^2 J_P for III-V devices. Now, it has been shown that large lattice matched systems can perform well on a Si platform. This work has accomplished part of its goal by building an empirical data set which may be used

for the design of many different devices.

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Appendix A: Sample Processes

A.1 Process Recipes

Table A.1: CVC 601 metal depsition process

Step	Process	Time
1	Mount samples near center of carrier wafer	10 - 20 min
2	Load carrier wafers	5 min
3	Clean seal	1 min
4	Pump Down to below 6×10^{-6} Torr	3-18 hours
5	Deposit Metal	30 min set up 5- 15 minute run time
6	Unload chamber and shut down tool	5 min

A.2 Process Traveler

Table A.2: Process Traveler

Step	Process	Completed
1	Sample identified and origin mapped	
2	Level 1 metalization Lift off or Metal first	
3	Lift off Photoresist: Process recipe: beam current: x move ——, y move —— Surface clean: Deposition tool: Deposition metal: Recipe: Base Pressure: Thickness:	Metal First Surface clean: Deposition tool: Deposition metal: Recipe: Base Pressure: Thickness: Photoresist: Process recipe: beam current: x move ——, y move —— Metal Etch Tool: Recipe:	
4	Mesa Etch: Chemistry:—— Time:—— Target Height: ——	
5	Undercut: x:—— y:——	
6	Area Analysis	
7	M1 testing notes:	
8	BCB application Time:— Temp:—	
9	L2 Lift off Photoresist: Process recipe: beam current: x move ——, y move —— Surface clean: Deposition tool: Deposition metal: Recipe: Base Pressure: Thickness:	
10	Level 2 Tool: Process recipe: Etch time:	
11	M2 testing notes	

A.3 Die Maps

A.3.1 NPGS Layout

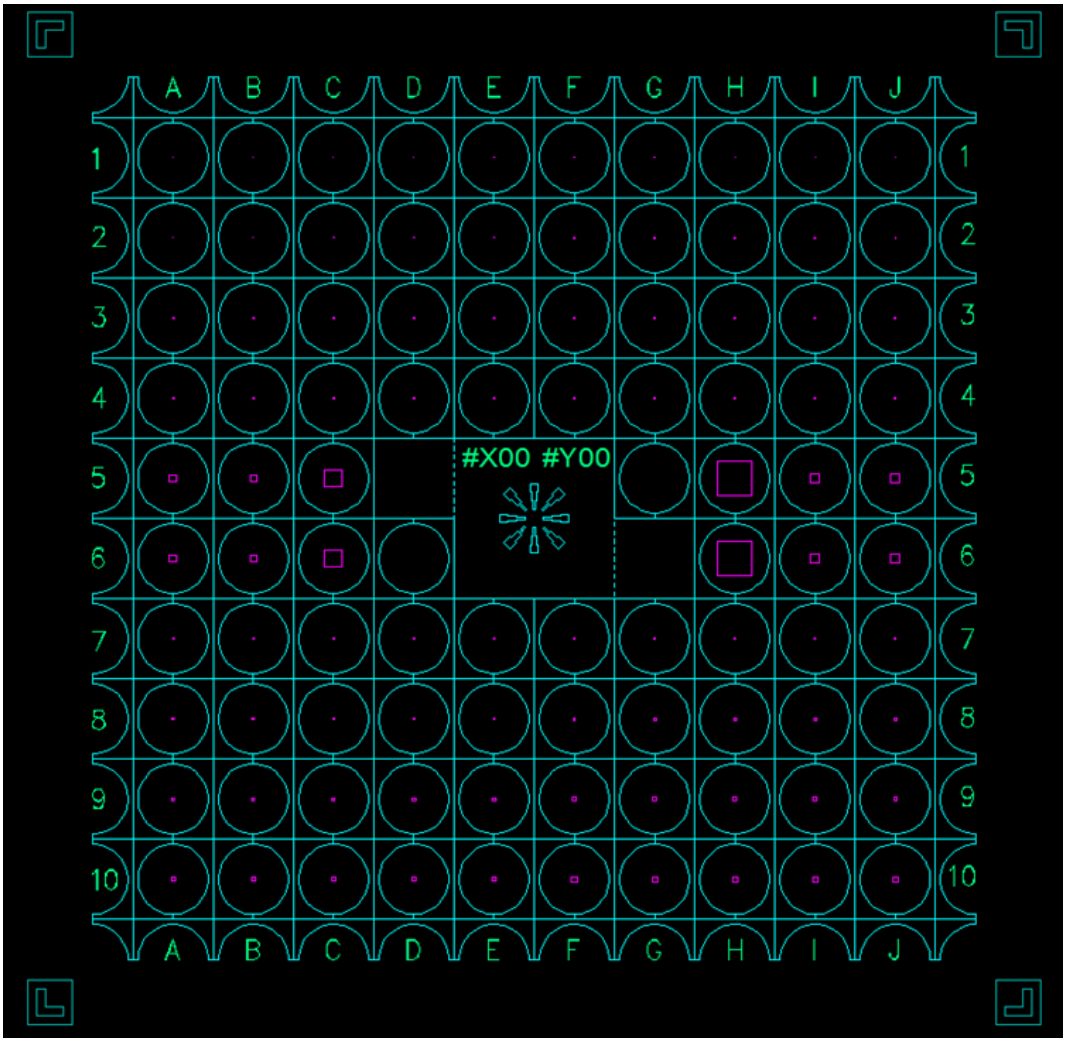

Figure A.1: Example layout of die

A.3.2 ETD layout 12

	A	B	C	D	E	F	G	H	I	J	
1			100					200			1
2			300					400			2
3			500					600			3
4			700					800			4
5	4.0	4.0	10	GND	FUSION REACTOR		CAP	20	5.0	5.0	5
6	4.0	4.0	10	CAP			GND	20	5.0	5.0	6
7			900					1.0			7
8			1.2					1.4			8
9			1.6					1.8			9
10			2.0					3.0			10
	A	B	C	D	E	F	G	H	I	J	

Figure A.2: Die layout for ETD12 ebeam file

A.3.3 ETD layout 13

	A	B	C	D	E	F	G	H	I	J	
1			500					500			1
2			600					600			2
3			700					700			3
4			800					800			4
5	4.0	4.0	10	GND	FUSION REACTOR		CAP	20	5.0	5.0	5
6	4.0	4.0	10	CAP			GND	20	5.0	5.0	6
7			900					1.0			7
8			1.2					1.4			8
9			1.6					1.8			9
10			2.0					3.0			10
	A	B	C	D	E	F	G	H	I	J	

Figure A.3: Die layout for ETD13 ebeam file

A.3.4 ETD layout 13b

	A	B	C	D	E	F	G	H	I	J	
1			500					500			1
2			600					600			2
3			700					700			3
4			800					800			4
5	4.0	4.0	10	GND	FUSION REACTOR		CAP	20	5.0	5.0	5
6	4.0	4.0	10	CAP			GND	20	5.0	5.0	6
7			900					1.0			7
8			1.2					1.4			8
9			410					410			9
10			410					410			10
	A	B	C	D	E	F	G	H	I	J	

Figure A.4: Die layout for ETD13b ebeam file

Appendix B: Sample Descriptions

Table B.1: Broken Gap Tunnel Diode

Device Name			Substrate
External	Internal	Grower	
SSG-TD1	TD1	Intelliepi	InP[a]
SSG-TD2	TD1A	IQE	InP[a]
SSG-TD3	TD2	Intelliepi	InP[a]
SSG-TD4	TD08	5-2206	InP[a]
SSG-TD5	TD09	5-2207	InP[a]
SSG-TD6	TD10	5-2208	InP[a]
LSG-TD1	TD3	Intelliepi	GaSb‡
LSG-TD2	TD3B	IQE	GaSb†
LSG-TD3	TD3D	IQE	GaSb†
LSG-TD4	TD3E	IQE	GaSb†
LSG-TD5	TD3A	IQE	GaSb†
LSG-TD6	TD3C	IQE	GaSb†
BG-3	TD7-D	7-546	GaSb†
BG-2	TD7-B	7-536	GaSb†
BG-1	TD7-A	7-524	GaSb†
BG-4	TD7-C	7-537	GaSb†
BG-5	TD7-E	7-616	GaSb†
BG-6	TD7-F	7-617	GaSb†
BG-7	TD7-G	7-618	GaSb†
BG-8	TD7-H	7-619	GaSb†
BG-9	TD7-I	IQE	GaSb‡
BG-10	TD7-J	IQE	GaSb‡ 5
BG-11	TD7-K	IQE	GaSb‡
BG-12	TD11-D	7-960	GaSb‡
InP-TD1	TD0G	1506	InP[a]
Si-TD2	TD0F	1478	Si[b]
ART-TD3	TD0H	1518	Si
GaSb-TD1	TD11D	7-960	GaSb‡
AlSb-TD2	TD11I	7-1220	GaSb‡
GaAs-TD3	TD11J	7-1370	GaSb‡
STO-TD4	TD11K	7-1312	GaSb‡

†<100> GaSb
‡<100> GaSb 0.35° offcut to <111>
[a] <100> InP
[b]<100> Si 4° offcut to <110>