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Passivation of Amorphous Indium-Gallium-Zinc Oxide (IGZO) Thin-Film Transistors

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PASSIVATION OF AMORPHOUS INDIUM-GALLIUM-ZINC OXIDE (IGZO) THIN-FILM TRANSISTORS

by

Nathaniel Walsh

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ABSTRACT

Thin-film transistors (TFTs) with channel materials made out of hydrogenated amorphous silicon (a-Si:H) and polycrystalline silicon (poly-Si) have been extensively investigated. Amorphous silicon continues to dominate the large-format display technology; however newer technologies demand a higher performance TFT which a-Si:H cannot deliver due to its low electron mobility, $\mu_n \sim 1\ cm^2/V \cdot s$. Metal-oxide materials such as Indium-Gallium-Zinc Oxide (IGZO) have demonstrated semiconductor properties, and are candidates to replace a Si:H for TFT backplane technologies.

This work involves the fabrication and characterization of TFTs utilizing a-IGZO deposited by RF sputtering. An overview of the process details and results from recently fabricated IGZO TFTs following designed experiments are presented, followed by analysis of electrical results. The investigated process variables were the thickness of the IGZO channel material, passivation layer material, and annealing conditions. The use of electron-beam deposited aluminum oxide (alumina or Al_2O_3) as back-channel passivation material resulted in improved device stability; however I_D-V_G transfer characteristics revealed the influence of back-channel interface traps.

Results indicate that an interaction effect between the annealing condition (time/temperature) and the IGZO thickness on the electrical behavior of alumina-passivated devices may be significant. A device model implementing fixed charge and donor-like interface traps that are consistent with oxygen vacancies (OV) resulted in a reasonable match to measured characteristics. Modified annealing conditions have resulted in a reduction of back-channel interface traps, with levels comparable to devices fabricated without the addition of passivation material.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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Chapter 1

INTRODUCTION

1.1 Introduction and Motivation

Thin-film transistors (TFTs) have been around since the 1960s, but their applications really came to fruition in the past two decades. The incumbent technology utilizes amorphous silicon (a-Si:H) for the channel. With emerging technologies, TFTs are utilized in the active-matrix liquid crystal display (LCD), active-matrix organic light-emitting diode (AMOLED) display, flexible displays, and many more applications [1,2]. Emerging applications require the device to operate at higher performance than a-Si:H, which is why there have been many semiconductors studied for the channel of these devices. The most prominent materials include polycrystalline silicon (poly-Si), Zinc Oxide (ZnO), Indium-Gallium-Zinc Oxide (IGZO), and Hafnium-Indium-Zinc Oxide (HIZO).

IGZO exhibits a high mobility ($\mu_{n\text{-}ch}$ ~15 $cm^2/V{\cdot}s$) for an amorphous material, which is much higher than a mobility of $\mu_{n\text{-}ch}$ ~1 $cm^2/V{\cdot}s$ for a-Si:H. Amorphous silicon is deposited at 350 ˚C with PECVD, but the low temperature sputter of IGZO is advantageous by making it suitable for flexible plastic displays [3]. Another benefit to IGZO is the very low off-state current because there are very few free hole carriers [3, 4].

A disadvantage of IGZO is that it is very difficult to generalize characteristics due to the number of factors that need to be taken into account, including the channel composition, deposition method, dielectrics and the associated interfaces, annealing conditions, and the physical structure of the device [5]. IGZO is also not like traditional silicon MOSFETs where the silicon is doped with boron, phosphorus, or arsenic. IGZO, has oxygen

vacancies (OV) inherent in the material, which act as donors. Thus, IGZO is an n-type channel semiconductor material. It is the filling of these donor-like vacancies that help manipulate the electrical properties of IGZO.

1.2 Work Covered by This Document

The primary focus of this work is to investigate the back channel passivation layer of TFTs fabricated with RF-sputtered IGZO. While IGZO TFTs fabricated without back-channel passivation material may result in excellent electrical performance, a passivation material is required for acceptable stability and process integration. A complete description of IGZO TFT technologies is given in Chapter 2. Preliminary work of annealing IGZO and contact metallurgy will be discussed in Chapter 3. Process flow, experimental design, and process integration strategies will be discussed in Chapter 4. Results of electrical testing and device simulation will be presented in Chapter 5. Finally, Chapter 6 will include a discussion summary followed by conclusions and future work.

Chapter 2

IGZO TFT TECHNOLOGIES

The first thin-film transistor was developed in the 1960s with CdS as the channel layer material [6]. By the mid-1980s, the use of silicon-based materials became more pronounced. TFTs are primarily utilized in display technologies and a-Si:H and low temperature polycrystalline silicon (LTPS) dominate for switching devices in active matrix displays. Oxide semiconductors have become popular in that last decade as a way to replace the incumbent silicon technologies. The benefit of these materials is that provide a better performance in a smaller geometry. One such promising oxide semiconductor is IGZO. This chapter will review the electrical properties, modeling and simulation, annealing and passivation of IGZO TFTs.

2.1 Characteristics of IGZO

A-IGZO is an n-type semiconductor and is basically composed of known n-type semiconductors: In_2O_3, Ga_2O_3, and ZnO. IGZO is a wide bandgap semiconductor, which according to optical absorption via the Tauc Plot is estimated to be 3.2 eV for high quality IGZO films; it decreases to about 3.0 eV for low quality films [1, 3]. Liu *et al.* have even reported that the bandgap is as high as 3.5 eV [7]. The electron mobility of IGZO has been reported to be greater than 10 $cm^2/V{\cdot}s$, which is more than ten times that of a-Si [1, 8, 9, 10], and a primary reason to replace a-Si:H with IGZO TFTs. Normura *et al.* studied coordination structures and electronic structure in a-IGZO by using x-ray absorption fine structure (XAFS), and they concluded that a-IGZO has a similar bonding arrangement as c-IGZO, which is shown in Figure 1 [8]. It is possible to fabricate c-IGZO

but not in thin-film format [11]. Amorphous IGZO has been an attractive material due to its ease of fabrication and the fact that it is electrically similar to c-IGZO.

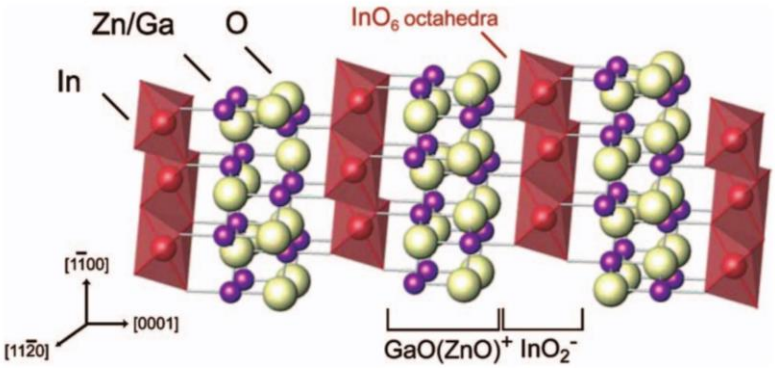


Figure 1: Structure of $IGZO_4$ crystal [8]

IGZO does not utilize standard silicon process technology where dopants are introduced into the substrate to create semiconductor devices. IGZO inherently has oxygen vacancies which act as donors. Due to the lack of free hole carriers low off-state currents can be realized [13]; this is due to the lack of a continuum of hole states to facilitate valance band transport. Thus, p-channel devices have not been made with IGZO, or any other metal-oxide for that matter.

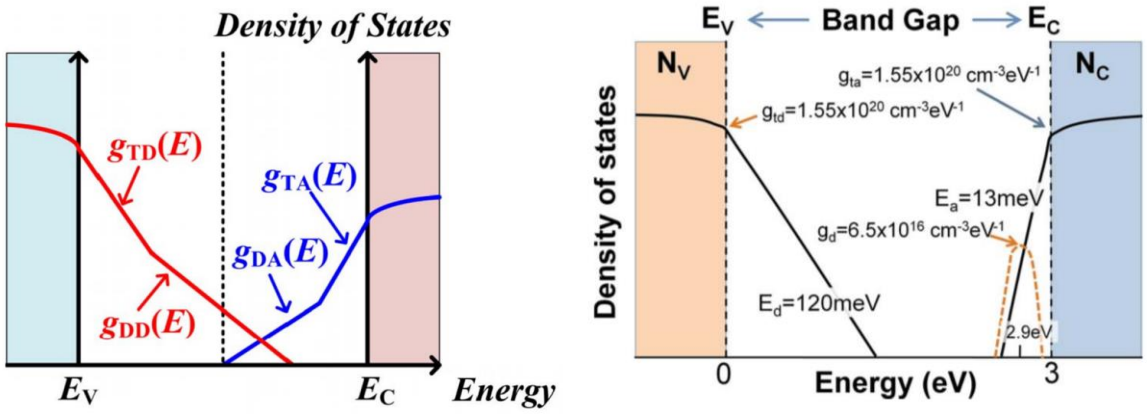
2.2 Modeling and Simulation of IGZO TFTs

The subgap density of states (DOS) consists of distributions defined as acceptor-like tail states, donor-like tail states, acceptor-like deep traps, and donor-like deep traps designated as $g_{TA}(E)$, $g_{TD}(E)$, $g_{DA}(E)$, and $g_{DD}(E)$, respectively, as shown in Figure 2 [13]. These DOS can be modeled as [13]:

$$g_A(E) = g_{DA}(E) + g_{TA}(E) = N_{DA} * \exp\left(\frac{E-E_C}{kT_{DA}}\right) + N_{TA} * \exp\left(\frac{E-E_C}{kT_{TA}}\right) \quad (1)$$

$$g_D(E) = g_{DD}(E) + g_{TD}(E) = N_{DD} * \exp\left(\frac{E_V-E}{kT_{DA}}\right) + N_{TA} * \exp\left(\frac{E_V-E}{kT_{TA}}\right) \quad (2)$$

where $g_A(E)$ is the acceptor-like DOS, $g_D(E)$ is the donor-like DOS, E_C is the conduction band, E_V is the valence band, N_{TA} is the density of acceptor-like tail trap states at E_C, N_{DA} is the density of acceptor-like deep trap states at E_C, N_{TD} is the density of donor-like tail trap states at E_V, N_{DD} is the density of donor-like deep trap states at E_V, kT_{TA} is the characteristic energy for acceptor-like tail trap states, kT_{DA} is the characteristic energy for acceptor-like deep trap states, kT_{TD} is the characteristic energy for donor-like tail trap states, and kT_{DD} is the characteristic energy for donor-like deep trap states [13].



(a) **(b)**

Figure 2: (a) General density of the deep and tail states in the bandgap of IGZO [13]. (b) Density of states in the bandgap utilized in Silvaco Atlas™ simulation with a mean energy of the oxygen vacancies at 2.9 eV.

Fung et al. compare experimental IGZO TFTs to simulated IGZO TFTs utilizing the well-established IGZO TFT model in Silvaco Atlas™ with Ti source/drain contacts [14]. The bandgap used in the model is shown in Figure 2b, with a Gaussian-distributed donor-like OV peak near the conduction band edge and a mean energy of 2.9 eV; this is because the IGZO exhibits a relaxed structure after an annealing process causing the energy level of the OV states to be located near the conduction band minimum. Based on the parameters in Table 1 the simulated IGZO came out to be very close to that of the actual devices as shown in Figure 3 [14].

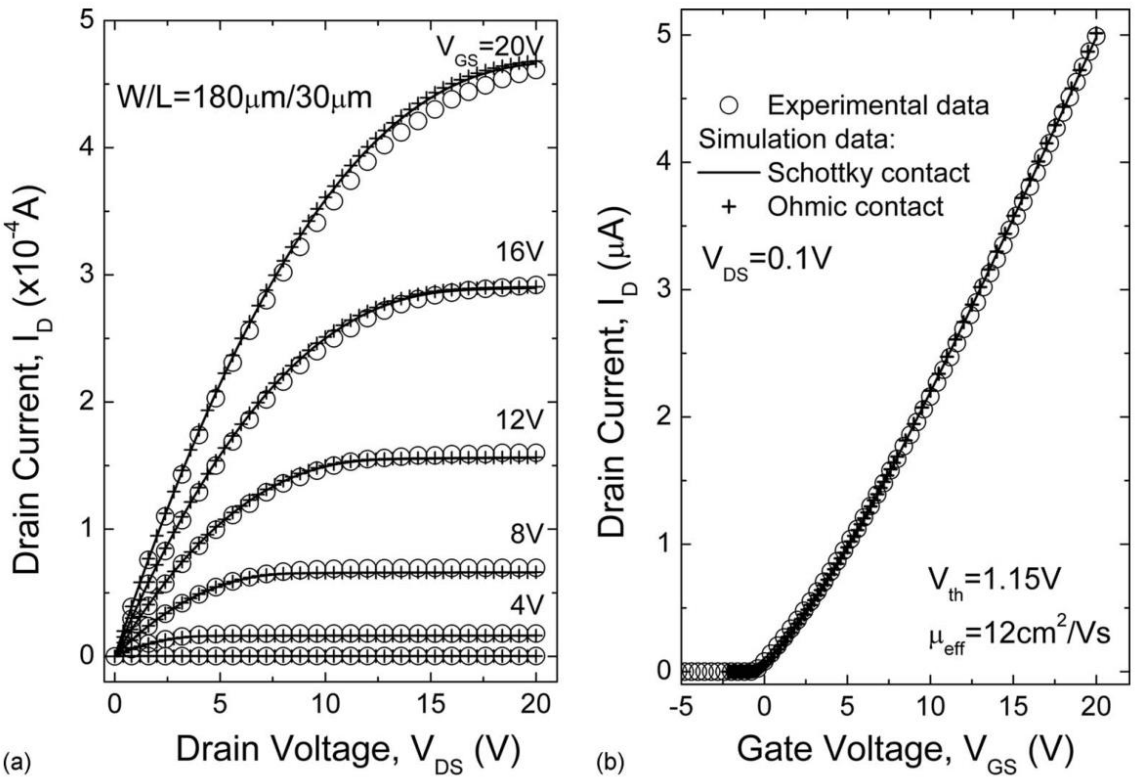


Figure 3: Overlay of the I_DV_G (a) and I_DV_D (b) characteristics of IGZO TFTs and Silvaco Atlas™ simulation with parameters defined in Table 1 [14].

Table 1: Simulation parameters and a-IGZO TFT properties [14]

Symbol	Value	Unit	Description
N_c	5×10^{18}	cm^{-3}	Effective conduction band DOS
N_v	5×10^{18}	cm^{-3}	Effective valence band DOS
g_{ta}	1.55×10^{20}	$cm^{-3}\ eV^{-1}$	Density of tail states at $E=E_C$
g_{td}	1.55×10^{20}	$cm^{-3}\ eV^{-1}$	Density of tail states at $E=E_V$
E_a	13	meV	Conduction-band-tail slope
E_d	120	meV	Valence-band-tail slope
E_g	3.05	eV	Bandgap
χ	4.16	eV	Electronic affinity
ε	10		Permittivity
μ_n	15	$cm^2/V\ s$	Band mobility (electron)
μ_p	0.1	$cm^2/V\ s$	Band mobility (hole)
m_c	0.34	m_e	Conduction band effective mass
g_d	6.5×10^{16}	$cm^{-3}\ eV^{-1}$	Peak of OV states
λ	2.9	eV	Mean energy of OV states
σ	0.1	eV	Standard deviation of OV states
		a-IGZO TFT properties	
μ_{eff}	12	$cm^2/V\ s$	Field-effect mobility
V_{th}	1.15	V	Threshold voltage
S	0.13	V/dec	Subthreshold swing
I_{off}	$<10^{-14}$	A	Off current
	10^{10}		On/off current ratio

Hsieh et al. considered only the acceptor-like states because IGZO is an n-type semiconductor and operates in the n-channel mode. The DOS is then broken into two parts, which include an exponential DOS and a Gaussian DOS [14]. These were put together to model the acceptor-like subgap DOS as [10]

$$g_A(E) = N_{TA} * \exp\left(\frac{E-E_C}{W_{TA}}\right) + N_{GA} * \exp\left(-\left(\frac{E_{GA}-E}{W_{GA}}\right)^2\right) \quad (3)$$

where N_{GA} is the total DOS, W_{GA} and W_{TA} are the characteristic decay energies, and E_{GA} is the Gaussian distribution peak energy [10]. The sub-threshold swing is related to the trap density in the bandgap at the Fermi level (D_{sg}) shown as

$$S = ln10 * \frac{k_B T}{q}(1 + \frac{qD_{sg}}{C_G}) \quad (4)$$

where C_G is the gate capacitance. It has also been reported that incorporating hydrogen into IGZO creates shallow donor states [3], which makes the channel more conductive.

Table 2: Electrical properties of three IGZO TFT compositions [5]

TTFT / Property	A-type	B-type	C-type
Composition ratio (In:Ga:Zn, at%)	2:1:2	1:1:1	2:2:1
Post-annealing temperature (°C)	~ 200	~ 300	~ 400
V_{on} (V)	–1.26	0.21	0.42
V_{th} (V)	2.06	4.76	5.17
μ_{sat} (cm^2/Vs)	18.09	7.90	9.12
Subthreshold swing	0.20	0.26	0.29

Table 2 shows that the composition of IGZO greatly affects the electrical properties especially the mobility. It was also found that the higher the concentration of Ga the more robust the TFT, which is due to there being a stronger binding of O atoms, in films with higher Ga content [5].

2.3 Annealing Conditions

One of the many ways to enhance the performance of IGZO is by annealing under specific gas ambient and temperature conditions. It was found that IGZO starts to form a nano-crystalline structure at 700 °C, which exhibits a poorer subthreshold swing than devices annealed at lower temperature, and this is attributed to the increase in the interface and bulk trap densities [16]. A low-temperature anneal (T < 400 °C) is typically utilized [17]. In a comparison of the ambient conditions for annealing IGZO, nitrogen and vacuum anneals resulted in a high conductance (metallic like) in the IGZO, presumably due to a higher carrier concentration from the increased oxygen vacancies. On the other hand, annealing IGZO in oxidizing ambient conditions results in a carrier concentration suitable for device operation, thus providing an appropriate level of oxygen-vacancy donors [18]. Nguyen et al. showed via XPS that there are more oxygen vacancies in N_2 annealed films and fewer in oxygen annealed films [19].

2.4 Back-Channel Passivation Materials

Passivating IGZO is key to making electrically and environmentally stable TFTs. C. Tu et al. and J. Li et al. reported that a passivation layer can improve the stability of IGZO TFTs [20, 21]. There are many materials which can be utilized to fulfill this requirement, but some are more adequate than others for the task. The industrial solutions to passivating the top surface of IGZO TFTs has not been reported as of yet [22], thus studying potential passivation materials is essential. To make it easier to compare all the passivation layers the characteristics of each passivation layer are compiled into Table 3.

Silicon oxide and nitride have been investigated as passivation materials. PECVD silicon dioxide as a passivation layer for IGZO has been known to create poor TFTs

because the channel becomes too conductive, presumably due to the presence of hydrogen, resulting in a degradation in subthreshold operation [23]. Kang et al. reported on passivating IGZO with PECVD SiN_x followed by a vacuum anneal; their results show an improvement in electrical performance with increasing anneal time [24]. Other studies have contradictory results. Chung et al. reported that IGZO TFTs passivated with SiO_x resulted in better device performance than SiN_x as the passivation material due to the presence of hydrogen causing an increase in the trap densities [25].

Table 3: List of reported IGZO characteristics for various passivation materials

Passivation	V_T *(V)*	μ_{fe} *(cm²/V·s)*	*SS (mV/dec)*	*Reference*
SiO_x	7.0	10.4	520	[23]
SiO_x	2.9	5.4	1500	[20]
SiO_x	1.49	5.02	290	[25]
SiO_2	0.1	0.8	330	[24]
ALD Al_2O_3	0.4	8.0	100	[26]
SiN_x	NA	22.2	150	[24]
SiN_x	0.65	7.78	650	[25]
Al_2O_3	NA	8.5	>200	[27]
Ga_2O_3	NA	7.5	>200	[27]
PVP	NA	16.5	~200	[27]
Parylene	NA	13.4	~200	[27]
Photoresist	NA	12.5	~200	[27]
Al_2O_3	-2.92	11.14	230	[28]
SU-8	NA	61	280	[29]
Y_2O_3	-1.0	12.1	140	[9]

A common passivation layer is atomic layer deposition (ALD) aluminum oxide (alumina or Al_2O_3). This material exhibits small leakage current below 10^{-7} A/cm^2 and a breakdown field of 3.5 MV/cm. The Al_2O_3 passivated IGZO TFTs are enhancement mode devices with a relatively high field effect mobility [26]. ALD-alumina was also found to increase the stability of the device by suppressing gas absorption [28, 31], and decreasing photo-excitation [31]. Organic polymers, such as have also been shown to improve

environmental and bias stability of IGZO TFTs, and reduce hysteresis (sweep up/down characteristic shift), without significant degradation of the electrical characteristics [27,30].

Other metal-oxide compositions have been investigated as passivation materials. Incorporating nitrogen into IGZO by reactive sputtering following deposition of the channel layer was shown to improve the electrical characteristics of the device in atmosphere and under gate bias stress [7]. IGZO:N also acts as a UV barrier, which makes it a viable light-blocking material. Another passivation layer is Zinc-Tin-Silicon-Oxide (ZTSO) was investigated by Sundholm et al. ZTSO provided a negative shift, indicating charge accumulation on the back side of the channel and severe distortion caused by increased surface states [32]. Yttrium oxide (Y_2O_3) is another passivation material studied for IGZO TFT stability, and shown to improve tolerance to constant current stress (CCS), and negative bias light illumination stability (NBLS).

2.5 Summary of IGZO TFTs

Reports show that composition, annealing conditions, and the various passivation materials greatly affect the electrical properties of IGZO. Overall performance enhancement for IGZO TFTs requires a low temperature anneal and as a promising passivation layer material, such as Al_2O_3. The next chapter discusses the fabrication and preliminary research into the anneal conditions of IGZO.

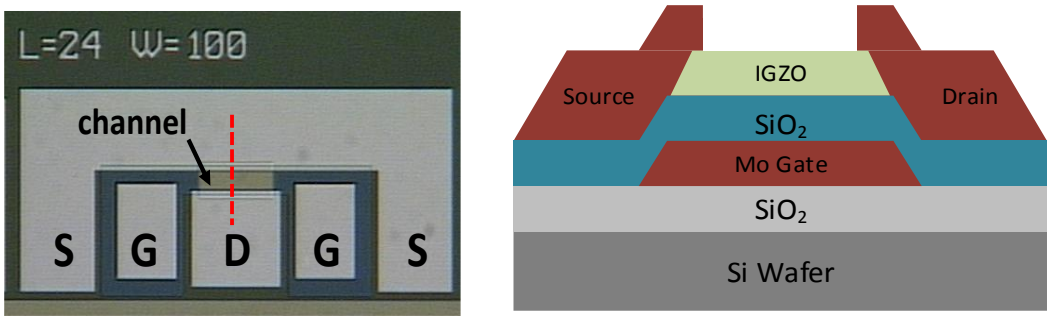
CHAPTER 3

PRELIMINARY RESEARCH

3.1 Fabrication

The impact of annealing IGZO has previously been studied at RIT [33]. For those experiments the contacts were either Mo or Al, and the wafers were either pre-metal or post-metal annealed. The various gas ambients included air, oxygen, nitrogen, forming gas (5% H_2 in N_2), and vacuum.

The wafers are fabricated on SiO_2 on a silicon wafer to emulate a glass wafer. A 250 nm layer of Mo is deposited and patterned for the bottom gate electrode. Utilizing PECVD TEOS at 390 °C a 100nm SiO_2 is deposited on the bottom-gate for the gate dielectric. A 65 nm film of IGZO is then RF sputtered onto the gate dielectric in a 7% O_2 by flow in an Ar ambient. The IGZO is then patterned and the mesa structure is then etched in a dilute HCL solution. Pre-metal annealing was then performed on some of the wafers. The source and drain metal was defined by a lift-off process; LOR 5A is coated onto the wafers followed by a photoresist coating and then exposed. The source drain metal is either sputtered Mo or evaporated Al. After the metal is deposited it is then lifted off. It should be noted that Al was evaporated on top of the Mo contacts to prevent the Mo from oxidizing in the subsequent anneals. After the metal lift-off some wafers were annealed (post-metal anneal). A topographical view of the fabricated structure can be seen in Figure 4.



(a) **(b)**

Figure 4: (a) Micrograph of a bottom-gate IGZO TFT with source (S), gate (G), drain (D), and channel labeled with cross section along the dotted line shown in (b). The source and drain are either Mo or Al, and the channel length is 24 µm and the channel width is 100 µm.

The mask defined channel lengths between the source and drain vary from 6 to 48 µm, and the purpose of creating such large contacts is to allow probe tips to make a good contact to test the TFT devices. Transfer characteristics were measured with a drain bias of 0.1 V and 10 V.

3.2 Preliminary Results and Discussion

Figure 5 shows the Silvaco Atlas™ simulation of the energy band diagram of various metal contacts to IGZO, and this is based on a well-established model developed with Ti source/drain contacts [14]. The simulation solved for a zero-bias initial condition, with a vertical cut taken through the source contact (X = 0 µm). Ti has a small metal-semicondutor barrier relative to IGZO, which makes for an ohmic behavior of the source/drain electrodes that results in minimal impact on the transistor operation [14]. According to the difference in the workfunctions shown in Figure 5 suggests that Mo forms a Schottky contact, and Al forms an ohmic contact to IGZO.

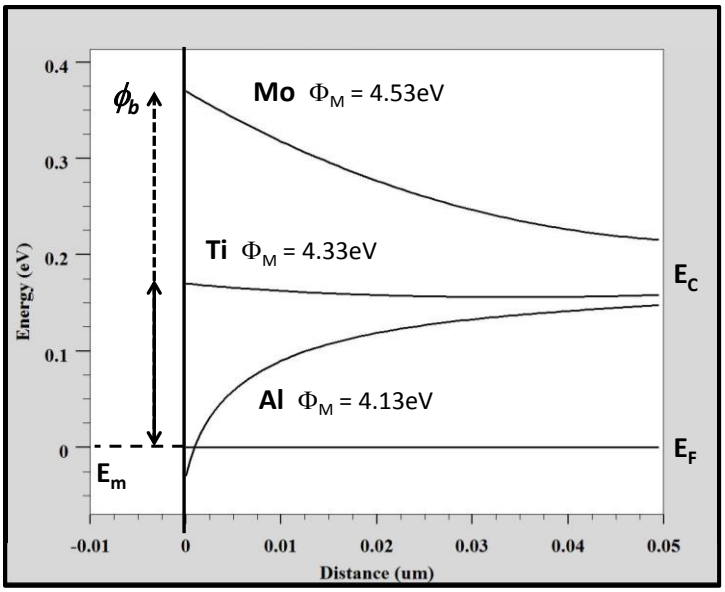


Figure 5: Energy band diagram generated by Silvaco Atlas™ showing the energy barriers associated with IGZO metal contacts utilizing a documented model [14]. The workfunction of Al should ideally provide an ohmic contact, whereas the Mo contact appears to present a significant source barrier (ϕ_b). Non-idealities such as M-S interface states are not considered. Note that the conduction band energy (EC) does not line up for each case due to additional influence (band-bending) from the Mo gate metal workfunction.

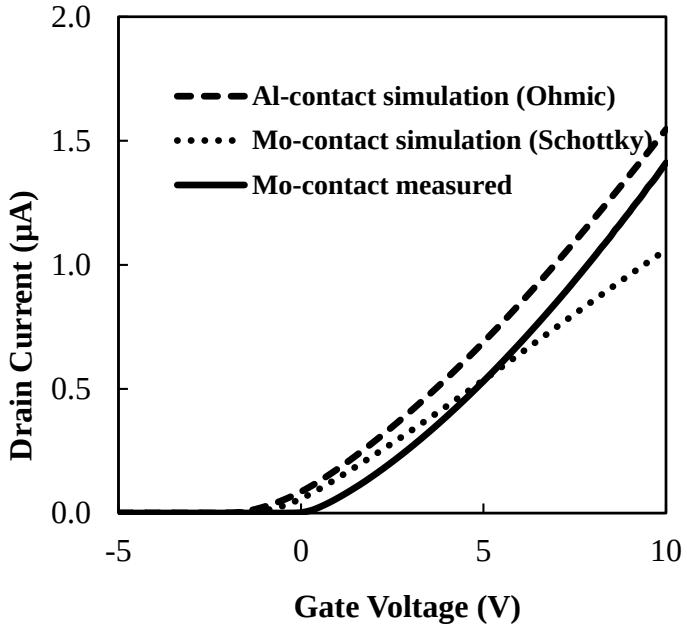


Figure 6: Overlay of a measured linear-mode (V_{DS} = 0.1 V) transfer characteristic from the device shown in Figure 8 (solid line), along with simulated characteristics consistent with M-S contact conditions for Al (dashed line) and Mo (dotted line) shown in Figure 5. The TFT channel dimensions were L = 24 µm & W = 100 µm.

The transfer characteristic in Figure 6 show that the actual measured Mo-contact device exhibits operation that is more consistent with the Al-contact simulation, which suggests that the interpretation of ohmic source/drain contacts is correct. The match between the measured characteristic and the simulated characteristic under ohmic contact conditions in the on-state is reasonable with a lateral shift of ~ 0.8 V.

IGZO thin-film samples and devices that were annealed at 400 °C in vacuum became very conductive with a measured sheet resistance Rs ~ 8 kΩ/□, or resistivity $\rho \sim 0.04\ \Omega\cdot$cm, confirming the importance of an oxidizing ambient. Similar results were obtained for samples annealed in N_2 without any exposure to air or O_2. Devices fabricated without any thermal anneal treatment exhibited very poor electrical behavior with exceedingly high contact and/or channel resistance. Results obtained from a pre-metal anneal treatment in air ambient (45% humidity, class 1000 cleanroom) at 350 °C for 1 hr, performed immediately after the IGZO mesa definition are shown in Figure 7. The transfer characteristics of Al-contact and Mo-contact devices demonstrate almost perfect overlay. While the TFT performance for this treatment does not demonstrate impressive channel mobility ($\mu_{sat} < 1$ cm^2/V·s) and subthreshold swing (SS ~ 550 mV/dec), the characteristic overlay of the two different source/drain contact metals indicates that the channel regions of the devices are essentially the same, and that the difference between the influence of the evaporated Al or sputtered Mo processes on the channel behavior of pre-metal annealed samples is insignificant. The contact behavior appears to be dominated by metal-semiconductor interface states which facilitate carrier injection, with no indication of non-ohmic behavior by either the Al-contact or Mo-contact devices.

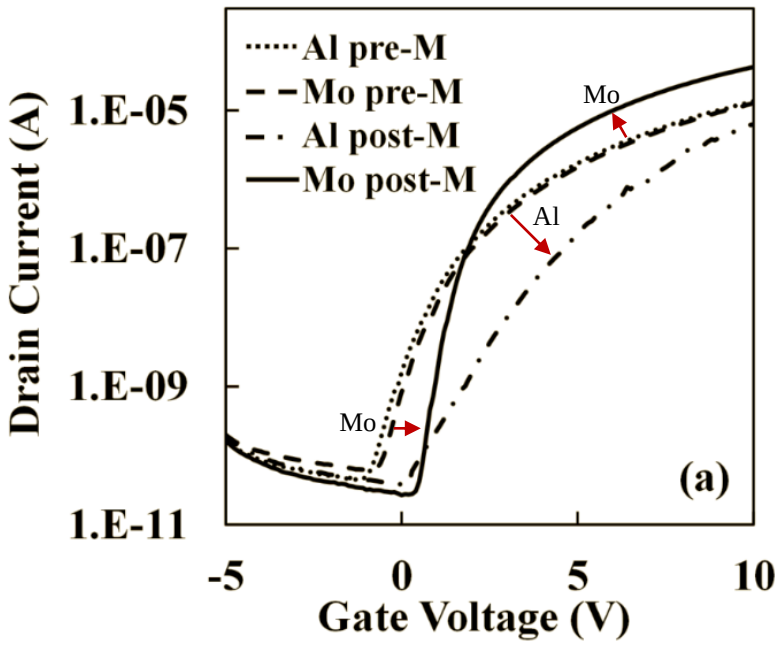


Figure 7: Overlay of transfer characteristic for Mo-contact and Al-contact devices that either had pre-metal or post-metal air anneal at 350 °C for 1 hr. The TFT channel dimensions are L = 12 µm & W = 100 µm.

The influence of a post-metal 350 °C anneal treatment on device performance is also shown by the arrows in Figure 7. The Mo-contact device demonstrated improvements over the pre-metal anneal both in the on-state (μ_{sat} ~ 3.2 $cm^2/V \cdot s$) and off-state (SS ~250 mV/dec) operation. Additionally, the characteristic is right-shifted, or more enhancement-mode, with slight hysteresis between the high and low drain bias characteristics noted. While the Mo-contacts to the IGZO facilitate electron injection, changes in the density and energy distributions of the metal-semiconductor interface defects appear to be responsible for the differences observed in the pre-metal and post-metal anneal treatments. Post-metal anneal Al-contact devices resulted in significant degradation in contact behavior. It was observed to have virtually no on-state current in the low V_{DS} characteristic, whereas the saturation characteristic showed a much higher SS and was right-shifted. This result was expected due to the formation of interfacial AlO_X layer during the annealing process, which acted as a barrier preventing current flow. Additional

experiments on Al-contact device with post-metal annealing in oxidizing ambient conditions demonstrated similar results.

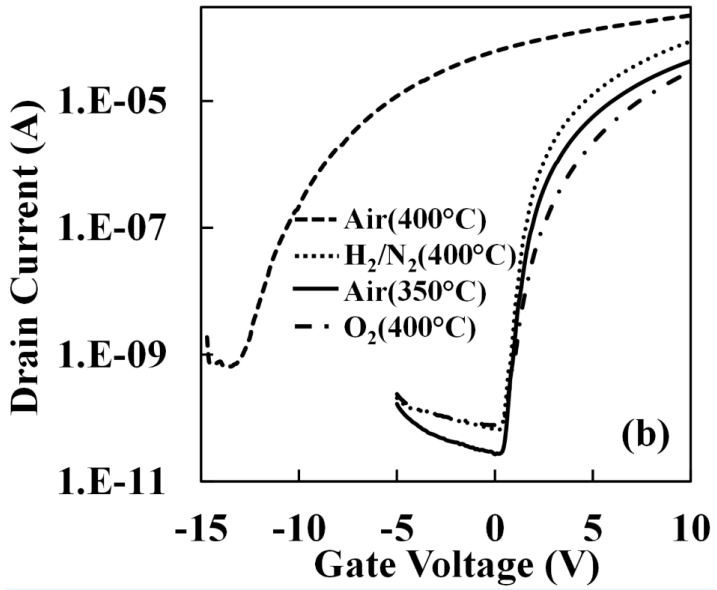


Figure 8: Overlay of saturation-mode transfer characteristics for Mo-contact post-metal anneal treatments: Air at 350 °C for 1 h; air at 400 °C for 30 min; O_2 at 400 °C for 30 min; H_2/N_2 at 400 °C for 30 min. Ramp-down conditions were in air ambient for each. The TFT channel dimensions are L =12 µm & W = 100 µm.

Figure 8 shows the saturation-mode transfer characteristics of Mo-contact TFTs which received different post-metal anneal treatments each with a ramp-down in air. The ramp-down rate was approximately constant, decreasing from 400 °C to 150 °C over 3 hr. The 400 °C anneal in air for 30 min was an aggressive oxidation treatment which resulted in a more depletion mode device with significant loss of gate control. The device did, however, have an enhanced current drive over the other treatments, but this is due to the conductivity of the IGZO rather than the transconductance. Ideally this reduces the oxygen vacancies, but this treatment seemed to create additional defects thus increasing the free carrier concentration. Other treatments included O_2 and forming gas (5% H_2 in N_2) at 400 °C for 30 min; extracted parameters are shown in Table 4.

Table 4: Parameters for Mo-contact post-metal anneal treatments in air, O_2, H_2/N_2, and N_2.

	V_T (V)	μ_{sat} ($cm^2/V{\cdot}s$)	*SS* (mV/dec)
Room Air (350 °C)	1.2	3.2	260
O_2 (400 °C)	1.5	2.4	420
H_2/N_2 (400 °C)	1.2	6.7	250

Annealing at 350 °C in an air ambient which contains water vapor (i.e. volume [H_2O] ~ 1.3% @ 45%RH) has been shown to be effective at reducing oxygen vacancy defects. The result for the air anneal at 400 °C for 30 min appears to be due to the excess oxygen incorporation into the channel. The post-metal O_2 anneal at 400 °C for 30 min demonstrated degradation in both SS and on-state performance in comparison to the 350 °C air anneal treatment result. This degradation is distinctly different from the aforementioned anneal in air at 400 °C for 30 min, and is attributed to enhanced suppression of oxygen vacancy donors. On the other hand, the post-metal H_2/N_2 anneal shows improvement, exhibiting a steeper SS and an increase in the on-state current. This suggests that the oxidation which occurs during the ramp-down in air following the H_2/N_2 anneal is closer to the optimum conditions; thus, time and temperature in air ambient are important in establishing improved electrical behavior.

The importance of H_2 in the forming gas ambient was not fully understood, so annealing in pure N_2 was studied for comparison. The electrical characteristics of a Mo-contact device with a post-metal N_2 anneal at 400 °C followed by an air ramp-down are shown in Figure 9. The N_2 anneal demonstrates a left-shift in V_T compared to the forming gas anneal treatment. However, the channel mobility and SS show improvements over the results listed in Table 4. These devices demonstrated voltage shifts in the transfer

characteristic observed during aging as well as hysteresis in the up/down sweeps as seen in Figure 9 [34].

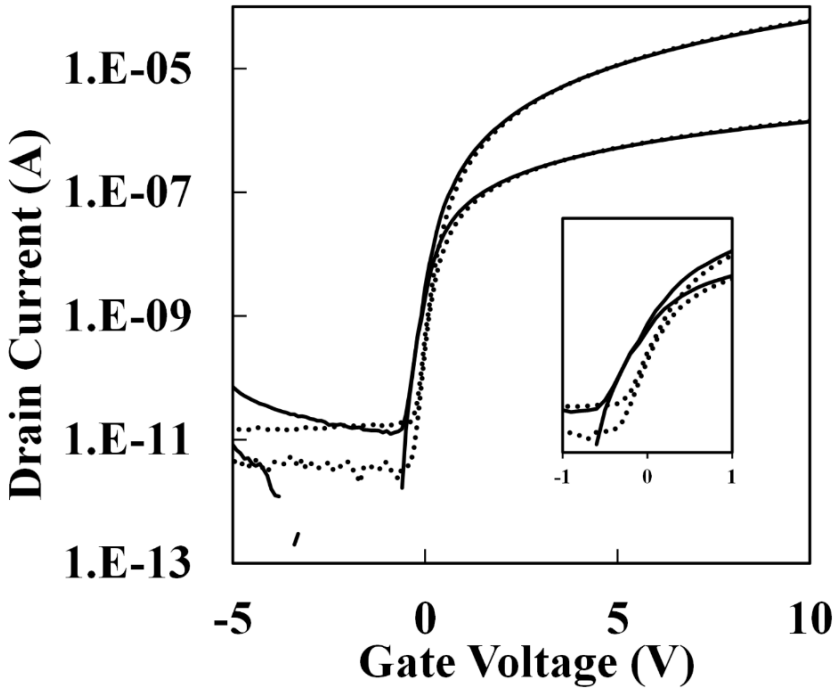


Figure 9: I_D-V_G transfer characteristic overlays of Mo-contact device with a post-metal N_2 anneal and air ramp-down. The inset shows up/down V_G sweep hysteresis. The TFT dimensions are L =12 µm & W = 100 µm.

3.3 Thickness Variation Results

The three IGZO thicknesses looked at were 5, 10, 30 nm. Each was annealed with the same annealing conditions of a N_2 ambient at 400 °C for 1 hr and an O_2 ramp down. The results of those unpassivated devices are shown below.

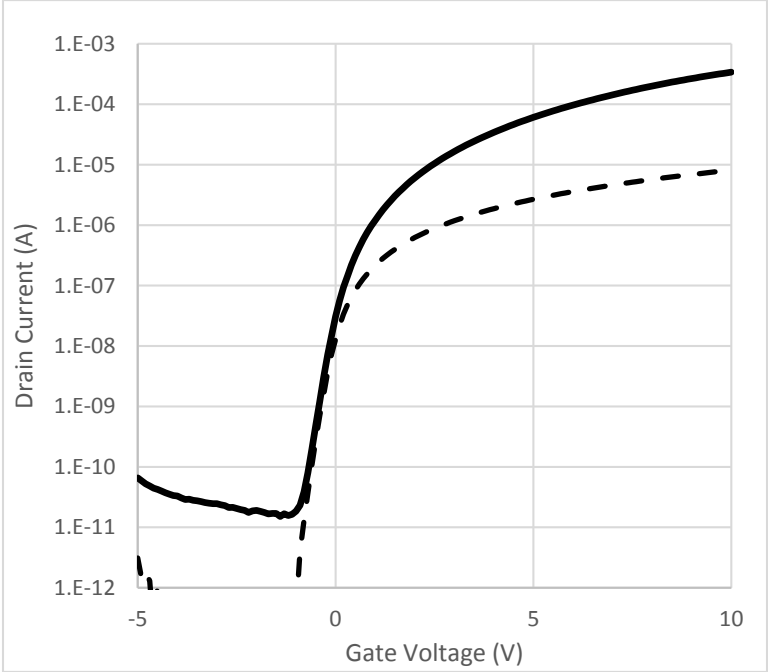


Figure 10: I_D-V_G transfer characteristic overlays of 5 nm thick IGZO with an anneal at 400 °C for 1 hr in N_2 with an O_2 ramp down.

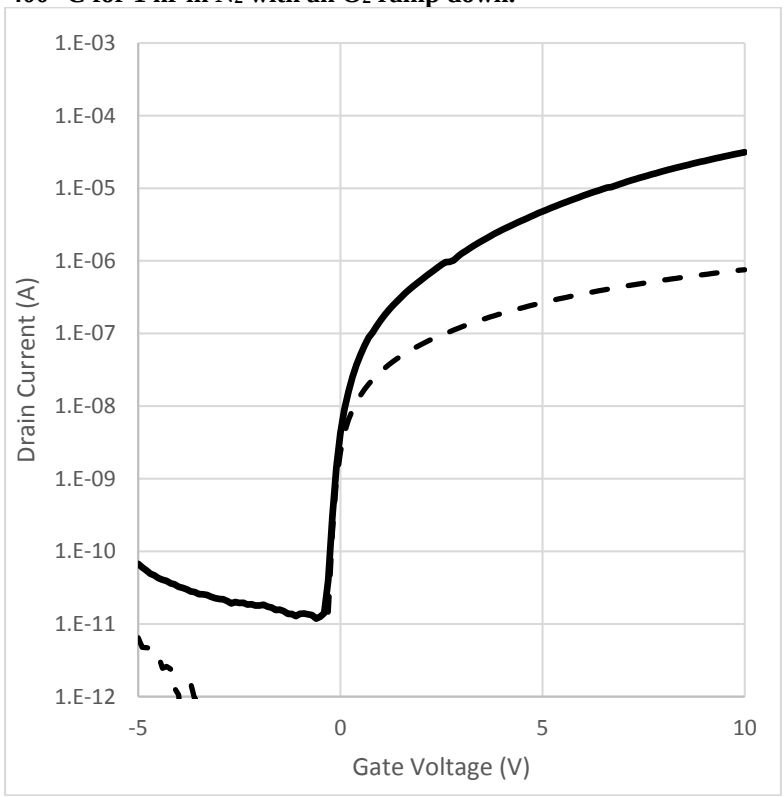


Figure 11: I_D-V_G transfer characteristic overlays of 10 nm thick IGZO with an anneal at 400 °C for 1 hr in N_2 with an O_2 ramp down.

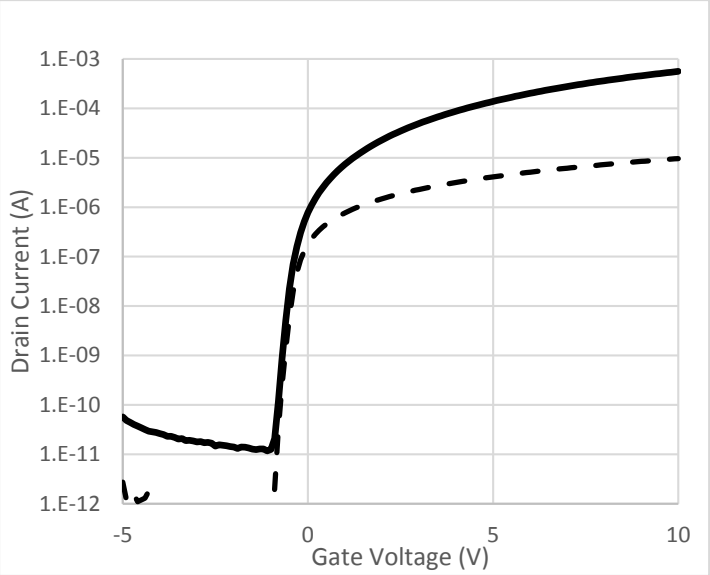


Figure 12: I_D-V_G transfer characteristic overlays of 30 nm thick IGZO with an anneal at 400 °C for 1 hr in N_2 with an O_2 ramp down.

The device I_D-V_G transfer curves in Figures 10-12 are the best case devices found with the extracted parameters shown in Table 5. The 30 nm thick IGZO exhibits a better SS, mobility, and current drive than the 5 or 10 nm thicknesses. Based on the disparities between the extracted parameters means that there is an optimal anneal condition for each IGZO thickness. These optimal anneals have yet to be determined thus far.

Table 5: Extracted parameters for 5, 10, and 30 nm thick IGZO TFTs

IGZO Thickness	V_T (V)	μ_{sat} (cm^2/V·s)	*SS* (mV/dec)
5 nm	-0.1	11.6	250
10 nm	-0.3	8.3	150
30 nm	-0.6	17.4	<150

3.4 Initial Passivation Material Results

The initial results of electron-beam evaporated alumina as a back-channel passivation material were not promising, with initial IGZO resistivity $\rho \sim 0.03\ \Omega\cdot$cm. The devices were annealed in N_2 ambient with a ramp-down in air, which was the best-case recipe for unpassivated devices; however, the electronic properties of IGZO were not suitable due to

the impedance of transport of oxidants through the alumina to IGZO. Annealing in an air ambient at 400 °C for 30 min provided an effective exposure to an oxidizing ambient; the devices exhibited improved stability over time as well as suppressed hysteresis. This is likely due to improved oxidant transport through the alumina passivation layer, providing a near-optimum degree of oxidation. Figure 13 shows an overlay of multiple (4) up/down V_G sweeps on a device after one month of storage in air ambient. There was no observable voltage shift compared to the initial results after annealing, and hysteresis is suppressed. Compared to devices without back-channel passivation there was a slight right-shift in the transfer characteristics (V_T ~ 0.3 V) and a decrease in device performance, with μ_{sat} ~ 5 $cm^2/V{\cdot}s$ and SS ~ 300 mV/dec.

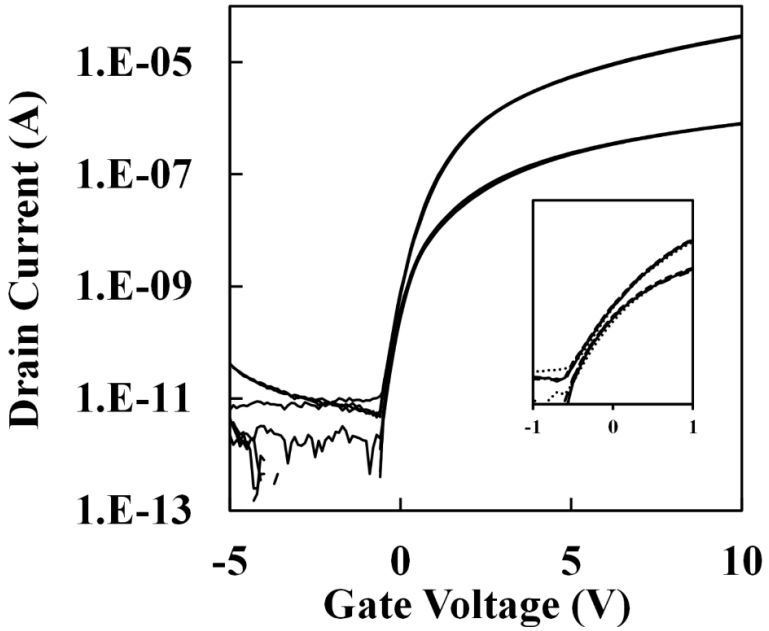


Figure 13: Mo-contact device with alumina back-channel passivation exhibiting suppressed hysteresis over multiple up/down sweeps

The initial results of B-based bisbenzocyclobutene-based (BCB) resin as a passivation layer material showed promising results. The maximum recommended temperature for BCB annealing is 250 °C, therefore, BCB-passivated devices were annealed in air at 250 °C for 2 hr after the cure. The results depicted in Figure 14 show negligible hysteresis with

dual-sweep transfer characteristics. Stability testing for BCB-passivated devices is currently in progress.

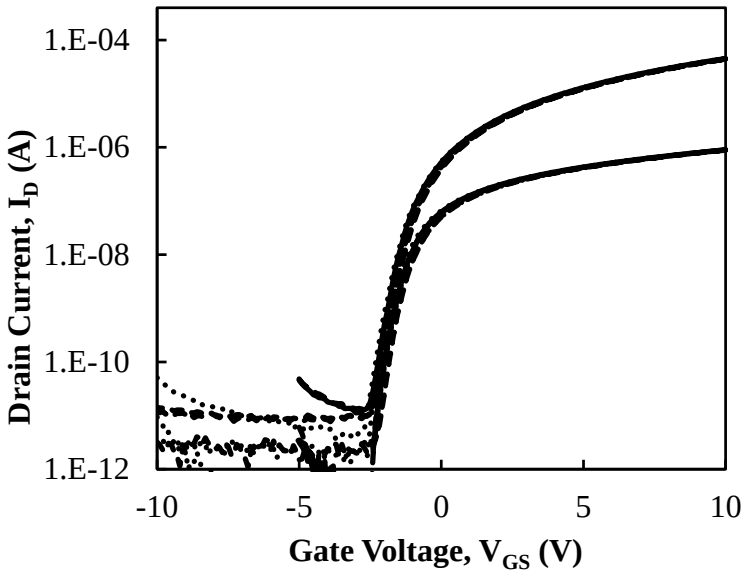


Figure 14: Overlay transfer characteristic of a BCB passivated IGZO TFT of multiple up/down V_G sweeps with suppressed hysteresis. The dimensions are L = 24 µm and W = 100 µm.

Chapter 4

FABRICATION

4.1 Device Fabrication and Design

The wafers are fabricated on oxidized silicon wafers with about 650 nm of SiO_2 to emulate a glass substrate, and glass wafers (Corning Eagle XG glass). The first layer is 250 nm of sputtered Mo (1000 W, 1000 sec, 2.6 mT), which is then patterned to form the bottom gate. Utilizing PECVD TEOS at 390 °C a 100nm SiO_2 is deposited on the bottom-gate for the gate dielectric. IGZO is then RF sputtered onto the gate dielectric utilizing an Applied Materials Centura system with a 12.8" target ($InGaZnO_4$) and 7% O_2 by flow in an Ar ambient, with thicknesses of 5, 10, 30, and 50 nm. The IGZO mesa is then patterned and etched in a dilute HCL solution to form the channel region. The source and drain contact metal is defined by a lift-off process because metal etchants will etch IGZO and contaminate the bath; the wafers are primed with HMDS and coated with lift-off resist (LOR 5A), then photoresist. The source/drain regions are exposed and developed, followed by a Mo sputter of the source/drain contacts. Aluminum is then evaporated prior to the lift-off process as a protective layer to avoid Mo oxidation during subsequent annealing. The Mo/Al bilayer is then lifted-off in Remover-PG with ultrasonic energy. The passivation layer is then applied; either Al_2O_3 was deposited via e-beam evaporation, or BCB was spin coated and oven cured. Contacts are then patterned and etched through the passivation layer using 10:1 BOE. The wafers were then broken into pieces and annealed, then subsequently tested. The full step-by-step process flow can be seen in Appendix A.

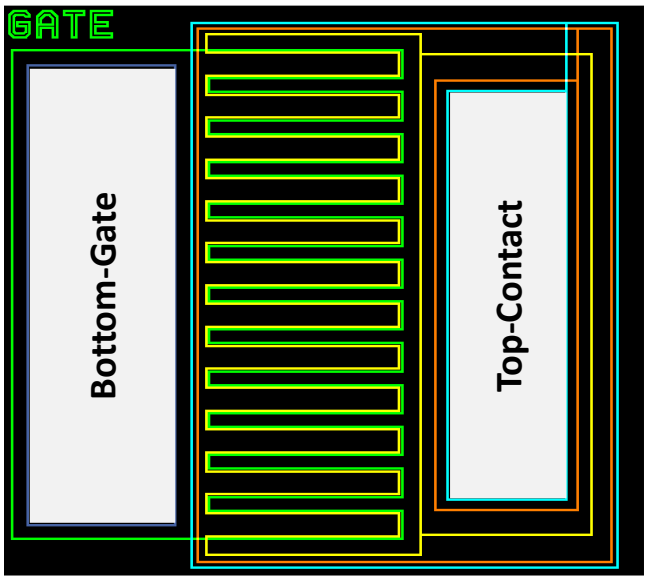


Figure 15: ICD layout, with twelve interdigitated fingers extending across the IGZO mesa. Each gated region has a width of 44 µm, and 5 µm side overlaps between the top-contact metal and the bottom-gate metal. The total gated area is ~ 0.002 cm^2.

The testchip design included both TFT and interdigitated capacitor (IDC) devices. The TFT structures have constant widths of 100 µm and varying lengths ranging from 6 µm to 48 µm in intervals of 6 µm. The cross-section of the passivated device is the same as that shown in Figure 4b but with a passivation layer covering the exposed IGZO.

While C-V analysis can be done directly on TFTs [35], the IDC was designed to be consistent with the TFT structure considering process exposure to the back-channel region, and overlap regions between the bottom-gate and top-contact (source/drain) electrodes. The IDC layout is shown in Figure 15, and this design ensures that the gated areas receive the same process treatments as the TFT channel region regardless of process options.

4.2 Process Integration Challenges

The addition of a passivation layer on the IGZO TFTs required modifications to the process flow. The alumina was etched in 10:1 BOE down to the Al source/drain and gate

contacts, which caused the Al surface to roughen (blackened) as shown in Figure 16. There was a concern that the Mo underneath the roughened Al will become oxidized during the passivation anneal and the yield was low; thus a new process integration strategy was needed.

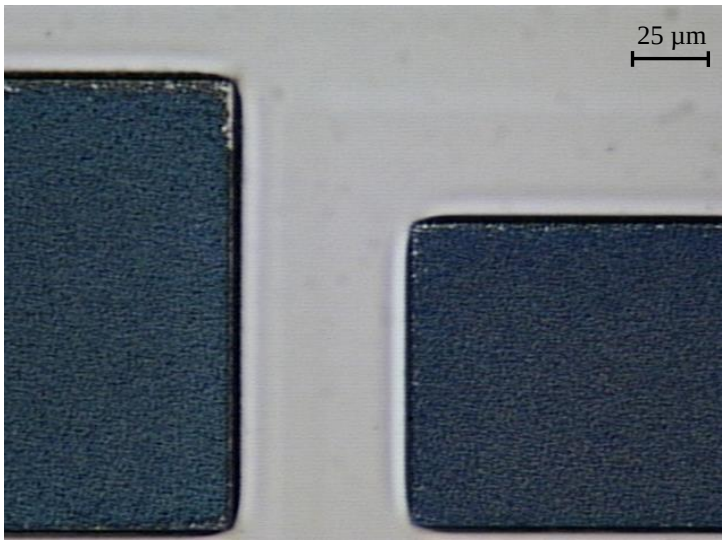


Figure 16: Al contacts after alumina etch in 10:1 BOE

Several approaches were made to solve the problem. One approach was to increase the thickness of the Mo layer and drop the Al that would be on top. The Mo was then tested to see if it would oxidized under the alumina layer. It was found that Mo does oxidize at temperatures T > 350 °C with only 50 nm of Al_2O_3 on top of it. It was also found that the etch rate of Mo in pad etch and 10:1 BOE is negligible, thus it would make for a suitable etch stop for etching alumina. The original sputter recipe (200 W) for Mo was adapted from an old stationary sputter onto LOR so as to not burn the resist. The previous process involved rotating the wafers resulting in a much lower deposition rate, and doubling the time to the current sputter process to double the thickness increased the stress such that the LOR underneath it started to delaminate causing the Mo to flake off. Different sputter recipes were investigated due to the uncertainty as to how much power could be utilized

before the resist would burn. The investigated sputter recipes are shown in Table 6. It was found that 1000 W does not burn the resist and the Mo lifted-off with no issues. The higher power (1000W) Mo sputter recipe was from the gate Mo sputter, and it was found to have the least amount of stress. This process resulted in poor devices.

Table 6: Mo sputter conditions and stress measurements

Material	Power (W)	Pressure (mTorr)	Time (sec)	Thickness (nm)	Stress (MPa)	Delamination
Mo	200	2.2	2040	100	_	Yes
Mo	500	2.6	1000	128	1809	Yes
Mo/Al/Mo	1000	2.6	200/300+300/200	270	504.6	No

Another approach to solve the oxidation problem was to create a tri-stack of Mo/Al/Mo for the source, drain, and gate contact regions. The sputter recipe is shown in Table 6 and utilizing the 1000 W recipe. The Al sputter was also at high power, but the amount of time the resist could withstand that high power was uncertain. Thus, the sputter was broken into two 300 sec portions, and between all of the sputters there was a ten minute cooling period to ensure the resist would not overheat.

Unfortunately, the tri-stack did not work as a solution to the etch problem, by comparing a device fabricated with and without the tri-stack as depicted in Figure 17 to Figure 9, respectively, shows evidence of there being a problem, which was due to the mask and not the actual layers. It was overlooked that using the same mask level to create the contact cut to the gate and deposit the tri-stack, and then again utilize it to make the passivation open contact cut through the alumina was not going to work. It was originally thought that the gate dielectric (TEOS) would protect the gate Mo, even if there was some over etch. It was overlooked that during the gate contact cut and source/drain lift-off lithography the LOR was undercut by the developer twice making it such that a ring of gate

Mo was exposed around the tri-stack, and this can be seen in Figure 18. This undercut was enhanced by the seemingly slow etch rate of alumina. The work-around to the issue was to do the passivation open lithography and etch of the tri-stack after annealing; this mitigated the chance of any Mo oxidizing, and allowed leniency with the wet etch.

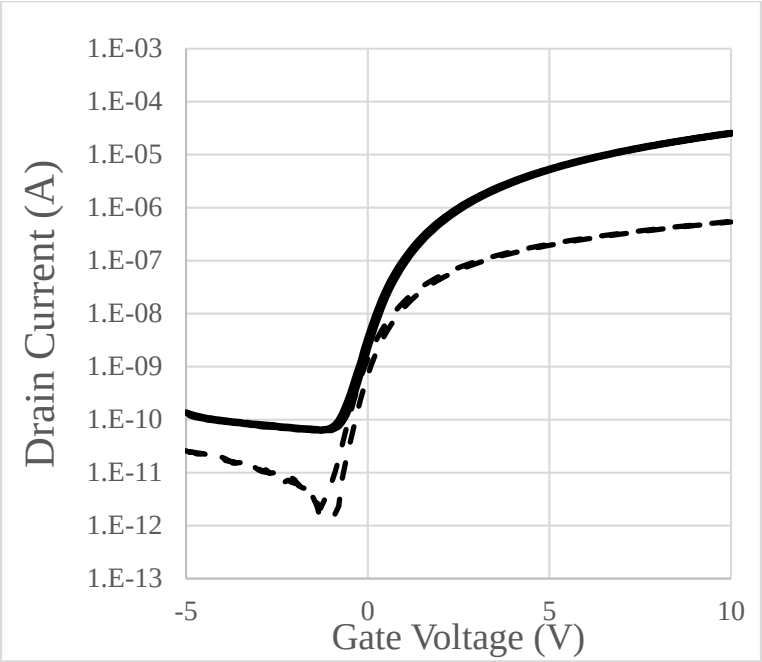


Figure 17: Overlay I_D-V_G transfer characteristic of an unpassivated IGZO TFT swept up and down with hysteresis. The dimensions are L = 24 µm and W = 100 µm.

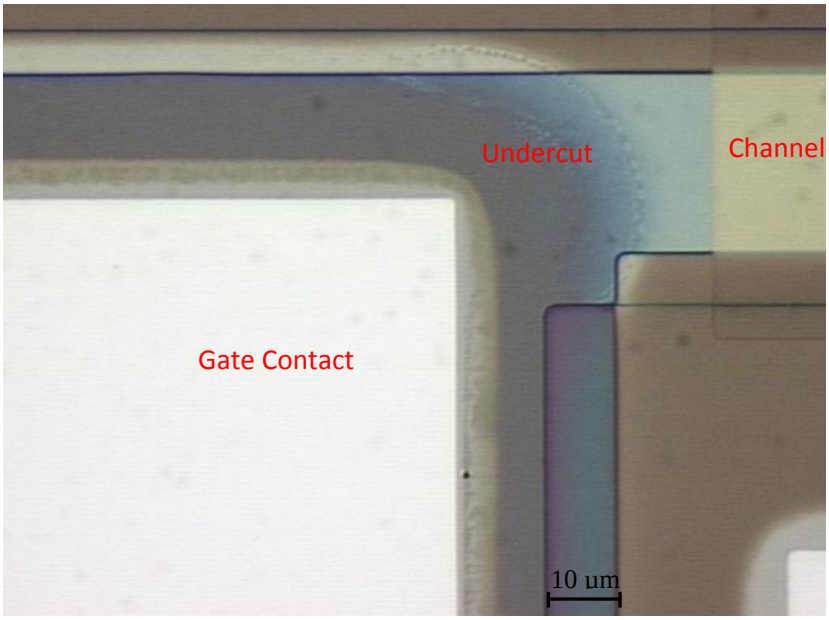


Figure 18: Undercut of the gate contacts during Al_2O_3 etch.

Chapter 5

ELECTRICAL CHARACTERIZATION AND ANALYSIS

The electrical characterization of devices were conducted with a HP-4145B parameter analyzer to acquire the I_D-V_G transfer characteristic measurement on TFTs with a constant channel width (W) of 100 μm and various lengths (L) ranging from 6 to 48 μm. Unless otherwise noted the measurements were taken with a low to high gate voltage sweep, medium integration, and low-drain bias and a high-drain bias of 0.1 V and 10 V respectively. C-V characteristics from the IDCs were obtained using a Materials Development Corporation (MDC) system with an HP 4284A precision LCR meter.

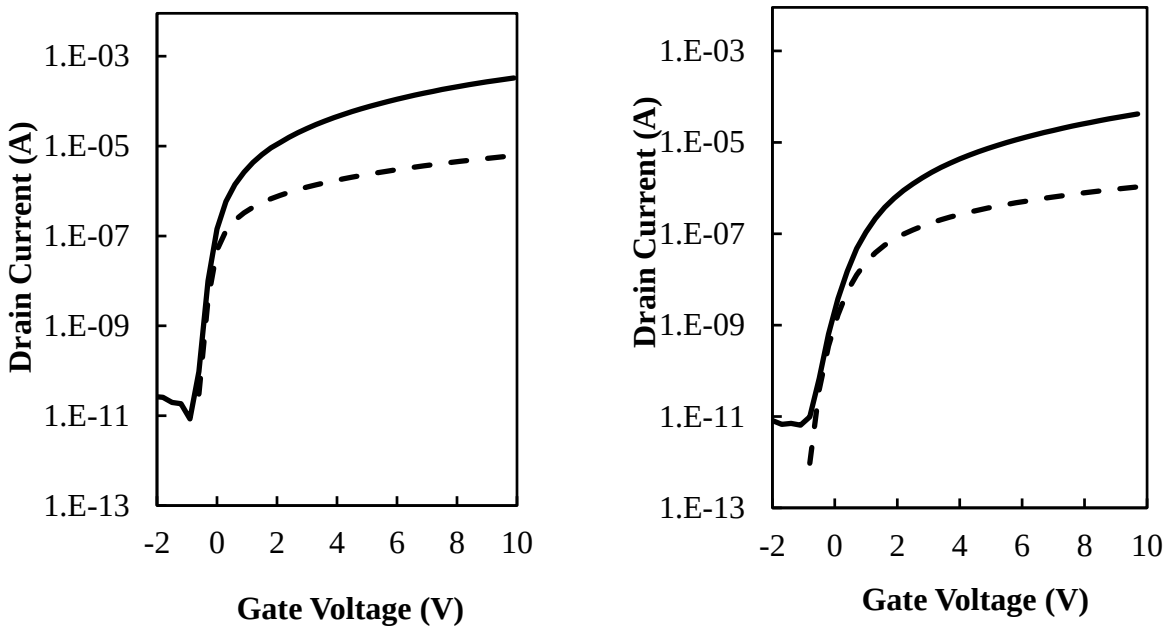


Figure 19: Measured I_D-V_G transfer characteristics of TFTs without (left) and with (right) alumina passivation, with channel dimensions of L = 24 μm & W = 100 μm. The TFT without alumina passivation exhibited the following operating parameters: μ_{ch} = 12 cm^2/V•sec, V_T = -0.3V, SS = 135 mV/dec. The TFT with alumina passivation exhibited the following operating parameters: μ_{ch} = 5 cm^2/V•sec, V_T = 0.3V, SS = 300 mV/dec.

Figure 19 depicts I_D-V_G curves of TFTs with and without alumina passivation. It was observed that the device without the passivation layer exhibits better device operation than the device with the alumina passivation layer. It was hypothesized that the device with passivation has some degree of defects causing the degraded performance. The origin of these defects were investigated through modeling and simulation.

5.1 Device Modeling

Silvaco® Atlas™ was used to simulate the TFT and IDC devices, and verify or establish material and device model parameters. Equations 5-7 are the density of defect states *g(E)* which represent the acceptor/donor-like band-tail states and oxygen vacancy donor states are defined as exponential and Gaussian distributions respectively.

$$g_{TA}(E) = NTA\ exp\left(\frac{E-E_C}{WTA}\right) \quad (5)$$

$$g_{TD}(E) = NTD \exp\left(\frac{E_V-E}{WTD}\right) \quad (6)$$

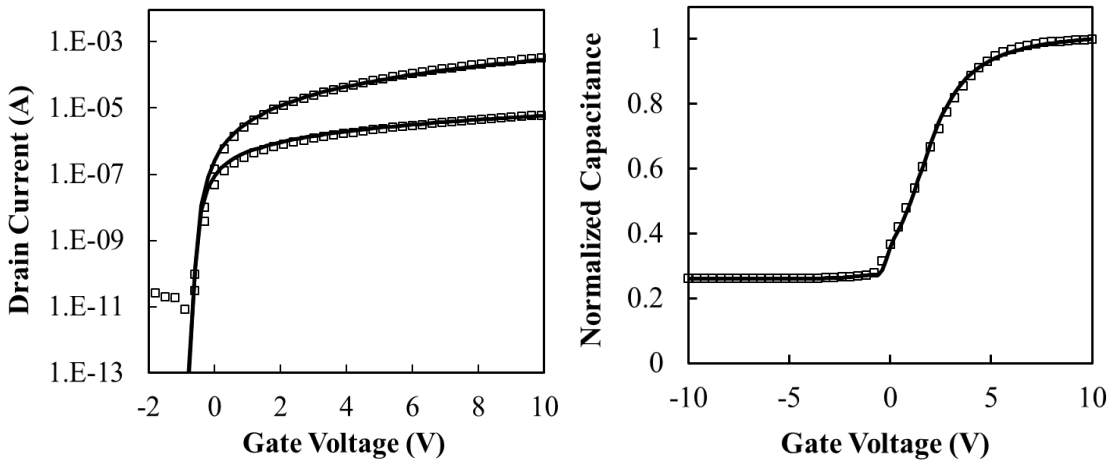
$$g_{GD}(E) = NGD \exp\left[-\left(\frac{E-EGD}{WGD}\right)^2\right] \quad (7)$$

where:

- $g_{TA}(E)$ and $g_{TD}(E)$ represent the density of acceptor-like conduction band-tail states and donor-like valence band-tail states, respectively
- E_c and E_v are energy levels at the conduction band and valance band edge in eV
- *NTA (NTD)* is the density of acceptor-like (donor-like) states in the tail distribution at the conduction band (valence band) edge in cm^{-3}/eV

- *WTA (WTD)* is the characteristic decay energy of conduction (valance) band-tail states in eV
- $g_{GD}(E)$ represents the density of donor-like states (oxygen-vacancies)
- *NGD, EGD,* and *WGD* are the peak value, mean energy, and the energy standard deviation, respectively, defining a Gaussian distribution for donor-like states, $g_{GD}(E)$.

5.2 Device Simulation



(a) (b)

Figure 20: (a) Measured (markers) and simulated I_D-V_G transfer characteristics of a "best-case" TFT without the application of a back-channel passivation material. The TFT channel dimensions were L=6 µm & W=100 µm. Model parameters and extracted properties are listed in Table I. (b) Measured (markers) and simulated C-V characteristics of an IDC with the same material model. Minor adjustments were made for structural calibration,

Devices fabricated without back-channel passivation exhibit excellent transfer characteristics with the best device shown in Figure 20(a). High-frequency C-V at 1 MHz on the IDC taken from the same testchip is shown in Figure 20(b). A simulation model was fit to both the I-V and C-V curves, and both have the same model parameters. These parameters are shown in Table 7. The only parameter that was changed in the reference model [14] was the peak density of oxygen-vacancy donor states (*NGD*). It should be noted

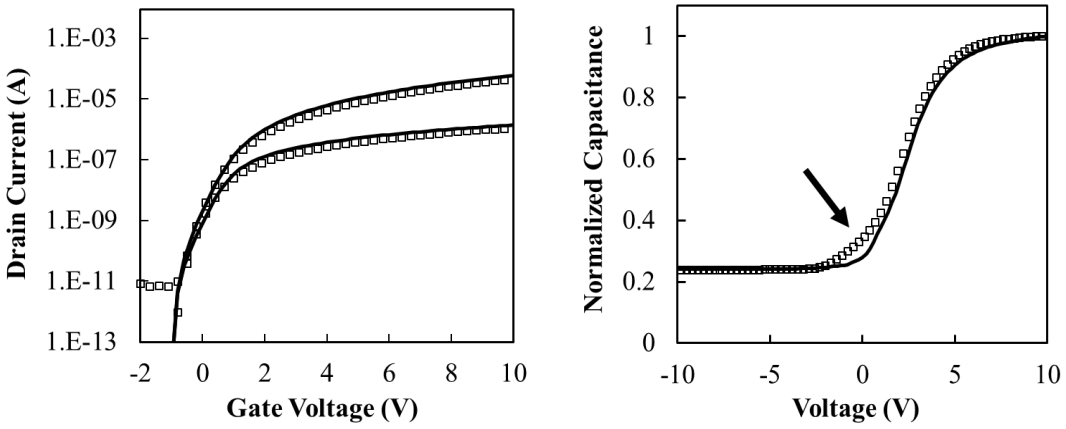
that the C-V model did require some adjustments to correct for the distributed resistance (slight offset in the IDC gated region width) and account for parasitic resistance.

Table 7: Material parameters and extracted TFT properties of Characteristics shown in Figure 20.

Symbol	Value
Band Gap	3.05 eV
Electron Affinity	4.16 eV
Relative Permittivity	10
Electron Mobility	15 $cm^2/V \cdot s$
NGD	$2x10^{16}$ cm^{-3}/eV
EGD	2.9 eV
WGD	0.1 eV
NTA	$1.55x10^{20}$ cm^{-3}/eV
WTA	0.013 eV
NTD	$1.55x10^{20}$ cm^{-3}/eV
WTD	0.12 eV
Extracted IGZO TFT properties	
Field-effect mobility	12 $cm^2/V \cdot s$
Threshold Voltage	-0.3 V
Subthreshold swing	135 mV/dec

While the "best case" unpassivated devices shown in Figure 20 have good characteristics in terms of performance and model consistency, the back channel is still exposed to the environment and it is necessary to be passivated for long term stability. Characteristics of devices fabricated with electron-beam deposited alumina as the passivation layer is shown in Figure 21. At first glance the devices seem to be inferior to those of the exposed back-channel. However, the performance across the entire wafer was very uniform and changes observed over a month of testing were negligible. The material model utilized for device simulation is also consistent with Table 7. However, additional parameters were added to establish charge centers and interface traps at the interface of the

IGZO back-channel and the alumina. These additional parameters are listed in Table 8, along with the extracted TFT properties.



(a) (b)

Figure 21. (a) Measured (markers) and simulated I_D-V_G transfer characteristics of a TFT with alumina passivation. The TFT channel dimensions were L = 24 µm & W = 100 µm. Material model parameters are consistent with Table I, with additional interface parameters and extracted properties listed in Table II. (b) Measured (markers) and simulated C-V characteristics of an IDC with the same set of model parameters. The arrow points to noted inconsistency between the measured and simulated characteristics.

The material model used for the simulation overlay in Figure 21 is consistent with that in Table 7, however additional parameters are needed to account for charge centers and interface traps associated with the interface between the IGZO and the back channel alumina. These additional parameters are listed in Table 8. A fixed charge density N_f = -1.9x10^{12} cm^{-2} and a Gaussian distribution of the donor-like interface traps were utilized to acquire a reasonable match to the I-V and C-V characteristics in Figure 21.The *EGD* and *WGD* parameters are unchanged from those listed in Table 7 for the Gaussian distribution of donor-like states in the IGZO material. The area of the density peak was set to *NGD* = 2x10^{12} cm^{-2}/eV, which brings the total integrated donor interface trapped charge state density to N_{IT} ~ 5x10^{11} cm^{-2}, and a net back-channel surface state density of N_{SS} ~ -1.4x10^{12} cm^{-2} when all the donor states are ionized.

While the origin of N_f has yet to be determined, the behavior of the interface traps is consistent with the energy distribution of oxygen vacancy donor states defined for the IGZO material. The total space charge in the IGZO material due to oxygen vacancies integrated over both energy and film thickness is N_{bulk} ~ 2.5x1010 cm^{-2}, so it is reasonable that interface states can dominate the device behavior. These interface defect parameter settings provide an excellent simulation match to the non-ideal TFT transfer characteristics, and provide insight on the extracted TFT properties listed in Table II. There is noted discrepancy in the simulated and measured IDC characteristics, however the model fit is still convincing without adding model complexity.

Table 8: Back channel interface parameters and TFT properties of the alumina-passivated devices shown in Figure 21.

Symbol	Value
NGD	$2x10^{12}$ cm^{-2}/Ev
EGD	2.9 eV
WGD	0.1 eV
N_f (fixed charge)	$-1.9x10^{12}$ cm^{-2}

Extracted IGZO TFT properties	
Field-effect mobility	5 $cm^2/V{\cdot}s$
Threshold Voltage	0.3 V
Subthreshold swing	300 mV/dec

Chapter 6

DISCUSSION

6.1 Discussion Summary

It was first established that Mo provides a more ohmic contact to IGZO than Al. There seemed to be some AlO_x at the interface causing the contact to be non-ohmic, even though the workfunction of Al is lower than that of Mo. The annealing conditions have a significant influence on the electronic properties of IGZO. Annealing in a non-oxidizing ambient at high temperature caused the IGZO material to be too conductive. To optimize these anneals some factors need to be taken into account, which include IGZO thickness and passivation layer material.

The initial passivation layer material of alumina enhanced the stability of the IGZO TFTs over time and suppressed hysteresis. The passivation material of BCB was shown to suppress hysteresis, but the long-term stability is still being investigated. Process integration processes were investigated to create a more robust process for IGZO TFTs with a passivation layer. Oxidation of Mo was a large problem and several approaches were made to correct the problem, but the main underlying issue was the repeated use of the same mask level for contact cuts and passivation open.

The well-established model with minor changes utilized to simulate unpassivated IGZO TFTs excellently matched the measured I-V and C-V characteristics. Comparing IGZO TFTs with and without a passivation layer revealed that there was some fixed charge and a change in the number of donor-like states. The fixed charge was found to be $N_f = -1.9 \times 10^{12}$ cm^{-2} and the area of the density peak was $NGD = 2 \times 10^{12}$ cm^{-2}/eV. These

changes to the model provide a very close overlay of the measured and simulated characteristics.

6.2 Conclusion

The methodology which was utilized in both the I-V and C-V analysis to interpret the defect states in IGZO TFT devices has been described. Interdigitated capacitors, used for C-V measurements, are complementary to the I-V measurements on TFTs, and TCAD simulation offers the capability to establish model parameters of both the material and device to match both I-V and C-V datasets. The application of the established material and defect model to devices which had the optimum annealing condition and no back-channel passivation material exhibited an excellent match between the simulation and measurements. The electron-beam deposited alumina as back-channel passivation material resulted in an improvement in the device stability. However, the I-V and C-V measurement both revealed the influence of interface defects. A device model implementing fixed charge and donor-like interface traps that are consistent with oxygen vacancies resulted in a reasonable match to measured characteristics, but further refinement to the model is necessary.

6.3 Future Work

While this work sheds some light on operation of IGZO TFTs, there is still more research to be done. Firstly, understanding all the material properties of IGZO is needed to make high performance TFTs. This can achieved by annealing the passivated IGZO and performing XPS and SIMS, which are currently in progress.

A new mask is needed to solve the Mo oxidation issue completely by expanding the metal contacts and shrinking the contact cut sizes. This allows for any undercut to still be on the metal contact pad and it will not affect the bottom gate Mo.

Other passivation materials need to be looked at to achieve the highest performing IGZO TFT. BCB was not analyzed as a passivation material because the wafers which were originally going to be part of the BCB passivation experiment had to be repurposed for alumina passivation due to flaws in the process integration strategies. Other materials to be utilized as potential passivators include HfO_2, Y_2O_3, and certain methods of depositing SiO_2.

The double gate structure, after the passivation of IGZO has been understood, is the next step going forward to increasing the performance of the IGZO TFT. There are not many foreseen process integration issues adding a top gate to the current process flow. Though, a new design will be needed to create a true double gate structure; the current process can only make a pseudo-double gate structure because the source and drain contacts partially cover the top of the IGZO.

The next step for IGZO TFTs is to create double-gate (DG) devices. Double-gate (DG) TFTs are very similar to that of a traditional CMOS transistor only with an extra gate oxide and electrode on the bottom of the channel. This allows for a higher current drive [36], and channel thicknesses can range from a few nanometers to hundreds of nanometers thick. The aforementioned passivation layer becomes the top gate dielectric in a double-gate structure.

APPENDIX A

Step-by-step process flow for fabricating a-IGZO TFTs on an oxidized silicon wafer.

#	Step	Process Parameters
3	RCA Clean	**Tool:** RCA Bench
4	Thick oxide growth	**Recipe # 350** **Tube # 1**
5	Mo Sputter	**Tool:** CVC 601 **Target:** 2 - Mo **Ar Flow:** 20sccm **Pressure:** ~2.7mTorr **Power:** 1000W **Thickness:** 2500 Å **Presputter:** 300 sec (use shutter) **Dep. Time:** 1000 seconds
6	Measure Mo thickness	**Tool:** Tencor P2 **Recipe:** Ger
7	Measure Mo Rs	**Tool:** CDE Resmap **Recipe:** 6", Rs 61 points
8	Measure Bow	**Tool:** Tencor P2 **Recipe:** 6_INCH_STRESS
9	**Gate Litho**	**Tool:** SVG - Coat program 1 **Tool:** GCA – Lithography **Tool:** SVG - Develop **Mask: RingFET reticle # 5, Gate** (clear field) **Job: RINGRET5.6IN** **Pass:** P1 **Time:** 2.8 sec (integrate mode) **Focus:** 0 **Alignment Marks:** N
10	**Inspection**	**Tool:** Leica Microscope
11	**Gate Etch**	**Tool:** Manual Bench in Wet Etch 2 **Chemistry:** Al etchant used for Mo etch in chemical cabinet in Wet Etch 2 **Time:** Until all Mo is removed (about 45 seconds)
12	**Inspection**	**Tool:** Leica Microscope

13	**Resist Strip**	**Tool**: Wet Bench **Solvent:** PRS2000 **Temp:** 90°C **Time:** 5 min (each bath)
14	**TEOS**	**Tool:** P5000 **Thickness:** 1,000Å of TEOS **Chamber:** A **Recipe:** LS 1000A **Time:** Check most recent times (about 11 seconds)
15	**Densify TEOS/LTO**	**Tool:** BruceTube 5 **Temperature:** 600˚C **Time:** 2 hours **Ramp Down:** Standard (not long) **Recipe:** 535
16	**Send to Corning for IGZO sputter**	Thickness depends on experimet
17	**Mesa Lithography**	**Tool:** SVG - Coat program 1 **Tool:** GCA – Lithography **Tool:** SVG - Develop **Mask: RingFET reticle # 5, Mesa** (clear field) **Job: RINGRET5.6IN** **Pass:** P4 **Time:** 2.8 sec (integrate mode) **Focus:** 0 **Alignment Marks:** N
18	**Inspection**	**Tool:** Leica Microscope
19	IGZO Etch	**Wetbench** **Etchant: DI + HCl,** 20:1 by volume, etch-rate increases with HCl proportion. Use IGZO monitor wafer for etch-time. Also look for visual end-point **Time:** Depends on thickness Use ZnO dedicated petridishes
20	**Inspection**	**Tool:** Leica Microscope
21	Resist Strip	**Use acetone + IPA on wet chemical bench** **Use ZnO dedicated petridishes**
22	Inspection	**Tool:** Leica Microsope
23	**Ring Oscillator Litho (Level 3)**	**Tool:** SVG - Coat program 1 **Tool:** GCA – Lithography **Tool:** SVG - Develop **Mask: RingFET reticle # 5,** Via (clear field) **Job: RINGRET5.6IN** **Pass:** P2 **Time:** 2.8 sec (integrate mode) **Focus:** 0 **Alignment Marks:** N

24	**Inspection**	**Tool:** Leica Microscope
25	**Oxide etch**	**Tool: MOS grade 10:1 BOE** **Time:** 2:30
26	**Inspection**	**Tool:** Leica Microscope
27	Resist Strip	**Use acetone + IPA on wet chemical bench** **Use ZnO dedicated petridishes**
28	Inspection	**Tool:** Leica Microsope
29	**S/D lift-off lithography**	**Use SVG in manual mode for HMDS prime, SCS spinner for LOR coat (LOR 5A 35sec @ 2k rpm), then 1 min 150C hot-plate bake and then manually coat HPR 504 on CEE spinner (recipe # 1) and then 1 min bake of resist**
30	**S/D lift-off exposure (level 4)**	**Tool:** SVG - Coat program 1 **Tool:** GCA – Lithography **Tool:** SVG - Develop **Mask: Ringret7.6in** (There is no ringret7 job use ringret 5 or 6 job) **Job: RINGRET5.6IN or RINGRET6.6IN** **Pass:** P1 (level 1 on mask is for S/D lift-off) **Time:** 2.8 sec (integrate mode) **Focus:** 0 **Alignment Marks:** N
31	Inspection	**Tool:** Leica Microsope
32	S/D metal deposition	**CVC 601 for Mo sputter, do overnight pump-down, 100nm** **Target: 2 - Molybdenum** **Ar Flow: ~17sccm** **Pressure: ~2.3mTorr** **Power: 200W** **Thickness: 100 nm** **Presputter: 300 sec (use shutter)** **Dep. Time: 2040 seconds**
33	**Metal lift-off**	**Tool: Ultrasonic Bench** Use IGZO dedicated petridish PG Remover about 1hr per wafer
34	Inspection	**Tool:** Leica Microsope

35a	Passivation layer/ Top-gate dielectric	**Sputtered SiOx, Al2O3, SiF4 oxide- depending on the experiment** **Thickness: 100 nm**
35b	Passivation layer/ Top-gate dielectric	**BCB** **Coat: SCS coater recipe #2, 3000rpm for 45 sec, bake 140C until Blue oven is at 140C** **Cure: With wafers in Blue oven ramp up to 250C in Nitrogen, once at temp cure for 60min**
36	Passivation Anneal	**Depends on the experiment**
37	Gate and S/D contact Lithography	**Tool:** SVG - Coat program 1 **Tool:** GCA – Lithography **Tool:** SVG - Develop **Mask: RingFET reticle # 6** **Job and Pass: ringret6.4in\P2,P4 or ringret6.6in \P2,P4 Pass:** P4 **Time:** 2.8 sec (integrate mode) **Focus:** 0 **Alignment Marks:** N
38	Gate and S/D contact etch	**HF MOS grade 10:1 or PAD etch** **Find etch rate first from monitor wafers**
39	Inspection	**Tool:** Leica Microsope
40	Final Testing	

APPENDIX B

Silvaco Atlas code for simulating IGZO TFTs.

```
go atlas simflags="-P 1"

#==========Set Variables=================
#-----------------Save variable
set save=24um_4.53
#--------------mobility variable
set mob=15
#----------thickness
set T=.05
#---------Length
set L=24
#-------------S/D workfunction
set wrkfcn=4.13
#---------------Gate workfunction
set gwrkfcn=4.53
#---------------Electron affinity
set chi=4.16
#--------------Number of Oxygen Vacancies (OV)
set nov=2e16
#-----------Average energy of OV
set eov=2.9
#----------Std Deviation of OV
set sov=.1
#----------Capture cross-section
set sig=1e-15
#=======================================
mesh width=100 outf=IGZOTFT_$"save".str master.out

x.m l=0 s=0.25
x.m l=10+$"L" s=0.25
y.m l=0 s=0.005
y.m l=$"T" s=0.0005
y.m l=0.1+$"T" s=0.005
#
#
#===============Define IGZO==================
region num=1 user.material=my_igzo y.min=0 y.max=$"T"
#============================================
region num=2 material=sio2 y.min=$"T" y.max=.1+$"T"

elec num=1 name=gate bottom
elec num=2 name=source y.max=0.0 x.min=0.0  x.max=5.0
elec num=3 name=drain  y.max=0.0 x.min=5+$"L" x.max=10+$"L"
#
#==================Gate====================
contact num=1 workf=$"gwrkfcn"
#
#============S/D Contacts===========
```

```
contact num=2 workf=$"wrkfcn"
contact num=3 workf=$"wrkfcn"
#contact num=2 neutral
#contact num=3 neutral
#
tonyplot
models fermi print
method autonr climit=10e-4
output con.band val.band
#
#===========Set IGZO Parameters=============
material region=1 material=my_igzo user.group=semiconductor
user.default=silicon mun=$"mob" mup=.1 nc300=5e18 nv300=5e18
eg300=3.05 affinity=$"chi" permittivity=10 mc=.34

#====================Defects=========================
#
# Key to the characterization of amorphous materials is the
# definition of the states within the band gap.
#
defects nta=1.55e20 ntd=1.55e20 wta=0.013 wtd=0.12 \
   nga=0.0 ngd=$"nov" egd=$"eov" wgd=$"sov" \
   sigtae=$"sig" sigtah=$"sig" sigtde=$"sig" sigtdh=$"sig" \
   siggae=$"sig" siggah=$"sig" siggde=$"sig" siggdh=$"sig" \
   tfile=defects.dat numa=128 numd=64



#interface    y.max=0.0     qf=-1.2e12
#interface    y.max=0 qf=-1.2e12

#inttrap y.max=0  e.level=2.9 donor density=1.8e12  degen=1
sign=1.0e-15 \
        sigp=1.0e-15
#inttrap y.max=0 e.level=2.9 donor density=1.8e12  degen=1
sign=1.0e-15 \
        sigp=1.0e-15
#
#======================== Id-Vg============================
#
solve init
solve vdrain=0.1

log outf=Lin1.log
solve vgate=0 vstep=-0.2 vfinal=-5 name=gate

log off

solve init
solve vdrain=0.1
log outf=Lin2.log
solve vgate=0.0 vstep=0.2 vfinal=10.0 name=gate
```

```
log off
save trap.file=traps2.dat x=10 y=0.03

#High Drain

solve init
solve vdrain=0.1
solve vdrain=0.2
solve vdrain=1
solve vdrain=2
solve vdrain=5
solve vdrain=10
save outf=linH_$"save".str
log outf=Sat1.log
solve vgate=0 vstep=-0.2 vfinal=-5 name=gate
save outf=Vd"10V"Vg"-5V".str
log off

load inf=linH_$"save".str master
solve init
solve vdrain=0.1
solve vdrain=0.2
solve vdrain=1
solve vdrain=2
solve vdrain=5
solve vdrain=10
log outf=Sat2.log
solve vgate=0.2 vstep=0.2 vfinal=10.0 name=gate

save outf=Vd"10V"Vg"10V".str

log off
tonyplot -overlay Lin1.log Lin2.log Sat1.log Sat2.log

quit
```

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