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Design and development of a radiation hardened color video sensor charge injection device chip

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Design and Development of a Radiation Hardened Color Video Sensor Charge Injection Device Chip

By

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Abstract

Voltage response of an active CID pixel is analyzed in detail theoretically. The linearity of the photo-response is assessed in destructive and non-destructive read-out modes of operation. The theoretical findings are illustrated by experimental data obtained from a test chip fabricated in 0.18 μm process. The test chip contained over 2400 active CID pixel structures with different geometries. The analysis is shown to be in good agreement with the experimental results.

The charge injection device, CID25, is presented. CID25 is a color video sensor compliant with the NTSC TV standard. It has 484 by 710 displayable pixels and is capable of producing 30 frames-per-second color video. CID25 is equipped with the active pixel technology combined with parallel row processing to achieve high conversion gain and low noise bandwidth. The on-chip correlated double sampling circuitry serves to reduce the low frequency noise components.

CID25 is operated by the camera system, ColoRAD, consisting of two parts, the head assembly and the camera control unit. These two parts are separated by a cable that can be up to 150 meter long. The CID25 imager and the head portion of the camera are radiation hardened. They can produce color video with insignificant signal-to-noise ratio degradation out to at least 4 Mrad of total dose of ^{60}Co γ-radiation. Detailed results of ColoRAD system testing before, during, and after irradiation are presented and discussed. In summary, ColoRAD is the first radiation hardened color video system, based on a semiconductor photo-detector that has an adequate sensitivity for operation in room lighting environments.

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List of Acronyms

ADU — Analog-to-Digital converter Unit

AGC — Automatic Gain Control

CCD — Charge-Coupled Device

CCU — Camera Control Unit

CDS — Correllated Double Sampling

CID — Charge Injection Device

CME — Coronal Mass Ejection

CMOS — Complimentary MOS

CMYG — Cyan-Magenta-Yellow-Green

CR — Cosmic Ray

DRO — Destructive Read-Out

FPGA — Field Programmable Gate Array

FPN — Fixed Pattern Noise

IR — Infra-Red

LD — Lateral Drain

LDG —Lateral Drain Gate

LED — Light Emitting Diode

MOS — Metal Oxide Semiconductor

MTF — Modulation Transfer Function

NDRO — Non-Destructive Read-Out

PCB — Printed Circuit Board

RGB — Red-Green-Blue

RIT — Rochester Institute of Technology

SAA — South Atlantic Anomaly

SNR — Signal-to-Noise Ratio

TE — Thermo-Electric

TID — Total Ionizing Dose

UV — Ultra-Violet

Introduction and Literature Overview

Charge Injection Devices (CID) form a class of semiconductor imaging devices alternative to CCDs and photodiode-based CMOS imagers. The main advantages of CIDs include random-access for read-out and clear, non-destructive read capability, high dynamic range, UV sensitivity, and radiation hardness. The combination of these properties makes a CID imager an excellent choice for scientific, industrial, machine-vision, and medical applications.

It is the goal of this work to advance the state of the art in the field of the CID photo-sensors by creating a radiation hardened low noise color video sensor. The main driving force behind this project is the desire to make nuclear power plant operation safer as color imaging allows one to discern rust and other products of undesired chemical reactions more readily.

The thesis is organized as follows. Chapter 1 provides a brief introduction into the field of semiconductors. Starting with the question of why the majority of semiconductor devices are made of silicon, the reader is guided through the most important building blocks of microelectronics, MOS transistor and MOS capacitor, to the charge transfer phenomenon and to the imaging devices based on it, CCD and CID. We then compare and contrast the properties of these devices and discuss the difference between passive and active pixel CIDs. Chapter 2 presents a theoretical study of the linearity of the response curve of an active CID pixel. We analyze both destructive and non-destructive types of read-out and provide some insight into the strength of

gate coupling in proximity-coupled structures. The theoretical analysis is extensively illustrated by experimental data. Chapter 3 presents the CID25 active pixel CID video sensor and the color camera ColoRAD based on this sensor. We describe in detail the architecture of the sensor and the camera and delineate the results of pre-irradiation performance evaluation of the camera in monochrome and color modes. Finally, Chapter 4 attempts to show that the main goal of this work is indeed accomplished. Starting with a history of radiation hardened products developed at CIDTEC, we then proceed to a description of space and terrestrial radiation environments that these cameras typically endure. The following section discusses radiation damage to MOS devices with implications for advanced technology node processes. We conclude by giving a detailed account of the results of 3 highly successful radiation tests of the ColoRAD video camera.

Extensive literature exists covering many topics discussed in this work. Detailed introduction into the field of semiconductors can be found in [1]. Theory of MOS devices is developed e.g. in [2]. Main principles of MOS device usage in digital and analog circuits are described in [3] and [4], respectively, whereas a comprehensive text on MOS layout is written by authors of [5]. A thorough exposition of charge transfer phenomena and CCDs is given in [6]. The basic description of passive CIDs is given in [7]–[9]. A comparison of performance characteristics of passive CIDs with those of CCDs can be found e.g. in [10] and references therein. Various types of read-out used in the case of passive pixel CIDs are discussed in [11]–[16].

The work on active pixel CIDs is deeply related to active pixel CMOS imaging. Active CMOS structures at early stages of their development are analyzed e.g. in [17]–[19]. A more modern outlook is presented e.g. in [20]. Active CID pixels were suggested in early 90's at CIDTEC. The first prototype active CID was actually built at RIT. This effort is described in [21]. Linearity of active CID pixel is studied theoretically and experimentally in [22]. Commercially successful active pixel charge injection devices, CID820 and CID25, are reported in [23] and [24], respectively. They

were being developed at about the same time but addressed different imaging needs, CID820 being a scientific imager and CID25 being a radiation hardened real-time video imager.

Book [25] serves as a broad scope reference text on the multitude of issues associated with the interaction of semiconductor components with radiation. Irradiation effects on solid-state photo-sensors are addressed more specifically e.g. in [26]. Some of the previously constructed radiation hardened (passive) CID imagers are described in [27]-[29], whereas detailed studies of the irradiation effects on the CID imagers were conducted e.g. in [30]-[32].

Chapter 1

Introduction into Semiconductors

1.1 Why Silicon?

Majority of semiconductor devices are built on silicon (Si). There are several reasons for silicon to be so popular. First of all, it is readily available and relatively cheap. Electrical conductivity of silicon can be varied by more than 10 orders of magnitude by introducing impurities of other elements, the process called doping. Silicon dioxide (SiO_2), glass, is an excellent insulator. Silicon and silicon dioxide form a high quality interface with a fairly small number of defects. Finally, the property that will be extremely important for the purpose of this thesis, silicon absorbs electro-magnetic radiation at wavelengths $\lambda < 1100$ nm through creation of electron-hole pairs.

1.2 Silicon of N- and P-Types

If one introduces (implants) into silicon ions from the 5^{th} group of the Mendeleev's periodic table of elements, such as arsenic (As) or phosphorus (P), one obtains silicon with surplus concentration of electrons or n-type silicon, Fig. 1.1. If, on the other hand, ions from the 3^{rd} group are implanted, such as boron (B), p-type silicon is obtained that has surplus concentration of holes, Fig. 1.1. By varying the dose and the energy of the implanted ions as well as by masking out certain areas, one can extensively vary geometry and conductivity of the implanted regions of silicon.

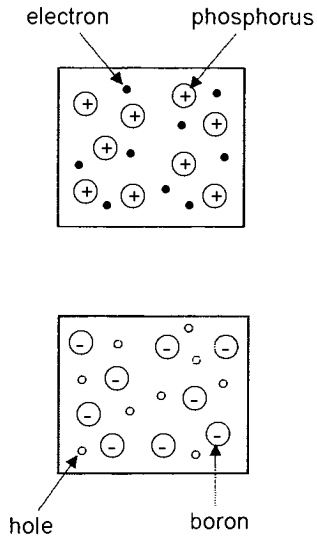

Figure 1.1: Silicon of n- and p-types.

1.3 PN-Junction

The crucial phenomenon occurs when regions of n- and p-type silicon are brought together to form a pn-junction. In this case, diffusion of mobile charge carriers (electrons from n-region to p-region and holes in the opposite direction) results in a formation of the space region with uncompensated charge of impurity ions (depleted region). This, in turn, results in the formation of a potential barrier that prevents any further diffusion from happening, Fig. 1.2.

1.4 MOS Transistor

The information in Sect. 1.3 allows one to understand the principles underlying the operation of an MOS transistor, the most important building block of modern microelectronics. For the purpose of this discussion we restrict ourselves to n-channel MOS transistors. P-channel MOS transistors can be treated in a similar fashion.

N-channel MOS (nMOS) transistor is built starting with weakly doped p-type silicon forming substrate. Two shallow regions are heavily implanted with n-type

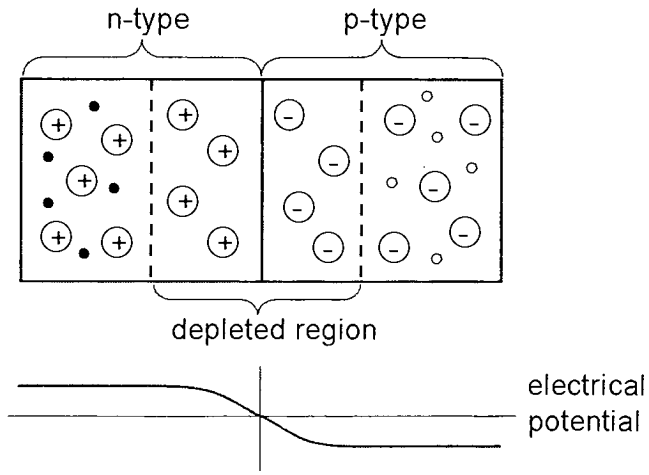

Figure 1.2: A potential barrier forms at a *pn*-junction.

impurities to form transistor source and drain. A very thin layer of high quality oxide is grown on top of the region between source and drain. Highly conductive polysilicon is deposited on top of the oxide to form the transistor gate, Fig. 1.3. (For technological reasons, in real life the sequence of steps is opposite: gate oxide growth, followed by polysilicon deposition and etch to form the gate electrode, followed by source/drain implant.)

The basic idea of transistor operation is as follows. The *pn*-junctions between the source and the substrate and between the drain and the substrate provide potential barriers for majority carriers, Figs. 1.3 and 1.2. This means that electrons cannot get from the source and the drain to the substrate while holes cannot flow in the opposite direction. Because of this, regardless of how positive the drain voltage V_d is, the electrons cannot get from the source to the drain. Hence, there is no current flowing between the source and the drain. The transistor is said to be in the "off" state.

As the gate voltage starts to increase, since the gate oxide is very thin and the gate itself is highly conductive, the potential of the gate strongly affects the potential of silicon right below Si/SiO_2 interface (known as the surface potential). Thus the

surface potential increases, whereas the potential of the source remains constant due to its very high conductivity. Eventually, when the gate voltage reaches the threshold voltage V_T, the potential barrier between the source and the substrate at the Si/SiO_2 interface is fully suppressed. At this point, electrons from the source enter the substrate and fill the entire area underneath the gate. This condition is known as channel formation. These electrons are swept by the drain-substrate junction into the drain (the potential barrier at the drain-substrate junction prevents electrons from going in the opposite direction) and, hence, the electrical current is flowing. The transistor is said to be in the "on" state.

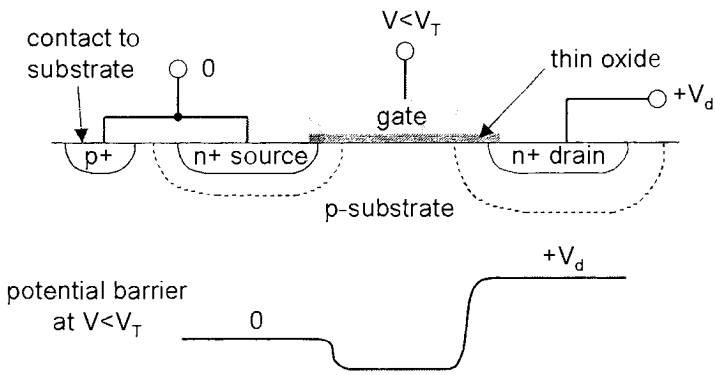

Figure 1.3: NMOS transistor. The graph shows the electrical potential along the Si/SiO_2 interface in the "off" state.

1.5 CMOS Inverter

The discussion above illustrates that an nMOS transistor can be used as a voltage controlled switch. If the gate-source voltage is below V_T, the switch is off, if the gate-source voltage is above V_T, the switch is on. Similar situation takes place in the case of a pMOS transistor. The only difference is that the threshold voltage for pMOS is negative, and, in order to turn it on, one needs to apply gate-source voltage, which is more negative than the negative threshold voltage.

A combination of nMOS and pMOS transistors, operating in the switch regime allows one to create a CMOS inverter, the most important digital circuit used extensively in all modern digital designs, Fig. 1.4.

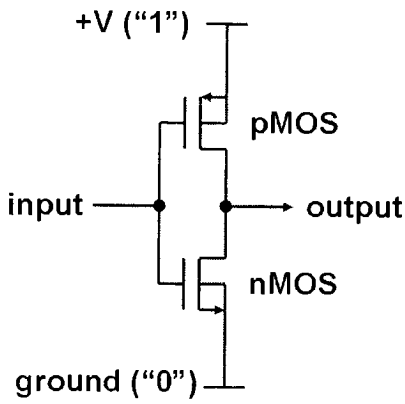

Figure 1.4: CMOS inverter.

In this case gates of the two transistors are connected to form the input, drains are connected to form the output. The source of the nMOS is connected to the ground (logic "0"), while the source of the pMOS is connected to the upper rail (logic "1"). If the input of the inverter is at 0, pMOS is on, and nMOS is off. Output is connected to the upper rail and produces logic "1". In the opposite case, where the input is at "1", nMOS is on, and the output is connected to the ground.

Using series and parallel combinations of nMOS and pMOS transistors, one can obtain various logical expressions at the output. For instance, if one have 2 nMOS transistors in series and 2 pMOS transistors in parallel, with gates of an nMOS and a pMOS connected to form input A, and gates of the other nMOS and pMOS connected to form input B, the output will represent logical expression NAND(A, B).

In order to implement the inverter in silicon its layout has to be created. Essentially, layout is the top view that shows all the device internal structure as a series of semi-transparent overlays, Fig. 1.5. Based on the layout a set of masks is created which will be used in silicon processing for selective etch, deposition, or implant. In

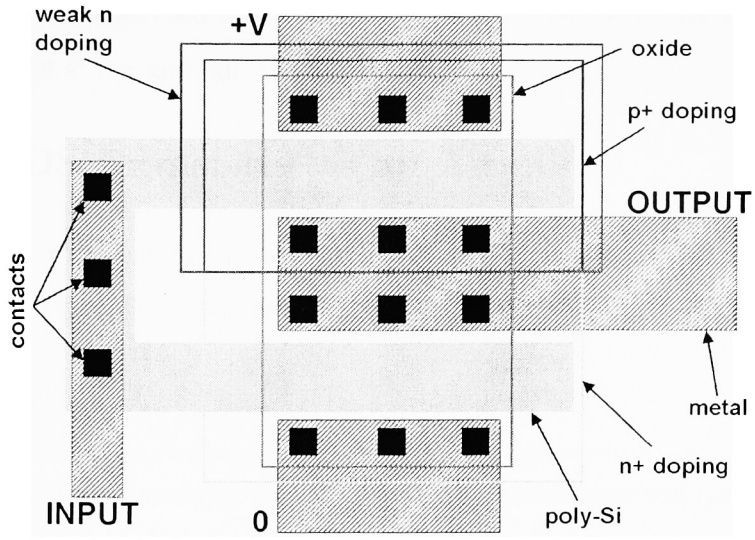

Figure 1.5: Layout of the CMOS inverter.

this case, it is assumed that the starting material is p-silicon. In order to form the substrate for the p-channel transistor, weak n-type doping is applied. The gates of the transistors are formed as the crossover of 2 layers: oxide and poly-Si. They determine the area of the high quality thin gate oxide and the position of the gate electrode with associated interconnects, respectively. Finally, source and drain of nMOS (pMOS) transistors are created via heavy $n^+(p^+)$ doping.

The shortest distance from source to drain is called the gate length L. The minimum value of this parameter achievable at a given semiconductor plant represents the "technology node" of that plant. The smaller is the technology node, the faster transistor can be built, and the more advanced is the technology. The size of the gate in the perpendicular to the length direction is called the width W of the gate. The bigger is the width, the smaller is the resistance of the switch, and the larger is the transistor transconductance, when it operates as an amplifier (see next section). A transistor with smaller channel resistance (higher transconductance) sometimes is called "stronger". Due to lower mobility of holes, pMOS transistors in inverters are

often made wider than their nMOS counterparts to achieve better balance of channel resistances and of rise and fall times at the output of the inverter.

1.6 MOS Transistor as an Amplifier

MOS transistor can operate not only as a switch but also as an active device, such as an amplifier. The main principles of its operation in this regime can be derived from the equation

$$I = K(V_{GS} - V_T)^2 \,, \tag{1.1}$$

which relates transistor drain current I with the gate-source voltage V_{GS}. In this case K is a proportionality coefficient, which, among other things, contains the factor W/L. The derivative $g_m = \mathrm{d}I/\mathrm{d}V_{GS}$ is called transconductance.

Consider 2 most popular active circuits involving an nMOS transistor. The circuit on the left-hand side of Fig. 1.6 is called common source amplifier. In this case, a small variable voltage U_{in} is applied to the gate (it is understood that there is also a DC voltage applied between gate and source to establish the working point of the amplifier, i.e. to make sure that it is biased into the desired regime of operation). The variable voltage causes change of transistor current $\mathrm{d}I = g_m U_{in}$. The change of transistor current causes the change of the output voltage by $R\mathrm{d}I$. Hence, we have an inverting amplifier with the gain of $-g_m R$.

The circuit on the right-hand side of Fig. 1.6 represents a buffer also known as source follower. In this case, the variable input voltage U_{in} causes the change of transistor current, which, in turns, causes the change of the source voltage: $\mathrm{d}I = g_m(U_{in} - R\mathrm{d}I)$. The change of the output voltage is equal to $R\mathrm{d}I$ and is given in the box below the circuit in Fig. 1.6.

As one notices, the parameter $g_m R$ determines both the gain of the amplifier and the precision of the buffer (the proximity of its gain coefficient to 1). Thus, it is desirable to make this parameter as large as possible. This can be accomplished by

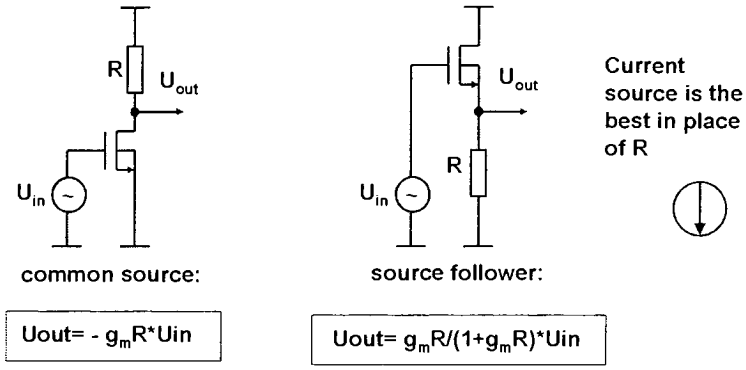

Figure 1.6: NMOS transistor as an active device: common source amplifier (left) and source follower (right).

using a "stronger" transistor, and by replacing R with a current source, a circuit that in theory has an infinite differential resistance (in practice it is never infinite but can be very high).

1.7 MOS Capacitor and Photogate

Another important device that can be built using the same principles is an MOS capacitor. As will be shown below this device is especially important for imaging applications, because it can be used to accumulate and store the photo-generated charge.

The MOS capacitor is composed of silicon substrate (assume p-type for the sake of the argument), thin insulating layer of oxide, and highly conductive polysilicon gate, Fig. 1.7. Suppose that back plate of the substrate is grounded. If negative voltage is applied to the gate, majority carriers (holes) will readily accumulate under the gate. This regime is called accumulation. The capacitance in this regime is frequency independent and equal to the gate oxide capacitance.

If positive voltage is applied to the gate, the holes are easily pushed away, while electrons slowly accumulate under the gate. This configuration is called inversion, and electrons are said to form the inversion layer. Electrons are created in the p-

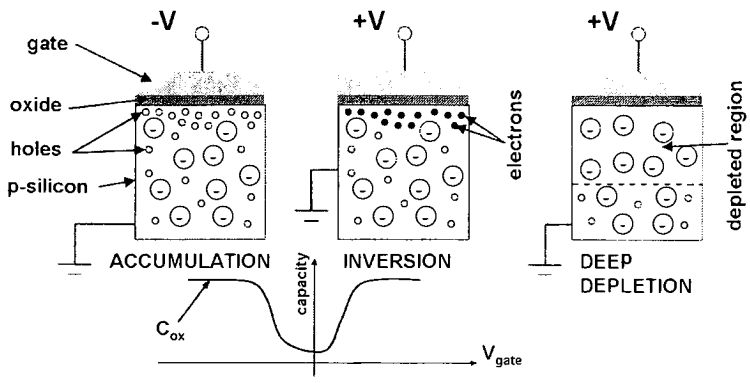

Figure 1.7: MOS capacitor in accumulation (left), inversion (middle) and deep depletion (right). The inset shows the low-frequency capacitance of the device as a function of the gate voltage.

substrate by relatively slow thermal generation process. Therefore, the capacitance in this regime depends on the frequency of the signal: at low frequency the capacitance is again equal to the gate oxide capacitance, whereas at high frequencies it is much lower. An MOS transistor in the "off" state is in the accumulation mode, while in the "on" state it is in the inversion mode. In the latter case the electrons are readily available from the source.

In both, accumulation and inversion, the thermodynamic equilibrium is reached. This means that various physical parameters, such as particle densities, do not depend on time, provided external conditions, such as voltages, do not change. For imaging applications, nonequilibrium (transient, kinetic) regime of operation called deep depletion is of primary importance. In this case voltage of the gate is rapidly increased. Holes are pushed away but there are no electrons in the substrate. Hence, a depletion region without mobile carriers forms underneath the gate. For typical doping densities of the substrate the depletion region can extend over several microns in all directions. If silicon is illuminated, the photo-generated electrons will accumulate under the gate, which will lead to the shrinkage of the deep depletion region. This process of "integration" of the photo-generated charge forms the basis of imag-

ing applications. If there is no light, the electrons will be slowly generated through thermal processes and will eventually fill the potential well created by the positive voltage of the gate. The deep depletion regime will thus equilibrate into inversion. This process, called "dark current" build-up, is parasitic for imaging applications. It can be minimized by cooling the imager.

1.8 Charge Transfer and Charge Coupled Devices

Placing 2 photogates in close proximity to each other and operating them in the deep depletion regime with independent voltages, one obtains the ability to transfer charge between them and thus to move charge in space. This principle is realized in Charge Coupled Devices (CCDs), the first semiconductor-based imaging devices.

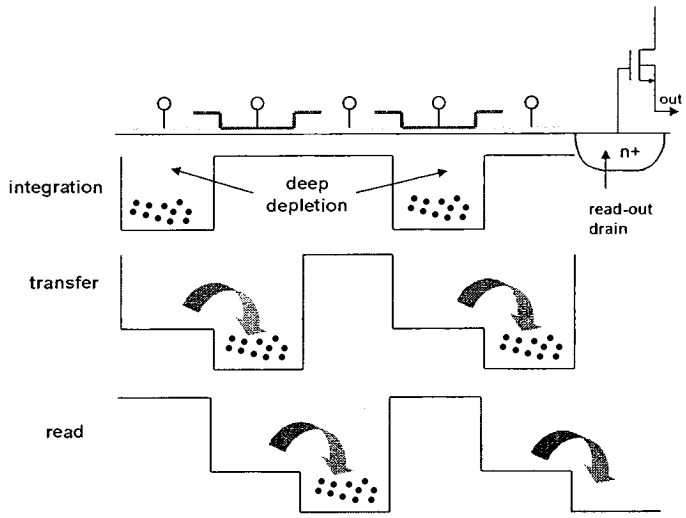

Figure 1.8: Integration, charge transfer and read-out in a CCD.

In a CCD (Fig. 1.8) there are 2 types of polysilicon gates deposited in such a way that the 2 types interlace, overlap, but do not touch each other. The voltages of these gates are controlled by 3 phases connected one to gates 1, 4, ..., $3n+1$, ..., another to gates 2, 5, ..., $3n+2$, ..., and the 3rd one to gates 3, 6, ..., $3n$, ... During the integration every gate, connected, say, to phase 1, is biased into deep depletion and

collects photo-charge. At transfer stage, phase 2 is biased into deep depletion, while voltage of phase 1 is reduced. Consequently, charge flows from gates connected to phase 1 to neighboring gates connected to phase 2. At the next step, phase 3 is biased into deep depletion, voltage of phase 2 is reduced, voltage of phase 1 brought to zero. Hence, photo-carriers move to the potential wells created under gates connected to phase 3. The process continues till a packet of charge reaches the end of the column.

At the end of each column the charge is transferred to a floating drain. Assuming p-type substrate the read-out drain will be a heavily doped n^+ region, so that electrons from the substrate readily enter the drain in agreement with the electrical potential structure of Fig. 1.2. The drain is connected to the gate of a source follower and is reset to a positive voltage shortly before the charge transfer (cf. Fig. 1.8). The capacitance of the read-out node is fairly small, and the addition of the photo-charge to it results in a significant voltage change at the gate of the source follower. The voltage change plays the role of U_{in} in the circuit on the right-hand side of Fig. 1.6. The source follower acts as a buffer or a charge amplifier. It charges the input capacitance of the following stage, which can be substantial, by approximately the same voltage as it sees at its input, which, obviously, requires much more charge than the photo-charge available initially. This scheme of operation results in excellent noise performance.

1.9 Charge Injection Devices

Despite the tremendous success of CCDs some of their inherent properties can be disadvantageous for certain applications. First of all, charge transfer efficiency must be extremely high as read-out of charge from some pixels involves several hundreds of transfers. This requirement is hard to meet when exposed to radiation, where charge transfer efficiency rapidly degrades due to damage created by highly energetic particles bombarding the imager. Another drawback is the necessity to transfer and read the entire frame every time data from any pixel is needed. In other words, there is no access to a random pixel for read-out or clear. This can be disadvantageous for

applications that require fine time resolution and cannot afford to wait till the entire array is serviced. Finally, the whole surface of the CCD is covered by polysilicon gates. This makes them unresponsive to light at shorter wavelength (soft UV and below) as these photons are absorbed by gates instead of the underlying substrate. This is obviously unacceptable for application targeting broader spectral range than just visible light. The way around this difficulty recently has been to illuminate CCDs form the backside. However, this approach requires back-thinning of the CCD substrate to a thickness of few tens of microns. This process proved to be rather expensive and is not readily available.

In an attempt to circumvent the problems outlined above Charge Injection Devices (CIDs) were invented. The basic description of CIDs is given in [7]–[9] and references therein. Typical CID pixel structure is shown in Fig. 1.9.

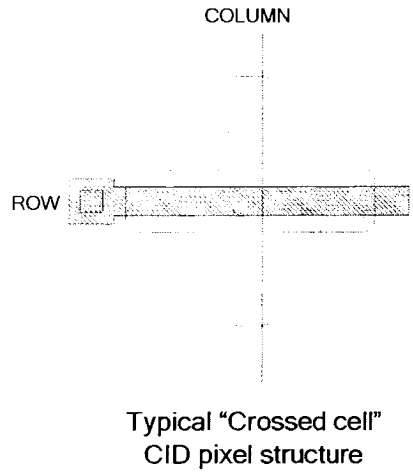

Figure 1.9: Typical configuration of a passive CID pixel.

In this structure polysilicon gates of the first type are deposited along columns of the imager, whereas those of the second type are deposited along rows of the imager. At every intersection the two poly layers overlap but do not touch each other. The area with thin oxide is limited to a certain region around each intersection (red contour in Fig. 1.9) and defines two photogates crossing each other.

At the read-out stage (discussed in detail below) all that needs to be done is the transfer of charge from one photogate to the other within a single pixel. Consequently, the requirement of high transfer efficiency no longer applies. The pixel is selected for read-out by its row and column address. Hence, full frame read is not necessary and pixels can be randomly accessed as required by an application. Finally, the greater part of the pixel area is not covered by polysilicon electrodes, which makes this device sensitive to UV. One concludes that CIDs eliminate all 3 main problems plaguing CCDs.

The CID gets rid of the photo-charge by injecting it into the substrate, where the charge recombines (CID derives its name from this process). The injection is achieved by biasing both photogates into accumulation, which pushes out minority carriers. As one can easily realize the injection can be also done selectively in a single pixel, in a rectangular region of interest, or in the entire array.

1.10 Passive Pixel CID Read-out

Let us describe the read-out in the "crossed cell" CID pixel in some detail. For reasons to be explained later pixels of this type are also called passive pixels.

During the integration stage both photogates are biased into deep depletion with the column gate biased stronger, Fig. 1.10. The photo-charge accumulates under the column gate. At the readout stage the row gate is floated and its voltage sampled and stored. Then the column gate is biased into accumulation which results in minority carriers flowing to the row gate. The new voltage of the row is sampled and stored again. The difference of the 2 samples is proportional to the amount of the photo-charge. If the row gate is also biased into accumulation the photo-carriers get injected into the substrate. If instead the column gate is brought back to its integration voltage the photo-charge falls back into the column gate and the integration may continue. This regime of operation is known as nondestructive read-out (NDRO). It is clear that CCDs are not capable of NDRO.

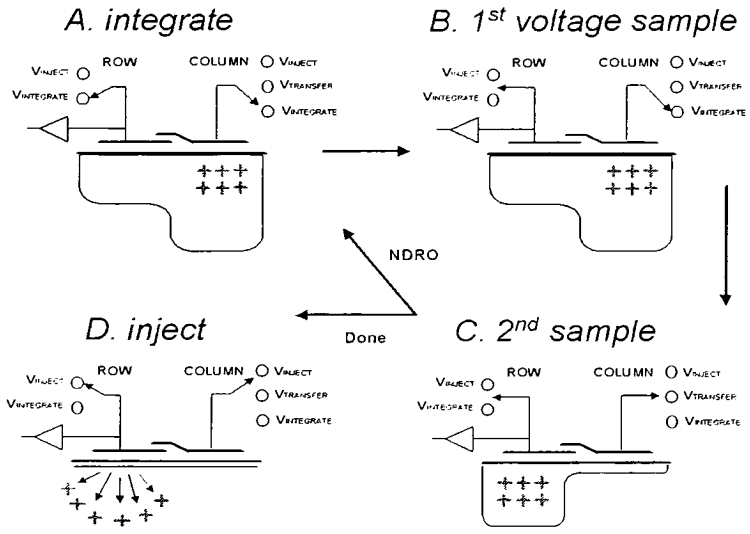

Figure 1.10: Passive CID pixel timing.

1.11 Passive and Active Pixels

The main disadvantage of the configuration described above is that the observed photo-signal is the result of the addition of a relatively small photo-charge, accumulated in a given pixel, to a fairly large capacitance of the whole row, i.e. of all the row photogates and the bus connecting them. As a result, the photo-signal turns out to be very small. The following stages of the circuit introduce fixed noise and it becomes impossible to achieve good signal-to-noise ratio (SNR). One of the solutions to this problem is to use multiple NDROs of the same charge in the given pixel. In this way the read noise decreases as a square root of the number of NDROs. However, this solution is not always acceptable, especially in applications that require fast update of the data, such as video applications. The charge transfer efficiency also becomes important.

Another way to improve SNR is to place a buffer, such as a source follower, in each pixel. In this configuration the read-out node is contained inside each pixel and its capacitance is small. Hence, the photo-charge develops a large voltage signal at

the gate of the pixel source follower, which results in much higher SNR. In this, active pixel, approach one can preserve such useful characteristics of traditional passive CID imager as random access for read and clear, NDRO, and UV sensitivity. High transfer efficiency is also not required.

Next chapter discusses the theory of active CID pixel in considerable detail following [22]. That chapter is written in a much more formal way than the Chapter 1. Readers not inclined to follow a fair amount of algebraic derivations can read the introduction (Sect. 2.1) and the conclusion (Sect. 2.5) to the Chapter 2 and skip to the Chapter 3.

Chapter 2

Device Physics of Active CID Pixel

2.1 Introduction

A CID pixel is built on low-doped epitaxial (epi) material, which resides on top of heavily doped substrate. Each pixel typically has 2 photogates and a means of transferring charge between them. During the integration stage the photons are absorbed by the epi layer in the areas free of photogates. The photo-generated minority carriers diffuse through the epi and are collected by the photogates biased into deep depletion. The read-out of the photo-charge can be accomplished in several ways. For instance, all the photo-charge can be transferred to one of the photogates (sense gate), which is then reset, left floating, and sampled. After that, by manipulating voltage of the second gate, the mobile charge is removed from the floating gate. Its voltage changes and is again sampled. The difference between the 2 samples is proportional to the transferred charge.

The charge clear can also be acomplished in various ways. Traditionally, both photogates are brought to the epi potential and the minoriy carriers are pushed out (injected) into the epi layer, where they can recombine or be absorbed by the epi-substrate junction. In this case the epi and the substrate must have different type of doping. Another approach consists of removing the photo-charge into a heavily-doped drain located at the front surface of the imager. The channel between this drain and the photogates is controlled by another gate. This approach is also suitable for device

back-thinnig.

Traditionally, CIDs had a passive pixel structure (cf. Sect. 1.9 and Fig. 1.9), where all the floating gates in a row were connected to a common bus and the photo-signal to be sensed developed across a large "row" capacitance. Various types of read-out used in this case were discussed in [11]–[16]. In general, passive pixel structure resulted in a rather high read-out noise. However, recently active pixel CIDs were introduced, e.g. [23]. In this case the floating gate is connected only to the gate of a source follower placed in each pixel. Along with the source follower each pixel contains reset and select switches. These three transistors are placed in a well of the same doping type as the epi layer. This configuration results in a significant reduction of the CID read-out noise. The aim of the present chapter is to analyze the voltage response of such an active CID pixel.

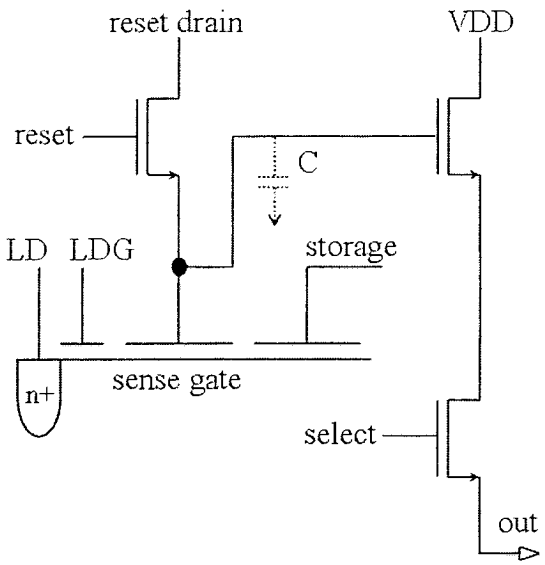

Figure 2.1: Typical configuration of an active CID pixel.

The models for destructive and non-destructive active CID pixel read-out are developed in Sects. 2.2 and 2.3, respectively. The theoretical findings are illustrated by raw experimental data obtained from a test chip fabricated in 0.18 μm process.

The test chip contained over 2400 active pixel structures with different geometries. Section 2.4 discusses certain problems for non-destructive read-out stemming from inadequate coupling of the photogates.

2.2 Destructive Read-out

The typical configuration of an active CID pixel is shown in Fig. 2.1. For the sake of discussion let us assume that the epitaxial layer is of p-type. The polysilicon sense photogate is connected to the gate of a source follower (SF) and to the source of a reset switch. The source of the SF is connected to the output bus through a select switch. Another polysilicon gate (storage gate) is located in close proximity to the sense gate (in a single poly process) and is driven by a pulsed source. The n^+ diffusion (lateral drain or LD), connected to a fixed positive DC voltage, provides means of removing photo-generated electrons from the sense gate. Finally, another gate (called a lateral drain gate or LDG) controls the channel between the sense gate and the LD.

The capacitance C represents a lumped linear capacitance that acts as if it was placed between the sense node and a DC power supply. In particular, it includes various parasitic capacitors (such as gate-drain capacitance of the SF) as well as the gate-source capacitance of the SF multiplied by $1-\gamma$, where γ is the gain of the SF.

Consider the simplest operation of a CID pixel with the storage gate set to 0 (same as epi) at all times. This mode of operation is known as Destructive Read-Out or DRO. During the integration the LDG is at $V_{\text{skim}} = 0$, while the sense gate is kept at a positive voltage V_i. For simplicity of notation, from here on we assume that the gate flat-band voltage is 0. It is straightforward to include a realistic flat-band voltage in the equations below.

During the read-out stage the select switch is turned on, the reset switch is turned off, and the first sample is taken on the output bus. Then the LDG is brought to a positive voltage V_{inject}, photo-generated electrons are drained into the LD, and the LDG is brought back to V_{skim}. After that the second sample is taken on the output

bus. The difference between the two samples represents the photo-signal, V_s.

When the charge drains from the sense gate the depletion region underneath it widens, and the surface potential becomes more positive. For any given V_{inject}, there exists such a value of the sense surface potential ϕ_j, at which no more charge can be drained out. Depending on the initial amount of the photo-charge, the electrons can either be drained out completely before ϕ_j is reached, or the potential reaches ϕ_j while some fraction of charge is left under the sense gate. Both these cases can occur before the sense gate saturates.

Here we analyse the two cases, described above, quantitatively. In the deep depletion regime of operation the gate voltage V, the surface potential ϕ, the absolute amount of the mobile charge under the gate Q, and the depletion width w are related to each other by the following equations:

$$V = \frac{eN_A w^2}{2\epsilon_{\text{Si}}} + \frac{t_{\text{ox}}}{\epsilon_{\text{ox}}}\left(eN_A w + \frac{Q}{S}\right) , \tag{2.1}$$

$$\phi = \frac{eN_A w^2}{2\epsilon_{\text{Si}}} , \tag{2.2}$$

where S is the gate area, t_{ox} is the gate oxide thickness, N_A is the substrate doping density, e is the elementary charge, while ϵ_{Si} and ϵ_{ox} are dielectric constants of silicon and silicon oxide, respectively. At the end of the integration stage $V = V_i$, $Q = Q_i$, and the depletion width w_i can be found as a solution of the quadratic Eq. (2.1).

If the electrons were removed completely, the final sense gate voltage V_f and the depletion width w_f can be found from Eq. (2.1) with Q set to 0, complemented by the charge conservation at the sense node:

$$V_f = \frac{eN_A w_f^2}{2\epsilon_{\text{Si}}} + \frac{t_{\text{ox}}}{\epsilon_{\text{ox}}} eN_A w_f , \tag{2.3}$$

$$eN_A w_f S + CV_f = eN_A w_i S + CV_i + Q_i . \tag{2.4}$$

In the other case, $w_f = w_j \equiv \sqrt{2\epsilon_{\text{Si}}\phi_j/(eN_A)}$. The two unknowns become V_f and the final charge under the sense gate Q_f. Hence, we obtain

$$V_f = \phi_j + \frac{t_{\text{ox}}}{\epsilon_{\text{ox}}}\left(eN_A w_j + \frac{Q_f}{S}\right) , \tag{2.5}$$

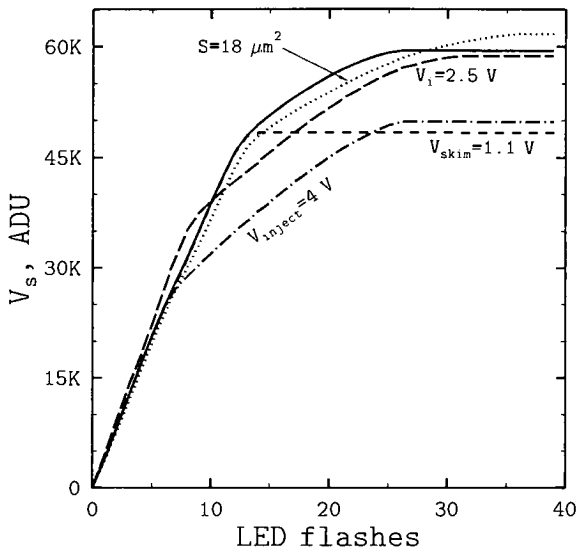

Figure 2.2: Experimental signal voltage of a CID (in ADUs) as a function of a number of red LED flashes during the integration. Solid curve corresponds to $V_i = 2$ V, $V_{\rm inject} = 5$ V, $S = 13$ μm^2, and $V_{\rm skim} = 0$. Long-dashed, dot-dashed, dotted, and short-dashed curves correspond to $V_i = 2.5$ V, $V_{\rm inject} = 4$ V, $S = 18$ μm^2, and $V_{\rm skim} = 1.1$ V, respectively.

$$eN_A w_j S + CV_f + Q_f = eN_A w_i S + CV_i + Q_i \ . \tag{2.6}$$

Consider the slope of the response curve in these two cases. Let us denote derivatives with respect to Q_i by a prime. We need to find V_f' at $Q_i = 0$ and V_f' at $Q_f = 0$ in the first and second regime, respectively. First of all, we note that according to (2.1), $eN_A w_i' S = -(C_{\rm D}||C_{\rm ox})/C_{\rm ox}$, where $C_{\rm ox} = \epsilon_{\rm ox} S/t_{\rm ox}$ is the sense gate oxide capacitance, and $C_{\rm D} = \epsilon_{\rm Si} S/w_i$ is its *initial* depletion capacitance[1]. Differentiating Eqs. (2.3) and (2.4) and substituting $w_f = w_i$ we arrive at

$$V_f'(Q_i = 0) = \frac{1 - (C_{\rm D}||C_{\rm ox})/C_{\rm ox}}{C + C_{\rm D}||C_{\rm ox}} \approx \frac{1}{C + C_{\rm D}} \ , \tag{2.7}$$

where the last simplification is based on the fact that typically $C_{\rm D} \ll C_{\rm ox}$. In the second case an analogous derivation yields:

$$V_f'(Q_f = 0) = \frac{1 - (C_{\rm D}||C_{\rm ox})/C_{\rm ox}}{C + C_{\rm ox}} \approx \frac{1}{C + C_{\rm ox}} \ . \tag{2.8}$$

[1] $a||b \equiv ab/(a+b)$

Therefore, the response curve of the CID pixel (i.e. dependence of the voltage signal on the photo-charge) has a dual-slope characteristic with the knee point determined by the simultaneous solution of Eqs. (2.1), (2.5), and (2.6) with $Q_f = 0$.

Now consider what happens when the sense gate saturates. From Eq. (2.1) it follows that the saturation occurs at $w_i = 0$ and $Q_i = C_{\rm ox}V_i$. Using Eq. (2.4) we can see that

$$V_s = \frac{1}{C}(C_{\rm ox}V_i - eN_A w_f S) \ . \tag{2.9}$$

The second term in the parenthesis is a small correction that can be expressed via V_i. More important is that in this case the saturated signal is proportional to the initial voltage V_i.

In the second case Eq. (2.6) can be rewritten as

$$(C + C_{\rm ox})V_f - C_{\rm ox}\phi_j = eN_A w_i S + CV_i + Q_i \ , \tag{2.10}$$

and hence at saturation

$$V_s = \frac{C_{\rm ox}\phi_j}{C + C_{\rm ox}} \ . \tag{2.11}$$

Therefore, in the latter case the saturated signal is completely determined by the LDG voltage, but not by the amount of charge at saturation nor the initial sense gate voltage.

Figure 2.2 shows the experimental signal voltage of a CID operated in the regime described above as a function of a number of red LED flashes during the integration (proportional to the amount of photo-generated electrons collected by the sense gate). The solid curve corresponds to $V_i = 2$ V, $V_{\rm inject} = 5$ V, $S = 13$ μm^2, and $V_{\rm skim} = 0$. One can clearly observe the dual-slope characteristic. The saturation occurs at 60 000 Analog-to-Digital converter Units (ADUs) of signal for 26 LED flashes. The long-dashed curve corresponds to the same parameters except for $V_i = 2.5$ V. In this case the saturation occurs at 31 LED flashes for the same signal level in agreement with Eq. (2.11). The difference in the first slope between the solid and the long-dashed curves is most likely to be attributed to the quantum efficiency effect: higher V_i

improves charge collection at the integration stage. The dot-dashed curve corresponds to $V_{\text{inject}} = 4$ V, which reduces ϕ_j and the respective saturation signal [cf. Eq. (2.11)] but not the saturation charge as compared to the solid curve. The dotted curve corresponds to increased sense gate area $S = 18\ \mu\text{m}^2$ and illustrates dependence (2.8) of the second slope on C_{ox}. It also saturates at higher photo-charge corresponding to 36 LED flashes. Finally, short dashes illustrate the dependence on V_{skim}. The LDG voltage is kept at 1.1 V at the integration stage. In this way the excess photo-charge is skimmed off by the LD and the second slope disappears.

2.3 Non-Destructive Read-out

One of the big advantages of CIDs is a possibility to add the second (storage) photo-gate. Then the photo-charge can be transferred between the sense and storage gates and thus read out multiple times (non-destructive read-out). The Non-Destructive Read-Out (NDRO) allows one to *(i)* improve sensitivity in the regime of weak signal (e.g., N NDROs result in $\sqrt{N}$ times reduction in read-out noise); and *(ii)* extend the upper boundary of the dynamic range by being able to selectively read and drain pixels that receive higher photon flux ("hot" pixels) instead of servicing the entire array. The latter might take considerably more time and result in the saturation of the "hot" pixels.

In the NDRO regime the pixel is operated as follows. During the integration the storage gate is kept at 0. At the read-out stage the first sample is taken as described in Sect. 2.2, then storage gate is brought up to a positive voltage V_t, photo-charge transfers from sense to storage and then the second sample is taken. The photo-signal is again given by the difference[2] of the two samples.

The pixel response depends on whether or not the charge is transferred to the storage gate completely. As the electrons move from sense to storage, the surface

[2]In what follows we neglect direct capacitive coupling between storage and sense. It can be taken out by dark frame subtraction or by having a transfer gate beween storage and sense.

potential of the sense increases while that of the storage decreases. If the amount of photo-charge is relatively large the surface potentials of the two gates become equal and the charge transfer stops.

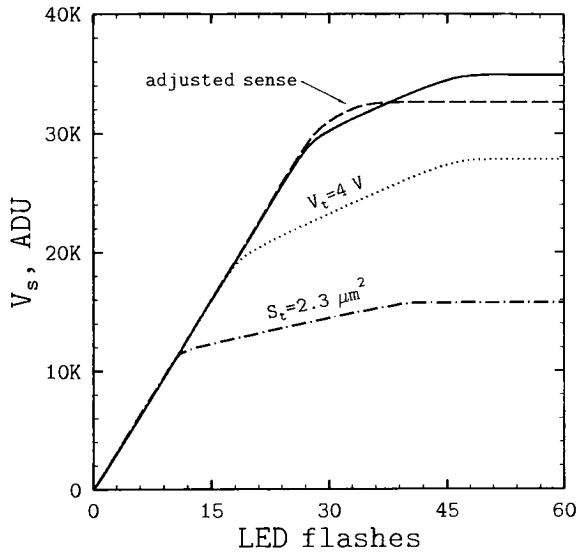

Figure 2.3: Experimental voltage response of a CID operated in the NDRO regime. Solid curve corresponds to $S_t = 8.6\ \mu\text{m}^2$ and $V_t = 5$ V. Dash-dotted and dotted curves show responses for $S_t = 2.3\ \mu\text{m}^2$ and $V_t = 4$ V, respectively. Dashed curve corresponds to the original pixel with S and V_i adjusted according to Eq. (2.15).

In the case of full charge transfer the pixel response is described by the same set of Eqs. (2.3) and (2.4). In the other case, Eqs. (2.5) and (2.6) must be complemented by a self-consistent expression for ϕ_j:

$$V_t = \phi_j + \frac{t_{\text{ox}}}{\epsilon_{\text{ox}}}\left(eN_A w_j + \frac{Q_i - Q_f}{S_t}\right) , \tag{2.12}$$

where S_t is the area of the storage gate. This equation is based on the fact that in this case storage and sense surface potentials and depletion widths must be equal.

The slope of the response in the case of the full charge transfer is given by Eq. (2.7). In the second case the situation is now more complex. The slope in question

reads:

$$V_f'(Q_f = 0) = \left[1 - \frac{C_{\rm D}||C_{\rm ox}}{C_{\rm ox}} - \frac{C_{\rm ox}(C_{\rm ox}||C_t)}{C_t(C_{\rm ox} + C_{{\rm D}j})}\right] \times \left[C + C_{{\rm D}j}||C_{\rm ox} + \frac{C_{\rm ox}(C_{\rm ox}||C_t)}{C_{\rm ox} + C_{{\rm D}j}}\right]^{-1} . \quad (2.13)$$

In this case $C_t = \epsilon_{\rm ox} S_t / t_{\rm ox}$ is the storage gate oxide capacitance, and $C_{{\rm D}j} = \epsilon_{\rm Si} S / w_j$ is the *final* depletion capacitance of the sense gate.

If $C_t \to \infty$, (2.13) reduces to (2.8). If $C_{\rm D}, C_{{\rm D}j} \ll C_{\rm ox}$, Eq. (2.13) simplifies to

$$V_f'(Q_f = 0) \approx \frac{(C + C_{{\rm D}j})||C_{\rm ox}||C_t}{C_{\rm ox}(C + C_{{\rm D}j})} . \quad (2.14)$$

The important property of Eqs. (2.13) and (2.14) is the dependence of the slope on C_t. In the case of the complete charge transfer (initial slope regime) such a dependence is absent.

Let us determine the point of the onset of the second slope (i.e. find maximum Q_i at which Q_f is still 0) and provide practical guidelines for the dual gate CID pixel design. From Eqs. (2.5) and (2.12) we see that at $Q_f = 0$, $V_t - V_f = Q_i / C_t$. Based on (2.7) and assuming that $C_{\rm D} \ll C$, V_f can be approximated as $V_i + Q_i / C$. Therefore, the knee point of the response curve occurs approximately at $Q_i = (C||C_t)(V_t - V_i)$. For a practical design this condition should occur simultaneously with the sense gate saturation $Q_i = C_{\rm ox} V_i$. Combining these expressions we arrive at the final result:

$$\frac{C_{\rm ox}}{C||C_t} = \frac{V_t - V_i}{V_i} . \quad (2.15)$$

Given V_t and V_i, Eq. (2.15) allows one to size the gates in such a way that incomplete charge transfer never takes place.

The NDRO regime of CID operation is illustrated in Fig. 2.3. The solid curve corresponds to the baseline pixel with $S_t = 8.6$ μm^2 operated at $V_t = 5$ V. One can observe a pronounced second slope indicating incomplete charge transfer. The dash-dotted curve shows response for a similar pixel with a smaller storage gate oxide capacitance, $S_t = 2.3$ μm^2. The onset of the second slope requires less photo-charge.

In accordance with Eq. (2.14) the second slope is less steep. This is in contrast with the behavior that one would expect from direct charge sharing between the sense and storage gates. In the latter case the slope would decrease as C_t increases approaching 0 in the limit of infinite C_t. The dotted curve corresponds to the baseline pixel operated at $V_t = 4$ V. In this case the incomplete charge transfer starts occuring at an earlier stage than for $V_t = 5$ V. The second slope is the same as at $V_t = 5$ V (solid curve), and so is the saturation charge. Finally, the dashed curve shows the original pixel adjusted according to the guidelines put forward by Eq. (2.15). The sense gate area is decreased by about 25% and initial voltage V_i is slightly reduced. The resulting response curve is optimised for maximum linear range and shows no dual-slope behavior.

2.4 The Importance of the Potential Barrier Between Storage and Sense Gates

In the previous section we assumed that the storage and sense gate surface potentials were the only factors governing the charge transfer. The real situation is more complex because the coupling between the surface layers under the gates is not ideal. The simplest approach to this problem is to locate the gates as close to each other as possible for a given process. In this proximity-coupled structure the charge transfer relies on the fringing fields provided by the poly gates. Let us note that for any modern process the minimum allowed spacing is still much larger than the gate oxide thickness. Extrapolating from the case of very large spacing, one can easily see, that if the gates have the same voltage and no charge under them, there will be a potential barrier between the gates. The properties of similar barriers were studied in [33]. The height of this barrier depends critically on the width of the spacing.

When the storage gate is at a somewhat higher voltage than the sense, as is the case during the charge transfer, the barrier disappears. However, as charge transfers, the potential of the sense gate rapidly increases (being determined by a relatively

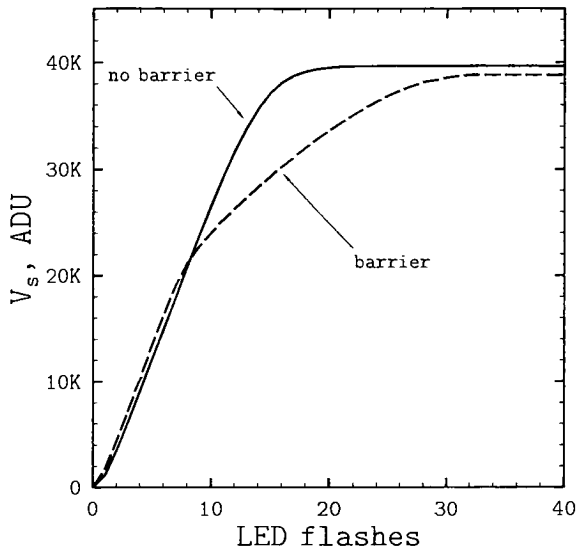

Figure 2.4: Experimental voltage response for the NDRO (Sect. 2.3) type of CID operation for proximiy-coupled (dashed) and n-coupled (solid) structures.

small value of C), and the barrier appears again. If by this point not all of the charge is transferred the dual-slope scenario takes place again.

The coupling can be enhanced (the barrier removed) by introducing a transfer gate made of the second poly layer that is located in the spacing and overlaps the sense and storage gates. Another way to remove the barrier is to introduce n-type doping in the spacing. In Fig. 2.4 we compare proximity-coupled and n-coupled structures. The solid and dashed curves correspond to pixels with doped and undoped spacings, respectively. The pixels are identical in all other respects. One can clearly see the influence of the barrier on the response curves.

2.5 Summary of the Results

We have considered the linearity of active pixel CIDs. It was shown that the response curve can exhibit a dual-slope characteristic. The dual slope is an indication of incomplete removal of the photo-charge from the sense gate due to the voltage increase of the latter. The dual slope can occur when the charge is transferred to either the

lateral drain (DRO) or the storage gate (for the NDRO purpose). In the latter case the second slope increases with increase of the storage gate size in contrast with the charge sharing scenraio. In the limit of very big storage gate the second slope approaches that for the DRO regime.

The second slope can be removed by careful gate sizing, capacitor C sizing, adjustment of the gate voltages, or by skimming off the excess charge during the integration. However, some applications may find the dual slopes useful in that a steep first slope provides low light level sensitivity while the second slope can accomodate highlights.

The linearity curve of CID in NDRO regime is very sensitive to the srength of the coupling between the sense and storage gates. A potential barrier between the two gates can give rise to the second slope even if all the other parameters related to the pixel and its operation are fixed. This makes a CID pixel with two photogates an excellent tool to study the charge transfer phenomena.

Chapter 3

Color Video Camera ColoRAD

3.1 Radiation Hardened Cameras at CIDTEC

As discussed in Sect. 1.9, up until recently all CID designs employed passive pixels. This meant that the photo-sensitive nodes of all pixels in a row or a column of an imager were connected together. Accordingly, the photo-charge generated in each pixel developed voltage across a very large capacitance of the entire row or column. This resulted in a rather low conversion gain and fairly high pixel-referred read noise (cf. Sect. 1.11). Multiple NDROs could not be used to minimize noise in real-time applications such as video. Thus the only means of improving the signal-to-noise ratio in this architecture was to increase the signal or, equivalently, the amount of charge corresponding to 700 mV, the full-level video signal. Naturally, this reduced the imager sensitivity as more light was needed to produce useful level of video. In the context of the radiation hardened video systems, discussed in this work, the sensitivity was still adequate for CID21 and CID22 sensors, designed for monochrome video imaging supporting RS170 and CCIR formats, respectively. The first attempt to design a radiation hardened color video imager, CID23, failed due to a deficiency of the column selection technique. This error was corrected in CID24, which was the first radiation hardened semiconductor-based imager to produce color video. However, the sensitivity issue for this device proved to be severe. Compared to CID21 and CID22 the conversion gain problem described above was further exacerbated by decreased

quantum efficiency due to reduction of the pixel open area and deposition of the color filters.

At about the same time as active CID pixel was introduced for scientific applications [23], it was decided to employ this concept for a design of a new radiation hardened color video imager. The main character of this thesis, the CID25 imager, is the result of this effort.

3.2 ColoRAD System Description

The CID25-based camera system, ColoRAD, consists of 3 main parts: the CID25 image sensor, head mechanicals mated to the set of printed circuit boards (head boards), and the Camera Control Unit (CCU), Fig. 3.1. There is also a power supply.

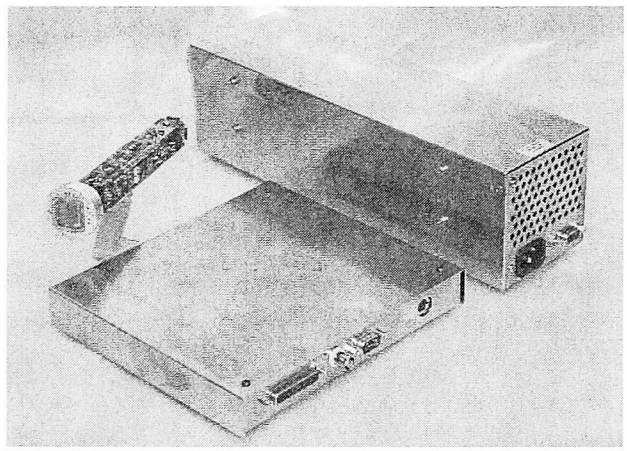

Figure 3.1: CID25-based video camera, ColoRAD, comprising radiation hardened head assembly (including the imager, the head mechanicals and the set of head boards), CCU, and power supply for operating at ambient temperatures up to 65C.

The CID25 image sensor produces color NTSC-video. The pixel array has a total of 512 rows by 730 columns. The displayed (active) area is 484 rows by 710 columns. The ratio of the width of the active area to its height is 1.3365. The imager has the active pixel structure. As a result, the photo-generated charge develops voltage across a relatively small capacitance. All pixels in a row are read into the on-chip

memory in parallel for low noise bandwidth operation. The imager has the capability of reading 2 rows simultaneously, necessary for Cyan-Magenta-Yellow-Green (CMYG) color imaging or progressive scan. It can also scan only odd (even) rows one by one to implement the RS170 standard. First 16 rows are covered with metal light shield to provide the black reference to the camera. The CID25 imager contains on-chip Correlated Double Sampling (CDS) circuitry to reduce the imager Fixed-Pattern Noise (FPN), kTC noise, and the low frequency temporal noise.

The CID25 imager is located in a sealed head which incorporates a 1-stage thermo-electric (TE) cooler and a thermistor. The TE cooler maintains the imager at 25C even if the ambient temperature is as high as 70C. The set of head boards attaches to the sealed head to form the head assembly. The head boards contain the circuitry that drives the CID25 imager and preprocesses the analog video generated by the imager. Both the imager and the circuitry of the head boards are radiation hardened.

The CCU features an FPGA to generate imager timing, an analog video processing chain and a digital color processor. The CCU is not radiation hardened and must be located outside the area exposed to radiation. The head assembly and the CCU are connected via a cable. The length of the cable can be up to 150 meters.

3.3 CID25 Imager Description

3.3.1 Pixel Design

The CID25 imager is built with the preamplifier-per-pixel technology using 0.8 micron process. The pixel size is 18 by 16.4 microns. The pixel schematic is shown in Fig. 3.2. Each pixel contains a photogate (cf. Sect. 1.7) connected to the source of the reset switch and to the gate of the source follower pMOS. The source of the source follower is connected to the pixel output bus through the row-select switch controlled by its gate voltage "Select". The source follower is biased by a current source for optimum operation as explained in Sect. 1.6. There are 2 pixel output buses, odd and even,

connected to pixels in odd and even rows, respectively (Fig. 3.4). The reset switch is controlled by its gate voltage "Reset". The drain of the reset switch is at a global DC voltage "Reset/Inject". This node serves 3 main purposes: *(i)* it is used to establish the voltage of the photogate (when the reset switch is "on"); *(ii)* it is the drain of the pixel source follower; and *(iii)* it acts as a lateral drain for the photo-charge injection.

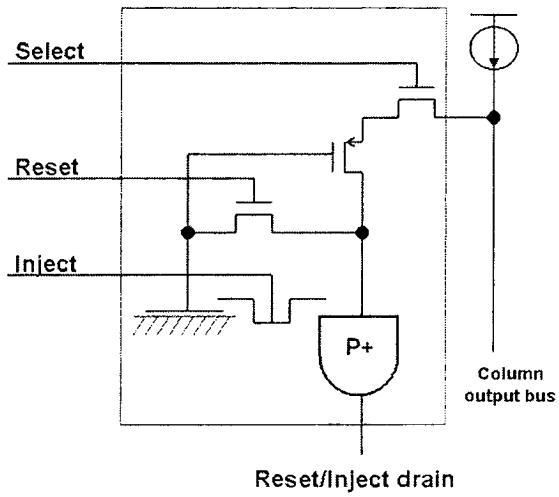

Figure 3.2: Schematic of the CID25 active pixel.

The pixel can be run with several possible timing sequences. The following details one of them. The pixel integrates the photo-charge for the duration of the frame. After a given row is selected, the reset switch is turned "on" and "off" to establish the voltage of the photogate (sense gate). After that, the first sample is stored on a capacitor. The integrated charge is then injected into the lateral drain by turning the transfer gate (controlled by the "Inject" signal) "on" and "off". Following that, the second sample is recorded on another capacitor.

The main purpose of the CID25 image sensor is to serve as a color NTSC video imager utilizing CMYG color matrix. An image of the sensor with CMYG color filters deposited over the pixel array is shown in Fig. 3.3.

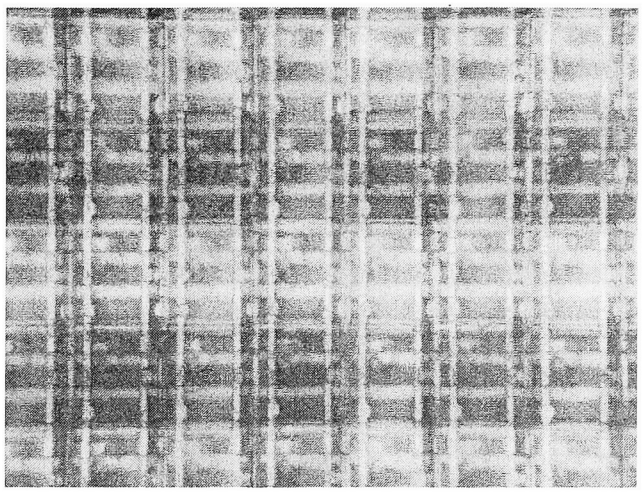

Figure 3.3: CID25 imager with CMYG color filters deposited.

3.3.2 Correlated Double Sampling Circuitry

The CID25 image sensor is equipped with on-chip CDS circuitry, Fig. 3.4. CDS generates 2 samples proportional to pixel outputs before and after charge injection. The photo-signal is the difference of these 2 samples. Since the pixel sense node capacitance is small, the photo-signal is relatively large, which results in the imager having fairly high SNR. Properties of a CDS circuitry, such as the one used here, are analyzed in detail in [34]. The purpose of double sampling is to reduce the $1/f$ noise from the pixel source follower, kTC noise due to the pixel reset switch, and FPN associated with various offsets (e.g., the variation of the threshold voltage of the pixel source followers across the array). It is important to note that the transfer gate moves bidirectionally between the 2 samples, which greatly reduces any FPN components, associated with the capacitive coupling to the transfer gate that, otherwise, wouldn't be removed by CDS.

The CDS circuitry of the CID25 imager produces current-mode signal for both pixel samples simultaneously (using 2 imager output buses). The current-mode operation contributes to imager's low noise performance, as well as makes it suitable for

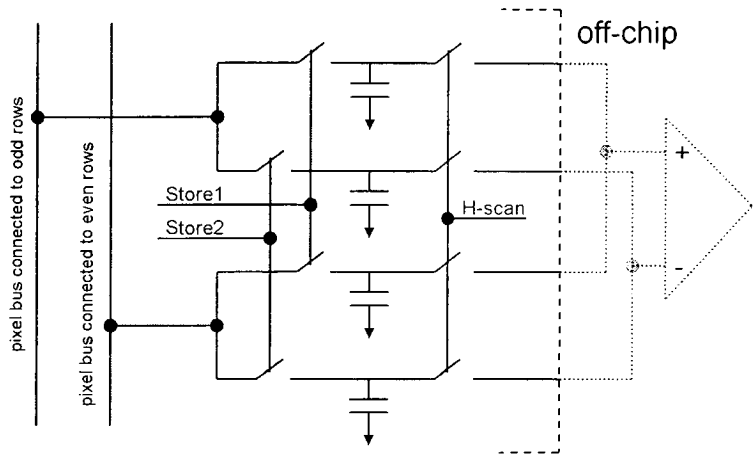

Figure 3.4: Schematic of the on-chip CDS circuitry of the CID25 imager.

integration with the CIDTEC's standard camera type. In the CMYG color mode of operation, 2 samples for 2 rows are generated simultaneously using 4 imager output buses (see Fig. 3.4). They are combined with appropriate signs outside the imager to generate a CMYG color line with subtracted noise signature.

3.3.3 Selection Circuitry

The imager uses proved radiation hardened shift register design for column and row selection (horizontal and vertical scanners, respectively). However, for CID25 the design was optimized for reduced current consumption, increased radiation tolerance and speed.

The horizontal scanner sequentially selects columns of the imager for read-out. Each column has 4 memory cells (cf. Fig. 3.4: "H-scan" signal is the output of the horizontal scanner). As soon as a column is selected the charges from its memory cells are dumped onto 4 imager output buses. The horizontal scanner is a continuously running circuit, which is driven by 2 clock phases. The phases are used to propagate the selection from column to column. There are also 2 additional reset phases to deselect the previously selected column. Additional data phase serves as horizontal

synchronization, i.e. it determines the moment when the first column is selected.

The vertical scanner sequentially selects rows of the imager for read-out and CDS processing. There are 2 independent vertical scanners, one for odd and the other for even rows. For optimum response each row is driven from both left and right sides. Vertical scanners have essentially the same architecture as the horizontal one. Two clock phases are used to propagate selection from row to row. Two reset phases are used to deselect previously selected rows. These phases are shared between odd and even scanners. By contrast, odd and even data signals are independent and serve for independent synchronization of odd and even rows.

The architecture with odd and even vertical scanners allows one to easily implement CMYG color and interlaced monochrome imaging. In the color mode of operation there are 2 types of frames. In one of them the displayed lines are combinations of rows 1+2, 3+4 etc. In the other frame the combinations are 2+3, 4+5 etc. These 2 frames alternate to produce the 30 fps video. In the interlaced monochrome (RS170) mode, there are odd and even frames, which are alternated. In the odd frame only odd rows are displayed and vice versa.

In the progressive scan and RGB color modes all frames are identical and are comprised of all the existing lines. This type of operation on the imager side is also possible as the imager can generate data from 2 rows independently (but simultaneously). However, this mode of operation would require significant modification of the camera, which would have to process 2 streams of data instead of combining them into one.

3.4 Head Description

The head portion of the system consists of several parts. The imager resides in a hermetically sealed, evacuated enclosure (on the left-hand side of Fig. 3.5) on top of a TE cooler. The cooler keeps imager at a temperature of 25C for ambient temperatures up to 70C. The purpose of the cooler is to reduce imager dark current.

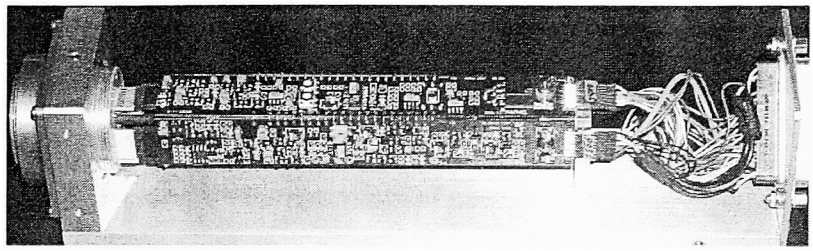

Figure 3.5: The CID25 head assembly. Imager hermetic enclosure with TE cooler on the left. The set of 4 printed circuit boards with head electronics attaches to it.

On top of the imager enclosure there is a BG38 filter (bluish square in Fig. 3.1) that cuts off infrared portion of the light spectrum. This is necessary for color reproduction. The lens mounts on top of the enclosure. The key requirement for the lens is that it does not brown in radiation (regular glass lenses do brown in radiation).

On the back of the imager enclosure a head board assembly is attached. The head board assembly consists of 4 PCBs with electronics. It provides drivers for imager control signals and video preprocessor that amplifies the video signal coming from the imager, subtracts low frequency noise component and converts to differential signalling. There are also powerful buffers that send the video down the cable to CCU.

In standard configuration (shown in Fig. 3.5) the cable connecting radiation hardened head and non rad-hard CCU can be up to 50 meters long. An add-on radiation hardened timing generation board (that extends the head board assembly by ~ 5 cm) allows one to increase the length of the cable to 150 meters.

3.5 Camera Control Unit Description

The Camera Control Unit serves several purposes. It contains all the components essential for camera operation that are not radiation hardened. First of all, there is a Xilinx FPGA that controls imaging timing. Secondly, there is an extensive analog block, which amplifies (equalizes) and filters analog video coming from the head.

Thirdly, there is a color processor used to synthesize RGB color from CMYG pixel information, as well as to adjust white balance, gamma etc. The color processor is based on 3 chips by Cirrus Logic. These chips are CCD Imager Analog Processor (basically, an A/D converter), Digital Color-Space Processor, and Digital Video Encoder. The CCU produces NTSC color video or monochrome video complying with RS170 standard at 30 frames per second.

CCU also realizes Automatic Gain Control (AGC) up to 12X. This feature is especially important if lighting is low. Under these circumstances the camera will boost the gain to produce full level video, 700 mV. The low read noise or high initial SNR of the imager are essential for meaningful AGC. Otherwise the noise will also get boosted and the SNR will drop to an objectionable level. The imager was also tested with a prototype CCU add-on dark frame subtraction board, which led to a significant improvement of the SNR. This result was very encouraging as it showed that it would be possible to run the imager with higher camera gain. At this point 24X AGC is being contemplated. Needless to say, that this will boost overall camera sensitivity and will enable one to operate at extremely low light conditions still producing useful video.

Finally, CCU also realizes the proprietary algorithm of timing modification in radiation.

3.6 Pre-irradition Performance

The camera was characterized before during and after irradiation. The results of the studies associated with radiation will be discussed in Chapter 4. In this section we describe some of the results of pre-irradiation tests.

The sensitivity and noise of the camera system were analyzed using the Davidson Optronics TV Optoliner with a broad band light source and the Rohde-Schwarz 40 Hz-10 MHz noise meter. The saturation of the monochrome imager (without IR cutoff and color filters) operated at pixel full well in the RS170 mode was observed at 0.35

ft-c of light. The gain of the camera was adjusted so that at pixel saturation the camera video output was equal to 700 mV. The camera system was set up using the most favorable configuration — a 2 meter cable separating the head assembly and the CCU. The resulting SNR was 59 dB. The main contributions to the noise were the temporal noise from the CCU and the fixed pattern noise from the imager. The SNR dropped to 58 dB with a 40 meter cable.

Using the test slides it was established that the system resolved at least 450 TV lines.

Related to the resolution is the Modulation Transfer Function (MTF). MTF is critical for color imaging as poor MTF is one of the principal sources of color cross-contamination. For CID25 the MTF was characterized by the camera response to the step-like target and was proven to have single pixel resolution. This result is further examplified by Fig. 3.6. The image in the figure can be divided into 2 regions. The first region, the synthesized color area, includes color bars, central white area, and 2 grey-scale strips between the color bars and the white area. The second region, the monochrome area, includes 4 sets of black-and-white bars (on each side of the image) and 2 grey-scale strips adjacent to the color bars but located closer to the edges of the image.

In this imager an additional layer of metal was deposited on top of the sensor active area. There were holes etched in the metal partially uncovering active area of each pixel. In the synthesized color area, the fraction of the uncovered active area for each hole was derived from the transmission of the color filter that would be deposited on top of the corresponding pixel in the final product. For instance, the central white area corresponds to white light seen through the color filters. In this area 100% of the active area was uncovered for pixels that were supposed to have Yellow color filter, 78.6% for pixels that would have Cyan color filter, 66.3% for Green pixels, and 46.1% for Magenta pixels. The grey-scale bars adjacent to the white area correspond to white light of decreasing intensity seen through the color filters. This is implemented

via additional coverage of the pixels starting from the open area fractions cited above and proceeding to complete opaqueness in 7 evenly spaced increments.

The colored bars correspond to white, yellow, cyan, green, magenta, red, blue, and no light seen through the color filters. For instance, cyan light is emulated by having 78.6% of the active area uncovered for pixels that are supposed to have Cyan color filter, 66.3% for pixels that would have Yellow and Green color filters, and 12.4% for Magenta pixels. The fact that color bars look so good (in fact, using vector-scope one can prove that the color bars are nearly perfect) proves that there is no appreciable color cross-contamination, or, equivalently, that single-pixel resolution is achieved.

In the monochrome area, black and white bars correspond to 100% covered or 100% open pixel active areas. The grey scale represents white light of decreasing intensity seen through pixels with 100% open active area. Interlaced black and white bars on all 4 sides of the image illustrate MTF. When this imager was run in the monochrome mode alternating black and white bars were easily discernible proving, once again, single-pixel resolution in both vertical and horizontal directions. However, after color processing (the way the slide in Fig. 3.6 was prepared) interlaced bars, showing resolution in vertical direction merged to produce uniform grey (color processing adds lines). Interlaced bars showing resolution in horizontal direction after color processing turned into blue and read areas seen in the top-left and bottom-right corners of the image.

The real color video was readily produced, once the actual color filter array was deposited (cf. Fig. 3.3). The saturation of the color imager (with IR cutoff and color filters) operated at pixel full well required 3 ft-c of light. The SNR in the color channel was measured for a sample of 6 cameras with 150 meter cable and on average was equal to 40.6 dB [minimum was 37.7 dB, maximum was 45.7 dB, camera-to-camera variation of 8 dB, data courtesy of the Nuclear Fuel Industries, Ltd, Osaka, Japan (NFI)]. With the color subcarrier trap filter "on", the average SNR increased to 47 dB. If, additionally, the weighting filter was turned "on" the average SNR rose to 58

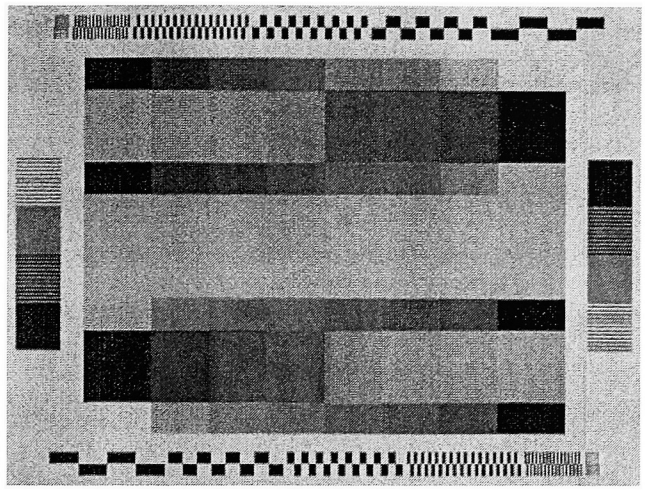

Figure 3.6: Modulation transfer function structures and synthesized colors obtained by depositing an extra metal mask, such that the area of a hole above any given pixel is related to transparency of the color filter that would normally be deposited on top of that pixel.

dB.

Since the SNR of the monochrome camera is more than adequate for video applications, the camera can be run with higher gain. As already mentioned in Sect. 3.5, the full-level video output is then achieved at a fraction of the pixel full well, which translates into better sensitivity. The camera was demonstrated to work adequately with 12X gain which reduced the light level necessary to produce the full-level video output to 0.03 ft-c. The SNR at 12X gain was 37 dB.

Chapter 4

Radiation Environments and Performance of the ColoRAD Camera in Radiation

4.1 CID Cameras and Radiation

Numerous imaging applications require the photo-sensor and the attendant camera to have a certain degree of radiation tolerance. By radiation tolerance we understand tolerance to irradiation by highly energetic massive particles (e.g., electrons, protons, ions, neutrons) as well as by photons in the X-ray and γ ranges.

Tube-based cameras have long been accepted as the industry standard radiation resistant detectors. CIDs were the first solid-state detectors to seriously challenge this position, first in the 1980's through the development of special purpose star tracking devices and, during the 1990's, by the development and introduction of monochrome-version video cameras (cf. Sect. 3.1).

The performance of a device in radiation is typically characterized as a function of Total Ionizing Dose (TID) and flux of ionizing radiation. The total dose corresponds to certain amount of energy absorbed and is different for different materials. The unit of 1 rad (Si) is often used. It corresponds to 100 ergs/g $= 1.6 \times 10^8$ MeV/g of absorbed energy per unit weight. Lethal dose for humans is about 400 rad. The flux is measured in rad/hour.

Although there are several possible scenarios where cameras can be exposed to radiation (examples are provided in the following section), for tests, it is customary to use ^{60}Co γ-radiation. ^{60}Co γ-cells can be accessed at a number of university and military facilities in USA. During these tests, one typically monitors the signal-to-noise ratio and a few other parameters of an operating camera exposed to a high flux of radiation for certain period of time. The general picture quality is also assessed to verify that the camera continues to generate usable video throughout the test.

4.2 Examples of Radiation Environments

In this section we will provide several examples of radiation environments, that CID-based photo-detectors have been exposed to or may be exposed to in the future. In doing so we try to accomplish 2 goals: *(i)* to underline the importance of work on radiation hardened imaging equipment, that is needed for a wide variety of applications, and *(ii)* to elucidate the challenges, that are being dealt with in the course of this work, associated with the extremely hostile conditions, that our cameras have to endure. Space applications provide several good examples of the environments with significant fluxes of energetic particles. We will consider a number of them in some detail in Subsects. 4.2.1, 4.2.2, 4.2.3. Subsection 4.2.4 provides some terrestrial examples of radiation environments.

4.2.1 Van Allen Belts

The first example is given by the so-called Van Allen belts. All space missions from simple communication satellites to the most elaborate scientific instruments and manned missions have to deal with this phenomenon and the damage that it causes.

The Earth has an approximately dipole magnetic field that is strong enough to trap charged particles through the Lorentz force, thus protecting the surface of the planet from bombardment by energetic particles. The particles spiral around the

magnetic field lines and are "reflected" at the mirror points, where they encounter stronger magnetic fields (close to North and South poles). There is also a net drift around the Earth — protons drift clockwise when viewed from the north and electrons drift counterclockwise, which has the effect of creating a net electrical current around the Earth. In general, the particle fluxes are treated as isotropic, although very low in the South Atlantic Anomaly (see below), < 500 km, the proton fluxes from the west are about 100 times higher than the fluxes from the east.

Belts consist of high energy protons ($E < 400$ MeV) and electrons ($E < 10$ MeV). Some heavy ions exist, but not in large quantities. Electrons regions can be characterized as two belts. The inner belt spans the heights from 400 km to 12,000 km and is composed of particles generated by energetic solar particles and reactions with cosmic rays. The outer belt spans the region between 12,000 km and 60,000 km of height and is composed of particles coming from solar wind and the ionosphere. The "slot region" between the belts has fluxes about 1-2 orders of magnitude lower than the belt regions, however even that is still rather high. Protons form a single belt centered at about 4000 km above the equator. Additionally, solar events (cf. Sect. 4.2.2) can create new belts of very high intensity.

The South Atlantic Anomaly (SAA) is a region of the Van Allen belts, where the magnetic field lines are closer to the surface of the Earth and allow particles to get closer. Its existence can be explained by the tilt and the offset in the Earth's magnetic field. The size of SAA increases as the altitude increases, but at 500 km it ranges from $-90°$ to $+40°$ longitude and $-50°$ to $0°$ in latitude, Fig. 4.1. The anomaly exists all the way down to the sensible atmosphere. For low Earth orbits (< 1200 km), virtually all of the exposure of spacecrafts to trapped protons is due to passage through SAA.

The radiation belts can be very dynamic during periods of solar activity, such as coronal mass ejections and solar flares, as well as during coronal hole passage. There is also a long-term correlation with the 11-year solar cycle: there are more electrons

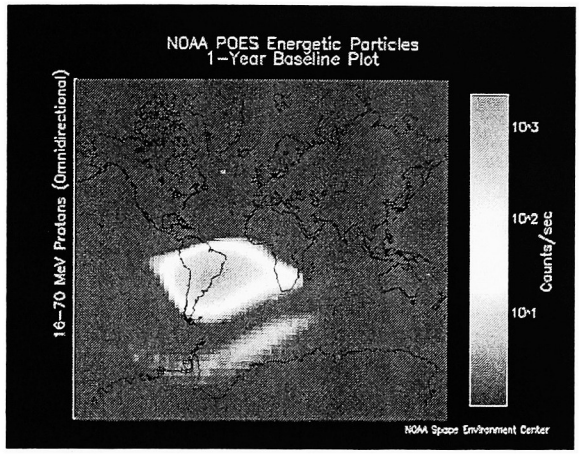

Figure 4.1: The passage of spacecrafts through Van Allen belts causes major degradation to the photo-detecting equipment. For instance, in the part of the belt called the South Atlantic Anomaly the density of highly energetic protons (16-70 MeV) can reach 1000 counts/sec.

and fewer protons during solar maximums. Solar events can also create additional quasi-stable belts by injecting particles into the magnetosphere. For instance, on March 21, 1991 a solar event created a new belt that was measured for 7 months and may still persist today.

4.2.2 Solar Coronal Mass Ejections

The Solar Coronal Mass Ejections (CME) are the biggest explosions in our solar system. There can be as much explosive power as produced by 1 billion megatons nuclear yield. The explosions can result in emissions of up to 100 billion kg of matter as plasma from the Sun. The speed of the emissions can reach 1000 km/s ($\sim$ 2 million mph). Besides severe damage to spacecraft equipment these events can cause geomagnetic storming on Earth by coupling to the Earth's magnetic field. The exact process of these releases is not entirely known. They can occur at any time, but are more frequent during periods of high sunspot activity. Sometimes, but not always, they are accompanied by the traditional X-ray solar flares.

The CMEs result in harsh radiation environments. They produce large fluxes of

protons and heavy ions that can last for days to weeks. Figure 4.2 shows proton flux from the so-called "Bastille Day Event" that happened on July 14, 2000. As one can see, significant flux of 10 MeV protons lasted for a very long time.

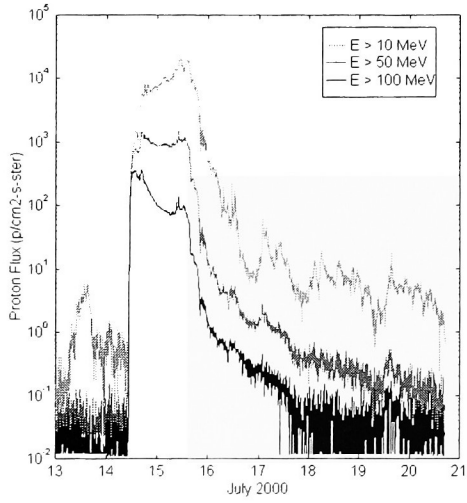

Figure 4.2: High energy proton flux from the Bastille Day event as a function of time.

Although low altitude, low inclination orbits are mostly shielded by the Earth's magnetic field, some shuttle extravehicle operations have been moved due to CMEs. The exposure over the poles, where magnetic field screening does not work very well, can be significant even for high-altitude aircrafts. Other measured effects of CMEs included complete shutdown of Hydro-Quebec power grid due to an event on March 13, 1989 (8 million people without power); a satellite loss by Inmarsat; many reports of single event effects from various satellites; operational problems with LORAN network and worldwide HF communications; and even astronauts onboard Atlantis reported "irritating flashes" in their eyes due to energetic protons penetrating the optic nerve.

4.2.3 Other Examples of Radiation Environments in Space

There are several other mechanism that can produce radiation environments affecting missions in space. First of all, there are Cosmic Rays (CRs). These are energetic particles generated by supernova. The composition of CRs is dominated by protons (83%), alphas (13%), electrons (3%), and heavier ions (1%) through to uranium. These are extremely relativistic particles. The highest energy ever measured was 3.2×10^{20} eV or 50 Joules (from a single particle!). Proton energy distribution peaks at $\sim$ 0.3 GeV. Cumulative effects due to CRs are not significant, but individual particles can cause single event damage in electronics. Space missions are partially shielded by the Earth's magnetic field, depending on their specific orbits. When CRs strike the upper atmosphere they create a "shower" of highly energetic particles. These particles were measured on the surface of the Earth and are known to produce undesirable effects in electronics on the ground and in airplane avionics systems.

Missions to other planets must take into account ionizing dose due to Van Allen belts of those planets. This is especially critical for Jupiter and Saturn. Jupiter's magnetic field is significantly stronger than the Earth's, which translates into a radiation environment, that is about 1000 times worse than the Earth's. The belt primarily consists of high-energy electrons (up to 100s of MeVs). Io's "disk" may also contain high-energy sulfur and oxygen. The total dose for a mission to Europa is estimated as $\sim$ 4 Mrad (Si) for 100 mils of aluminum shielding. Inside Jupiter missions expect radiation environment of 250 krad (Si).

Nuclear weapons can create both prompt (short time duration) and long-lasting radiation environments in space. The prompt environments for space systems consist of X-rays, γ-rays, neutrons, and ionized debris. The long term environment is a result of "pumping" the radiation belts with additional electrons that stick around for years. The Starfish nuclear event in 1962 is blamed for the death of 7 satellites within 7 months, of which Telstar was lost due to TID damage to the command

decoder, while other losses were due to radiation damage to solar arrays shortening the satellite lifetime. Current estimates suggest that a 10 kT explosion at 150 km over Japan would kill virtually all low Earth orbit satellites within 1-2 months.

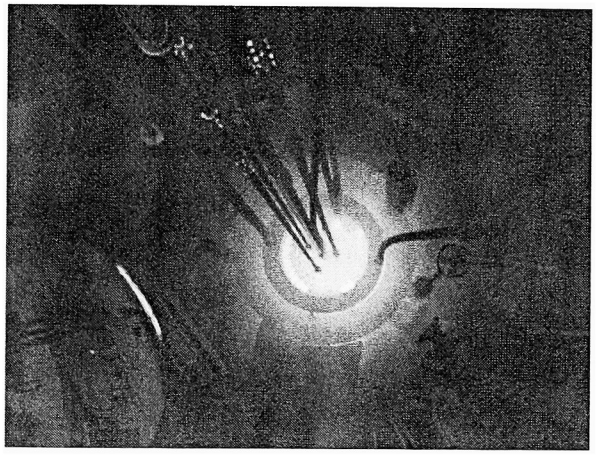

Figure 4.3: Nuclear fuel inspection setup.

4.2.4 Radiation Environments on Earth

Examples of extremely hostile radiation environment can also be found on Earth, for instance, in medicine, specifically, in oncology treatment systems. In this case, one has a linear accelerator producing ultrarelativistic electrons, which bombard a metal target and emit bremsstrahlung γ-radiation. The latter irradiates the tumor area, whereas the healthy tissue is protected by a tungsten shield. The position of the shield needs to be monitored in real time to verify that the healthy tissue is not exposed to γ-rays due to some accidental movement of the system or a patient. The camera observing the shield has to be radiation hardened as it is constantly exposed to highly energetic recoil particles including X-rays.

Not surprisingly, radiation hardened cameras can find a number of applications in nuclear power plants. The cameras can be used in those locations of the power plant that have life threatening levels of radiation flux during reactor operation, to monitor

various gauges and verify the integrity of the facility (promptly detect leaks, fire etc.). Nuclear fuel inspection (Fig. 4.3) as well as detection of structural faults (such as rust and cracks) in those elements of the plant, that are subject to irradiation even during the outage cycles, also require radiation hardened imaging equipment.

4.3 Radiation Damage to Semiconductor Devices

It is generally perceived that semiconductor based devices (e.g., photo-sensors) cannot be used in radiation environments due to fast and severe degradation. There are important exceptions from this rule. CIDs has long been used in radiation environments (cf. Sect. 3.1) and proved to be extremely useful in all the applications described above. Advances of semiconductor technology further improve radiation tolerance of CID devices as higher quality gate oxide usually results in better radiation tolerance.

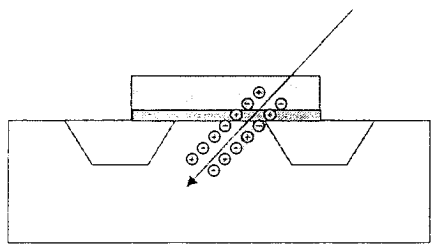

Figure 4.4: Interaction of an energetic particle with an MOS device.

The typical process resulting in a damage to an MOS device is shown in Fig. 4.4. Most of the energy of highly energetic particles incident on a chip is dissipated through ionization processes (creation of electron-hole pairs). Electrons and holes that are born in silicon manifest themselves as additional "signal", the so-called scintillation (or radiation-induced shot) noise. Electrons that are born in the oxide get swept out of it, while holes that are born in the oxide get stuck there and migrate towards the Si/SiO_2 interface. These holes result in increased leakage current and also in the change of transistor threshold voltage.

Certain interaction events, especially involving fast protons, may result in silicon

crystal lattice damage. CCDs and solar cells are particularly sensitive to this effect. As a result of an especially unfortunate hit, when a highly energetic particle strikes a sensitive node of a chip, its elements can be completely destroyed (for instance, if gate oxide of a transistor is ruptured and broken-down). This effect becomes more significant as critical dimensions of chip elements become smaller.

Furthermore, ionization processes in optical elements (lenses, mirrors, beam splitters etc.) lead to their browning and parasitic light attenuation. This emphasizes photo-detector sensitivity and noise requirements.

4.4 ColoRAD Radiation Tests

The results of a radiation test of a commercially available CCD camera are presented in Fig. 4.5. On the left-hand side of Fig. 4.5 color CCD image of a test chart is shown in the beginning of irradiation by γ-quanta. Incident radiation flux is 30 krad/hr and the accumulated dose is 0. The picture on the right-hand side is taken 1 hour later, i.e. the camera accumulated about 30 krad of ionizing dose. It is clear that at this point the degradation of the CCD is severe and the image it produces is no longer useful. It was precisely this kind of CCD camera behavior in radiation that motivated attempts to design radiation hardened cameras based on CID technology.

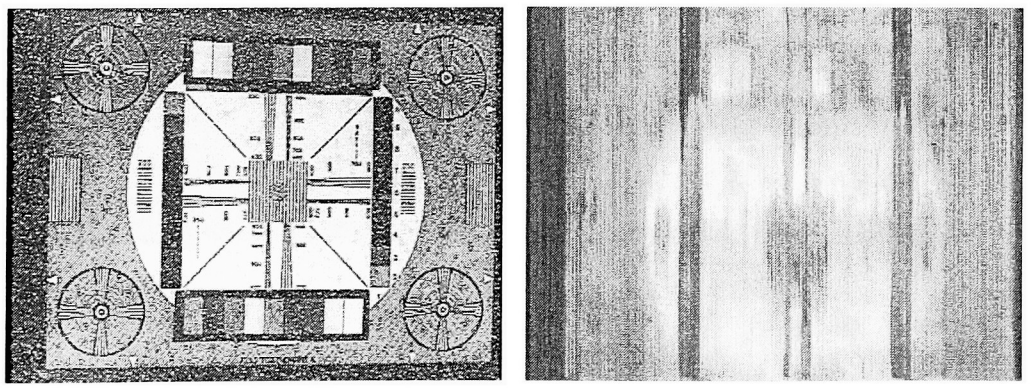

Figure 4.5: Radiation test of a CCD camera: TID=0 and γ-flux=30 krad/hr on the left panel; TID=30 krad (1 hour later) on the right panel.

The ColoRAD video cameras were subject to several radiation tests. Let us describe some results observed in those tests.

4.4.1 First Radiation Test

The first test was performed at the University of Maryland in April of 2005. The maximum radiation flux achievable at this facility was 35 krad/hr. Six cameras subject to the test received an accumulated dose of 1 Mrad. At the end of the test all cameras were fully operational while producing satisfactory video. The still frames captured in this test are shown in Fig. 4.6 and should be contrasted with those in Fig. 4.5. In this case we have an imager with synthesized colors and MTF structures as described in Sect. 3.6. The left-hand side panel of Fig. 4.6 was captured before the beginning of the test (at TID=0 and γ-flux=0), while the slide on the right was taken in the end of the test (at TID=1 Mrad) with sources still present and producing γ-flux of 22 krad/hr. In spite of the bad row that developed as a result of the radiation-induced stress, the camera still produced good quality video. It should be noted that an initial defect of this row is visible faintly on the left-hand side of Fig. 4.6.

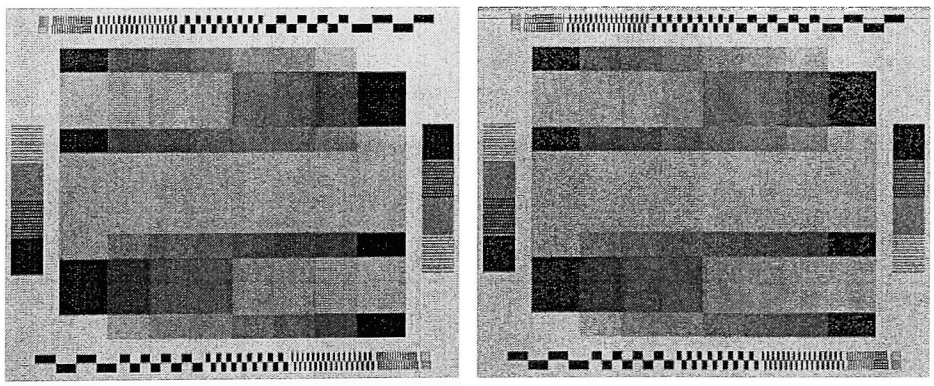

Figure 4.6: Radiation test of a CID camera with MTF/Synthesized colors mask imager. TID=0, γ-flux=0 on the left-hand side. TID=1 Mrad, γ-flux=22 krad/hr on the righ-hand side.

Signal-to-noise ratio was measured in the color channel with color subcarrier trap

filter and weighting filter turned "on" as a function of dose at γ-flux=22 krad/hr, and as a function of γ-flux at TID=0. These results are shown in Tab. 4.1. Several important observations have to be made. First, there is a big drop in SNR (58 to 41 dB) as soon as γ-radiation is turned "on" (flux rises above zero). This means that already at γ-flux=6.7 krad/hr the scintillation noise dominates all the noise sources inherent to the camera. Second, the dependence of SNR on the accumulated dose is flat. There is no degradation of SNR (at least at flux=22 krad/hr) with dose. On the contrary, a small improvement of SNR (from 38 to 40 dB) is observed. This behavior is spurious and is due to the fact that the camera gain decreases with dose, which reduces noise, while numbers in Tab. 4.1 are obtained under assumption that the full-level signal is always 700 mV. This point will be further illustrated by test results below. Third, the dependence of SNR on the γ-flux also appears to be much more flat than one would expect given that the random noise due to radiation events is the dominating noise source. For instance, for the square root dependence the difference in SNR at γ-flux=6.7 krad/hr and 35 krad/hr must be 7.2 dB, while we observe only 4.5 dB. The possible reason for this effect will be discussed after the results of the following radiation test are described.

TID (krad)	0	420	500	840	1000
SNR (dB)	38	39.5	39.5	40	40
γ-flux (krad/hr)	0	6.7	13.3	22	35
SNR (dB)	58	41	41	38	36.5

Table 4.1: SNR data from the first University of Maryland test. Top 2 rows are at γ-flux=22 krad/hr. Bottom 2 rows are at TID=0.

4.4.2 Second Radiation Test

The second radiation test was performed at the Osaka Prefecture University in July of 2005. In this case, 2 cameras were subject to irradiation and the total dose of 2.85 Mrad was achieved. The results of the SNR measurements (in dB) for one of the

cameras are presented in Tab. 4.2.

	0	510	1070	1730	2360	2850
0	62.6	57.5	55.6	55.7	56.8	56.4
10	45.3	43.9	46.3	48.5	50.5	
20	43.2	42.1	45.3	47.2	49.6	
50	41	40.1	43.6	46.2	49.1	
100	40.5	39.6	42.3	44.9	48.2	

Table 4.2: SNR data (in dB) from the second radiation test performed at the Osaka Prefecture University. Top row shows TID in krad. Left column shows γ-flux in krad/hr.

Once again the measurements were obtained from the color channel with both color subcarrier trap and weighting filters activated. The data in Tab. 4.2 show essentially the same trends as observed in the first test. The dependence of the SNR on TID at γ-flux>0 has an upward trend that likely has to do with the decrease of the overall system gain. The magnitude of this effect for TID$\leq$1070 krad is consistent with the data in Tab. 4.1 (about 2 dB by TID$\approx$1 Mrad measured at γ-flux$\approx$20 krad/hr). At γ-flux=0 the dependence on TID is reverted and SNR drops by 6 dB by the end of the test.

The dependence of SNR on the flux is also similar to the first test: there is a significant drop when γ-flux is increased from 0 to 10 krad/hr. This indicates that the scintillation noise becomes dominant as soon as it appears. Then the dependence flattens out more than the square root model would predict (in the square-root model a 10 dB differences in SNR should be observed for 10-times difference of γ-fluxes).

Our interpretation of this effect is as follows. Camera noise measurements are normally done in the dark. Hence, if the dark current is small, the average video level is zero and noise corresponds to relatively small random excursions up and down from zero. In the case of the scintillation noise the situation is different. Minority carriers generated by the ionizing γ-radiation compete with the photo-generated carriers and may account for a significant fraction of the full well. Scintillation noise rides on top

of this average scintillation signal coming from each pixel. Under these conditions the noisemeters may simply produce erroneous results (e.g., by failing to properly subtract the average video level). Alternatively, when the γ-flux is especially high the scintillation signal may be close to the pixel saturation level, which will clip off the shot noise associated with the γ-flux (if the imager is fully saturated the shot noise is zero).

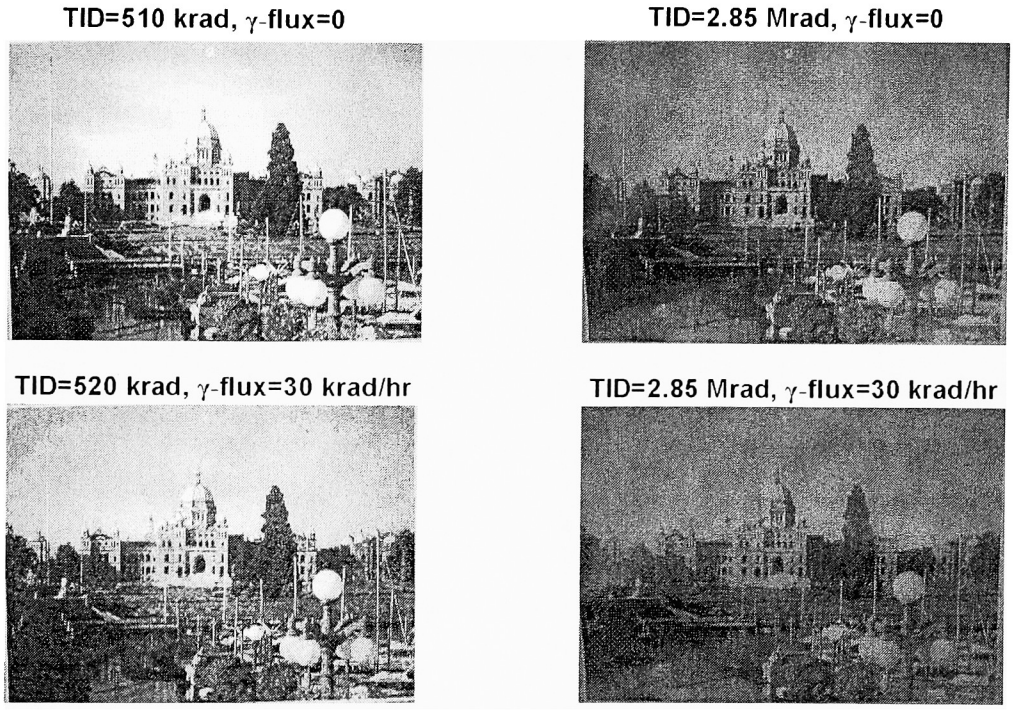

Figure 4.7: Still frame captures taken during the second radiation test.

In Fig. 4.7 we present still frame captures taken at the beginning and in the end of the test: left and right columns correspond to $\sim$ 500 krad and 2.85 Mrad total dose, respectively; and also at 2 values of γ-flux: top and bottom rows correspond to 0 and 30 krad/hr γ-flux, respectively. As one compares the slides taken at different values of flux but at the same accumulated dose, the immediate conclusion is that at 30 krad/hr the degradation of picture quality is insignificant and the color video the

camera generates is useful (cf. Fig. 4.6). In the end of the test, at TID=2.85 Mrad, the camera was still fully functional and was producing color video of reasonable quality. Unfortunately, the lens suffered significant browning after 2.85 Mrad of TID, while the light level was never adjusted to compensate for that. That is why pictures in the right column of Fig. 4.7 look darker than they should.

4.4.3 Third Radiation Test

The third radiation test was performed again at the University of Maryland in February of 2006. Three cameras were subject to the test. In this case full level video output was studied as a function of TID to get a better understanding of the camera gain decrease observed in the first and second radiation tests. The data on camera output level variation are presented in Fig. 4.8. The video level in mV is plotted versus accumulated ionizing dose in rad. Cameras A and B had MTF masks deposited on top of their imagers. They used no lenses or mirrors. Hence, the blue and pink curve behavior reflects true camera gain degradation with radiation. Camera C had certain elements in the optical path that browned as a result of irradiation (in a similar fashion as the 2.85 Mrad slides in Fig. 4.7). Hence, video output level decrease of camera C is bigger, but not all of it should be attributed to the gain degradation.

The results of the SNR measurements in the third radiation test could be summarized as follows. Brand new ColoRAD cameras in the absence of radiation show SNR of about 60 dB in monochrome and about 50 dB in color channel. As soon as the radiation flux of about 35 krad/hr is applied, SNR drops in the monochrome channel to about 40 dB and in the color channel to about 36 dB. As long as the radiation flux is present there is very little dependence of SNR on the total dose (by TID=4 Mrad SNR increases by about 5%). The small increase of SNR with the dose should be attributed to camera gain degradation (see above). After the radiation flux is removed SNR increases to about 52 dB in the monochrome and to about 46 dB in the color channel. The fact that these numbers are about 4-8 dB smaller than the

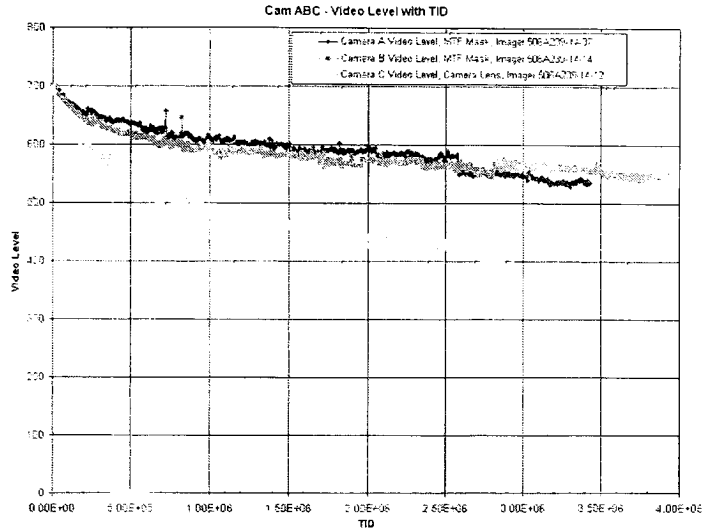

Figure 4.8: Camera video output level in mV as a function of TID in rad. Cameras A and B had MTF/Synthesized colors imagers. Camera C had a lens and a special light source, both of which browned in radiation.

corresponding numbers in the beginning of the test is likely due to increased FPN of the irradiated imagers and a deficiency of CDS control algorithm that precludes CDS from removing FPN as effectively as it does before irradiation (e.g., source follower runs out of headroom, becomes unable to fully charge CDS capacitors, and is also responsible for reduced camera gain discussed above).

Summarizing the above, all 3 cameras successfully survived till the end of the test while producing color video of excellent quality. Camera B reached TID of 4 Mrad. The AGC circuit in CCU (Sects. 3.5, 3.6) was disabled in all 3 radiation tests. Had it been enabled, the camera gain degradation and optics browning, discussed above, would not have been noticeable to the end user. The camera would have to slightly boost the gain to compensate for these deficiencies. Furthermore, the dark frame cancellation block in CCU (Sect. 3.5) was also not enabled. When this block comes on-line, the problems, associated with the extra FPN after irradiation, are expected to go away. At this point we are unaware of any other possible imager and camera

failure mechanisms in radiation.

Conclusion

We have studied theoretically the linearity of an active CID pixel. It is shown that the response curve can exhibit a dual-slope characteristic. The dual slope is an indication of incomplete removal of the photo-charge from the sense gate due to the voltage increase of the latter. The dual slope can occur when the charge is transferred from the sense gate to either the lateral drain (DRO) or to the storage gate (for NDRO purposes). In the latter case the second slope increases with increase of the storage gate size in contrast with the charge sharing scenraio. In the limit of very big storage gate the second slope approaches that for the DRO regime. The theoretical findings were illustrated by and shown to be in good agreement with the experimental data The second slope can be removed by careful gate sizing, parasitic capacitor sizing, adjustment of the gate voltages, or by skimming off the excess charge during the integration.

We have presented the color video sensor CID25 and the color video camera ColoRAD based on it. The sensor is equipped with the preamplifier-per-pixel technology, on-chip CDS circuitry and parallel row processing to achieve high conversion gain and low noise. The saturation of the monochrome imager (without IR cutoff and color filters) operated at pixel full well in the RS170 mode was observed at 0.35 ft-c of light with SNR of 59 dB. The saturation of the monochrome imager operated at $1/12^{th}$ of the pixel full well in the RS170 mode was observed at 0.03 ft-c of light with SNR of 37 dB. The second set of numbers indicated that the imager was capable of operating at very low light levels while producing a picture of fully adequate quality.

Using the test slides it was established that the system had single pixel resolution

and resolved at least 450 TV lines. Consequently, color was easily produced once the color filters were deposited. The saturation of the color imager (with IR cutoff and color filters) operated at pixel full well required 3 ft-c of light with SNR of 41 dB. With the color subcarrier trap filter "on", the SNR increased to 47 dB. If, additionally, the weighting filter was turned "on" the SNR rose to 58 dB.

The CID25 video imager and the head part of the camera were shown to be radiation hardened. In one radiation test the ColoRAD camera produced adequate color video out to 4 Mrad of total dose of ^{60}Co γ-radiation with insignificant SNR degradation. The picture quality was shown to be acceptable in the presence of γ-flux of up to 35 krad/hr.

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