8-15-2014

# Design and Simulation of Short Channel Si:HfO2 Ferroelectric Field Effect Transistor (FeFET)

Idris H. Smaili

# Design and Simulation of Short Channel Si:$HfO_2$ Ferroelectric Field Effect Transistor (FeFET)

By

Idris H. Smaili

A Thesis Submitted
in Partial Fulfillment
of the Requirements for the Degree of
Master of Science
in Microelectronic Engineering

Approved by:

Professor: _____
Dr. Santosh K. Kurinec (Thesis Advisor)

Professor: _____
Dr. Robert Pearson (Thesis Committee Member)

Professor: _____
Dr. Karl D. Hirschman (Thesis Committee Member)

Professor: _____
Dr. Ivan Puchades (Thesis Committee Member)

Approved on: Aug 15, 2014

DEPARTMENT OF ELECTRICAL & MICROELECTRONIC ENGINEERING
KATE GLEASON COLLEGE OF ENGINEERING
ROCHESTER INSTITUTE OF TECHNOLOGY
ROCHESTER, NEW YORK

# Design and Simulation of Short Channel Si:$HfO_2$ Ferroelectric Field Effect Transistor (FeFET)

By

Idris H. Smaili



_____ _____

Idris H. Smaili Date

# Dedication

***I dedicate this thesis to my family: my father, my mother, my wife and my sons. Without your encouragement and support this work would not have been possible.***

# Acknowledgements

I would like to thank my advisor Dr. Santosh Kurinec for her support and guidance over the past years. Dr. Kurinec's encouragement and insistence on student involvement and collaboration with academic and industrial research has opened many doors. I would also like to thank Dr. Robert Pearson, Dr. Karl Hirschman and Dr. Ivan Puchades, my thesis committee members for their assistance and continuing support.

I would like to acknowledge my fellow graduate students in the Microelectronic Engineering program at RIT. I would especially like to thank Varun Ashok. He was always there to listen to my ideas, to offer suggestions and to answer any questions.

I gratefully acknowledge the academic donation of Silvaco TCAD tools by Silvaco used in this study.

# Abstract

Non-volatile memories using ferroelectric capacitors, known as Ferroelectric Random Access Memory (FRAM) have been studied for many years, but they suffer from loss of data during read out process. Ferroelectric Field Effect Transistors (FeFETs), which are based on ferroelectric gate oxide, have been of recent interest for non-volatile memory applications. The FeFETs utilize the polarization of the ferroelectric layer incorporated into the transistor gate stack to control the channel conductivity. Therefore, in FeFET devices, the read out process is non-destructive because it is only processed by measuring the resistivity in the channel region. The drain current-gate voltage ($I_D$-$V_G$) characteristics of FeFETs exhibit a voltage shift due to polarization hysteresis known as the "memory window", an important figure of merit of a FeFET that provides a window for the read voltage. A dielectric layer between semiconductor layer and the ferroelectric is required to reduce charge injection effect, and to compensate lattice mismatch between the ferroelectric and the semiconductor. In addition, a non-ferroelectric interfacial layer may form between the semiconductor and the ferroelectric layer. However, this dielectric layer causes a voltage drop since the system becomes equivalent to two serial capacitors. It also causes an electric field that opposes the polarization. Using a high permittivity material such as $HfO_2$ reduces the voltage drop and the effect of depolarization.

To date, the majority of the work involving FeFETs has been based on conventional ferroelectric materials such as Lead Zirconate Titanate (PZT) and Strontium Bismuth Tantalate (SBT). These materials are not compatible with standard IC processing and furthermore scaling thicknesses in PZT and SBT result in loss of polarization

characteristics. Recently, ferroelectricity has been reported in doped hafnium oxide thin films with dopants such as Si, Al, and Gd. Particularly, silicon doped hafnium oxide ($Si:HfO_2$) has shown promise. In this material, the remnant polarization considerably increases by decreasing the layer thickness. The lower permittivity of $Si:HfO_2$ compared to that of PZT and SBT, allows to employ thinner films that reduce fringing effects.

This study focuses on employing $Si:HfO_2$ in short channel FeFETs. The study has two major objectives. First, to show that short channel FeFETs can be accomplished with large memory window. Second, to demonstrate the role of bulk layer thickness and permittivity on FeFET performance.

N-channel metal oxide semiconductor FET (N-MOSFET) with printed channel length of 26 nm has been designed with $Si:HfO_2$ as the ferroelectric layer, and TiN as the gate electrode. The effects of buffer layer thickness and permittivity and ferroelectric layer thickness on the memory window have been explored using Silvaco Atlas software that employs ferroelectric FET device physics developed by Miller et al. Polarization characteristics reported for $Si:HfO_2$ have been incorporated in this model. The simulations performed in this study have shown that using $Si:HfO_2$ as a ferroelectric material makes it possible to accomplish short channel FeFETs with good performance even without using buffer layers. This means it is possible to minimize depolarization effects. Using $Si:HfO_2$ as a ferroelectric layer makes it possible to accomplish highly scaled and ultra-low-power FeFETs.

# Table of Contents

# List of Figures

# List of Tables

# List of Symbols

| | |
|---|---|
| $P_s$ | Spontaneous polarization |
| $P_r$ | Remnant polarization |
| $E_c$ | Coercive field |
| $V_g$ | Gate voltage |
| $I_d$ | Drain Current |
| $\Phi$ | Electric potential |
| E | Electric field |
| $\rho$ | Charge density |
| $\varepsilon$ | Semiconductor permittivity |
| q | Electron charge |
| p | Holes |
| n | Electrons |
| $N_d^+$ | Charge density of ionized donors |
| $N_a^-$ | Charge density of ionized acceptors |
| $\mu_p$ | Hole mobility |
| $D_p$ | Hole diffusivity |
| $\mu_n$ | Electron mobility |
| $D_n$ | Electron diffusivity |
| D | Diffusion coefficient |
| $\mu$ | Mobility |
| $G_p$ | Generation rate of excess holes |
| $G_n$ | Generation rate of excess electrons |
| $R_p$ | Recombination rate of holes |

| | |
|---|---|
| $R_n$ | Recombination rates of electrons |
| $J_p$ | Current density of holes |
| $J_n$ | Current density of electrons |
| $P_d$ | Position dependent dipole polarization |
| $P_{sat}$ | Saturated loop polarization |
| $\Gamma$ | Unity function |
| $\xi$ | Polarization direction |

# List of Acronyms

| | |
|---|---|
| FeFET | Ferroelectric Field Effect Transistor |
| Si:$HfO_2$ | Silicon doped hafnium oxide |
| SCE | Short Channel effects |
| PZT | Lead Zirconate Titanate |
| SBT | Strontium Bismuth Tantalate |
| MFS | Metal Ferroelectric semiconductor |
| MFIS | Metal Ferroelectric Insulator Semiconductor |
| MSM | Metal Ferroelectric Metal |
| MFMIS | Metal Ferroelectric Metal Insulator Semiconductor |
| QMFeFET | Quantum Metal FeFET |
| ITRS | International Technology Roadmap for Semiconductors |
| VWF | Virtual Wafer Fab |
| MW | Memory Window |
| NCFET | Negative Capacitance FET |
| FTJ | Ferroelectric Tunnel Junction |

# CHAPTER 1 - INTRODUCTION

This chapter gives an introduction to ferroelectric materials and their applications to achieve non-volatile memories. It subsequently develops the primary focus of the study in this thesis.

## 1.1 Introduction and Motivation:

Ferroelectricity is a property of certain materials in which they possess a spontaneous electric polarization that can be reversed by the application of an external electric field. Ferroelectric materials were discovered during studies of Rochelle salt. These materials have the ability to show reversible and spontaneous polarization even when there is no electric field and are characterized by a characteristic polarization hysteresis loop. Above the Curie temperature of a ferroelectric material, it can be polarized under an electric field, i.e. paraelectric material. This is because of the change in the structure at this transition temperature. On the other hand, ferroelectric materials show spontaneous polarization below the Curie temperature.

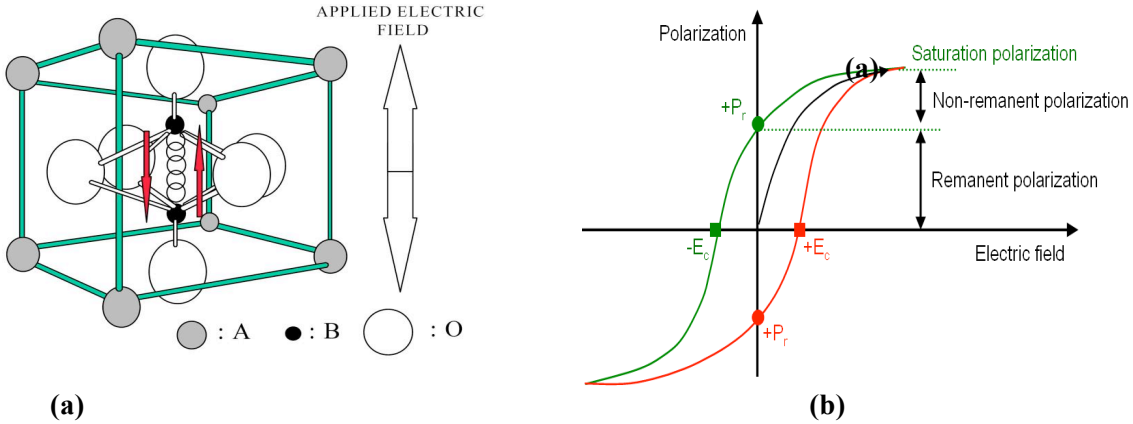



**Fig. 1.1. (a) $ABO_3$ perovskite unit cell; (b) Polarization – Electric field hysteresis [1].**

This occurs as a result of the displacement of the central ion in a crystal unit cell as seen in Fig. 1.1 [2]-[4]. The main advantage of ferroelectric materials is their ability to maintain a memory state. The hysteresis of polarization with electric field is the key to memory applications.

It has been a growing trend in modern times to develop ferroelectric memories that can keep data without changing state. The main advantage of integrating ferroelectric materials with FETs is that the reading process is a non-destructive process. Fig. 2.1 shows the landscape of ferroelectric-based semiconductor devices.

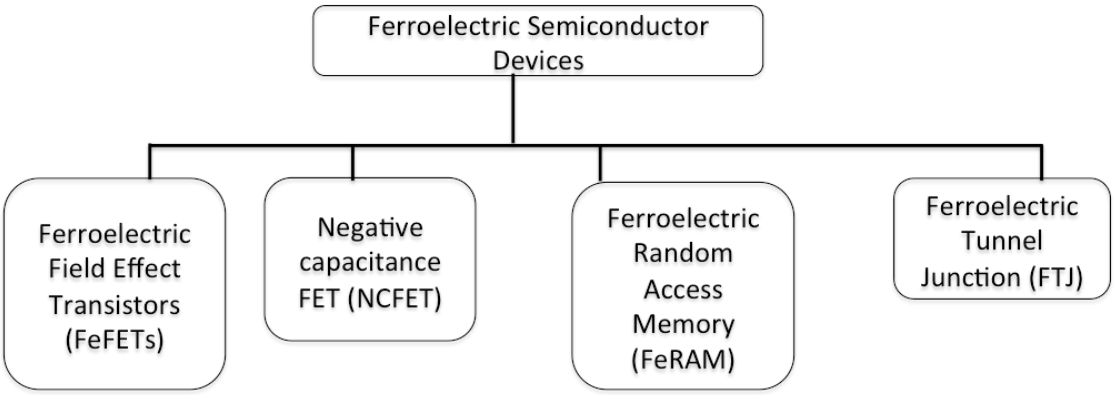



**Fig. 1.2. Ferroelectric based semiconductor devices.**

FeRAM is a ferroelectric capacitor that is combined with a MOSFET in a random access memory circuit. These types of devices suffer from loss of data during the readout process. Therefore, it was necessary to find a new approach in order to keep data without change. In FeFET devices, the typical ferroelectric capacitor is replaced with a ferroelectric –gate field effect transistor. FeFET devices depend on the resistance between source and drain during the reading process to indicate the data state of “0” or “1”. Thus, it is possible to avoid data loss [5].

## 1.2 Scaling Theory:

The scaling of CMOS devices in microelectronics is driven by the performance metrics and the integration density. Several rules of scaling have been proposed to study the effect of size reduction. The first rules were introduced by R. H. Dennard (1974) as seen in Table 1.1.

**Table 1.1: Main scaling rules of MOSFETs [6]**

| Device Parameter | Scaling Factor |
|---|---|
| Dimensions (L, W, $X_{ox}$ and $X_j$) | 1/K |
| Area | $1/K^2$ |
| Packing Density | $K^2$ |
| Bias Voltage and $V_t$ | 1/K |
| Bias Currents | 1/K |
| Power Dissipation | $1/K^2$ |
| Capacitance | $1/K^2$ |
| Electric Field Intensity | 1 |
| Body Effect Coefficient | $1/K^{0.5}$ |
| Transistor Transit time | 1/K |
| Transistor Power Delay Product | $1/K^3$ |

Where K is the scaling factor and it can be calculated as following:

$$K=\frac{Old\ \text{Size}}{New\ \text{Size}} \qquad (1.1)$$

Since the ultimate limit for the scaling is determined by physical parameters, the scaling rules in Table 1.1 do not show limits for the MOSFETs scaling.

## 1.3 Focus of this Study:

This work studies designing and simulation of a short channel Si:$HfO_2$ Ferroelectric Field Effect Transistor (Si:$HfO_2$ FeFET). The proposed device is mainly based on ferroelectric gate oxide.

Silvaco Atlas has been used to simulate this device and to study the polarization and hysteresis characteristics. FeFETs are novel and promising devices since they provide fast and non-volatile memories, which would be a major technological advance. A short channel device has been chosen to be studied in order to match the International Technology Roadmap for Semiconductors (ITRS). This device has been simulated with silicon doped hafnium oxide (Si:$HfO_2$) as a ferroelectric layer. The polarization characteristics of this material have been studied with short channel FeFETs. This is important because the ferroelectric material can significantly affect the FeFET performance.

The main goal of this work is to accomplish short channel FeFETs that have large memory windows by using Si:$HfO_2$ as a ferroelectric layer. The second goal of this work is to investigate the role of using a buffer layer with Si:$HfO_2$ as a ferroelectric material.

# CHAPTER 2 - BACKGROUND INFORMATION

This chapter focuses on ferroelectric materials and their applications. It provides additional details beyond what was described in Chapter 1. Section 2.1 discusses the properties of ferroelectric materials. Section 2.2 explains the basics of FeRAM device and its limitations. Section 2.3 describes the concept of FeFETs and the advantages of these kinds of devices. Section 2.4 covers the electrostatics of Metal-Insulator-Ferroelectric-Semiconductor (MFIS) FeFETs. Sections 2.5 discusses the current-voltage characteristics of FeFETs. Section 2.6 explains the depolarization, charge injection and trapping effects. Section 2.7 covers the evolution of FeFET devices on conventional perovskite materials. Section 2.8 discusses the limitations of $PbZn_{1-x}Ti_xO_3$ (PZT) and $SrBi_2Ta_2O_9$ (SBT) ferroelectric materials. Section 2.9 gives a literature review about ferroelectricity in silicon doped hafnium oxide ($Si:HfO_2$).

## 2.1 Ferroelectric Materials:

Most Ferroelectric materials have perovskite crystalline structure. The perovskite structure has the general stoichiometry $ABO_3$, where "A" and "B" are cations and "O" is an anion. The atom in the middle has two stable low energy levels as seen in Fig. 2.1. When an electric field is applied, the middle atom moves in the same direction as that of the electric field resulting in polarization. The two states of the middle atom are typically classified as up polarization and down polarization according to the position of the atom. Fig. 2.1 shows the two states of the middle atom in a perovskite barium titanate ($BaTiO_3$) ferroelectric material.

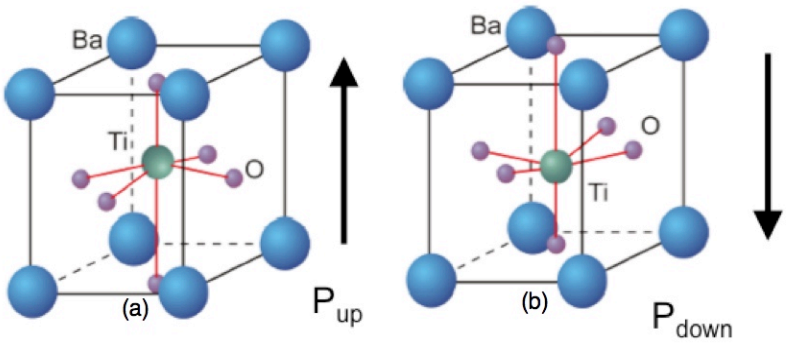



**Fig. 2.1. States of middle atom in $BaTiO_3$ (a) up polarization (b) down polarization [7].**

Ferroelectric materials typically show spontaneous polarization, which means that the ferroelectric material is able to get polarized even when the applied electric field is equal to zero. This property is known as ferroelectricity, which is caused by the presence of permanent dipole moment. In ferroelectric materials, there are certain regions, i.e. domains, where in all dipoles are pointed in certain directions. When there is no applied electric field, the net polarization is equal to zero due to random orientations of domains as seen in Fig. 2.2(a). When an external electric field is applied, dipole moments rotate to align themselves along the electric field forming a bigger region that has a net dipole moment oriented in a single direction as seen in Fig. 2.2(b) [5]

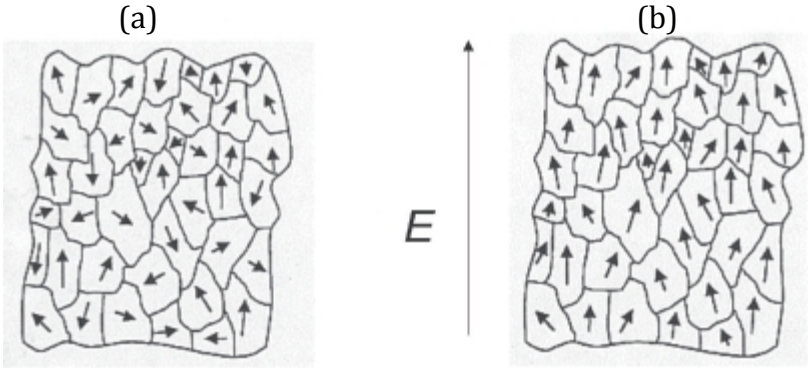



**Fig. 2.2. Ferroelectric domains concept.**

These created domains do not disappear when the electric field is removed. The hysteresis effect results by these irreversible polarization processes as shown in Fig. 2.3. Small displacements that occur in weak electrical fields are reversible. Remnant polarization ($P_r$) refers to the polarization value when there is no applied electric field.

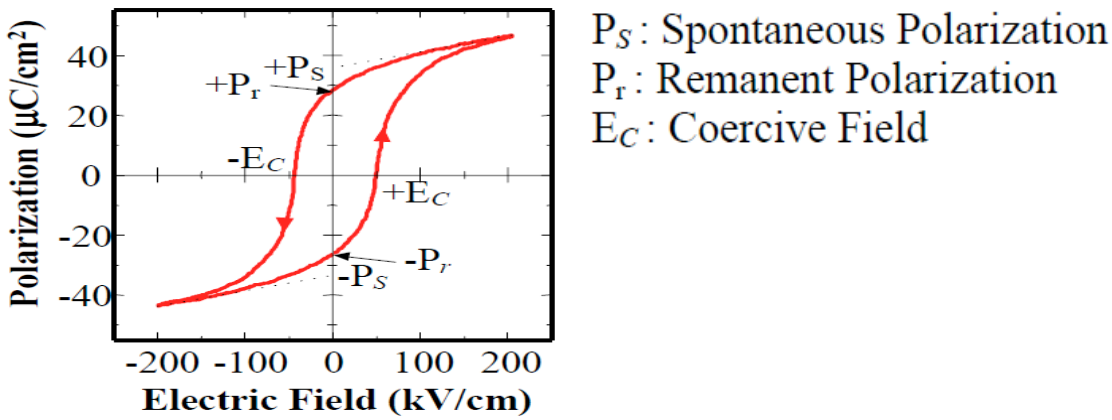



**Fig. 2.3. Typical curve of polarization hysteresis loop [1].**

The strength of the electric field that is needed to bring back the polarization to zero is known as coercive field ($E_c$). To switch the state of a ferroelectric device, the threshold electric field should be greater than the coercive field ($E_c$). If the electric field is applied in the same direction of the previous applied electric field, no switching will take place and the charge will still be the same [5].

Shur, Makarov and Volegov (1995) developed a method to estimate domain kinetics of ferroelectric materials. In their results, they found that it is possible to estimate domain kinetics in real devices and to produce devices with controlled domain structure. It is important to understand that domain kinetics differ with regard to the type of ferroelectric material which can significantly affect the device performance [8].

Two most widely studied ferroelectric materials are $PbZn_{1-x}Ti_xO_3$ (PZT) and $SrBi_2Ta_2O_9$ (SBT). They both have perovskite structure. PZT is a more classic type of ferroelectric whereas SBT is a layered perovskite. In PZT, the zirconium and titanium in the lattice have two stabilization points. They can move between the points according to the external electric field resulting in polarization. An electric polarization of PZT (shift up/down of Zr/Ti atom) remains after applying and removing an external electric field, from which a nonvolatile property results. Typically, ferroelectric materials show ferroelectricity below a certain transition temperature, which is also known as the Curie temperature. PZT is an intermetallic inorganic compound that shows a marked piezoelectric effect. PZT material shows larger spontaneous polarization and it has a high polarization coefficients. Its transition temperature is about 370 °C. The properties of PZT depend on the composition of the alloy. Currently, high switchable polarization and clearly defined switching are offered by employing Ti/Zr ratios of 60/40 and 70/30 [5]. Fig. 2.4 shows the crystal structure of PZT material.

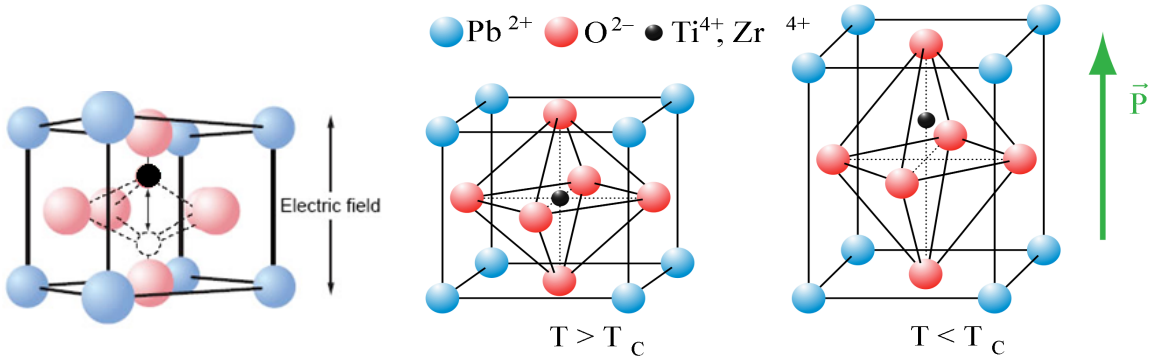



**Fig. 2.4. The crystal structure of PZT showing movement of Ti/Zr ion that result in two states of polarization for temperatures below the Curie temperature [9].**

In the layered perovskite structure of the SBT, the perovskite unit cells (SrTaO) are interrupted with bismuth oxide layers. Refer to Fig. 2.5 for the structure of SBT where a

half unit cell is displayed [10]. SBT material has few allowed directions of spontaneous polarization and it has a lower remnant polarization. Its transition temperature is about 570 °C. The advantage of this material is that it does not show polarization fatigue like PZT due to repeated switching process [5].

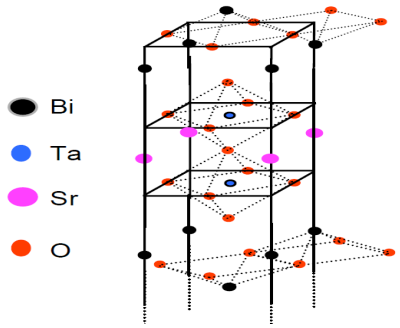
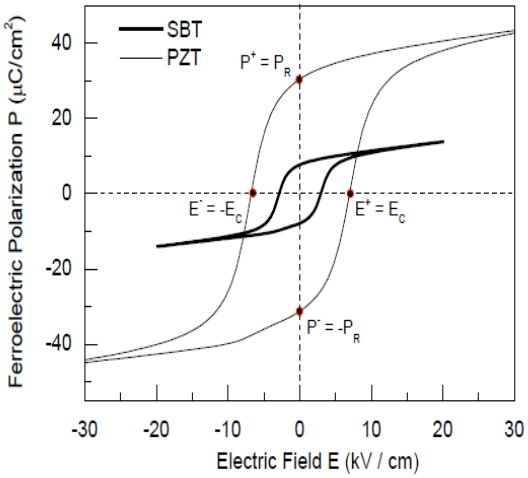



**Fig. 2.5. Crystal structure of -layered perovskite $SrBi_2Ta_2O_9$ (SBT) showing an upper half of the unit cell) [10].**

In principle, any of the above mentioned materials is suitable for the ferroelectric memory operation and is being considered for applications in the ferroelectric field effect transistors (FeFETs) too. The two materials differ in the polarization and coercive field values. Table in Fig. 2.6 shows the parameters of these two materials. Fig. 2.6 shows a comparison of polarization behavior of these two ferroelectric materials.




| Param. | Unit | PZT | SBT |
|---|---|---|---|
| $P_R$ | $\mu C/cm^2$ | 32 | 8 |
| $P_S$ | $\mu C/cm^2$ | 40 | 10 |
| $E_C$ | $kV/cm$ | 70 | 30 |
| $\varepsilon_r$ | - | 250 | 250 |

**Fig. 2.6. Polarization hysteresis loops of PZT and SBT ferroelectric thin films [11].**

## 2.2 Ferroelectric Capacitor:

A Ferroelectric capacitor is a device consisting of ferroelectric film between two electrodes. Since there are two states within ferroelectric materials, a proper electric field can be applied to polarize the capacitor either up or down as shown in Fig. 2.7.

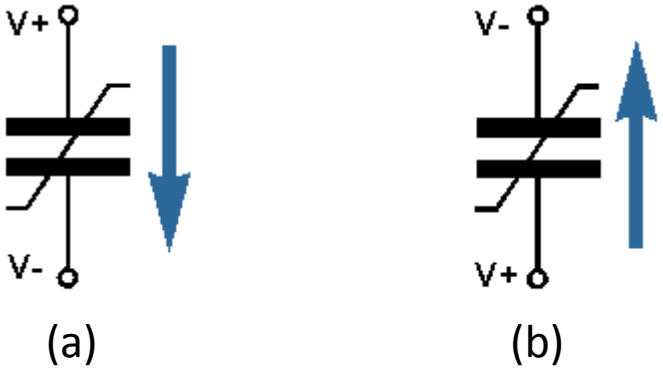



**Fig. 2.7. Polarization states of a ferroelectric capacitor [7].**

Ferroelectric capacitor can be considered as the first generation of non-volatile ferroelectric memories and it is typically addressed by using a conventional field effect transistor forming 1T-1C cell configuration as shown in Fig. 2.8 [12].

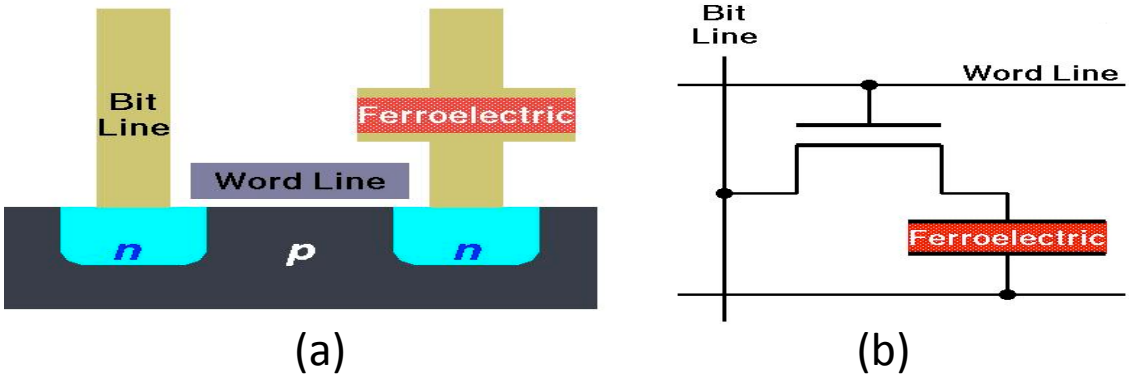



**Fig. 2.8 (a) Cross section of a 1T-1C cell structure; (b) basic memory unit cell array [13]**

The capacitance of the ferroelectric capacitor is not stable. When the capacitor is not switched, it behaves in the normal linear fashion. When it is switched, an increase in the capacitance will induce an additional charge. In a memory cell, this effect can be enabled by using an active element, i.e. a field effect transistor (FET). The individual cell can be accessed by a word line and a bit line as seen in Fig. 2.8 (b).

The read operation requires a number of stages. The bit line voltage is compared to a reference, which is set to be below the switch voltage and above the un-switch voltage. A sense amplifier is typically used to amplify the difference giving either logic "0" or logic "1". When the bit line, plate line and the word line are low, the cell will be in its inactive state as shown in Fig. 2.9 (a).

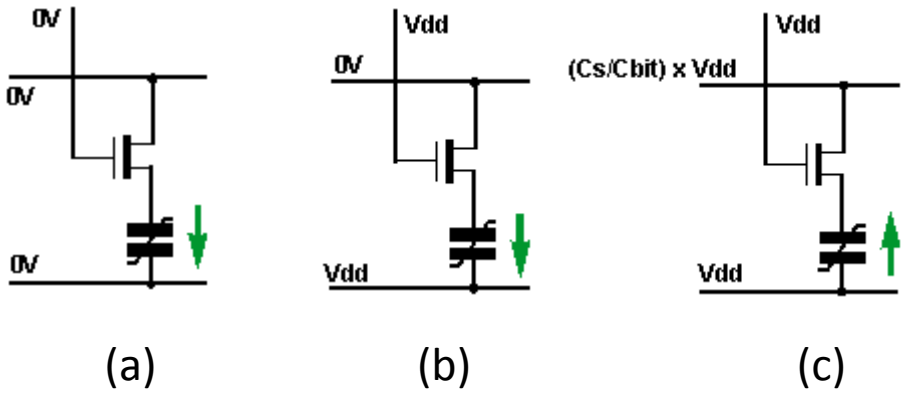



**Fig. 2.9. FeRAM read cycle [7].**

When a voltage is applied onto the word line and plate line, the access operation starts as illustrated in Fig. 2.9 (b). When a voltage is applied across the capacitor, it will either switch or not switch. When the capacitor is switched, a charge, which is shared with the bit line capacitance ($C_{bit}$), is induced as shown in Fig. 2.9 (c). The voltage on the bit line is given by:

$$V_{bit} = \frac{C_s}{C_{bit}} V_{dd} \qquad (2.1)$$

Where, $C_s$ is the capacitance of the switched ferroelectric capacitor. No additional charge is induced when the capacitor does not switch. Thus, the data within the cell can be changed during the read process. The writing process uses the same principles of the read operation. An electric field is applied in the required direction by the control circuitry to write the desired data [7].

## 2.3 Ferroelectric Field Effect Transistor (FeFET):

In a FeFET, the gate oxide of a typical MOSFET is replaced by a ferroelectric material or a stack of materials with a ferroelectric layer as shown in Fig. 2.10.

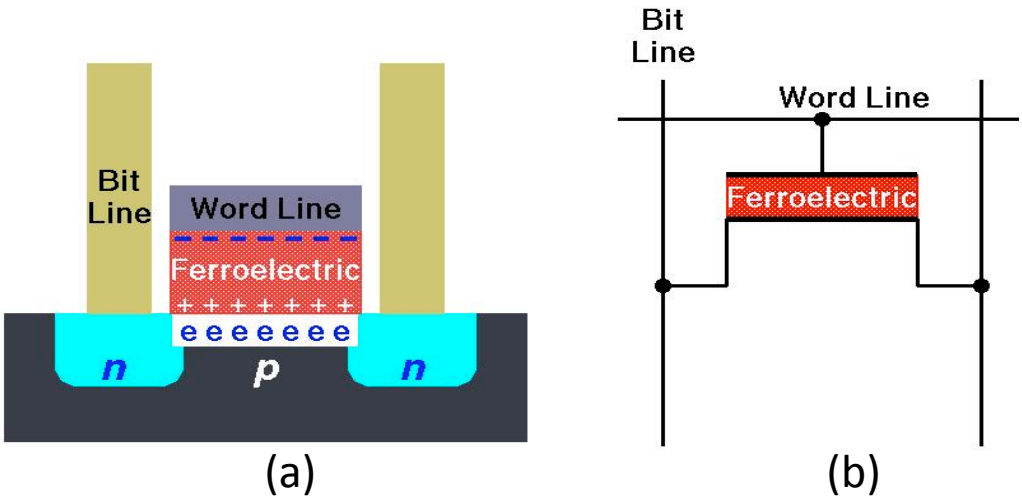



**Fig. 2.10. (a) Main structure of FeFET; (b) 1T type memory cell [13].**

The FeFET is programmed by applying a pulse to switch its polarization to "on" state that is written by its remnant polarization as shown in Fig.2.11. The off-state is written by applying a negative pulse. The read operation is carried out by applying a read voltage

at the gate that senses the channel conductivity between the source and the drain as seen in Fig. 2.12.

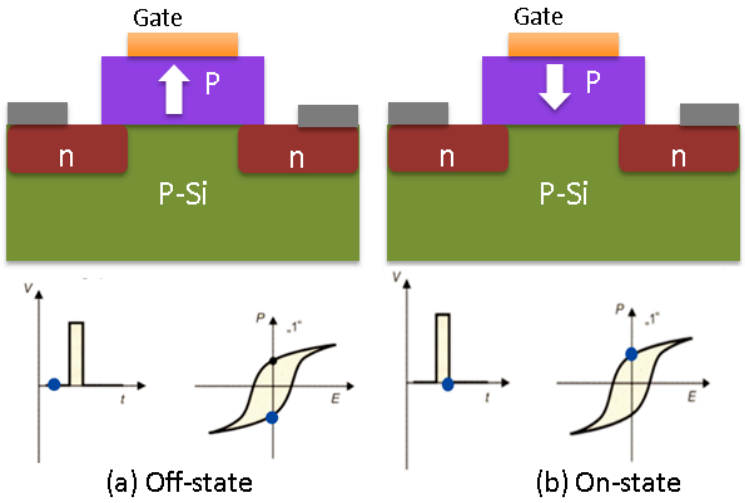



**Fig. 2.11. Schematic of programming a FeFET. (a) The device is in off-state with its polarization in negative direction; (b) application of a pulse that drives it to saturation ($P_s$) and retained at its remnant value ($P_r$).**

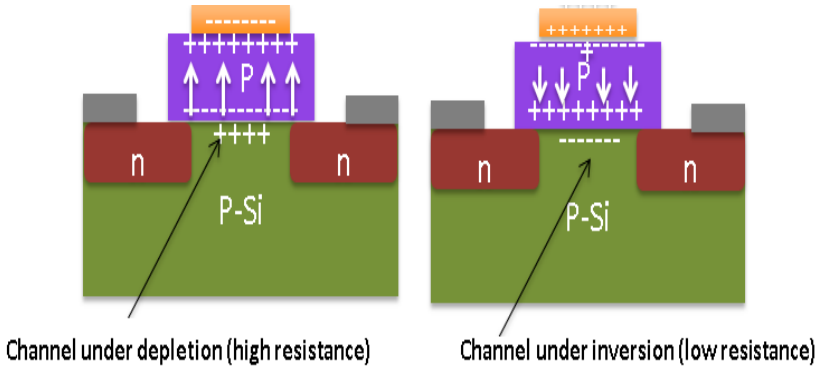



**Fig. 2.12. Schematic of reading a FeFET. The read voltage lies in the 'memory window' of the FeFET.**

## 2.4 Electrostatics of Metal-Insulator-Ferroelectric-Semiconductor (MFIS) FeFET:

Typically, an insulating interfacial layer exists between the ferroelectric layer and the semiconductor either intentionally to overcome stresses, to minimize charge injection or

to reduce interfacial reaction between the adjacent materials making it an MFIS device as seen in Fig. 2.13.

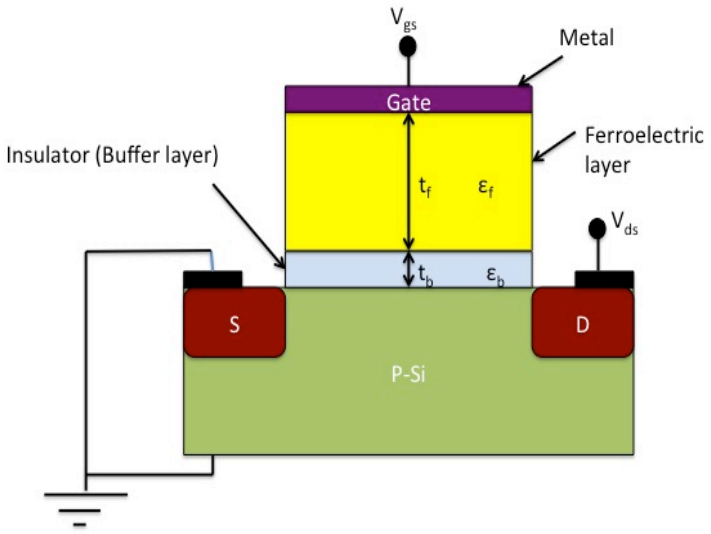



**Fig. 2.13. Schematic of a MFIS FeFET.**

For an MFIS-FeFET, shown in Fig. 2.13, the gate voltage is given as following [14]:

$$V_G = V_{FB} + V_f + V_b + \Psi_s \tag{2.2}$$

Where $V_f$ is the voltage dropping in the ferroelectric layer, $V_b$ is the voltage dropping in the insulator (buffer layer), and $\Psi_s$ is the surface potential of the semiconductor. The electric displacements can be expressed as following:

$$D_k = \varepsilon_k E_k + P_k \tag{2.3}$$

Where

$$k=\{f,b,s\} \tag{2.4}$$

Where *f, b* and *s refer* to ferroelectric layer, insulator layer (buffer layer) and semiconductor layer, respectively. $\varepsilon_k$ is the permittivity, $E_k$ is the electric field and $P_k$ represents the polarization. According to the Gauss's law:

$$\varepsilon_s E_s = Q_s(\Psi_s) \tag{2.5}$$

Where $Q_s(\Psi_s)$ is the space charge/area in the semiconductor. Thus, equation 2.3 can be rewritten as following [15]:

$$Q_s(\Psi_s) = P\left(\frac{V_f}{t_f}\right) \tag{2.6}$$

$$Q_s(\Psi_s) = \frac{\varepsilon_b}{t_b} V_b \tag{2.7}$$

The semiconductor charge density for a p-type substrate can be expressed as:

$$Q_s(\Psi_s) = \Psi_s \times \frac{\sqrt{2}\varepsilon_s}{\beta L_D}\left(\frac{n_i^2}{N_A^2}\left(e^{-\beta\Psi_s} + \beta\Psi_s - 1\right) + \left(e^{\beta\Psi_s} - \beta\Psi_s - 1\right)\right)^{1/2} \tag{2.8}$$

Where,

$$\mathrm{L}_D = \sqrt{\frac{\varepsilon_s}{qN_A\beta}} \tag{2.9}$$

$$\beta = \frac{q}{kT} \tag{2.10}$$

$L_D$ is the Debye length, $N_A$ refers to the majority carrier concentration, $n_i$ is the intrinsic carrier concentration, k is the Boltzmann constant and $Q_s$ represents the semiconductor surface charge.

$$Q_G + Q_b + Q_s = 0 \tag{2.11}$$

$$V_f = \frac{Q_G - P}{C_f} \tag{2.12}$$

$$V_b = \frac{Q_G}{C_b} \tag{2.13}$$

Where, $V_f$ is the voltage dropping in the ferroelectric layer and $V_b$ is the voltage dropping in the buffer layer. Introducing effective gate voltage :

$$V_{G,eff} = V_G + \frac{P}{C_f} \tag{2.14}$$

And stack capacitance/area;

$$C_{stack} = \left( \frac{1}{C_f} + \frac{1}{C_b} \right)^{-1} = \left( \frac{t_f}{\varepsilon_0 \varepsilon_{rf}} + \frac{t_b}{\varepsilon_0 \varepsilon_{rb}} \right)^{-1} \tag{2.15}$$

$$V_{G,eff} = V_G + \frac{P}{C_f} = V_{FB} + \psi_s + \frac{Q_G}{C_{stack}} \tag{2.16}$$

Assume $Q_i = 0$ (no interface charge) $\Rightarrow \quad Q_G = -Q_s$

$$V_{G,eff} = V_{FB} + \psi_s - \frac{Q_s}{C_{stack}} \tag{2.17}$$

$$V_{G,eff} = V_{FB} + \psi_s \pm \gamma \left[ \left( \frac{kT}{q} e^{-\frac{q\psi_s}{kT}} + \psi_s - \frac{kT}{q} \right) + e^{-\frac{2q\phi_F}{kT}} \left( \frac{kT}{q} e^{\frac{q\psi_s}{kT}} - \psi_s - \frac{kT}{q} \right) \right]^{1/2} \tag{2.18}$$

where $\gamma$ is now defined as :

$$\gamma = \frac{\sqrt{2q\varepsilon_s N_a}}{C_{stack}} \tag{2.19}$$

Where $C_s$ is the semiconductor capacitance, $C_f$ is the ferroelectric capacitance and $C_b$ is the buffer layer capacitance.

In a typical P-E hysteresis loop, as the field is ramped between large absolute values opposite in sign, the switching dipole polarization P approaches asymptotic value of $\pm P_s$, where $P_s$ is the spontaneous polarization, when all the dipoles are aligned, the resulting polarization is referred to as the saturation polarization. The polarization has a zero value

at a value of the electric field $E_c$. At zero field, the value of polarization is $P_r$, the remnant polarization. This is expressed as:

$$P^{+}(E) = -P^{-}(-E) \tag{2.20}$$

Where the plus (+) sign indicates the branch of the polarization for the positive going field ramp and the minus (-) sign indicates the negative going ramp. Various mathematical functions have been proposed to describe the hysteresis loop. The hyperbolic tangent function is chosen due to its convenient mathematical properties.

$$P^{+}(E) = P_s \tanh\left(\frac{E - E_c}{2\delta}\right) \tag{2.21}$$

Where,

$$\delta = E_c \left[\ln\left(\frac{1 + \mathrm{P_r}/P_s}{1 - \mathrm{P_r}/P_s}\right)\right]^{-1} \tag{2.22}$$

Here $P_r$, $P_s$ and $E_c$ are taken as positive quantities. Differentiating:

$$\frac{dP^{+}(E)}{dE} = P_s\left[2\delta\cosh^2\left(\frac{E - E_c}{2\delta}\right)\right]^{-1} = \frac{P_s}{2\delta}\mathrm{sech}^2\left(\frac{E - E_c}{2\delta}\right) \tag{2.23}$$

At the semiconductor ferroelectric interface:

$$\varepsilon_0\varepsilon_s E_s = \varepsilon_0\varepsilon_f E_f + P \tag{2.24}$$

Where $\varepsilon_s$ is the relative permittivity of the semiconductor and $E_s$ is the electric field in the semiconductor. Using Gauss's law

$$\varepsilon_0\varepsilon_s E_s = -Q_s = \varepsilon_0\varepsilon_f E_f + P \tag{2.25}$$

Differentiating:

$$dE_f = -\frac{dQ_s}{\varepsilon_0\varepsilon_f + \dfrac{dP}{dE_f}} = -\frac{dQ_s}{\varepsilon_{ferro}} \tag{2.26}$$

Where;

$$\varepsilon_{ferro} = \varepsilon_0 \varepsilon_f = \frac{P_s}{2\delta} \operatorname{sech}^2\left(\frac{E - E_c}{2\delta}\right) \tag{2.27}$$

This equation is used in solving the Poisson's equation in the ferroelectric region.

$$\frac{d^2\Psi}{dx^2} = -\frac{\rho}{\varepsilon_f} \tag{2.28}$$

According to equation 2.2, the ferroelectric layer in the MFIS structure adds a memory function to the MOS capacitor. Due to the hysteretic nature of the ferroelectric, the *C-V* curves are now hysteretic too and are shown in Fig. 2.14. The width of the hysteresis loop is referred to as "memory window" and can have a maximum value (for the saturated hysteresis) of ~ $2E_c \cdot t_f$ , where $E_c$ is the coercive field and $t_f$ is the thickness of the ferroelectric layer according to equation 2.29 [16].

$$\text{Saturation MW} = \text{Shift in flatband voltage} = 2E_c t_f \left(1 - \frac{\delta \varepsilon_f \varepsilon_0}{P_s}\right) \tag{2.29}$$

It should be noted that the direction in the *C-V* curve is clockwise when the semiconductor is p-type, in contrast to the counterclockwise polarization hysteresis curve [11]

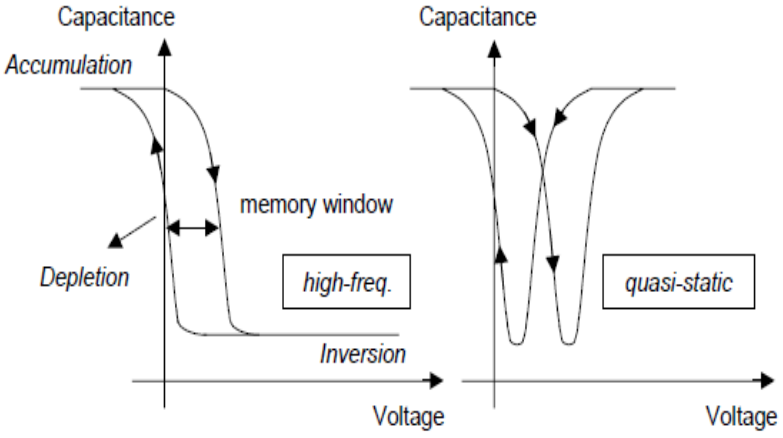



**Fig. 2.14. C-V curves of a metal-ferroelectric-insulator-semiconductor capacitor [11].**

## 2.5 Current-Voltage Characteristics:

Taking into account the mechanisms of drift and diffusion, the current can be expressed in terms of the Quasi-Fermi potential ($\phi_{Fn}$) as following:

$$I = -Wq\mu N_{inv}\frac{d\phi_{Fn}}{dx} \tag{2.30}$$

Where W is the channel width, $N_{inv}$ is the inversion charge and μ is the channel mobility. Substituting for inversion charge, we obtain [16]:

$$\mathrm{I}=\frac{-W}{L}\frac{\mu C_{stack}}{\beta^2}\left[\begin{array}{l}\left(1+\beta V+\frac{\beta t_b}{\varepsilon_0\varepsilon_{b\,g}}\right)P\left(\beta\phi_{sL}-\beta\phi_{s0}\right)-\frac{1}{2}\left[\left(\beta\phi_{sL}\right)^2-\left(\beta\phi_{s0}\right)^2\right] \\ -\frac{2}{3}a\left[\left(\beta\phi_{sL}\right)^{2/3}-\left(\beta\phi_{s0}\right)^{2/3}\right]+a\left[\left(\beta\phi_{sL}\right)^{1/2}-\left(\beta\phi_{s0}\right)^{1/2}\right]\end{array}\right] \tag{2.31}$$

Where;

$$a=\sqrt{2}\left(\frac{\varepsilon_0\varepsilon_s}{L.C_{stack}}\right) \tag{2.32}$$

The values of the surface potential, which are $\phi_{sL}$ and $\phi_{s0}$, can be determined using the boundary conditions as following [17]:

$$\phi_{Fn}(source)=\phi_F+V_{bs} \tag{2.33}$$

$$\phi_{Fn}(drain)=\phi_F+V_{bs}+V_{ds} \tag{2.34}$$

Where, $V_{bs}$ is the applied voltage, $V_s$ is the applied transistor source voltage, and $V_d$ is the applied transistor drain voltage. Simplistically, a FeFET can be viewed as a MOSFET combined with a ferroelectric capacitor as shown in Fig. 2.15.

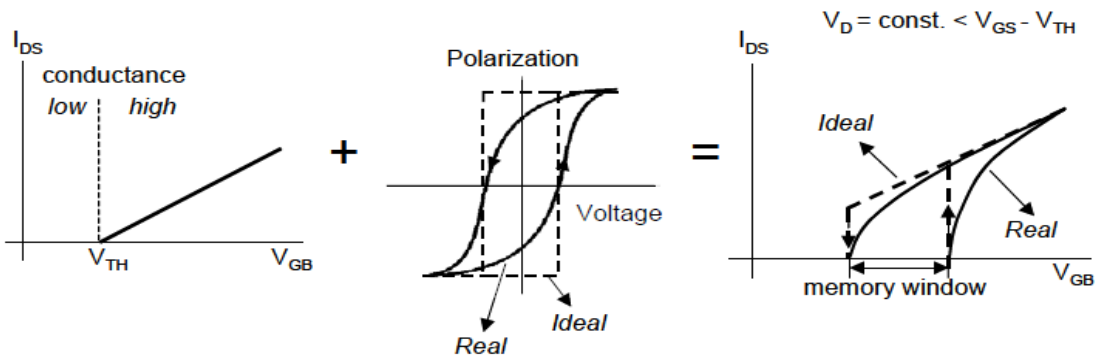



**Fig. 2.15. A MOSFET and a ferroelectric capacitor characteristics combine to give the FeFET I-V characteristics. The dashed curve represents an ideal ferroelectric [11].**

Extensive numerical analyses are performed in Silvaco Ferro model and in other models such as BISIM3 as polarization is a function of electric field in the ferroelectric region to obtain I-V characteristics. Fig. 2.16 shows an example of $I_{ds}$-$V_g$ characteristics and sub-loops of a FeFET.

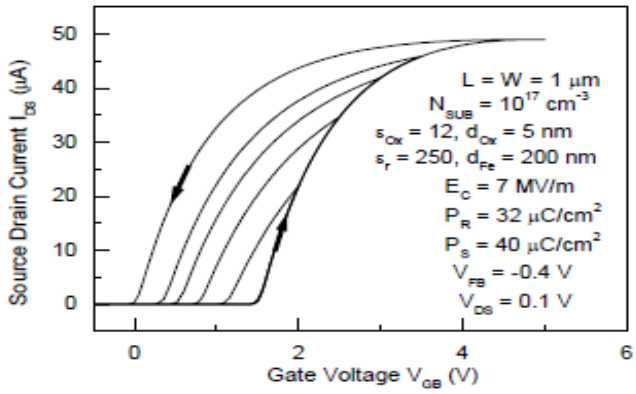



**Fig. 2.16 Simulated I-V sub-loops in the $I_{DS}$-$V_G$ characteristics for the parameters shown. [11].**

It is apparent that a FeFET has many similarities with the floating gate transistor, widely used in the Flash memory. In Flash, a high voltage is applied to the gate while grounding the drain to inject hot electrons into the floating gate. For erasing, the voltage is applied to the source while grounding the gate facilitated by the Fowler-Nordheim

tunneling. In FeFET, a gate voltage corresponding to the P+ polarization writes the state "1" while a negative voltage corresponding to the polarization state P- writes the state "0". In both cases, read process is same, applying a read voltage somewhere in the memory window where $I_{on}/I_{off}$ ratio is maximum as shown in Fig. 2.17 [11].

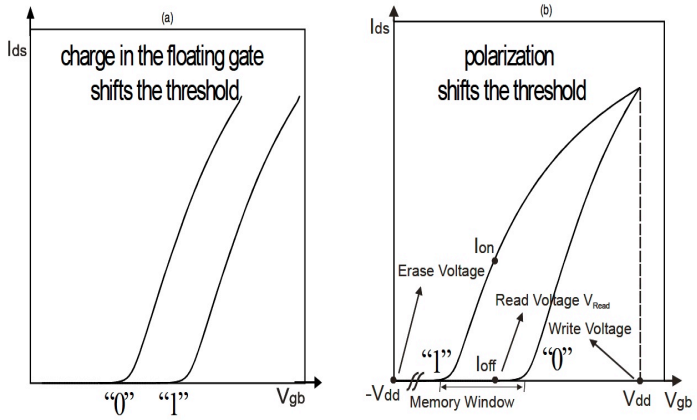



**Fig. 2.17. Reading performed by applying a read voltage somewhere in memory window: where $I_{on}/I_{off}$ ratio is high; (a) for Flash; (b) for FeFET [11].**

## 2.6 Depolarization, Charge Injection and Trapping Effects:

The depolarization electric field is an electric field that opposes the direction of polarization. This causes the polarization state in the ferroelectric film to become unstable. The depolarization field results from incomplete charge compensation at the ferroelectric/electrode interface which gives rise to a passive dielectric layer. In MFIS structure, the insulator layer and the semiconductor layer together play exactly the same role as the passive layer. The only difference is that the thickness of the layers is much thicker than the passive layer.

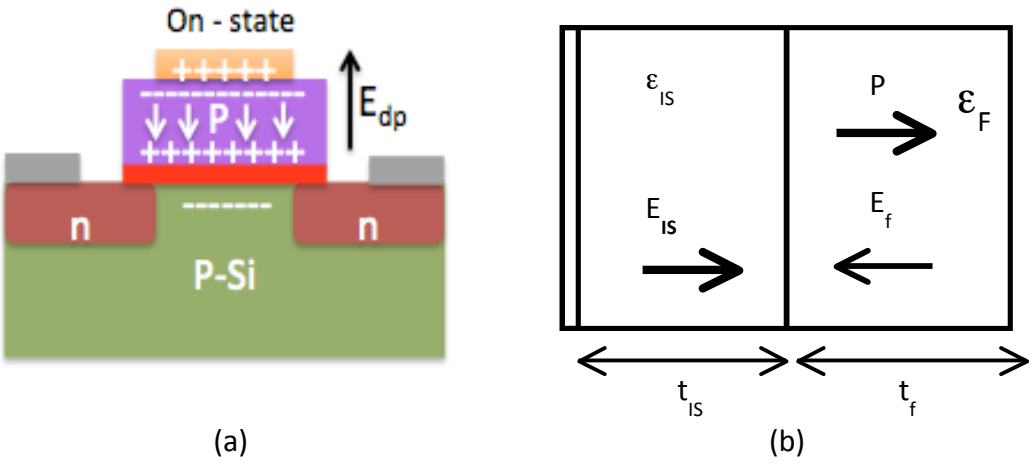



**Fig. 2.18. Model of a MFIS ferroelectric capacitor with a depolarization field.**

Referring to Fig 2.18 (b), the electric field seen by the whole structure is the sum of two components, the electric field in the ferroelectric film, $E_f$, and the electric field in the passive (buffer) layer, $E_{IS}$.

$$\left(t_{IS}+t_f\right)E = t_{IS}E_{IS}+t_fE_f \tag{2.35}$$

Where $t_{IS}$ and $t_f$ are the thicknesses of the passive layer and the ferroelectric layer respectively. When no field is applied across the structure, E=0

$$0 = t_{IS}E_{IS}+t_fE_f \tag{2.36}$$

$$E_{dp} = E_f = -\frac{t_{IS}E_{IS}}{t_f} \tag{2.37}$$

The continuity equation states that electric flux density is continuous.

$$D_{IS} = \varepsilon_{IS}E_{IS} = D_f = \varepsilon_f E_f = P \tag{2.38}$$

Where symbols D refer to the electric flux densities in each region and P is the spontaneous polarization in the ferroelectric layer.

$$E_{dp} = -\frac{t_{IS}P}{t_f \varepsilon_{IS}} \tag{2.39}$$

Referring to the schematic in Fig. 2.19, where the ferroelectric layer is represented as one capacitor with a certain spontaneous polarization, P, and an amount of charge compensated at the electrodes, $Q_F$, with total capacitance $C_f$. The insulator (buffer) and semiconductor layers are represented by a capacitor $C_{IS}$. The voltage drop across the ferroelectric layer is represented in two terms: one due to its capacitance and the voltage applied across it, $V_f$, and another due to its internal spontaneous polarization. Note that all capacitances are expressed as capacitance per unit area.

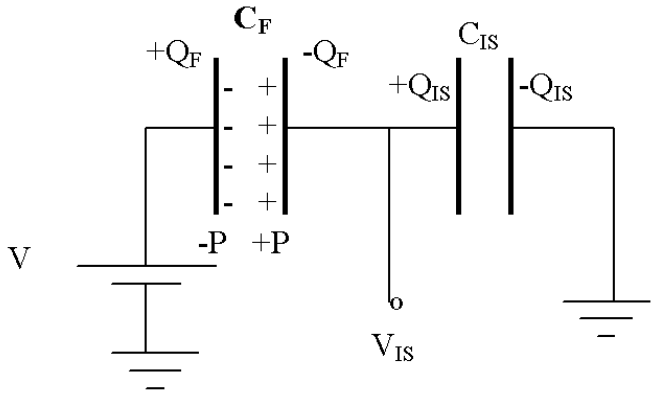



**Fig. 2.19. A schematic capacitance design of the MFIS structure [18].**

$$C_{IS}V_{IS} = P + C_f V_f \tag{2.40}$$

Where;

$$V = V_{IS} + V_f \tag{2.41}$$

By solving for $V_f$, we obtain:

$$V_f = \frac{C_{IS}V - P}{\left(C_{IS} + C_f\right)} \tag{2.42}$$

Including the magnitude of polarization P as $E_{dp}\varepsilon_f$ and substituting for capacitances as permittivity/thickness:

$$V_f = \frac{V}{1+\frac{\varepsilon_f}{\varepsilon_{IS}}\frac{t_{IS}}{t_f}} - \frac{E_{dp}}{\frac{\varepsilon_{IS}}{\varepsilon_f t_{IS}}+\frac{1}{t_f}} \tag{2.43}$$

Note that if the thickness of insulating layer, $t_{IS}$ goes to zero, $V_f$=V, and all of the applied voltage is dropped across the ferroelectric layer, and no depolarization effect happens. It can be observed that when the source and the gate are shorted, V=0, the voltage across the ferroelectric is $E_{dp}$ (proportional to polarization P) is reduced by some function of the relative permittivities of the materials in the stack.

$$V_f = -\frac{E_{dp}}{\frac{\varepsilon_{IS}}{\varepsilon_f t_{IS}}+\frac{1}{t_f}} \tag{2.44}$$

It is evident from the above equations, that a higher $\varepsilon_{IS}$ and a smaller $t_{IS}$ are desired to reduce the effect of the insulating layers on the polarization of the ferroelectric. This makes it possible to invert the channel at a lower voltage and improve on/off ratio. To minimize depolarization field, buffer layer capacitance must be as large as possible [18].

The other important issue of ferroelectric and semiconductor interfaces is the charge injection, which typically occurs from the semiconductor to the ferroelectric gate region during the switching process in FeFETs as seen in Fig. 2.20 [19]. Ferroelectric polarization attracts electron injection towards the ferroelectric/insulator interface from both the gate electrode and the semiconductor channel. Electron injection and trapping in the dielectric stack cause local charge compensation in the ferroelectric, reducing the polarization. Insulating buffer layers on both sides of the ferroelectric layer can reduce

this problem, but would increase the depolarization field and the applied field that is necessary to polarize the device.

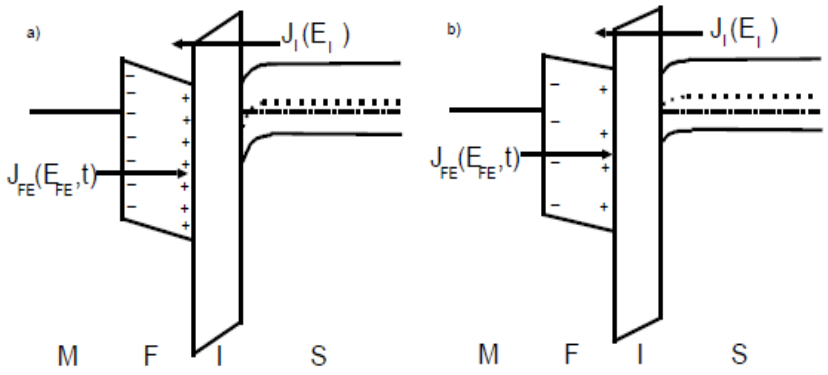



**Fig.2.20 Gate leakage effects in MFIS FeFET devices (a) Inverted semiconductor immediately after polarization, and (b) depolarization after time [18].**

Despite the high energy bandgap in insulators and a large thickness, charge transport does occur and can lead in several cases to an unwanted leakage current. The leakage current through the gate stack in the case of the FeFET can reduce the data retention time (polarization). The charge transport in insulators can be attributed to a number of mechanisms as can be seen in Fig. 2.21 extensively studied for conventional CMOS with thin gate dielectric. They are divided in the injection mechanisms, such as tunnel and thermionic injection, and the transport mechanisms, such as Poole-Frenkel, hopping, drift and diffusion. The condition for drift is the existence of enough free states in the valence or conduction band, and for diffusion, a carrier concentration gradient.

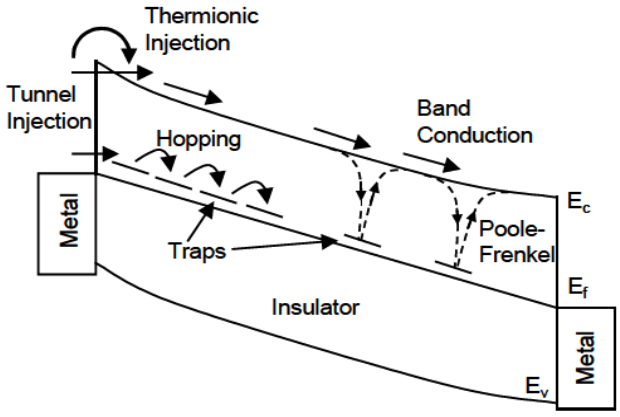



**Fig. 2.21. Various charge transport mechanisms in insulators [11].**

Based on these discussions, following observations are summarized:

- Buffer layer reduces the problem of intermixing silicon and ferroelectric
- Gate voltage is divided according to capacitance ratio of the buffer layer and the ferroelectric layer
- To minimize depolarization field, buffer layer capacitance must be as large as possible
- Too thick ferroelectric makes the operation voltage too high
- The effect of charge injection can be minimized by employing an engineered buffer sandwiched between the silicon and the ferroelectric layer
- Leakage current between ferroelectric and buffer, removes the charges, hence the stored data cannot be readout

It is inferred that optimization of buffer layer is extremely important.

## 2.7 Evolution of FeFETs on Conventional Perovskites:

Ferroelectric FETs have been proposed in 1957 as an alternative to FeRAMs, which suffer from data loss. FeFETs have been being studied for more than fifty years. PZT and SBT ferroelectric materials have been studied for a long time. Roy, Dhar and Ray (2007) studied the performance of SBT based FeFET devices. In their study, they fabricated a FeFET with 280 nm SBT ferroelectric layer. The general structure of their device was Al/SBT/$HfO_2$/Si. In their study, they found that a large memory window could be accomplished by using 12 nm of $HfO_2$ buffer layer as seen in Fig. 2.22 [20].

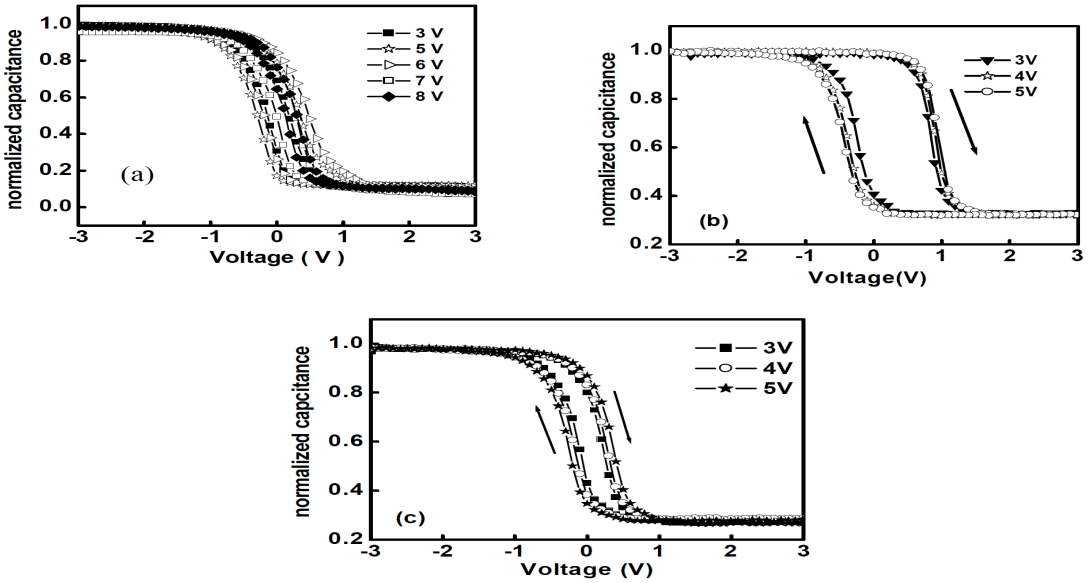



**Fig. 2.22. C-V characteristics of Al/SBT (280 nm)/$HfO_2$/Si (a) with 3 nm $HfO_2$ buffer layer (b) with 12 nm buffer layer, and (c) with 18 nm buffer layer [20].**

Phan Trong Tue et al. (2010) fabricated a PZT-based FeFET with indium tin oxide (ITO)/PZT/ $SrRuO_3$(SRO)/Pt stacked structure. The gate length of fabricated device was 60 μm and the gate width was 20 μm. Fig. 2.23 shows the hysteresis loop of this device [19].

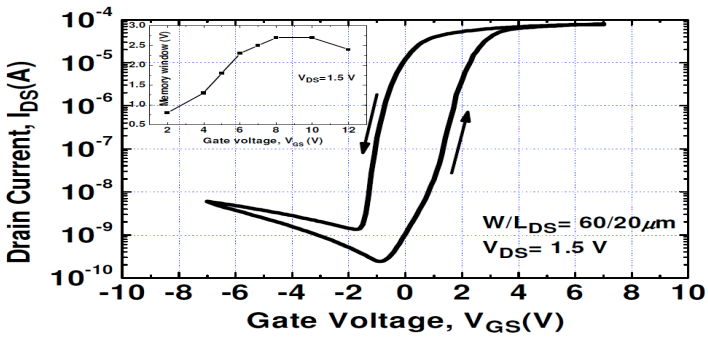



**Fig. 2.23. I-V characteristics of the PZT-based FeFET using ITO/PZT/SRO/Pt structure [18].**

Chai et al. (1995) studied the relation of the ferroelectric thickness and the niobium doping levels in capacitor memories. They found that reducing the ferroelectric thickness (in 0.3 µm range) by a factor of 2 should be compensated by increasing the doping up to 5% to reduce the effect of leakage in capacitor memories. Their study focused only on capacitor memories [16]. Therefore, it is significant to understand the scaling effect of ferroelectric gates in field effect Transistors. Fig. 2.24 shows the effect of doping on the hysteresis loops of capacitor memories [17].

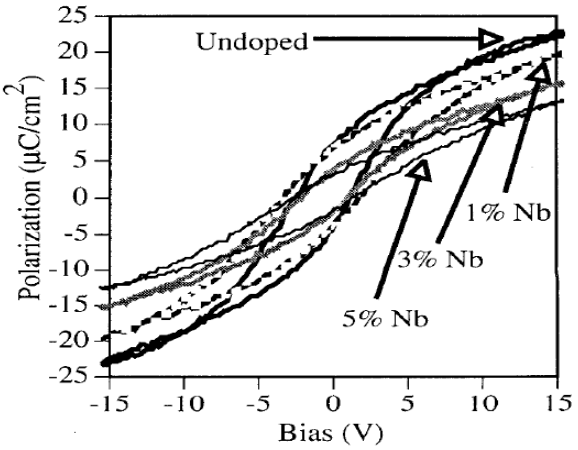



**Fig. 2.24: Measured hysteresis loops of ferroelectric films with different niobium doping levels [17].**

Using an insulator layer forms two serial capacitors (voltage divider) as seen in Fig. 2.25. The effect of this voltage divider can be reduced by using high-k dielectric materials in the insulator [21].

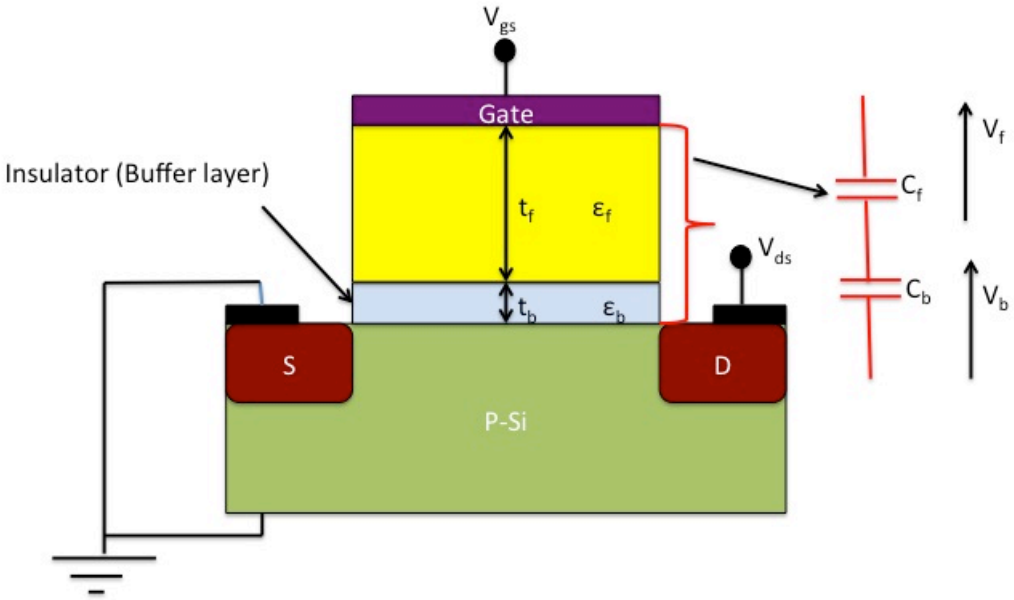



**Fig.2.25. Effect of voltage divider due to using a buffer layer.**

Kim et al. (1998) investigated the effect of the insulator layer on the I-V characteristics of FeFETs. They studied three different insulating materials, which are cerium oxide ($CeO_2$), yttrium oxide ($Y_2O_3$) and silicon dioxide ($SiO_2$). Their study focused on FeFETs with Strontium Bismuth Tantalate $SrBi_2Ta_2O_9$ (SBT) ferroelectric material. Their results showed that using $CeO_2$ and $Y_2O_3$ insulation materials effectively reduced the charge injection between semiconductor and SBT interface and reduced the effect of voltage divider effect [22]. There are other common high-K dielectric materials that can be investigated such as hafnium oxide ($HfO_2$) and strontium tantalate ($SrTa_2O_6$). Fig. 2.26 (a) and (b) shows the $I_d$-$V_d$ curves of the FeFET with yttrium oxide ($Y_2O_3$) and silicon dioxide ($SiO_2$) layers, respectively.

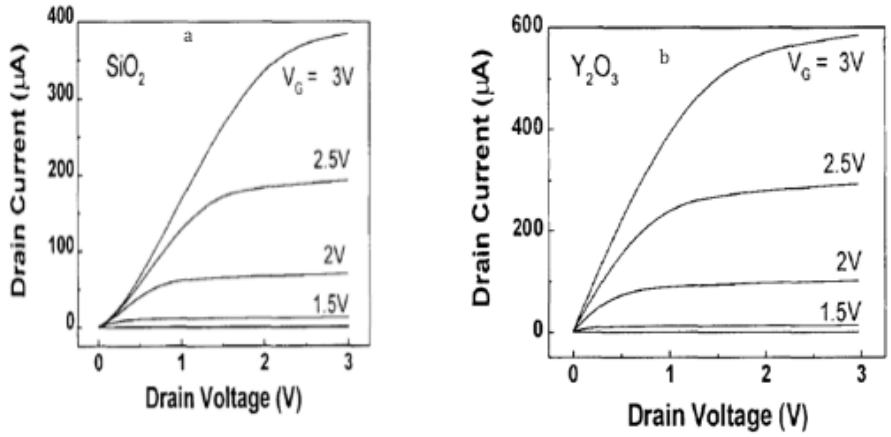



**Fig. 2.26. $I_d$-$V_d$ characteristics of the FeFET with (a) $SiO_2$ (b) $Y_2O_3$ dielectric layers [22].**

Roy, Dhar and Ray (2007) studied the effect of using hafnium oxide ($HfO_2$) as a buffer layer for FeFETs. Their study depended on FeFETs with 280nm thick SBT ferroelectric material and aluminum gate metal. Final results showed that FeFETs with $HfO_2$ buffer layers had larger memory windows than devices with no buffer layer as seen in Fig. 2.27. They found also that the current leakage decreased with increasing the $HfO_2$ buffer layer thickness [20].

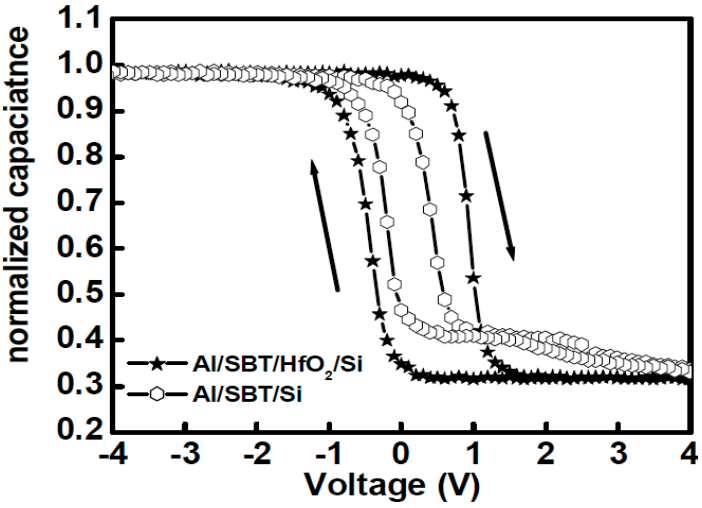



**Fig. 2.27. C-V characteristics of FeFET with $HfO_2$ and $SiO_2$ dielectrics [20].**

## 2.8 Limitations of PZT and SBT for FeFET Applications:

Commonly used perovskite ferroelectrics such as PZT and SBT are high dielectric constant (high-k) materials ($\varepsilon_r$~250) in thin films. A high-k material, although favored as a gate dielectric, is not a desirable property for the ferroelectric in the FeFET, because of the low-k dielectric buffer layer that is always present in the FeFET gate stack. The dielectric's lower permittivity (lower capacitance) results in a higher voltage drop across the buffer layer compared to that across the ferroelectric. PZT and SBT also suffer from an increase in coercive fields as thickness is scaled down [23]. These materials possess only limited compatibility with standard semiconductor processing. Integration into transistor devices is only possible with interfacial barriers and FE layers thicker than 100 nm need to be used in order to achieve non-volatility. Hence, no easy scaling of the devices according to current technology node requirements can be realized. Thicker films also lead to more fringing effects which cause degradation of sub-threshold characteristics. Fig. 2.28 shows the main concept of fringing [24].

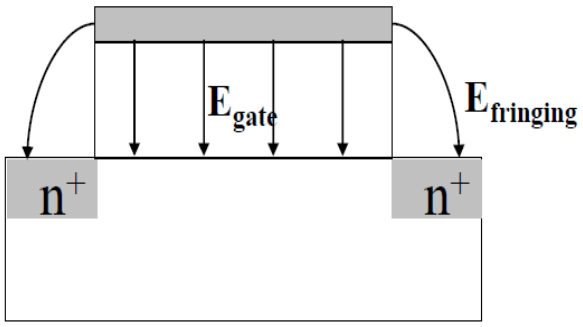



**Fig. 2.28 Fringing effects due to thicker gate dielectric [24].**

## 2.9 Ferroelectricity in Silicon Doped Hafnium Oxide (Si:$HfO_2$):

FeFETs have been being studied for more than fifty years but the ideal device remains elusive. This is because many issues in gate stack and interface states densities. Discovery of ferroelectricity in doped hafnium oxide ($HfO_2$) has opened doors for realizing high performance FeFETs.

Boscke, Muller et al. (September 2011) studied ferroelectricity in thin films of silicon doped hafnium oxide (Si:$HfO_2$). These films were 10nm thick with less than 4 mol. % of $SiO_2$. They observed that the large band offset between Si and $HfO_2$ allows for minimal current leakage and it is otherwise thermodynamically compatible with silicon technology, allowing for contact without the need for a thick buffer layer [25].

Sun and Zheng (October 2011) studied the effect of the buffer layer thickness on MFIS-FeFETs. Their study focused on $SiO_2$ dielectric layers. They studied a FeFET device with 5µm channel length and 5nm thick $SiO_2$. Their results showed that the I-V characteristics of the FeFET became worse as the $SiO_2$ thickness increased because of the retention loss [26].

Tingting Feng et al. (2011) studied a MFIS-FeFET with 2µm channel length, 400 nm thick ferroelectric and 5nm thick $HfO_2$ dielectric. Their study focused on using Nd-doped Bismuth Titanate $B_{3.15}Nd_{0.85}Ti_3O_{12}$ (BNdT) ferroelectric material, which has a large remnant polarization ($P_r$). They used Silvaco software to study all the performance parameters such as gate voltage and buffer layer thickness. Their final results showed that there was insignificant charge injection between Si and ferroelectric material because of the use a thin layer of $HfO_2$ as a buffer layer. The BNdT ferroelectric layer showed a wide memory window as seen in Fig. 2.29 [27].

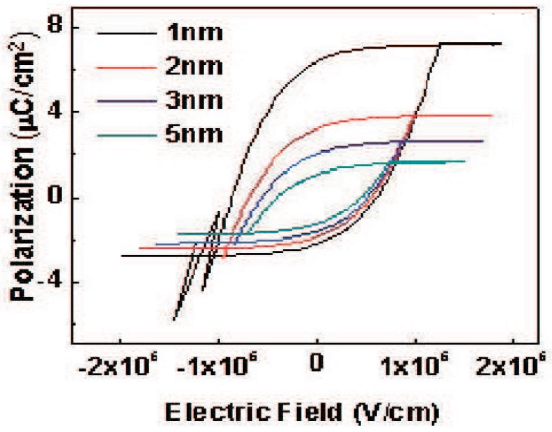



**Fig. 2.29. Polarization hysteresis loop of the simulated FeFET [27].**

Ekaterina Yurchuk et al. (2012) fabricated a sub-0.3 μm (260nm) FeFET with 9nm thick Si:$HfO_2$. The general stack form of their device was poly-Si/TiN/Si:$HfO_2$ /$SiO_2$ /Si. Their results showed that the FeFET performance could be improved by doping the 9nm thick $HfO_2$ films with 4.4 mol. % $SiO_2$ as shown in Fig. 2.30 [28].

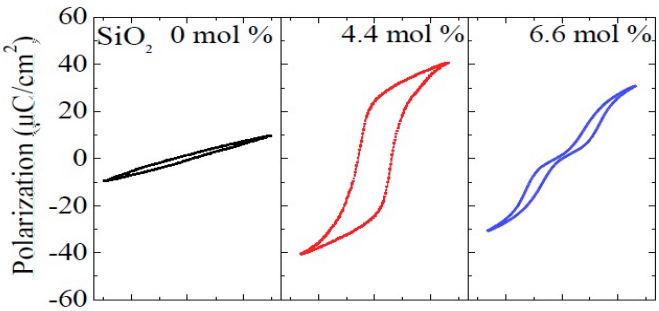



**Fig. 2.30. Improved polarization by doping $HfO_2$ with 4.4 mol. % $SiO_2$ [28].**

Stefan Mueller et al. (2013) studied the performance of Si:$HfO_2$ FeFETs based on a 28nm bulk technology. Their study used Sentaurus TCAD simulations where material parameters such as coercive field, remnant polarization, saturation polarization, and permittivity were determined experimentally and then input into the simulation. The

accuracy of their model was verified on Metal-Ferroelectric-Metal (MFM) structures. Their study focused on two different ferroelectric material thicknesses, which are 10nm and 30nm [29]. The results of hysteresis loops of these structures are shown in Fig. 2.31.

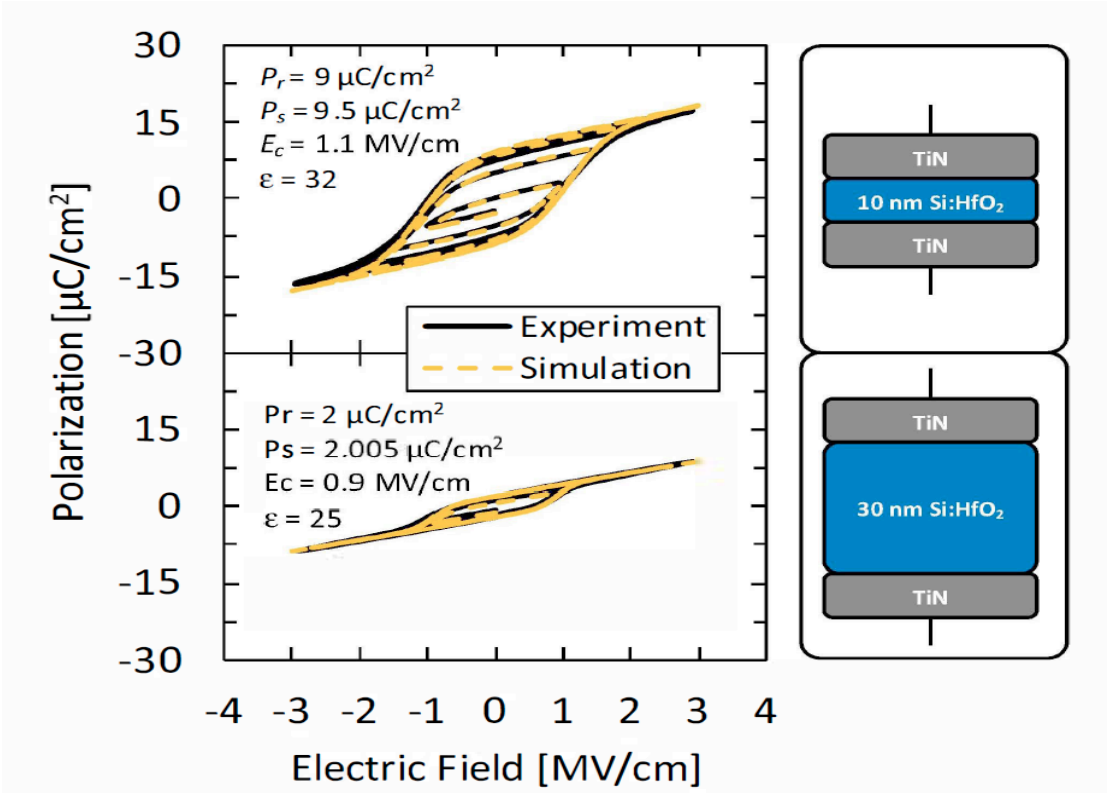



**Fig. 2.31. The experimental verification of TCAD simulations [29]**

The 10 nm thick ferroelectric layer has larger remnant polarization compared to the 30 nm thick layer. The remnant polarization values are 9µC/cm$^2$ and 2µC/cm$^2$ for 10nm and 30 nm thick ferroelectric layers, respectively [29]. Since 10nm ferroelectric layer has a larger remnant polarization, it showed much more pronounced depolarization compared to the 30nm layer as seen in Fig. 2.32. Their experimental results and their simulations showed the remnant polarization ($P_r$) of Si:$HfO_2$ increased by decreasing the layer thickness. The thinner device was able to operate at lower voltages (5 V as compared to 6 -7 V for the thicker device).

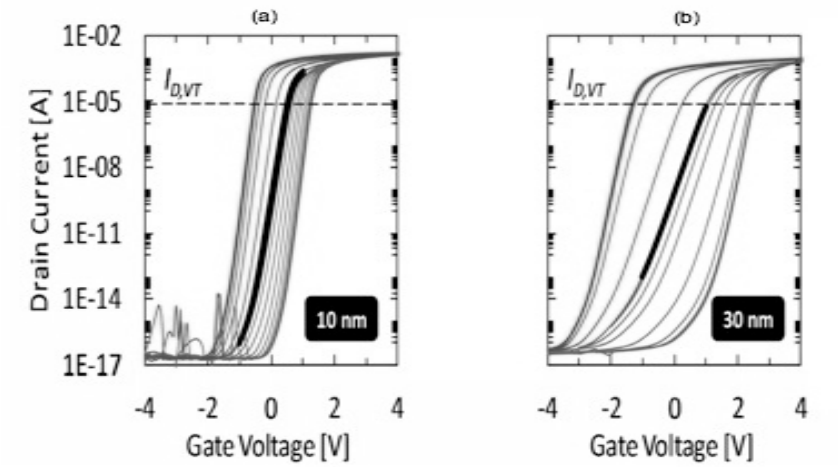



**Fig. 2.32. The $I_d$ - $V_g$ curves of the simulated FeFET device (a) with 10 nm thick ferroelectric layer (b) with 30 nm thick ferroelectric layer [29].**

David J. Frank et al (2014) studied the quantum metal FeFET (QMFeFET). They introduced a mathematical module to achieve steep sub-threshold slope FeFET by using a very thin metal or a quantum metal. Their model showed that a QMFeFET with very steep sub-threshold, which was about 2mV/decade over 11 decades, could be accomplished. In their study, two approaches have been introduced as seen in Fig. 2.33 (a) and (b). These approaches include a QMFeFET with and without a thin buffer layer between the semiconductor and the quantum metal [30].

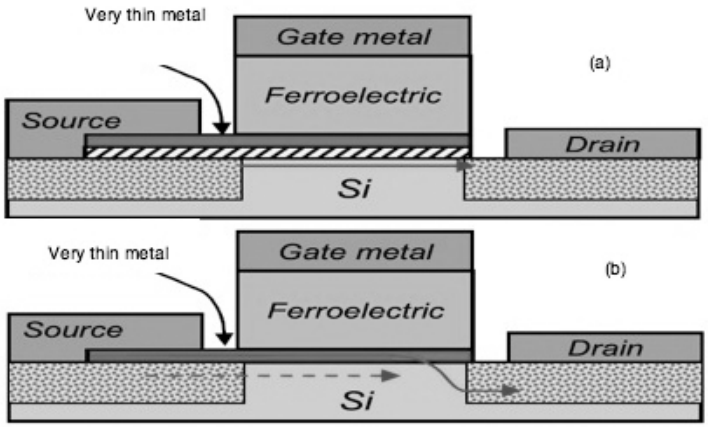



**Fig. 2.33. Structure of the QMFeFET (a) with buffer layer (b) without buffer layer [30].**

The International Technology Roadmap for Semiconductors (ITRS) 2013 emerging research devices edition indicates that there is a need for more work to be done to improve FeFETs performance parameters such as retention time and integrating the technology into actual CMOS based devices [31].

The last three years show that extraordinary improvements have been accomplished in FeFET devices. It has been shown that FeFET devices can be fabricated down to the 28nm node in modern factory lines. This indicates that optimization of shorter channel devices is certainly warranted. However, much research, developments, and optimizations are still needed since FeFET devices are very variable prospect in the non-volatile memory market.

## 2.10 Research Objectives:

After conducting the literature study presented above, the following research objectives were proposed and carried out in this study;

1. Perform simulations of 26 nm FeFETs utilizing the data for Si:$HfO_2$ reported in the literature using SILVACO ATLAS software. Obtain drain current versus gate voltage characteristics by using the device parameters such as channel doping, source drain doping and junction depth, and gate electrode in simulations according to state of the art 26 nm NMOS.
2. Investigate the effects of ferroelectric thickness, buffer layer thickness and buffer layer permittivity on the memory window of FeFET. Investigate non-ferroelectric pure hafnium oxide as a buffer layer and compared with $SiO_2$ and $Si_3N_4$ as buffer layer materials.

# CHAPTER 3 – SILVACO ATLAS SIMULATIONS METHODOLOGY

This chapter focuses on Silvaco Atlas software. It gives an introduction to Silvaco software. Then, it follows an explanation of Silvaco atlas parameters. The ferroelectric used model is discussed in this chapter.

## 3.1 Silvaco:

Silvaco is a TCAD software package that can be used to achieve device and process simulations. Fig. 3.1 shows the main modules of the Silvaco software [32].

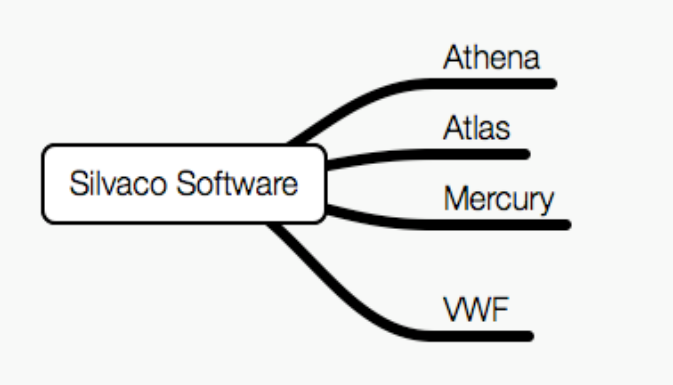



**Fig. 3.1. Silvaco main modules.**

- Athena: It is considered as a process software module. It is basically used to treat serial steps of devices fabrication. The most common processes that can be treated include deposition, diffusion, ion implantation, etching, lithography, silicidation of semiconductor materials and oxidation. Athena provides a good alternative for practical experiments that usually cost a lot of money.
- Atlas: It is a good tool to study behavior of semiconductor devices such as electrical, optical and thermal behavior. It provides accurate simulations in 2D and 3D to study

and analyze AC, DC and time domain responses for all semiconductor based technologies.

- Mercury: It is a group of device simulations that include MESFET and HEMT devices. It contains FastBlaze, Mocasim, FastNoise and FastDevEdit device simulation products. FastBlaze simulator is used to generate accurate and proper electrical characteristics of MESFET and HEMT devices by using physics based calculations. Mocasim is mainly used to achieve accurate calculations of wurtzite and zincblende semiconductors fundamental electron transport properties.
- Virtual Wafer Fab (VWF): It is used to emulate and automate physical wafer manufacturing processes. VWF tools are effective in facilitating the input, run-time optimization, execution and results into a flow managed through a database.

Physically based simulations, which are different from empirical modeling, are typically used in Silvaco. The simulated devices are represented onto a two dimensional grid, which consists of a number of nodes. To simulate the transport of carriers, a set of fundamental semiconductor differential equations are solved on this two dimensional grid. These differential equations are solved by integrating relevant physics. The most common equation can be classified to transport equations, continuity equations and Poisson's equation [32].

Poisson's equation shows the relation between electrostatics potential, electric field and electrostatic charges, which include mobile and fixed charges. This equation can be expressed as following:

$$\Delta^2\Phi = -\Delta E = \frac{\rho}{\varepsilon} \tag{3.1}$$

$$\Delta^2\Phi = -\frac{q}{\varepsilon}\left(p - n + N_d^+ - N_a^-\right) \tag{3.2}$$

Where Φ represents the electric potential, E represents the electric field, ρ represents the charge density, and ε is the semiconductor permittivity. In equation 3.2, q represents the electron charge, which is about $-1.602\times10^{-19}$ C, p and n represent the densities of free holes and electrons respectively, and $N_d^+$ and $N_a^-$ are the charge densities of ionized donors and acceptors, respectively.

The drift-diffusion model can be used to express the transport equation as following:

$$J_p(x) = q\mu_p p(x)E(x) + qD_p \frac{dp(x)}{dx} \tag{3.3}$$

$$J_n(x) = q\mu_n n(x)E(x) - qD_n \frac{dn(x)}{dx} \tag{3.4}$$

These equations are a combination of drift current and diffusion current components. In equation 3.3, $\mu_p$ is the hole mobility and $D_p$ is the hole diffusivity. In equation 3.4, $\mu_n$ is the electron mobility and $D_n$ represents the electron diffusivity. Einstein relation expresses the relation between diffusion coefficient and mobility as following:

$$\frac{kT}{q} = \frac{D}{\mu} \tag{3.5}$$

Where D is the diffusion coefficient and μ is the mobility. The following equations express the carrier continuity for holes and electrons.

$$\frac{\partial p}{\partial t} = G_p - R_p - \frac{1}{q}\Delta.J_p \tag{3.6}$$

$$\frac{\partial n}{\partial t} = G_n - R_n - \frac{1}{q}\Delta.J_n \tag{3.7}$$

Where, $G_p$ and $G_n$ represent the generation rates of excess holes and electrons, respectively, $J_p$ and $J_n$ are the current densities of holes and electrons and $R_p$ and $R_n$ represent the recombination rates of holes and electrons [32]. The permittivity model is explained in section 3.3.

## 3.2 Silvaco Atlas:

In Silvaco Atlas, it is significant to specify physical structure, physical model and bias conditions of the simulated device. Fig. 3.2 shows the inputs and outputs of Silvaco atlas.

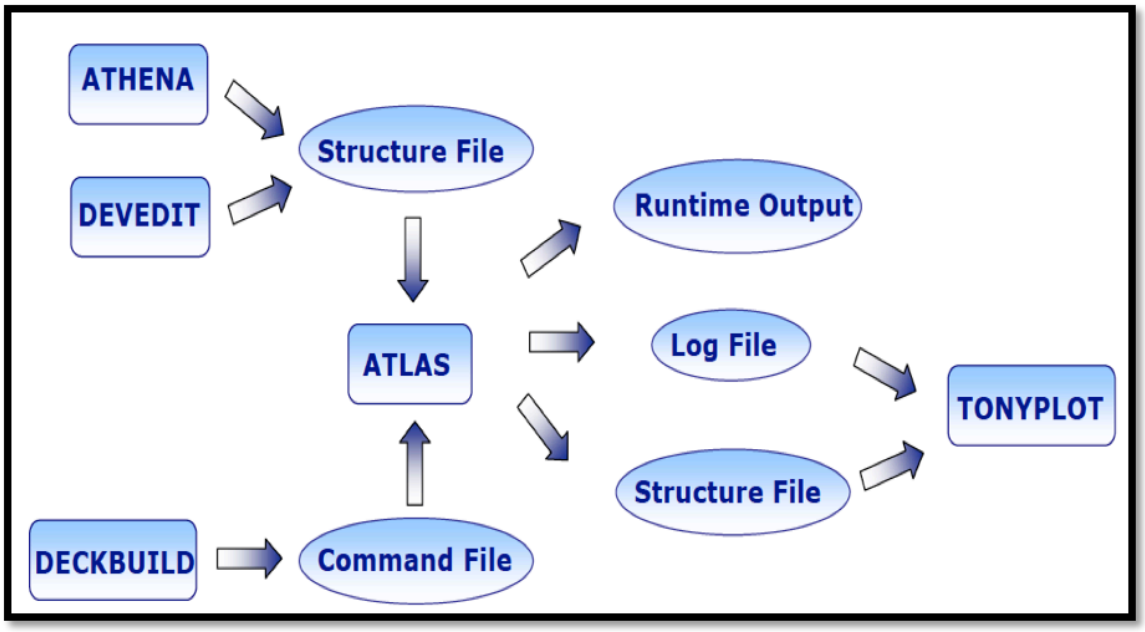



**Fig. 3.2. Inputs and outputs of Silvaco Atlas [33].**

Atlas typically uses two types of input file. First type is the structure file that is used to define the structure of the simulated device. Second type is the text file, which includes all the atlas commands. The key function of the structure file is to store the 2D and 3D data that are related to the values of solution variables [32]. The general syntax of an input statement is Atlas is:

<statement><parameter>=<value>

The parameter value in Atlas can be logical, character, real or integer. Statements are generally classified to five groups. These groups include structure specification, material model specification, numerical method selection, solution specification and results

analysis. Table 3.1 shows Atlas input specifications.

**Table 3.1: Input specifications of Silvaco Atlas [32]**

| Group | Statement |
|---|---|
| Structure Specification | mesh |
| | region |
| | electrode |
| | doping |
| Material Models Specification | material |
| | models |
| | contact |
| | interface |
| Numerical Method Selection | method |
| Solution Specification | log |
| | solve |
| | load |
| | save |
| Results Analysis | extract |
| | tonyplot |

Output files of Atlas can be classified to three types, which are run-time output, log file output and structure file output. Run-time output files basically give the messages of warnings, progress and errors of simulations. Log file outputs (.log) are used to store the terminal characteristics that are calculated by Silvaco Atlas. In DC simulations, these

calculations include current and voltages at electrodes of the simulated device. In transient simulations, log files are used to store time. In AC simulations, this type of output files is used to save the conductance, the small signal frequency and capacitance. Structure files (.str) are used to provide an image of the simulated device at a certain bias point. Doping profiles, band parameters, electric fields and electron concentrations can be effectively displayed using structure file outputs.

## 3.3 The Ferroelectric Permittivity Model in Atlas:

To simulate polarization and hysteresis effects of ferroelectric materials, the ferroelectric model in Atlas should be used in the simulation code. This model can be enabled by setting the "FERRO" parameter in the "MODELS" statement. The permittivity, which is used in Poisson's equation, is expressed as derived in equation 2.27 as following [32]:

$$\varepsilon(E) = ferro.\ epsf + \frac{ferro.ps}{2\delta} \bullet \sec h^2 \left[ \frac{E - ferro.ec}{2\delta} \right] \qquad (3.8)$$

Where, E is the electric field, *ferro.epsf* is the permittivity. δ can be mathematically expressed as following:

$$\delta = ferro.ec \left[ \log \left( \frac{1 + \frac{ferro.pr}{ferro.ps}}{1 - \frac{ferro.pr}{ferro.ps}} \right) \right]^{-1} \qquad (3.9)$$

The ferroelectric parameters, which are *ferro.pr, ferro.ps, ferro.epsf* and *ferro.ec,* can be specified in the "MATERIAL" statement. Each material has different parameters

depending on its characteristics. Table 3.2 shows the default values of the ferroelectric parameters [32].

**Table 3.2: Default values and units of ferroelectric parameters [32]**

| Statement | Parameter | Default Value | Unit |
|---|---|---|---|
| MATERIAL | *Ferro.ec* | 0.0 | V/cm |
| MATERIAL | *Ferro.epsf* | 1.0 | |
| MATERIAL | *Ferro.ps* | 0.0 | C/sqcm |
| MATERIAL | *Ferro.pr* | 0.0 | C/sqcm |

The permittivity in equation 3.8 can be redefined by using the C-Interpreter. To define the file that contains the C-function, the "*f.ferro*" parameters should be included in the "MATERIAL" statement. The key function of this step is to allow the permittivity to be position. The dipole polarization can be expressed with respect to the electric field as following:

$$\frac{dP_d}{dE} = \Gamma \frac{dP_{sat}}{dE} \tag{3.10}$$

Where $P_d$ represents the position dependent dipole polarization and $P_{sat}$ is the saturated loop polarization. Γ is a unity function, and it corresponds to the default model. The Γ function can be modified to be more general by specifying the "*unsat.ferro*" parameter in the "MODELS" statement. Γ can be expressed in this case as following:

$$\Gamma = 1 - \tanh\left[\left(\frac{P_d - P_{sat}}{\xi P_s - P_d}\right)^{1/2}\right] \tag{3.11}$$

Where ξ signal depends on the direction of electric field. It equals to "+1" for increasing electric field and "-1" for decreasing electric fields.

## 3.4 Methodology Specifications:

To simulate and study the performance of a short channel FeFET, it is important to proceed through the following steps in the proper order.

- Defining the device structure: Device structure is typically defined by the mesh of each region and specifying these regions according to the desired device structure. For example:

  *region num=1 silicon y.min=0.0*
  *region num=2 material=HfO2 y.max=0.0 y.min=-0.00005*
  *region num=3 oxide y.max=-0.00005 y.min=-0.010*
  *region num=4 oxide y.max=-0.010 y.min=-0.0101*

- Defining electrodes for source, drain and gate contacts: Electrodes are typically defined by locating the desired electrode with its dimensions. For example:

  *electrode num=1 material=NiSi name=source y.max=0.0 x.max=0.002*
  *electrode num=2 material=NiSi name=drain y.max=0.0 x.min=0.026409*
  *electrode num=3 material=TiN name=gate top x.min=0.002841 x.max=0.025568*
  *electrode num=4 name=substrate bottom*

- Defining doping values for source, drain and substrate: Doping can be obtained by specifying the doping type and its value. For example:

  *doping uniform conc=3e16 p.type*
  *doping gaus conc=1e19 n.type x.right=0.004066 char=0.0008*
  *doping gaus conc=1e19 n.type x.left=0.024343 char=0.0008*

- Defining the ferroelectric material: Ferroelectric materials are defined by using the order "*ferro*". In addition, the permittivity characteristics, i.e. remnant polarization, spontaneous polarization, critical electric field and zero field relative

permittivity, should be defined for each ferroelectric layer. The following numbers are measured by Stefan Mueller et al. (2013) [29]. For example:

*model region=3 ferro*
*material region=3 ferro.ec=1.1e6 ferro.pr=9.0e-6 ferro.ps=9.5e-6 ferro.epsf=32*

- Obtaining I-V characteristics: To obtain I-V curves, it is significant to use an accurate method. For example:

  *method gummel newton itlim=25 trap maxtrap=12 vsatmod.inc=0.01 carriers=2 output con.band val.band band.param e.mobility h.mobility*

  This method consists of several parts. These parts include:

  - ✓ method gummel newton: To obtain an improved initial guess for the newton solution scheme.
  - ✓ itlim : Controlling the maximum number of iterations.
  - ✓ Maxtrap: Specifying the number of times the trap procedure will be repeated.
  - ✓ Vsatmod.inc: Specifying that the derivatives of the negative differential mobility will not be for potential that is less than the value specified by vsatmod.

  The I-V curve can be obtained by drawing the forward and reverse sweep of the FeFET. Then, the threshold voltage ($V_T$) shift can be effectively obtained. For example:

  *solve*
  *solve vd=0.1*
  *##########################################*
  *# forward sweep*
  *##########################################*
  *log outf=ferro1_2.log master*
  *solve vgate=-3.0 vstep=0.05 vfinal=3.0 name=gate*

```
##########################################
# reverse sweep
##########################################
material ferro.ec=-100000
solve vstep=-0.05 vfinal=-3.0 name=gate
```

# CHAPTER 4 – RESULTS AND ANALYSIS

This chapter focuses on the results of the simulated devices. Four different devices have been simulated to study the effect of ferroelectric thickness on the performance of the FeFET. The purpose of these simulations is to suggest that it is possible to get short channel FeFETs with high performance by using Si:$HfO_2$ as a ferroelectric material.

## 4.1 Device Parameters (n-FeFET Parameters):

This device was designed with 26 nm gate metal length. Table 4.1 shows the parameters of the simulated device.

**Table 4.1: Parameters of the simulated device**

| Parameter | Value |
|---|---|
| P-well Doping ($cm^{-3}$) | $1\times10^{17}$ |
| S/D Doping ($cm^{-3}$) | $1\times10^{19}$ |
| Junction depth (nm) | 10 |
| Gate Metal Length (nm) | 26 |
| $HfO_2$ Buffer Layer Thickness (Å) | 8 |
| Gate Electrode | TiN |
| S/D Electrodes | NiSi |
| Ferroelectric Layer | Si:$HfO_2$ |

Since punchthrough typically occurs at lower voltages in the device with deeper source-drain junction depths, the S/D depths were designed to be too shallow (10nm). Titanium nitride (TiN) was used as a gate electrode to reduce gate depletion effect. Nickel silicide

(NiSi) was used to reduce S/D series resistance in order to avoid the decreasing in the drive current ($I_{drive}$). Silicon doped hafnium oxide (Si:$HfO_2$) was used as a ferroelectric material. Si:$HfO_2$ material was studied by Stefan Mueller et al. (2013), and they found that the remnant polarization of this material considerably increased with decreasing thickness. This means that it is possible to achieve short channel FeFETs that are able to operate at lower voltages. In this work, four different ferroelectric thicknesses were used. Table 4.2 shows these thicknesses with the permittivity characteristics of each thickness and the theoretical maximum memory window ($MW_{max}$) that can be accomplished at each thickness. Permittivity characteristics of Si:$HfO_2$ material have been measured by Stefan Mueller et al for 10 nm and 30 nm thicknesses. A calculator was developed to estimate these characteristics for any thickness as seen in Appendix A.

**Table 4.2: Permittivity characteristics of the Si:$HfO_2$ ferroelectric material for different thicknesses and the calculated maximum memory window values**

| **Ferroelectric Thickness** | $P_r$ ($\mu C/cm^2$) | $P_s$ ($\mu C/cm^2$) | $E_c$ (MV/cm) | $\varepsilon_f$ | $t_b$ (nm) | $\varepsilon_b$ | $MW_{max}=2E_ct_f$ |
|---|---|---|---|---|---|---|---|
| **15 nm** | 7.25 | 7.63 | 1.05 | 30.25 | 0.8 | 25 | 3.15 V |
| **12 nm** | 8.3 | 8.75 | 1.08 | 31.3 | 0.8 | 25 | 2.59 V |
| **10 nm** | 9 | 9.5 | 1.1 | 32 | 0.8 | 25 | 2.2 V |
| **8 nm** | 9.7 | 10.25 | 1.12 | 32.7 | 0.8 | 25 | 1.9 V |

Fig. 4.1 shows the main structure of the simulated Si:$HfO_2$ FeFET device.

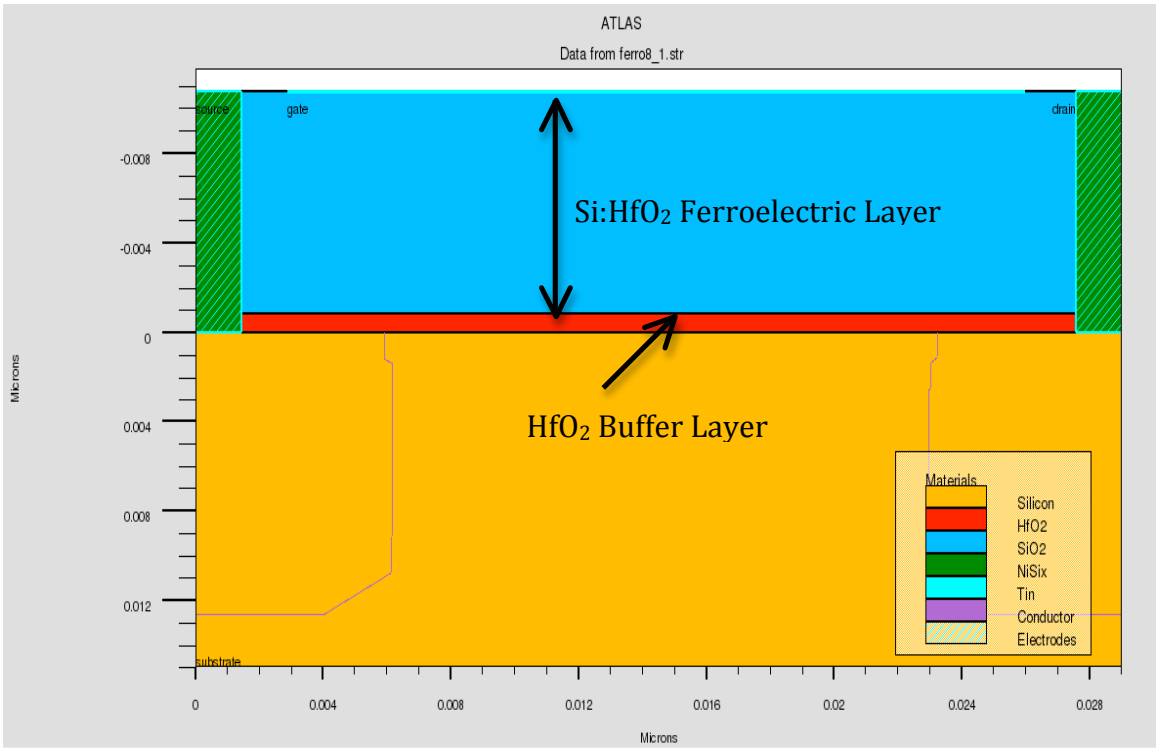



**Fig. 4.1. Main structure of the simulated FeFET (dimensions in µm).**

## 4.2 Effect of the Ferroelectric Layer Thickness:

The key features of these simulations is using silicon doped hafnium oxide (Si:$HfO_2$) as a ferroelectric layer. Four transistor geometrics were created, the first one has 15 nm, the second one has 12 nm, the third one has 10 nm, and the last one has 8 nm of Si:$HfO_2$ as a ferroelectric layer. All these devices have 8 Å of $HfO_2$ as a buffer layer. The main purpose of simulating devices with different ferroelectric thicknesses was to study the effect of the ferroelectric thickness on the performance of the FeFET. The gate voltage was swept from -7 V to +7 V for all FeFET devices. Then, the sweep amplitude was decreased to 0 V while keeping the drain voltage at 0.1 V. Fig. 4.2 and 4.3 show the simulated devices and the I-V hysteresis loops, respectively.

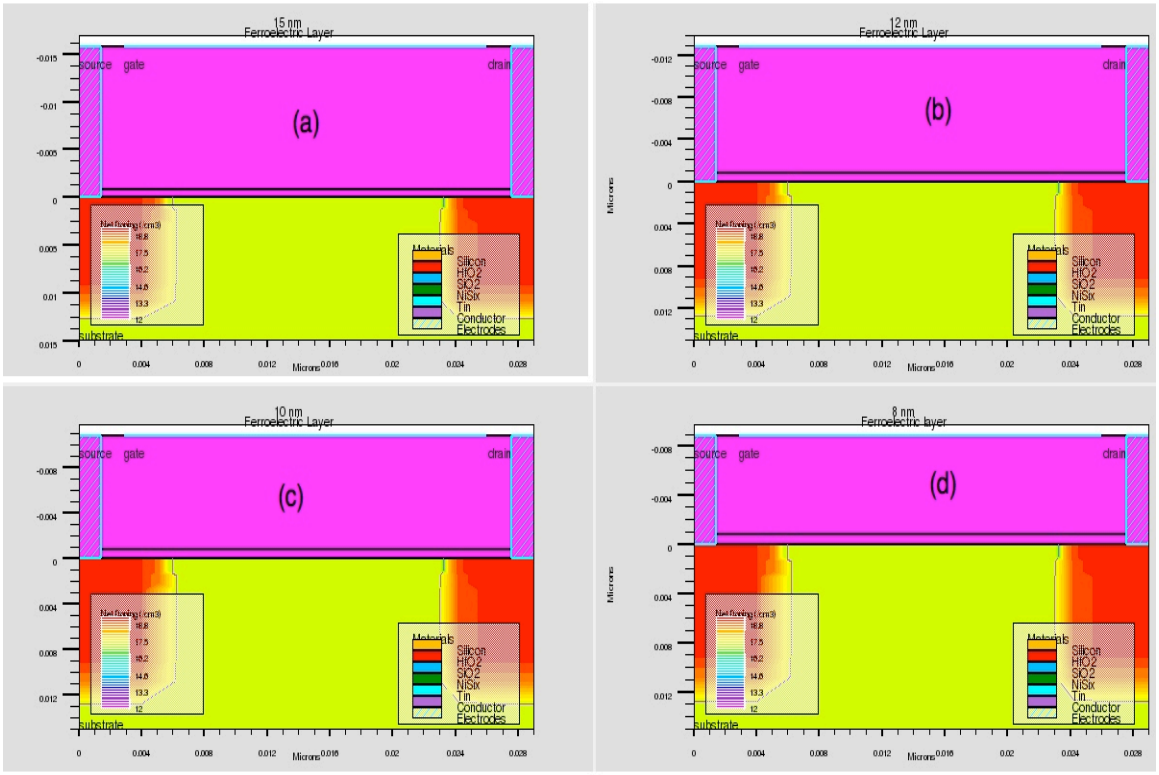



**Fig. 4.2. Simulated FeFET device (a) with 15 nm (b) with 12 nm (c) with 10 nm, and (d) with 8 nm thick ferroelectric layer (dimensions in µm).**

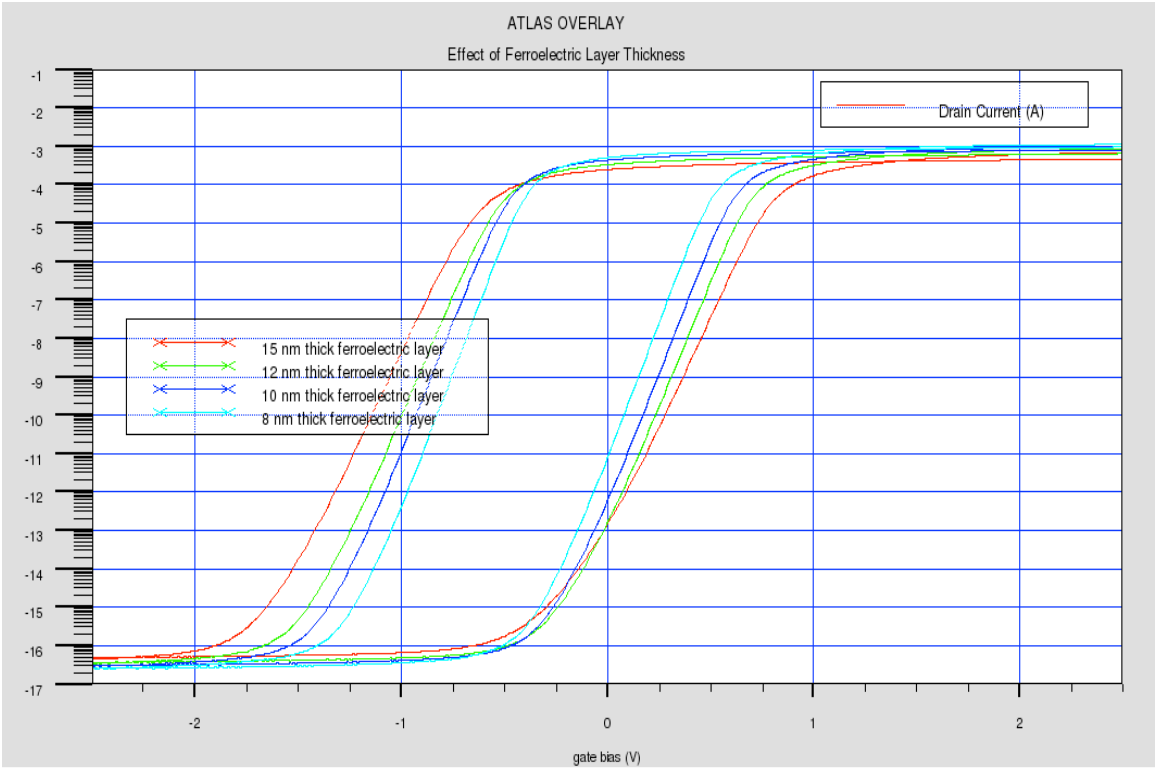



**Fig. 4.3. Effect of ferroelectric layer thickness.**

Since the remnant polarization of Si:$HfO_2$ considerably increased by decreasing the layer thickness, the memory window (MW) decreased. The advantage of using thinner layer of Si:$HfO_2$ ferroelectric material is the possibility of accomplishing ultra low-power FeFET devices. As seen in Fig. 4.3, the Memory window (MW) decreased from 1.4 V to about 0.85 V as the ferroelectric layer thickness was decreased from 15 nm to 8 nm, respectively. Table 4.3 shows a comparison between the simulated devices.

**Table 4.3: Comparison of results of the simulated devices.**

| Ferroelectric Layer Thickness | Memory Window (MW) |
|---|---|
| 15 nm | 1.4 V |
| 12 nm | 1.25 V |
| 10 nm | 1.1 V |
| 8 nm | 0.85 V |

## 4.3 Effect of Buffer Layer Thickness:

The FeFET device, which has 10 nm thick ferroelectric layer, has been simulated with 8 Å thick $HfO_2$ buffer layer, with 5 Å thick $HfO_2$ buffer layer and without buffer layer. These simulations have shown that the FeFET device with no buffer layer has the largest memory window. This means removing the buffer layer has reduced the effect of voltage divider. Fig. 4.4 and 4.5 show the simulated device and the hysteresis loops, respectively.

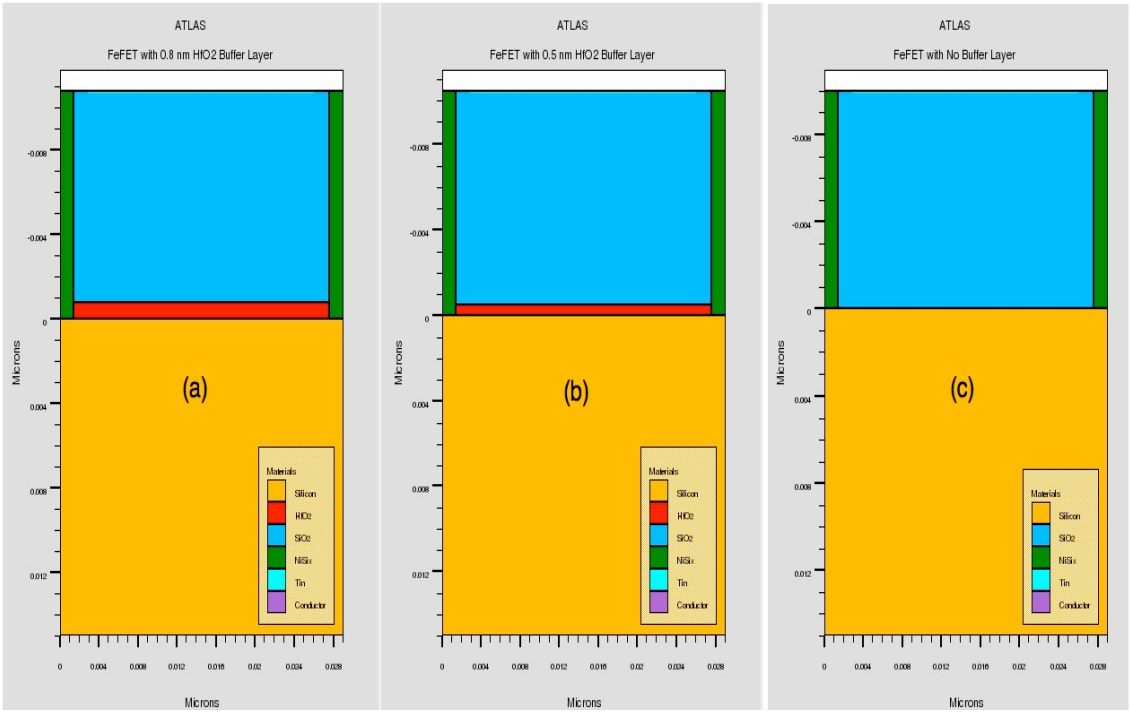



**Fig. 4.4. FeFET device (a) with 8 Å thick $HfO_2$ buffer layer (b) with 5 Å thick $HfO_2$ buffer layer, and (c) without buffer layer (dimensions in μm).**

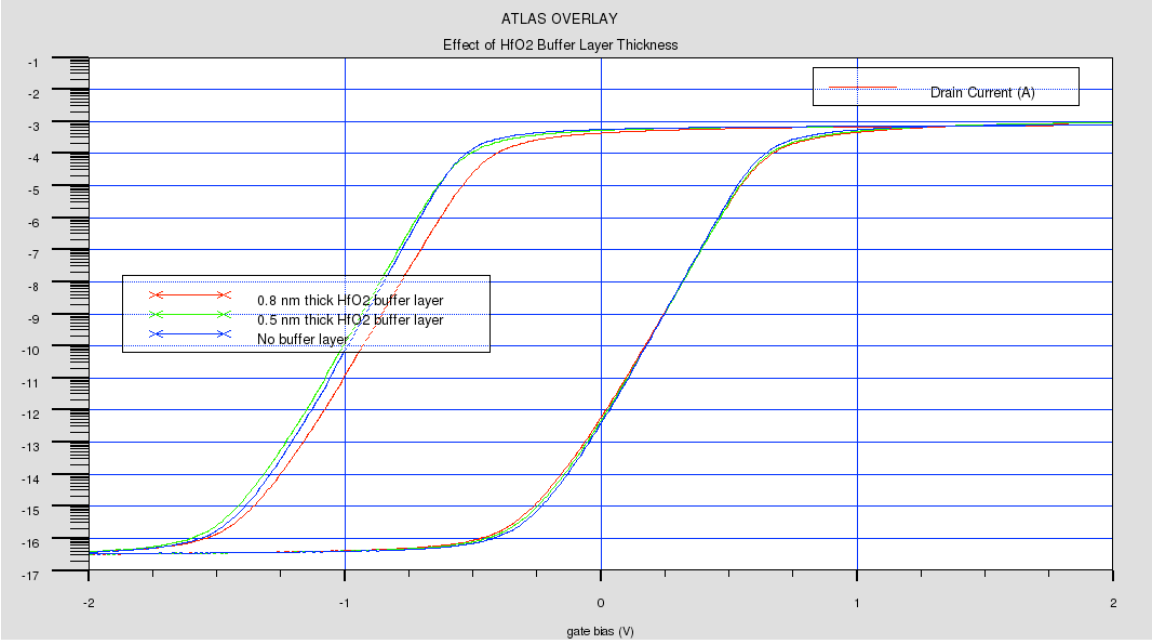



**Fig. 4.5. I-V hysteresis loops of the FeFET device with 8 Å thick $HfO_2$ buffer layer, with 5 Å thick $HfO_2$ buffer layer and without buffer layer.**

As seen in Fig. 4.5, the higher thickness, which is 8 Å, reduced the buffer layer capacitance and caused a higher voltage drop across the buffer layer and a smaller voltage drop across the ferroelectric layer. Table 4.4 shows the effect of the $HfO_2$ buffer layer thickness on the memory window value.

**Table 4.4: Effect of buffer layer thickness on the FeFET performance.**

| Buffer layer Thickness | Memory Window (MW) |
|---|---|
| 8 Å | 1.1 V |
| 5 Å | 1.2 V |
| No Buffer Layer | 1.22 V |

## 4.4 Effect of the Buffer Layer Permittivity:

When buffer layers with low permittivity were used instead of the hafnium oxide ($HfO_2$) buffer layer, the total capacitance decreased. Thus, the memory window of the FeFET (with 10 nm ferroelectric) decreased. Fig. 4.7 shows the degradation in memory window value when the hafnium oxide ($HfO_2$) was replaced by other materials. These materials are silicon oxide ($SiO_2$) and silicon nitride ($Si_3N_4$).

The total capacitance of an MFIS-FeFET is given by:

$$C_{total} = \left( \frac{1}{C_f} + \frac{1}{C_b} + \frac{1}{C_s} \right)^{-1} \tag{4.1}$$

Where,

$$C_f = \frac{\varepsilon_f A_f}{t_f} \tag{4.2}$$

$$C_b = \frac{\varepsilon_b A_b}{t_b} \tag{4.3}$$

Where,

$$\varepsilon_f = \varepsilon_0 \varepsilon_{f,r} \tag{4.4}$$

$$\varepsilon_b = \varepsilon_0 \varepsilon_{f,b} \tag{4.5}$$

A is the area in square meters, and $t_f$ is the ferroelectric layer thickness. Fig 4.6 and 4.7 show the simulated FeFET with different buffer layer materials and the I-V hysteresis loops, respectively.

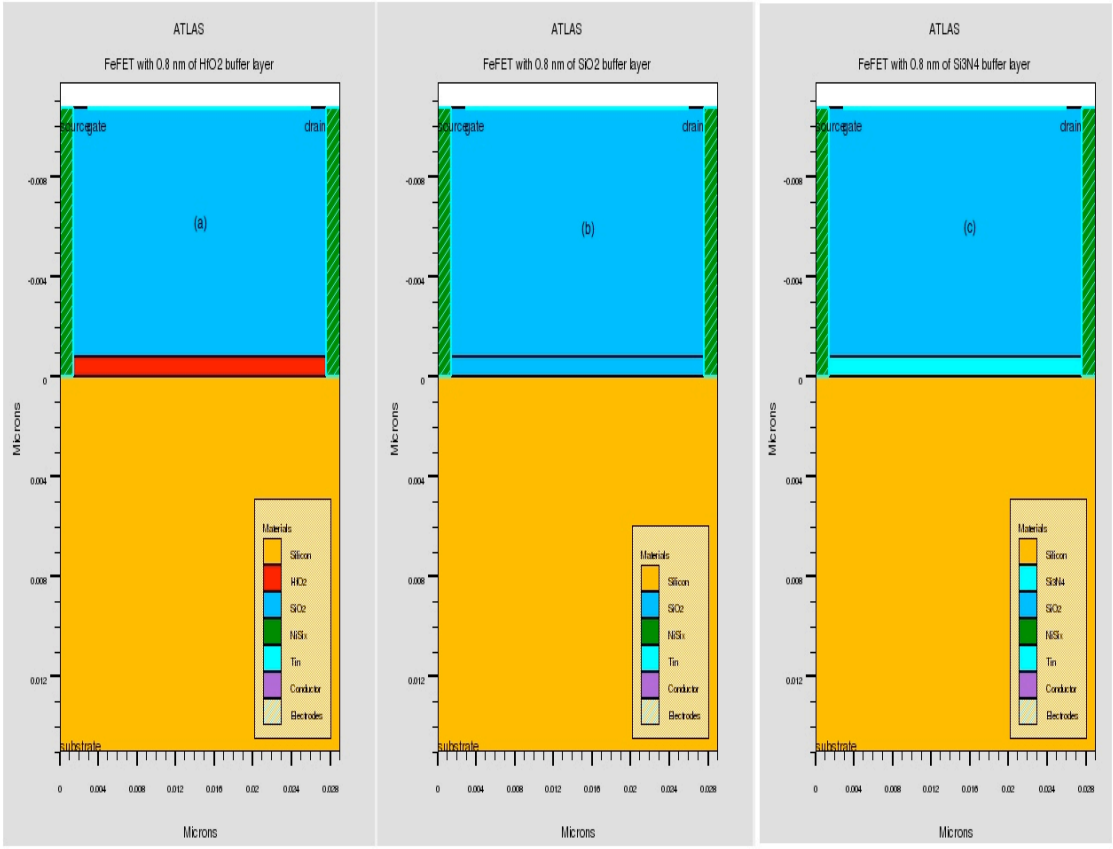



**Fig. 4.6. FeFET device with 8 Å of (a) $HfO_2$ buffer layer (b) $SiO_2$ buffer layer, and (c) $Si_3N_4$ buffer layer (dimensions in µm).**

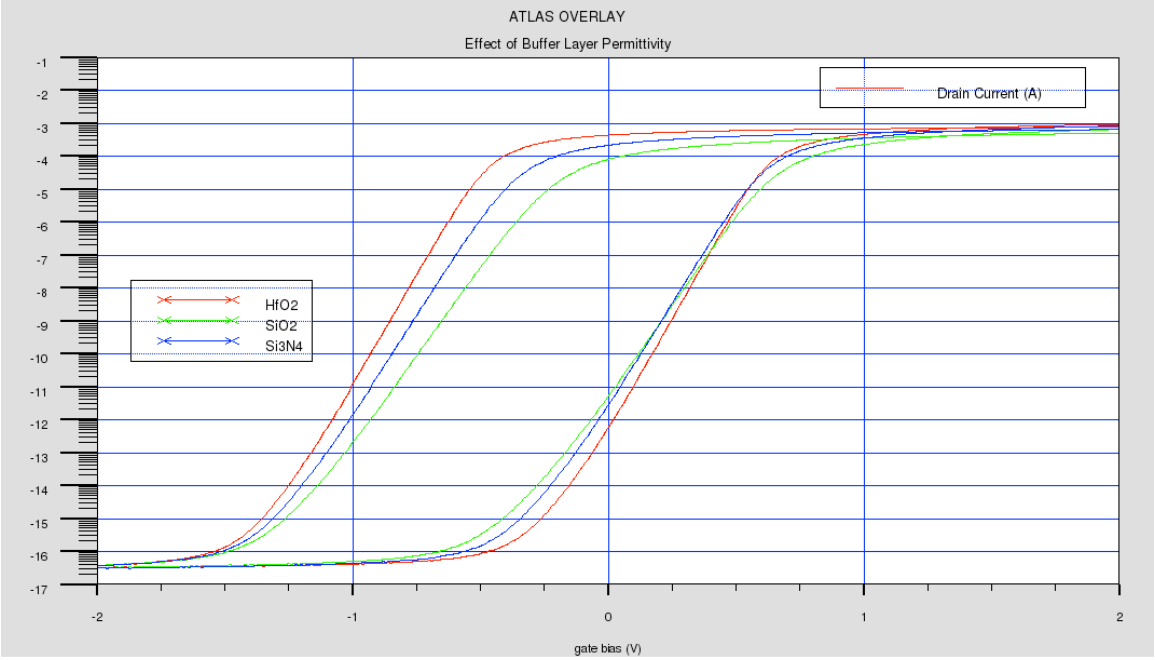



**Fig. 4.7. I-V hysteresis loops of the FeFET device with 8 Å of $HfO_2$ buffer layer, $SiO_2$ buffer layer, and $Si_3N_4$ buffer layer.**

Table 4.5 shows the effect of the buffer layer permittivity on the FeFET performance.

**Table 4.5: Effect of buffer layer permittivity on the FeFET performance.**

| Buffer Layer Material | Dielectric Constant [34] | Memory Window (MW) |
|---|---|---|
| $HfO_2$ | 25 | 1.1 V |
| $SiO_2$ | 3.9 | 0.85 V |
| $Si_3N_4$ | 7 | 0.95 V |

## 4.5 Effect of the Applied Electric Field:

When the applied electric field was less then the coercive field of the ferroelectric layer, minor hysteresis loops with smaller memory window were observed. The memory window increased as the applied electric field increased as seen in Fig. 4.8. The I-V

curves were obtained by keeping the drain voltage constant and sweeping the gate voltage between the write-voltage ($V_{dd}$) and the erase-voltage ($-V_{dd}$).

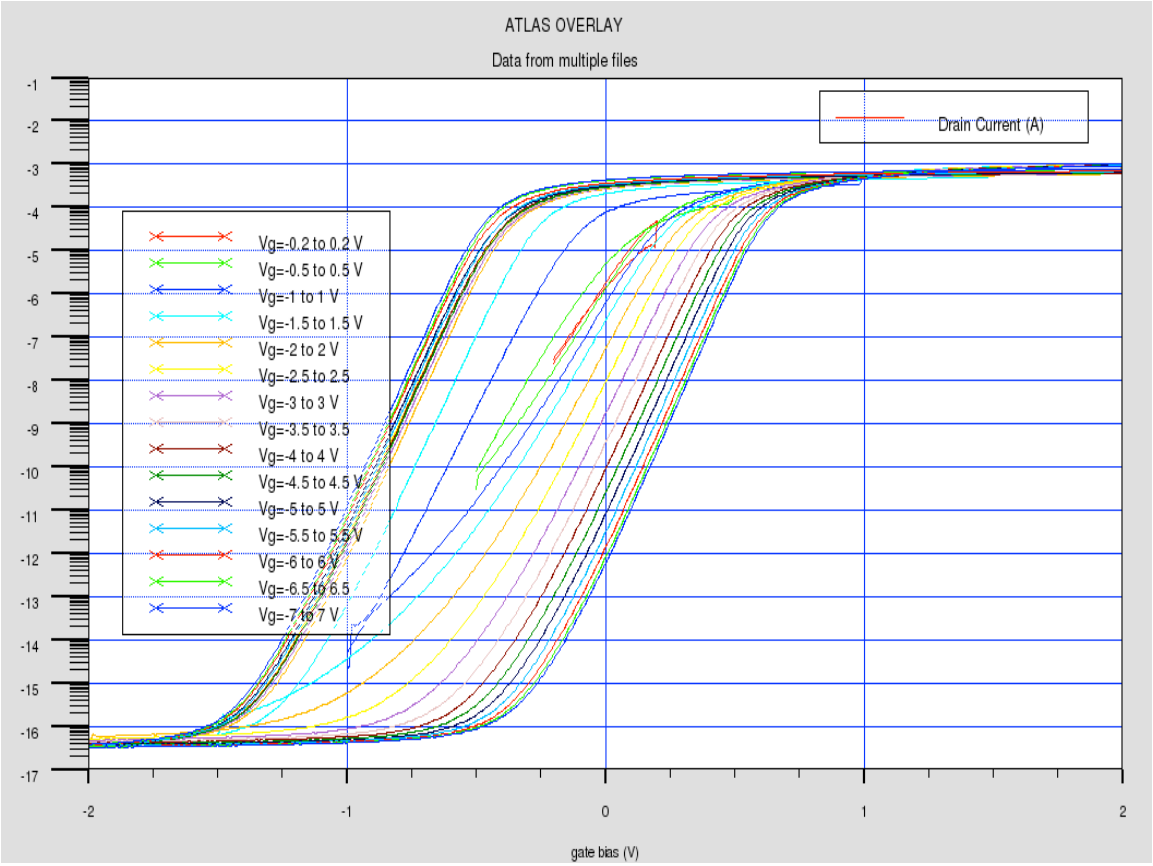



**Fig. 4.8. I-V hysteresis loops of the FeFET device with different applied electric fields.**

## 4.6 Effect of Polarization on Threshold Voltage:

Previous results have shown that the hysteresis effect of the Si:$HfO_2$ ferroelectric material has produced a significant shift in the transistor threshold voltage. This shift shows that the hysteresis effect in the ferroelectric polarization has resulted in different threshold voltages depending upon the direction of the gate sweep. Fig. 4.9 and 4.10 show the transistor with no ferroelectric material and the resulted I-V curve.

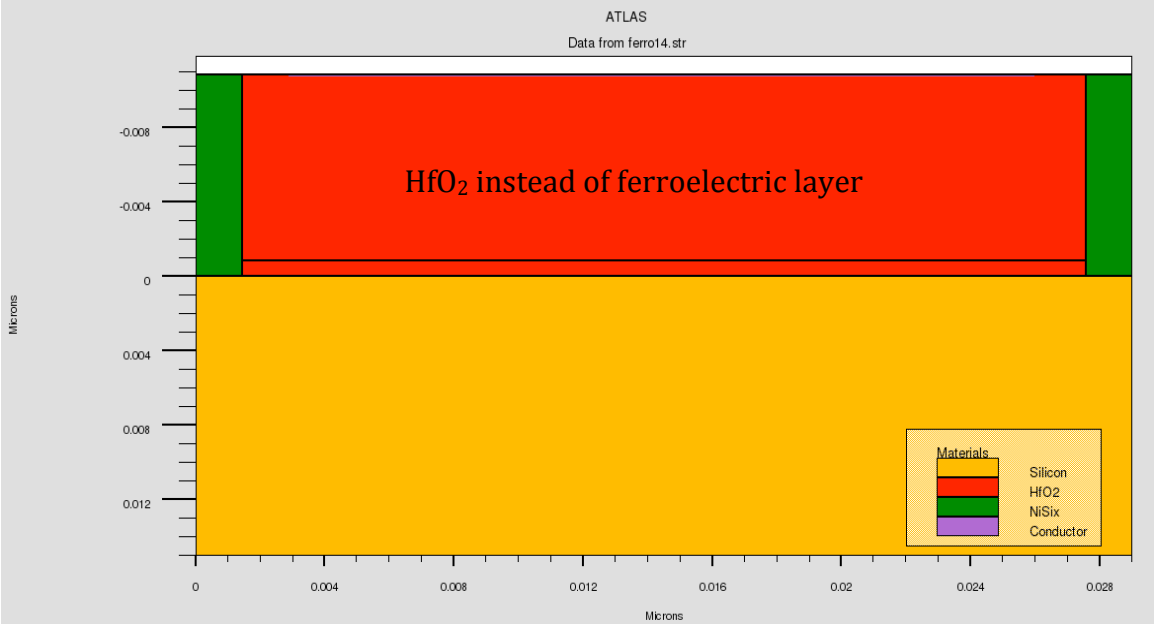



**Fig. 4.9. Transistor device with no ferroelectric layer (dimensions in µm).**

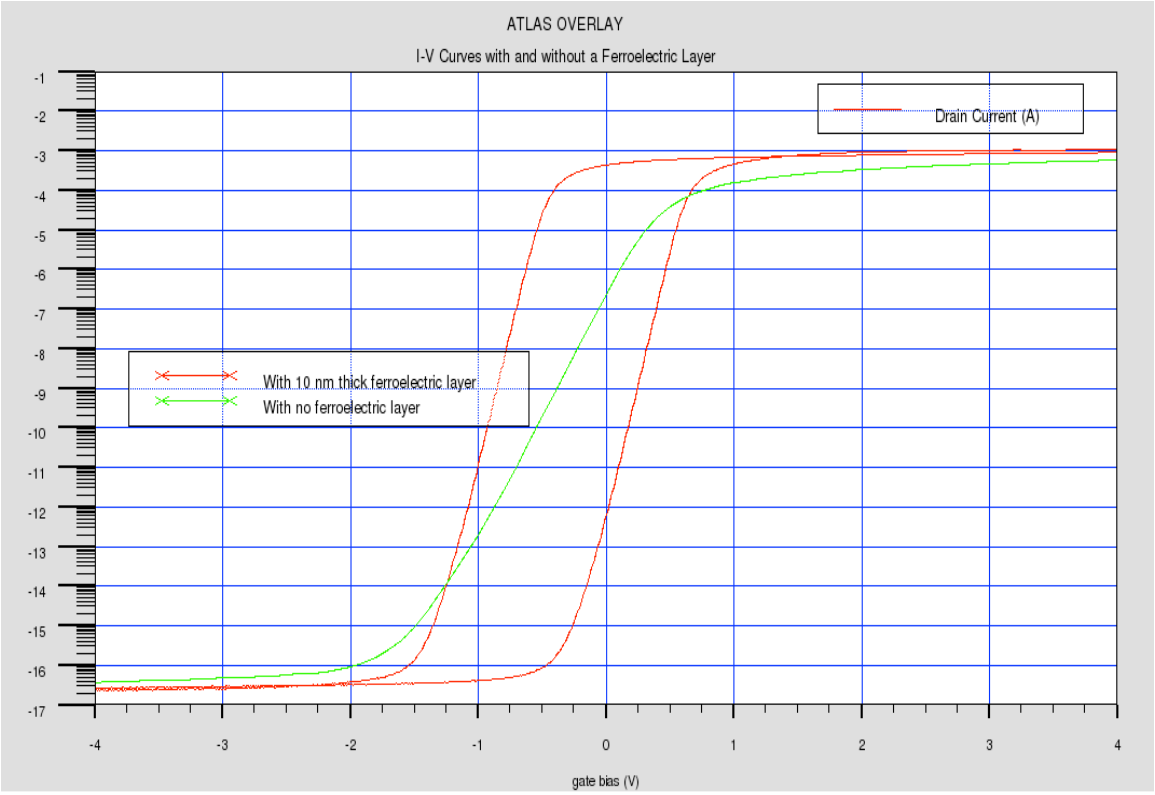



**Fig. 4.10. I-V curves with 10 nm thick ferroelectric layer and with no ferroelectric layer**

As observed in Fig. 4.10, the sub-threshold slop is better in FeFET due to internal voltage amplification. The improvement in the sub-threshold voltage due to incorporating a ferroelectric layer is called internal voltage amplification due to negative capacitance.

# CHAPTER 5 – CONCLUSIONS AND FUTURE WORK

This chapter summarizes the key points of this study. Moreover, It suggests future studies in the field of ferroelectric-based devices.

## 5.1 Conclusions:

Ferroelectric Field Effect Transistors (FeFETs) have been introduced as the best solution to avoid data loss during read out processes in FeRAMs. Since the reading process depends on the sensing of the conductance in the channel region in FeFETs, data can be kept with no change.

Lead Zirconate Titanate (PZT) and Strontium Bismuth Tantalate (SBT) ferroelectric materials have been studied for a long time. The main disadvantage of these ferroelectric materials is that the coercive fields considerably increase as thickness is scaled down. FeFET devices that have PZT or SBT ferroelectric materials suffer from charge injection from semiconductor to ferroelectric material. Therefore, it is required to incorporate a dielectric layer between the semiconductor and the ferroelectric layer to reduce the charge injection effect. Using silicon doped hafnium oxide ($Si:HfO_2$) as a ferroelectric layer has successfully reduced this effect; thus, there is no need for using a buffer layer. Since the dielectric layer causes a voltage drop due to the formation of two serial capacitors, using $Si:HfO_2$ makes it possible to avoid this unwanted effect. Another disadvantage of using a buffer layer is that a depolarization field can be created. This effect can be avoided by using $Si:HfO_2$ as a ferroelectric layer.

The simulated $Si:HfO_2$ FeFET has shown large memory windows even with a very thin ferroelectric layer. When the ferroelectric thickness was 10 nm, the memory window was about 1.22 V even without a buffer layer. This means that the $Si:HfO_2$ can

effectively reduce the current leakage. When low permittivity buffer layers were used, the memory window of the FeFET, which has 10 nm ferroelectric layer, was degraded to less than 1 V.

The discovery of ferroelectric properties in silicon doped hafnium oxide (Si:$HfO_2$) has resolved the obstacles of limited scalability and CMOS incompatibility of conventional ferroelectric materials. The gap to the logic technology roadmap could be finally closed by using novel material as a ferroelectric material. Si:$HfO_2$ makes it possible to accomplish highly scaled and ultra low-power FeFETs.

## 5.2 Future Work:

Two components of the Si:$HfO_2$ FeFET device are in need for further study. The first is the negative capacitance effect of Si:$HfO_2$ material in FeFETs. The negative capacitance FETs (NCFETs) can be used as step-up voltage transformers. This novel technique can reduce the sub-threshold swing (SS) to less than 60 mV/decade. The second component is the surface potential of the NCFeFET devices.

To accomplish this study, the structure of the device should be modified to make it possible to access the negative capacitance region. In other words, the semiconductor capacitance should be reduced to make it smaller than the ferroelectric capacitance. It is significant to develop a proper surface potential model for Silvaco Atlas to achieve effective simulations of NCFETs.

Another area for future work is to replace the Si:$HfO_2$ material by aluminium doped hafnium oxide (Al:HfO2). This material can be studied as a ferroelectric material. By selecting either a divalent or trivalent doping metal, the electron affinity of the dielectric material can be controlled, while also providing a higher dielectric constant material then silicon dioxide. It is significant to have some permittivity measurements to simulate Al:$HfO_2$ FeFET devices using Silvaco Atlas . In addition, Al:$HfO_2$ Ferroelectric Tunnel Junction (Al:$HfO_2$ FTJ) is a good area to be studied in the future. In Ferroelectric Tunnel Junction (FJT) devices, two metal electrodes are separated by a thin ferroelectric layer. The resistance of this kind of devices, which is known as tunneling electroresistance (TER), mainly depends on the direction of the polarization. There are at least two mechanisms of the TER effect that can be studied in the future. The first mechanism is the change in the electrostatic potential across the ferroelectric layer. The second suggested mechanism is the change in the attenuation constant of the barrier. Fig. 5.1 shows the main suggested subjects that can be studied in the future.

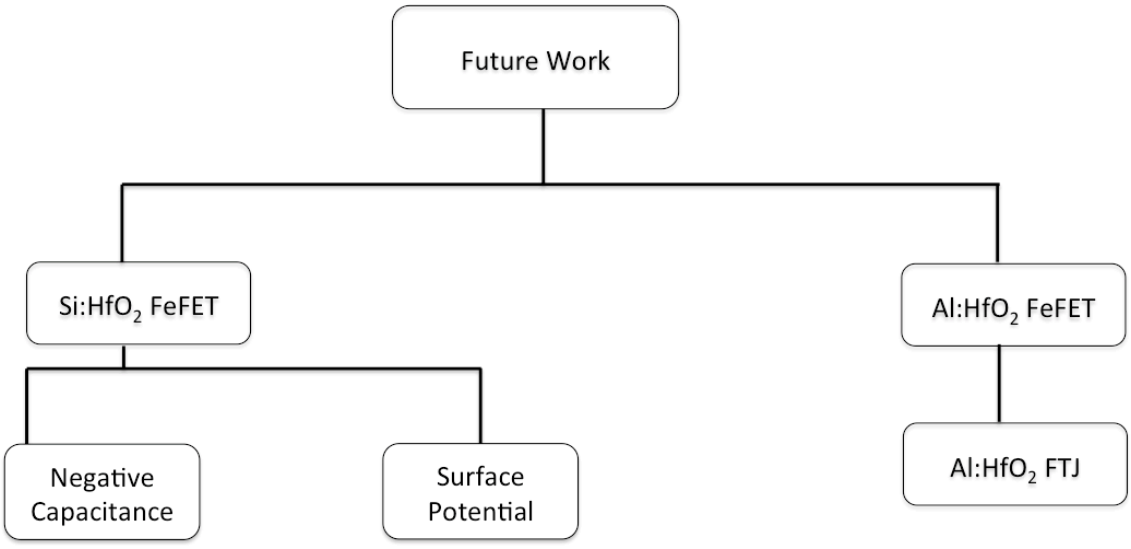



**Fig. 5.1. Suggested subjects for future work.**

# References


[1] S. H. Le, B. R. Salmassi, J. N. Burghartz,, P. M. Sarro, ―Characterization of ferroelectric thin films materials for FeRAM,‖ Proc SAFE & Prorisc 2004, Veldhoven, Nov 2004, pp. 710-713.

[2] P. Muralt, ―Ferroelectric thin film for micro-sensors and actuators: A review,‖ *J. Micromech. Microeng.*, vol. 10, no. 2, pp. 136–146, 2000.

[3] D. K. Uchino, *Ferroelectric Devices*, Boca Raton, FL: CRC, 2000.

[4] J. F. Scott, F. D. Morrison, Y. K. Hoo, A. D. Milliken, H. J. Fan, S. Kawasaki, M. Miyake, T. Tatsuta, and O. Tsuji, ―Ferroelectric thin film devices: Failure mechanisms and new prototype nano-structures,‖ *Proc. 16th IEEE Int. Symp. Appl. Ferroelectr.*, pp. 5–8, 2007.

[5] Dawber, M., K. M. Rabe, and J. F. Scott. "Physics of thin-film ferroelectric oxides." *REVIEWS OF MODERN PHYSICS* 77 (2005): 1083-130.

[6] R. H. Dennard et al., "Design of ion-implanted MOSFET's with very small physical dimensions", IEEE Journal of Solid-State Circuits, SC-9 (5) pp. 256–268, (1974).

[7] *Stony Brook University - Matt Dawber's Group*. 21 May 2013. Web. 2 July 2014. <http://mini.physics.sunysb.edu/~mdawber/research.htm>.

[8] Shur, V. Ya, et al. "Switching in Ferroelectric Thin Films: How to Extract Information about Domain Kinetics from Traditional Current Data." IEEE 16.5 (1995): 669-73

[9] Poppel, Matthias. "The FRAM Pentathlon." *EP&Dee*. 21 June 2011. Web. 27 July 2014. <http://www.epd-ee.eu/article/7686>.

[10] Onodera, Akira, Masanori Fukunaga, and Masaki Takesada. "Ferroelectric Instability and Dimensionality in Bi-Layered Perovskites and Thin Films." *Advances in Condensed Matter Physics* (2012): 1-10.

[11] Fitsilis, Michael. "Scaling of the Ferroelectric Field Effect Transistor and Programming Concepts for Non-volatile Memory Applications." Diss. 2005.

[12] Ishiwara, Hiroshi. "Recent Progress in Ferroelectirc Memory Technology." *IEEE* (2006).

[13] Nishimatsu, Takeshi. "Molecular Dynamics Simulations of Hysteresis Loops for BaTiO3 Ferroelectric Thin-Film Capacitors Using the feram Code." *SourceForge*. 2010. Web. 29 May 2014. <http://loto.sourceforge.net/feram/>.

[14] Poole, Ian. "FRAM Ferroelectric RAM Technology & Operation." Radio-Electronics. Web. 14 Apr. 2014.
<http://www.radio-electronics.com/info/data/semicond/memory/fram-ferroelectric-random-access-memory-technology-operation-theory.php>.

[15] Zhang, J., et al. "Influence of the ferroelectric–electrode interface on the characteristics of MFIS-FETs." Solid-State Electronics (2009): 563-66.

[16] H.T Lue et.al IEEE transactions on electron devices 49, No.10 ,2002

[17] Chai, Francis K., et al. "Effects of Scaling Thickness and Niobium Doping Level on Ferroelectric Thin Film Capacitor Memory Operation." Electron Devices Meeting (IEDM) 95 (1995): 123-26.

[18] Ma, T. P. "FEFET (Ferroelectric FET) -FEDRAM (Ferroelectric DRAM)." Yale University. New Haven, CT, USA. Lecture.

[19] Tue, Phan Trong, Bui Trinh, and Takaaki Miyasako. "Fabrication and Characterization of a Ferroelectric-Gate FET With a ITO/PZT/SRO/Pt Stacked Structure." *22nd International Conference on Microelectronics* (2010).

[20] Roy, A., A. Dhar, and S. K. Ray. "Characteristics of Al/SrBi2Ta2O9/HfO2/Si structure using HfO2 as buffer layer for ferroelectric-gate field effect transistors." *IEEE* (2007).

[21] Setter, N., et al. "Ferroelectric thin films: Review of materials, properties, and applications." JOURNAL OF APPLIED PHYSICS 100 (2006): 051606-1-051606-46.

[22] Kim, Y. T., et al. "Effect of Insulator on Memory Window of Metal-Ferroelectric-Insulator - Semiconductor – Field Effect Transistor (MEFISFET) - Non Destructive Readout Memory Devices." *IEEE* (1998): 35-38.

[23] N. A. Pertsev, J. R. Contreras, V. G. Kukhar, B. Hermanns, H. Kohlstedt, and R. Waser, Appl. Phys. Lett. 83, 3356 (2003).

[24] Ma, T.P.; Han, J.P. Why is nonvolatile ferroelectric memory field-effect transistor still elusive? IEEE Electron. Device Lett. 2002, 23, 386-388.

[25] Boscke, T. S., et al. "Ferroelectricity in Hafnium Oxide Thin Films." Applied Physics Letters 99.1 (2011).

[26] Sun, Jing, and Xuejun Zheng. "Modeling of MFIS-FETs for the Application of Ferroelectric Random Access Memory." *IEEE TRANSACTIONS ON ELECTRON DEVICES* 58.10 (2011): 3559-65.

[27] Feng, Tingting, Dan Xie, and Seppo Honkanen. "Nd-doped Bismuth Titanate Based Ferroelectric Field Effect Transistor: Design, Fabrication, and Optimization." *IEEE* (2011).

[28] Yurchuk, Ekaterina, Johannes Müller, and Raik Hoffmann. "HfO2-based Ferroelectric Field-Effect Transistors with 260 nm channel length and long data retention." *IEEE* (2012).

[29] Mueller, Stefan, Johannes Muller, and Tom Herrmann. "Performance Investigation and Optimization of Si:Hf02 FeFETs on a 28 nm Bulk Technology." 2013 Joint UFFC, EFTF and PFM Symposium (2013).

[30] Frank, David J., et al. "The Quantum Metal Ferroelectric Field-Effect Transistor." *IEEE TRANSACTIONS ON ELECTRON DEVICES* 61.6 (2014): 2145-46.

[31] International Roadmap Committee (2014, Jun 6). International Technology Roadmap for Semiconductors [Online]. Available: http://www.itrs.net/Links/2013ITRS/Home2013.htm

[32] *Silvaco International, Atlas User's manual,* Silvaco International, October 17, 2013.

[33] Device, Maria Concetta. "Device Simulation." IMS CAD & Design Services. *Device simulation*. By Maria Concetta Allia.

[34] Huang, A. P., Z. C. Yang, and Paul K. Chu. "Hafnium-based High-k Gate Dielectrics." *intechopen* (2010): 333-50.

# Appendix A

## Ferroelectric Parameters Calculator

```
clc;

clear;

close all;

t=10;

x=0.35;

y=0.37475;

w=0.01;

z=0.35;

thickness=input('thickness= ');

if thickness > t

    pr=9-(x*(thickness-t))

    ps=9.5-(y*(thickness-t))

    ec=1.1-(w*(thickness-t))

    epsf=32-(z*(thickness-t))

else pr=9+(x*(t-thickness))

    ps=9.5+(y*(t-thickness))

    ec=1.1+(w*(t-thickness))

    epsf=32+(z*(t-thickness))

end
```

# Appendix B

# Atlas Code of the FeFET with Different Ferroelectric Thicknesses

```
##############################################################################
#####
##############################################################################
#####
#

go atlas simflags="-p 1"

####################################
# mesh and structure definition
####################################
#
mesh space.mult=1.0 outf=ferro1_1.str
x.m l=0    s=0.000578
x.m l=0.00144 s=0.000578
x.m l=0.00288  s=0.000568
x.m l=0.026  s=0.000289
x.m l=0.027 s=0.000289
x.m l=0.029  s=0.000578

#y.m l=-0.010225 s=0.00017
y.m l=-0.0158 s=0.00017
y.m l=-0.00029 s=0.000284
y.m l=-0.0008 s=0.0025
y.m l=0.0  s=0.000114
y.m l=0.015  s=0.002273

eliminate y.dir y.min=0.00125 x.min=0.003125 x.max=0.028125
eliminate y.dir y.min=0.0025

region num=1 silicon y.min=0.0
region num=2 material=HfO2 y.max=0.0 y.min=-0.0008
region num=3 oxide y.max=-0.0008 y.min=-0.0158
#region num=4 oxide y.max=-0.01020 y.min=-0.010225

electrode num=1 material=NiSi name=source y.max=0.0 x.max=0.001444
electrode num=2 material=NiSi name=drain y.max=0.0 x.min=0.027444
electrode num=3 material=TiN name=gate top x.min=0.002889 x.max=0.026
electrode num=4 name=substrate bottom
```

```
doping uniform conc=1e17 p.type
doping gaus conc=1e19 n.type x.right=0.004546 y.min=0 y.max=0.01 char=0.0008
doping gaus conc=1e19 n.type x.left=0.024454 y.min=0 y.max=0.01 char=0.0008


#####################################
# ferroelectric material defining
#####################################
model region=3 ferro
material region=3 ferro.ec=1.05e6 ferro.pr=7.25e-6 ferro.ps=7.6262e-6 ferro.epsf=30.25

#########################################
# gate workfunction and channel mobility
#########################################
contact num=3
material mun=800.0

save outf=ferro1_1.str
tonyplot ferro1_1.str

#######################################
# obtaining Id - Vg characteristic
#######################################
#method newton autonr
method gummel newton itlim=4 trap maxtrap=2 vsatmod.inc=0.01 carriers=2
output con.band val.band band.param e.mobility h.mobility

solve init
solve vd=0.1
probe x=0 y=-0.0075 dir=90 polarization
#######################################
# forward sweep
#######################################
log outf=ferro1_2.log master
solve vgate=-7.0 vstep=0.01 vfinal=7.0 name=gate
#######################################
# reverse sweep
#######################################
material ferro.ec=-1.05e6
solve vstep=-0.01 vfinal=-7.0 name=gate
#######################################
#Id-Vg plot
#######################################
tonyplot -st ferro1_2.log -set ferro_1.set
#############################################################################
```

```
#####
################################################################################
#####
go atlas simflags="-p 1"

####################################
# mesh and structure definition
####################################
#
mesh space.mult=1.0 outf=ferro2_1.str
x.m l=0    s=0.000578
x.m l=0.00144 s=0.000578
x.m l=0.00288  s=0.000568
x.m l=0.026  s=0.000289
x.m l=0.027 s=0.000289
x.m l=0.029  s=0.000578

#y.m l=-0.010225 s=0.00017
y.m l=-0.0128 s=0.00017
y.m l=-0.00029 s=0.000284
y.m l=-0.0008 s=0.0025
y.m l=0.0  s=0.000114
y.m l=0.015  s=0.002273

eliminate y.dir y.min=0.00125 x.min=0.003125 x.max=0.028125
eliminate y.dir y.min=0.0025

region num=1 silicon y.min=0.0
region num=2 material=HfO2 y.max=0.0 y.min=-0.0008
region num=3 oxide y.max=-0.0008 y.min=-0.0128
#region num=4 oxide y.max=-0.01020 y.min=-0.010225

electrode num=1 material=NiSi name=source y.max=0.0 x.max=0.001444
electrode num=2 material=NiSi name=drain y.max=0.0 x.min=0.027444
electrode num=3 material=TiN name=gate top x.min=0.002889 x.max=0.026
electrode num=4 name=substrate bottom

doping uniform conc=1e17 p.type
doping gaus conc=1e19 n.type x.right=0.004546 y.min=0 y.max=0.01 char=0.0008
doping gaus conc=1e19 n.type x.left=0.024454 y.min=0 y.max=0.01 char=0.0008


####################################
# ferroelectric material defining
####################################
model region=3 ferro
```

```
material region=3 ferro.ec=1.08e6 ferro.pr=8.3e-6 ferro.ps=8.7505e-6 ferro.epsf=31.3

########################################
# gate workfunction and channel mobility
########################################
contact num=3
material mun=800.0

save outf=ferro2_1.str
tonyplot ferro2_1.str

########################################
# obtaining Id - Vg characteristic
########################################
#method newton autonr
method gummel newton itlim=20 trap maxtrap=10 vsatmod.inc=0.01 carriers=2
output con.band val.band band.param e.mobility h.mobility

solve init
solve vd=0.1
probe x=0 y=-0.006 dir=90 polarization
########################################
# forward sweep
########################################
log outf=ferro2_2.log master
solve vgate=-7.0 vstep=0.01 vfinal=7.0 name=gate
########################################
# reverse sweep
########################################
material ferro.ec=-1.08e6
solve vstep=-0.01 vfinal=-7.0 name=gate
########################################
#Id-Vg plot
########################################
tonyplot -st ferro2_2.log -set ferro_1.set
################################################################################
#####
go atlas simflags="-p 1"

####################################
# mesh and structure definition
####################################
#
mesh space.mult=1.0 outf=ferro3_1.str
x.m l=0    s=0.000578
x.m l=0.00144 s=0.000578
```

```
x.m l=0.00288  s=0.000568
x.m l=0.026  s=0.000289
x.m l=0.027 s=0.000289
x.m l=0.029  s=0.000578

#y.m l=-0.010225 s=0.00017
y.m l=-0.01080 s=0.00017
y.m l=-0.00029 s=0.000284
y.m l=-0.00080 s=0.0025
y.m l=0.0  s=0.000114
y.m l=0.015  s=0.002273

eliminate y.dir y.min=0.00125 x.min=0.003125 x.max=0.028125
eliminate y.dir y.min=0.0025

region num=1 silicon y.min=0.0
region num=2 material=HfO2 y.max=0.0 y.min=-0.00080
region num=3 oxide y.max=-0.00080 y.min=-0.01080
#region num=4 oxide y.max=-0.01020 y.min=-0.010225

electrode num=1 material=NiSi name=source y.max=0.0 x.max=0.001444
electrode num=2 material=NiSi name=drain y.max=0.0 x.min=0.027444
electrode num=3 material=TiN name=gate top x.min=0.002889 x.max=0.026
electrode num=4 name=substrate bottom

doping uniform conc=1e17 p.type
doping gaus conc=1e19 n.type x.right=0.004546 y.min=0 y.max=0.01 char=0.0008
doping gaus conc=1e19 n.type x.left=0.024454 y.min=0 y.max=0.01 char=0.0008

#####################################
# ferroelectric material defining
#####################################
model region=3 ferro
material region=3 ferro.ec=1.1e6 ferro.pr=9.0e-6 ferro.ps=9.5e-6 ferro.epsf=32

#########################################
# gate workfunction and channel mobility
#########################################
contact num=3
material mun=800.0

save outf=ferro3_1.str
tonyplot ferro3_1.str

#####################################
# obtaining Id - Vg characteristic
```

```
########################################
#method newton autonr
method gummel newton itlim=20 trap maxtrap=10 vsatmod.inc=0.01 carriers=2
output con.band val.band band.param e.mobility h.mobility

solve init
solve vd=0.1
probe x=0 y=-0.005 dir=90 polarization
########################################
# forward sweep
########################################
log outf=ferro3_2.log master
solve vgate=-7.0 vstep=0.01 vfinal=7.0 name=gate
########################################
# reverse sweep
########################################
material ferro.ec=-1.1e6
solve vstep=-0.01 vfinal=-7.0 name=gate
########################################
#Id-Vg plot
########################################
tonyplot -st ferro3_2.log -set ferro_1.set


################################################
################################################################################
################################################################################
###############
################################################################################
#####

go atlas simflags="-p 1"

###################################
# mesh and structure definition
###################################
#
mesh space.mult=1.0 outf=ferro4_1.str
x.m l=0    s=0.000578
x.m l=0.00144 s=0.000578
x.m l=0.00288  s=0.000568
x.m l=0.026  s=0.000289
x.m l=0.027 s=0.000289
x.m l=0.029  s=0.000578

#y.m l=-0.010225 s=0.00017
```

```
y.m l=-0.0088 s=0.00017
y.m l=-0.00029 s=0.000284
y.m l=-0.0008 s=0.0025
y.m l=0.0  s=0.000114
y.m l=0.015  s=0.002273

eliminate y.dir y.min=0.00125 x.min=0.003125 x.max=0.028125
eliminate y.dir y.min=0.0025

region num=1 silicon y.min=0.0
region num=2 material=HfO2 y.max=0.0 y.min=-0.0008
region num=3 oxide y.max=-0.0008 y.min=-0.0088
#region num=4 oxide y.max=-0.01020 y.min=-0.010225

electrode num=1 material=NiSi name=source y.max=0.0 x.max=0.001444
electrode num=2 material=NiSi name=drain y.max=0.0 x.min=0.027444
electrode num=3 material=TiN name=gate top x.min=0.002889 x.max=0.026
electrode num=4 name=substrate bottom

doping uniform conc=1e17 p.type
doping gaus conc=1e19 n.type x.right=0.004546 y.min=0 y.max=0.01 char=0.0008
doping gaus conc=1e19 n.type x.left=0.024454 y.min=0 y.max=0.01 char=0.0008


#####################################
# ferroelectric material defining
#####################################
model region=3 ferro
material region=3 ferro.ec=1.12e6 ferro.pr=9.7e-6 ferro.ps=10.25e-6 ferro.epsf=32.7

#########################################
# gate workfunction and channel mobility
#########################################
contact num=3
material mun=800.0

save outf=ferro4_1.str
tonyplot ferro4_1.str

#######################################
# obtaining Id - Vg characteristic
#######################################
#method newton autonr
method gummel newton itlim=20 trap maxtrap=10 vsatmod.inc=0.01 carriers=2
output con.band val.band band.param e.mobility h.mobility
```

```
solve init
solve vd=0.1
probe x=0 y=-0.004 dir=90 polarization
########################################
# forward sweep
########################################
log outf=ferro4_2.log master
solve vgate=-7.0 vstep=0.01 vfinal=7.0 name=gate
########################################
# reverse sweep
########################################
material ferro.ec=-1.0e6
solve vstep=-0.01 vfinal=-7.0 name=gate
########################################
#Id-Vg plot
########################################
tonyplot -st ferro4_2.log -set ferro_1.set
#########################################################################
#####
#########################################################################
#####
tonyplot -overlay -st ferro1_2.log  ferro2_2.log ferro3_2.log ferro4_2.log -set ferro_1.set

tonyplot -st ferro1_2.log  -overlay ferro2_2.log -overlay ferro3_2.log -overlay
ferro4_2.log -set ferro_1.set

quit
```

# Appendix C

# Atlas Code of the FeFET with Different Buffer Layer Thicknesses

```
go atlas simflags="-p 1"

####################################
# mesh and structure definition
####################################
#
mesh space.mult=1.0 outf=ferro5_1.str
x.m l=0    s=0.000578
x.m l=0.00144 s=0.000578
x.m l=0.00288  s=0.000568
x.m l=0.026  s=0.000289
x.m l=0.027 s=0.000289
x.m l=0.029  s=0.000578

#y.m l=-0.010225 s=0.00017
y.m l=-0.01080 s=0.00017
y.m l=-0.00029 s=0.000284
y.m l=-0.00080 s=0.0025
y.m l=0.0  s=0.000114
y.m l=0.015  s=0.002273

eliminate y.dir y.min=0.00125 x.min=0.003125 x.max=0.028125
eliminate y.dir y.min=0.0025

region num=1 silicon y.min=0.0
region num=2 material=HfO2 y.max=0.0 y.min=-0.00080
region num=3 oxide y.max=-0.00080 y.min=-0.01080
```

```
#region num=4 oxide y.max=-0.01020 y.min=-0.010225

electrode num=1 material=NiSi name=source y.max=0.0 x.max=0.001444
electrode num=2 material=NiSi name=drain y.max=0.0 x.min=0.027444
electrode num=3 material=TiN name=gate top x.min=0.002889 x.max=0.026
electrode num=4 name=substrate bottom

doping uniform conc=1e17 p.type
doping gaus conc=1e19 n.type x.right=0.004546 y.min=0 y.max=0.01 char=0.0008
doping gaus conc=1e19 n.type x.left=0.024454 y.min=0 y.max=0.01 char=0.0008

#####################################
# ferroelectric material defining
#####################################
model region=3 ferro
material region=3 ferro.ec=1.1e6 ferro.pr=9.0e-6 ferro.ps=9.5e-6 ferro.epsf=32

#########################################
# gate workfunction and channel mobility
#########################################
contact num=3
material mun=800.0

save outf=ferro5_1.str
tonyplot ferro5_1.str

#########################################
# obtaining Id - Vg characteristic
#########################################
#method newton autonr
method gummel newton itlim=20 trap maxtrap=10 vsatmod.inc=0.01 carriers=2
```

```
output con.band val.band band.param e.mobility h.mobility

solve init
solve vd=0.1
probe x=0 y=-0.005 dir=90 polarization
########################################
# forward sweep
########################################
log outf=ferro5_2.log master
solve vgate=-7.0 vstep=0.01 vfinal=7.0 name=gate
########################################
# reverse sweep
########################################
material ferro.ec=-1.1e6
solve vstep=-0.01 vfinal=-7.0 name=gate
########################################
#Id-Vg plot
########################################
tonyplot -st ferro5_2.log -set ferro_1.set



################################################
#############################################################################
    #########################################################################
    ###################
go atlas simflags="-p 1"

####################################
# mesh and structure definition
####################################
#
```

```
mesh space.mult=1.0 outf=ferro6_1.str
x.m l=0    s=0.000578
x.m l=0.00144 s=0.000578
x.m l=0.00288  s=0.000568
x.m l=0.026  s=0.000289
x.m l=0.027 s=0.000289
x.m l=0.029  s=0.000578

#y.m l=-0.010125 s=0.00017
y.m l=-0.01050 s=0.00017
y.m l=-0.00029 s=0.000284
y.m l=-0.00050 s=0.0025
y.m l=0.0  s=0.000114
y.m l=0.015  s=0.002273

eliminate y.dir y.min=0.00125 x.min=0.003125 x.max=0.028125
eliminate y.dir y.min=0.0025

region num=1 silicon y.min=0.0
region num=2 material=HfO2 y.max=0.0 y.min=-0.00050
region num=3 oxide y.max=-0.00050 y.min=-0.01050
#region num=4 oxide y.max=-0.01010 y.min=-0.010125

electrode num=1 material=NiSi name=source y.max=0.0 x.max=0.001444
electrode num=2 material=NiSi name=drain y.max=0.0 x.min=0.027444
electrode num=3 material=TiN name=gate top x.min=0.002889 x.max=0.026
electrode num=4 name=substrate bottom

doping uniform conc=1e17 p.type
doping gaus conc=1e19 n.type x.right=0.004546 y.min=0 y.max=0.01 char=0.0008
doping gaus conc=1e19 n.type x.left=0.024454 y.min=0 y.max=0.01 char=0.0008
```

```
#####################################
# ferroelectric material defining
#####################################
model region=3 ferro
material region=3 ferro.ec=1.1e6 ferro.pr=9.0e-6 ferro.ps=9.5e-6 ferro.epsf=32

#########################################
# gate workfunction and channel mobility
#########################################
contact num=3
material mun=800.0

save outf=ferro6_1.str
tonyplot ferro6_1.str

#########################################
# obtaining Id - Vg characteristic
#########################################
#method newton autonr
method gummel newton itlim=20 trap maxtrap=10 vsatmod.inc=0.01 carriers=2
output con.band val.band band.param e.mobility h.mobility

solve init
solve vd=0.1
probe x=0 y=-0.005 dir=90 polarization
#########################################
# forward sweep
#########################################
log outf=ferro6_2.log master
solve vgate=-7.0 vstep=0.01 vfinal=7.0 name=gate
```

```
########################################
# reverse sweep
########################################
material ferro.ec=-1.1e6
solve vstep=-0.01 vfinal=-7.0 name=gate
########################################
#Id-Vg plot
########################################
tonyplot -st ferro6_2.log -set ferro_1.set
################################################
#############################################################################
    #############################################################################
    ####################
go atlas simflags="-p 1"

#####################################
# mesh and structure definition
#####################################
#
mesh space.mult=1.0 outf=ferro7_1.str
x.m l=0    s=0.000578
x.m l=0.00144 s=0.000578
x.m l=0.00288  s=0.000568
x.m l=0.026  s=0.000289
x.m l=0.027 s=0.000289
x.m l=0.029  s=0.000578

#y.m l=-0.010125 s=0.00017
y.m l=-0.01 s=0.00017
#y.m l=-0.00029 s=0.000284
#y.m l=-0.00010 s=0.0025
```

```
y.m l=0.0  s=0.000114
y.m l=0.015  s=0.002273

eliminate y.dir y.min=0.00125 x.min=0.003125 x.max=0.028125
eliminate y.dir y.min=0.0025

region num=1 silicon y.min=0.0
#region num=2 material=HfO2 y.max=0.0 y.min=-0.00010
region num=2 oxide y.max=0.0 y.min=-0.01
#region num=4 oxide y.max=-0.01010 y.min=-0.010125

electrode num=1 material=NiSi name=source y.max=0.0 x.max=0.001444
electrode num=2 material=NiSi name=drain y.max=0.0 x.min=0.027444
electrode num=3 material=TiN name=gate top x.min=0.002889 x.max=0.026
electrode num=4 name=substrate bottom

doping uniform conc=1e17 p.type
doping gaus conc=1e19 n.type x.right=0.004546 y.min=0 y.max=0.01 char=0.0008
doping gaus conc=1e19 n.type x.left=0.024454 y.min=0 y.max=0.01 char=0.0008

#####################################
# ferroelectric material defining
#####################################
model region=2 ferro
material region=2 ferro.ec=1.1e6 ferro.pr=9.0e-6 ferro.ps=9.5e-6 ferro.epsf=32

#########################################
# gate workfunction and channel mobility
#########################################
contact num=3
material mun=800.0
```

```
save outf=ferro7_1.str
tonyplot ferro7_1.str

########################################
# obtaining Id - Vg characteristic
########################################
#method newton autonr
method gummel newton itlim=20 trap maxtrap=10 vsatmod.inc=0.01 carriers=2
output con.band val.band band.param e.mobility h.mobility

solve init
solve vd=0.1
probe x=0 y=-0.005 dir=90 polarization
########################################
# forward sweep
########################################
log outf=ferro7_2.log master
solve vgate=-7.0 vstep=0.01 vfinal=7.0 name=gate
########################################
# reverse sweep
########################################
material ferro.ec=-1.1e6
solve vstep=-0.01 vfinal=-7.0 name=gate
########################################
#Id-Vg plot
########################################
tonyplot -st ferro7_2.log -set ferro_1.set
################################################
```

```
##########################################################################
    ##########################################################################
    ###################
tonyplot -overlay -st ferro5_2.log  ferro6_2.log ferro7_2.log -set ferro_1.set

tonyplot -st ferro5_2.log  -overlay ferro6_2.log -overlay ferro7_2.log -set ferro_1.set

quit
```