8-2014

Process Development for Single-Crystal Silicon Solar Cells

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PROCESS DEVELOPMENT FOR SINGLE-CRYSTAL SILICON SOLAR CELLS

By

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A Thesis
Submitted in Partial Fulfillment
of the Requirements of the Degree of

Master of Science

in Microelectronic Engineering

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ACKNOWLEDGMENT

I would like to express my gratitude by thanking people who have guided me in the best way possible enabling me to successfully complete my Master's degree in the Microelectronic Engineering program at Rochester Institute of Technology.

First and foremost, I would like to thank Almighty for showering his blessings and granting me with strength and confidence to pursue this passion with sheer excitement and determination. I would also like to thank my family, especially ChetAn, RPM, AB, San and Sid, for their undying support and believing in me and my abilities to succeed in this phase of my life.

I would like to express my deep gratitude towards Dr. Michael Jackson for his guidance throughout my tenure at R.I.T. He has been a great advisor and a great educator. Thank you guiding me through with the courses as well as my research. Thank you Dr. Kurinec for being instrumental with my courses, thesis as well as making me a part of the SiSoC research team. I sincerely appreciate the efforts of Dr. Pearson in guiding me through the Microelectronic Engineering Program and also my thesis.

A big vote of thanks to all my professors and staff in MicroE department and Dr. Moon for sharing their wisdom and making me a confident engineer. I sincerely appreciate the efforts of the SMFL staff helping me unconditionally with lab work. My friends, especially Sid, KD, Tarun, Preethi, Dan, QL, Abhi, Karine, Josh have been instrumental in completion of my thesis.

Thank you Varun, Maria, Amoeba, "RIT Losers", CricEngineers, BWW team and all my roomies for the last three years for making my stay in Rochester a bliss and an extremely memorable one. I appreciate your patience and thank you for all the fun times we had.

ABSTRACT

Solar energy is a viable, rapidly growing and an important renewable alternative to other sources of energy generation because of its abundant supply and low manufacturing cost. Silicon still remains the major contributor for manufacturing solar cells accounting for 80% of the market share [1]. Of this, single-crystal solar cells account for half of the share. Laboratory cells have demonstrated 25% efficiency; however, commercial cells have efficiencies of 16% - 20% resulting from a focus on implementation processes geared to rapid throughput and low cost, thereby reducing the energy pay-back time. An example would be the use of metal pastes which dissolve the dielectric during the firing process as opposed to lithographically defined contacts. With current trends of single-crystal silicon photovoltaic (PV) module prices down to *$0.60/W,* almost all other PV technologies are challenged to remain cost competitive. This presents a unique opportunity in revisiting the PV cell fabrication process and incorporating moderately more expensive IC process practices into PV manufacturing. While they may drive the cost toward a *$1/W* benchmark, there is substantial room to "experiment", leading to higher efficiencies which will help maintain the overall system cost.

This work entails a turn-key process designed to provide a platform for rapid evaluation of novel materials and processes. A two-step lithographic process yielding a baseline 11% - 13% efficient cell is described. Results of three studies have shown improvements in solar cell output parameters due to the inclusion of a back-surface field implant, a higher emitter doping and also an additional RCA Clean.

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CHAPTER 1: INTRODUCTION

Sunlight is an essential source of the earth's energy needs and solar technology provides an important renewable alternative source for energy generation. This has been possible because of the comparatively low manufacturing costs associated with photovoltaics (PV). It is often economically feasible and the best form of energy to provide power to places where other sources of energy (wind, thermal or water) are not an option. Much of photovoltaic technology's success may be attributed to its relatively early discovery in the *1950's* and its development that parallels the semiconductor industry.

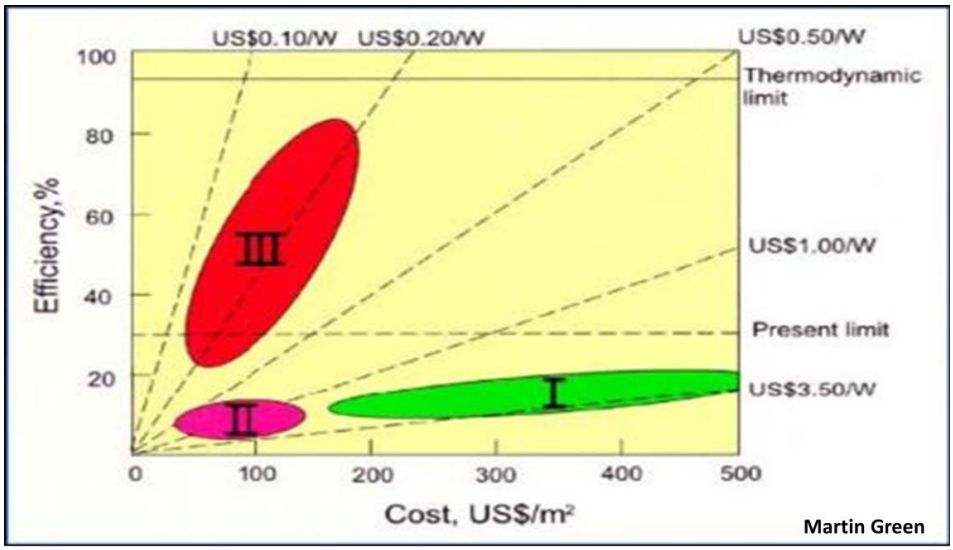


Figure 1: Cost/Efficiency of Photovoltaic Technology [2]

Figure 1 shows the famous graph by Martin A. Green grouping the solar technologies by their generation and comparing their efficiencies with cost. The classification of solar technologies starts with the first generation solar cells which refers to the single-crystal silicon and gallium-arsenide (*GaAs*) devices. This is the technology which is most mature because of its early invention and parallel development with the microelectronic industry. The abundance, material non-toxicity,

as well as the inexpensiveness have made the silicon-based technology a favorable one for terrestrial applications while GaAs cells are preferred for space applications.

The second generation cells, also known as thin-film solar cells, include devices made by chemical vapor deposition of thin-film materials such as Cadmium Telluride (CdTe), Copper-Indium-Gallium-Selenide (CIGS), as well as amorphous silicon (a-Si). CdTe inherently has a high absorption coefficient and its bandgap of 1.45 *eV* is near to optimum to harness incident radiation. A stoichiometric composition of CdTe can be formed using the evaporation process and 16.7% power conversion efficiencies have been reported [3]. Cadmium toxicity and tellurium availability poses a major challenge to the large-scale CdTe solar cell manufacturing. Another contender, Copper-Indium-Gallium-Selenide (CIGS) have made recent improvements to reach the power conversion efficiency of 19.6% [3]. CIGS fabrication involves co-evaporation process (alternate copper-rich and copper-poor conditions and graded Ga/In profiles), metal selenization process (metals are sputtered and then converted to CIGS through annealing in chalcogen ambient and solution processing (application of a coating followed by high temperature annealing). However, there are still challenges with regards to the process like usage of large glass substrates for high temperature processing, excessive use of relatively unreactive selenium, and potential contamination due to the non-vacuum technologies (solution processing). Hydrogenated amorphous silicon (a-Si:H) is another technology that has exceeded 10% efficiency with *p-i-n* configuration. This technology aligned very well with the IC industry and holds the advantage of low temperature processing, a-Si solar cells were a successful thin-film technology compared to others. However, this type of device suffered from light-induced degradation known as the Staebler-Wronksi effect [4].

The third generation solar cell includes *III-V* compounds like Gallium-Arsenide fabricated to form hetero-junction and stacked-junction devices. These devices are higher in efficiency, but more expensive than other generations. While their application is most promising for space, inherent material properties, toxicity, availability and complex processing marks major obstacles for their use in terrestrial applications.

Another classification of PV technology includes Organic solar cells (OPV) and dye-sensitized solar cells (*DSC*). These device technologies own the advantage of not having significant material constraints and have exhibited efficiencies at 8.3% and 10.4% respectively [3]. While these devices can be fabricated on flexible substrates and are useful for portable electronics, the physical and mechanical stability of these types of cells is a concern along with realizing high module level efficiencies.

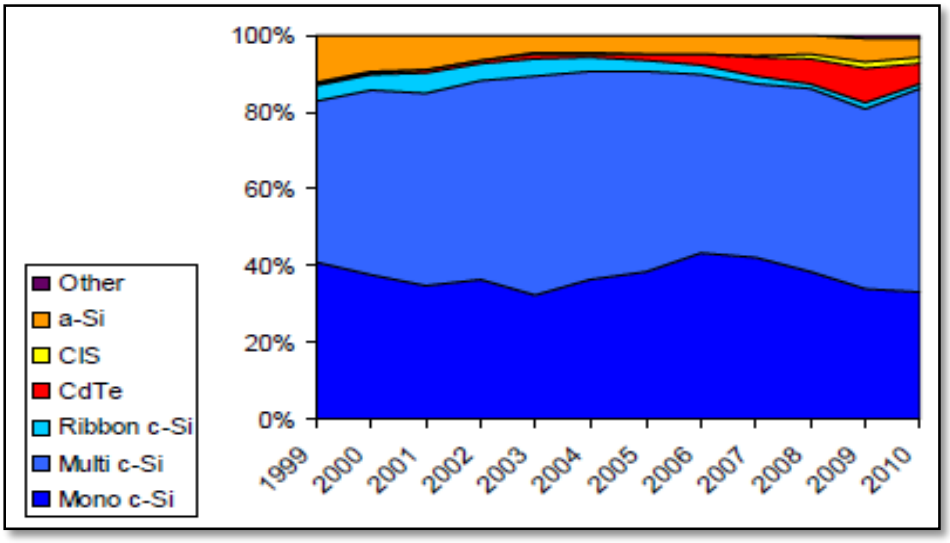


Figure 2: Market Share of Different PV technologies [5]

Figure 2 shows the market share of different photovoltaic technologies over the last decade and the market share have been growing at an average rate of more than 40% [5]. Well established silicon solar cell technologies have benefited from this growth capturing around 85% of the photovoltaic market [5]. The reasons for the dominance of silicon technology are its abundance, non-toxicity, the high energy-conversion efficiency amongst other single junction PV technologies, improved energy pay-back time and long-term stability. Moreover, a constant ability to realize further reductions with regards to material and manufacturing costs have made crystalline silicon the leader in the current PV market. A trade-off between the use of advanced materials, manufacturing equipment and higher energy-conversion efficiencies is worth investigating since sufficient gains can offset the added investment.

To sustain development with regards to manufacturing and competitiveness, the photovoltaic industry banks on two crucial aspects. One is increasing the energy-conversion efficiency of a solar cell and the other is to lower the manufacturing cost. Once these two aspects are simultaneously achieved, photovoltaic energy production would be poised to reach parity with the conventional electricity generation technologies. Multi-crystalline silicon solar cells have played an important role in the success of silicon technology because of low polysilicon prices blended with modestly high efficiencies and improvements in the wire-cutting technology leading to reduced thickness wafers, thus reducing the cost of the silicon materials. At the time of this work, module prices were down to *$0.60/W*.

Techniques employed in the IC industry produce high purity electronic grade silicon. To realize high purity, silica is first reduced with coke in a high-temperature environment to produce 98% pure metallurgical grade silicon. To further purify the polysilicon feedstock, energy intensive Siemens process [6] is widely used, which involves production and distillation of trichlorosilane

(TCS). A high temperature (1150 ^{0}C) processing step involving the hydrogenation of TCS, with HCL as a catalyst, serves to activate polysilicon growth over the surface of silicon rods that are placed inside Siemens reactors. After growth, the rods are broken to produce chunks of polysilcon.

Another technique that produces granules of polysilicon is the Fluidized bed reactor (*FBR*) process which involves fluidizing small crystalline silicon seed particles in a cone-shaped vessel, suspended by an upward-flowing fluidizing gas (hydrogen). Once the decomposition temperature of silane is reached, purified crystalline silicon layer builds up and reaches a size which forces the silicon granules fall to the bottom of the cone where they are collected. This process is efficient with regards to the use of reactant gases as well as energy consumption. Another significant advantage in the following step of melting the polysilicon is that the FBR granules can be continuously fed in the Czochralski pullers to bear up to three daughter ingots versus having to load polysilicon chunks in single batch processing. Some technical challenges with heating the fluidized beds have limited the capability of providing FBR materials.

Improvements in the wire-saw technology are producing 180 μm thick wafers, allowing more wafers per unit volume. However while the Kerf produced during wafer sawing could be recycled, eliminating the waste is more desirable. Two new technologies, edge-defined film-fed growth (*EFG*) and string ribbon silicon technology are capable to produce 100 *mm* wide 300 μm thick wafers eliminating the wire-saw method [5]. Kerfless wafers, or even ultra-thin silicon ribbons, are being developed for the manufacturing of solar cells. Initial investments on realizing these process improvements did add to the cost, but improved power conversion efficiencies and process improvements have helped offset the initial investment.

Another method that was considered is an ultra-thin silicon (ut-Si) technology where the absorbing silicon layer was 5-50 μm thick [5]. A few strategies employed were heteroepitaxial growth followed by lift-off, depositing amorphous silicon followed by thermal recrystallization, peeling ut-Si layers off of silicon ingot using stress-induced lift-off. Mechanical handling of the wafers yet maintaining high throughput and low cost is a challenge with ut-Si wafers [5].

To summarize, with the current trends in silicon photovoltaic (PV) technology, module prices are down to *$0.60/W*. Hence other PV technologies are challenged to remain cost competitive. Figure 3 illustrates the revised Martin Green's graph showing the first generation solar cell (efficiency vs. cost) oval moving to the left, surpassing the second generation solar cells in terms of efficiency and being cost competitive.

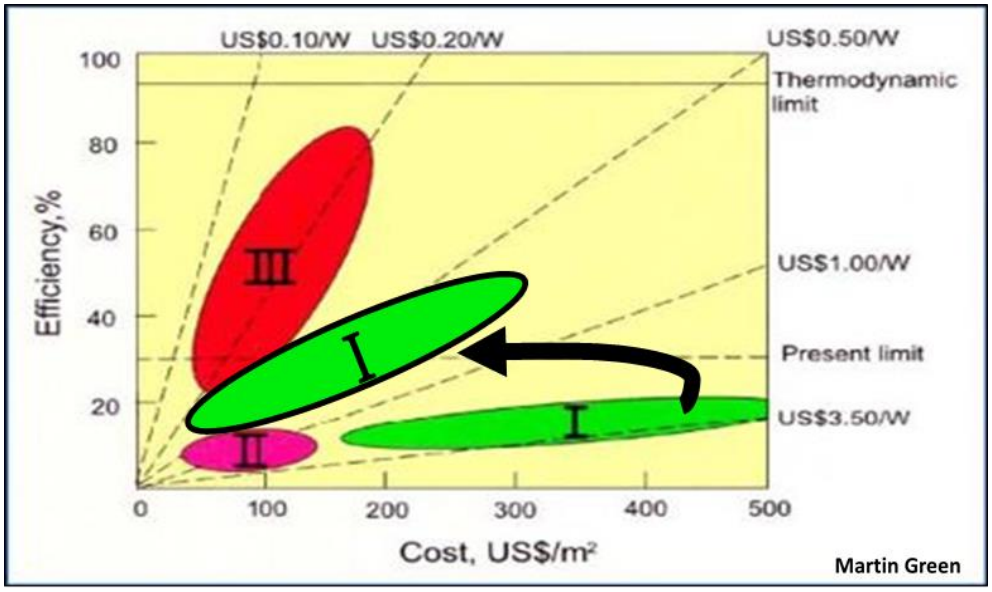


Figure 3: Cost/Efficiency of Photovoltaic Technology [2]

This economic advantage over the second generation solar cells has presented an opportunity for the silicon PV manufacturers to revisit solar cell fabrication process and incorporate moderately more expensive IC process practices into PV manufacturing. With these

processing improvements the cost may again trend upwards, however, there exists substantial room for improvements leading to higher efficiencies which may help maintain the overall system cost and balance the energy pay-back time. So long as the final cost is below the economic benchmark of *$1.00/W* used for PV, the gain in efficiency should outweigh the added cost.

This work focuses on the refinement of a turn-key silicon solar cell process enabling rapid evaluation of novel materials and processes. The basics of solar cells are presented in Chapter 2 to provide key areas of investigation and important performance metrics which will be used to evaluate process changes. Our turn-key process is described in Chapter 3. The results of the experiments performed are presented in Chapter 4. The observations and results are discussed in Chapter 5. Chapter 6 concludes the results of the experiments performed using the turn-key process. Chapter 7 presents future opportunities to the existing turn-key process towards improving the device performance.

CHAPTER 2: SOLAR CELL OVERVIEW

A photovoltaic cell (solar cell) is a device that converts incident solar energy into electrical power. Figure 4 shows a basic cross-section of a solar cell [7]. Fundamentally, the solar cell consists of three basic structural elements. The first element is the absorber material which takes the incoming photons and transfers their energy to its valence electrons leading them to an excited state. Semiconductors are typically used as the absorbing material which utilizes incident light to generate free electron hole pairs that are available for conduction. The second element is a *p-n* junction which may be a combination of an *n-type* (emitter) and a *p-type* (base) region forming a built-in electric field. The electric field assists in the collection of free carriers. Finally, the third element is the metal grid which can capture electrons that are available for conduction and results in the flow of current in the external circuit. The grid design must be optimized to minimize resistance and shadowing.

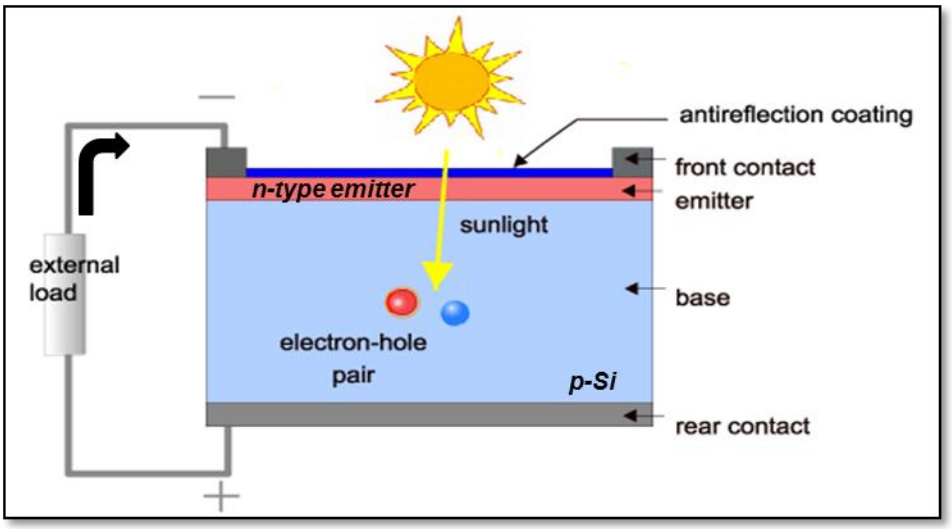


Figure 4: Cross-section of a basic solar cell [7]

2.1 Incident Spectrum

The radiant power per unit area perpendicular to the direction of the sun at the mean earth-sun distance is referred to as the solar constant [8]. Figure 5 depicts the solar radiation as a function of wavelength. The spectrum outside the Earth's atmosphere is called Air Mass 0 and is labelled as AM0 radiation. This particular spectrum is used as an incident spectrum to measure efficiencies of solar cells for space applications. The spectrum incident upon the earth surface is further attenuated by at least 30% [8] and is marked as AM1.5 radiation. The causes for such attenuation are the scattering of light by the molecules, dust particles in the atmosphere and absorption of light by atmospheric gases.

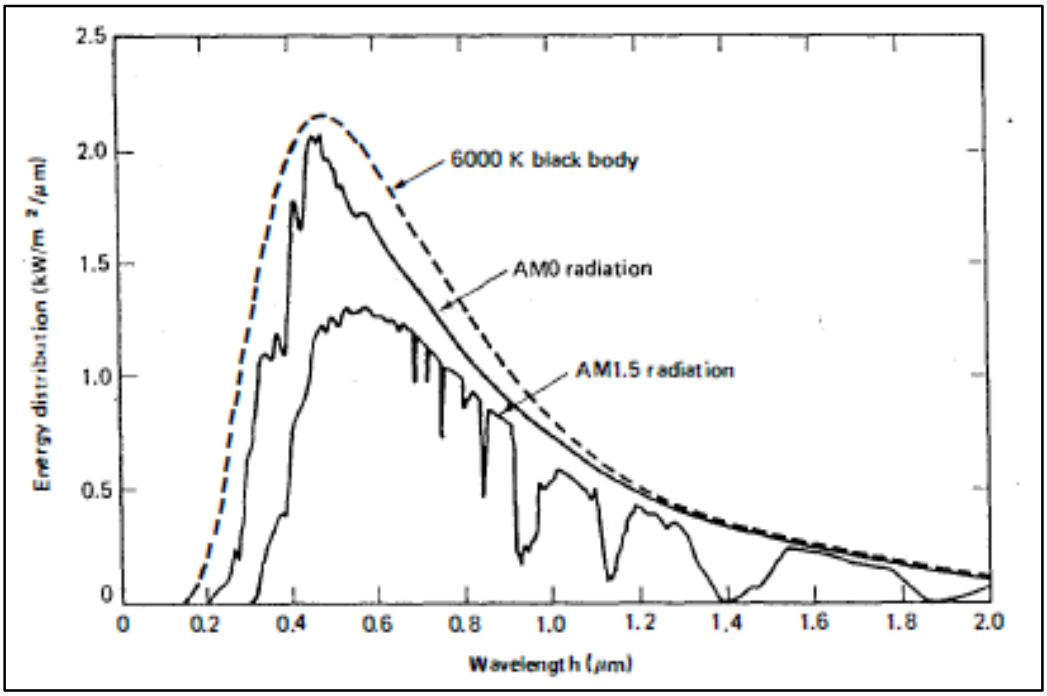


Figure 5: Spectral radiation of sunlight showing AM0, AM1.5 and black body radiation at 6000K [8]

The attenuation throughout the range of wavelength for AM1.5 radiation is highly variable. The air mass quantifies the reduction in the light intensity as it passes through the atmosphere and

is absorbed by dust particles or the gases in the atmosphere. Because the path length through the atmosphere is a function of the sun's position in the sky relative to the cell, the air mass is the ratio of any actual path length to the shortest possible path length (when sun is directly overhead) and it can be expressed as

$$Air\ Mass = \frac{1}{\cos\theta} \tag{1}$$

where θ is the zenith angle. When the sun is directly overhead the air mass is unity and the radiation is described as air mass one (AM1) radiation spectrum. The AM1.5 radiation spectrum corresponds to an average zenith angle of θ equals 48.2°.

Figure 6 illustrated an alternative way to estimate the air mass is by measuring the height *h* of the structure and the length *s* of the shadow of the object [7], and can be expressed as,

$$\text{Air Mass} = \sqrt{1 + \left(\frac{s}{h}\right)^2} \tag{2}$$

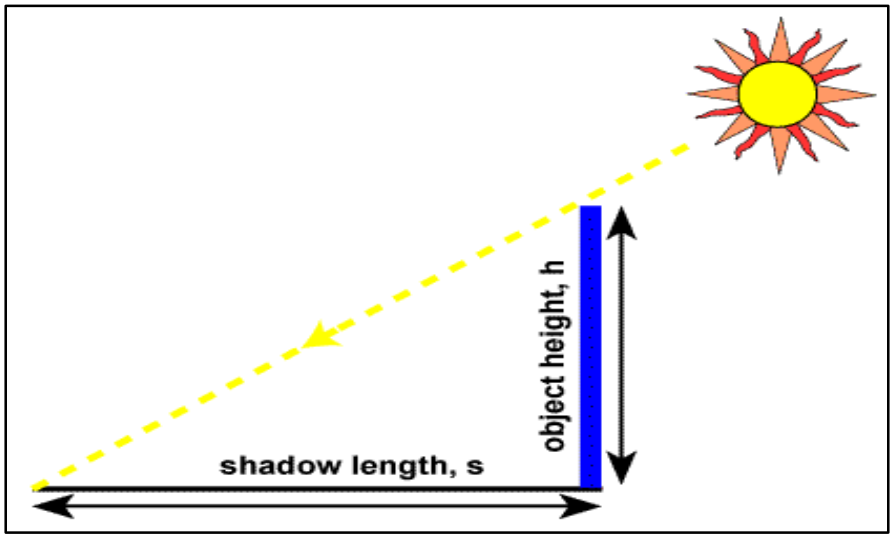


Figure 6: Calculating Air Mass with vertical height *h* and shadow length *s* [7]

2.2 Generation and Recombination

The light incident on the solar cell needs to be effectively absorbed. The incoming photons can be transmitted, absorbed, or reflected from the top surface. However, absorption of the incident photon is a characteristic of the material and is measured by the absorption coefficient of the material. Figure 7 shows the absorption coefficients of several semiconducting materials versus the wavelength. Silicon has a lower absorption coefficient as compared to other semiconducting materials like Gallium-Arsenide (GaAs) and Germanium (Ge). Hence the light with lower energy or longer wavelength travels a few hundred microns deep into the silicon substrate before it gets absorbed. Conversely, the lower energy light travels a relatively shorter distance before it gets absorbed in materials like GaAs and Germanium.

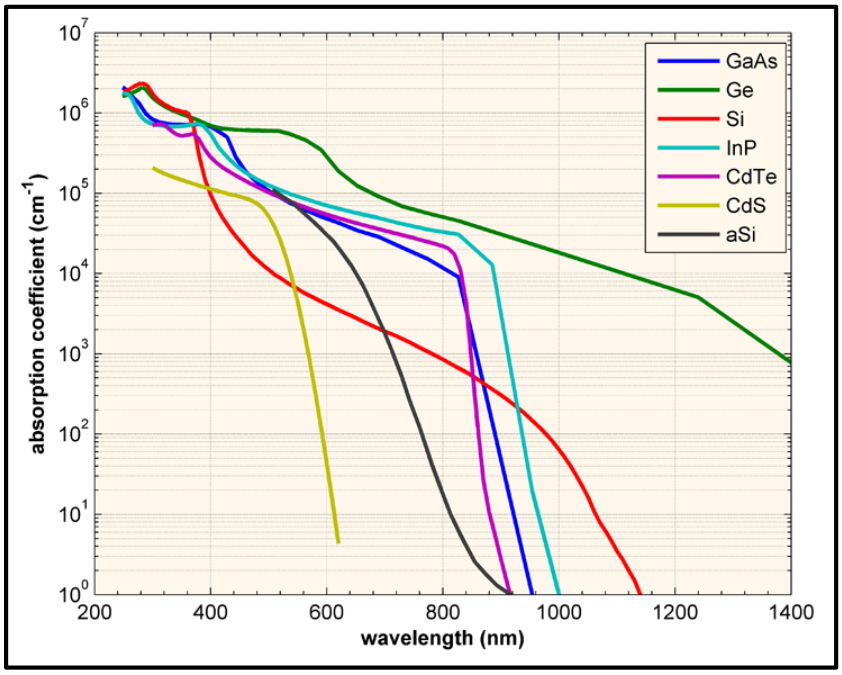


Figure 7: Graph showing absorption coefficient of various semiconductors [7]

Generation of carriers is only part of the phenomenon as these carriers must then be collected. Figure 8 shows a generic collection probability curve and generation rate versus distance

into the substrate. The collection probability approaches unity within the depletion region because of the presence of the built-in electric field that sweeps the minority carriers in the majority carrier region and then decays exponentially as it trends away from the depletion region since the effect of the built-in field decreases and recombination events are higher.

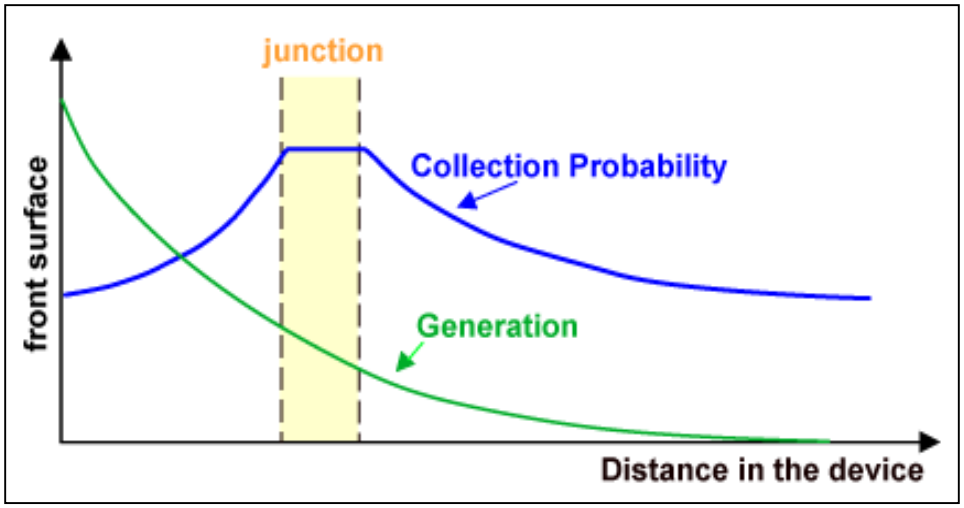


Figure 8: Graph showing collection probability and carrier generation [7]

The generation rate decays exponentially with thickness of the substrate because the energy of the photons with longer wavelength is low to effectively transfer their kinetic energy and generate an electron hole pair. The generation rate *G(λ, x)* can be expressed as,

$$G(\lambda, x) = (1 - s) \int F(\lambda, x)\alpha(\lambda) = (1 - s) \int \big(1 - R(\lambda)\big)F(\lambda, x)e^{-\alpha(\lambda)x}\alpha(\lambda)\,.\,d\lambda \qquad (3)$$

where *s* is the shadowing factor of the grid, *F(λ, x)* being the incident photon flux, the absorption coefficient α is a function of wavelength λ, and *R(λ)* is the reflection coefficient [9].

High energy photons (shorter wavelength) generate electron-hole pairs within a few hundred nanometers from the surface whereas the photons with longer wavelengths travel several microns into the substrate to generate the excess carriers. In both cases, the light generated charge

carriers need to travel some distance in the substrate before they reach the depletion region and are collected. The average distance traveled by a charge carrier from its point of generation before it recombines is known as the minority carrier diffusion length (L) and depends on the quality of the semiconductor material. The diffusion length is a function of the diffusion coefficient (D) and the lifetime of minority charge carriers (τ) and directly impacts the recombination rate. Heavily doped (emitter) regions have a shorter lifetime, which results in high recombination rates, whereas the regions with relatively low doping concentration (substrate) have a longer lifetime and hence a relatively longer diffusion length. Figure 9 gives an empirical fit to the lifetime and the diffusion length of minority charge carriers [10].

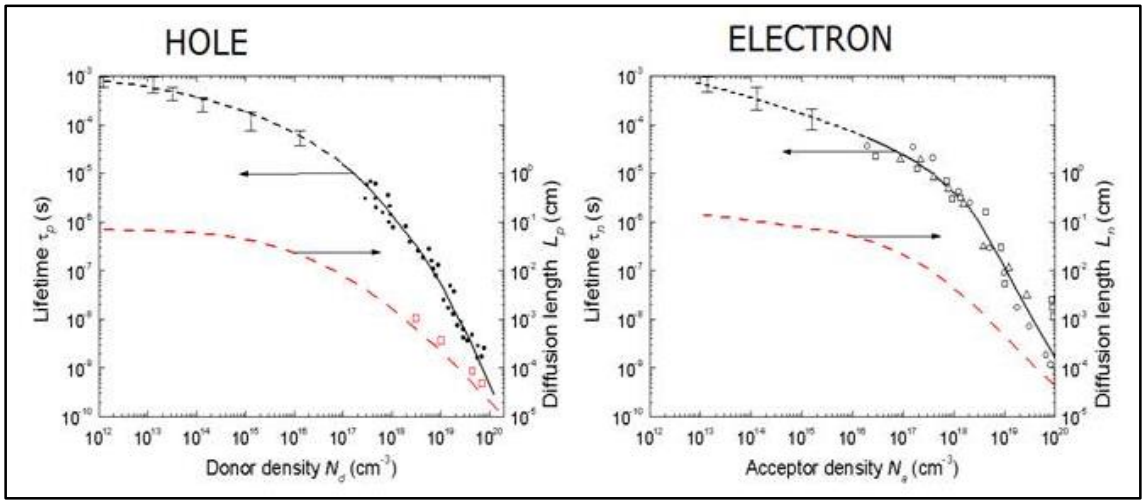


Figure 9: Empirical fit of minority carrier lifetime, diffusion length with doping [10]

A shallower junction is required to maximize the overlap integral of the generation rate and the collection probability resulting in effective collection of the charge carriers, as depicted in Figure 8. The surface needs to be well passivated to minimize any dangling bonds that might assist the recombination process and result in loss of photon generated carriers. For silicon-based solar cells, thicker substrates (example: 550 μm for 4" substrate) present a challenge in that minority charge carriers must travel through the bulk to contribute to current. A *p-type* starting substrate

was used since electrons (minority charge carriers) hold an advantage with a better diffusion length and high mobility, as opposed to holes (minority charge carriers) in an *n-type* starting substrate. However, with current improvements in the wire-saw technology, 180 μm thick substrates are commonly used creating an option to use either n-type or p-type as the starting substrate since the diffusion length can be much longer than the thickness of the substrate.

2.3 Current in a Solar Cell

The current in a solar cell depends on various parameters, among them substrate doping, choice and thickness of anti-reflective coating (ARC), surface passivation, emitter sheet resistance, and junction depth. A synopsis of the diode current derivations is provided below, with a focus on the effects of series and shunt resistances. Parameters, such as the ARC and surface passivation were not the focus of this work.

To mathematically derive current in a solar cell, Poisson's equation must be solved [11]. The general form can be written as:

$$\nabla \cdot \vec{E} = \frac{q}{\varepsilon}(p + N_D^+ - n - N_A^-) \tag{4}$$

where $\vec{E}$ is the electric field measured in *V/cm*, ε represents the permittivity of the material, q is the electron charge, *p* and *n* are the free hole and electron concentrations in the substrate, with N_A^- and N_D^+ being the ionized acceptors and donors, respectively.

The continuity equation is used to define the change with time of the charge carriers and can be expressed as follows:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\left(\nabla \cdot \overrightarrow{J_n}\right) - (R_n - G) \tag{5}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\left(\nabla \cdot \overrightarrow{J_p}\right) - \left(R_p - G\right) \tag{6}$$

where $\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ are the electron and hole current densities measured in *A/cm*^{2}, respectively. R_n and R_p are the electron and hole thermal recombination rate, respectively and G is the optical generation rate. The left-hand-side of the above equations denotes the time varying concentrations which are zero in a steady state condition. Hence the above equations can be written as:

$$\nabla \cdot \overrightarrow{J_n} = q(R_n - G) \tag{7}$$

$$\nabla \cdot \overrightarrow{J_p} = -q\left(R_p - G\right) \tag{8}$$

The current transport equations comprised of the diffusion current which is due to any concentration gradient and the drift current which is influenced by the electric field, can be expressed as:

$$J_n = q\mu_n n\vec{E} + qD_n \frac{\partial n}{\partial x} \tag{9}$$

$$J_p = q\mu_p p\vec{E} - qD_p \frac{\partial p}{\partial x} \tag{10}$$

Assumptions are made including one-dimensional device structure, the depletion approximation; the electric field is present only in the depletion and not the quasi neutral regions (*QNR's*). Also assumed are low-level injection with uniform doping and a steady state condition.

$$\nabla \cdot \overrightarrow{J_n} = q\mu_n \frac{d(n\overrightarrow{E})}{dx} + qD_n \frac{d^2\Delta n}{dx^2} = q(R_n - G) \tag{11}$$

$$\nabla \cdot \overrightarrow{J_p} = q\mu_p \frac{d(p\overrightarrow{E})}{dx} - qD_p \frac{d^2\Delta p}{dx^2} = -q\left(R_p - G\right) \tag{12}$$

Δn and Δp are the excess minority carrier concentrations which can be defined as $\Delta n = n - n_0$, in a p-type material and $\Delta p = p - p_0$, in an n-type material.

The general form of the recombination rate R, given by Shockley Read Hall equation [3] is:

$$R = \frac{(np - n_i)^2}{\tau_{p0}(n + n_1) + \tau_{n0}(p + p_1)} \tag{13}$$

where τ_{p0} and τ_{n0} are the minority carrier lifetimes at equilibrium, n_i is the intrinsic carrier concentration and n_1, p_1 are concentration of charge carriers in the recombination sites such that $n >> n_1$ and $p >> p_1$. Considering *p-type* substrate, the hole concentration $p \approx p_0$ and $p >> n$. Applying these conditions and the law of Mass Action ($n_i^2 = n_0 * p_0$) in Equation 13 gives,

$$R_p = \frac{\Delta n}{\tau_n}; \quad R_n = \frac{\Delta p}{\tau_p} \tag{14}$$

Assuming no electric field in the quasi neutral regions and also considering low level injection, Equations 11 and 12 can be rewritten using Equation 14 as:

$$D_n \frac{d^2 \Delta n}{dx^2} - \frac{\Delta p}{\tau_p} = -G \tag{15}$$

$$D_p \frac{d^2 \Delta p}{dx^2} - \frac{\Delta n}{\tau_n} = -G \tag{16}$$

The current in quasi neutral regions that has diffusion components due to the minority carriers, and the hole diffusion current density on the n-side may be written as:

$$J_{pn} = -qD_p \frac{dp}{dx} = -qD_p \frac{d\Delta p}{dx} = \frac{qD_p}{L_p} p_{n0} \left\{ exp\left(\frac{qV_{app}}{kT}\right) - 1 \right\} \tag{17}$$

where V_{app} is the applied voltage.

The expression for excess charge carriers (Δp) in Equation 17 can be found by solving the general solution along with the boundary conditions for a long base diode under no application of light. V_{app} is the applied voltage. The same can be repeated to derive an expression for electron diffusion current density on the p-side of the device which can be expressed as:

$$J_{np} = qn\frac{dn}{dx} = qn\frac{d\Delta n}{dx} = \frac{qD_n}{L_n}n_{p0}\left\{exp\left(\frac{qV_{app}}{kT}\right) - 1\right\} \tag{18}$$

The total diffusion current density (J_{total}) under the application of a forwards bias (V_{app}) is given by the summation of Equations 17 and 18.

$$J_{total} = J_{pn} + J_{np} = \left(\frac{qD_p p_{n0}}{L_p} + \frac{qD_n n_{p0}}{L_n}\right)\left\{exp\left(\frac{qV_{app}}{kT}\right) - 1\right\} \tag{19}$$

A simple expression for a diode with cross-sectional area A in a more representative form may be written as:

$$I_{total} = I_{01}\left\{exp\left(\frac{qV_{app}}{nkT}\right) - 1\right\} \tag{20}$$

where n is the ideality factor (ideally n=1) and I_{01} is the saturation current density, and is equal to

$$I_{01} = A\left(\frac{qD_p n_i^2}{L_p N_D} + \frac{qD_n n_i^2}{L_n N_A}\right) \tag{21}$$

Under applied bias, the total concentration of carriers at the metallurgical junction of the p-n junction of width W must to be considered. The carrier concentrations can be written as:

$$n = p = n_i\left[exp\left(\frac{qV_{app}}{2kT}\right) - 1\right] \tag{22}$$

Hence the total current due to the generation and recombination, $I_{R/G}$, under the application of a forward bias can be written as:

$$I_{R/G} = I_{02}\left\{exp\left(\frac{qV_{app}}{kT}\right) - 1\right\} \tag{23}$$

where I_{o2} is the saturation current density depending on the average lifetimes (τ_0) of the carriers in the depletion region and is defined as:

$$I_{02} = \frac{qn_iAW}{2\tau_0} \tag{23}$$

The total illuminated diode current can be expressed as a sum of Equations 20 and 23.

$$I_{total} = I_{01}\left[exp\left(\frac{qV_{app}}{1kT}\right) - 1\right] + I_{02}\left[exp\left(\frac{qV_{app}}{2kT}\right) - 1\right] - I_{ph} \tag{24}$$

where I_{ph} is the photon generated current which can be calculated to be

$$I_{ph} = -qAG\left(L_p + L_n\right) \tag{25}$$

where A is cell area and G is generation rate which is a function of photon absorption, reflectivity of top surface, and grid shading.

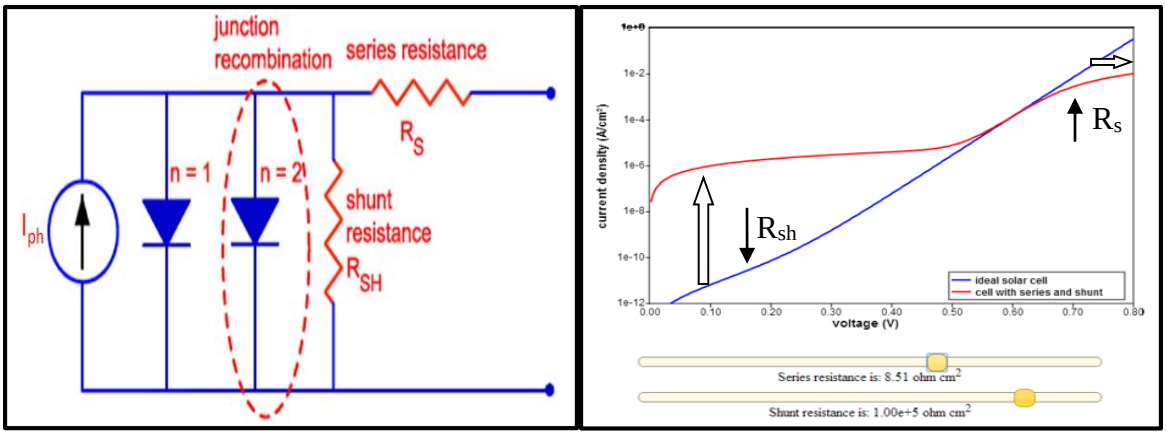


Figure 10: (a) Solar cell double diode model [8] (b) Effect of R_s and R_{sh} on dark *IV* response [7]

Figure 10 (a) illustrates the double diode equivalent circuit model of a solar cell. The parasitic parameters that limit the performance of the solar cell are the junction recombination, the shunt and the series resistances.

Figure 10 (b) illustrates the effect of parasitic resistance on the dark *I-V* response. At low voltages, the shunt resistance dominates the device performance. Lower shunt resistance values indicate higher recombination events occurring at the junction leading to higher saturation current density (and n_2 value) leading to poor device performance. The effect of the parasitic series resistances is high at higher voltages. The dark *I-V* curve starts to bend at higher values of series resistance, signifying less current is supplied to the load.

2.4 Output Parameters

The fabricated solar cells were characterized for important output parameters such as short-circuit current, open-circuit voltage, maximum output power, Fill Factor (FF) and the energy-conversion efficiency. These parameters can be extracted from *I-V* curves when the solar cell is subjected to illumination. Other parameters such as series and shunt resistances, ideality factors and saturation current densities can also be extracted from I_{sc}-V_{oc} curves and dark *I-V* curves. These parameters do not directly relate as output parameters but are crucial in identifying the causes of degradation in the cell performance.

Illuminated *I-V* curves are measured under a standard incident spectrum (AM1.5 for terrestrial applications). Figure 11 shows an illuminated *I-V* curve and a Power curve along with

the output parameters of the solar cell. When the output terminals are short-circuited, the maximum current that can flow through the output terminals is the short-circuit current (I_{sc}) of the solar cell and is expressed as shown in Equation 24. Ideally, the photon current (I_{ph}) is equal to I_{sc}, but non-idealities such as parasitic resistances and diode leakage current reduce the output current from its maximum value.

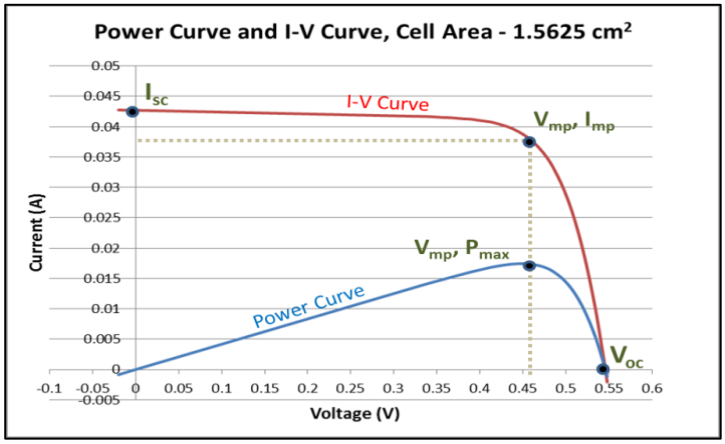


Figure 11: Power and *I-V* curve with output parameters

The maximum voltage that can be measured across the solar cell with no current flowing through the output terminals is the open-circuit voltage (V_{oc}) of the device. The expression for V_{oc} can be determined by setting left-hand side of Equation 24 to zero and combining the saturation current density as I_0 for a single diode based model.

$$V_{oc} = \frac{nKT}{q} ln\left(\frac{I_{ph}}{I_0} + 1\right) \tag{26}$$

V_{oc} is influenced by the properties of the semiconductor material by virtue of its dependence on I_0. I_0 depends on the intrinsic carrier concentration and hence the band-gap of the material. It also depends on L and hence τ_{min} which makes V_{oc} strongly dependent on the material

properties. The maximum power that can be delivered is given by the maximum power points V_{mp} and I_{mp}.

Another parameter that determines the performance of the device is the Fill Factor (FF). It is a measure of the "squareness" of the *I-V* curve of a solar cell. It can be expressed as the ratio of the product of V_{oc} and I_{sc} to the product of V_{mp} and I_{mp} as shown in Equation 27.

$$FF = \frac{V_{mp} I_{mp}}{V_{oc} I_{sc}} \tag{27}$$

FF has a strong dependence on the open-circuit voltage. Another method that can be used to determine FF is by defining a normalized voltage, v_{oc} as qV_{oc}/KT. This empirical relationship is given as [7],

$$FF = \frac{v_{oc} - \ln(v_{oc} + 0.72)}{(v_{oc} + 1)} \tag{28}$$

Finally, the energy-conversion efficiency, η, can be calculated as the ratio of the maximum output power to the incident power (P_{in}) on the solar cell.

$$\eta = \frac{V_{oc} I_{sc} FF}{P_{in}} \tag{29}$$

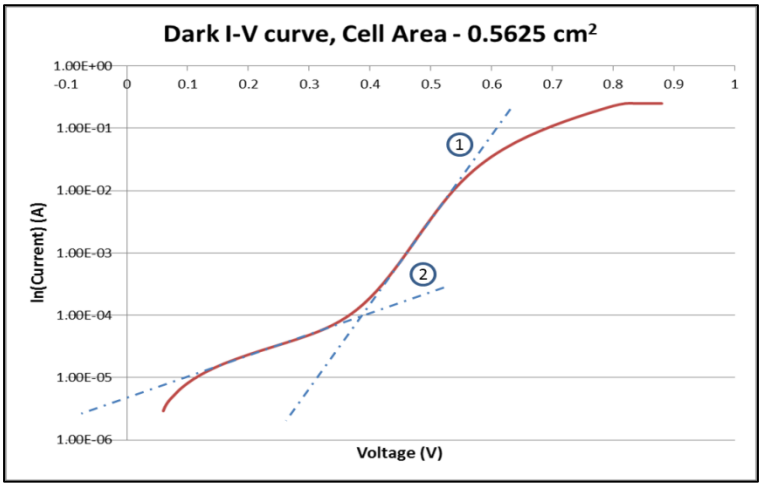


Figure 12: Sample semilog plot of *I-V* curve in dark

I-V curves measured with no illumination gives information about the non-idealities that affect the device performance and the diode properties are examined via this curve. The carriers are injected into the diode sweeping the voltage from 0.1 *V* to 0.9 *V*. The current is measured at every voltage point and *I-V* curve is plotted on a semi-logarithmic (semilog) scale. Figure 12 shows a sample dark *I-V* curve plotted on semilog scale. The ideality factor for various regions on the curve can be found by calculating the slopes of the two lines labeled 1 and 2. Ideality factor from line 1 (n_1) gives information about the recombination events in the quasi neutral regions whereas the line 2 (n_2) provides information about the recombination events occurring in the depletion region.

2.5 Experiment Design Parameters:

To maximize absorption of the incident photons, one of the parameters that must be controlled is the front surface reflectance of the cell. Anti-reflection coatings (ARC) are chosen to minimize the reflection of incident photons from the surface. Other surface optimization techniques such as surface texturing may be employed to enhance controlled reflection which

increases the probability of the photon getting absorbed and contributes towards the carrier collection efficiency.

A thin layer of dielectric material is used as an ARC with an effective thickness to minimize reflection from the front surface of the cell. The incident and the reflected wave should interfere destructively allowing most of the light to transmit into the semiconductor where electron-hole pairs can be generated creating current. The optimum refractive index for the ARC film to provide minimum reflection can be calculated as,

$$n_f = \sqrt{n_1 n_2} \tag{26}$$

where n_f is the refractive index of the film, n_1 is the refractive index of medium 1 (air) and n_2 is the refractive index of medium 2 (silicon). Substituting the values of n_1 as 1 and n_2 as 3.85, the optimum refractive index of the anti-reflective film calculates to be 1.96. Silicon nitride with refractive index very close to 1.96 is commonly used in industrial applications. For research purposes, silicon dioxide can also be used with a chosen thickness as an effective ARC.

The thickness of the ARC is chosen such that the wavelength in the ARC is one quarter of the wavelength of the incoming wave in free space. Hence for a film with refractive index n_f, the effective thickness, t can be calculated as:

$$t = \frac{\lambda}{4n_f} \tag{27}$$

The dielectric material (ARC) is also advantageous since it passivates the surface. The dangling bonds on the top surface of the cell act as recombination sites and reduce the lifetime of minority carriers, reducing the total number of charge carriers available for conduction. Because

the generation of the charge carriers is maximum near the surface, a well passivated surface will benefit current collected in the device by reducing the front surface recombination velocity.

The back-surface recombination is also an important parameter that affects the short-circuit current and the open-circuit voltage. With high back-surface recombination, the lifetime of the charge carriers decreases, leading to a poorer solar response. In addition to passivating the back surface, a back surface field (BSF) can be created such that the minority charge carriers encounter a barrier and are reflected towards the depletion region. Figure 13 shows the band diagram with the inclusion of back-surface field.

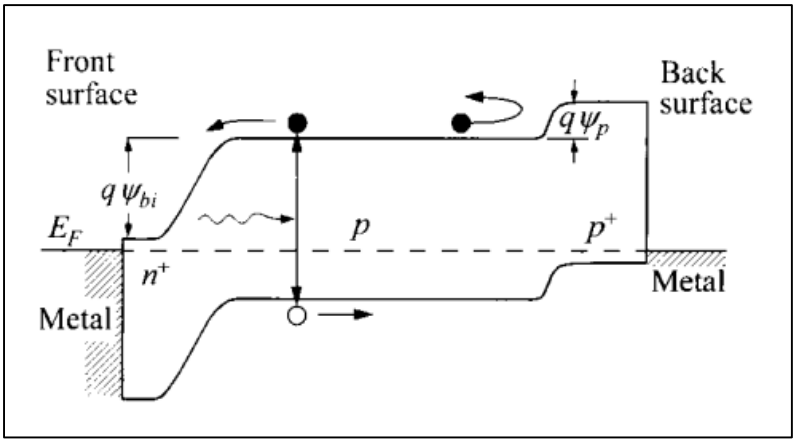


Figure 13: Energy band diagram showing advantages of BSF [9]

To implement the BSF, a higher doping region with similar base species needs to be formed. Due to the high and low doping of the same species, there exists a band bending (junction) which inhibits the minority carrier being lost at the back of the cell. The minority charge carriers in the base are reflected by the barrier created by BSF ($q\psi_p$). The reflected carriers are forced to diffuse through the base towards the depletion region where they can be swept away by the built-in electric field towards the majority carrier region contributing to photon-assisted current. Hence, BSF increases both the short-circuit current, as well as the open-circuit voltage, due to band-

bending. An added advantage with the BSF is forming a better ohmic contact with the metal thereby reducing contact resistance.

The process improvements including surface texturing, anti-reflective coating and back-surface field all boosts the solar cell performance. However, to manufacture these devices, requires a higher number of masking steps as well as complex fabrication techniques which increase the manufacturing complexity and cost. Figure 14 (a) depicts the Passivated Emitter Rear Locally diffused (PERL) solar cell structure developed by the University of New South Wales in Australia, which has achieved the highest efficiency (25%) for single-crystal silicon solar cells.

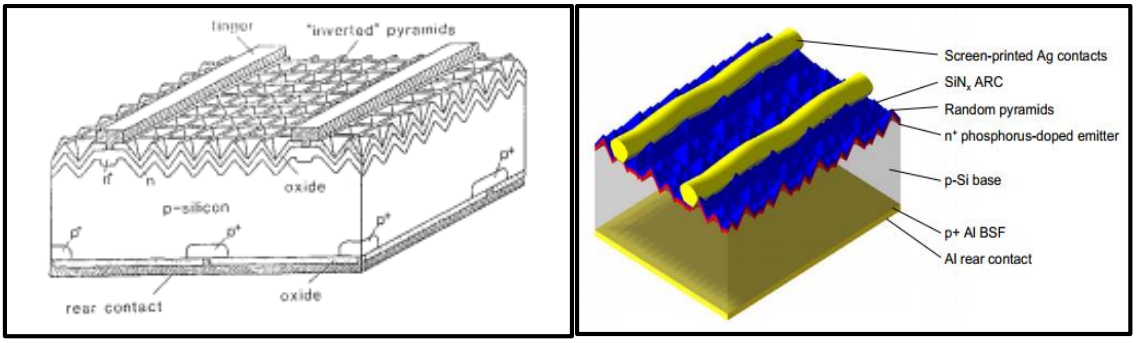


Figure 14: (a) Passivated Emitter Rear Locally diffused (PERL) solar cell structure [12], (b) Aluminum-BSF (Al-BSF) industrial solar cell [1]

The PERL cell fabrication involves complex processing including lithographically defined surface texturing and contacts, rear locally diffused contacts defined using another lithography step, and use of Titanium-Palladium-Silver (Ti-Pd-Ag) as a front metal contact. With these complex fabrication techniques, the PERL cell has exhibited 25% efficiency as compared to the commercial solar cells of 18%-20%.

Figure 14 (b) shows an example of commercial solar cell structure. The Al-BSF industrial solar cell involves cheaper processing techniques like random texturization, screen printed silver contacts which dissolves the dielectric during a firing process, blanket back-side metal deposition

etc. The result is reduced manufacturing cost at the cost of reduced efficiency. Figure 15 shows the basic process flow for fabricating a standard crystalline silicon industrial solar cell.

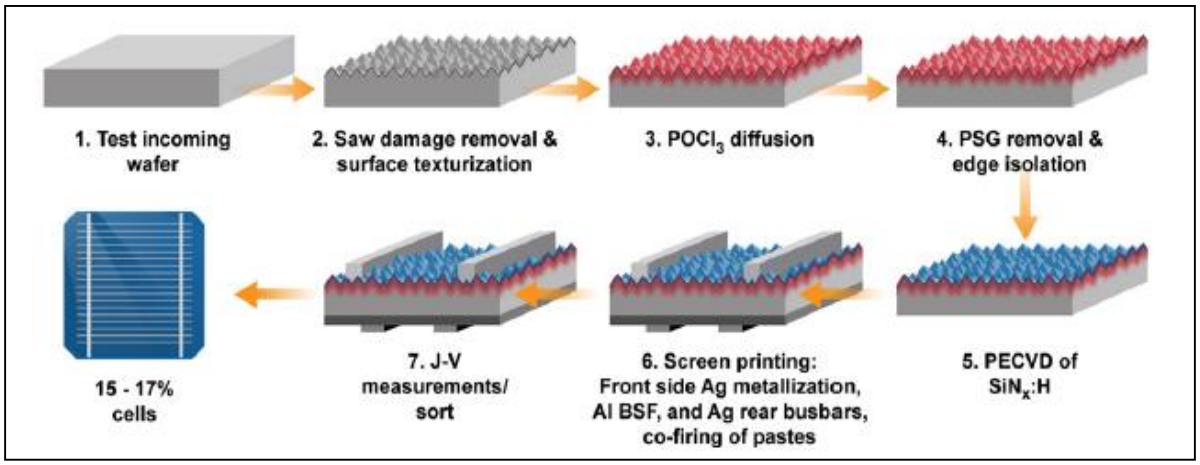


Figure 15: Basic Process Flow for standard c-Si solar cell fabrication [6]

However, with recent successful process improvisations and dropping silicon prices, transitioning from a standard industrial solar cell process toward a PERL cell process is now a viable option. While the cost of these solar panels may approach *$1/W*, the efficiency of the solar should simultaneously increase towards 22%, balancing the overall system cost and improving the energy payback time.

Chapter 3 reviews a turn-key process developed at RIT to minimize the fabrication steps while achieving respectable efficiencies, thus providing a vehicle for rapid evaluation for process innovations. Chapter 4 will report the experiments performed with a few process improvements. Chapter 5 discusses the observations and results obtained from these experiments and Chapter 6 presents the conclusion of the experiments performed using the turn-key process. Chapter 7 will proceed into the recommendations on future opportunities to increase the energy-conversion efficiency.

CHAPTER 3: TURN-KEY SOLAR PROCESS

3.1 General Process Flow

The turn-key process is designed to fabricate solar cells quickly by limiting the process to two photolithography steps. The general flow starts with resistivity measurement of the starting substrate using an automated 4-point probe. RCA (Radio Corporation of America) clean is performed on newly acquired substrates (device grade) to free them of any metal or any organic contaminants that may act as recombination centers. A 5000 *Å* silicon dioxide film, which acts as a field oxide, is thermally grown on the wafer in a steam ambient for 42 minutes at 1000 ^{0}C. Following the oxide growth, first level of lithography is performed to define active area islands.

To perform the first lithography, Hexamethyldisilazane (HMDS) is coated on the wafer and baked at 140 ^{0}C for 1 minute to promote adhesion of photoresist. HPR 504 photoresist is coated and a post application bake at 110 ^{0}C for 1 minute is performed. A contact aligner is used to expose the wafer to image the active area islands for the time calculated by measuring the light intensity and knowing the exposure dose for the resist. A post exposure baked is performed at 100 ^{0}C for 1 minute to eliminate any line edge roughness and standing wave effects before it is developed on the manual developer using CD-26 or Tetramethylammonium hydroxide (TMAH). A post develop bake was performed at 100 ^{0}C for 1 minute.

The next step is to remove the oxide from the front of the wafer where lithographically defined active area islands are formed. A plasma assisted dry-etch was performed to thin down the oxide film from the front while maintaining the oxide on the back. The remaining oxide thickness was measured using a reflectance tool and a timed 5.2:1 Buffered Oxide Etch (BOE) was performed to reach down to bare silicon. Photoresist was stripped in a hot solvent bath and then

the wafers were again RCA cleaned. Following the clean, the wafers were implanted to define the emitter of the device. A typical implant dose of 5 x 10^{15} cm^{-2} of phosphorus (P^{31}) (n-type dopant) is implanted with an energy of 65 *KeV*. Figure 16 shows the cross section of the device post the first lithography and the emitter implant. The simulation for the emitter definition is discussed in the following section.

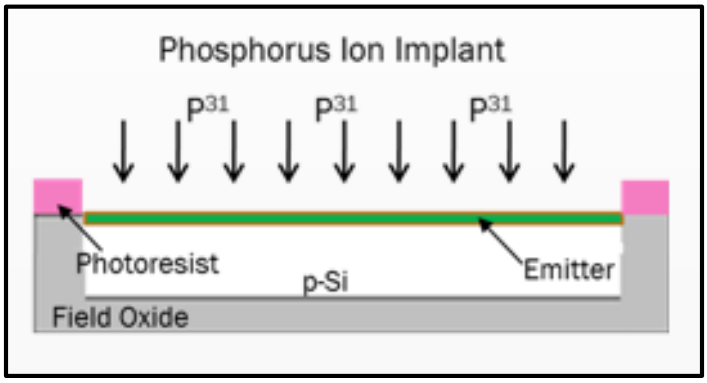


Figure 16: Device cross-section post the first lithography and emitter implant

In the first step of the integrated thermal anneal process; the wafers were processed in the furnace at 925 ^{0}C under Nitrogen ambient for 60 minutes. This is done to re-crystallize the wafer because of the damage done due to implantation. For the second step, the wafers were exposed to a steam ambient at 900 ^{0}C for 12 minutes to grow 950 *Å* silicon dioxide film which was designed to act as an anti-reflective coat (ARC). The third step in the thermal cycle was designed to be at 925 ^{0}C under nitrogen ambient to define the emitter junction depth and passivate the charge levels in the oxide.

A monitor wafer is measured for the thickness of the in-situ grown ARC. The oxide from the monitor wafer is completely etched off using BOE to measure the sheet resistance of the implanted emitter using 4-point probe. Lithography is then performed to define the metal grid on the device wafers using Lift-Off process. The wafers are coated with HMDS and soft baked at

140 ^{0}C for 1 minute. A lift-off resist, AZ-1518, was coated and exposed for a calculated time using the appropriate mask. Manual alignment needs to be done so as to properly place the metal grid in the active area. A post exposure bake is performed at 100 ^{0}C for 1 minute. The wafers are developed using CD-26 developer and a post develop bake is done at 100 ^{0}C for 1 minute. Figure 17 depicts the cross-section of the device post the emitter drive-in, ARC growth and lift-off lithography to define the metal grid.

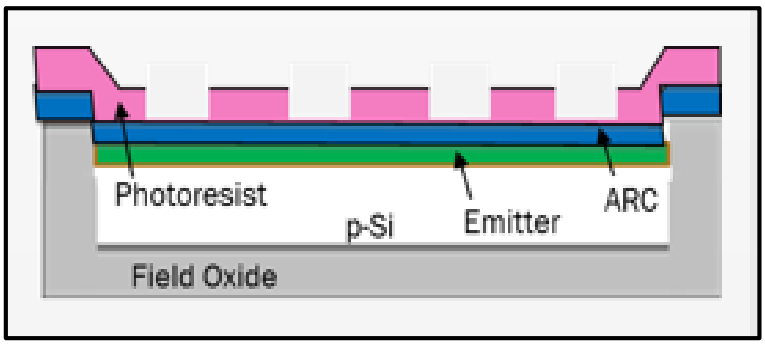


Figure 17: Device cross-section post emitter drive-in, ARC growth and lift-off lithography

To allow direct contact of metal to the silicon, the ARC is been etched off using BOE bath followed by a spin, rinse and dry (SRD) just prior to metal evaporation. Aluminum (Al) was evaporated using resistive heating. Three pellets of 99% Aluminum (1% Silicon, to avoid junction spiking and surface migration issues) were placed in separate tungsten baskets. The target substrates were placed at a distance of 22 *cm* from the metal source. The evaporator was pumped down to a pressure of about 2 x 10^{-6} *Torr* to allow for sufficient mean free path length for aluminum vapors to the reach the wafers. A high current is passed through the tungsten basket to evaporate aluminum on to the wafers. The glass jar is vented and wafers are retrieved.

The metal is lifted-off using acetone to dissolve the resist, which takes about an hour. The wafers are then cleaned using Isopropyl Alcohol (IPA) and SRD. For the rear side metal

evaporation, the front is protected with photoresist and the oxide is etched from the back using BOE. The evaporation of aluminum for the back contact follows the same procedure as mentioned above. After aluminum evaporation has been completed, the photoresist on the front side of the wafers is stripped using acetone, IPA and SRD to complete the cleaning procedure. The final step of the fabrication process is sintering which is performed under the presence of forming gas H_2/N_2. This allows for the passivation of the Al-Si interfaces so as to achieve ohmic contact between the metal (Al) and the semiconductor (Si). Figure 18 shows the final cross-section of the device.

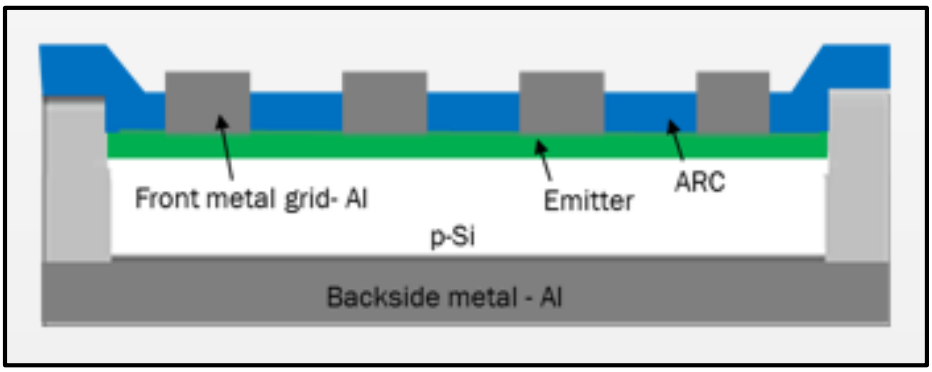


Figure 18: Final device cross-section with front and backside metal contacts

3.2 Revisions for Process Improvement

3.2.1 ARC Thickness Optimization

For minimum reflectivity from the front-surface of the cell, photon management in terms of an anti-reflective coat was implemented. An appropriate ARC thickness was necessary to minimize the reflection. KLA Tencor's Prolith software was used to simulate the optimum ARC thickness. The reflectivity (%) from the top surface of the stack (SiO_2/Si) was be measured for a range of wavelengths (300 *nm* – 1000 *nm*). The optimum ARC (SiO_2) thickness for which minimum reflection was observed was 95 *nm*. Figure 19 illustrates the minimum reflection of incident light using ARC thickness of 95 *nm*.

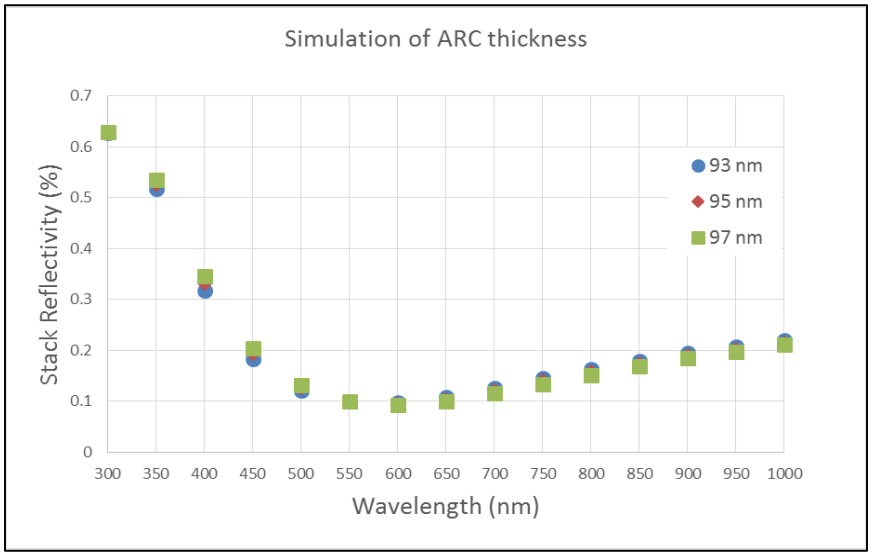


Figure 19: Simulated (Prolith) ARC thickness for minimum reflection

3.2.2 Emitter Optimization

The emitter implant parameters that were used (mentioned in the general process flow) were based on private communication with Nathaniel Kane: RIT Microelectronics Program, 2011. However, these parameters were further tweaked for better device performance.

Simulations were performed using Silvaco ATHENA software to engineer the sheet resistance and the junction depth of the emitter. For the parameters used (mentioned in the general process flow) for emitter implantation, the emitter sheet resistance was 70 $\Omega/\square$ and the junction depth was 0.8 μm. Figure 20 shows a sample simulation that was designed to meet the target parameters. However, in the experiments performed the implant dose was varied to achieve a shallower junction so as to collect most of the carriers generated at the front surface.

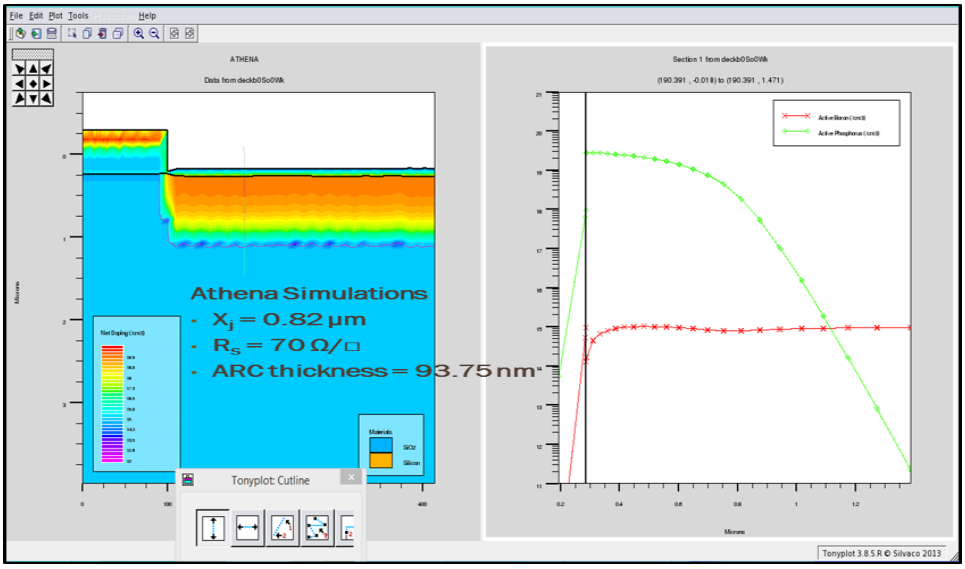


Figure 20: Silvaco ATHENA sample simulation to engineer emitter parameters

The thermal budget on the emitter drive-in and the ARC growth was carefully optimized for more efficient performance. The temperature were kept at a stable 900 ^{0}C to avoid temperature variations within the three step integrated thermal anneal and the time was suitably (due to different emitter implant doses) chosen to achieve the ARC thickness of 95 *nm*.

3.2.3 Two Dimensional Model

As mentioned in the Athena manual [13], the two dimensional model accurately simulates the interstitials and the vacancy movement unlike the basic Fermi model. The two dimensional model is very similar to a generally used fully-coupled model. However, for modeling processes that involve high dose implantation and diffusion processes including oxidation, it is recommended to use the two-dimensional model. The two dimensional model was used while simulating the ARC thickness as well as the emitter junction depth. During thermal oxidation of silicon, some of the dopants in silicon migrate into the oxide and some of it diffuses into the silicon. The silicon lattice atoms become interstitials as oxygen molecules are incorporated into the lattice

to form SiO_2. There exists a possibility that the dopant diffusivity can be enhanced due to the injection of interstitials.

Hence to simulate the creation and movement of the point defects, vacancies and interstitials, TWO.DIM was specified for accurate estimation of thermal anneal time leading to an accurate ARC thickness and emitter junction depth.

3.3 Solar Cell Layout Design

Figure 21 shows the final completed wafer with different area cells. The cells were numbered one through ten for the sake of convenience and to maintain consistency across runs that eased comparison.

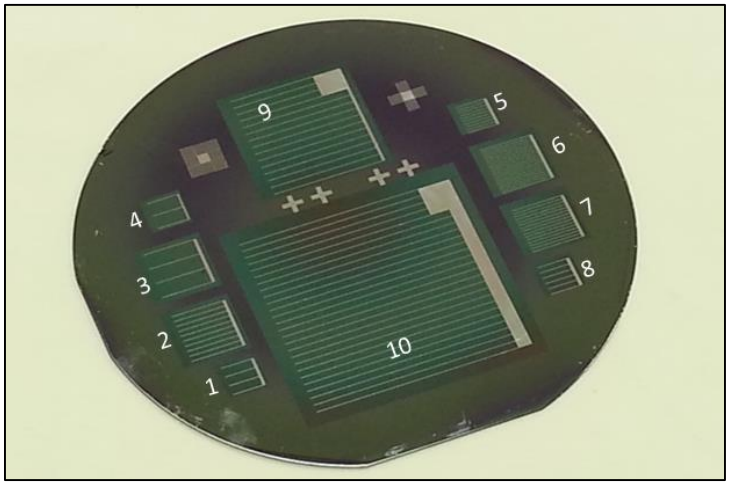


Figure 21: Final completed wafer

The cells 1, 4, 5 and 8 were designed and fabricated with cell area of 0.5625 cm^2 whereas the cells 2, 3, 6 and 7 were desgined and fabricated with a larger cell area of 1.5625 cm^2. The percentage shading on these cells differed to test different design grid patterns. The cells with more number of grid fingers had a high percentage of shading and conversely cells with less grid fingers had less shading, but more series resistance. Cells numbered 9 and 10 were large area cells

producing current over a few amperes which exceeded the current capacity of the Oriel AM1.5 and AM0 solar simulator being used for measuring small area cells. Hence cells 1 through 8 were measured using the calibrator simulator.

Chapter 4 reports the experiments performed including the emitter implant studies, effect of an additional RCA clean and the implementation of a BSF to the turn-key process. It also reports the test setup for the dark and the illuminated solar cell response. Chapter 5 discusses the results obtained from these experiments and Chapter 6 presents the conclusion of the experiments performed using the turn-key process. Chapter 7 will present recommendations on future opportunities with the existing turn-key process focusing towards improving the device performance and increasing the energy-conversion efficiency.

CHAPTER 4: EXPERIMENTATION

With the turn-key process as a baseline for rapid evaluation for process improvements, some of the experiments that were performed are detailed below.

4.1 Substrate quality

Two wafers, one device grade and the other test grade were used to fabricate solar cells with exactly the same fabrication process as described in Section 3.1. The purpose of this experiment was to evaluate the quality of starting substrate on device performance.

4.2 Emitter Profile Engineering

Four device grade wafers and one monitor wafer were used for fabrication of solar cells. Primarily, the fabrication process was the same as described in Section 3.1. However, the screen oxide (ion-implant screening oxide) thickness as well as the anneal time (time 3) were varied to optimize sheet resistance and junction depth of the implanted emitter. Table 1 shows the setup for this experiment.

Table 1: Emitter Profile Engineering Setup

P^{31}, 65 keV, Time 1: 60 mins, Time 2: 15 mins		
Wafer	Screen Oxide (nm)	Anneal Time (mins)
R2W1	90	60
R2W2	90	15
R2W3	0	60
R2W4	0	15

After the front oxide is dry etched, as stated in the general process flow, the monitor wafer was measured for the remaining oxide thickness. A timed 5.2:1 BOE was performed to attain different screen oxide thicknesses (0 *nm* or 90 *nm*). Following the implantation of the desired

species (phosphorus) with dose of $3x10^{15}$ cm^{-2} at 65 *keV*, the wafers with 90 *nm* of screen oxide was stripped in a 10:1 BOE bath.

The experiment was then split for different thermal anneal cycles. All the wafers underwent the step one (Section 3.1) anneal time of 60 minutes at 900 ^{0}C in Nitrogen ambient and step two (Section 3.1) of thermal cycle of 15 minutes at 925 ^{0}C in steam ambient. Wafers 1 and 3 were loaded in the furnace together for step three anneal time of 60 minutes whereas wafers 2 and 4 were annealed with the step three anneal time of 15 minutes. The screen oxide and the step three anneal time were chosen as parameters to be optimized to engineer the junction depth and the sheet resistance of the emitter.

4.3 Implant Parameter Engineering

Two device grade wafers were used to fabricate solar cells with the process flow as described in Section 3.1. However, the two different emitter doses (high and low) were implemented on the device wafers with the purpose of understanding their effects on the solar cell output parameters including short-circuit current, open-circuit voltage and the energy-conversion efficiency. Table 2 shows the setup for this experiment.

Table 2: Implant Parameter Engineering Setup

P^{31}, 65 keV, 900 ^{0}C Anneal		
Wafer	Dose (cm^{-2})	Step 2 Time (mins)
R3W1	1×10^{15}	23
R3W2	6×10^{14}	28

Emitter definition was performed by implanting phosphorus ions into a bare silicon wafer (no screening oxide). A furnace anneal is performed with a set temperature of 900 ^{0}C. There were no variations with the temperature settings unlike the previous runs. The step 2 time on both the

wafers varied due to the difference in the implanted dose. A higher dose implant (more damage) required less time versus a low dose implant to attain a 95 *nm* ARC growth. Athena simulations were performed to analyze the time for which the wafers would receive the steam ambient to produce a target ARC thickness of 95 *nm*. The two dimensional model was implemented to take into consideration the oxidation enhanced diffusion effect.

4.4 Back Surface Engineering

Four device grade wafers were fabricated implementing a back surface field (BSF) which would enhance the current collection at the front surface and reduce recombination at the back surface. The BSF would also assist in lowering contact resistance between the metal and the semiconductor. Also two device grade wafers were used to try a different metal stack (Titanium/Aluminum) that provided a better contact resistance because of the titanium silicide formation. Table 3 shows the setup for this experiment.

Table 3: Back Surface Engineering Setup

BSF (B^{11}, 50 keV); Emitter (P^{31}, 65 keV); 900 ^{o}C Anneal			
Wafer	Dose (cm^{-2})	BSF	Metal Grid Type
R4W1	1×10^{15}	Yes	Aluminum
R4W2	6×10^{14}	No	Aluminum
R4W3	1×10^{15}	Yes	Aluminum
R4W4	6×10^{14}	No	Aluminum
R4W5	1×10^{15}	No	Titanium/Aluminum
R4W6	6×10^{14}	No	Titanium/Aluminum

To realize BSF to improve solar cell performance, the general process flow (Section 3.1) was modified. Prior to the first RCA clean, the wafers were coated with resist and appropriately baked to protect the front. The back of the wafers was implanted with a high dose ($1x10^{16}$ cm^{-2}) of

Boron at 50 *keV* to form a p/p+ junction. The photoresist is stripped in a solvent bath followed by the furnace anneal in Nitrogen ambient at 900 ^{0}C for 30 minutes. For this particular experiment, unlike previous runs, the wafers were implanted into the emitter islands with photoresist/oxide stack as a mask. The thicker mask was used to ensure that the dopants do not implant the un-intended regions. The masking photoresist was then stripped using a Piranha (H_2SO_4:H_2O_2) chemistry. The wafers were then RCA cleaned to remove any organic or metallic impurities. The rest of the steps were followed as per the general process flow, starting with the integrated thermal anneal.

After the metal grid region was lithographically defined, the underlying ARC was etched using BOE solution. Titanium and Aluminum were sputtered without breaking the vacuum on the sputter system at a base pressure of $5x10^{-7}$ *Torr*. 40 *sccm* of Argon powered at 400 *W* was used as the inert gas to sputter the target material. With these parameters, titanium was sputtered for 5 minutes to attain a target of around 250 *Å*. This was followed by an aluminum sputter powered at 400 *W* for 60 minutes with a target thickness of 3000 *Å*. Since the grid needs a thick metal for low series resistance, more aluminum was evaporated using 2 pellets on the evaporator. The wafers were then sintered in a forming gas environment.

4.5 Revised Clean Process

This experiment was primarily the repeat of the previous run, however, only two device grade wafers were doped with an emitter doping of $1x10^{15}$ cm^{-2}. The purpose of this experiment was to revisit the processing steps of the previous experiment since the results were not in accordance to what was anticipated. The causes for the poor output response could either be contamination in the furnace, which would potentially drive defects into the silicon or there could be impurities from the implanter that would contaminate the top surface of the wafer. More

importantly, a key RCA Clean step was noted missing while trying to implement a back-surface field in the previous run. So careful processing with the additional RCA clean was carried out after the first front-surface resist strip. Table 4 shows the setup with the revised process flow.

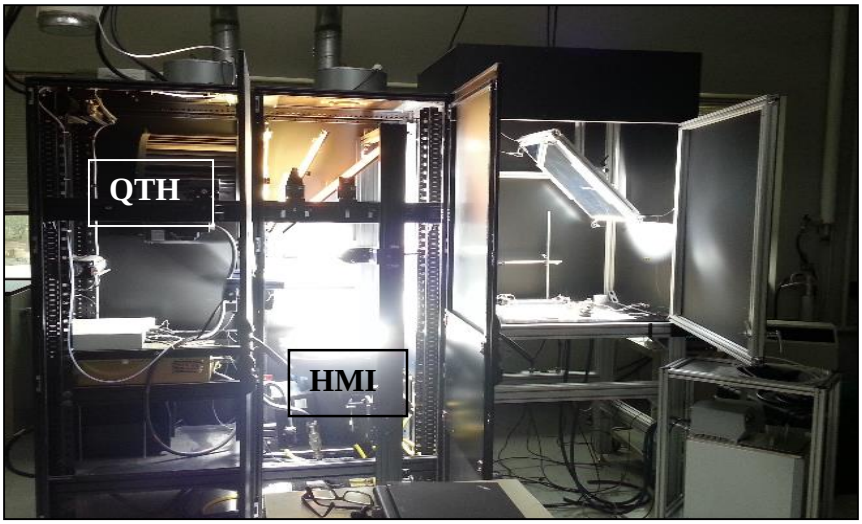
Table 4: Revised Clean Process Setup

P^{31}, 65 keV, 900 ^{0}C Anneal		
Wafer	Dose (cm^{-2})	BSF
R5W1	1×10^{15}	Yes
R5W2	1×10^{15}	No

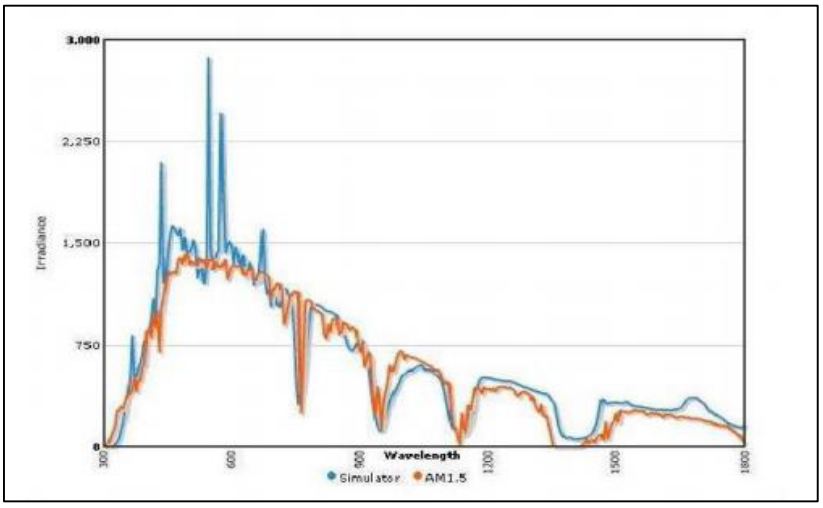
The second wafer (R5W2) did not receive a BSF implant however it did see a furnace run to match all the processing steps as the first wafer (R5W1). After the photoresist was stripped, the wafers went through an RCA clean to get rid of all the impurities in the solvent bath that may have contaminated the wafer which resulted in poor response in the previous experiment. The general process flow was followed after the RCA clean was performed.

4.6 Test Setup

The fabricated solar cells are tested for *I-V* curves in the dark as well as under AM1.5 illumination. Figure 22 (a) shows the test setup of the Oriel AM1.5 and AM0 solar simulator used to characterize the response under AM1.5 spectrum. Two light sources, a QTH (Quartz Tungsten Halogen) bulb and a Mercury-Arc lamp (HMI Lamp) were used to emulate the AM1.5 spectrum. Figure 22 (b) shows the solar simulator spectral output emulating the AM1.5 spectrum.



(a)



(b)

Figure 22: (a) Oriel AM0 and AM1.5 Solar simulator setup (b) Spectral output response from the solar simulator emulating AM1.5 spectrum [14]

A larger bandgap, 1 cm^2 InGaP (Indium-Gallium-Phosphide) characterization cell was used to calibrate the HMI lamp that tunes to the short wavelength spectrum. To calibrate the QTH lamp, a National Renewable Energy Laboratory (NREL) calibrated 4 cm^2 silicon solar cell was used to tune the long-wavelength spectrum. To maintain a constant temperature of the chuck, a chiller was used and was set to room temperature (25 ^0C). The backside of the wafer was grounded

with the help of a vacuum chuck and a probing tip. The other probe tip was connected to the busbar on the metal grid for top-contact. Using the programmed solar simulator, the solar cell output parameters like short-circuit current (I_{sc}), open-circuit voltage (V_{oc}), the maximum power points (V_m, I_m), the Fill Factor (FF) as well as the energy conversion efficiency were generated.

Figure 23: Setup to extract Dark *I-V* and I_{sc}-V_{oc}

Dark *I-V* curves as well as I_{sc}-V_{oc} curves do not directly provide output parameters. However, they are critical to understand the performance of the solar cell with respect to the effect of parasitic resistances and the saturation current densities. Figure 23 shows the test setup to extract the dark *I-V* and I_{sc}-V_{oc} curves using a source measuring unit and a power supply.

Chapter 5 presents the results and the discussions from the various experiments performed including the emitter implant studies, effect of an additional RCA clean and the implementation of a BSF to the turn-key process. Chapter 6 concludes with the results obtained from these experiments and Chapter 7 makes recommendations on future opportunities with the existing turn-key process focusing towards increasing the energy-conversion efficiency.

CHAPTER 5: RESULTS AND DISCUSSIONS

For the first experiment, two 100 *mm* (100) orientation p-Si wafers were used for the fabrication of solar cells with the intent of evaluating the quality of substrate on the device performance. One wafer was test grade (TG) with bulk resistivity range of 10-25 Ω-*cm* and an average thickness of 525 μm whereas the other wafer with the same average thickness was device grade (DG) wafer with resistivity 14-22 Ω-*cm* and the same average thickness. Solar cells were fabricated with the process flow mentioned in section 3.1. Cells 1 through 8 were tested for their illuminated and dark response using the setup shown in Figure 22 and Figure 23.

Table 5 presents the output parameters of different cells from two different quality substrates. These output parameters were extracted using the solar simulator while the cells were being tested for their illuminated characteristics.

The ideality factors for the cells fabricated on the device grade substrate improved by approximately 5% as compared to the cells fabricated on the test grade substrate. The V_{oc} for device grade was a higher by approximately 4% than the test grade whereas the I_{sc} and the Fill Factors were nearly comparable.

Table 5: Solar cell output parameters for Experiment 1

Device Grade (DG)	Area (cm^2)	Isc (mA)	Voc (mV)	Pm (W)	FF (%)	Eff (%)	n (Ideality factor)		I_{01}	I_{02}
5	0.5625	15.359	0.534	5.593	68.217	9.943	1.466	5.015	3.50E-09	8.50E-06
8	0.5625	15.673	0.537	5.88	69.926	10.454	1.461	4.44	6.10E-09	5.80E-06
3	1.5625	41.912	0.538	15.494	68.743	9.916	1.396	3.923	7.00E-09	7.00E-06
7	1.5625	40.02	0.536	15.245	71.011	9.757	1.374	4.002	4.50E-09	9.00E-06
Test Grade (TG)	**Area (cm^2)**	**Isc (mA)**	**Voc (mV)**	**Pm (W)**	**FF (%)**	**Eff (%)**	**n (Ideality factor)**		**I_{01}**	**I_{02}**
5	0.5625	15.442	0.522	5.509	68.382	9.793	1.528	4.84	7.00E-09	7.00E-06
8	0.5625	15.988	0.532	5.98	70.252	10.63	1.511	4.905	9.20E-09	8.50E-06
3	1.5625	42.745	0.52	14.872	66..867	9.518	1.361	4.64	8.50E-09	9.00E-06
7	1.5625	40.996	0.532	15.443	70.828	9.883	1.4	5.028	9.00E-09	1.00E-05

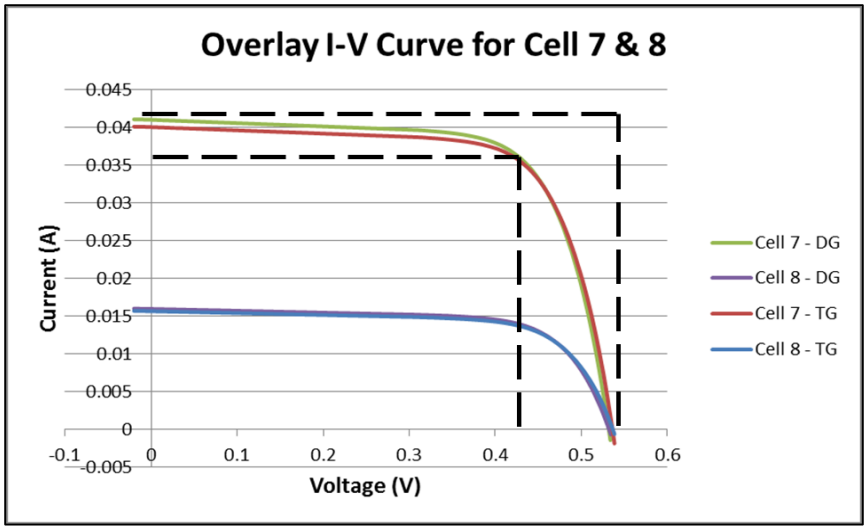


Figure 24: Overlay plot of *I-V* curve for Cell # 7 and # 8 from both substrates

Figure 24 compares the two cells fabricated on different quality substrates. The cells with larger area (1.5625 cm^2) had a higher current output compared to cells with area of 0.5625 cm^2. There wasn't any noticeable difference in the output parameters of similar sized cells to distinguish between the device performances of two different grade substrates. This is because the device performance was degraded by the non-idealities in the device like high series resistance, surface inversion (low shunt resistance) and also poor lifetimes. According to the definition of fill factor, the roundness in the *I-V* curve occupying a lesser area lowers the maximum power points (V_{mp}, I_{mp}) and the output of the device. This is due to high series resistance that restricts the flow of current through the output terminals leading to low output power.

The surface underneath the field oxide was inverted connecting the emitters from the neighboring cells. The trapped oxide charges are positive in nature that repelled the majority holes in the surface connecting two emitter islands. This lead to a high amount of leakage in the device that contribute to low shunt resistance degrading the device. This was confirmed when multimeter leads were placed on the top grid of two neighboring cells and measured for resistance. The result

was 3-7 $K\Omega$ versus an ideal condition of an open circuit. The low quality starting substrate that leads to poor lifetime of the carriers was also one of the reasons of degraded output response.

Figure 25 shows the overlay of the I_{sc}-V_{oc} curves comparing cell 3 from a test grade and a device grade wafer. Comparing the fabricated cells from two different substrates, there appears no significant effect on performance for the two different substrates. High values of the ideality factor in the 4-5 range signify high series resistance. This can be attributed to the surface inversion, connecting the neighboring emitter islands leading to poor device performance.

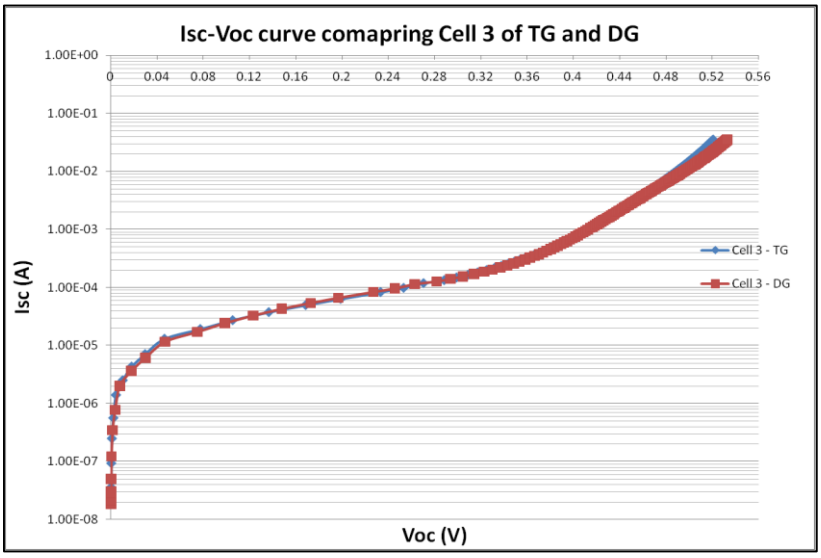


Figure 25: Overlay plot of I_{sc}-V_{oc} curves for TG and DG substrates

A few reasons that can be attributed to poor device performance are poor lifetimes due to poor quality substrate, high emitter doping (3 x 10^{15} cm^{-2}), deeper emitter junction and also the shunting effect caused due to the formation of inversion layer because of the trapped charges in the field oxide. Along with poor lifetime and deeper junction, the collection probability degrades and increases the recombination towards the surface. Combining these non-idealities in the device,

the difference between the substrate quality and the device performance was masked and inconclusive.

For the following experiments, 100 *mm* (100) oriented p-Si device grade wafers with an average thickness of 525 μm were used to fabricate solar cells. The resistivity of the starting substrate was measured on the monitor wafer to be 14-15 Ω-*cm*.

Table 6 shows the experimental and simulated sheet resistances for this experiment. The monitor wafer was cleaved in two pieces. One part of the piece was underwent a timed BOE etch to realize 90 *nm* screening oxide. The other half of the cleaved wafer had the silicon exposed. These cleaved wafer pieces were implanted and annealed along with the device wafers. The sheet resistances were measured on different areas of the cleaved monitor wafer.

Table 6: Athena simulated versus experimental emitter sheet resistance (R_s)

Wafer	Screen Oxide (nm)	Anneal Time 3 (mins)	Athena Simulated Rs (Ω/□)	Experimental Rs (Ω/□)
1	90	60	108.31	34.23
2	90	15	109.63	104.1
3	0	60	34.62	33.7
4	0	15	34.38	34.1

The sheet resistance values from the experimental wafers matched closely with the simulated sheet resistance except for Wafer 1. The reason for this variation is uncertain.

Table 7 shows the output parameters that were extracted from the solar simulator using AM1.5 incident spectrum.

Wafer #1	Area (cm2)	Isc (mA)	Voc (V)	Im (mA)	Vm (V)	Pm (mW)	FF (%)	Eff (%)	n (Ideality Factor)		I_{01}	I_{02}
5	0.5625	16.352	0.531	14.325	0.424	6.080	70.014	10.809	1.403	5.347	2.00E-09	8.00E-06
8	0.5625	18.398	0.528	16.144	0.412	6.649	68.468	11.820	1.472	4.936	2.80E-09	9.00E-06
3	1.5625	38.721	0.524	23.399	0.344	8.059	39.725	5.158	1.980	3.400	3.00E-07	9.00E-05
6	1.5625	41.244	0.532	36.997	0.425	15.739	71.763	10.073	1.355	4.752	3.00E-09	1.00E-05
Wafer #2	Area (cm2)	Isc (mA)	Voc (V)	Im (mA)	Vm (V)	Pm (mW)	FF (%)	Eff (%)	n (Ideality Factor)		I_{01}	I_{02}
5	0.5625	16.169	0.525	14.558	0.410	5.972	70.297	10.617	1.296	4.324	8.00E-10	4.00E-07
8	0.5625	17.091	0.541	15.593	0.433	6.752	73.032	12.003	1.365	4.430	1.50E-09	4.00E-06
3	1.5625	44.849	0.529	38.111	0.396	15.093	63.637	9.660	1.620	4.552	3.00E-09	3.10E-06
6	1.5625	45.982	0.543	41.242	0.434	17.919	71.776	11.468	1.260	3.684	1.50E-09	1.00E-06
Wafer #3	Area (cm2)	Isc (mA)	Voc (V)	Im (mA)	Vm (V)	Pm (mW)	FF (%)	Eff (%)	n (Ideality Factor)		I_{01}	I_{02}
5	0.5625	18.572	0.533	16.637	0.435	7.233	73.131	12.859	1.396	4.883	2.60E-09	4.00E-06
8	0.5625	18.398	0.528	16.144	0.412	6.649	68.468	11.820	1.365	5.213	3.20E-09	6.00E-06
3	1.5625	48.688	0.541	42.953	0.422	18.143	68.942	11.611	1.514	4.671	7.00E-09	1.40E-05
6	1.5625	48.703	0.533	43.921	0.435	19.096	73.586	12.222	1.365	5.031	5.50E-09	7.00E-06
Wafer #4	Area (cm2)	Isc (mA)	Voc (V)	Im (mA)	Vm (V)	Pm (mW)	FF (%)	Eff (%)	n (Ideality Factor)		I_{01}	I_{02}
5	0.5625	16.182	0.541	14.552	0.449	6.538	74.709	11.624	1.393	5.579	3.20E-09	3.30E-06
8	0.5625	18.112	0.544	15.994	0.444	7.100	72.070	12.621	1.385	4.950	2.20E-09	8.50E-06
3	1.5625	45.174	0.536	40.516	0.419	16.966	70.118	10.858	1.498	4.551	5.50E-09	8.50E-06
6	1.5625	42.699	0.546	39.135	0.445	17.432	74.780	11.156	1.391	4.804	5.50E-09	7.00E-06

Table 7: Solar cell output parameters for Experiment 2

Cell 3 compared to all other cells consistently had a lower FF, lower efficiency and comparatively higher ideality factors. This is because there were a few mask (glass plate) defects that were present on cell numbered 3. Figure 26 shows the defects that accounted for non-idealities to the device performance.

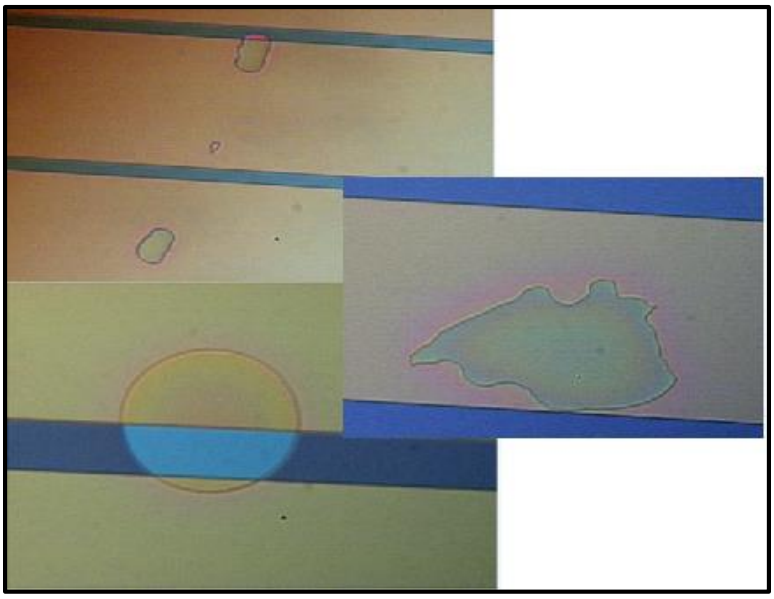


Figure 26: Mask Defects on Cell #3

The metal grid on that particular cell was not optimally designed. With fewer metal grid fingers, the shadowing factor was less resulting in relatively higher short-circuit current values. However since the grid fingers were widely spaced the charge carriers had to travel a long distance before they were collected which contributed to the high series resistance.

Figure 27 (a) and (b) shows the overlay plot of cell with area 1.5625 cm^2 comparing the I_{sc} and V_{oc} generated from the same cell (Cell #3) of each wafer. Considering the average V_{oc} of 0.54 V and the average I_{sc} of 45 mA, the V_{oc} and the I_{sc} of the similar sized cells varied by approximately 6% and 12% respectively.

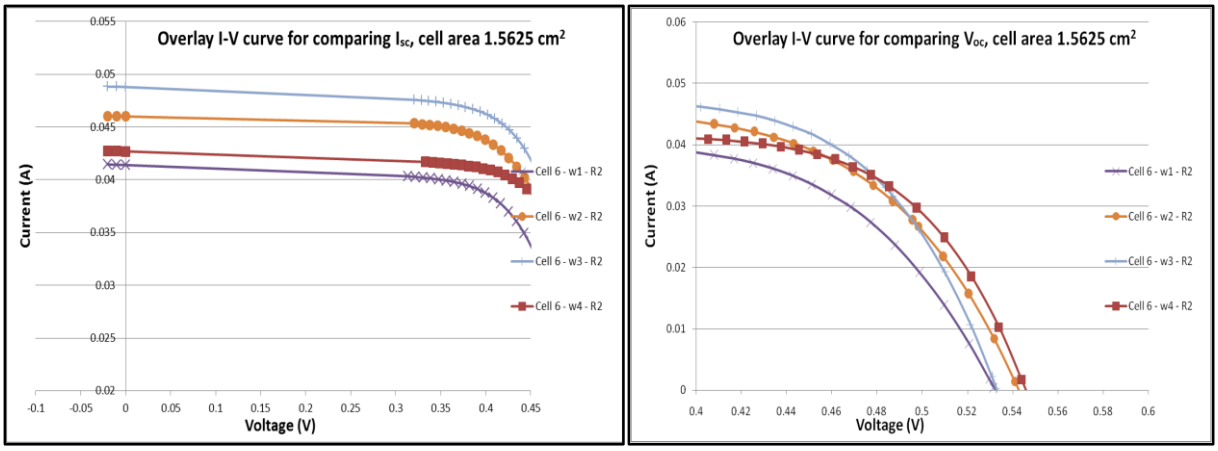


Figure 27: Overlay plot of Cells 6 and 8 for all wafers comparing (a) I_{sc} and (b) V_{oc}

There were no certain conclusions comparing cell 6 from different wafers. For all the wafers, the ARC thickness and the junction depth were larger than the simulated results. This is because the oxidation enhanced diffusion effects were not taken into consideration. However, due to the effect of high series resistances and poor lifetimes, the performance of these devices was degraded. The recombination events in the device impacted the V_{oc} and the I_{sc} of the device. Also the ARC oxide thickness was away from target by 20 *nm* since the TWO.DIM model was not included in the simulations. Inaccurate ARC thickness meant there was more reflection from the top surface which otherwise would have contributed towards current from the device. The energy conversion efficiency on wafer 3 higher by approximately 9% compared to other wafers.

Table 8: Athena simulated versus experimental averaged ARC thickness.

Wafer	Screen Oxide (nm)	Anneal Time 3 (mins)	Athena Simulated ARC Thickness (Å)	Experimental averaged ARC Thickness (Å)	Athena Simulated Junction Depth (µm)	Experimental averaged Junction Depth (µm)
1	90	60	578	850	0.65	1.1
2	90	15	578	700	0.65	1.1
3	0	60	985	1130	0.82	1.24
4	0	15	985	1120	0.82	1.24

In this experiment, only screen oxide thickness and the anneal time on step 3 were the variables. The time on step 2 of the thermal anneal that was responsible for the anti-reflective oxide growth was kept constant at 15 minutes for all wafers. A desired target thickness of 95 nm was anticipated for the wafers with no screening oxide.

Table 8 shows the simulated versus the experimental ARC thickness and junction depth. The extracted ARC thickness was approximately 20 *nm* thicker than the simulated ARC thickness. Also, the junctions were deeper by 0.4 μm when compared to simulated values. On further review, it was noticed that oxidation enhanced diffusion effects in Athena simulation were not considered. These enhanced diffusion effects led to deeper junctions and relatively thicker oxide growth.

The field oxide separating the two emitter islands had charges trapped in it. These positive charges repelled the holes in the substrate. Since the substrate was a lightly doped p-type substrate, the inversion took place rather easily connecting the emitter islands. This provided a shunt path to the charge carriers and impacting the device performance. The leakage current in the devices was higher which was evident when two metal lines of adjacent cells were probed to show resistance in the range of 3-7 $K\Omega$. This inversion added to the non-ideal current leading to higher ideality factors denoting poor performing device.

Figure 28 shows an overlay of *I-V* curves from the 1st and the 2nd experiment. The difference between the two runs (Device grade wafer (run 1) and Wafer #3 (run 2)) for the same parameters (no screen oxide and step three time - 60 minutes) were the phosphorus implant dose of $5 \times 10^{15}\ cm^{-2}$ for the first run versus the $3 \times 10^{15}\ cm^{-2}$ for the second.

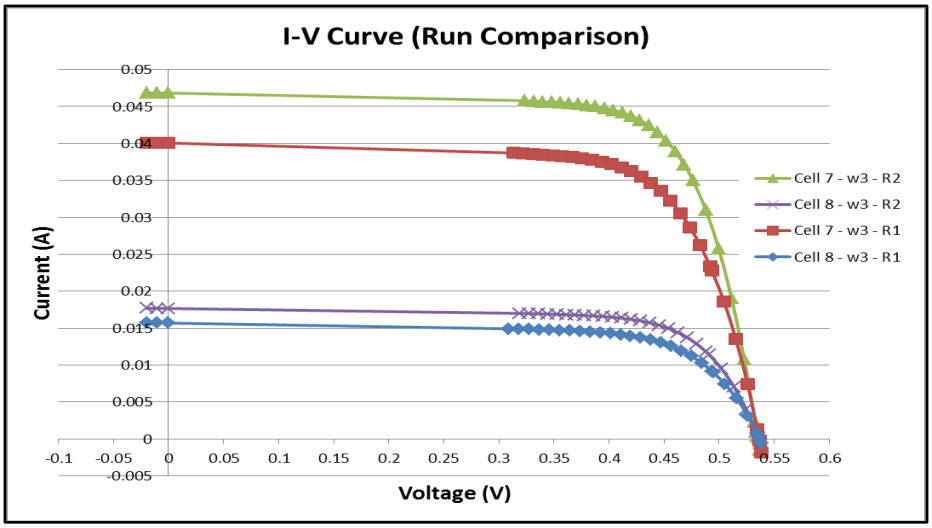


Figure 28: Comparison of the *I-V* curve for Experiment 1 and Experiment 2

The step two thermal anneal time was 12 minutes for the first run vs. 15 minutes for the second run. Also, multiple RCA cleans were performed during the second experiment. A 13 % increase in the short-circuit current was observed for the 2nd run. This increment can be attributed to the fact that the emitter was relatively lightly doped which meant the lifetimes of holes in the emitter region were a little better leading to less recombination. The wafers in run 2 were RCA cleaned after they were dipped in either a BOE solution or the resist solvent strip bath to eliminate any impurity that would act as a trap.

The charges trapped in the oxide inverted the surface beneath the field oxide connecting the islands. The lightly doped substrate assisted the formation of the inversion layer owing to increase in the saturation (leakage) current and hence a poor ideality factor. To characterize the surface inversion, the cells on one of the wafers (wafer 3) were cleaved and isolated. These separated cells were then re-measured. Table 9 compares the output parameters for the isolated cells (marked with arrows) with the non-isolated cells.

Table 9: Solar cell output parameters for Isolated Cells – Experiment 2

R2W3	Area (cm2)	Isc (mA)	Voc (V)	Im (mA)	Vm (V)	Pm (mW)	Fill Factor (%)	Efficiency (%)	n1	n2
1	0.5625	16.947	0.532	14.588	0.425	6.202	68.793	11.027	1.448	4.44
1.1	0.5625	18.959	0.524	16.247	0.408	6.630	66.760	11.787	1.3	3.244
2	1.5625	46.702	0.540	41.369	0.432	17.883	70.844	11.445	1.435	4.48
2.1	1.5625	49.600	0.535	43.722	0.428	18.697	70.516	11.966	1.35	2.955
3	1.5625	48.688	0.541	42.953	0.422	18.143	68.942	11.611	1.514	4.67
3.1	1.5625	50.225	0.538	43.880	0.420	18.437	68.177	11.799	1.303	2.906

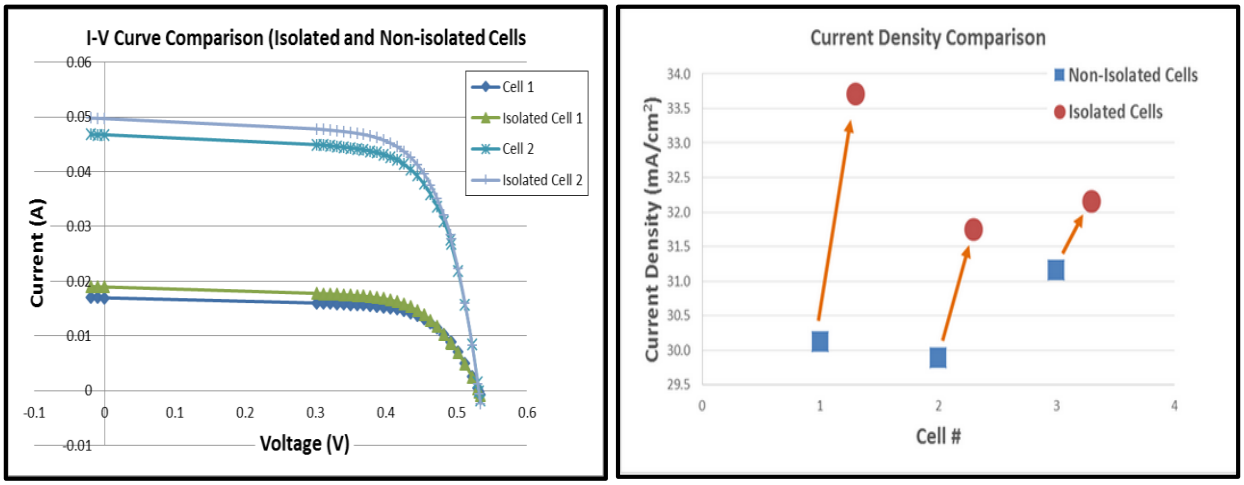


Figure 29: (a) *I-V* Curve (b) J_{sc} comparison of isolated and Non-isolated cells

Figure 29 (a) compares the *I-V* curves and 29 (b) compares the current density of isolated and non-isolated cells. The cells were isolated by cleaving them manually. The current generated by the isolated cells were higher by 6-8% with a marginal change in the open-circuit voltage. The inversion charge layer was essentially cut-off because of the isolation. Hence the overall saturation current (leakage current) in the device was reduced leading to relatively better ideality factors. Since these non-idealities were mitigated to an extent, the overall output power of the device was increased, leading to better efficiencies compared to the non-isolated cells.

For experiment 3, two 100 *mm* device grade wafers were used to fabricate devices with the experimental setup as shown in Table 2. The purpose of this experiment was to fabricate devices with a low and a high implant dose and to understand their effects on the short-circuit current and

the open-circuit voltage. The time on step 2 of the integrated thermal anneal had to be adjusted according to the implant dose. For the highly doped emitter (1 x 10^{15} cm^{-2}), the steam was allowed to flow for 23 minutes vs. 28 minutes for the lightly doped emitter (6 x 10^{14} cm^{-2}). Two-dimensional model was incorporated to take into consideration the oxidation enhanced diffusion in the Athena simulations. The measured ARC thickness was approximately equal to the target of 95 *nm*.

The devices failed to perform for this experimental run. The reason for this failure wasn't completely understood. However, revisiting the process, a timed BOE etch was performed to etch away the ARC oxide for the metal evaporation. Speculations on the incomplete removal of ARC oxide could be a possibility which prevented the contact between the aluminum metal and the highly doped emitter.

Since no results were observed from experiment 3, a fourth experiment with 6 device grade wafers (Table 3) duplicating the same run was performed. Four wafers received an additional back surface field to enhance the current collection as well as increase the V_{oc} of the device due to the band-bending, as shown in Figure 13. With the last two wafers a different metal stack (Ti/Al) was implemented so as to achieve better contact resistance. Table 10 shows the solar cell output response for experiment 4.

Table 10: Solar cell output parameters for Experiment 4

R4W1 (1e15 + BSF)	Area (cm^2)	Isc (mA)	Voc (mV)	Im (mA)	Vm (mV)	Pm (mW)	FF (%)	Eff (%)	n1	n2
1	0.5625	15.366	0.505	13.637	0.395	5.381	69.329	9.566	1.300	4.455
3	1.5625	42.435	0.504	36.954	0.377	13.915	65.122	8.905	1.263	4.649
5	0.5625	14.746	0.491	13.123	0.384	5.041	69.579	8.961	1.483	4.949
7	1.5625	39.783	0.500	35.070	0.391	13.696	68.816	8.766	1.251	4.398
R4W2 (6e14 + BSF)	Area (cm^2)	Isc (mA)	Voc (mV)	Im (mA)	Vm (mV)	Pm (mW)	FF (%)	Eff (%)	n1	n2
1	0.5625	15.673	0.508	13.512	0.384	5.188	65.166	9.223	1.243	4.394
3	1.5625	43.752	0.502	37.696	0.353	13.307	60.606	8.517	1.229	4.232
5	0.5625	15.119	0.490	13.244	0.382	5.065	68.362	9.004	1.228	4.443
7	1.5625	40.964	0.495	35.811	0.375	13.432	66.233	8.597	1.234	4.785
R4W3 (1e15)	Area (cm^2)	Isc (mA)	Voc (mV)	Im (mA)	Vm (mV)	Pm (mW)	FF (%)	Eff (%)	n1	n2
1	0.5625	18.073	0.527	16.087	0.422	6.781	71.218	12.055	1.338	4.572
3	1.5625	49.869	0.522	44.703	0.390	17.436	67.003	11.159	1.283	4.676
5	0.5625	17.645	0.521	15.695	0.426	6.687	72.778	11.888	1.296	4.264
7	1.5625	47.893	0.527	43.616	0.414	18.049	71.460	11.552	1.276	4.383
R4W4 (6e14)	Area (cm^2)	Isc (mA)	Voc (mV)	Im (mA)	Vm (mV)	Pm (mW)	FF (%)	Eff (%)	n1	n2
1	0.5625	18.051	0.522	15.626	0.407	6.355	67.482	11.298	1.374	4.256
3	1.5625	49.155	0.523	41.533	0.381	15.834	61.590	10.134	1.263	4.260
5	0.5625	17.388	0.516	15.634	0.404	6.315	70.359	11.226	1.242	4.488
7	1.5625	46.940	0.518	41.267	0.392	16.193	66.552	10.364	1.221	4.253

Data for 4 out of the 8 tested cells is tabulated in Table 10. Wafers 1 (R4W1) and 2 (R4W2) received the BSF implant with a high and low emitter dose variation while wafers 3 (R4W3) and 4 (R4W4) had no BSF implant but received a high and low emitter dose respectively. In theory, wafers 1 and 2 were expected to show a much better response than 3 and 4 because of the advantages offered by the BSF. In addition, wafers 1 and 3 with high emitter doping were expected to show a better response since I_{sc} and V_{oc} increases with doping. However, the data extracted from the output response was completely contradictory. Wafers that did not receive a BSF implant performed better than the wafers that received the BSF implant.

Figure 30 compares the energy-conversion efficiencies of all four wafers. The BSF implanted wafers underwent extra processing steps of protecting the front with photoresist, backside implant, solvent resist strip and then furnace annealing for 30 min in Nitrogen ambient.

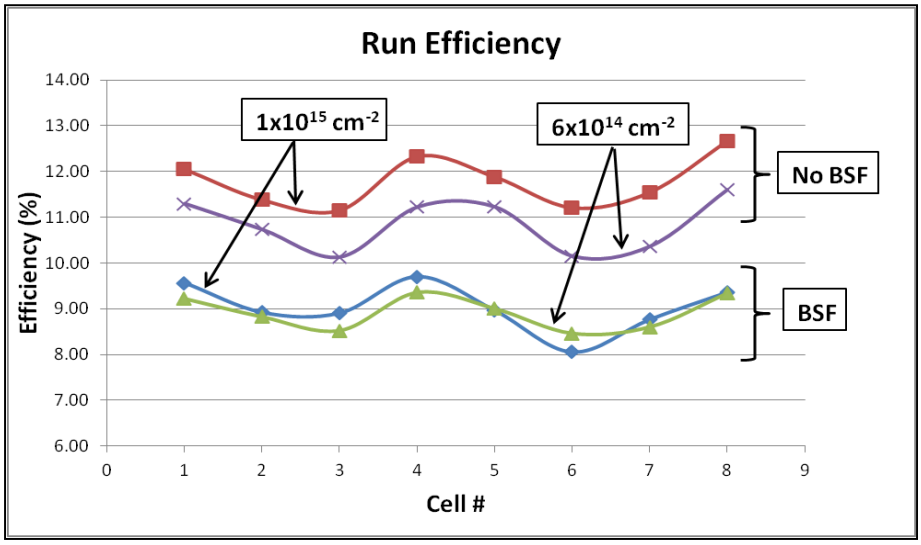


Figure 30: Comparison of Efficiencies from all 4 wafers

Assuming these processing steps contributed to the poor performing devices, an explanation may be that the two BSF implanted wafers did not receive an RCA clean after the resist was stripped. Thus, the potential impurities in the solvent bath were incorporated in the silicon via diffusion during the following high temperature furnace anneal. These impurities acted as trap sites for minority charge carriers, which otherwise would contribute to the short-circuit current.

Figure 31 shows the impact of an extra thermal anneal step on the maximum voltage point (V_m). Since the wafers had to go through an extra thermal step (to anneal BSF implant damage), the lifetime of minority charge carriers are directly impacted. This led to a poor output voltage and power response.

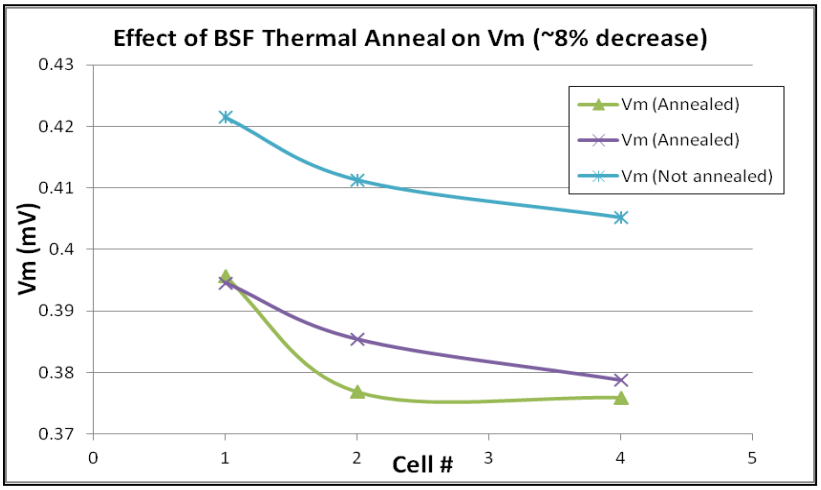


Figure 31: Impact of an extra furnace run on V_m

The ideality factors were somewhat better because of the extra cleaning procedures that were incorporated in the process run. However, they were still far away from ideal indicating leakage in the device. The probable suspect that can be attributed to the leakage is the surface inversion beneath the oxide. Our assumption is the fixed charges trapped in the oxide repelled the holes from the surface beneath the oxide and connected the islands causing leakage in the device when under no illumination. The use of lightly doped substrates and trapped oxide charges were amongst the probable causes of the surface inversion.

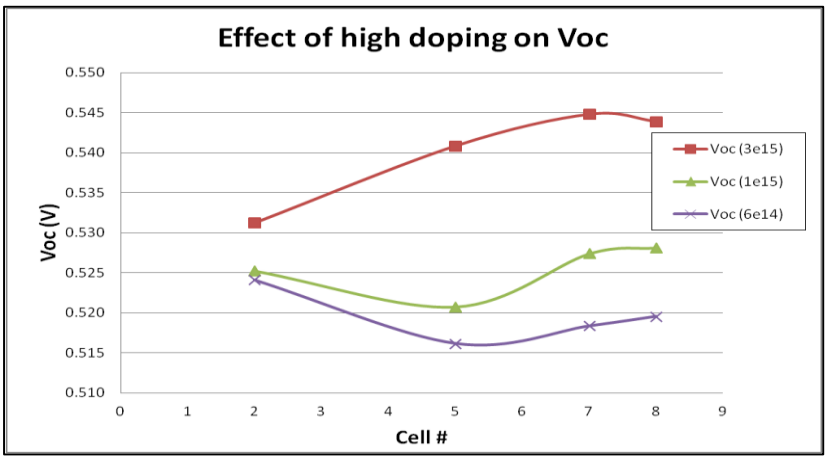


Figure 32: Effect of high emitter doping on V_{oc}

Figure 32 shows the effect of high emitter doping on V_{oc}. Wafers with high emitter doping showed a better output voltage compared to lighter doped wafers. This is because the current and the voltage are directly proportional to the emitter doping. The equation showing the V_{oc} dependence on doping is as shown below. [3]

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{(N_A + \Delta n)}{n_i^2} \Delta n\right) \tag{31}$$

Wafers 5 and 6 with Titanium/Aluminum stack were not tested due to issues with the calibration cells required to calibrate the mercury-arc lamp. However, these wafers are expected to show a better response compared to wafers 3 and 4 because of the lower series and contact resistance.

Experiment 5 was a replicate experiment 4 with two device grade wafers undergoing high dose emitter implant ($1x10^{15}$ cm^{-2}) and exactly the same processing steps except wafer 1 received the BSF implant while wafer 2 did not receive the same. However, both the wafers received the BSF furnace anneal treatment for easy comparison of the fabricated devices. Extra care was taken to include an RCA clean after the front-side photoresist for BSF was solvent stripped.

Table 11: Solar cell output parameters for Experiment 5

R5W1 (1e15 + BSF)	Area (cm^2)	Isc (mA)	Voc (mV)	Im (mA)	Vm (mV)	Pm (mW)	FF (%)	Eff (%)	n1	n2
1	0.5625	20.332	0.522	17.800	0.396	7.043	66.330	12.520	1.439	4.844
2	1.5625	51.787	0.519	45.076	0.377	16.988	63.264	10.872	1.447	4.674
4	0.5625	19.263	0.502	16.869	0.376	6.342	65.528	11.274	1.337	4.722
8	0.5625	19.813	0.528	17.715	0.413	7.321	70.003	13.015	1.365	4.709
R5W2 (1e15)	Area (cm^2)	Isc (mA)	Voc (mV)	Im (mA)	Vm (mV)	Pm (mW)	FF (%)	Eff (%)	n1	n2
1	0.5625	18.608	0.511	16.354	0.399	6.520	68.609	11.590	1.375	4.705
2	1.5625	48.396	0.511	42.248	0.398	16.833	68.092	10.773	1.308	4.375
4	0.5625	18.243	0.505	15.970	0.383	6.114	66.350	10.869	1.342	4.355

Table 11 presents the solar output response for experiment 5. Only 3 cells from wafer 2 (R5W2) were tested because the wafer broke during the course of processing rendering other cells useless. The BSF implanted wafers produced much better results when compared to the wafer that did not receive BSF implant. The short-circuit current and the open-circuit voltage were positively impacted due to the implementation of back-surface field. Figure 33 shows the effect of back-surface field on (a) short-circuit current and (b) energy-conversion efficiency.

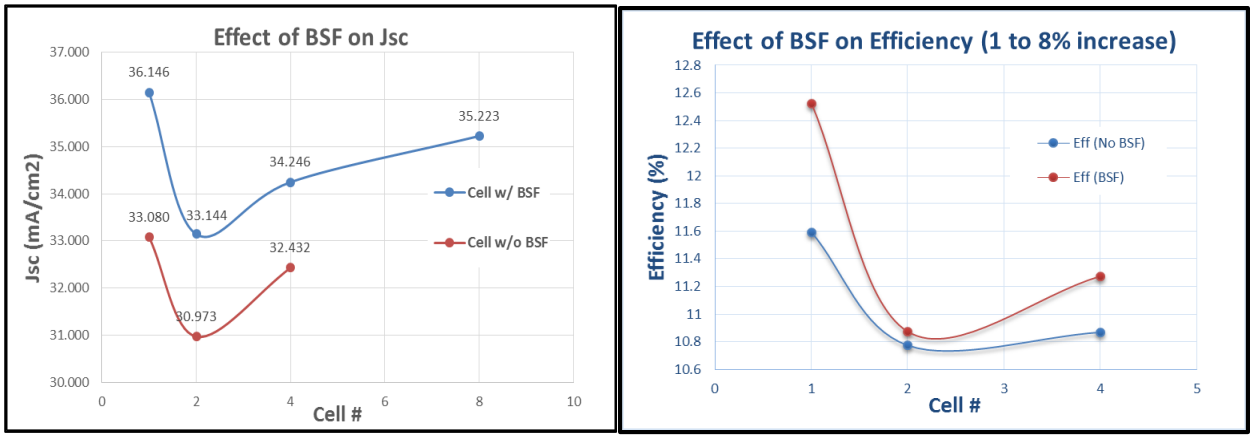


Figure 33: Effect of BSF on (a) J_{sc} and (b) Efficiency

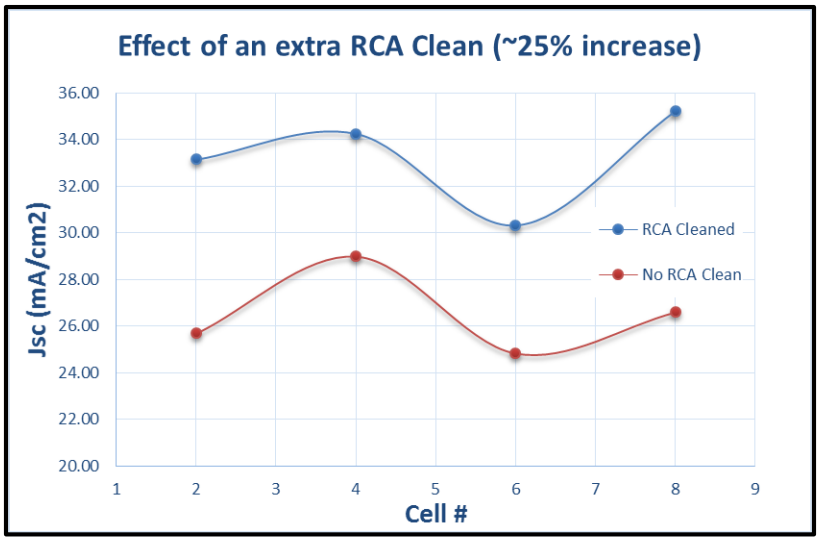


Figure 34: Effect of an extra RCA clean on current

In addition to the BSF, an additional RCA clean helped get rid of impurities that may have acted as trap sites for the charge carriers, which was the degrading factor for wafers 1 and 2 in experiment 4. The additional RCA clean led to an approximate 25% increase in the short-circuit current generated by the device and hence bumped up the energy-conversion efficiency. Figure 34 depicts the effect of RCA clean on the short-circuit current.

Due to an additional BSF implant anneal furnace step, for both the wafers, the maximum voltage point (V_m) was affected due to the deterioration of the lifetime of the carriers. Figure 31 confirms that the wafer that underwent an additional furnace run had a degraded lifetime that led to a poor maximum voltage response. There were no significant improvements in the ideality factors of the fabricated solar cells.

CHAPTER 6: CONCLUSION

Attempts to optimize the process flow of single-crystal silicon solar cell were successfully performed. A basic process flow has been created and further improvements to the process have been implemented yielding a modest 13% efficient solar cells. A definite opportunity to incorporate sophisticated IC practices into PV practices can be seen while still keeping the process flow simple and executing the fabrication as a quick turnkey process.

A difference between the test and device grade wafers was evaluated with fabricating solar cells on the respective substrates. A conventional process flow was followed to yield an energy-conversion efficiency of about 9.5%. The actual performance parameters differentiating the substrate qualities were masked by the non-idealities in the device.

An attempt to further engineer the sheet resistance and the junction depth of the highly-doped emitter region was successfully simulated using ATHENA. Also, an integrated thermal anneal step along with an appropriate ARC thickness was simulated and fabricated on device grade wafers. Improved 12% efficient solar cells were successfully fabricated.

Another attempt with implementing a back-surface field implant on high and low doped wafers was successfully performed. A p-type dopant (Boron) was implanted on the backside of the wafer. This helped to redirect the electrons towards the front of the device because of the barrier created with the p/p+ region. This implementation resulted in an 8-9% increase in the short-circuit current and it did boost the open-circuit voltage by a few millivolts. In addition, the open-circuit voltage is directly proportional to the emitter doping. With higher doping, the output voltage response was higher compared to lightly doped emitters.

An additional RCA clean step was performed to get rid of impurities after the photoresist was stripped in the solvent bath. A 25% increase in short-circuit was observed due to an extra cleaning step. This marks to importance of incorporating IC practices into PV production systems which otherwise is often neglected.

The ideality factors on the devices fabricated were still poor and that was because of the charges trapped in the oxide which resulted in surface inversion connecting the two islands providing a shunting path. The substrate was lightly doped and hence affected the ideality factor of the device.

It can also be concluded that the wafers that received the back-surface implant had to go through an extra furnace step to anneal out the damage. The lifetime of the carriers were highly affected which resulted in a poor maximum voltage point on the *I-V* curve. Hence the efficiency was degraded.

Summarizing the conclusion, the process developments that are discussed in this report and the future opportunities clubbed with the recent trends in the photovoltaic market with single-crystal silicon production, while still keeping the process flow simple and as a turnkey process, provides a unique and a very promising opportunity to blend the IC practices in the photovoltaic industry.

CHAPTER 7: FUTURE WORK

A few experiments with successful operation of the solar cell devices with a modest output current, fill factor and the energy-conversion efficiency were performed. However, there are a few propositions for further improvements that have been noted. While mentioning these inputs, an effort to keep the process flow less complex and yet commendable has been proposed.

7.1 Mask Design

A new mask set is required to ease the process of fabrication. With the current mask-set, the alignment marks on the second-level lithography were inaccurately placed and were incompatible with the contact aligner used. Hence the location of the alignment marks needs to be changed to manually align the features to the patterned wafer. The grid dimension and the design can be engineered for optimum device performance.

7.2 Anti-Reflection Coating

Silicon dioxide was used as an ARC to minimize reflection of the incident light. Theoretically, the optimum refractive index of the ARC material is around 2. This indicates that options including silicon nitride, tantalum-pentaoxide, indium tin oxide or even a stacked ARC (Oxide/Nitride stack) with refractive index nearly about the optimum can be used to minimize the reflection from the top surface. A careful thought on front-surface recombination also needs to be given to optimize the device performance.

7.3 Substrate Quality

The starting substrate used to fabricate the solar cell should have a higher doping concentration. A lower substrate doping concentration will allow the minority charge carriers

(electrons) to migrate freely and invert the surface underneath the oxide due to the non-ideal oxide charges. An optimum value of substrate doping in the range of $5x10^{15}$ to $1x10^{16}$ cm^{-3} would yield a proper balance between the short-circuit current and also the open-circuit voltage. Along with higher substrate doping and a better substrate quality, the thickness of the substrate is an important parameter since it would help determine the lifetime of minority charge carriers.

7.4 Metallization

The devices that were tested showed high parasitic resistances which degraded the device performance. Titanium/Aluminum stack is a viable option that can provide a higher conductivity and can present a better ohmic contact to n-type emitter. The next strong consideration is the implementation of copper as a front metal contact with a Nickel as a diffusion barrier. It significantly lowers down the cost of operation with better electrical characteristics.

7.5 Thermal Cycle Parameters

Two separate furnaces step, to anneal the damage from the back-surface implant and to grow field oxide, can be merged better thermal budget. Also temperature inconsistencies would be minimized. Simulations on the step two of thermal anneal to determine an effective ARC thickness needs to be performed for different emitter doping and different ARC materials.

7.6 Implant Anneal Process

Process development with regards to a turnkey process can be further optimized. The back-surface implant anneal as well as the emitter anneal can be performed together in the integrated thermal anneal run. This would eliminate an extra temperature step and hopefully preserve the lifetime of the minority charge carriers, which otherwise were getting deteriorated. This development is flexible with different ARC materials.

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