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Development of Nickel Silicide for Integrated Circuit Technology

A thesis submitted in
partial fulfillment of the requirements for the degree of
Master of Science in
Materials Science & Engineering

By

Phu Do
Materials Science & Engineering Department
Rochester Institute of Technology
February 2006

Dr. Sean L. Rommel (Thesis Advisor) Sean L. Rommel Date: 3/21/06

Dr. Santosh Kurinec (Committee Member) Santosh K. Kurinec Date: 03/21/06

Dr. Surendra K. Gupta (Committee Member) S. K. Gupta Date: 03/22/06

Dr. K.S.V. Santhanam (Department Head) Santhanam KSV Date: March 29, 06

Development of Nickel Silicide for Integrated Circuit Technology

By

Phu H. Do

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Phu H. Do March 23, 2006

First M. Last Month Day, Year

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Abstract

Continuous advancements in devices, materials and processes have resulted in integrated circuits with smaller device dimensions, higher functionality and higher speed. The complementary metal oxide semiconductor (CMOS) technology has been the engine of this success. The MOS transistor is shrinking following the Moore's Law over the last several decades. As the device dimensions are approaching nanometer regime, parasitic resistance, capacitance and inductance are beginning to influence the performance significantly.

Self-aligned silicide process was developed in mid eighties that allowed reduction of gate and contact resistance by using metal silicides as low resistivity materials. The process also enabled higher packing density.

Many silicides have been extensively studied and Titanium silicide ($TiSi_2$) and Cobalt silicide ($CoSi_2$) have been implemented into modern devices. With devices shrinking, $TiSi_2$ and $CoSi_2$ are finding serious limitations of linewidth effect and excessive silicon consumption. One attractive alternative is nickel monosilicide (NiSi). NiSi has comparable resistivity as traditional silicides yet consumes less silicon during formation, no line width dependence, single thermal treatment, and relatively planar silicide-silicon interface. However, implementation of NiSi into future generation devices has been delayed by limited knowledge of its thermal instability.

In the study presented in this thesis, silicidation of nickel metal has been investigated. Silicidation has been carried out on doped and non-doped polycrystalline and crystalline silicon regions. Rapid thermal process was used for the silicidation of sputtered nickel metal into nickel silicide. The electrical and material properties of nickel silicide were

characterized, and correlations between electrical data, material properties, and silicidation conditions have been made.

Electrical resistivity was calculated through the uses of sheet resistivity measurements using the four-point probe technique and the grooving technique. The grooving technique was used to measure the silicide's thickness necessary for electrical resistivity calculation. The silicide surface topography and phase composition were analyzed using the AFM and XRD technique respectively. Furthermore, RBS and SIMS analysis were done to complement the material properties study of nickel silicide.

The experimental result showed strong correlation between nickel silicide's electrical resistivity with surface topography and phase composition. A multiple phases mixture composition was observed in crystalline silicon and polysilicon regions at temperature less than 573°C and 695°C respectively. It is concluded that the most optimal silicidation condition for obtaining the single-phase nickel monosilicide was at 695°c for 60 sec. Such condition yield a NiSi film with an electrical resistivity of ~1.6×10^{-5} (Si), 3.3×10^{-5} Ω-cm (Poly). The most optimal silicidation for obtaining the lowest multi-phase mixture silicide was found to be at 500°C for 20sec or more. Such condition yielded a Ni_xSi + NiSi phase mixture with an electrical resistivity of ~ 1.6×10^{-5} (Si), 2.5×10^{-5} Ω-cm (Poly).

Table of Content

Acknowledgement iii
Table of Content viii
List of Figures x
List of Tables xii
1. Introduction/Motivation 1
1.1. Integrated Circuit Technology Overview 2
1.2. MOSFET Fundamentals 3
1.3. IC Technology Challenges 6
1.4. Rationale 9
1.5. Silicide 13
1.6. Conclusion 14
Reference 16
2. Background: Silicide Technology 17
2.1. Titanium Silicide 19
2.2. Cobalt Silicide 22
2.3. Nickel Silicide 26
2.4. Silicidation Kinetics and Transformation 28
2.5. Material and Electrical Property 30
2.6. Transition to NiSi 31
2.7. Conclusion 32
Reference 34
3. Experimental and Analytical Technique 35
3.1. Atomic Force Microscopy 37
3.2. X-Ray Diffraction 40
3.3. Four-Point Probe: Sheet Resistivity 42
3.4. Conclusion 45
Reference 46
4. Electrical Characterization 47
4.1. Sheet Resistivity (Rs) by Four-Point Probe 47
4.2. Depth Profile by Grooving 51
4.3. Electrical Resistivity of Nickel Silicide 55
4.4. Discussions 60
4.5. Conclusion 62
Reference 64
5. Material Characterization 65
5.1. Surface Morphology by AFM 65
5.1.1. Reference Regions 66
5.1.2. Near Critical Temperature and Constant Time 67
5.1.3. Silicidation Temperature Effect 68
5.1.4. Silicidation Time Effect 69
5.2. Phase Identification by XRD 70
5.3. Phase Composition by RBS 74

5.4. Elemental Concentration by SIMS 78
5.5. Discussions 82
5.6. Conclusion 84
Reference 86
6. Closing Summary 87
Future Work 90
APPENDIX 91
1. Fabrication Process Procedures 91
2. Fabrication Process Cross-Sectional Diagram 92
3. Design of Experiment 92
4. Raw AFM Data 93
5. Raw XRD Data 95
6. Raw RBS Data 105
References 111

List of Figures

Figure	Description	Page
1.1	Cross-section model of a NMOSFET with no apply gate voltage, V_g	3
1.2.	MOS Capacitor of a NMOSFET	5
1.3	NMOS transistor cross-section prior to salicidation	10
1.4.	Schematic cross section showing various contributions to series resistance	11
1.5	Channel MOSFET with salicidation showing current flow from channel to silicide	12
2.1	$TiSi_2$ silicidation process. Not to scale	20
2.2	Sheet resistance of Co silicide as a function of temperature.	23
2.3	General $CoSi_2$ silicidation process	24
2.4	Poly N^+ sheet resistance vs. gate length for $TiSi_2$, $CoSi_2$, and NiSi silicides	25
3.1	Experimental wafer quadrant division	37
3.2	General Setup of an AFM	38
3.3	Schematic of X-Ray Diffraction	41
3.4	Typical XRD plot of intensity vs. 2θ angle	42
3.5	Four-Point Probe Schematic	43
4.1	Sheet resistivity of four regions	50
4.2	Top-down diagram of groove (a) and cross sectional view of groove and wheel	52
4.3	Calculated junction depth of four regions	53
4.4	depth profile as a function of temperature at 20sec and 60sec time	54
4.5	Calculated electrical resistivity plotted by regions	57
4.6	Resistivity as a function of RTP time at 695 °C and 573 °C	57

Figure	Description	Page
4.7	Resistivity as a function of RTP temperature	**58**
4.8	Electrical resistivity of D3 implanted regions after 2nd RTP	60
5.1	Reference AFM of doped polysilicon, nickel on doped polysilicon, and nickel on doped silicon regions	66
5.2	Surface roughness of silicide's surface around known critical temperature valued	67
5.3	RMS roughness as a function of temperature at 60sec	68
5.4	RMS roughness as a function of time at 573°C and 695°C	69
5.5	XRD intensity plot D3 prior to and after metal wet etch	71
5.6	General observed nickel silicide phase transition in doped crystalline silicon and polysilicon	74
5.7	Cross sectional view of samples sent for RBS analysis	75
5.8	Summary of RBS result with elemental ratio and RBS thicknesses	76
5.9	SIMS result for sample D15-Poly_P+.	79
5.10	SIMS result for sample D15-Si_P+.	79
5.11	SIMS result for sample D14-Poly_P+.	80

List of Tables

Table	Description	Page
2.1	Desired Properties of Silicides for Integrated Circuits	18
2.2	Comparison of Noble and Refractory Metal Silicides	19
2.3	Phase Formation Temperature and Kinetics	29
2.4	Crystal Parameters and density for IC Technology Silicide	30
2.5	Mechanical Properties of bulk silicides: compressive stress at 293K	30
2.6	Electrical Properties of bulk silicides	30
2.7	Characteristic of semiconductor silicides	31
3.1	composition of experimental wafer quadrants	36
4.1	Sheet Resistivity of samples prior to processing	48
4.2	Average sheet resistivity measured by CD ResMapper after wet etch	49
4.3	Calculated junction depth of four regions based on grooving technique	53
4.4	Calculated electrical resistivity based on R_S and junction depth data	56
4.5	Measured junction depth, R_S, and resistivity of implanted D3 regions	60
5.1	Nickel silicide phase(s) detected by XRD analysis	72
5.2	Calculated silicide thickness based on single-phase density and RBS thickness compared to thicknesses from groove technique.	77
5.3	Detected film layer from surface down through SIMS analysis	81
6.1	Result Summary	88
6.2	Conclusion Summary and Optimal Condition	89

1. Introduction/Motivation

Metal silicidation has been and continues to be an important technology in the semiconductor industry. This thesis will focus on the formation of NiSi in particular. In this chapter, the author presents a brief overview of the integrated circuits and transistors to explain the rationale and requirements for this material.

An integrated circuit (IC) is a "circuit in which many elements (transistors, diodes, and resistors) are fabricated and interconnected on a single chip of semiconductor material" [1]. The IC industry has experienced tremendous growth since the invention of the first bipolar transistor in 1947 [10]. The growth of this industry has given rise to numerous technological advances that have influenced the way people live and work. Such impact is most evident in the fields of communication (mobile phones), education (computers) and entertainment (DVDs).

The continuing growth of the IC industry is maintained by the continued scaling (shrinking) of transistors to smaller dimensions. The benefits of transistor size reduction are faster circuit speed, lower power consumption and higher packing density. However, the continuation of transistor scaling in modern technology presents numerous challenges. The most obvious is the limitation of the conventional optical lithography system and the increase in the transistor series resistance. Future IC technology advances require imaging of smaller and sharper features that are at or beyond the capability of the imaging system. Moreover, at smaller transistor dimensions, many phenomena that were once negligible begin to take the dominant role in influencing the transistor's characteristics. Such examples can be seen in the transistor series resistance where the

importance of the materials property begins to be more crucial than the device's geometry with decreasing transistor size.

The following chapter will provide a quick synopsis of the semiconductor industry. This includes the fundamental operation of a metal oxide semiconductor field effect transistor (MOSFET). The chapter will also introduce several major challenges faced by the industry in the fabrication of the MOSFET device as its dimensions continue to scale down. Specifically, this chapter, as well as all subsequent chapters, will focus mainly on issues related to the transistor's series resistance since coverage of all challenges in fabricating a scaled down MOSFET would be impractical.

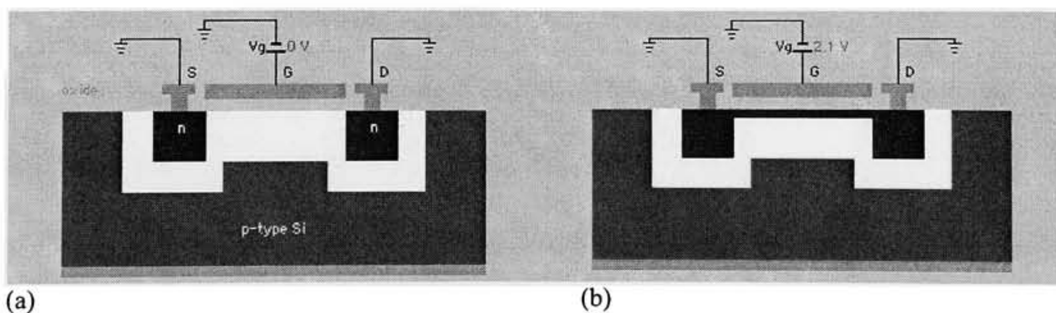
1.1. Integrated Circuit Technology Overview

The origin of the integrated circuit technology began in 1940 with the development of the PN junction by Russel Ohl at Bell Labs [10]. The PN junction is merely two materials with dissimilar electrical property, such as electron charges, that are in intimate contact (near perfect contact) with each other. The PN junction developed at the time was capable of producing 0.5 volts when exposed to light due to the recombination-generation of charge carriers. In 1947, Bardeen, Brittain, and Shockley at Bell Labs [10] invented the first 3-terminal semiconductor transistor. The transistor was initially known as a point-contact "transfer resistance" device since its operation is nothing more than a transfer of resistance from one terminal to the others. Due to the complexity in producing the point-contact transistor, in 1951 Shockley developed the junction transistor. The junction transistor quickly became the essential component of all electronic devices such as the telephone, radio, and other electronics.

In 1955, Bell Labs successfully fabricated the first field effect transistor (FET). The FET sparked the birth of the IC technology in 1958 when Kilby, from Texas Instruments, successfully built a "simple oscillator IC" consisting of 5 integrated components. Further advancements were made in 1959 when Noyce introduced "planar technology" from Fairchild [10]. Noyce produced the integrated circuit by combining the P and N junctions silicon separated by a layer of silicon dioxide (SiO_2), developed by Hoerni and Lehovec [2], with a process of evaporating a thin layer of metal over the circuit. The evaporated metal layer was then etched into pattern to create the integrated circuitry. This idea and processing technique is the primary method of fabricating complex MOSFET integrated circuits seen today.

1.2. MOSFET Fundamentals

A MOSFET, metal-oxide-semiconductor field-effect transistor, is the building block device in today's electronic circuits. Typically, a MOSFET consists of two electrically active regions, a source and a drain, that are selectively connected by a channel of n-type or p-type semiconductor material. Refer to Fig. 1.1 for detail. The three terminals, source, gate, and drain, are labeled as S, G, and D respectively.



(a) (b)

Fig. 1.1. Cross-section model of a NMOSFET with no apply gate voltage, V_g, (a) and with an apply gate voltage, V_g, equals to the threshold voltage, V_t, (b). An electrically conductive channel is induced when the $V_g = V_t$ in (b). Image adopted from [4].

The source and drain are highly doped regions in the silicon wafer. Doping is a method of altering the conductivity of a semiconductor material by the additions of impurities. Certain impurities contain an extra valence electron relative to the valence structure of Si. These impurities have low activation energy and at room temperature contribute these excess electrons to current transport. These impurities are termed "donors"; A Si lattice doped with a donor such as Phosphorus is termed to be **n-type** dopant. Similarly, a "*p-type*" semiconductor contains impurities with one less valence electron relative to the Si lattice. This absence of an electron mathematically behaves as a positive charge and is commonly referred to as a hole. Typically, Boron is used as the **p-type** dopant for Si. The dopants, boron or phosphorus, are usually ion implanted into the semiconductor wafer by the use of high-energy ion implantation technique. The type of dopant implanted into the source and drain regions depends on the type of MOSFET that has been fabricated. A n-channel MOSFET, NMOSFET, uses n-type dopant whereas a p-channel MOSFET, PMOSFET, uses p-type dopant. The source and drain regions are separated by a region of normal semiconductor silicon which provides for the electrical isolation. On top of the isolating semiconductor silicon is a thin stack of metal (typically heavily doped polysilicon) layer above an isolating silicon dioxide layer. Together, the three layers stack (polysilicon, oxide, and silicon) forms the metal-oxide-semiconductor, MOS, gate capacitor. The polysilicon is normally doped with the same dopant type as the source and drain regions.

The operation of the MOSFET is controlled by the application of voltage on the MOS gate capacitor, V_g. Assuming a NMOSFET device in Fig. 1.1, its operation is as follows. In a NMOS transistor, the silicon semiconductor layer below the gate is p-type which is

rich in excess holes, while the polysilicon is rich in excess electron, n-type. When a positive voltage is applied on the polysilicon gate, an electric field is created across the thin oxide layer. A positive voltage on the polysilicon gate induces the concentration of electrons near the interface of oxide-silicon by pushing all the holes away from the interface. This is commonly known as the depletion stage since the concentration of holes near the oxide-silicon interface in much lower than that of the p-type silicon layer. The depletion of holes near the interface results in an induced n-type channel near the oxide-silicon interface, a condition defined as $V_g = V_t$ where V_t is the threshold voltage. The threshold voltage of a MOSFET is usually defined as the gate voltage where an inversion region forms in the substrate (semiconductor silicon) of the transistor. With higher positive voltage on the gate, a well-defined n-channel is established to provide a direct connection between the source and the drain regions. This condition is known as the *inversion stage* where electrical carriers, electrons for n-channel, can flow from the source region to the drain region to set up an electrical current flow from the drain to the source (current flow in opposite direction of electrons flow) if a voltage bias (V_d or drain voltage) is applied between the two regions. The inversion stage defines the on-state of a MOSFET where $V_g >> V_t$. Refer to Fig. 1.2. The MOSFET can be turned off when $V_g < V_t$ which removes the induced channel connecting the source to the drain.

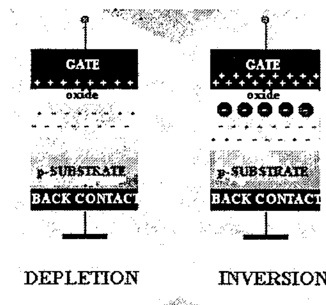


Fig. 1.2. MOS Capacitor of a NMOSFET [4].

1.3. IC Technology Challenges

Over the past decades, the MOSFET device has continually been scaled down in size to fulfill Moore's Law. Typical MOSFET channel lengths 20 years ago were several micrometers whereas modern MOSFET channel lengths are in the tens of nanometers. The origin of Moore's Law came from Gordon Moore's observation made in 1965 that the number of transistors per IC increases as an exponential function, doubling about every year. However, he later modified the observation in 1975 stating that the number of transistors per IC doubles about every two years. This final observation has been true ever since and has been known as Moore's Law.

Why do MOSFET need to be scaled down in size? The most important reason for MOSFET scaling is to increase the operation speed of the transistor. Smaller MOSFETs enable more current to pass through the induced channel. In the linear mode, MOSFET is like a resistor. In saturation, on-state, the MOSFETs behaves as a current source. The resistance arises along the path of the current traveling from the drain through the induced channel and to the source. A shorter resistor has a shorter channel length MOSFET and less resistance and thereby more current flow. In addition, a smaller MOSFET has smaller gate, and thus smaller gate capacitance. Therefore, the higher current flow and smaller gate capacitance contribute to a higher processing speed and lower switching time of a MOSFET. Another important reason for scaling down is to obtain higher MOSFET packing density and lower fabrication cost. Reducing the channel length size allows a higher number of MOSFETs to fit in a fixed area. The resulting effect is smaller chip size or chips with higher processing power on the same chip area.

Therefore, the cost of fabrication is lower since more chips can fit into the same wafer or chips with higher processing power and price.

Since the invention of the MOSFET, the difficulties in satisfying Moore's Law have been in the fabrication process capability. The industry is constantly battling with the difficulty of developing new tools and processes that would enable them to continue decreasing the size of the MOSFET, thereby increasing the MOSFET density per IC and fulfilling Moore's Law. Currently, the IC industry is capable of fabricating MOSFET with channel lengths as small as 90nm.

However, the fabrication process capability is becoming less of a major challenge in today's MOSFET scaling. The material related issue is becoming more of a concern for the industry in further scaling advances. Continuing advancement in IC technology is faced with material related issues ranging from the dielectric breakdown of the ultra thin gate oxide insulator to the increase in series resistance of the source/drain and the increase in resistance of the doped polysilicon gate. The primary requirement of a gate material is that it must be a good conductor. At the birth of the transistor, metal gate was the ideal material; however, metals have high work function differences compared to silicon. With such high work function differences, a higher gate voltage must be applied to overcome the difference and induce a channel in the silicon substrate. This does not meet the criteria for MOSFET scaling since the applied voltage must also scale down with size to limit power consumption and heating. Therefore, a polysilicon gate was used to substitute for metal. Highly doped polysilicon is an acceptable conductor since it has the same chemical composition and similar work function as silicon.

Polysilicon is an acceptable gate material in previous IC technology. However, it is highly resistive (about 1000X more resistive) compared to metals. Even with high doping levels, its sheet resistance is still significantly higher than metals. This was not a major concern in previous IC technology where the polysilicon gate is relatively large. It is a well-known fact that geometry plays a major role in a material's resistance such as polysilicon, also known as line-width dependence. As MOSFET size continues to decrease, the geometry of the polysilicon gate is getting smaller thereby amplifying the resistance property of the material. Therefore, a different material is needed to control the line width dependence of the polysilicon gate or to replace it altogether.

In addition, a similar challenge related to the geometry dependence nature of silicon resistance is present in the source and drain region of the MOSFET. Since the source and drain regions are essentially silicon similar to that of the polysilicon gate, the increase in resistance due to MOSFET scaling also exists. The overall source/drain resistance, known as the source/drain (S/D) series resistance, consists of several resistive components due to the geometry and stacking of different material layers in the region. The different components that make up the overall S/D series resistance will be covered in greater depth in the subsequent Rational section. However, it is clear that with smaller source and drain regions, there is a pronounced increase in the series resistance of the two regions that significantly affects the overall operation of the MOSFET.

The two major challenges addressed above can be resolved together by the introduction of a new material: metal silicide. A metal silicide is an alloy mixture of a transition metal with silicon. The alloy is easily formed when a metal, in contact with a silicon surface, is heated to a specific temperature. The heat allows the two materials to

intermix to form the alloy, commonly referred to as silicide. Metal silicide possesses material properties similar to that of silicon as well as electrical properties similar to that of a metal. Silicide retains the high melting point and hardness of silicon which allows it to withstand the various fabrication processes. It also has the low resistance property found in metal, and some silicides have low sheet resistance with no line width dependence. This makes it a suitable substitute material for the polysilicon gate.

1.4. Rationale

Metal silicidation has been and continues to be an important technique in the semiconductor industry. The most beneficial aspect of it is its self-aligning nature, often referred to as silicide-self aligned silicidation (salicide). The process of metal silicidation only occurs in regions where the metal is in contact with the silicon surface. This makes it a self-aligned process because in MOSFET fabrication, the only metal-silicon interface is in the source/drain and the gate regions. All other areas of the MOSFET are normally isolated by a thick silicon dioxide (oxide) layer. Refer to Fig. 1.3 for detail (not to scale). The metal is normally deposited several steps after the formation of the polysilicon gate over the S/D regions. Several in-between steps are needed to form the sidewall spacers between the gate and the S/D to provide the necessary electrical isolation during the silicidation process. This prevents the silicidation on the two sides of the polysilicon gate that may create a short of the entire device. The sidewall spacers are usually made of oxide. Once the spacers are in place, the metal layer is deposited to cover the entire wafer. As seen in Fig. 1.3, the only areas where the metal is in direct contact with a silicon

surface are in the S/D regions and the polysilicon gate region. Hence, these are the only regions where metal silicidation can occur which makes it a salicide process.

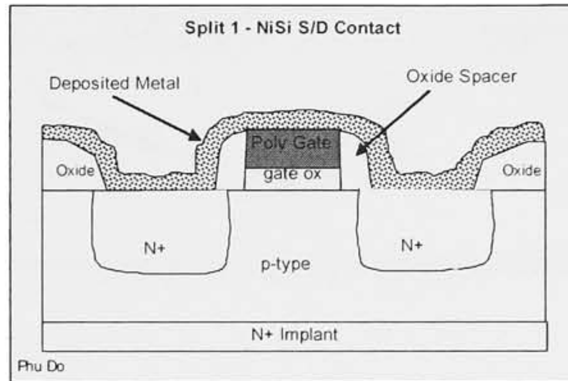


Fig. 1.3. NMOS transistor cross-section prior to salicidation.

As complementary metal oxide semiconductor (CMOS) technology progresses with decreasing dimensions and increasing devices number, metal silicidation takes on an essential role to reduce the resistance of the gate and source/drain (S/D) regions. The continuing technology advancement requires S/D and gate contacts to maintain ohmic behavior with low resistance. Source-drain series resistance degrades the current of a MOSFET, particularly on the source region as it also degrades the gate drive current. The total resistance of the source or drain region is due to the accumulation layer resistance (R_{ac}) from overlap region in the gate to S/D, resistance associated with the current spreading (R_{sp}) from the surface layer across the depth of the S/D, the sheet resistance (R_{sh}) of the S/D region, and the contact resistance (R_{co}) between metal and silicon. See Fig. 1.4.

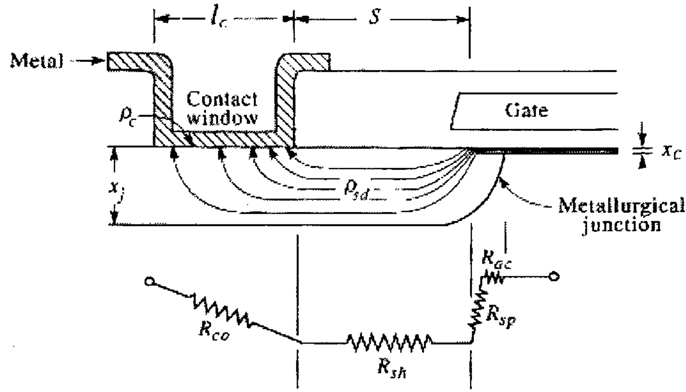


Fig. 1.4. Schematic cross section showing various contributions to series resistance [5].

Both R_{ac} and R_{sp} are not easily measurable in practice since R_{ac} is incorporated into the active channel resistance and current spreading usually takes place in a region with non-uniform resistivity due to the lateral S/D doping gradient. The sheet resistance can be accurately accounted for by equation 1.1 where *w* is the device width, *s* is the gate and contact edge spacing, and ρ_{sd} [Ω/□] is the sheet resistivity of the S/D diffusion [5].

(1.1) $$R_{sh} = \rho_{sd}\frac{s}{w} \quad [\Omega]$$

(1.2) $$\mathrm{R_{co}} = \frac{\sqrt{\rho_{sd}\rho_c}}{w}\coth\left(l_c\sqrt{\frac{\rho_{sd}}{\rho_c}}\right) \quad [\Omega]$$

(1.3) $$\mathrm{R_{co}} = \frac{\rho_c}{wl_c},\ l_c << \sqrt{\rho_c/\rho_{sd}} \quad [\Omega]$$

(1.4) $$\mathrm{R_{co}} = \frac{\sqrt{\rho_c\rho_{sd}}}{w},\ l_c >> \sqrt{\rho_c/\rho_{sd}} \quad [\Omega]$$

Equation 1.2 depicts the contact resistance, R_{co}, where l_c is the contact window width, and ρ_c [Ω-cm^2] is the interfacial contact resistivity between metal and silicon. Equations 1.3 and 1.4 represent the short contact and long contact cases of R_{co} respectively. The short contact case is driven by the interfacial contact resistance while the long contact case is driven mostly by the current flowing into the front edge of the contact.

As evident from the above discussion, S/D resistances are mainly driven by the sheet resistance and contact resistance, R_{sh} and R_{co} respectively. However, these two resistances can be reduced to a minimum with metal silicide such as $TiSi_2$, $CoSi_2$, and NiSi. An example of this is illustrated in Fig. 1.5. The sheet resistance of silicide is typically 1-2 orders of magnitude less than that of the source and drain silicon. The highly conductive silicide thin film reduces the edge spacing s to a minimum so that the only contributing sheet resistance, R_{sh} is under the spacer region. In addition, the contact resistance, R_{co}, is also reduced since the contact window width, l_c, is now the entire S/D region. This allows for the variation of the contact width to satisfy the long contact constraint in equation 1.4. The contact resistance between silicide and metal is typically negligible since interfacial contact resistivity is around $10^{-7} - 10^{-8}$ Ω-cm^{-2}. [5]

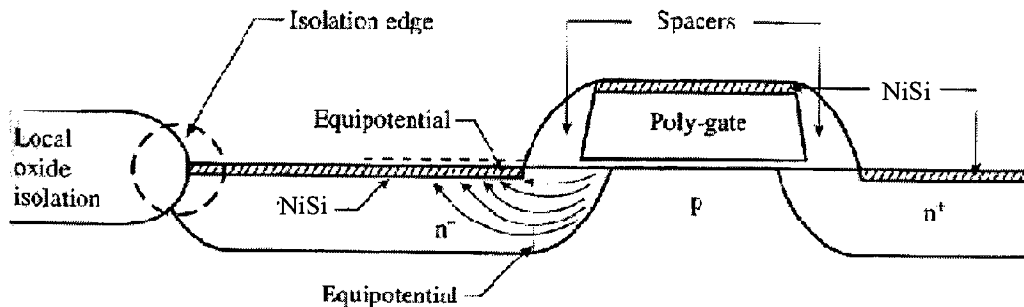


Fig. 1.5. N-Channel MOSFET with salicidation showing current flow from channel to silicide [5].

Silicide is also implemented over the polysilicon gate to provide ohmic contact to the gate as well as reducing the contact resistance with metal interconnects. However, as gate dimension continues to decrease with advances in technology, silicide resistivity begins to increase due to lack of nucleation sites. The increase in silicide resistivity contributes to the increase in gate RC delay of the MOSFET.

1.5. Silicide

Traditionally, the standard silicide materials of choice for CMOS device were $TiSi_2$ and $CoSi_2$ due to their low resistivity and high thermal stability [9]. However, as device dimension decreases with advances in technology, $TiSi_2$ resistivity begins to increase due to lack of nucleation sites caused by the incomplete phase transformation to the low resistivity C54 phase [11]. Therefore, $TiSi_2$ has been phased out with the introduction of $CoSi_2$ since it suffers no increase in resistivity with a decrease in line width. Unfortunately, the use of $CoSi_2$ is also limited by its high silicon consumption and junction leakage. The most promising alternative for future CMOS advances, especially with shallow junction, is nickel monosilicide, NiSi. NiSi has no line width dependence, a low resistivity of about 14 $\mu\Omega$-cm, low Si consumption, and a single step silicidation temperature treatment instead of a two steps silicidation required by previous silicides. The Si consumption rate due to NiSi formation is about 1nm of Ni to 1.84nm of Si, forming 2.22nm of NiSi [6]. The 2005 International Technology Roadmap for Semiconductor, ITRS, has identified the used of nickel silicide material in the ≥32nm IC technology node [7]. Its incorporation is anticipated to be mainly over the S/D regions. The ITRS report is a global assessment of the semiconductor technology. It is published by the global collaboration of the semiconductor industry leaders, researchers, and universities. The sole purpose of the report is to assess, identify, and predict current and future semiconductor technology and associated challenges.

Despite the benefits of NiSi as stated above, the main concern of Ni silicidation is the known issue of thermal instability [8]. There are mainly three phases of nickel silicide (Ni_2Si, NiSi, $NiSi_2$), each of which is characterized by dramatic differences in sheet

resistance. The silicidation process is driven by thermal energy treatment through rapid thermal processes (RTP). The highly resistive Ni_2Si formation is reported to be between 250-300°C followed by a low resistivity (~14μΩ-cm) NiSi phase at temperature between 400-550°C. At temperatures above 550°C, NiSi begins to agglomerate and transform into $NiSi_2$ which has sheet resistance twice that of NiSi [9]. A thorough investigation of nickel silicidation is needed to better understand and identify the required silicidation conditions for nickel monosilicide formation. X-Ray Diffraction (XRD) is used to obtain the silicide composition for phase identification, Atomic Force Microscopy (AFM) to study the grain structure associated with the three silicide phases, and the four point probe technique to obtain the sheet resistance of the phase(s).

1.6. Conclusion

This chapter presented a quick synopsis of the integrated circuit technology that included a brief history of the IC technology. The most basic operation of a MOSFET was discussed to provide the fundamental understating needed to ease the reading of subsequent chapters. MOSFET scaling was also covered, and the rational for such scaling was presented as well as some critical challenges the semiconductor industry must face to continue the advancement of the IC technology. However, not all challenges were discussed since they are not relevant to this thesis. The general consensus in facing the critical challenges discussed in this chapter is the need for a new material. A metal silicide was proposed, nickel monosilicide (NiSi), that potentially can address such challenges and the rational for the metal silicide was also presented.

The focus of this thesis is to investigate and characterize the formation of nickel silicide. In addition, a nickel silicide fabrication process will be developed to be compatible with RIT current CMOS processes. The main objective is to define the formation condition needed to form thin film nickel silicide with the lowest resistivity. Furthermore, its primary phase and surface topography will be identified through XRD, RBS, and AFM analytical techniques.

The following chapter will discuss the different silicides that are of most interest to the IC technology in the past as well as the current and future advances. In particular, the fundamentals of silicide formations will be covered for nickel silicide. Chapter 2 will also cover the current knowledge of the morphology, phase composition, electrical properties, and the material properties of these silicides in more detail.

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2. Background: Silicide Technology

The investigation of metal silicides can be grouped into four major categories: high temperature stability, physical properties in terms of the electronic and crystal structure, Schottky barriers and ohmic contacts in IC technology, and low resistivity silicide metallization for gates and interconnects in IC technology [1]. The current technology trend of smaller and faster devices has made the low resistivity silicide metallization the primary development focus for reasons discussed in the previous chapter.

More than half of the known metals react with silicon to form some form of silicides. However, not all are suitable for VLSI application. Most metals have at least one or more undesirable properties. Such properties include low eutectic temperature (Au and Pd) and high diffusivity in silicon, while others have high oxidation rates (Mg and Fe) and low melting points (Al and Mg) [3]. Other undesirable properties for VLSI application are the interaction of metal with silicon at temperatures less than 450°C, interaction with SiO_2, poor chemical stability, poor etchability, electromigration, and contact spiking due to diffusion as seen in Al [1]. However, there are a handful of metals with properties that are suited for VLSI application, most of which are refractory metals (group IVA, VA, and VIA) and noble metals (group VIII). The most commonly used metals are Ti, Co, and perhaps Ni as discussed earlier. The usefulness of such metal silicides for IC technology depends on many other factors besides their low resistivity. Table 2.1 shows a summary of desirable properties of silicides suited for VLSI application.

Table 2.1. Desired Properties of Silicides for Integrated Circuits [1].

1	Low resistivity
2	Easy to form
3	Easy to etch for pattern generation
4	Should be stable in oxidizing ambient; oxidizable
5	Mechanical stability; good adherence, low stress
6	Surface smoothness
7	Stability throughout processing, including high-temperature sinter, dry or wet oxidation, gettering, metallization
8	No reaction with final metal
9	Should not contaminate devices, wafers, or tools
10	Good device characteristics and lifetime
11	For window contacts – low contact resistance, minimal junction penetration

As previously mentioned, most metals suitable for VLSI application are noble or refractory metals. However, there are distinct differences between silicides formed from the two groups as seen in Table 2.2. Refractory metal silicides are more suitable for gate metallization due to their high formation temperature and stability whereas noble metal silicides are better for contacts metallization due to their low temperature formation and relatively higher Schottky barrier height.

Until now, the mainstream IC technology has successfully implemented two metal silicides into full-scale device fabrication. The earlier metal silicide was $TiSi_2$ and the more recent $CoSi_2$; $TiSi_2$ belongs to the refractory metal silicide group with high formation temperature and the dominant diffuser being silicon whereas $CoSi_2$ belongs to the noble metal silicide group with metal being the primary diffuser. $TiSi_2$ has been known to exhibit line width dependence for features below 200nm, and recently, $CoSi_2$ has been observed to show some degree of line width dependence for feature below 50nm [7]. Line width dependence is an increase in silicide's resistivity due to insufficient

nucleation sites with decreasing line width. Further reduction in device size has attracted the attention of the IC technology industry toward NiSi, a noble metal silicide with no observable line width dependence, as being the next silicide replacement for $CoSi_2$.

Table 2.2. Comparison of Noble and Refractory Metal Silicides [1].

Property	Noble Metal	Refractory Metal
Resistivity of metal	Nearly the same for all metals: 7.5 ± 2.5 μΩ-cm	Decreases with atomic number in a group and in a period
Resistivity of silicide	Nearly the same: 25 ±10 μΩ-cm. no correlation with atomic number	Increases with atomic number in a group and period
Crystal structure of silicide	No correlation with atomic number or group	Same for metals in one group; changes with atomic number of metal
Schottky barrier height (n-type Si)	Greater than half the silicon band gap energy; increases with atomic number	All have similar value, 0.55 ± 0.05 eV
Formation temperature	200-600°C	>600°C
Dominant diffuser	Metal	Silicon
Interatomic distances	$D_{M-M} < D_{M-Si}$ $D_{M-M} < D_{Si-Si}$	$D_{M-M} > D_{M-Si}$ $D_{M-M} > D_{Si-Si}$
High temperature (>1000°C) stability	Poor	Good

2.1. Titanium Silicide

Titanium silicide belongs to the refractory metal silicide group. It was the first metal silicide to utilize IC technology for low resistivity gate and interconnects applications. The well-established thin film formation process of $TiSi_2$ is a two-step thermal annealing process. The thermal annealing process may be done in a thermal furnace or a rapid thermal anneal chamber, commonly known as RTA or RTP. Typically, titanium metal is deposited onto the silicon wafer via sputtering technique. Silicon dioxide (SiO_2 - oxide) and/or silicon nitride (Si_3N_4 - nitride) are usually utilized for isolation between different

silicon regions and gate isolation since titanium generally has little or no interaction/reaction with oxide or nitride during the thermal anneal. The first thermal anneal step is usually done in a RTP chamber at temperature above 500°C in N_2 ambient. The RTP process causes the silicon to diffuse into the titanium metal to form the moderately low resistivity C49-$TiSi_2$ phase at the silicon-titanium interface and a thin layer of C54-$TiSi_2$ phase on the surface [2]. Refer to Fig. 2.1 for detail.

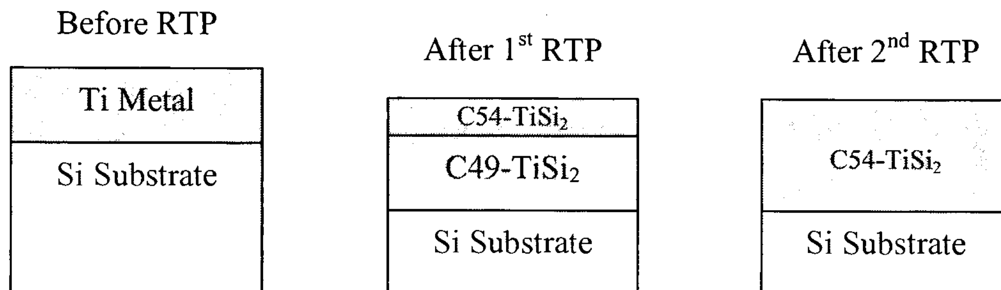

Fig. 2.1. $TiSi_2$ silicidation process. Not to scale.

Once the C49-$TiSi_2$ phase is formed, all un-reacted titanium metal is removed by the use of a wet etching chemistry consisting of 1 part H_2SO_4 and 2 parts H_2O_2 at a temperature of ~90°C for 1-2 minutes [6]. The wet chemistry only reacts to pure metals and leaves the silicide untouched. A second RTP process at a temperature of ~750°C is needed to transform the moderately low resistivity C49-$TiSi_2$ phase completely into a more stable and lower resistivity C54-$TiSi_2$ phase. However, the RTP temperature should be below 775°C to avoid the formation of TiSi, TiO_x, or TiN over the spacer regions because they are not easily etchable by standard wet chemistry. This could potentially create a parasitic circuit short between the device's regions. The resistivity of the metastable C49-$TiSi_2$ phase is about 4 times higher than the equilibrium C54-$TiSi_2$ phase with resistivity of ~11.0 μΩ-cm at 293K, which is desirable for IC device metallization [3].

$TiSi_2$ has previously been used in IC device fabrication for contact metallization due to its low resistivity, low contact resistivity to both p-type and n-type silicon, and relatively high thermal stability since $TiSi_2$ is the final stable phase of titanium silicide. Moreover, $TiSi_2$ is relatively insensitive to oxygen contamination compared to other silicides [4]. Therefore, it is best suited for atmospheric RTP processing and makes its implementation into traditional CMOS process an ease. However, as devices continue to scale down below 200nm, $TiSi_2$ begins to show certain undesirable characteristics.

During the initial C49-$TiSi_2$ phase formation, silicon in the oxide or nitride spacer can diffuse laterally across a device's' isolation regions to form a thin $TiSi_2$ layer and short out the devices, an effect known as "bridging." However, this effect can be suppressed if the thermal annealing is done in N_2 ambient, which is the case for most RTP anneals [2]. The more critical problem with $TiSi_2$ in devices smaller than 200nm is the incomplete phase transformation from the C49 to C54 phase. $TiSi_2$ phase transformation from the C49 to the C54 phase requires an activation energy of ~5.7eV on lightly doped silicon [5]. Since titanium silicidation is a nucleation-limited process, devices with features less than 200nm inherently have less available nucleation sites. This result in an incomplete phase transformation from the C49 to the C54 phase, which leads to higher resistivity compared to pure C54-$TiSi_2$. This is commonly known as the line width dependence effect as discussed earlier. One way to compensate for the line width dependence effect of $TiSi_2$ is to increase the 2nd RTP annealing temperature to create more C54 nucleation sites and complete the transformation [2]. However, the higher temperature will lead to shorts across the spacer as described previously.

The use of $TiSi_2$ for further IC technology advancement (smaller device dimension) requires additional steps, strategies, time, and labor to increase the nucleation density of the C54 phase at low temperature. Therefore, researchers and industries have shifted their focus onto a new silicide that has more promising benefits and minimal line width dependence. The new and more recent silicide of choice for the IC technology industry is cobalt disilicide, $CoSi_2$.

2.2. Cobalt Silicide

Cobalt silicide belongs to the noble metal silicide group. It has been introduced into the IC technology as a replacement for $TiSi_2$ due to possible reactions of the Ti metal with the sidewall spacers and its line width dependence behavior. Cobalt silicide has been shown to have comparable properties to $TiSi_2$ with low resistivity and the ability to withstand the selective etch of un-reacted metal. Moreover, cobalt silicide has better resistance to HF cleaning and plasma etching compare to $TiSi_2$ [8]. Similar to $TiSi_2$, the formation of cobalt silicide involves a two-step RTP annealing process with a selective metal etch in between. The metal is normally sputtered onto the wafers with oxide and/or nitride sidewall spacers and device isolations. The first RTP anneal condition is between 500°C to 675°C where the amorphous Co diffuses into the silicon to quickly form the Co_2Si phase at 350°C and immediately transforms to the metastable crystalline CoSi phase at temperatures of 500°C and beyond [3, 9]. A wet etch consisting of 3 parts HCl and 1 part H_2O_2 mixture is used to selectively remove all un-reacted Co leaving behind the CoSi [9]. A 2nd RTP anneal at temperatures between 875°C to 1000°C is needed to convert all the metastable CoSi phase to its final equilibrium $CoSi_2$ phase with resistivity

of 14.5 μΩ-cm (bulk single crystal $CoSi_2$) [9]. Fig, 2.2 shows the sheet resistance profile of cobalt metal as it transforms to $CoSi_2$.

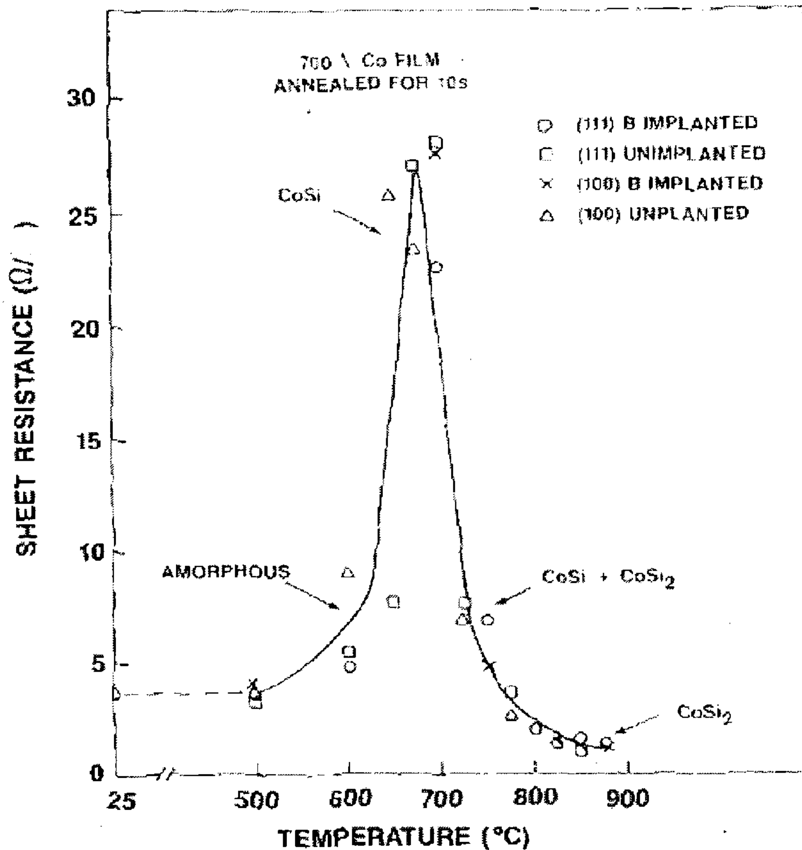

Fig. 2.2. Sheet resistance of Co silicide as a function of temperature during the two-steps anneals process. Adopted from [9].

It has been observed that the sheet resistance of the initial CoSi phase is a strong function of time at a specific temperature, and the final $CoSi_2$ phase can be achieved at lower temperatures (700°C) giving enough time (~120 seconds) [9].

$CoSi_2$ has been widely used as a replacement for $TiSi_2$ for many years since its benefits overwhelmingly resolve many issues associated with its predecessor. However,

these benefits are only realized with the use of a Ti capping layer on top of the deposited Co metal. Fig. 2.3 depicts the general cobalt silicidation process.

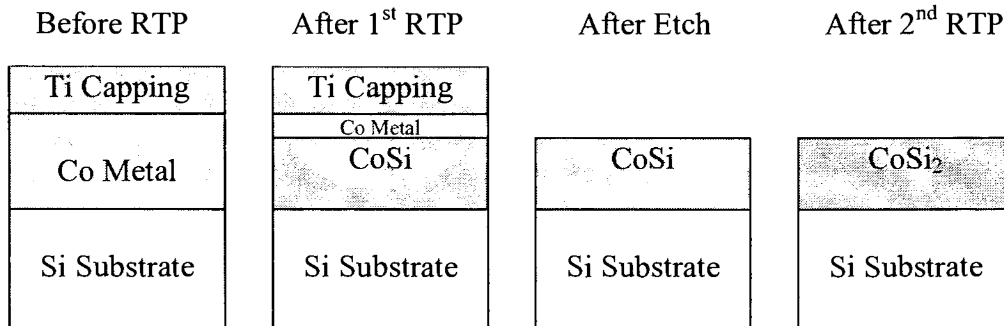

Fig. 2.3. General $CoSi_2$ silicidation process. Not to scale.

With the use of a Ti capping layer, there is minimal or no lateral silicidation observable during the annealing steps since Ti sufficiently blocks the diffusion path of Si along the Co metal surface [10]. This leads to a better self-aligned silicidation process compared to $TiSi_2$. In addition, the Ti capping layer eliminates the line width dependence associated with the transformation from Co metal to $CoSi_2$. It has been found by K. Maex that the use of a TiN capping layer resulted in a line width dependence observed as early as the first RTP annealing process for temperature below 550°C whereas the use of Ti capping layer showed no such behavior [10]. Maex also observed that a Ti capping layer reduces the interfacial oxide layer between the Co silicide-silicon interface and captures desorbed elements during the silicidation process. The interfacial oxide layer may be the inherent native oxide layer on top of the silicon surface prior to Co deposition or may be from the presence of O-elements in the RTP chamber during the silicidation process. The silicidation of $CoSi_2$ is very sensitive to traces of O_2 and moisture [10]. The Ti capping layer prevents the growth of oxide on top of the Co surface as well as further growth of any native oxide layer as the growing CoSi underneath raises it to the surface. If the

oxide layer is allowed to grow during the RTP process, the diffusion of Co through the oxide and into the Si substrate may be partially or completely blocked thereby affecting the overall silicidation process.

$CoSi_2$ undoubtedly resolves many issues associated with $TiSi_2$. However, further advances in IC technology continue to push the critical dimensions (CD) down to 45nm and below. Today, the usefulness of $CoSi_2$ is beginning to reach its limit as the IC industry prepares to manufacture devices with 65nm CD by the end of 2005 and 45nm CD within the next 5-10 years. Recent studies have shown $CoSi_2$ to have line width dependence on polysilicon gate region with CD below 50nm [7]. Although its usage is still tolerable for current device generation (65nm CD), a new metal silicide is needed to advance to the next generation device at 45nm CD.

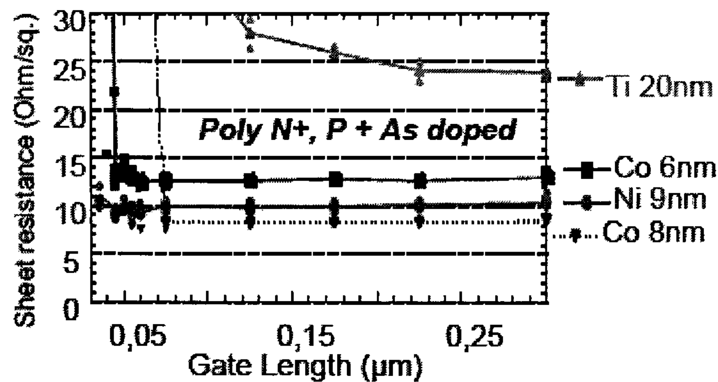

Fig. 2.4. Poly N^+ sheet resistance vs. gate length for $TiSi_2$, $CoSi_2$, and NiSi silicides. Adopted from [7].

Fig. 2.4 demonstrated the line width dependence of $TiSi_2$ and $CoSi_2$ as CD decreases beyond 45nm. As stated earlier, the line width dependence of $TiSi_2$ starts to be apparent as CD reaches beyond 200nm. Similar behavior can be seen for $CoSi_2$ as CD continues to reach below 50nm. Note however, that no such behavior was observed for nickel

monosilicide (NiSi). B. Froment has demonstrated that the use of NiSi can accommodate future generation devices with CD beyond 45nm [7]. Therefore, many researchers have turned to NiSi as the next metal silicide replacement for the IC technology.

2.3. Nickel Silicide

Similar to cobalt silicide, nickel silicide belongs to the noble metal silicide group with Ni metal being the primary diffuser. Since the use of $CoSi_2$ is limited to devices with critical dimensions above 50nm, nickel silicide has been suggested by many experts to be the next metal silicide that will enable development of smaller devices. However, the knowledge base of nickel silicide for IC application is not as vast as that of its two predecessors, $TiSi_2$ and $CoSi_2$. Its interest has only been sparked within the past several years. Therefore, there remain many ambiguous phenomena and properties to be understood prior to its successful integration into future IC devices.

The general silicidation process of nickel silicide involves a one-step RTP anneal process based on recent publication [7]. Similar to Ti and Co silicidation processes, nickel is sputtered onto silicon wafers with oxide and/or nitride sidewall spacers and isolations. However, only one RTP annealing at around 450°C is required to transform the Ni metal into the di-nickel silicide (Ni_2Si) phase which then quickly transforms into the metastable nickel monosilicide (NiSi) phase with resistivity of about 10.5 μΩ-cm [3]. Similar to cobalt silicide, nickel silicide also has an intermediate metal-rich Ni_2Si phase with formation temperatures around 325°C and resistivity of 24 μΩ-cm [3]. There also exists a third and equilibrium $NiSi_2$ phase for nickel silicide with formation temperature around 750°C and a resistivity of 34 μΩ-cm [3, 11, 12].

Since the NiSi phase possesses the lowest resistivity out of the three phases, it is obvious that this is the phase of choice for integration into future IC devices. As mentioned previously, NiSi shows no signs of line width dependence, the main reason for the phase-out of $TiSi_2$ and $CoSi_2$ in IC device advances, for CD beyond 45nm. It also has other electrical properties (refer to Electrical Properties Section) that are superior to its two predecessors in term of device operations. However, the difficulty in maintaining the desired nickel monosilicide phase and its integration into device fabrication processes has delayed its interest until recently. It is a well-known fact that the major problem with NiSi is its thermal stability. Since NiSi is not the last phase for nickel silicide, it is extremely sensitive to any temperature history above its formation temperature during subsequent processing steps. Previous device fabrication processes normally contain subsequent thermal process steps with temperatures at or above 700°C found in the metal sintering or metal reflow steps in back-end processing. Back-end processing refers to processing steps where metal interconnects are deposited and patterned to complete the necessary circuitry. These steps traditionally involve one or more high temperature annealing steps that are detrimental to the underlying NiSi. For this reason, $TiSi_2$ and $CoSi_2$ were implemented in previous and current IC technology. However, recent technological advances in metallization technology have lowered the thermal requirements for many back-end processing steps. Such reduced thermal requirements have alleviated the major obstacle of thermal stability of NiSi and made its implementation into future devices a viable possibility. The thermal stability is still a concern but the severity is much less than with prior metallization processes.

Since its renewed interest, numerous publications have been made available concerning NiSi thermal stability. It has been shown that the use of N_2^+ implantation and/or impurity in silicon can increase the thermal stability of NiSi to higher temperatures [11, 12]. Similar findings were reported for other impurities such as Pt, Pd, F, and Ti [13]. Furthermore, it has been shown that the use of a Ti capping layer has successfully increased the thermal stability of NiSi up to 700°C making its implementation closer to realization [14]. The phase formation process of nickel silicide have been confirmed by many studies; though differences exist as to the specific formation temperature of the three phases depending on the methods used, a relative range has been established for all three phases [3, 4, 7, 9, 11, 12].

The remaining sections of chapter 2 compare the material and electrical properties of Ti, Co, and Ni silicides based on previous and recent published works. A brief comparison will be made concerning the morphology, phase composition, and other material properties of the three silicides whenever data is available.

2.4. Silicidation Kinetics and Transformation

The kinetics of reactions for metal silicide fall into two main categories: diffusion-controlled kinetics and nucleation-controlled kinetics. In diffusion-controlled kinetics, the reaction between metal and silicon to form a new phase is limited by the diffusion of the dominant diffusing species toward the interface.

For $TiSi_2$, the dominant diffuser is Si whereas for $CoSi_2$ and NiSi, the dominant diffusers are the metal species. Initially, the growth rate is high since it is easier for the primary diffuser to reach the reaction interface. As the silicide continues to grow, the

primary diffuser must travel through the increasing silicide film thickness to reach the reaction interface, thus the silicide growth rate is decreased with increasing thickness. Such growth pattern is best described by a parabolic function with temperature and time being the two variables [3]. However, temperature is the most critical variable in the formation of new phases. It is possible to form new phases at lower temperatures given enough time, but extended reaction time is generally not favorable in IC fabrication since it adversely affects throughput. Diffusion-controlled kinetics is the most reproducible formation kinetics of the two categories and usually dictates the formation of metal-rich silicide phases such as Ti_2Si, Co_2Si, and Ni_2Si.

Nucleation-controlled kinetics is typically associated with high temperatures. Such kinetics occur when "the grain in free energy produced by the formation of the new phase is small and cannot compensate the additional interfacial energy associated with phase formation" [3]. Nucleation-controlled kinetics usually dictates the transformation of intermediate phase, such as NiSi and CoSi, to silicon-rich phase, such as $NiSi_2$ and $CoSi_2$. Table 2.3 shows the associated kinetics of the silicide phases and the corresponding formation temperature. Other known mechanical and electrical properties of the silicide phases are also found in section 2.5 below.

Table 2.3. Phase Formation Temperature and Kinetics [3].

	Diffusion-Limited		**Nucleation-Limited**	
Metal	**Phase**	**Temp [°C]**	**Phase**	**Temp [°C]**
Ti	$TiSi_2$	425	$TiSi_2$	-
Co	Co_2Si	350	-	-
	CoSi	350	-	-
	$CoSi_2$	400	$CoSi_2$	500
Ni	Ni_2Si	200	-	-
	NiSi	275	-	-
	$NiSi_2$	350	$NiSi_2$	800

2.5. Material and Electrical Property

Table 2.4. Crystal Parameters and density for IC Technology Silicide. Adopted from [3].

Silicide Compound	Crystal System	Lattice Constant a/b/c [Å] a	b	c	Density [g/cm^3]
Ti	Hexagonal	2.950	-	4.686	4.504
TiSi	Orthorhombic	6.544	3.638	4.997	4.24
C49-$TiSi_2$	Orthorhombic	3.62	13.76	3.61	3.85
C54-$TiSi_2$	Orthorhombic	8.2687	8.5534	4.7983	4.07
Co	Cubic	3.5446			8.789
Co_2Si	Orthorhombic	4.918	3.737	7.109	7.42
CoSi	Cubic	4.447	-	-	6.65
$CoSi_2$	Cubic	5.3640	-	-	4.95
Ni	Cubic	3.541	-	-	8.91
Ni_2Si	Orthorhombic	7.060	4.990	3.720	7.40
NiSi	Orthorhombic	5.233	3.258	5.659	6.56
$NiSi_2$	Cubic	5.406	-	-	4.859

Table 2.5. Mechanical Properties of bulk silicides: compressive stress at 293K, melting point, and thermal linear expansion coefficient (α). Adopted from [3].

Silicide Phase	Compressive Stress σ_{comp} [MPa]	Melting Point [°C]	α [10^{-6} K^{-1}]
Si		1414	2.6
$TiSi_2$	117.9	1500	18.89 ± 0.55
CoSi	38	1460	11.1 ± 1.0
$CoSi_2$	100	1326	9.469 ± 0.18
Ni_2Si	316	1306	16.5
NiSi	158	992	-

Table 2.6. Electrical Properties of bulk silicides. Adopted from [3].

Silicide Compound	Resistivity [μΩ-cm]
C49-$TiSi_2$	60
C54-$TiSi_2$	15
Co_2Si	110
CoSi	147
$CoSi_2$	15
Ni_2Si	24
NiSi	10.5
$NiSi_2$	34

2.6. Transition to NiSi

As discussed earlier, the three metal silicides of interest to the semiconductor industry have numerous similarities and differences in characteristics. Some characteristics are favorable while many are not in terms of process integration. Overall, NiSi seems to possess the most favorable characteristics over its predecessors: $TiSi_2$ and $CoSi_2$. The most crucial fact that makes NiSi most favorable is because the use of the other two silicides have reached their limits due to technological advances. The benefit of low resistivity associated with these traditional silicides can no longer be maintained as device size decreases beyond 50nm. Table 2.7 details some major characteristics of the three silicides of interest.

Table: 2.7. Characteristic of semiconductor silicides [1-15].

Characteristics	**Titanium Silicide ($TiSi_2$)**	**Cobalt Silicide ($CoSi_2$)**	**Nickel Silicide (NiSi)**
Formation Temperature (°C)	900	900	500
2-Steps Anneal	Yes	Yes	No
Resistivity (μΩ-cm)	13-16	16-20	14-20
Primary Diffuser	Si	Co	Ni
Prone to Bridging Effect	*Yes*	*Yes*	*No*
Line Width dependence	*Yes*	*Yes**	*No*
Silicon Consumption	*High*	*High*	*Low*
Thermal Stability	Good	Good	Poor
Junction Current Leakage (Interface Spike)	High	High	Low

*For dimension < 50nm [15]

As evident from Table 2.7, NiSi seems to be the only silicide, out of the three, capable of enabling further device scale-down. Its formation requires much less thermal energy as well as less time due to its single step annealing. Furthermore, NiSi has much lower junction current leakage due to interface spike, and its resistivity is comparable to that of its predecessors. However, the most crucial characteristics of NiSi that enable its usability are resistance to the bridging effect, low silicon consumption, and resistance to the line width dependence effect. These are the three characteristics that $TiSi_2$ and $CoSi_2$ lacked, and the reasons that sparked the industry's interest in NiSi.

2.7. Conclusion

Numerous metal silicides exist, yet not all are well suited for IC device fabrication. Based on the current knowledgebase of the IC industry, only a handful of metal silicides are useable. In addition, these useable silicides have a short lifespan in the IC technology industry as further advances push the silicides to their limit. The technological advances have far surpassed the limit of $TiSi_2$ and are closely approaching the limit of today's silicide ($CoSi_2$). Therefore, there is an urgent need to research the next metal silicide to enable further technological advancement. Based on previous studies, nickel monosilicide appears to be the optimal candidate. Preliminary experiments have shown its capability to be beneficial to current and future IC technology. However, the current knowledgebase on NiSi is limited. Many of its characteristics are not fully comprehended or require further verification. Therefore, it is the intention of this thesis study to verify some reported characteristics of NiSi while attempting to gain a better understanding of its behavior and contribute to its current knowledgebase. In addition, another intention of

this study is to establish a nickel silicides knowledgebase for the Semiconductor & Microsystems Fabrication Laboratory (SMFL) at RIT. Such knowledgebase will include processing conditions of nickel silicides based on RIT current processing tool set.

This study will systematically investigate the silicidation process of nickel silicide based on the two most critical parameters reported in previous researches: silicidation temperature and silicidation time. The following chapter will cover the experimental and analytical technique used to investigate the silicidation process of nickel silicide. Detailed discussions will be given wherever necessary to provide a better understanding of the experiment.

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3. Experimental and Analytical Technique

The study of nickel silicide is intended to be a process development study to confirm and gain better insight into the silicidation process of nickel metal in semiconductor processing conditions. Therefore, all experiments were done on blanket silicon wafers. These are standard 150mm p-type (boron dopant) silicon wafers with an initial electrical resistivity in the range of 25-45 Ω-cm (sheet resistivity of 382-687 Ω/□ based on an average wafer thickness of 655μm).

Each wafer was divided into four primary quadrants, each having a different material composition. Table 3.1 shows the content of each quadrant in detail. With the wafer flat oriented on top, three general regions could be seen going from left to right. The left region consisted of single crystal silicon with a thickness equals to the thickness of the wafer, and it represents the silicon source/drain of a transistor. The right region consisted of a 200nm polysilicon layer, on top of a 41nm silicon dioxide layer, on top of the single crystal silicon wafer. This 3-region stack represented the poly MOS (metal oxide semiconductor) gate of a transistor. In between these two regions was a 1200nm thick silicon dioxide region. This oxide was used primarily as a separation region between the silicon and polysilicon regions. Looking at the wafer from top to bottom, the upper half of the wafer was doped, by ion implantation, with P^{+31} at 75KeV and dose of 2E15 atoms/cm^2. This was to mimic the heavily doped source, poly-gate, and drain regions of the transistor. The lower half of the wafer did not receive any additional doping. See Fig. 3.1 for details.

The establishment of these quadrants and separation regions was followed by a wet chemical clean process, Radio Corporation of America (RCA) Clean Process, to remove

any organic/inorganic contaminations. To ensure proper removal of oxide on the silicon and polysilicon regions, an additional HF immersion was done for 10-15 seconds prior to nickel metal deposition. An average of 335nm of 99.9% purity nickel metal was deposited onto the wafers by DC sputtering, and each wafer was RTP annealed at a different temperature and time based on the design of the experiment in the Appendix section. Any un-reacted nickel metal not consumed during the RTP anneal was selectively removed by wet chemistry; 1 part H_2SO_4 : 2 part H_2O_2 at 90°C.

All four quadrants of each wafer were analyzed by Atomic Force Microscopy (AFM) for surface topography, X-Ray Diffraction (XRD) for silicide composition, and four-point probe technique for sheet resistance. These measurements were taken before and after the nickel silicidation process. This chapter will briefly cover the fundamental principles of the three analytical techniques used at RIT: AFM, XRD, and four-point probe technique. Several samples with crucial silicidation conditions, as identified by literature, were also sent out for secondary ion mass spectroscopy (SIMS) and RBS analysis to complement the "in-house" analytical techniques.

Table 3.1. Material composition of experimental wafer quadrants.

Quadrant	ID	Material Composition	Avg. Thickness (nm)	Additional Implant Dose
Upper Left	Si_P+	Si	Substrate	2E15 cm^{-2} P^{+31}, 75KeV
Lower Left	Si_N	Si	Substrate	N/A
Lower Right	Poly_N	Poly/Oxide/Si	200/41/Substrate	N/A
Upper Right	Poly_P+	Poly/Oxide/Si	200/41/Substrate	2E15 cm^{-2} P^{+31}, 75KeV

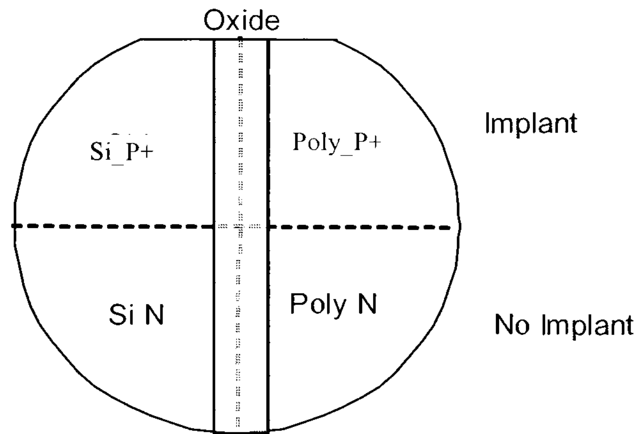

Fig. 3.1. Experimental wafer quadrant division.

3.1. Atomic Force Microscopy

The atomic force microscope (AFM) belongs to the class of scanned-proximity probe microscopes. This class of microscopes utilizes a probe or a tip placed very close to the surface of a sample to measure the attractive or repulsive force between the probe and the sample. Since scanned-proximity probe microscopes do not utilize lenses as seen in optical microscope and scanning electron microscope, the major resolution limitation lies in the size of the probe.

Atomic force microscopy is typically used to investigate the surface topography of a sample. Unlike other microscopy, AFM gives the most accurate representation of the sample's surface with atomic level resolution. Such resolution is capable of resolving the grain sizes and shapes as well as the surface roughness of a sample. An AFM consists of 5 essential components: a microscopic tip attached to the cantilever, a scanner, a laser, a photodiode detector, and a data processor unit. Refer to Fig. 3.2 for details.

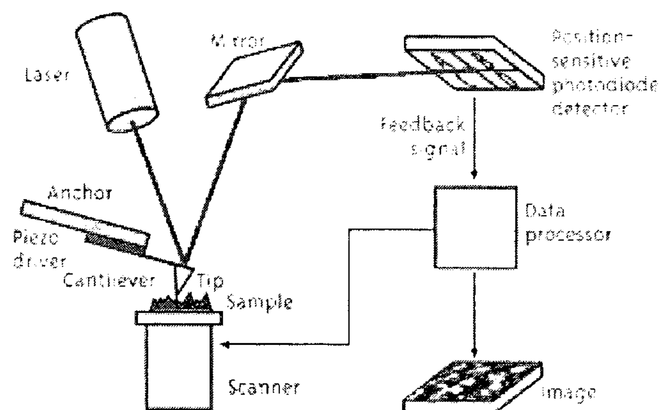

Fig. 3.2. General Setup of an AFM [1].

There are two major modes of analysis possible on an AFM: one with a feedback mechanism and one without. A microscopic tip-cantilever assembly is scan over a sample's surface with feedback mechanisms that enable a piezoelectric scanner or a piezoelectric cantilever driver to maintain the tip at a constant force above the sample's surface to obtain height information. The tip can also be controlled to maintain a constant height above the sample's surface to back out force information associated to the sample-tip interactions. The tip is usually made from Si_3N_4 or Si, and extends down from the end of a cantilever. An optical detection system is normally used to measure any changes in the cantilever as it is scanned across the sample. The upward or downward movement of the cantilever due to the contour or interaction with the sample's surface causes an angular deflection of the laser beam. This deflection is detected by the position-sensitive photodiode detector consisting of two side by side photodiodes. The detector system measures the difference between the two photodiodes signal intensities which indicates the deflection of the cantilever, and the information is converted to a voltage signal that can be processed by the data processor. The data processor provides feedback

information to the scanner to maintain the constant force or height of the cantilever-tip assembly. The three dimensional surface topology can be constructed based on the deflections of the cantilever and the feedback changes necessary to maintain the constant force/height of the cantilever.

The most typical use of the atomic force microscope is to analyze the surface morphology of a sample such as grain size, grain structure, surface porosity, surface height, and surface roughness. In addition, it may also be used to analyze differences in a material's surface properties such as elasticity, charges, and magnetism. More advanced uses of the tool include identification of transitions between different components in polymer blends and composites through Lateral Force Microscopy (LFM), and the detection of variations in sample's composition, adhesion, friction, viscoelasticity, and surface hardness through the used of Phase Contrast Mode (PCM) imaging. Many other modes of operation exist that can be used to study different material properties. Three of the most basic and commonly used modes are contact mode, tapping mode, and non-contact mode. See the Appendix section for discussions on the many different AFM modes of operation.

For this study, the AFM was used to measure the surface topography of the sample using the tapping mode. The primary interest was in the surface roughness and grain size of the film. A Veeco Dimension 3000 Scanning Probe Microscope (SPM) was used for all surface morphology analysis. The Dimension 3000 SPM utilizes automated atomic force microscopy (AFM) and scanning tunneling microscopy (STM) techniques to measure surface characteristics. No special surface preparations were done on any samples prior to the analysis. All samples were air cleaned using a commercial nitrogen-

based air duster product. A Veeco OTESPA silicon probe-tip assembly, with a tip radius of 7nm, was used for all measurements in room temperature at atmospheric conditions [5]. Refer to Chapter 5 for AFM results and analysis.

3.2. X-Ray Diffraction

X-rays are short wavelength electromagnetic radiations produced due to decelerating charged particles such as electrons. A X-Ray Diffraction (XRD) tool typically consists of a monochromatic x-ray generating source, an x-ray detector, and a data processor. In the x-ray generating source, a high voltage draws electrons from the anode to the cathode metal target. The incoming electrons bombard the metal target and excite its electrons to higher energy band for short period of time. X-rays are generated when these electrons return to their normal states and are radiated in all directions. The emitted x-rays are then directed toward the sample, which generally causes scattering. Most scattered x-rays interfere destructively and eliminate themselves. However, diffraction does occur when the scattered x-rays are in phase with other scattered rays from atomic planes. This condition is known as the Bragg condition in which the reflected rays interfere constructively. Equation 3.1 shows the Bragg law which satisfies such a condition. In this equation, "d" represents the lattice interplanar spacing of the crystal, θ is the x-ray incident angle, and λ is the wavelength of the characteristic x-ray. Different materials have unique atomic structures that give them unique x-ray diffraction characteristic patterns.

(3.1) $$2d \sin\theta = \lambda_o$$

To capture all possible diffractions from a sample, the sample is placed in the center of a graduated circle with x-ray detector situated on the circumference. Non-diffracted radiations are limited from the x-ray detector by the use of divergent slits between the x-ray source and the sample as well as from the sample to the detector. This is to reduce background noise and collimate the radiation. Refer to Fig. 3.3 for details.

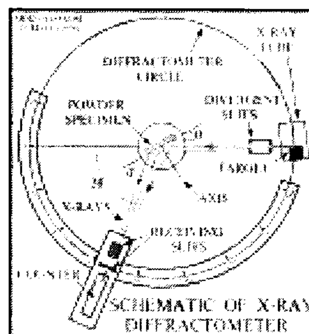

Fig. 3.3. Schematic of X-Ray Diffraction [2].

Signals from the x-ray detector are typically filtered by a pulse-height analyzer scaled to measurable proportions, and the filtered signals are sent to the linear ratemeter to convert into electrical currents that can be recorded or analyzed [2]. Typically, the final information obtained from the processor will be an intensity vs. 2θ plot. This processed information shows peaks due to one or more crystalline phases. From this plot and other reference sources, phases (and the relative phase composition) in the silicide film can be identified. Refer to Fig. 3.4 below.

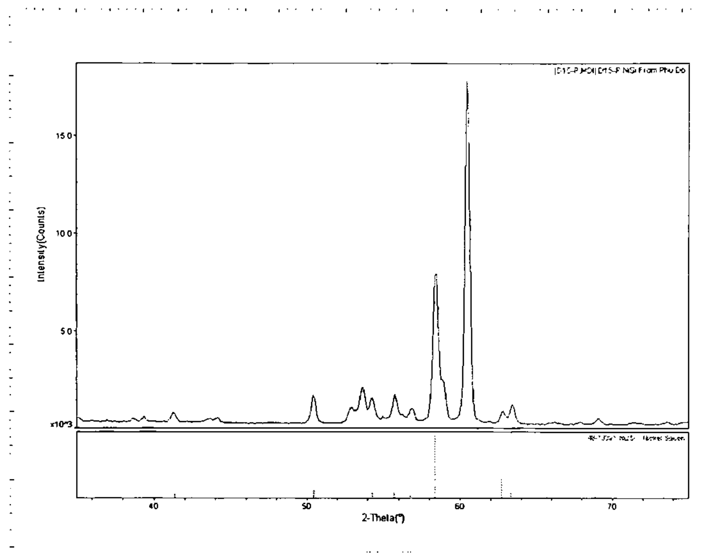

Fig. 3.4. Typical XRD plot of intensity vs. 2θ angle [3].

The Rigaku DMAX-IIB XRD system was used to analyze all samples at room temperature and in atmospheric pressure. All measurements were taken using a Cu radiation source ($K\alpha_1$ = 1.540562 Å, $K\alpha_2$ = 1.544390 Å) at 40 kV and 35 mA. The scan angle varied from 30° 2θ to 120° 2θ with a step size of 0.01° and at a rate of 1.5°/min. Refer to chapter 5 for XRD results and analysis.

3.3. Four-Point Probe: Sheet Resistivity

A four-point probe system consists of four contact needles, separated by a distance "*s,*" aligned linearly. Refer to Fig. 3.5 for detail. A direct current is apply to probe 1 across the substrate or film and measured on probe 4. As the current travels across the film, potential drops occur due to the internal resistance of the film. These potential differences are measured by probe 2 and 3. From the voltage and current measurements along with the film thickness and probe spacing (s), the resistivity can be calculated based on equation 3.2 through 3.5 below.

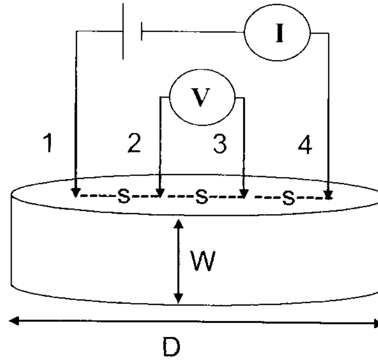

Fig. 3.5. Four-Point Probe Schematic.

* All units are in (Ω - cm)

(3.2) $$\rho = 2\pi S\left(\frac{V}{I}\right)$$ $W >> S, \quad D >> S$ (thick film)

(3.3 $$\rho = \frac{2\pi S\left(\frac{V}{I}\right)}{K}$$ $0.01 < \frac{W}{S} < 10$ (moderately thick film)

(3.4) $$K = 1 + 4\sum_{n=1}^{\infty}\left(\left[1+\left(\frac{2nW}{S}\right)^2\right]^{-1/2} - \left[2^2+\left(\frac{2nW}{S}\right)^2\right]^{-1/2}\right)$$

(3.5) $$\rho = \frac{\pi}{\ln(2)}W\left(\frac{V}{I}\right)$$ $W << S, \quad D << S$ (thin film)

Equations 3.2 through 3.5 show the resistivity relationship for different film thickness range (W) and sample diameter (D) at constant probe spacing (S = 0.0625" = 0.15875cm) [4]. For thick film, equation 3.2 assumes that the film thickness and sample diameter are much greater than the probe spacing. Ideally, the slope of a resistivity curve should be zero since the resistivity of a material should be constant. However, this ideal resistivity was based on the assumptions that the diameter and thickness were infinitely wide to

account for the hemispherical current distribution from probe 1. To condition the ideal case to a finite diameter and thickness, a geometric correction factor is necessary. Equation 3.3 represented the resistivity for moderately thick film. With probe spacing of 1587.5μm, moderately thick film would be between 15.88μm to 15,880μm. Due to its modified boundary conditions, the geometric correction factor K is use in this equation to account for the non-ideal case of equation 3.2. Since thickness in equation 3.3 is a finite thickness with value comparable to the probe spacing, equation 3.2 can no longer be used for this case. Finally, equation 3.5 shows the resistivity formula for thin film with thickness and sample diameter much less than the probe spacing of 0.15875cm. For this equation, the correction factor was replaced by the thickness itself to better represent resistivity under such extreme boundary. All measurements were done for this study in this regime.

The four-point probe system used was a CD Automatic ResMapper with a probe spacing of 0.15875cm. The system is capable of outputting both sheet resistance (also known as sheet resistivity) and resistivity. Resistivity (Ω-cm) is a unique electrical property of a material, whereas the sheet resistance (Ω/□) is only the resistivity of a material per square centimeter area. The electrical resistivity requires the needs to know the material's thickness, assuming a single phase composition exist, whereas the sheet resistance does not. Since the silicide thickness was not known for each sample, the four-point probe system reported all measurements in Ω/□ (sheet resistance). All measurements were done in room temperature at standard atmospheric pressure. Refer to chapter 5 for four-point probe results and analysis.

3.4. Conclusion

This chapter covered the experimental procedures and the analytical analyses used for the study of nickel silicidation. The complete processing steps can be found in the Appendix section. The following two chapters will cover the results and analysis of the study. Chapter 4 will cover the electrical characterization of the nickel silicidation process. Chapter 5 will provide detailed analysis and discussion of the material characteristics of nickel silicidation.

Reference

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4. Electrical Characterization

The electrical characterization of this study was done through four-point probe technique to investigate the electrical resistivity of nickel silicide. Resistivity of a material requires prior knowledge of its thickness. Since the silicide's thickness was under investigation in this study, its resistivity must be indirectly calculated. The CD ResMapper was used to measures the sheet resistivity of all samples before the nickel deposition and after the nickel silicidation process. As mentioned earlier, the sheet resistivity represents the resistance of the silicide film per square unit (Ω-cm/cm or Ω/□). This information alone was not sufficient for phase to phase comparison of the silicide's resistivity. The depth profile from the grooving technique was also needed to enable such comparison. This chapter presents the sheet resistivity results collected from the four-point probe technique and the silicide depth profile from the grooving technique. These two pieces of information were used to calculate the electrical resistivity of the silicide film.

4.1. Sheet Resistivity (Rs) by Four-Point Probe

The sheet resistivity (Rs) of all samples was taken at several steps of the fabrication process. Measurements were taken prior to any processing to obtain the bulk silicon sheet resistivity value, post dopant activation anneal, post nickel metal deposition, post RTP anneal, and post wet etching of un-reacted nickel metal. Table 4.1 shows the average sheet resistivity of the bulk silicon wafer prior to any processing. The corresponding electrical resistivity was also calculated base on the measured thickness of the wafer at 550μm. The average resistivity was 30.3826 Ω-cm which is within the manufacturer

specification of 25 – 45 Ω-cm. Table 4.1 also shows the average sheet resistivity of sample D12 after the removal of thermally grown oxide during the dopant activation anneal process. This step was immediately before the nickel metal deposition. Since all samples at this part of the fabrication received identical processing, the sheet resistivity in each region of D12 was taken to be the same for all samples respectively. Notice the unknown value for the Poly-N region. The dashes indicate the values were beyond the measurable limit of the CD ResMapper. The sheet resistivity of the Poly-N region was too high above the maximum limit of the tool. This was expected since the region did not receive any doping, and non-doped polysilicon was known to be an insulator. In addition, no meaningful measurements were obtained for the Si_P+ region on all samples. This region was highly doped with P^{+31} dopant at $2x10^{15}$ atoms/cm^2.

Table 4.1. Sheet Resistivity of samples prior to processing and nickel metal deposition.

Region	Avg. R_S (Ω/□)	Std. Dev. (Ω/□)	Avg. ρ (Ω-cm)
Prior to Processing			
Bulk Si	552	3	30.4
Post Dopant Activation Anneal			
Poly_P+	532	7	-
Poly-N	-	-	-
Si-N	638	9	-
Si_P+	-	-	-

The average sheet resistivities for the different regions are shown in Table 4.2. The average value was calculated base on six (6) measurement points in each respective region. These measurements were taken after the wet etching of un-reacted nickel metal. Each sample was etched individually for 60 seconds at 90°C. The bath consisted of 30mL of H_2SO_4 and 60mL of H_2O_2. It was observed that the etching of sample D3 showed a dark discolored cloud above the sample's surface. This seemed to indicate there was un-

reacted nickel metal remaining after the silicidation process. This fact was confirmed by XRD and RBS analysis techniques in chapter 5. All other samples showed no visible discolorations during wet etch.

Table 4.2. Average sheet resistivity measured by CD ResMapper after wet etch.

Average Sheet Resistivity (Ω/□)						
Wafer ID	**Temp [°C]**	**Time [sec]**	**Si_P+**	**Si-N**	**Poly-N**	**Poly_P+**
D1	746	60	0.28	0.31	1.3	1.1
D3	400	60	8.4	14	27	18
D4	450	45	0.41	0.47	0.69	0.78
D5	450	75	0.35	0.45	0.63	0.72
D6	573	39	0.21	0.29	1.06	0.85
D7	573	81	-	0.26	0.76	-
D8	573	60	0.26	0.30	0.88	0.82
D9	573	60	0.25	0.29	0.70	0.82
D10	695	60	0.23	0.32	0.59	0.70
D11	695	45	0.25	0.30	0.66	0.86
D12	695	75	0.26	0.30	0.69	0.87
D14	520	20	0.35	0.39	0.58	0.61
D15	500	20	0.40	0.41	0.57	0.61
D16	480	20	0.43	0.46	0.59	0.60

Notice the remarkably high sheet resistivity values of sample D3 compared to other samples. The only process condition that was different for sample D3 was its low RTP temperature at 400°C. The first metastable phase of nickel silicide, Ni_2Si, was known to occur closely below this temperature based on Table 2.3. The RTP temperature of all other samples should result in one or more of three phases: NiSi, $NiSi_2$, or a mixture of two or more of the three known phases.

A statistical analysis of the average Rs data showed that the silicidation temperature was the only significant factor in influencing the silicide's Rs. The Central Composite Design of experiment, see appendix section 3, was analyzed using the statistical JMP IN software.

Figure 4.1 shows the plot of the Rs for the four different sample regions: Si_P+ (doped silicon), Si-N (non-doped silicon), Poly-N (non-doped polysilicon), and Poly_P+ (doped polysilicon). Notice sample D3 was plotted on the secondary y-axis on the right whereas all other samples were plotted on the primary y-axis on the left. This is to aid in the visibility of the plot. The general trend showed the doped regions have slightly lower Rs as compared to the non-doped regions. This was similar to Zimmerman's observation of dopant "snowplowing" effect where dopants were pushed down toward the silicide/silicon interface as the silicidation process consumed the silicon/polysilicon material [1]. Such an effect would aid in reducing the interfacial resistance between the silicide and the underlying layer. This lower Rs observation was also confirmed by the electrical resistivity data in the next section.

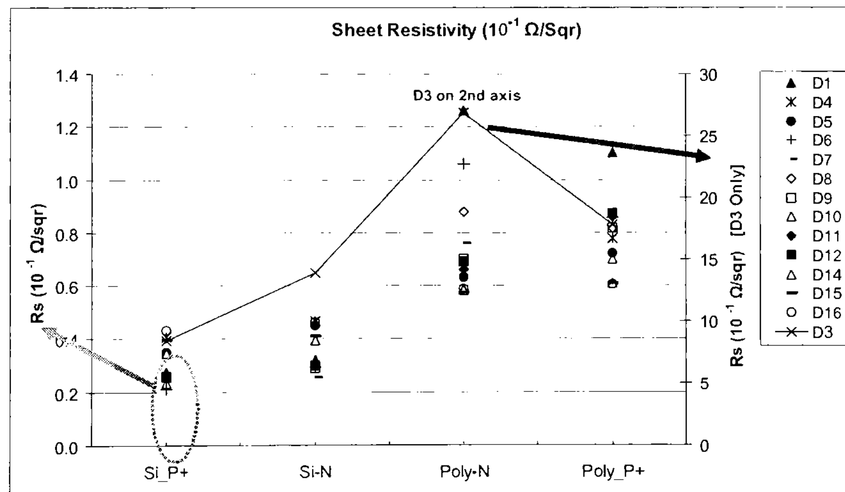

Fig. 4.1. Sheet resistivity of four regions. RTP processing conditions were varied for each sample.

In addition, it was observable that the Rs was generally much lower in doped and non-doped silicon regions than in polysilicon respectively. Since the polysilicon regions are polycrystalline silicon whereas the silicon regions are crystalline silicon, this

suggested that nickel silicidation was preferential to more ordered crystal structure. Such observation was also confirmed by the silicide's depth profile and electrical resistivity data. Refer to the section 4.4 for further detail.

4.2. Depth Profile by Grooving

The grooving technique was done using the Signatone grooving tool with a diamond impregnated groove wheel. The groove wheel diameter was measured to be 1.560 inches. Each sample was grooved for 15 seconds under constant pressure. Fig. 4.2 shows the diagram and actual images of the groove. From the groove, a top down image was captured using an optical microscope equipped with polarized light. Measurements for "m" and "n" were made using Image Pro software. With the measurements of "m and n," equation 4.1 was used to calculate the actual junction depth, X_D, of the silicide film where "D" is the diameter of the groove wheel [2]. Due to limitations of the grooving and measurement techniques, the junction depths obtained were not 100% accurate. These values provided a good estimate of the actual silicide depth since precise measurements of "m and n" were impossibly with such technique. The junction depth through SIMS and RBS analyses were done to validate this technique. Based on SIMS and RBS analyses, a correction factor was needed to represent the actual silicide depth using the groove technique more accurately. This is illustrated in section 5.3 and 5.4.

$$X_D = \frac{m \times n}{D} \qquad [nm] \tag{4.1}$$

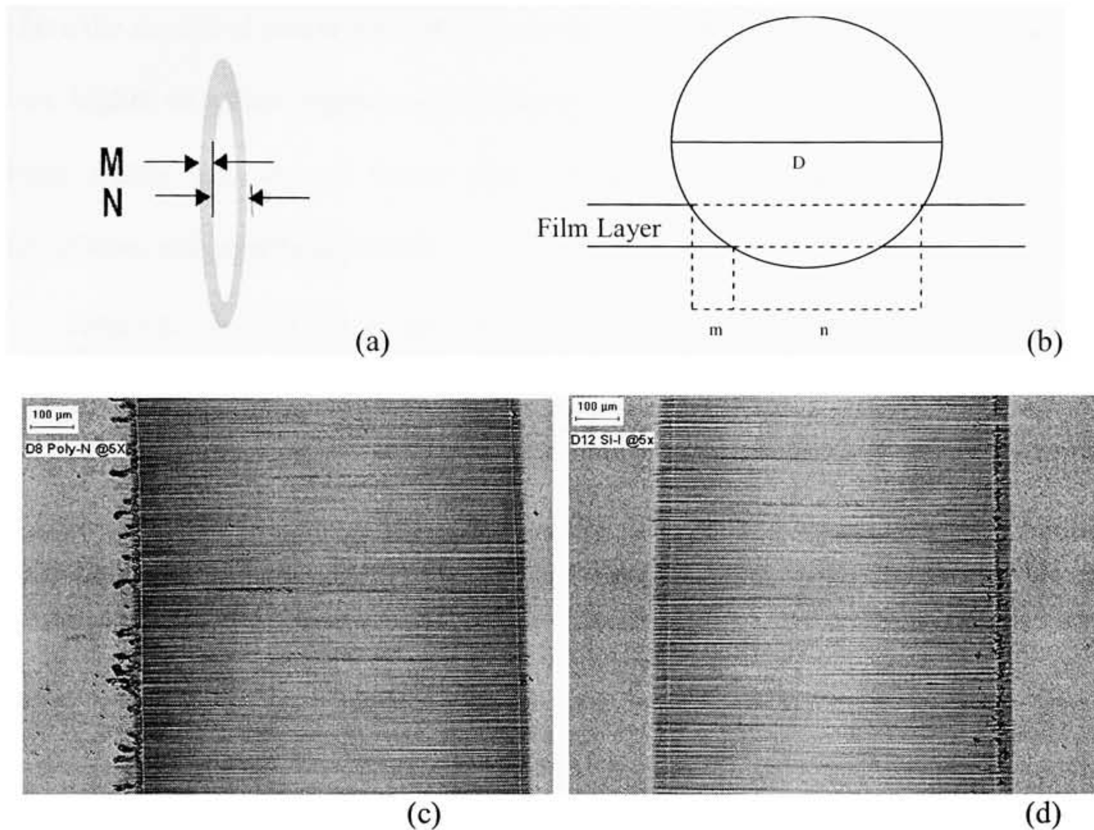

Fig. 4.2. Top-down diagram of groove (a) and cross sectional view of groove and wheel. Actual groove image of non-doped poly (c) and doped silicon (d). Courtesy of Dr. Gupta, Mechanical Engineering Department at RIT.

The calculated junction depths, X_D, were reported in Table 4.3 and plotted in Fig. 4.3. The junction depth of all samples ranged from 397nm to 867nm except for sample D3 (176nm to 215nm). This observation was expected since the deposited nickel was not fully consumed during the silicidation process. Notice sample D7 does not have depth data for the two doped regions. This was due to insufficient sample size to accommodate the groove.

Similar to the Rs plot, sample D3 was also plotted on its own axis to improve visibility. A closer look at sample D3 showed that the junction depth of the doped regions was similar in both silicon and polysilicon. However, the non-doped polysilicon region had much higher depth profile than the non-doped silicon region. For all other samples

where the deposited nickel was fully consumed, the trend showed that the junction depths were higher in silicon regions as compared to polysilicon despite doping. The highest depth profile was seen in doped silicon followed by non-doped silicon, non-doped polysilicon, and doped polysilicon.

Table 4.3. Calculated junction depth of four regions based on grooving technique. Grooving of sample D7 doped regions was unavailable due to insufficient sample size.

			X_D (10^2 nm)			
Wafer ID	**Temp [°C]**	**Time [sec]**	**Si_P+**	**Si-N**	**Poly-N**	**Poly_P+**
D1	746	60	5.8	5.8	5.8	4.4
D3	400	60	2.0	1.8	2.2	1.9
D4	450	45	5.8	7.2	4.9	5.6
D5	450	75	6.2	5.6	4.7	4.9
D6	573	39	7.0	5.4	4.9	4.4
D7	573	81	-	7.7	5.8	-
D8	573	60	7.9	8.7	4.0	5.5
D9	573	60	9.0	6.5	5.1	5.6
D10	695	60	6.9	7.3	5.4	4.7
D11	695	45	7.8	6.6	6.1	4.4
D12	695	75	7.4	7.0	6.2	4.1
D14	520	20	6.0	5.2	6.3	5.3
D15	500	20	4.0	5.1	5.0	4.0
D16	480	20	5.6	5.8	4.2	3.8

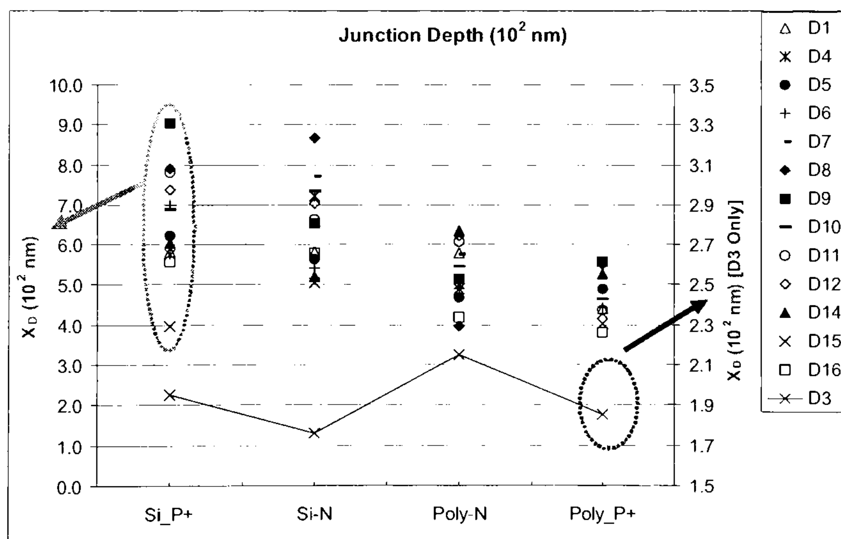

Fig. 4.3. Calculated junction depth of four regions. Sample D3 is on a secondary y-axis whereas all other samples are on the primary.

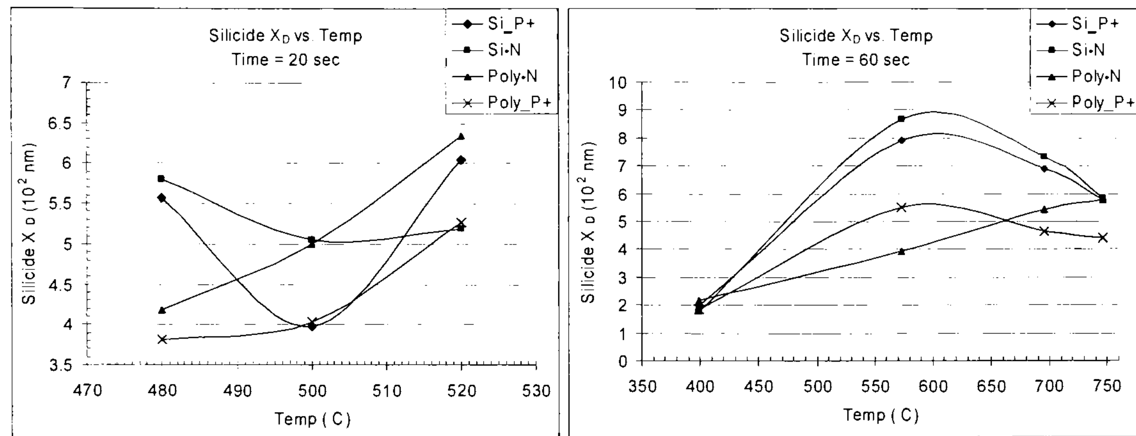

Fig. 4.4. Silicide depth profile as a function of temperature at 20sec and 60sec time.

Fig. 4.4 shows the depth profile of nickel silicide as a function of silicidation temperature at two different silicidation times. For silicidation time of 60sec, the deepest junction was seen at temperature around 550 °C to 600 °C in all regions except the non-implanted polysilicon. Within the temperatures range of 400-750 °C, the silicidation rate of the polysilicon and silicon regions were never the same for both implanted and non-implanted films. However, at silicidation time of 20sec, the silicide's depth profile was drastically different. There was one small temperatures range where the silicidation rate of polysilicon and silicon regions in both implanted and non-implanted regions were similar. At 500 °C, the silicide's depth for polysilicon and silicon were around 500nm and 400nm for non-implanted and implanted regions respectively. In addition, the junction depth of non-implanted polysilicon was deeper than that of non-implanted silicon at temperature above 500 °C. This fact suggested the silicidation rate of non-doped polysilicon was higher than that of corresponding silicon region only at temperatures above 500 °C for the silicidation time of 20sec. However, the SIMS data was incomplete at this silicidation condition to verify such observation due to limited SIMS analysis.

Similar analysis was done to correlates silicide's depth profile as a function of time. However, no relevant correlations were found.

Once again, it should be mentioned that the junction depth calculated by this grooving technique did not correlates to the actual silicide junction depth 100%. Limited junction depth profiles obtained by SIMS and RBS analysis techniques suggested the need for an offset value (correction factor) to match these calculated values with actual value. Such offset value can be seen in the next chapter. However, there was low confidence in the accuracy of the correction factor derived from the next chapter due to insufficient RBS and SIMS data. Nonetheless, the qualitative analysis and comparison of all samples relative to each other are still valid and could be valuable in understanding nickel silicidation.

4.3. Electrical Resistivity of Nickel Silicide

The electrical resistivity of each silicide samples were calculated using equation 4.2, Rs data, and junction depth information. The calculated resistivity data are shown in Table 4.4 and plotted in Fig. 4.5. The plot showed that the electrical resistivity was generally lower for silicides formed in crystalline regions compared to polycrystalline regions. Once again, this confirmed the silicidation preference in crystalline region as previously suggested by the R_S data. In term of doping effect, doped regions showed lower resistivity in both crystalline and polycrystalline materials. This further confirmed the snowplowing effect of dopants as seen in the Rs data. The lower resistivity indicated that the silicide phase composition was closer to the NiSi phase. However, such phase composition was most likely to be a mixture of two or more metastable phase since all

calculated resistivities were higher than that of the published NiSi value (1.05×10^{-5} Ω-cm) [3].

(4.2) $$\rho = R_S \times X_J \qquad [\Omega - cm]$$

Table 4.4. Calculated electrical resistivity based on R_S and junction depth data.

			Resistivity (10^{-5} Ω-cm)			
Wafer ID	Temp [°C]	Time [sec]	Si_P+	Si-N	Poly-N	Poly_P+
D1	746	60	1.6	1.8	7.3	4.8
D3	400	60	16	25	58	33
D4	450	45	2.3	3.4	3.4	4.3
D5	450	75	2.2	2.5	2.9	3.5
D6	573	39	1.5	1.6	5.2	3.8
D7	573	81	-	2.0	4.4	-
D8	573	60	2.0	2.6	3.5	4.5
D9	573	60	2.3	1.9	3.6	4.6
D10	695	60	1.6	2.4	3.2	3.2
D11	695	45	2.0	2.0	4.0	3.8
D12	695	75	1.9	2.1	4.3	3.6
D14	520	20	2.1	2.0	3.7	3.2
D15	500	20	1.6	2.1	2.9	2.5

Sample D3 followed the same trend as all other wafers but at one order of magnitude higher in resistivity values. It was plotted with a dotted line and indicator was used to point toward the secondary axis on the right for ease of visibility. Overall, the resistivity data showed that doped silicon and polysilicon were the most optimal material to obtain the lowest electrical resistivity for nickel silicide. Similar to the Rs data, the electrical resistivities in polysilicon regions were distinctly higher than the silicon regions.

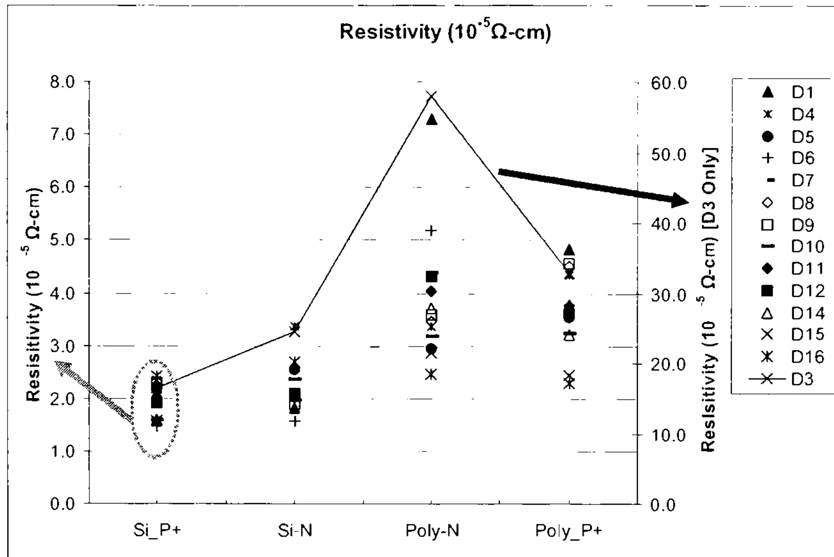

Fig. 4.5. Calculated electrical resistivity plotted by regions. Note that sample D3 is plotted on a separate axis to its high value.

Fig 4.6 shows the electrical resistivity as a function of silicidation time. The plots indicated that silicidation time (RTP anneal time) had insignificant effect on the overall resistivity of the silicide. There was very little variation in resistivity over a wide time range of 45 sec to 75 sec in all four regions. However, the plots did show the resistivity differences between crystalline and polycrystalline regions as previously seen.

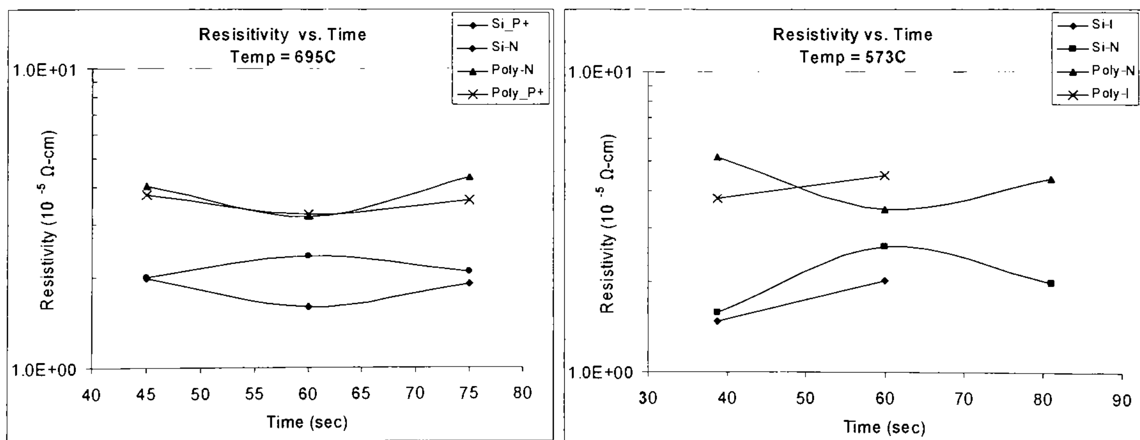

Fig. 4.6. Resistivity as a function of RTP time at 695 °C and 573 °C. There is little or no correlation between electrical resistivity and silicidation time.

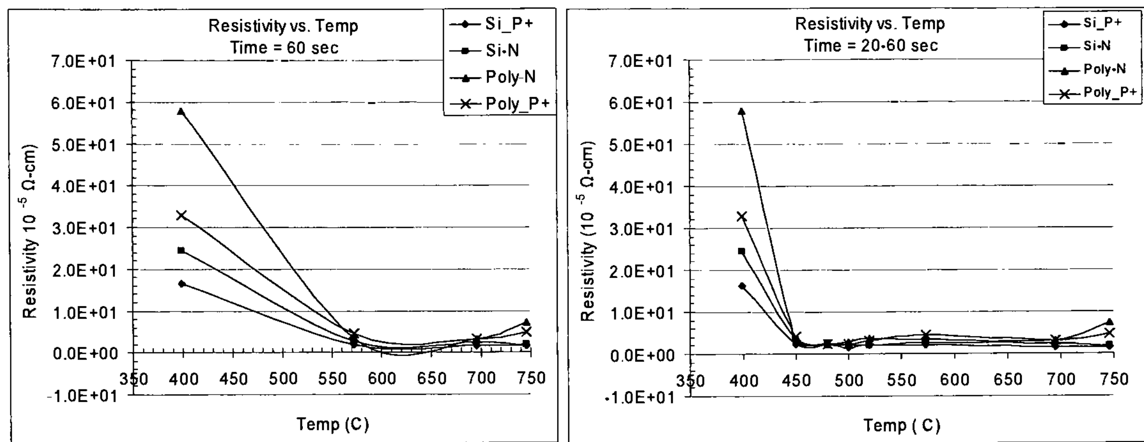

Fig. 4.7. Resistivity as a function of RTP temperature. Data at 450°C to 550°C were at 20sec RTP time while all other data were at 60sec time. A dramatic increase in resistivity is seen at 400 °C RTP temperature while an up-tick is visible at 750 °C.

Although the silicidation time showed no correlation, there was significant correlation between resistivity and silicidation temperature as suggested by the DOE analysis. Fig. 4.7 shows the correlation between resistivity and silicidation temperature at variable time. A time range of 20-60 sec was plotted since Fig. 4.6 suggested no significant impact was seen for this silicidation variable. Based on Fig. 4.7, it was apparent that three distinct regions were visible. The first region being around 400 °C with characteristic of extremely high resistivity, the second region was characterized by lowest observed resistivity that existed between 450 – 695 °C, and the beginning of the third region was visible at 746 °C with an increase in resistivity. Comparing the resistivity value of each region to published resistivity of nickel silicide phases, it seemed like the phase composition of all samples at 450 to 746 °C was mainly Ni_2Si or a mixture of Ni_2Si with the other two phases.

In the first region, the resistivity of D3 was over one order of magnitude higher than the published resistivity of all nickel silicide phases. This suggested that the silicidation process was incomplete for the given condition. This was evident by the fact that there

was un-reacted nickel metal on this sample and not on any others. All other samples received much higher temperature treatment for much shorter (20 sec) and much longer (75 sec) time. Yet no samples showed any un-reacted nickel left over after the RTP anneal. Despite the RTP time, the RTP temperature at 400 °C was insufficient to trigger a complete nickel silicidation into the known stable phase.

In the second region, the resistivity hovered around that of the Ni_2Si and/or $NiSi_2$ phases. However, another possible condition is that the observed resistivity may be the overall resistivity for a mixture of multiple silicide phases such as Ni_2Si/NiSi, NiSi/$NiSi_2$, or any other possible mixture combinations that may exist within the measured silicide thickness. Unfortunately, there was no published nickel silicide resistivity for phase combinations to use as references. However, the confirmation of such phase mixtures were possible based on SIMS and XRD analyses. Refer to chapter 5 for further detail.

Previous published works have implemented a two-step RTP silicidation process for previous metal silicide such as cobalt silicide [4, 5]. Although not necessary, the two-step annealing approach was also studied on sample D3. This sample was the only sample that allowed for reasonable control over the silicide's depth. Relative to all other samples, D3 has the shallowest depth profile as well as the highest measured resistivity. As stated earlier, this suggested an incomplete silicidation process therefore making it the best candidate for the two-step silicidation study. After all un-reacted nickel metal was removed from D3, the implanted polysilicon and silicon regions underwent a second RTP annealing process at 500 °C for 60sec. Inspection of the grooves showed little variation in the junction depth, yet a dramatic drop in the sheet resistivity was seen. Such drop resulted in the decrease of its electrical resistivity by about one order of magnitude. See

Table 4.5 and Fig. 4.8 for detail. The final electrical resistivity of the implanted D3 regions was on the mid to high side yet comparable to similar regions from other samples. However, its junction depth remained fairly the same and much less than any other samples. Similar second RTP processing step was done on several other samples. However, there were insignificant changes in the sheet resistivity and junction depth.

Table 4.5. Measured junction depth, R_S, and resistivity of implanted D3 regions.

Wafer Region	Temp [°C]	Time [sec]	X_D [nm]	R_S [Ω/□]	Rs Std. Dev [Ω/□]	ρ [Ω-cm]
D3 Si_P+	400	60	195.1	8.4195	0.3730	1.6425E-04
D3 Si_P+ 2nd RTP	500	60	187.2	2.0960	0.0203	3.9235E-05
D3 Poly_P+	400	60	185.5	17.7650	0.3249	3.2946E-04
D3 Poly_P+ 2nd RTP	500	60	172.6	4.1157	0.0787	7.1039E-05

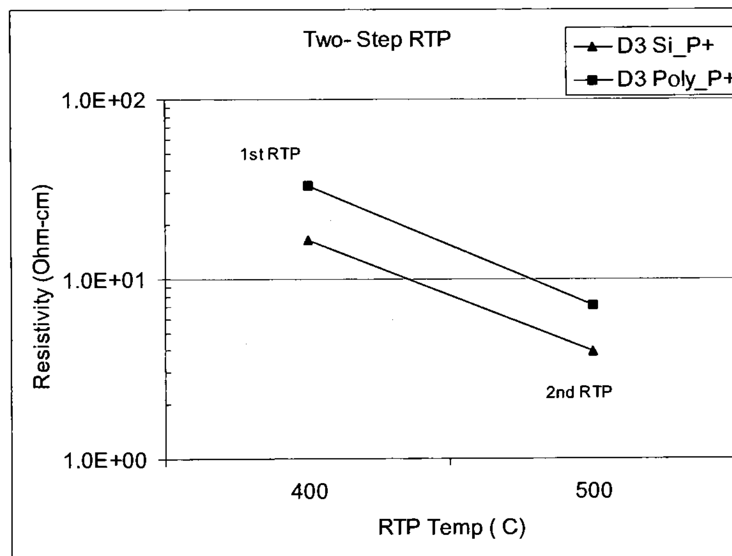

Fig. 4.8. Electrical resistivity of D3 implanted regions after 2nd RTP.

4.4. Discussions

The observations made in section 4.1 were supported by the electrical resistivity result. Doped regions generally have lower resistivity than that of non-doped regions,

although this was more apparent in silicon than in polysilicon region. Similar sheet resistivity and electrical resistivity trends were observed in Fig. 4.1 and 4.5 respectively. Such lower resistivity in doped regions was believed to be partly due to the dopant snowplowing effect discussed earlier. An absolute confirmation of this claim could not be done through SIMS analysis due to resources and budgetary constraints. The external SIMS analysis did not actively study the dopant profile needed for such confirmation.

The depth profile obtained by the groove technique revealed that for a given nickel thickness and annealing condition, the silicide's thickness was generally thicker in the crystalline silicon than in polycrystalline silicon regions. This was apparent in Fig. 4.3 above. The difference in thickness was mainly due to the difference in nickel atomic diffusion coefficient in the two regions [6]. Kuznetsov has reported that the diffusion coefficient of nickel in polysilicon, $2.9 \times 10^{-3} \exp\{-1.30(eV)/kT\}$ [cm^2/sec], was about six to eight orders of magnitude lower than in crystalline silicon for the temperatures range of 270 °C to 435 °C. Nickel was reported to be a fast interstitial diffuser in crystalline silicon. However, the presence of high concentration of intrinsic traps in polysilicon retarded the interstitial diffuser [6]. This caused the dramatic drop in diffusion coefficient and consequently the thinner silicide film in polysilicon region as seen in Fig. 4.3.

In addition, Fig. 4.1 and 4.5 also showed significantly lower resistivity in crystalline silicon than in polysilicon regions despite implant effect. This observation contributed to the conclusion that nickel silicidation was preferential to crystalline silicon compared to polysilicon in terms of both formation rate and silicide's property. The silicidation rate was higher in crystalline regions as confirmed by thicker junction depth result seen in Fig.

4.3. The higher silicidation rate allowed for faster phase transformation into one or more of the three known stable phases. Although the exact silicide's phase or mixture of phases were not known through electrical measurements, the lower resistivity of crystalline silicon regions suggested that the silicide composition consisted primarily of the first two phases, Ni_2Si and NiSi, due to their lower resistivity. Refer to the XRD and SIMS discussion section in Chapter 5 for further detail.

4.5. Conclusion

The electrical resistivity data of nickel silicide is successfully calculated based on sheet resistivity and silicide's junction depth measurements through four-point probe and grooving techniques. The calculated electrical resistivity represents the overall resistivity of the entire silicide layer without regards to any composition mixture of silicide phases. Material characterization of these silicide films shows the existence of multiple silicide phase compositions. Therefore, the calculated resistivity is not and should not correlate to any published single-phase nickel silicide values.

Furthermore, the accuracy of the electrical resistivity is not absolute due to the need for a correction factor of the depth data mentioned in the section 4.2. The correction factor is expected to modulate the junction depth and consequently the electrical resistivity data. However, the qualitative analysis between the four different regions, doped/non-doped silicon/polysilicon, is still valid. The silicidation rate in crystalline silicon is much higher than in the polysilicon regions. This consequently results in thicker nickel silicide film in the crystalline silicon source/drain regions of a MOSFET. This information is crucial future MOSFET design and fabrication if shallow source/drain and

fully silicide poly-gate are desire. Furthermore, the electrical resistivity of nickel silicide is moderately higher in polysilicon compared to crystalline silicon regions and should be considered in such device design.

Reference

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[2] Dr. Lynn Fuller, "RIT PMOS Process Details," Department of Microelectronic Engineering at RIT, Rochester, NY(2002).
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[5] B. Froment, M. Muller, "Nickel vs. Cobalt Silicide Integration for Sub-50nm CMOS," ESSDERC, pp.215-218, (2003).
[6] A. Yu. Kuznetsov, B. G. Svensson, "Nickel atomic diffusion in amorphous silicon," Applied Physics Letters, **66** (17), pp.2229-2231, (1995).

5. Material Characterization

Various analytical techniques were used to study the material characteristics of nickel silicidation. Atomic force microscope (AFM) was used to study the surface topography of the silicide films, x-ray diffraction (XRD) was used for silicide's phase identification, Rutherford backscattering (RBS) was used to determine phase composition, and secondary ion mass spectroscopy (SIMS) was used for silicide elemental concentration determination as well as junction depth. The intention of AFM analysis was to determine whether there were any correlations between surface topography with the silicide's electrical data and phase composition. The other three techniques were used to complement and validate the actual composition, junction depth, and identification of the silicide phase at specific RTP annealing condition.

5.1. Surface Morphology by AFM

AFM was used to analyze the surface topography of the sample using the basic tapping mode as described in chapter 3. The primary interest was in the surface roughness and grain size of the film. The surface roughness was characterized quantitatively by the root mean square (RMS) value, and the grain size was qualitatively characterized through visual inspection. A Veeco Dimension 3000 Scanning Probe Microscope (SPM) was used for all surface morphology analysis. The Dimension 3000 SPM utilized automated atomic force microscopy (AFM) and scanning tunneling microscopy (STM) techniques to measure surface characteristics. No special surface preparations were done on any samples prior to the analysis. All samples were air cleaned using a commercial nitrogen-based air duster product. A Veeco OTESPA silicon probe-

tip assembly, with a tip radius of 7nm, was used for all measurements at room temperature and atmospheric condition.

5.1.1. Reference Regions

AFM analysis was done on several reference samples prior to any silicide analysis. Fig. 5.1 shows the grain structure and root mean square (RMS) roughness of doped polysilicon, nickel metal on doped polysilicon, and nickel metal on doped silicon regions from left to right respectively. No information was available for doped silicon region. It was apparent that nickel grain structure and roughness were much less in doped crystalline silicon compared to polysilicon region. Furthermore, the grain structure and roughness of deposited nickel were very similar to that of the underlying polysilicon film. Although there were limited data, this seemed to suggest that sputtered nickel tends to mimic the surface morphology of the underlying film.

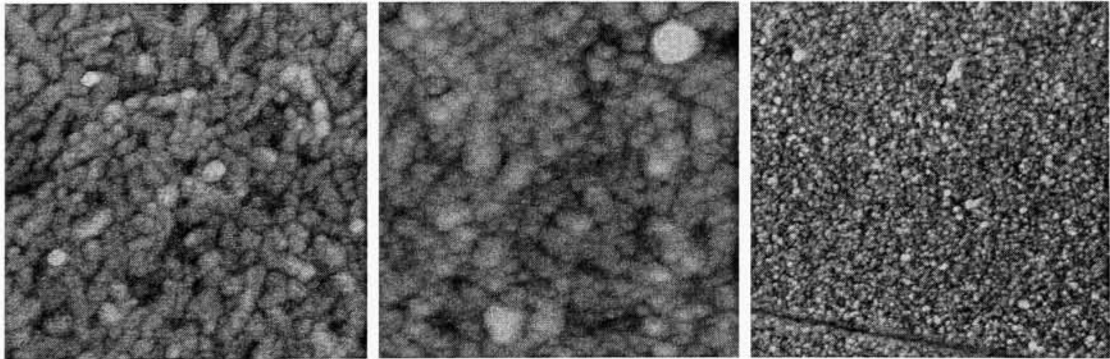


Fig. 5.1. Reference AFM of doped polysilicon, nickel on doped polysilicon, and nickel on doped silicon regions from left to right respectively. Fixed scan size at 2.5μm x 2.5μm. Courtesy of Dr. V. Gupta, Mechanical Engineering Department, RIT.

5.1.2. Near Critical Temperature and Constant Time

Based on literature references, the critical conditions for Ni_2Si, NiSi, and $NiSi_2$ were at RTP annealing temperature of around 350°C, 500°C, and 700°C respectively [1, 2]. Due to limitation of the RTP tool, the lowest possible temperature setting was limited to 400°C. Fig. 5.2 shows the surface morphology and RMS roughness of nickel silicide at 400°C, 573°C, and 746°C. The top images were taken in doped polysilicon regions whereas the bottoms were taken in the doped silicon regions. It was apparent that the smallest grain structure and the lowest RMS roughness were visible at 400°C.

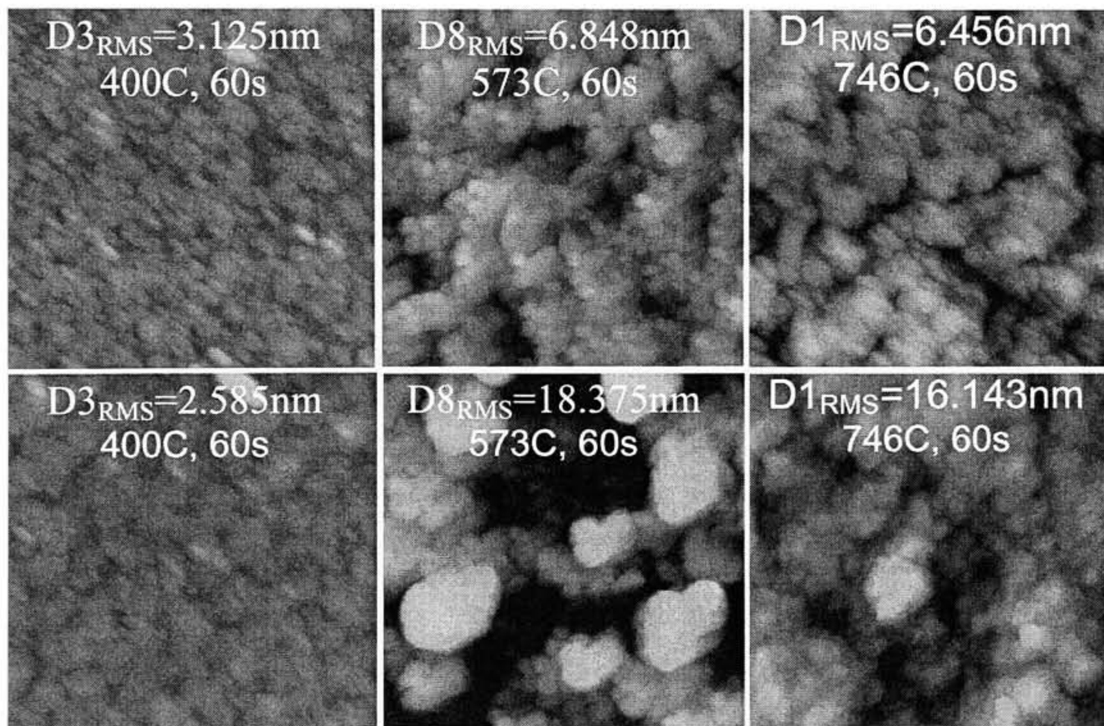


Fig. 5.2. Surface roughness of silicide's surface around known critical temperature valued. The top images were taken from doped polysilicon regions whereas the bottoms were taken from doped crystalline silicon regions. Fixed scan size at 2.5μm x 2.5μm. Courtesy of Dr. V. Gupta, Mechanical Engineering Department, RIT.

The surface morphology (grain structure and RMS roughness) was slightly higher at 573°C than at 746°C. This was most visible in crystalline silicon region. In the polysilicon region, the grain structure at 746°C seemed to be a result of agglomerations of the spherical and cylindrical grains found at 573°C. The same agglomeration effect was seen in crystalline region. However, the rate of agglomeration appeared to be much faster in crystalline silicon since the overall grain structure and RMS roughness were higher.

5.1.3. Silicidation Temperature Effect

Similar to the electrical resistivity characteristic, the RMS roughness exhibited a strong correlation with silicidation temperature. Fig. 5.3 shows the plot for such correlation. The RMS roughness increased linearly as temperature increased from 400°C to 700°C, and began to drop off at higher temperature. This was as expected since increasing temperature leads to the merging and eventually agglomeration of nickel silicide grains as observed in previous works [1, 3].

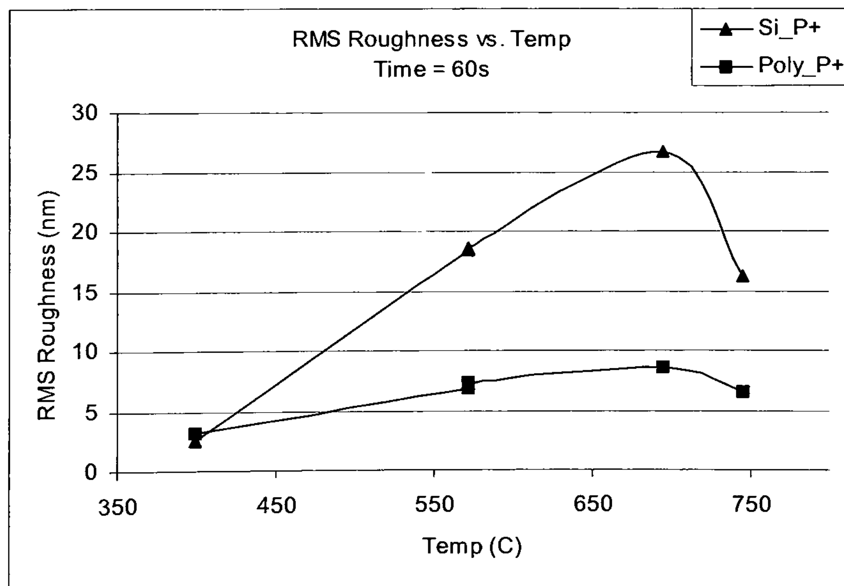


Fig. 5.3. RMS roughness as a function of temperature at 60sec.

The correlation of such observation with the electrical resistivity results showed that higher RMS roughness leads to lower resistivity. Refer to Fig. 4.7. Note the highly resistive silicide value at 400°C, the drop in resistivity in the range of 450°C to 700°C, and the increase in resistivity at higher temperature. Fig. 5.3 also showed that such changes in RMS roughness were more pronounced in doped crystalline silicon than doped polysilicon regions. This seemed to support earlier reasoning that silicidation rate was much faster in crystalline regions due to higher nickel diffusion coefficient.

5.1.4. Silicidation Time Effect

Unlike silicidation temperature, silicidation time showed moderate effect on the RMS roughness of silicide film. Fig. 5.4 depicts the effect of time on silicide's surface roughness.

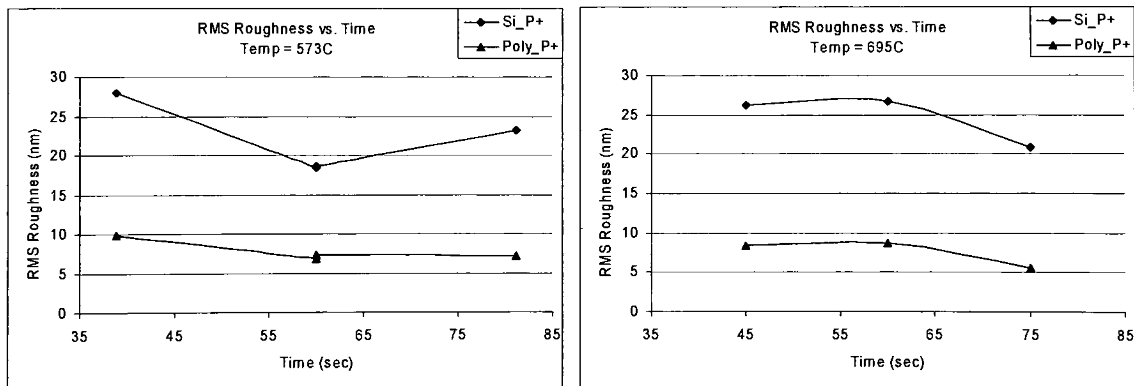


Fig. 5.4. RMS roughness as a function of time at 573°C and 695°C.

As observed, the effect of time was more pronounced in crystalline than polysilicon regions. This was consistent with previous observations and further supported the fact that silicidation rate was much faster in crystalline regions.

Surface roughness was highest at 40sec and 60sec for temperature of 573°C and 695°C respectively. This corresponded to the lowest electrical resistivity found in Fig. 4.6 for both regions. Thus the observation was consistent in relating higher surface roughness to lower silicide resistivity based on the calculated values in chapter 4. In comparison between 573°C and 695°C, increased in temperature seemed to delay/shift the effect of time on surface roughness. The lowest surface roughness found at 573°C was delayed by about 15sec at 695°C. However, there was low confidence level in such conclusion since another data point at longer time was needed in the lateral temperature plot for completeness.

5.2. Phase Identification by XRD

X-ray diffraction (XRD) analysis was used to identify the phase(s) of nickel silicide film. Doped crystalline silicon and polysilicon regions from selected samples were analyzed, and the results were shown in Table 5.1. XRD analysis was done on these samples prior to and after the wet etch of un-reacted nickel metal. Nickel metal was detected only in sample D3 at $2\theta = 44.6°$. This confirmed that the dark cloud seen during wet etch of D3 was indeed un-reacted nickel metal. Such observation was also be confirmed by RBS analysis. Refer to Fig. 5.5 for detail.

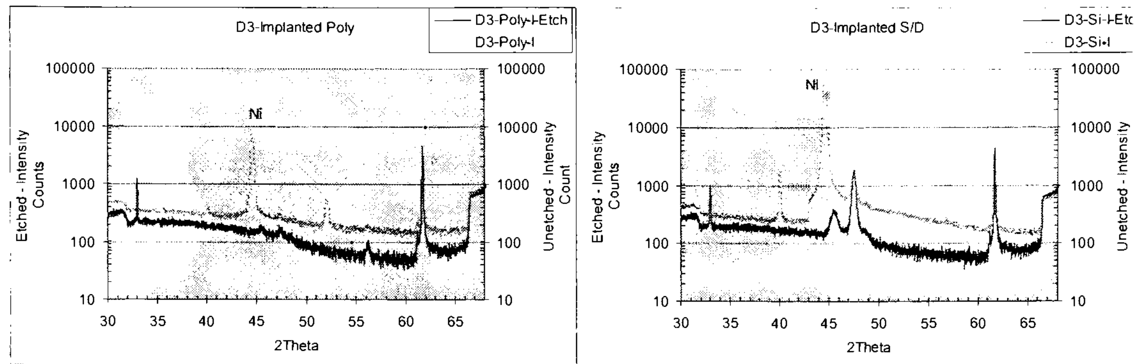


Fig. 5.5. XRD intensity plot of D3 prior to and after metal wet etch. Nickel peak is presence at 2θ = 44.6°. Courtesy of Dr. Gupta, Mechanical Engineering Department at RIT.

Besides sample D15, all samples were analyzed at RIT Mechanical Engineering Lab using the Rigaku DMAX-IIB XRD system. All measurements were taken using a Cu radiation source ($K\alpha_1$ = 1.540562 Å, $K\alpha_2$ = 1.544390 Å) at 40 kV and 35 mA. The scan was set with a step size of 0.01° at 1.5°/min, and the angle was varied from 30° 2θ to 120° 2θ for sample D1, D3, and D6. All other samples were done at an angle of 30° 2θ to 68° 2θ since no useful information could be seen beyond such range. In addition, sample D15 was analyzed on a Siemens DMAX XRD at IBM. The tool utilized a Fe radiation source (λ = 1.93604 Å) at 35 kV and 35mA. The scan angle varied from 35° 2θ to 75° 2θ with a step size of 0.01° at 20sec/pt. The difference in XRD tools was not expected to cause any critical variations in the analysis.

As evident from Table 5.1, the majority of the samples contained mixture of nickel silicide phases (primarily of Ni_2Si and NiSi). Sample D3 consisted mostly of Ni_2Si phase with a trace presence of NiSi peak. The intensity of the one NiSi signature peak seen in D3 was significantly less than all other samples. Consequently, this suggested the silicidation condition of D3 (400°C and 60sec) was close to the transition condition of

Ni_2Si into NiSi. Such observation was evident in both doped crystalline silicon and polysilicon regions.

Table 5.1. Nickel silicide phase(s) detected by XRD analysis. Sample D15 was analyzed using Fe radiation from the Siemens DMAX XRD at IBM, and all other samples were analyzed using Cu radiation from the Rigaku DMAX-IIB XRD at RIT. Courtesy of Dr. V. Gupta at RIT and Mrs. A. Madam at IBM.

Wafer ID	Temp [°C]	Time [sec]	Si_P+ Detected Phase(s)	Poly_P+ Detected Phase(s)
D3	400	60	Ni_2Si, *slightly* NiSi	Ni_2Si, *slightly* NiSi
D4	450	45	Ni_2Si, NiSi	NiSi
D15	500	20	Ni_2Si, NiSi	Ni_2Si, NiSi
D14	520	20	Ni_2Si, NiSi	Ni_2Si
D6	573	39	NiSi	Ni_2Si, NiSi
D7	573	81	NiSi	Ni_2Si, $Ni_{31}Si_{12}$
D11	695	45	NiSi	NiSi
D1	746	60	Ni_2S, NiSi	Ni_2Si, NiSi

Based on the silicidation temperature in the doped crystalline silicon region alone, the temperature ranges from 450°C to 520°C and at 746°C showed strong presence of Ni_2Si and NiSi phases. However, the intensity of Ni_2Si peaks were an order of magnitude higher than that of NiSi near the lower and higher temperature range, 450°C and 746°C respectively. The two phases' peak intensities were more comparable as temperature increased/decreased from the lower/higher temperature regime respectively. Within the temperature of 573°C to 695°C, the presence of Ni_2Si peaks were completely gone leaving only strong signals of NiSi phase. Note that this was only true in the crystalline silicon region. Different silicide phase mixtures were seen in doped polysilicon regions. Refer to Fig. 5.6 and Table 5.1. In general, the mixture of Ni_2Si and NiSi occurred for a wider temperature range on polysilicon region before the complete transition to NiSi phase was seen. The single phase NiSi was seen at 695°C compare to 573°C in crystalline silicon region. Once again, this seemed to agree and support earlier observations that the

silicidation was much faster in crystalline silicon than in polysilicon regions. Furthermore, it should be noted that the observed Ni_2Si and NiSi phase mixture was consistent with Zhang's experimental results where multiple phase growth were observed for nickel silicide [4]. His experimental results showed Ni_2Si and NiSi as the two primary multiple phase that coexisted during silicidation.

The transition trend was more apparent and well defined in crystalline silicon than in polysilicon regions. In sample D4, the analysis clearly detected NiSi phase in polysilicon region. However, this was intuitively unlikely since the presence of Ni_2Si was clearly and strongly identified at four higher temperature samples. Similar occurrences were seen in polysilicon region of samples D14 and D7. D14 showed distinct peaks of the single phase Ni_2Si whereas NiSi was seen at lower temperature samples. D4 showed a strong presence of Ni_2Si phase in mixture with $Ni_{31}Si_{12}$, a highly unstable phase that is generally not seen. $Ni_{31}Si_{12}$ is a metal rich silicide phase that would have come at the beginning of the silicidation process and instantaneously transform into the first observable Ni_2Si phase [4]. Therefore, Fig. 5.6 generalized trend observed without accounting such highly improbable occurrences. One phenomenon that was not quite understood was the presence of Ni_2Si and NiSi mixture at 746°C in sample D1. The reasoning is not yet known as to why Ni_2Si was seen at such high temperature where the final $NiSi_2$ phase was expected to be the primary, if not in mixture with NiSi, phase. This observation was confirmed by RBS analysis.

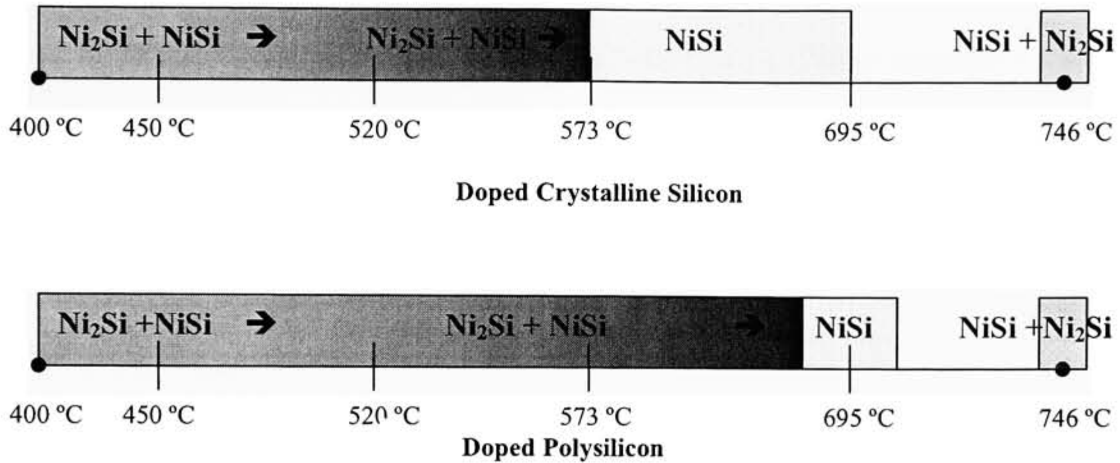


Fig. 5.6. General observed nickel silicide phase transition in doped crystalline silicon and polysilicon.

The effect of silicidation time on phase presence and concentration in mixture was not well understood. Based on the limited XRD data, D6 and D7, it was apparent that the intensity of NiSi peaks was higher with longer silicidation time in crystalline silicon regions. This seemed to suggest that the longer silicidation time allowed for thorough transitioning to the more stable phase, in this case NiSi instead of Ni_2Si. The inclination to draw such conclusion was supported by earlier AFM results where it was observed that longer time yielded higher surface roughness and lower electrical resistivity, a characteristic of NiSi phase as concluded in earlier chapter.

5.3. Phase Composition by RBS

External Rutherford backscattering (RBS) analysis was done to complement and validate XRD data. RBS is capable of detecting elemental ratios of a material. In this case, the elemental ratios of interest were Ni and Si in the silicide film. The ratios obtained would reveal the overall nickel silicide phase in the film. One limitation of RBS analysis was its inability to distinguish and identify the presence of multi-phases such as

$Ni_2Si/NiSi$. In addition, the calculated phase thickness based on RBS data assumed that there is one uniform phase throughout the entire layer. Such assumption would undoubtedly result in some thickness variations when compared with other technique such as grooving and SIMS. Equation 5.1 was used to calculate the overall silicides phase thicknesses based on measured RBS thicknesses and single silicide phase density. The single silicide phase density was obtained from K. Maex reference [5].

$$t = \frac{T\sum(M_i F_i)}{\rho N_A} \quad (5.1)$$

t = real thickness (cm)
T = RBS thickness ($atoms/cm^2$)
M_i = atomic weight (g/mol)
F_i = fraction of material in compound
ρ = compound density (g/cm^3)
$N_A = 6.025 \times 10^{23}$ atoms/mol

Doped crystalline silicon and polysilicon regions of samples D1, D3, and D6 were sent to the University of Florida for RBS analysis. (Courtesy of Dr. Gabriel Braunstein, Department of Physics, University of Central Florida.) Fig. 5.7 depicts the film stacks of all samples sent for RBS.

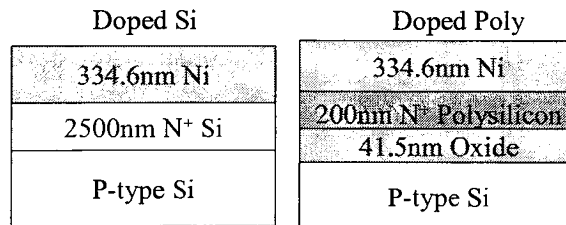


Fig. 5.7. Cross sectional view of samples sent for RBS analysis.

Fig. 5.8 summarizes the RBS results of all samples. It was apparent that the doped crystalline silicon region of D6 consisted purely of NiSi phase, Ni/Si ratio of 0.5/0.5. The other two crystalline silicon samples showed slightly uneven distribution of Ni/Si ratio,

with Si ratio being slightly higher. This tended to suggest that the silicide was primarily but not entirely NiSi phase as seen in D6 and that some multi-phase mixture was a possibility. However, this technique did not give sufficient information to determine the content of such multi-phase.

746C, 60sec	400C, 60sec	573C, 39sec
Sample 1P Ni 65%, Si 35% 3600x10^{15} atoms/cm^2 415 Å of SiO_2 Si The polysilicon has been consumed and Ni2Si has formed.	**Sample 3P** Ni 100%, 2800 Å Si 100%, 2500 Å SiO_2 415 Å Si Sample did not change	**Sample 6P** Ni 65%, Si 35% 3525x10^{15} atoms/cm_2 415 Å of SiO_2 Si The polysilicon has been consumed and Ni2Si has formed.
Sample 1S Ni 49%, Si 51% 4850x10^{15} atoms/cm^2 Si There is a rough interface between the top layer and the second layer, or a rough surface.	**Sample 3S** Ni 100%, 2800 Å Ni 48%, Si 52% 450x10^{15} atoms/cm^2 Si There is a thin layer of about 48% Ni and 52% Si, between the Ni top layer and the Si	**Sample 6S** Ni 50%, Si 50% 4900x10^{15} atoms/cm^2 Si There is a rough interface between the top layer and the second layer, or a rough surface.

Fig. 5.8. Summary of RBS result with elemental ratio and RBS thicknesses. Courtesy of Dr. Braunstein, Department of Physics, University of Central Florida. Sample 1P=D1 Poly_P+, 1S=D1 Si_P+.

In the doped polysilicon regions, samples D1 and D6 showed a Ni/Si ratio of 0.65/0.35. The significantly higher Ni ratio (~ 2:1) suggested that the primary silicide phase was a metal rich phase, Ni_2Si. Similar to the crystalline region, the slightly disproportional ratio suggested the presence of multi-phase silicide composition as well. This confirmed the XRD detection of Ni_2Si and NiSi mixture in D1 at 746°C. Although not anticipated, Fig. 5.6 was valid with the presence of Ni_2Si/NiSi mixture at the lower and higher temperature range where single-phase NiSi existed. Notice that the polysilicon was completely consumed during the silicidation process for both D1 and D6 samples.

The slight difference in the RBS thickness was insignificant and could be related to the non-uniformity of the polysilicon deposition process.

Unlike the two samples discussed, sample D3 yielded differently. There was undoubtedly the presence of 280nm of nickel metal on the surface. This observation validated earlier conclusion that nickel metal was present on the sample after silicidation. Notice there was a thin layer of silicide with Ni/Si ratio of 0.48/0.52 in the crystalline silicon region. The thickness of this silicide layer was about an order of magnitude lower that the other two samples. In addition, there was no detectable presence of nickel silicide on the polysilicon region at 400°C. This is highly unlikely since the sheet resistivity of the region changed by an order of magnitude from before and after the silicidation process. Furthermore, XRD also detected a strong presence of Ni_2Si in the region. Refer to Table 5.2 for the actual silicide thickness calculated for each region.

Table 5.2. Calculated silicide thickness based on single-phase density and RBS thickness compared to thicknesses from groove technique. Density adopted from [5]. D1-P = D1-Poly_P+, D1-S = D1-Si_P+ etc.

Sample	RTP Temp (°C)	RTP Time (sec)	Ni Ratio	Si Ratio	Phase	RBS Thickness (atoms/cm^2)	Thickness (nm)	Groove Thickness (nm)
D1-P	746	60	0.65	0.35	Ni_2Si	3.60E+18	387	439
D1-S	746	60	0.49	0.51	NiSi	4.85E+18	529	581
D3-P	400	60	-	-	-	-	-	119
D3-S	400	60	0.48	0.52	NiSi	4.50E+17	49	195
D6-P	573	39	0.65	0.35	Ni_2Si	3.53E+18	379	442
D6-S	573	39	0.50	0.50	NiSi	4.90E+18	538	700

Table 5.2 shows the calculated silicide thickness based on the measured RBS thicknesses and single-phase silicide density reference [5]. Notice that the phase density for the primary phase in the silicide mixture was used in the calculation. No account could be made for the minor silicide mixture. Based on this information, it was clear that the silicide was thicker in crystalline silicon than polysilicon regions by 36%-42%. The

significant of this is that it further confirmed the higher silicidation rate in crystalline silicon as concluded earlier. Furthermore, it showed that with a 49nm thick silicide film in D3 crystalline region, the expected silicide thickness in the corresponding polysilicon region would be about 34nm thick. Such thickness should have been detectable by the RBS tool in Florida.

5.4. Elemental Concentration by SIMS

To complement RBS analysis, secondary ion mass spectroscopy (SIMS) analysis was done on selected samples. Three samples (D15 doped silicon and polysilicon regions and D14 doped polysilicon region) were sent to the University of Florida for SIMS analysis. Due to budgetary constraints and limitation on the number of samples sent for RBS, SIMS analysis was used as an alternative to obtaining the necessary phase composition information. It was also a more accurate technique in obtaining the actual silicide thicknesses.

Table 5.3 shows the SIMS results for the three samples. The detected layers of each sample are listed from top to bottom with #1 being the surface layer. Notice all samples showed an ultra thin layer of native oxide on the surface. This native oxide layer grew on all silicon and silicide surfaces in atmospheric conditions during shipping and storage. This layer was not picked up by the RBS technique perhaps due to its ultra thin thickness and polycrystalline structure. The last oxide layer seen in both polysilicon samples was the pad oxide grown during processing. This oxide layer was used to isolate the polysilicon from the silicon substrate. Fig. 5.9 through 5.11 shows the SIMS results from the University of Florida.

SIMS: Poly_P+ (500°C, 20sec)

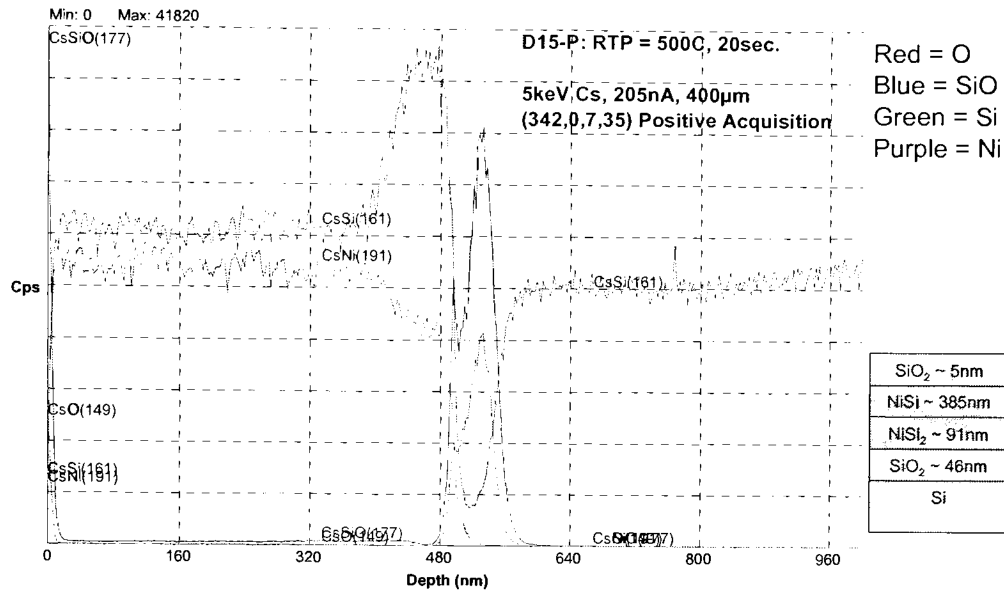


Fig. 5.9. SIMS result for sample D15-Poly_P+. Courtesy of Dr. Lambers, University of Florida

SIMS: Si_P+ (500°C, 20sec)

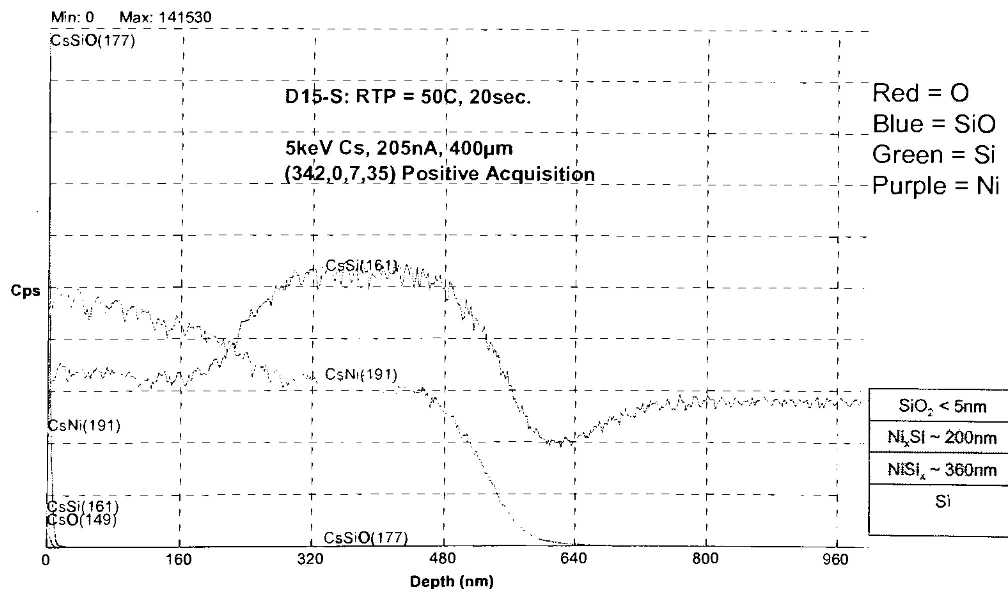


Fig. 5.10. SIMS result for sample D15-Si_P+. Courtesy of Dr. Lambers, University of Florida

SIMS: Poly_P+ (520°C, 20sec)

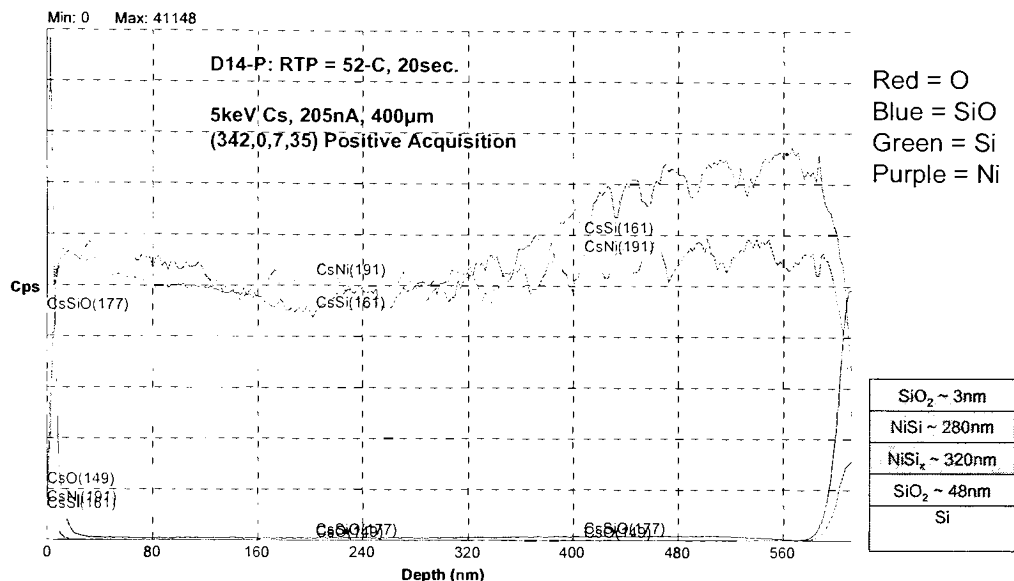


Fig. 5.11. SIMS result for sample D14-Poly_P+. Courtesy of Dr. Lambers, University of Florida

Based on the SIMS results, multi-phase silicides were visible in all three samples similar to those seen in XRD and possibly RBS results. Since the temperature range of all three samples was between 500°C to 520°C, such multi-phase results were expected based on XRD data. In the polysilicon region, D15-Poly_P+ showed primarily NiSi phase near the surface that accounted for about 80% of the entire silicide thickness. $NiSi_2$ was present toward the bottom of the layer near the pad oxide interface. The overall silicide thickness was about 476nm. D14-Poly_P+ also showed similar result with the existence of multi-phase silicide film. However, the exact ratio of the bottom film was not clear. In addition, the bottom $NiSi_x$ phase accounted for about 53% of the overall silicide layer. This suggested that the additional 20°C allowed for further conversion of the NiSi phase into more silicon rich silicide phase. The overall silicide thickness was

about 600nm. Silicide phase labeled with "x" subscript indicates ratio that did not fell within the three commonly known nickel silicide phases: Ni_2Si, NiSi, and $NiSi_2$.

Table 5.3. Detected film layer from surface down through SIMS analysis. Courtesy of Dr. Lambers, University of Florida.

Sample	RTP Temp (°C)	RTP Time (sec)	Detected Layer	Thickness (nm)
D15 - Poly_P+	500	20	1. SiO_2	~ 5
Silicide Thickness ~ 476 nm			2. NiSi	~ 385
			3. $NiSi_2$	~ 91
			4. SiO_2	~ 46
D15 - Si_P+	500	20	1. SiO_2	< 5
Silicide Thickness ~ 560 nm			2. Ni_XSi	~ 200
			3. $NiSi_2$	~ 360
D14 - Poly_P+	520	20	1. SiO_2	~ 5
Silicide Thickness ~ 600 nm			2. NiSi	~ 280
			3. $NiSi_X$	~ 320
			4. SiO_2	~ 48

In the crystalline silicon region, sample D15-Si_P+ also showed the presence of multi-phase silicide. However, the two phases seemed to be Ni_xSi and $NiSi_2$. Near the surface, Ni_xSi accounted for about 36% of the overall thickness. The monosilicide, NiSi, phase was debatably present near the transition point between Ni_xSi and $NiSi_2$. However, its presence was not clearly defined as in the polysilicon region. The overall silicide thickness was about 560nm. Notice that the silicide thickness in this crystalline silicon region was about 18% thicker than the corresponding polysilicon region. This was significantly less than the 36-42% seen with the RBS analysis. More merit should be entrusted in the SIMS percentage since SIMS analysis is more accurate, and it does not rely on the density assumption made with RBS calculation. SIMS technique is a physically damaging technique where ions are bombard against the sample surface to sputter away the sample material. As a result, a crater is created and the depth profile is acquired through profilometer measurements of this crater.

The thicker silicide layer in crystalline silicon also supported previous conclusion that silicidation was much faster in this region compare to polysilicon region. Notice the top silicide layer was thinner and the bottom layer was thicker on crystalline silicon sample compare to polysilicon. Similarly, the polysilicon sample at higher temperature (520°C) also showed thinner top and thicker bottom silicide thickness compare to corresponding sample at 500°C. Higher temperature seemed to enhance the silicidation process and aided in the conversion of the silicide mixture into more stable silicide phase, silicon rich phase.

5.5. Discussions

As previously mentioned, the silicide depth information obtained by grooving technique required an offset factor to represent the actual depth more closely. Based on the depth information obtained by RBS and SIMS analysis techniques, the correction factor seemed to vary between regions and temperature range. Within the temperature range of 400°C to 573°C, the average correction factor was ±157nm in crystalline region and ±70nm in polysilicon region. In addition, at 746°C, the average correction factor was ±52nm in both crystalline silicon and polysilicon regions. The dramatic drop in the correction value at higher temperature was due mainly to the fact that the boundaries were visually more defined in the optical microscope than at lower temperature.

With more accurate silicide thicknesses from RBS and SIMS techniques, the metal to silicide ratio could be calculated and compared to reference works. On average, 1nm of Ni metal yielded 1.389nm of nickel silicide based on RBS results and 1.65nm of nickel silicide based on SIMS results. Due to the unavoidable limitation of RBS technique,

SIMS results are more accurate since no assumption was made to calculate the silicide thickness. In comparison with literature reference, both experimental values obtained were below the referenced value of 2.2nm [1]. Froment and Muller experimental results confirmed the law of 1Ni + 1.84Si = 2.2NiSi [1]. Keep in mind that such referenced value was for pure NiSi phase silicide only. However, this was clearly not the case for this study since all results showed multi-phase silicide. Therefore, the value obtained from this study should not be the same as the referenced value.

Recall that the SIMS results showed evidence of the third nickel silicide phase, $NiSi_2$, in both silicon and polysilicon regions of sample D15. In addition, notice the silicidation temperature and time of all three SIMS samples. Both regions of sample D15 received 500°C for 20sec of RTP while sample D14 received 520°C for 20sec. In the polysilicon region, it was evident that at 500°C, the $NiSi_2$ phase was significantly thinner than the NiSi phase. On the other hand, at 520°C, the $NiSi_x$ phase was thicker than the NiSi phase. Notice the "x" ratio was less than that of "2" as characteristic of $NiSi_2$. Zhang and Ivey have observed nickel silicide formation sequence during direct depositions to be $NiSi_2$, followed by Ni_2Si, NiSi, and finally to a nickel rich silicide as being the first stable phase [6]. This observation was seen during direct deposition of nickel metal onto heated silicon substrate in a vacuum environment of less than 2×10^{-6} torr. Most importantly, their experimental results showed local epitaxial growth of Ni_2Si and NiSi on the initial $NiSi_2$ layer. Such results seen by this group could be related to the SIMS results of this study. For this study, it is highly possibly that the $NiSi_2$ phase seen at the bottom of the silicide film was part of the initial $NiSi_2$ phase formed at the start of the silicidation, and the upper Ni_xSi and NiSi phases were formed as observed by Zhang's experiment. Since

the silicidation time was significantly shorter than all other samples (20 sec), the presence of $NiSi_2$ was still detected by SIMS analysis for these three samples.

Notice that $NiSi_2$ was not detected in these three samples through XRD analysis. There are three signature peaks for $NiSi_2$ within the 2θ range scanned. However, its primary peak at about 47.5° coincides with one of Ni_2Si primary signature peak, and the remaining two signature peaks of coincide with that of NiSi and Si. Therefore, the strong presence of Ni_2Si and NiSi phases could have possibly drown out the detection of $NiSi_2$ in the XRD analysis. Such similarity in signature peaks requires $NiSi_2$ be the only single phase or the most dominant phase in a multi-phase mixture in order to be sufficiently detected by XRD analysis. Other possibility for not detecting NiSi2 in the XRD analysis could be due to the longer silicidation time of all samples analyzed by XRD. The longer time could allow for the complete transformation of the initial $NiSi_2$ phase into the stable phases, Ni_2Si and/or NiSi.

5.6. Conclusion

The material analytical techniques are used successful in characterizing the material characteristics of nickel silicidation. AFM analysis is used to obtain the surface morphology of nickel silicide. Such results are successfully correlated to the electrical resistivity of the silicide film. XRD analysis is used to identify the most dominant silicide phase(s), RBS analysis is used to extend the characterization and obtain the phase composition as well as the overall thickness of nickel silicide, and SIMS analysis is used to complement the RBS technique in obtained the stated information. Overall, these analytical techniques are successful in obtaining the information of interest. In addition,

the information obtained from each technique is successfully used to validate common characteristics of the silicide films.

Reference

[1] B. Froment, M. Muller, "Nickel vs. Cobalt Silicide Integration for Sub-50nm CMOS," ESSDERC, pp.215-218, (2003).
[2] K. Maex, M. Rossum, Properties of Metal Silicides, Datareviews Series No. 4, INPSEC, London, United Kingdom, (1995).
[3] J. Seger, "Interaction of Ni with SiGe for Electrical Contacts in CMOS Technology", Doctoral Thesis,IMIT, Royal Institute of Technology, Stockholm, Sweden, (2005).
[4] L. Zhang, D. Ivey, "Prediction of Silicide Formation Sequence from the Principle of the Largest Free Energy Degradation Rate," Mat. Res. Soc. Symp. Proc. Vol. 311, pp 299-304, (1993).
[5] K. Maex, M. Rossum, Properties of Metal Silicides, Datareviews Series No. 4, INPSEC, London, United Kingdom, (1995).
[6] L. Zhang, D. Ivey, "Direct Deposition Reactions Between Nickel and Silicon Substrates," Mat. Res. Soc. Symp. Proc. Vol. 311, pp 335-340, (1993).

6. Closing Summary

Various electrical and material analytical techniques are utilized to study the overall characteristics of nickel silicide at varying silicidation time and temperature. There is a strong correlation between the material characteristics of nickel silicide and its electrical properties. The existence of multi-phase nickel silicide, predominantly Ni_2Si and NiSi, is observed and confirmed by several analytical techniques as well as published works. It is observed that low electrical resistivity was generally characterized by higher degree of silicide's surface roughness. Furthermore, the increased in silicidation temperature from 400°C to 695°C yields higher surface roughness and consequently lower resistivity. In addition, the continued increase in temperature beyond 695°C results in lower surface roughness and higher resistivity. Such observation could be a result of multi-phase silicide mixture involving Ni_2Si and NiSi. XRD results strongly suggest the primary reason for such increase in resistivity is due to reformation the earlier Ni_2Si phase in the silicide mixture. This observation is also confirmed by RBS analysis. The reasoning for such reoccurrence is not well understood at this time.

Concerning the method of obtaining silicide's thickness through grooving, the technique works and can be used as a quick way to estimate the thickness of nickel silicides. The average correction factor is found to be ±157nm in crystalline silicon region and ±70nm in polysilicon region for the temperature of 400°C to 573°C. At temperature of 746°C, the correction factor reduces to an average of ±52nm in both regions due to visually more defined silicide boundaries in the optical microscope.

In addition, it is observed and confirmed by all utilized analytical techniques that the silicidation is much faster in crystalline silicon than in polysilicon regions. As observed

in previous work, the reason is believed to be due to the reduction of nickel diffusion coefficient in polysilicon by six to eight orders of magnitude due to interstial traps. Furthermore, the silicidation temperature range where the most dominant nickel silicide phase was NiSi is identified to be between 573°C to 695°C and 695°C for crystalline silicon and polysilicon regions respectively. Table 6.1 and 6.2 show the conclusion summary and the optimal nickel silicidation conditions that yield the thinnest silicide thickness without substantial sacrifice of electrical resistivity as well as the lowest electrical resistivity that is best for IC device integration. Only silicidation temperature has significant impact on the overall silicide's resistivity as well as its primary phase formation. However, the silicidation time does seem to influence the overall phase composition of the multi-phase silicide film but not significantly enough to change the overall electrical resistivity of the silicide film.

Table 6.1. Result Summary

- Surface Roughness RMS
  - @ fix temp, longer time = moderately higher RMS
  - @ fix time, higher temp = higher RMS
  - Lower ρ = higher RMS
- Phase Composition
  - Ni_2S + NiSi mixture in temp 400°C – 573°C, NiSi ratio increase with higher temp
  - Single phase NiSi at 695°C for both poly & Si regions
  - Reoccurrence of Ni_2Si + NiSi mixture at 746°C
- Silicide Thickness
  - <100nm at temp = 400°C
  - ~625nm (Si), ~450nm (Poly) at temp >400°C
- Resistivity
  - @ 400°C
    - Si ~ 1.6×10^{-4} Ω-cm, Poly ~ 3.3×10^{-4} Ω-cm
  - @ 450C – 750°C
    - Si ~ 3.1×10^{-5} Ω-cm, Poly ~ 6.1×10^{-5} Ω-cm

Table 6.2. Conclusion Summary and Optimal Condition

- **Temp : 400°C**
  - ρ ~ 9×10^{-5} to 3×10^{-4} Ω-cm
  - Phase ~ Ni_2Si + NiSi mixture, mostly Ni_2Si
  - RMS ~ 2.6nm (Si), 3.1nm (Poly)
  - Thickness ~ [RBS]

- **Temp : 450°C – 700°C**
  - ρ ~ 2×10^{-5} to 4×10^{-5} Ω-cm
  - Phase ~ Ni_2Si + NiSi mixture
    (more NiSi at higher temperature)
  - RMS ~ 8.0-28.0nm (Si), 5.5-10.0nm (Poly)
  - Thickness ~ 549nm (Si), 485nm (Poly) [RBS, SIMS]

- **Temp : 750°C**
  - ρ ~ 2×10^{-5} to 8×10^{-5} Ω-cm
  - Phase ~ Ni_2Si + NiSi mixture
  - RMS ~ 16.1nm (Si), 6.5nm (Poly)
  - Thickness ~ 529nm (Si), 387nm (Poly) [RBS]

- **Optimal Condition:**
  - **Lowest ρ:500°C, ≥ 20sec**
  - ρ ~ 1.6×10^{-5} (Si), 2.5×10^{-5} Ω-cm (Poly)
  - Phase ~ Ni_xSi + NiSi mixture
  - RMS ~ 8.9nm (Si), 7.1nm (Poly) at 20sec
  - Thickness ~ 560nm (Si), 576nm (Poly) [SIMS]

  - **Optimal Silicide: 695°C, 60sec**
  - ρ ~ 1.6×10^{-5} (Si), 3.3×10^{-5} Ω-cm (Poly)
  - Phase ~ NiSi
  - RMS ~ 26.6nm (Si), 8.6nm (Poly)

Future Work

Additional work is needed to extend the silicidation temperature range of this study in order to observe the most dominant silicide phase in the multi-phase mixture to be $NiSi_2$. It is believed that such dominant phase should be observable and detectable with higher silicidation temperature. Furthermore, more experimental samples should be processed within the silicidation temperature range of 573°C to 746°C to obtain a clearer understanding of the phase(s) composition of nickel silicide and the reasoning for the reoccurrences of Ni_2Si at 746°C.

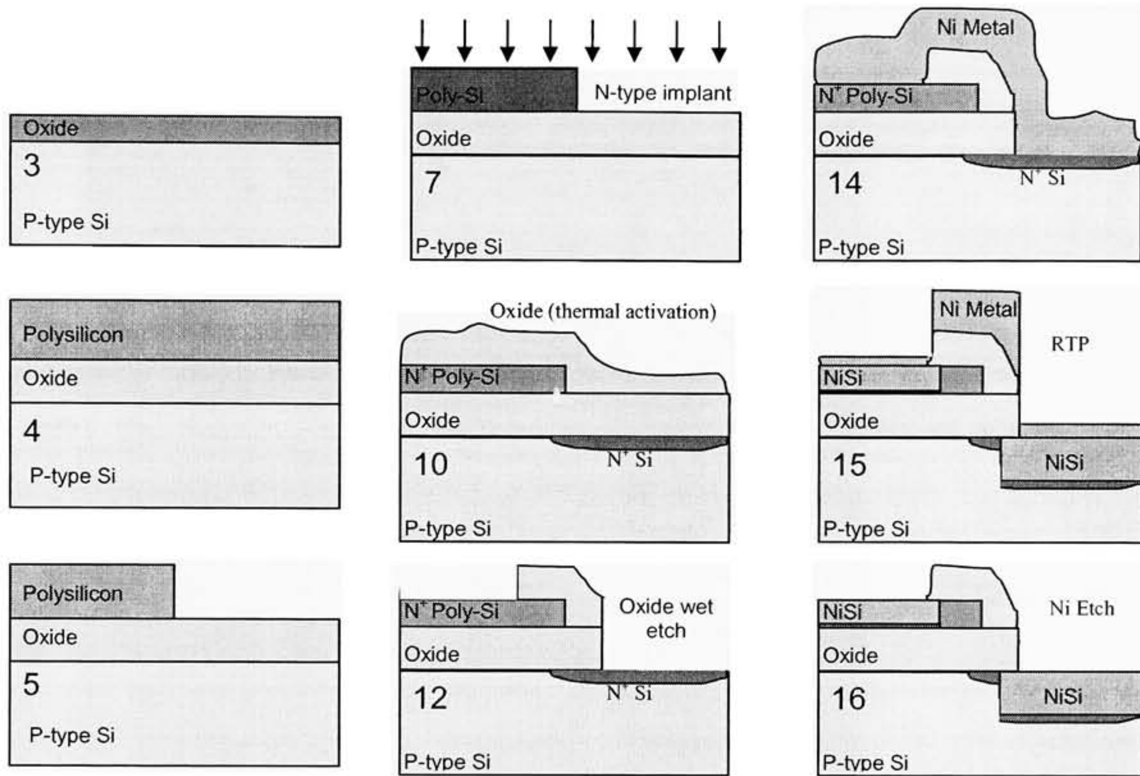
This study was successful in developing the fabrication process and obtaining the necessary silicidation temperature/time to achieve significantly low nickel silicide's electrical resistivity. However, further work is needed to implement the developed process into a CMOS transistor fabrication process to determine compatibility. Nonetheless, this study was successful in meeting the proposed objectives and should be useful in future implementation of nickel silicide into RIT CMOS designs and fabrications.

APPENDIX

1. Fabrication Process Procedures

Step	Process	Comments
1	Measure sheet resistance	
2	RCA clean	
3	Grow thin thermal oxide	Target ~ 500Å
4	Grow polysilicon film	Target ~ 2000Å
5	Etch polysilicon by wet chemistry	
6	Coat and develop resist to cover non-doped half of wafers.	RIT 6" WaferTrac, standard coat and develop recipes.
7	S/D dopant implantation	P31 Dose - 2E15 Energy - 75 KeV
8	Strip off photo resist in wet chemistry	
9	RCA Clean	
10	Thermal S/D anneal	BRUCE 01 TUBE 02 846 1000C S/D ANNEAL
11	Coat and develop resist to cover middle of wafer over poly and silicon intersection.	This is to protect the oxide at the center of the wafer from being etch off. This will form the necessary divider between polysilicon and silicon regions during silicidation.
12	Etch off any oxide on polysilicon and silicon substrate	HF dip immediately prior to metal deposition
13	Measure sheet resistance	
14	Deposit nickel metal	Target ~ 3000Å
15	RTP anneal	Vary temperature & time
16	Remove any un-reacted Ni metal	Wet chemistry; 90°C for 60sec in 1 part H_2SO_4 : 2 part H_2O_2
17	Data collection. Measure sheet resistance.	

2. *Fabrication Process Cross-Sectional Diagram*

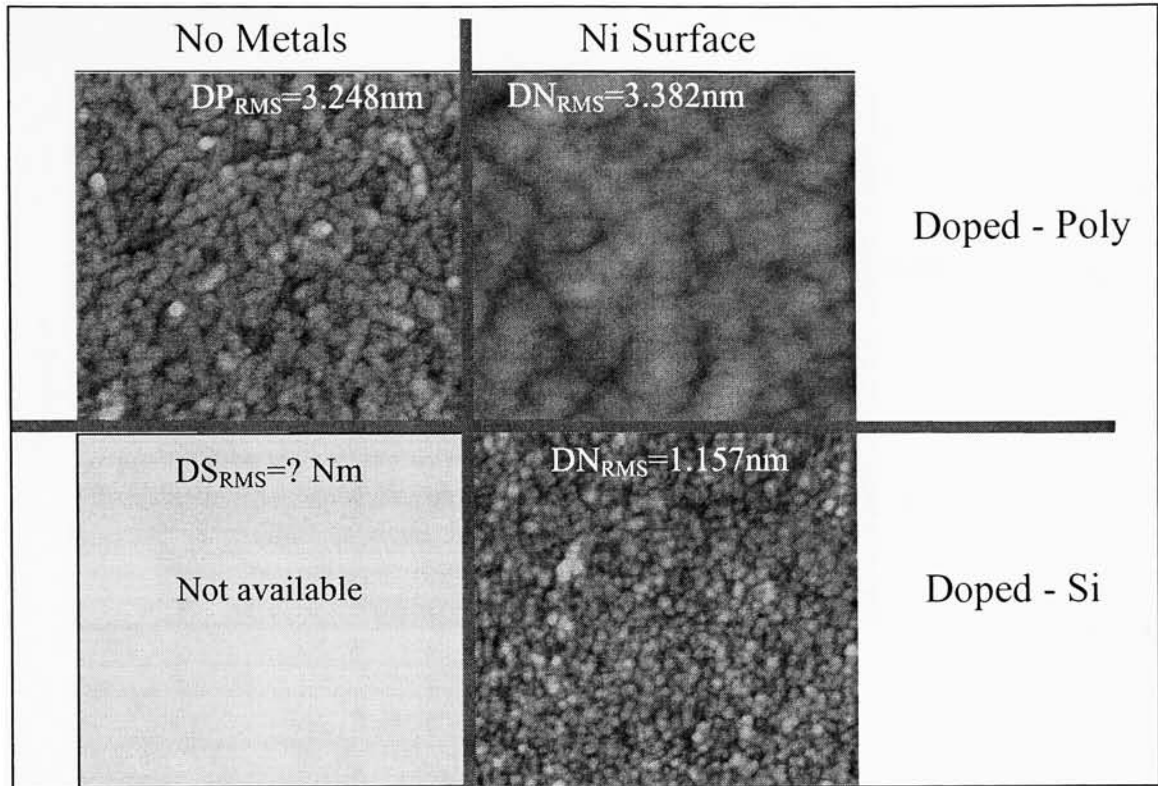


3. *Design of Experiment*

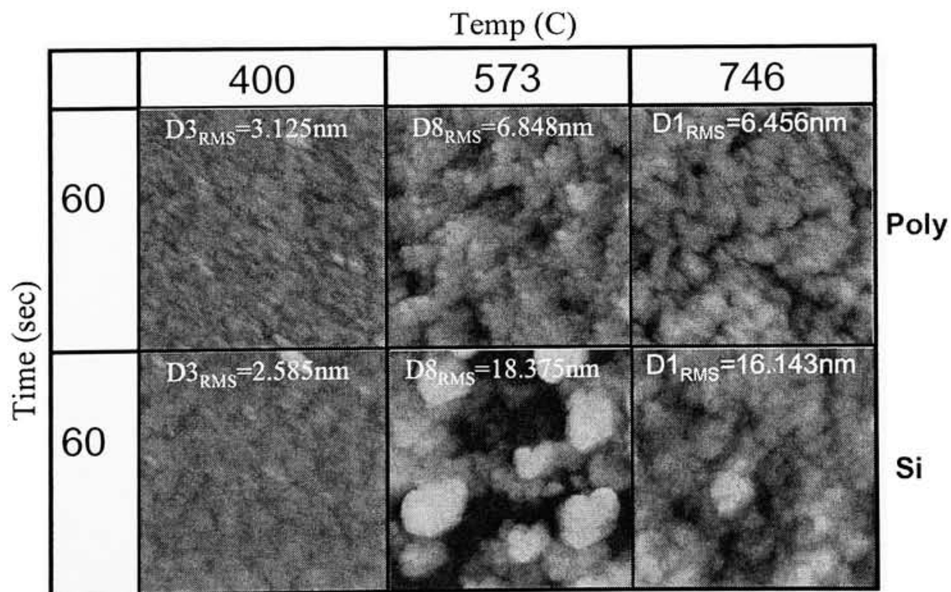
Central Composite Design (CCD)

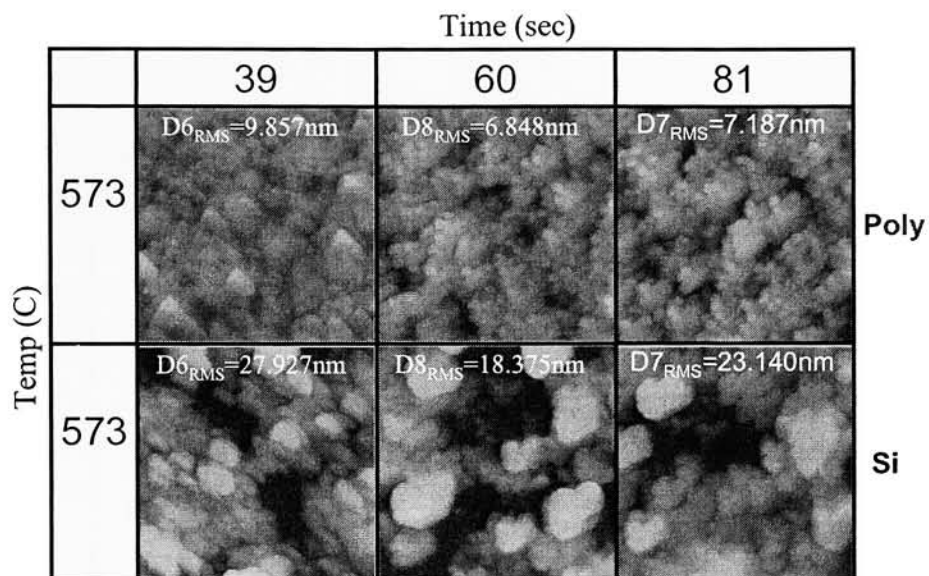
Pattern	Wafer ID	Temp (C)	Time (s)
--	D4	450	45
-+	D5	450	75
+-	D11	695	45
++	D12	695	75
a0	D3	400	60
A0	D1	746	60
0a	D6	573	39
0A	D7	573	81
0	D8	573	60
0	D9	573	60

4. Raw AFM Data



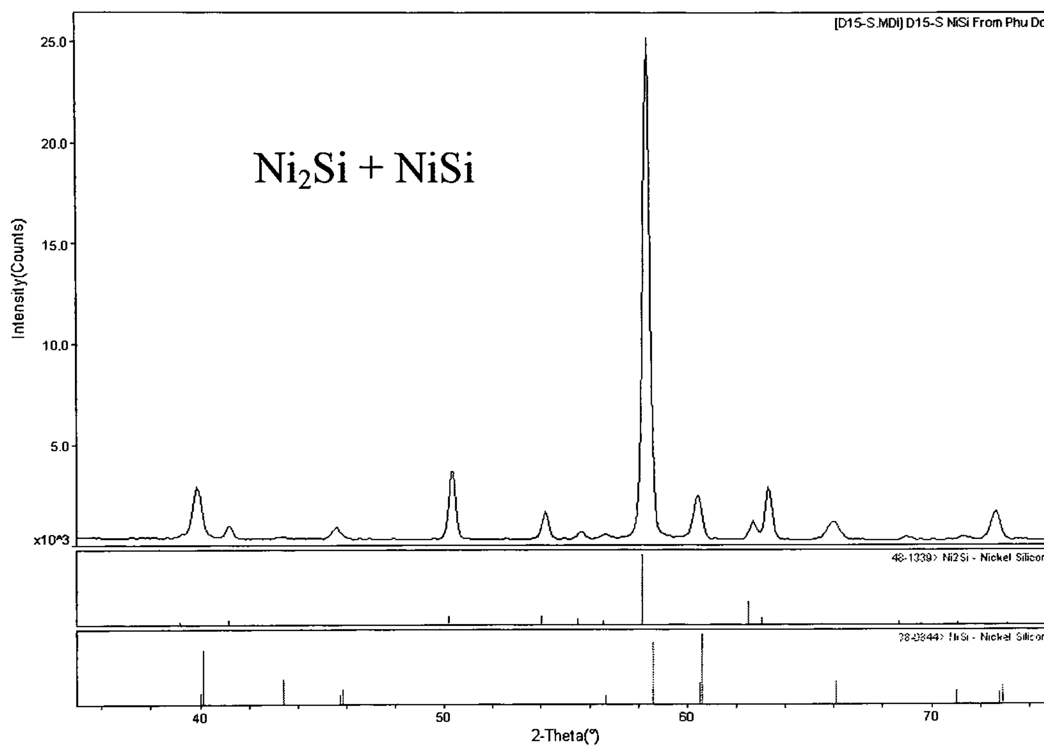
Constant Time: **Poly-I & Si** Region



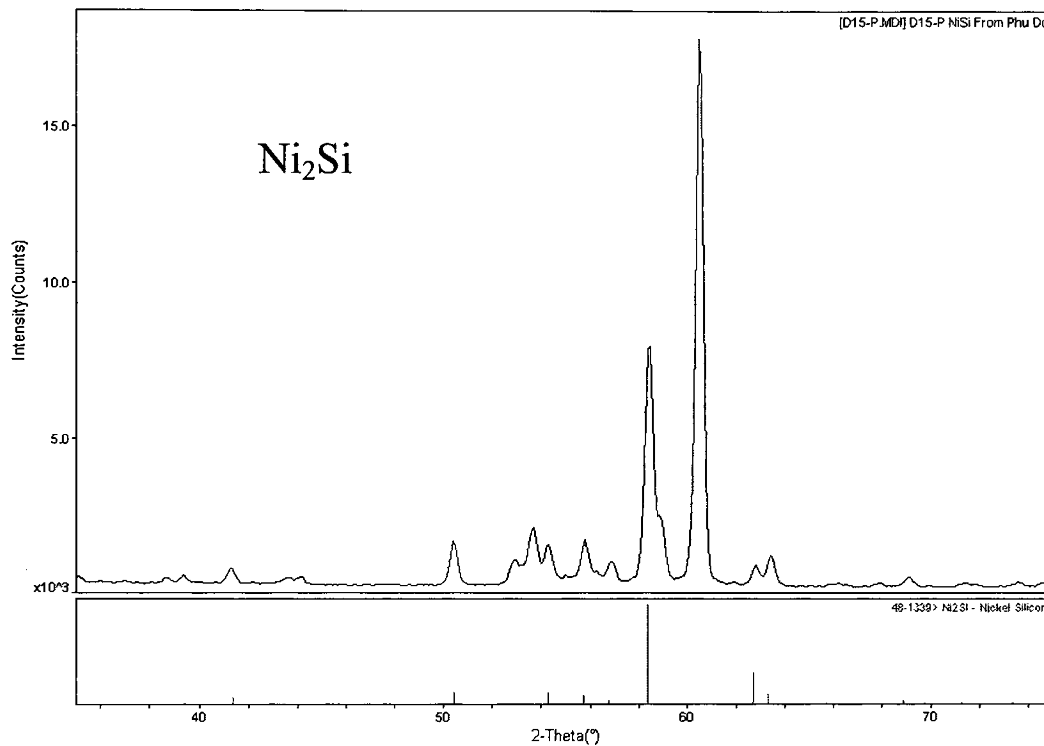

Constant Temp: Poly-I & Si Region
Time (sec)
39
60
81
Temp (C)
573
573
D6RMS=9.857nm
D8RMS=6.848nm
D7RMS=7.187nm
D6RMS=27.927nm
D8RMS=18.375nm
D7RMS=23.140nm
Poly
Si

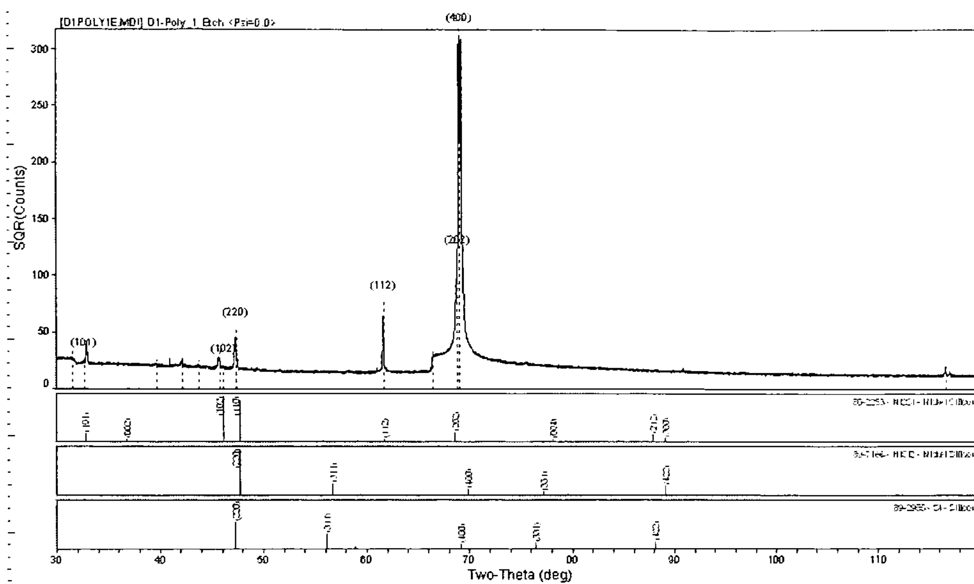
5. Raw XRD Data

Sample D15 Si_P+ (IBM)



Sample D15 Poly_P+ (IBM)




[D1POLY1E.MDI] D1-Poly_1_Etch <Psi=0.0>
(400)
SQR(Counts)
300
250
200
150
100
50
0
(202)
(112)
(220)
(101)
(102)
30
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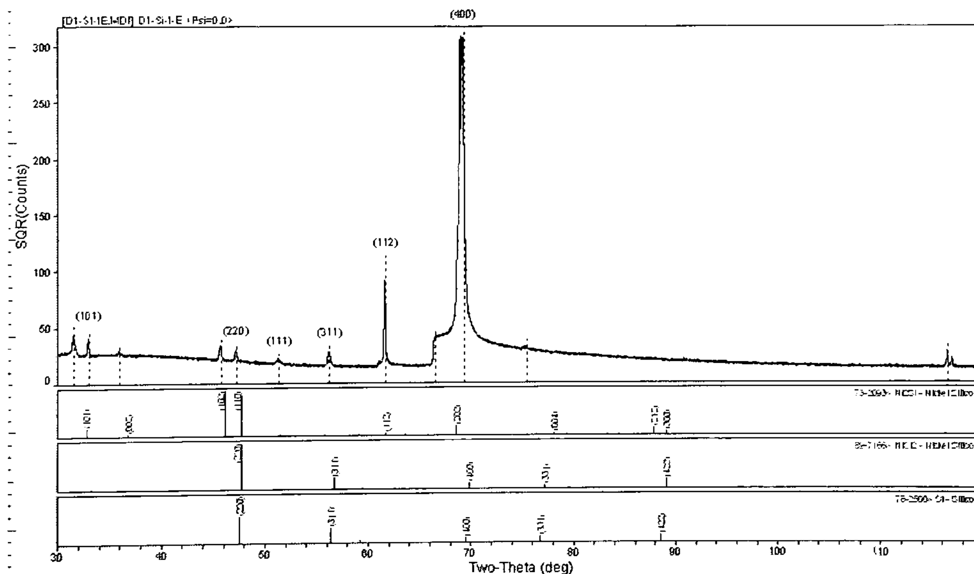
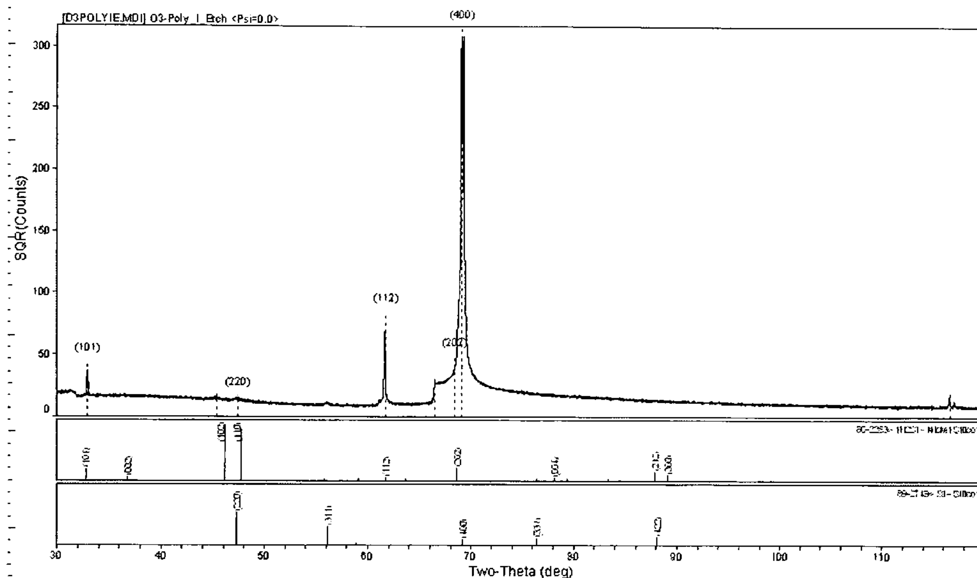
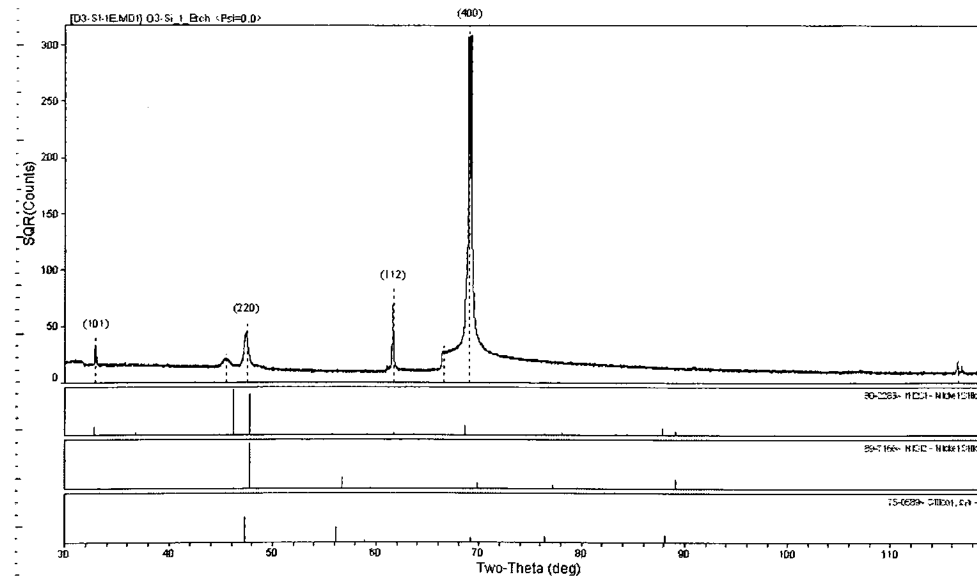
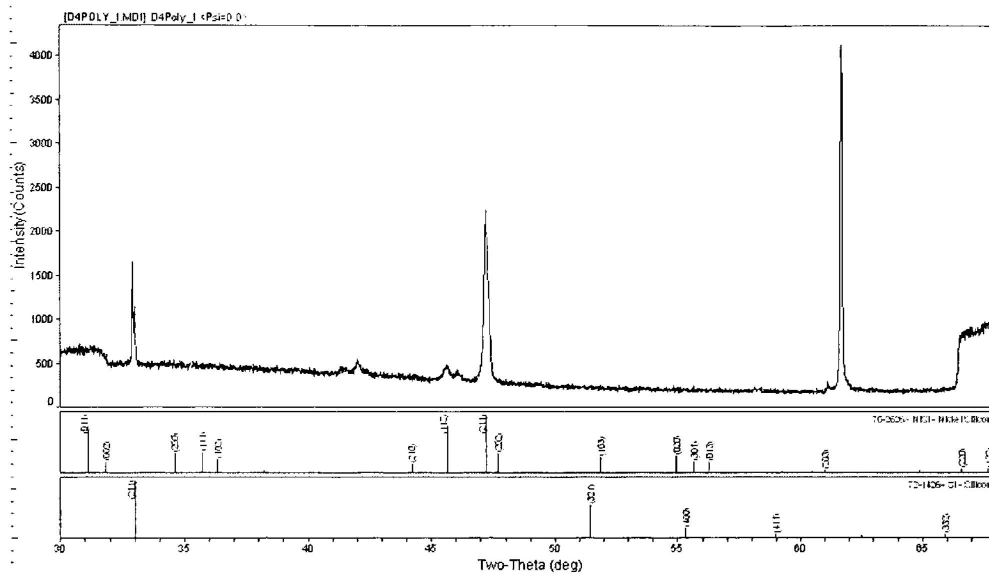
Two-Theta (deg)
RIT
<c:\DATASCAN\DATA-05\PHUDO\DOE-1> Saturday, Jul 09, 2005 07:57p (MDI/JADE8)


[D1-Si-1E.MDI] D1-Si-1-E <Psi=0.0>
(400)
SQR(Counts)
300
250
200
150
100
50
0
(112)
(101)
(220)
(111)
(311)
30
40
50
60
70
80
90
100
110
Two-Theta (deg)
RIT
<c:\DATASCAN\DATA-05\PHUDO\DOE-1> Saturday, Jul 09, 2005 07:59p (MDI/JADE8)

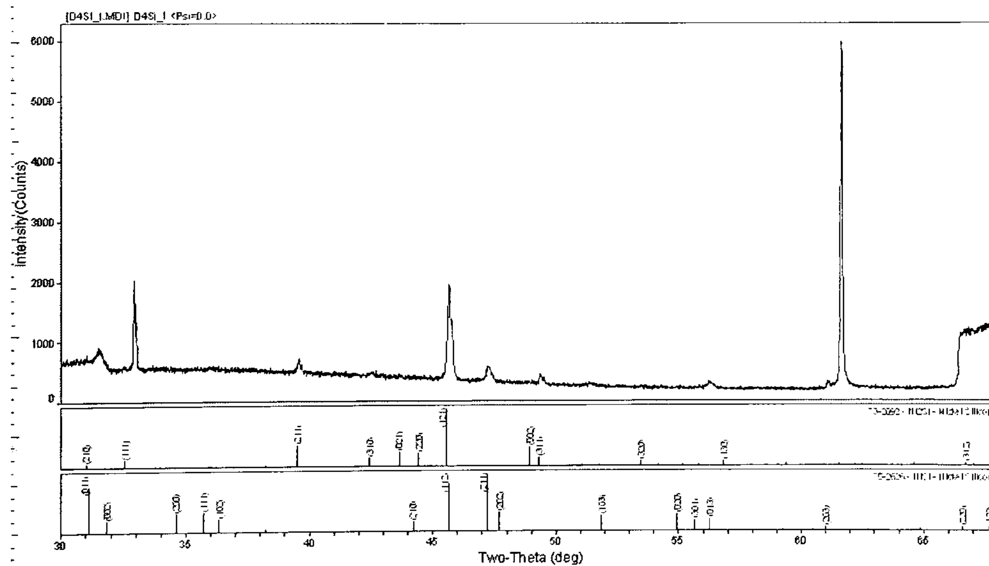

[D3POLYIE.MDI] O3-Poly_I_Etch <Psi=0.0>
(400)
(112)
(101)
(202)
(220)
SQR(Counts)
Two-Theta (deg)
RIT


[D3-SI-IE.MDI] O3-Si_I_Etch <Psi=0.0>
(400)
(112)
(220)
(101)
SQR(Counts)
Two-Theta (deg)
RIT



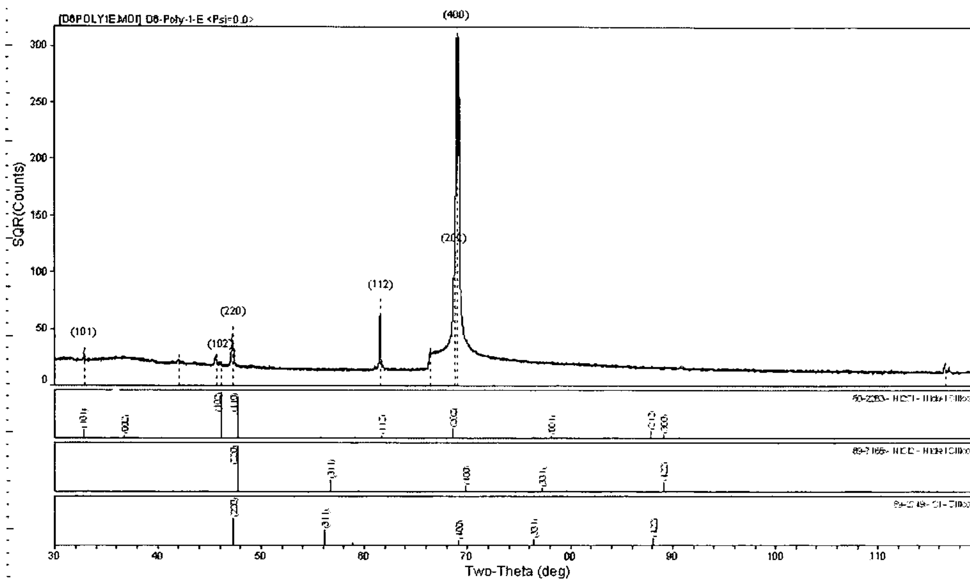
RIT

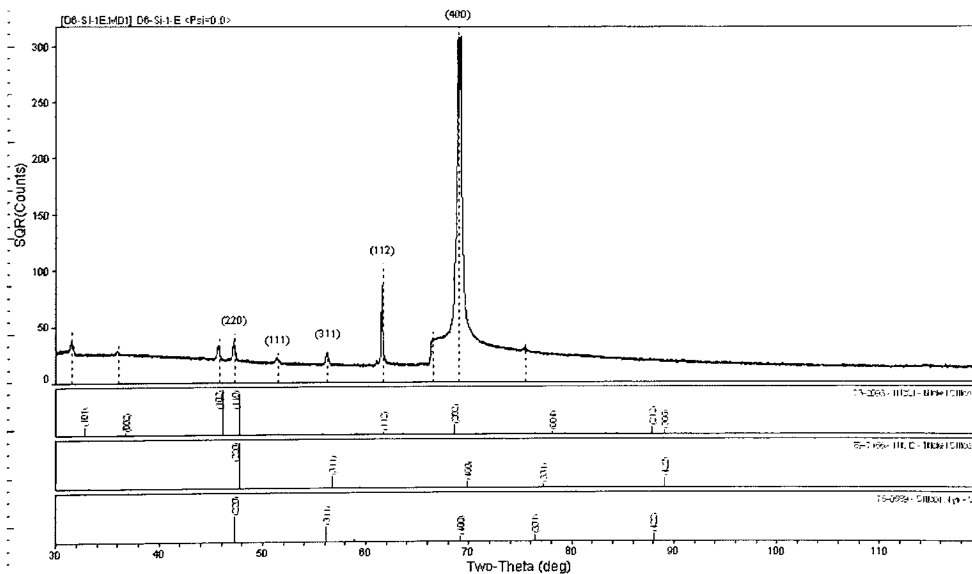
<c:\DATASCAN\DATA-05\PHUDO\DOE3> Friday, Dec 09, 2005 08:55p (MDI/JADE6)

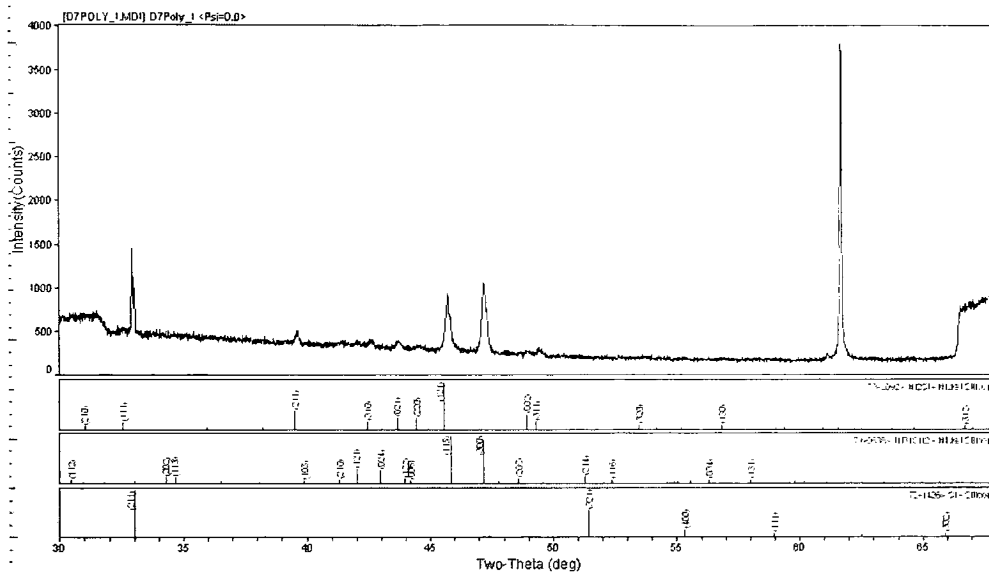


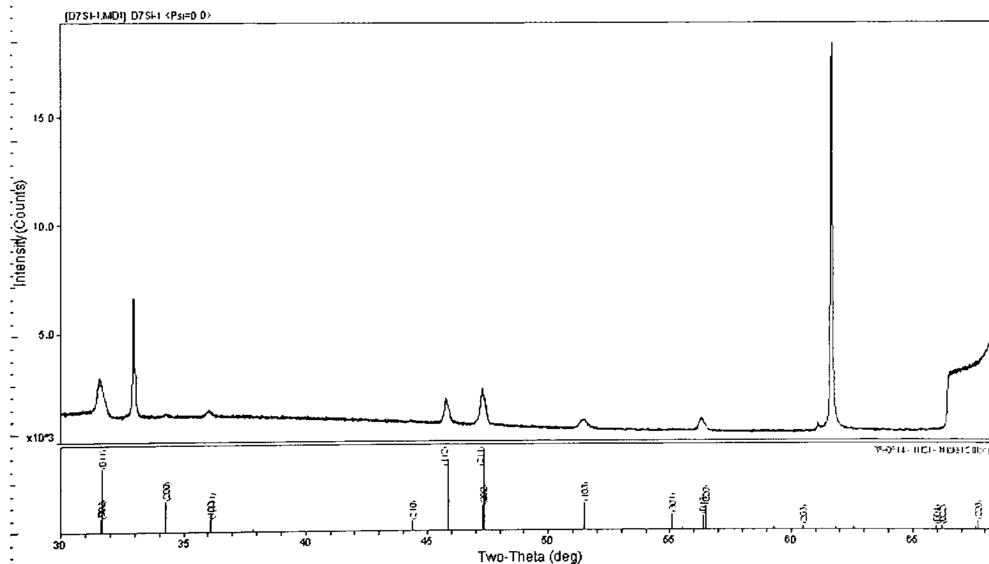
RIT

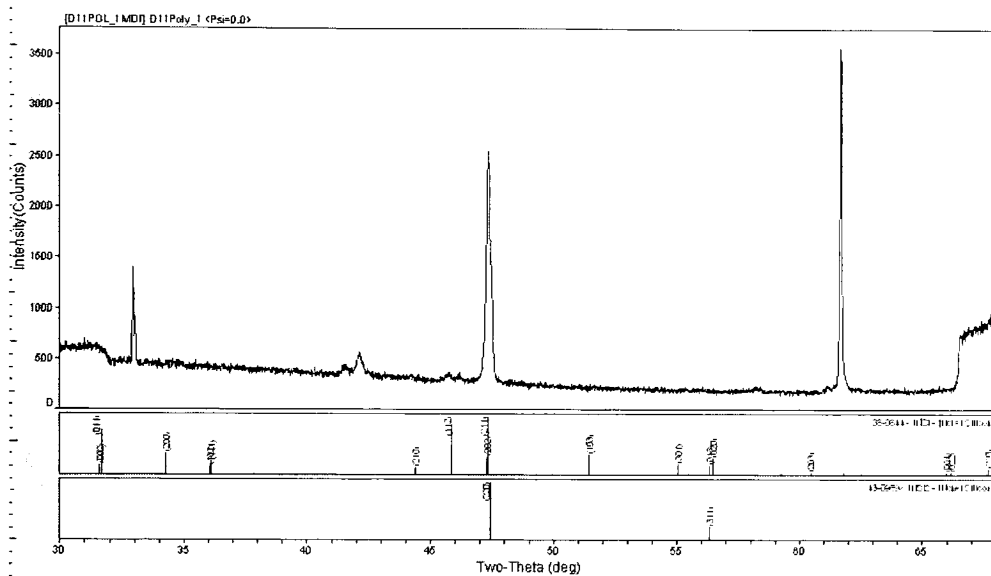
<c:\DATASCAN\DATA-05\PHUDO\DOE3> Friday, Dec 09, 2005 07:07p (MDI/JADE6)


[D6POLY1E.MDI] D6-Poly-1-E <Psi=0.0>
(400)
(200)
(112)
(220)
(101)
(102)
SQR(Counts)
Two-Theta (deg)
RIT
<o:\DATASCAN\DATA-05\PHUDO\DOE-1> Saturday, Jul 09, 2005 08:01p (MDI/JADE8)


[D6-SI-1E.MDI] D6-Si-1-E <Psi=0.0>
(400)
(112)
(220)
(111)
(311)
SQR(Counts)
Two-Theta (deg)
RIT
<o:\DATASCAN\DATA-05\PHUDO\DOE-1> Saturday, Jul 09, 2005 08:02p (MDI/JADE8)

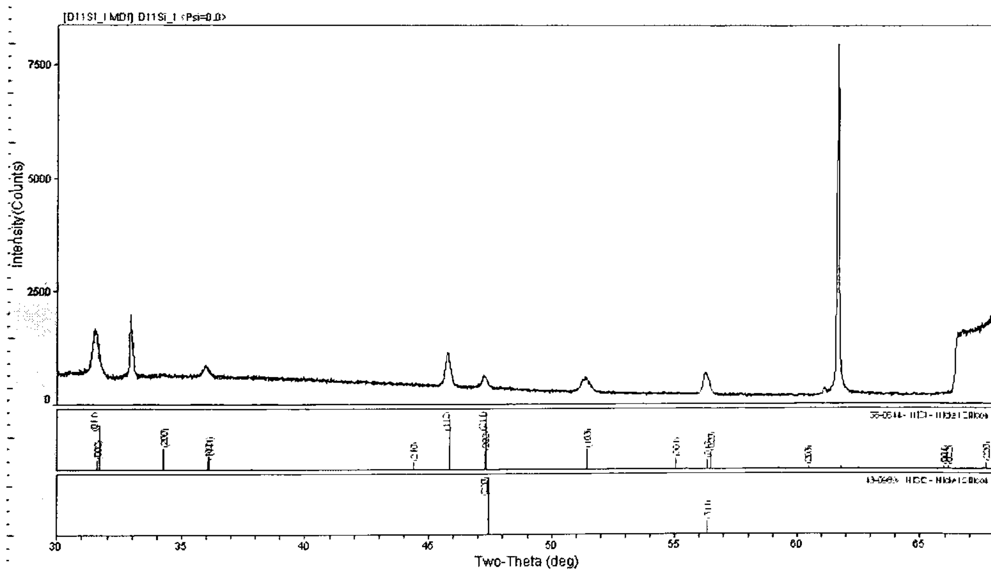

[D7POLY_1.MDI] D7Poly_1 <Psi=0.0>
Intensity(Counts)
Two-Theta (deg)
RIT
<c:\DATASCAN\DATA-05\PHUDO\DOE3> Friday, Dec 09, 2005 07:13p (MDI/JADE6)


[D7SI-1.MDI] D7SI-1 <Psi=0.0>
Intensity(Counts)
x10^3
Two-Theta (deg)
RIT
<c:\DATASCAN\DATA-05\PHUDO\DOE2> Friday, Dec 09, 2005 04:02p (MDI/JADE6)



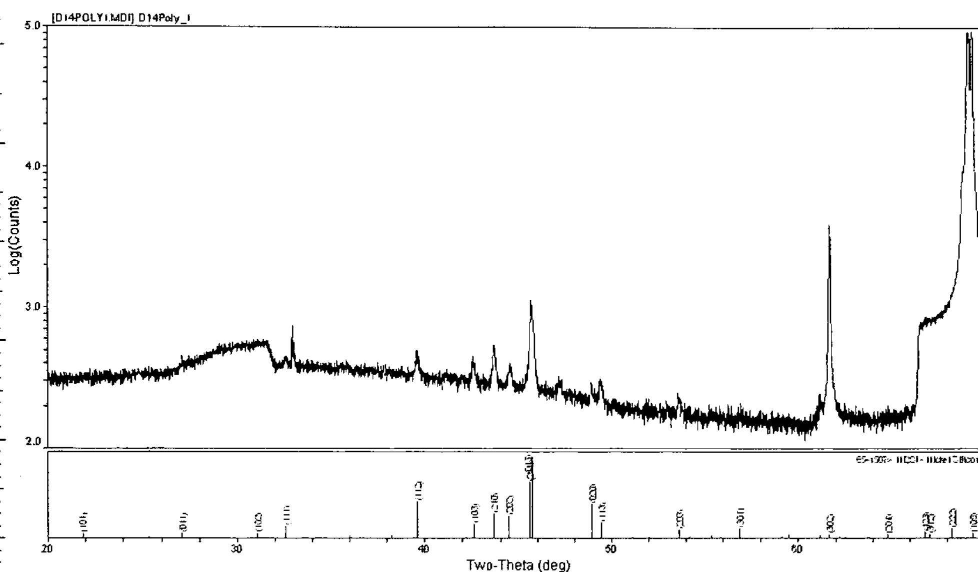
RIT

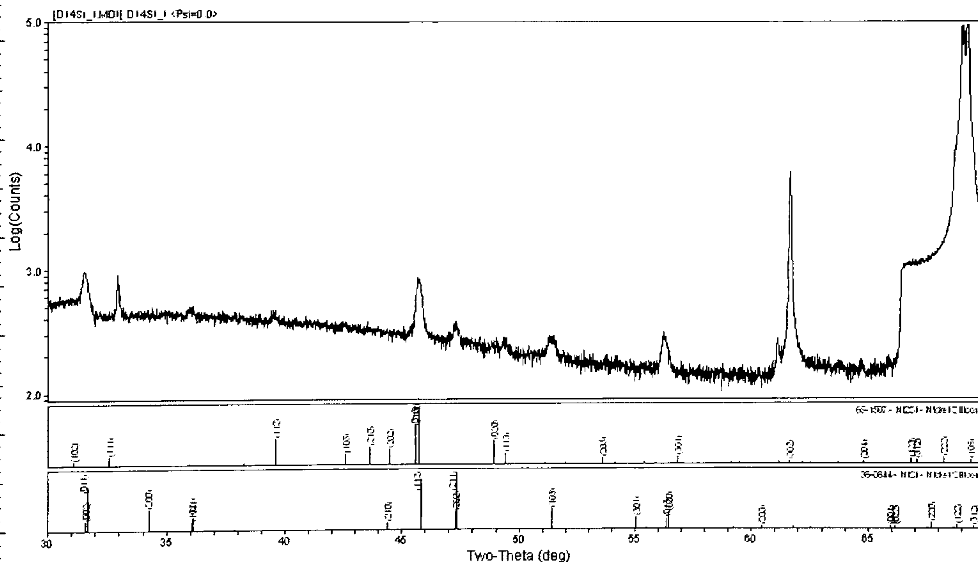
<o:\DATASCAN\DATA-05\PHUDD\DDE3> Friday, Dec 09, 2005 05:59p (MDI/JADE6)



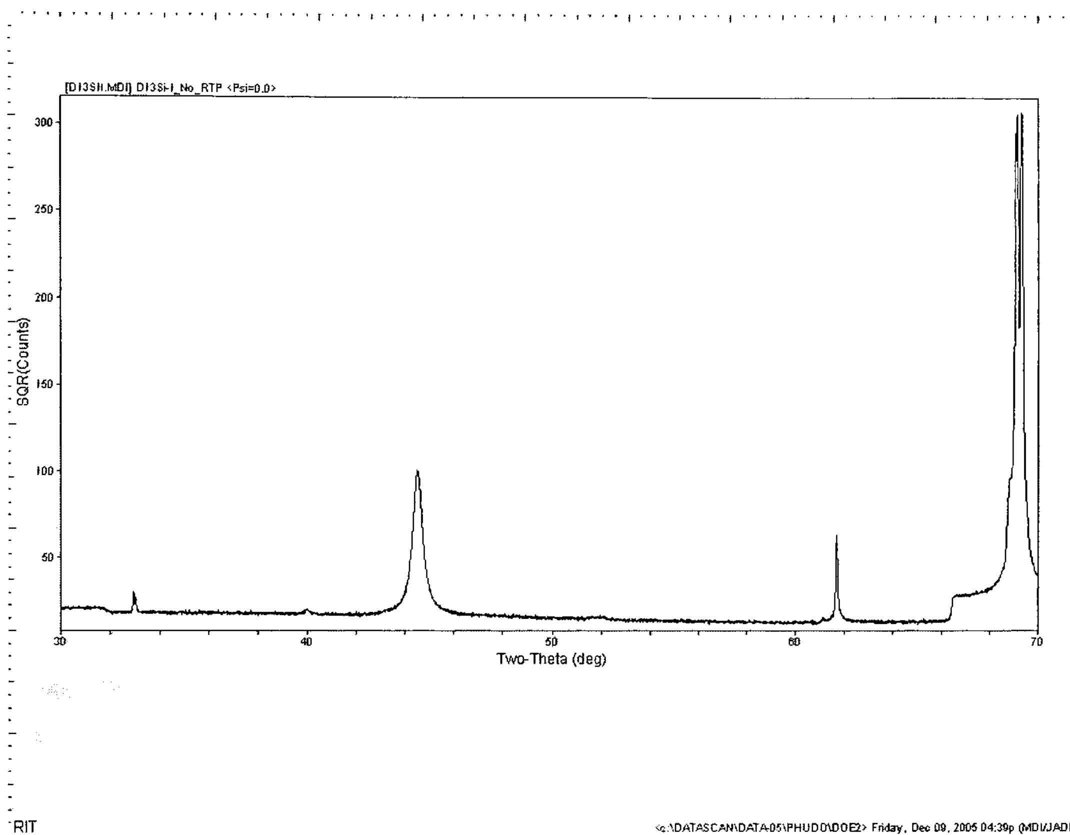
RIT

<o:\DATASCAN\DATA-05\PHUDD\DDE3> Friday, Dec 09, 2005 06:00p (MDI/JADE6)


Log(Counts)
5.0
4.0
3.0
2.0
20
30
40
50
60
Two-Theta (deg)
RIT
<o:\DATASCAN\DATA-05\PHUDO\DOE3> Friday, Dec 09, 2005 04:57p (MDI/JADE8)

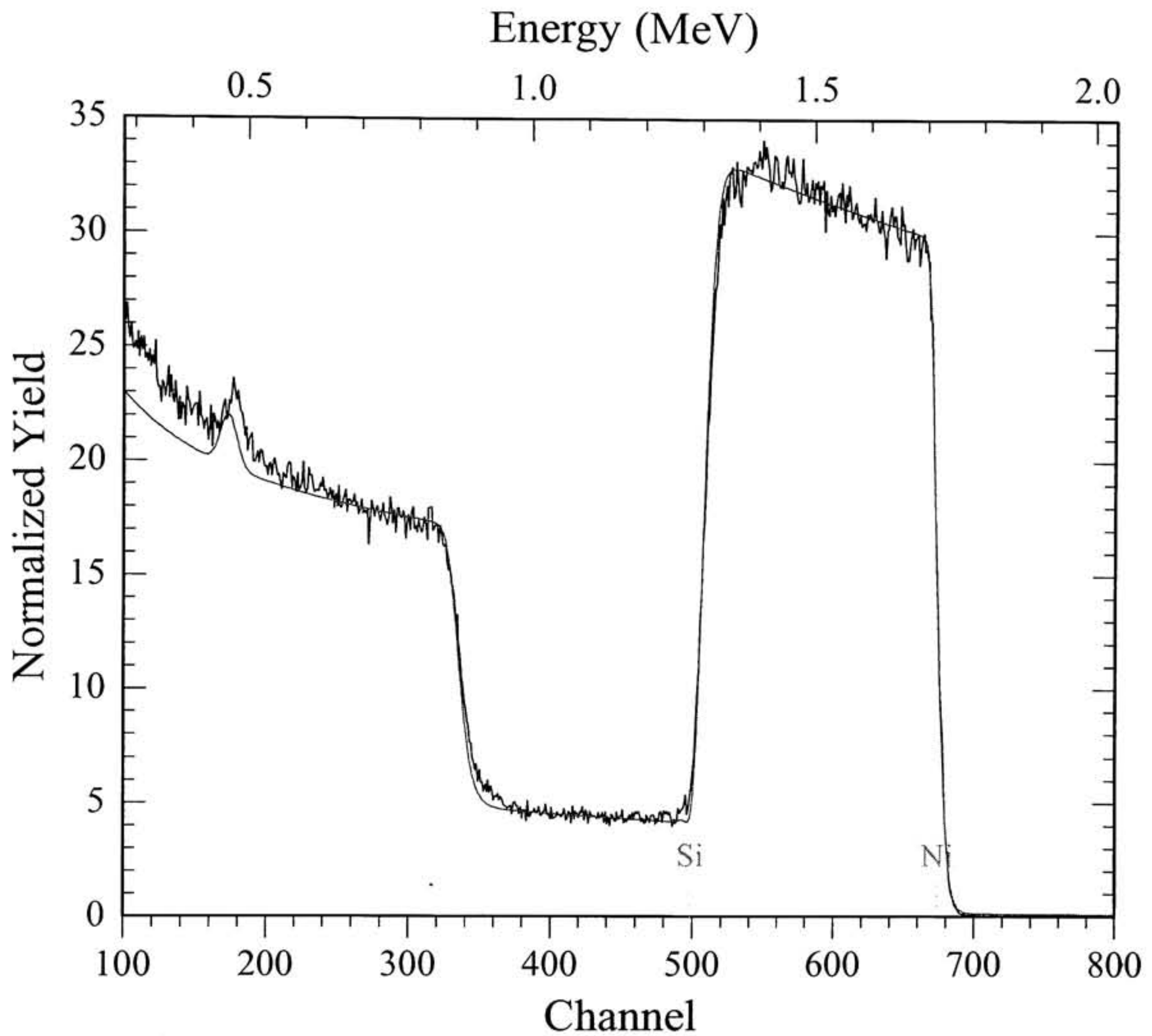

Log(Counts)
5.0
4.0
3.0
2.0
30
35
40
45
50
55
60
65
Two-Theta (deg)
RIT
<o:\DATASCAN\DATA-05\PHUDO\DOE3> Friday, Dec 09, 2005 05:26p (MDI/JADE8)

Reference Ni Metal Sample without RTP Anneal



6. Raw RBS Data

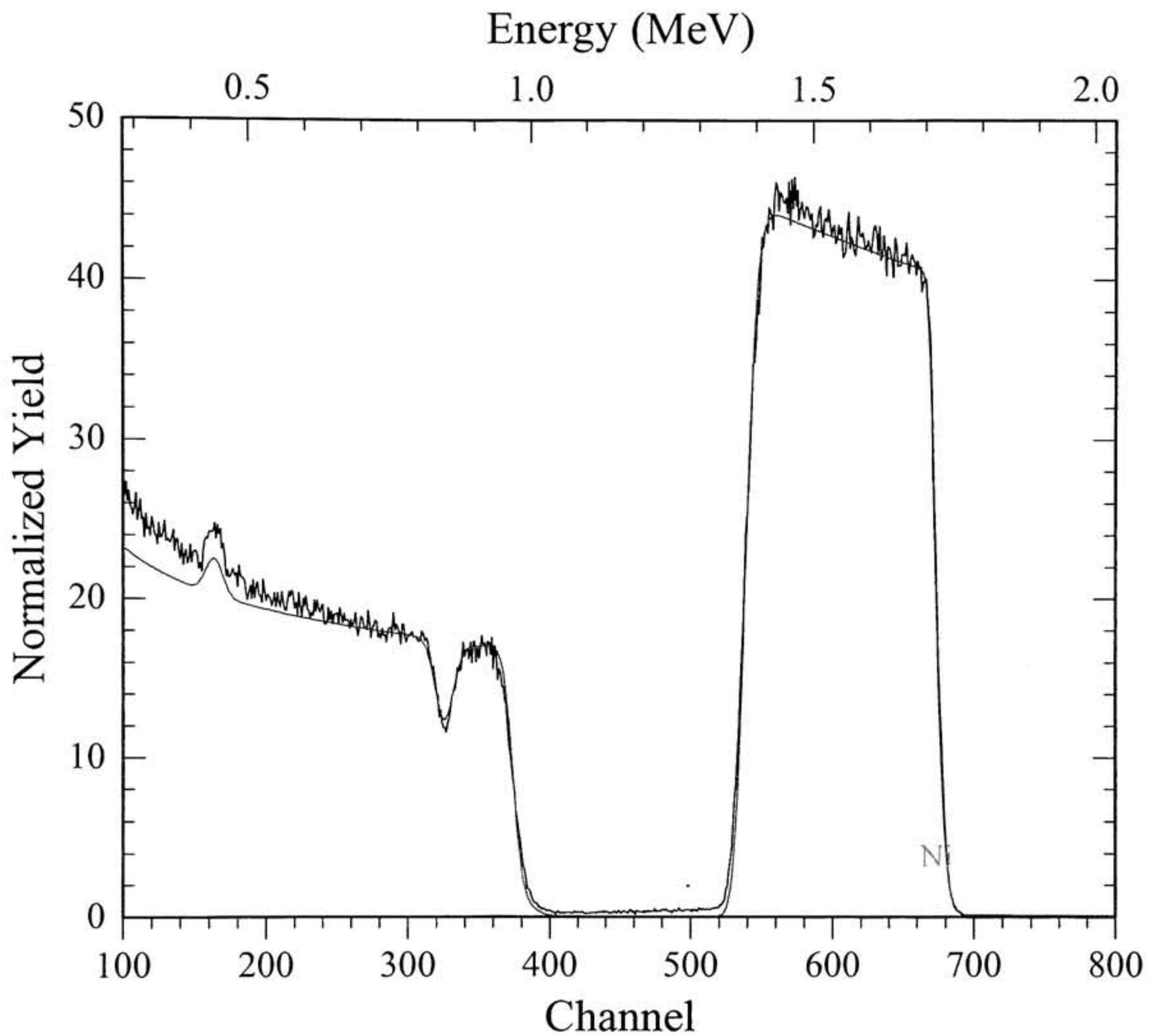
1) Sample D6 Poly_P+




```
XRump
File/Plot  Window  Layout  Edit  Variables  Help
Beam me up Scottie! sim show
  #          Thickness            Sublayers      Composition  . . .
* 1          3525.00  /CM2          auto          Ni    0.650      Si    0.350
  2           415.00  SiO2          auto          Si    1.000      O     2.000
  3         40000.00  /CM2          auto          Si    1.000
================================================================================
SIM Command: active
  RBS  File:     c:\rumpdata\oct1005\0029_02n.rbs
  Identifier:    RIT 6P
  LTCT Text:     Not implemented
  Date:          10/10, 09:45:33
  Beam:          2.250 MeV   4He++      20.00 uCoul  @ 13.55 nA
  Geometry:          IBM  Theta:     8.00  Phi:    15.00  Psi:  615.00
  MCA:           Econv:    2.509    29.320  First chan:   0.0  NPT: 1024
  Detector:      FWHM: 18.0 keV  Tau: 10.0    Omega: 4.000
  Correction:    0.9800
Go for it!
```

The polysilicon has been consumed and Ni_2Si has formed.

2) Sample D3 Poly_P+




```
XRump
File/Plot  Window  Layout  Edit  Variables  Help
  #          Thickness             Sublayers      Composition  . . .
   1         2800.00      A          auto          Ni    1.000
*  2         2500.00      A          auto          Si    1.000
   3          415.00  SiO2           auto          Si    1.000       O    2.000
   4        40000.00  /CM2           auto          Si    1.000
==========================================================================
SIM Command: active
  RBS  File:    c:\rumpdata\oct1005\0029_03n.rbs
  Identifier:   RIT 3P
  LTCT Text:    Not implemented
  Date:         10/10, 10:15:43
  Beam:         2.250 MeV   4He++    20.00 uCoul  @ 11.09 nA
  Geometry:         IBM  Theta:    8.00  Phi:   15.00  Psi:  630.00
  MCA:          Econv:   2.509   29.320  First chan:  0.0  NPT: 1024
  Detector:     FWHM: 18.0 keV  Tau: 10.0   Omega: 4.000
  Correction:   1.0000
Next?
```

This sample remained similar to the as-prepared condition.

3) Sample D1 Poly_P+

Energy (MeV)

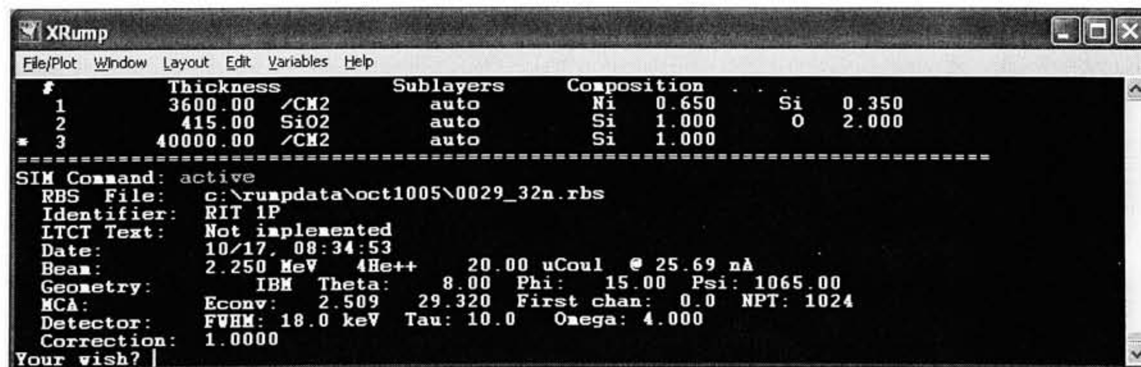
0.5 1.0 1.5 2.0

Normalized Yield

0 10 20 30 40

100 200 300 400 500 600 700 800

Channel



The polysilicon has been consumed and Ni_2Si has formed.

4) Sample D6 Si_P+

Energy (MeV)

0.5 1.0 1.5 2.0

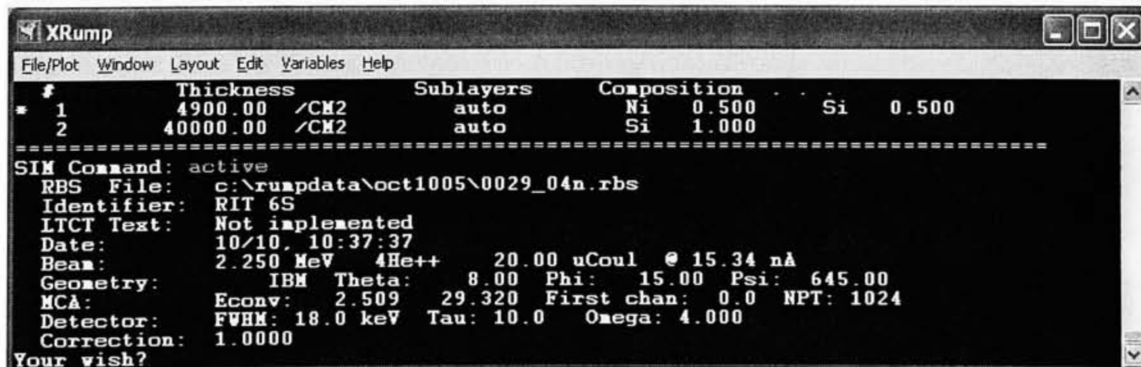
Normalized Yield

35 30 25 20 15 10 5 0

Si Ni

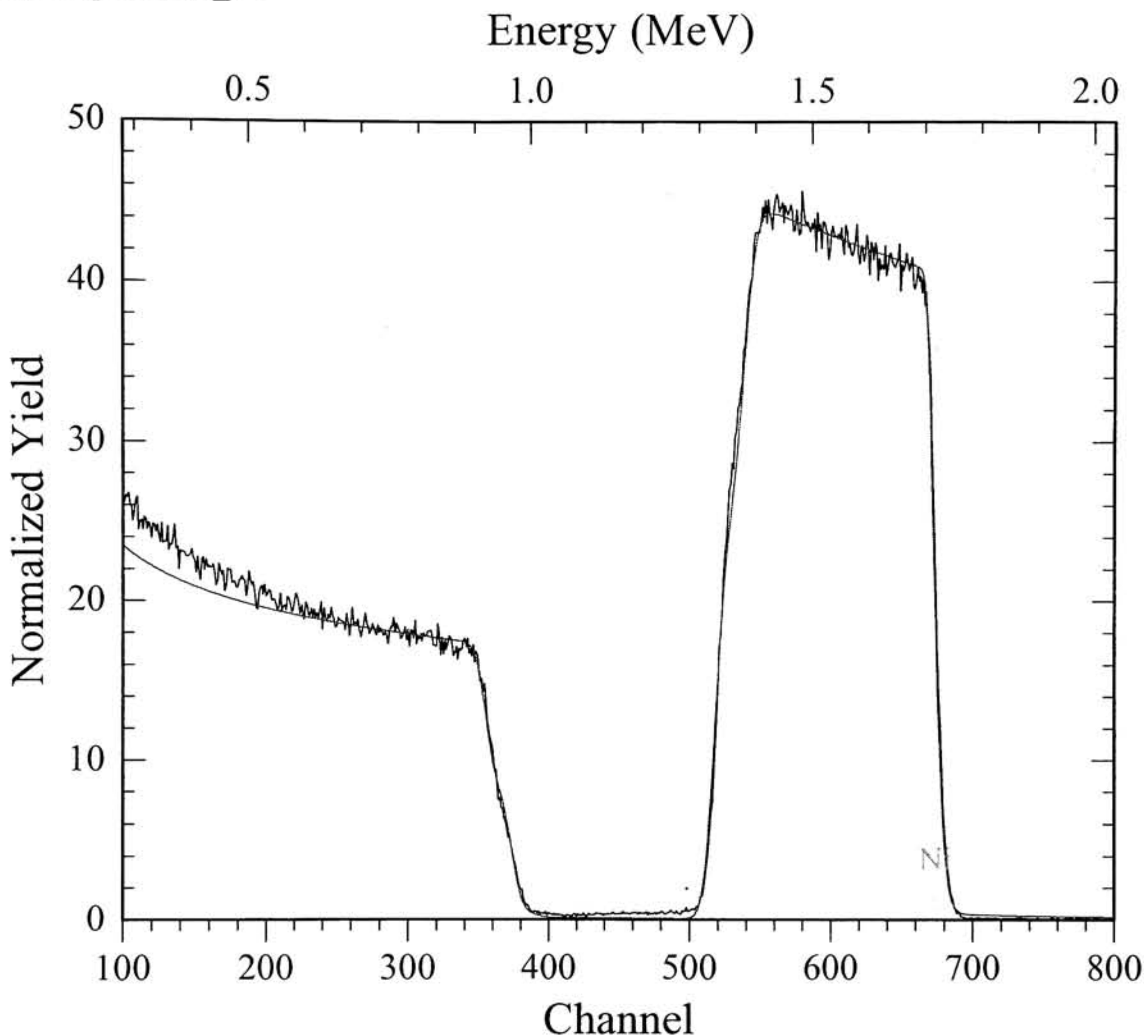
100 200 300 400 500 600 700 800

Channel



The top layer is about 50% Si and 50% Ni. There is a rough interface between the top layer and the second layer, or a rough surface.

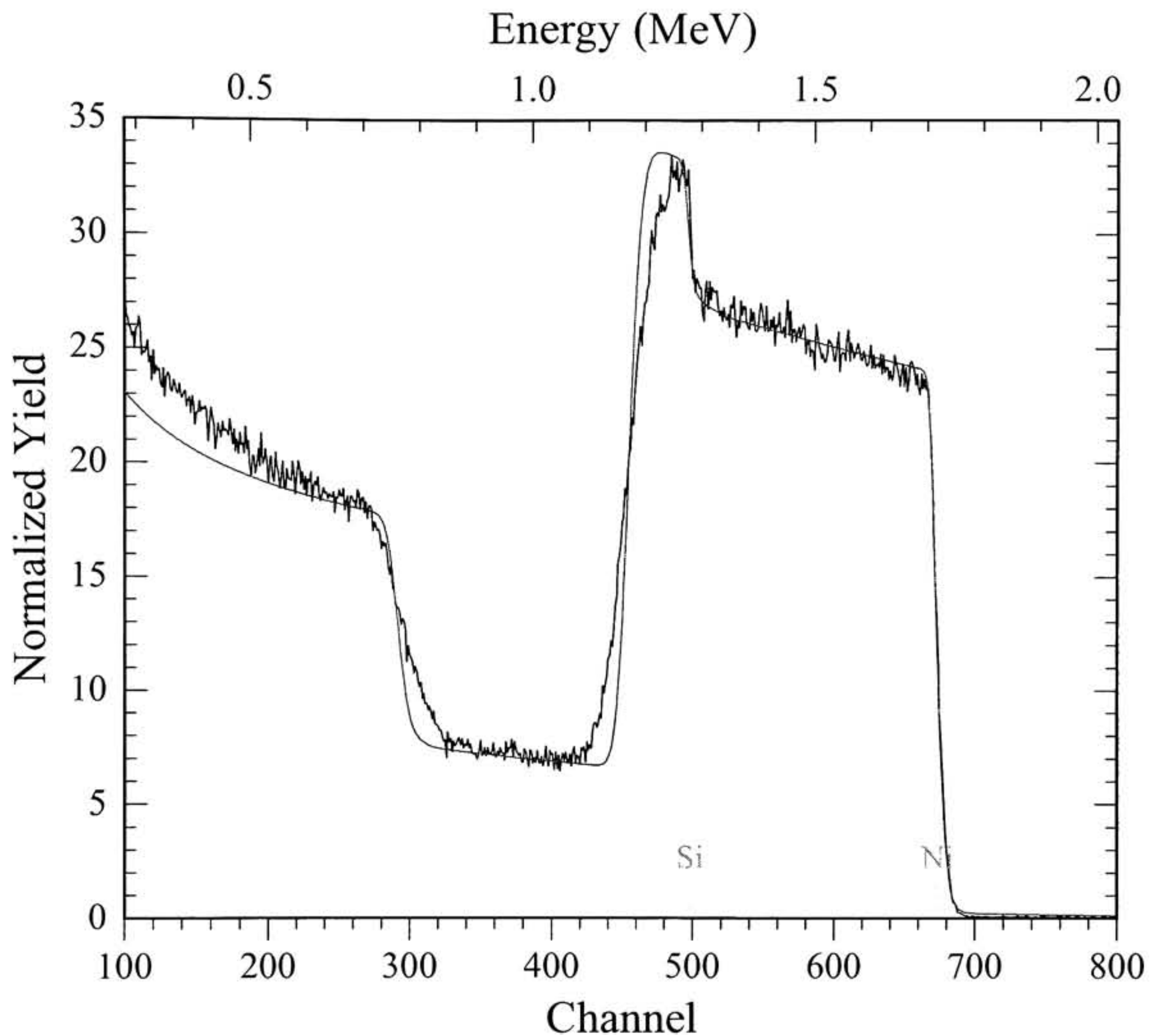
5) Sample D3 Si_P+




```
XRump
File/Plot  Window  Layout  Edit  Variables  Help
Igen, uram! sim show
  #      Thickness          Sublayers      Composition . . .
  1      2800.00     A         auto          Ni    1.000
* 2       450.00   /CM2        auto          Ni    0.480      Si    0.520
  3     40000.00   /CM2        auto          Si    1.000
==========================================================================
SIM Command: active
  RBS File:      c:\rumpdata\oct1005\0029_30n.rbs
  Identifier:    RIT 3S
  LTCT Text:     Not implemented
  Date:          10/17, 07:40:45
  Beam:          2.250 MeV   4He++    20.00 uCoul  @ 25.44 nA
  Geometry:          IBM  Theta:     8.00  Phi:    15.00  Psi: 1035.00
  MCA:           Econv:    2.509    29.320  First chan:   0.0  NPT: 1024
  Detector:      FWHM: 18.0 keV  Tau: 10.0    Omega: 4.000
  Correction:    1.0000
Next? |
```

There is a thin layer of about 48% Ni and 52% Si, between the Ni top layer and the Si layer (can not distinguish between N-type and P-type Si).

6) Sample D1 Si_P+




```
XRump
File/Plot  Window  Layout  Edit  Variables  Help
Yes Master? sim show
  #          Thickness          Sublayers     Composition . . .
* 1          4850.00  /CM2        auto          Ni   0.490     Si   0.510
  2         40000.00  /CM2        auto          Si   1.000
==========================================================================
SIM Command: active
  RBS  File:      c:\rumpdata\oct1005\0029_31n.rbs
  Identifier:     RIT 1S
  LTCT Text:      Not implemented
  Date:           10/17, 08:17:43
  Beam:           2.250 MeV    4He++     20.00 uCoul  @ 22.10 nA
  Geometry:           IBM  Theta:     8.00  Phi:    15.00  Psi: 1050.00
  MCA:            Econv:    2.509   29.320  First chan:   0.0  NPT: 1024
  Detector:       FWHM: 18.0 keV  Tau: 10.0    Omega: 4.000
  Correction:     1.0000
At your service!
```

The top layer is about 51% Si and 49% Ni. There is a rough interface between the top layer and the second layer, or a rough surface.

References

[1] D. Baselt, "The tip-sample interaction in atomic force microscopy and its implications for biological applications ", Ph.D. Thesis, California Institute of Technology, (1993).
[2] T.R. Albrecht, P. Grutter, D. Horne, D. Rugar, J. Appl. Phys. **69**, 668 (1991).
[3] AFM Tutorial, Pacific Nanotechnology, URL: http://www.pacificnanotech.com, Access Date: 05/04/05.
[4] Veeco AFM product description, URL: http://www.veeco.com. Access Date: 05/04/05.