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Fault-tolerant design of RF front-end circuits

Tejasvi Das

FAULT-TOLERANT DESIGN OF RF FRONT-END CIRCUITS

by

TEJASVI DAS

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By

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Submitted by Tejasvi Das in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Microsystems Engineering and accepted on behalf of the Rochester Institute of Technology by the dissertation committee.

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ABSTRACT

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Degree _Doctor of Philosophy_ **Program** _Microsystems Engineering_

Name of Candidate _Tejasvi Das_

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The continuing trends of scaling in the CMOS industry have, inevitably, been accompanied by an ever-increasing array of process faults and fabrication complexities. The relentless march towards miniaturization and massive integration, in addition to increasing operating frequencies has resulted in increasing concerns about the reliability of integrated RF front-ends. Coupled with rising cost per chip, the fault-tolerant paradigm has become pertinent in the RFIC domain. Two main reasons have contributed to the fact that fault-tolerant solutions for circuits that operate in the GHz domain have not been realized so far. First, GHz signals are extremely sensitive to higher-order effects such as stray pick-ups, interference, package & on-chip parasitics, etc. Secondly, the use of passives, especially inductors, in the feedback path poses huge area overheads, in addition to a slew of instability problems due to wide variations and soft faults. Hence traditional fault-tolerance methods used in digital and low frequency analog circuits cannot be applied in the RF domain.

This work presents a unique methodology to achieve fault-tolerance in RF circuits through dynamic sensing and on-chip self-correction, along with the development of robust algorithms. This technique is minimally intrusive and is transparent during 'normal' use of the circuit. It is characterized by low area and power overheads, does not need any off-chip computing or DSP cores, and is characterized by self-correction times in the range of a few hundreds of microseconds. It compares very well with existing commercial RF test solutions that use DSP cores and require hundreds of milliseconds. The methodology is demonstrated on a LNA, since it is critical for the performance of the entire front-end. It is validated with simulation and fabrication results of the system designed in IBM 0.25 μm CMOS 6RF process.

Abstract Approval:

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This work and my time here at RIT are humbly dedicated to my teacher, my *Guru*, Dr. Mukund; from him I have had the privilege of learning much more than circuit design.

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Chapter 1. INTRODUCTION

CMOS integrated circuits have become ubiquitous in today's electronics industry, offering the advantages of low cost, small size, high yield and reliability. The rapid shrinking of channel lengths has enabled MOS transistors to work at higher frequencies, breaking the GHz barrier. Along with the increasing demand for wireless and other forms of high-speed communication in the past few years, these factors have fuelled the development of a wide range of RF integrated circuit (RFIC) products [1].

The unprecedented drive towards miniaturization within the CMOS semiconductor industry has manifested itself in two major directions – aggressive scaling of transistor feature sizes with gate oxide thicknesses a few atoms wide, and high levels of system integration, with RF, mixed-signal and digital sub-systems residing on the same die (SoC, Figure 1.1) or in the same package (SiP, Figure 1.2).

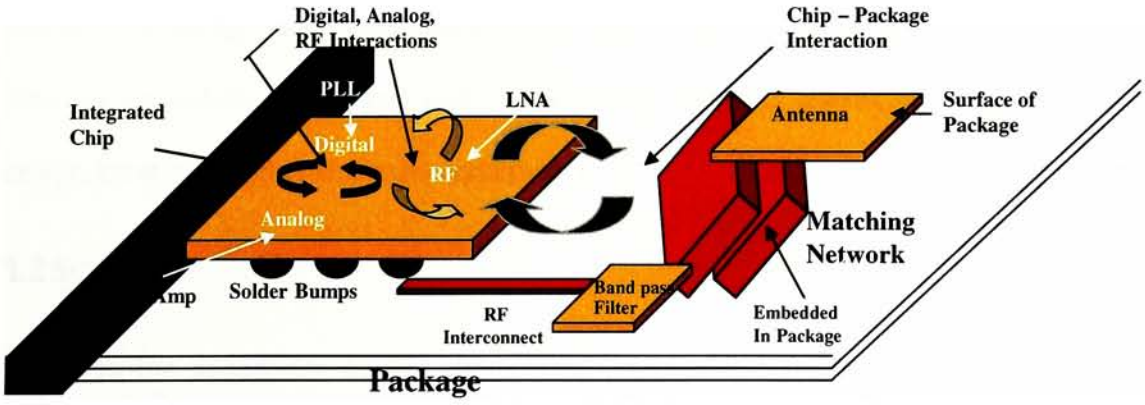


Figure 1.1 System-on-Chip (SoC) implementations [34]

1.1 INTEGRATION

The *International Technology Roadmap Update (ITRS)* predicts that the next 10-15 years will see an increasing number of system on chip and system in the package implementations with digital, base-analog, RF, mixed-signal, MEMS, electro-optical, chemical and electro-biological types of components merged within the package (SiP) or within a single chip (SoC). In either approach, increasingly complex and diverse interaction of signals occurs across the analog, digital and RF domains, and between the chip & the package[1]. With increasing clock speeds in the digital domain, these circuits generate noise that can severely limit the performance and precision of the RF front end. The trend in on-chip signaling techniques and interconnects leads to wireless intra-chip signal distributions in future silicon systems [2] [3]. Such signaling systems will also need to have highly reliable RF sub-systems. With higher frequencies of operation, the RF front-end exhibits heightened sensitivity to package parasitics (usually in the same order of magnitude as the circuit elements, Figure 1.3), mutual-coupling, electro-magnetic coupling, stray inductances, etc. These issues continue to increase the gap between simulation models and performance of the RFIC in silicon, resulting in several design iterations, higher test costs and lower yield.

1.2 SCALING

In the nanometer regime, fabrication complexity exponentially increases with every transition to a new technology node, inevitably accompanied by a larger number of process faults and higher process variations. The problem is exacerbated by the fact that

[1] The package exerts significant influence on the system performance, and consequently, its accurate characterization is a necessity for the success of such RFIC implementations.

in RF circuits, process variations and hard process faults are only part of the list of probable causes for failure or performance degradation. Another severe problem in RF circuits is the variability in the package parasitics. The package presents several parasitics to the signal in its path from the outside world to the die, such as inductances in bond wires, solder bumps, pad capacitances, mutual inductances between pins, etc. At high frequencies, these parasitics can significantly affect the performance of the RF circuit. The wide tolerances in these parasitics, as well as the lack of good models make it difficult for the designer to take them completely into account. Also, most RF circuits use passives like capacitors, inductors and resistors. With the drive towards greater levels of integration, many of these passives are beginning to be implemented on-chip. However the quality of these passives is very poor with reported Q values of 4-10. The quality factor is also not very predictable and is significantly influenced by slight variations in metal layer thickness, thickness of dielectric between the metal layers, etc. Thus these passives will also introduce soft faults in the RF circuit by degrading its performance beyond the required specification window.

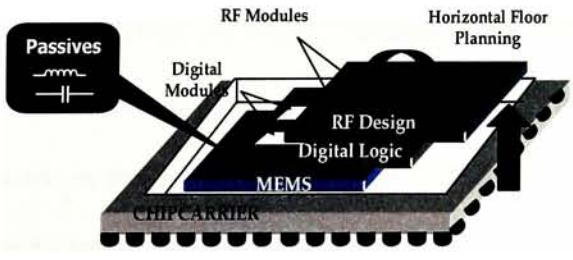


Figure 1.2 System-in-a-Package

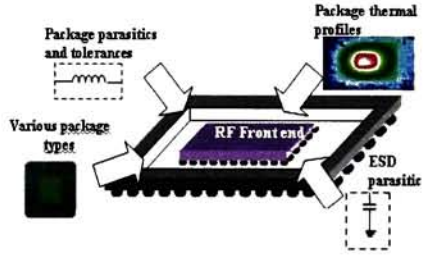


Figure 1.3 Packaging effects on the RF Front-end

Testing these RF circuits is a complicated process, since any contact or probing will modify the performance of the circuit. Automated Test Equipments (ATE) used to

test these GHz circuits are very expensive, and often test costs of a RFIC can absorb up to 40% of the entire design cycle cost. These factors, along with the increasing frequency of operation of RF circuits, render their reliability an issue of growing concern. The yield of RFICs is typically about 10%-12% lesser than that of digital ASICs.

1.3 MOTIVATION

These widening arrays of soft faults, large tolerances and issues such as coupling and interference cannot be accounted for in models; they require some form of post-fabrication processing. While testing plays an important role in quantifying yield and performance, it stops short of enhancing or optimizing them. An RF front-end that can dynamically re-calibrate its performance without external intervention can successfully overcome these challenges. Fault-tolerant design techniques, widely used in digital circuits, utilize redundancy and reconfigurability [4]. These techniques cannot be applied to the RF domain due to massive real-estate and power overheads. Feedback topologies, popular in the design of low-frequency analog circuits, cannot be implemented in RFICs due to stability issues and performance constraints. Due to these reasons, the *fault tolerant design* paradigm, although essential and relevant for RFIC design in the deep-submicron era, has not been successfully implemented yet. Further, there is no existing work in the RFIC domain that studies the impact of process tolerances and faults on performance specifications of the circuit.

This work offers an on-chip, low-overhead solution to the reliability issues faced by the wireless and RF semiconductor industry – it successfully overcomes the obstacles discussed above. The sensitivity analysis constructed in this work is low (processing)

intensive, requires no simulation support, and is a stand-alone process that lends itself well to multiple iterations. It provides a quantitative understanding of the performance degradations suffered due to process variations and soft-faults, and presents a theoretical foundation for the self-calibration of these performance specifications. The fault-tolerance methodology involves minimally intrusive sensing of the circuit specifications, and self-calibration mechanisms are based on the sensed information and the sensitivity analysis. It requires no off-chip computation or DSP processors and is extremely fast compared to existing test solutions. The algorithms, sensitivity analysis, and methodology are demonstrated on the most important circuit of the RF front-end, the Low Noise Amplifier (LNA).

Typically, R.F. front-end circuitry is interfaced to the outside world (antenna) through a Low Noise Amplifier (LNA) [12]. Consequently, it is the LNA that forms the physical connection between the package and the I.C., and package parasitics have a direct impact on its performance. Further, the LNA is the most critical block of any front end since its noise and gain affects the performance of the entire system. The Single-ended Cascode LNA is perhaps one the most widely used LNA topologies [19]. Although the balanced (differential) topology offers more advantages, the single-ended LNA enjoys popularity for its ease of implementation, and the fact that it possesses lesser real-estate and power consumption requirements[2].

[2] Although the specific implementation details may differ, the methodology, in general, can be implemented for other topologies, and other classes of circuits as well.

Chapter 2. BACKGROUND

No published body of work exists on reliability enhancement in the RF domain. The present work, to the author's knowledge, is the first attempt of its kind. This chapter briefly outlines some prior work in the area of self-test and low-frequency circuits.

2.1 SELF-TEST

Several attempts have been made in recent literature to address the problem of RF front-end reliability with the view of quantifying the effect of the various above-mentioned factors on circuit performance through self-test, thereby attempting to improve the robustness of the RF part shipped to the end customer. Many approaches such as the loop-back technique proposed in [5] and the end-to-end approach proposed in [6] involve significant processing and real estate overheads since they require the presence of additional DSP processing to achieve self test. Approaches such as the signature test method proposed in [7] are very computationally intensive, requiring a large amount of off-line computation to estimate circuit performance. Current commercial approaches require the use of costly ATE (Automated Test Equipment), which results in high test cost in addition to very large test times to test RF parts. Power-supply current based testing [8] [9] [10] has been one of the more promising techniques, where the supply current is analyzed, and signature patterns quantify the performance degradation.

2.1.1 Statistical Approaches

The statistical approaches described in [7] [23] [24] develop an optimal test stimulus or a set of stimuli that invokes outputs (from the circuit-under-test) which are then analyzed for faults and variations in the circuit. Multiple simulation runs of Monte-Carlo and process corners are executed for every given circuit, and these variations are mapped to variations in performance specifications of the circuit. The possible range and pattern of performance deviations are then studied, based on Monte-Carlo simulations. An optimization problem is then defined and a set of optimal test stimuli is generated using Genetic algorithms and additional simulation data. The circuit is simulated using various different stimuli until the algorithm picks an optimal set of stimuli. The circuit is further simulated with this optimal set to ascertain the range and coverage of faults it offers, using Monte-carlo analysis.

The ascertained optimal stimuli is specific to a given topology and design. Dedicated test hardware (on-chip or off-chip) is then designed to generate the stimuli, which are multi-tonal in nature. The output of the circuit is then processed, filtered, and subject to spectral analysis using either on-chip or off-chip DSP sub-systems. The sub-system analyzes the output signatures obtained (using FFT and DFT operations) and compares it with the output signature of an ideal, fault-free circuit to arrive at the test report.

This approach requires prior simulation (to collect statistical data) and optimization for every design. The list of overheads involved include the use of DSP cores, dedicated test hardware (offset VCO, mixer, attenuator, and-pass filter, A/D converter and a spectral analyzer component) and extensive computations (order of

hundreds of milliseconds). The power overheads are not mentioned in the work. This approach also does not fully eliminate the need for expensive Automated Test Equipment (ATE); they are needed to perform a one-time calibration on the entire system. A number of obstacles need to be overcome (primary, among them, is the need for accurate, calibrated circuit blocks) if the entire test hardware can be implemented on-chip. The success rate of the approach ranged from 88% to 95%.

2.1.2 Loopback-mode testing

In [5] [25] [26], a system-level test scheme is described where the digitally modulated RF carrier from the transmitter is looped back to the receiver. The received signal is processed by the RF front-end and the output is analyzed (using DSP cores and attenuators) to evaluate the system-level specifications of the entire transceiver. Different input stimuli are applied and their outputs are analyzed to arrive at the final conclusions. [26] uses the base-band processor of the transceiver system to perform the output signature analysis.

Several drawbacks exist in these approaches. The system-level decision does not provide localization of either the faults or the faulty circuit. Further, it cannot distinguish between faults on the receiver and the transmitter. Faults closer to the receiver side are not detectable due to the high power content of the transmitted signal. [5] suggests the need for testing the receiver separately to achieve desired accuracies (too achieve fault-coverage accuracies of greater than 85%). This will lead to additional overheads of test signal generation, algorithms, etc as mentioned in the previous section. Further, these approaches consider a highly simplified system-level behavioral model in MATLAB. [25] mentions that the Loopback mode of testing has inherently less test coverage and

higher overheads (more DSP processing) compared to testing the receiver on a circuit-by-circuit or a sub-system basis.

2.1.3 Power supply Current based testing

Power supply based testing has been a popular approach in digital and analog circuits [8] [9], and a on-chip self-test scheme for RF front-ends has been recently published in [10] [29] [30]. The methodology used in this approach is to sense the High Frequency (HF) transient current of the given circuit by placing a relatively small resistor (under 10 ohms) in its current path. The voltage developed across this resistor is then interfaced to a high-frequency current monitor circuit, which outputs a current proportional to the HF current drawn by the circuit. This current is then down-converted to baseband and the signature thus obtained is mapped to the performance specifications of the circuit. The test inputs required for this test are simple enough to be generated on-chip: no spectral-generators and analyzers are needed. This work is characterized by the low overheads (no DSP cores), low intrusion (the resistor adds to the noise of the system by approximately 10% and degrades the dynamic range by approximately 5%) and fast test times (30 μs). The approach has been demonstrated on Low Noise Amplifiers, Mixers and Voltage Controlled Oscillators (VCO). The self-test of VCO provides confirmation of only the operating frequency and none of the other specifications. The self-test for mixer also does not address the important specifications of linearity and port leakage.

The work in [29] was part of the same SRC project as the current work, and its sensing mechanisms[3] form the platform for the self-calibration system developed in the current work, which senses and *corrects* circuit performance.

2.1.4 Other methods

In [27], self-test of amplifiers is accomplished by introducing positive feedback into the circuit and measuring the frequency of oscillation as the fault-detection metric. The approach poses considerable intrusion, since the circuit topology has to be changed, in addition to the instability issues posed by the positive feedback. Further, this method cannot be used for front-end circuits such as mixers and VCOs. The authors of [28] present a high-overhead method of testing Low Noise Amplifiers by measuring its transient output voltage. The overhead circuitry includes a test amplifier, five inductors, six capacitors and resistors. In addition, the method uses switches in the RF signal path at the output node of the circuit-under-test, degrading signal purity.

2.2 FAULT-TOLERANCE IN DIGITAL AND LOW-FREQUENCY ANALOG DOMAINS

Digital circuits accomplish fault tolerance by either redundancy along the signal path or reconfigurability [4]. These methods involve huge real-estate and power overheads to replicate in the RF domain[4]. Further, due to the binary nature of signals, soft

[3] The current work senses the transient HF current (as in [29]) for quantifying impedance-match specifications. It also senses the transient voltage at the output node (a technique not used in [29]) of the circuit for quantifying other circuit specifications. Chapter 5 contains more detailed description of these mechanisms.

[4] A typical coil occupies about 300 X 300 μm^2, and a LNA draws upwards of 5 mA. Having a redundant coil or a supply path requires overheads that cannot be afforded.

fault degradation can be neglected in majority of the cases. In analog circuits, traditional correction for soft-faults uses voltage or current feedback, where a part of the output voltage or current is sampled and fed back to the input to achieve increased robustness. As will be shown in the succeeding chapters, this approach has several pitfalls when applied to the RF domain, and is not practicable. Chapter 4 discusses the obstacles of using feedback in RF circuits in greater detail.

Chapter 3. SENSITIVITY ANALYSIS

The system-level objective of this work is to sense critical performance attributes of the given circuit and to then self-calibrate the circuit by modifying its behavior (component values). It becomes necessary, then, to study the mapping of all circuit component variations onto performance specifications of the circuit. This analysis provides a quantitative insight into the performance deviations caused due to process variations and soft faults. The Sensitivity analysis further addresses the following issues:

- Sensitivity of each component with respect to the circuit specification parameters
- Quantified impact and dependence of each component with respect to all circuit specifications
- Quantified deviation from ideal performance specifications for variations in each circuit component
- Most suitable component to be dynamically modified for each specification
- Impact of this modification for the rest of the circuit specifications and compensation in the case of negative effects, if any
- If the circuit component is modified in discrete steps (as it is in this work), then the spacing between these steps has to be determined
- Number of such steps to be programmed into the design

The analysis is expected to provide inputs to early (pre-simulation) stages of the design cycle, and cannot rely upon several time-intensive simulations – especially since multiple iterations are to be expected, and it is impractical to necessitate simulation cycles for each sensitivity analysis cycle. The ideal solution for such a scenario is to develop a theoretical, 'no-simulation required', generic process (as has been developed for this work) that can be re-used for different designs and iterations, across process technologies and different applications.

This analysis, in addition to answering the aforementioned questions, also finds utility as an early-design aid for designs of normal[5] circuit topologies. It provides the designer with useful insight by quantifying parameter-performance dependencies, trends and trade-offs involved in meeting the application specifications.

The fault-tolerant methodology developed in this work is demonstrated on the single-ended cascode Low Noise Amplifier (LNA) topology. The LNA is the most critical circuit in the RF front-end – in addition to being the interface between the package and the chip, its performance greatly impacts the functioning of the front-end chain. The remainder of this chapter presents a theoretical sensitivity analysis for cascode LNA topology; first-order equations are used, with second-order effects included only where the impact on accuracy is significant. The end-result is a series of stand-alone sensitivity tables that are fast to compute and require no simulation support. The math computations use Maple ® software, and the tables lend themselves very easily for multiple iterations – the user has to simply re-input the new design variables and values are re-computed.

[5] Not using the fault-tolerant approach

3.1 COMPONENTS AND SPECIFICATIONS

For the LNA, the following standard specifications are applicable[6]:

- **Input match** (S_{11}, typically specified in dB): The input-match reflection coefficient is defined as $10*\log\left(\frac{Z_{IN}-Z_O}{Z_{IN}+Z_O}\right)$, where Z_{IN} is the input impedance of the circuit in ohms, and Z_O is the characteristic impedance of the source that feeds the circuit.

- **Output match** (S_{22}, typically specified in dB): The output-match reflection coefficient is defined as $10*\log\left(\frac{Z_{OUT}-Z_O}{Z_{OUT}+Z_O}\right)$, where Z_{OUT} is the output impedance of the circuit in ohms, and Z_O is the characteristic impedance of the load that follows the circuit.

- **Gain** (S_{21}, typically specified in dB): S_{21} is defined as $10*\log\left(\frac{P_{OUT}}{P_{IN}}\right)$, where P_{OUT} is the output power of the circuit for a given input power, P_{IN}. S_{21} definitions assume that the output of the circuit is terminated with an impedance that offers maximum power transfer.

- **Reverse isolation** (S_{12}, typically specified in dB): The reverse reflection coefficient is defined as $10*\log\left(\frac{P_{IN}}{P_{OUT}}\right)$, where P_{OUT} is a signal applied at the output node of the circuit, and P_{IN} is the measured input power at the input node of the circuit, when the input-node is terminated for maximum power transfer.

---

[6] These specifications form the standard set used for most IC design purposes, and their values are application specific. This set is also found in most commercial discrete LNAs such as the MAXIM series.

- **Noise figure** (NF, typically specified in dB): Noise Figure is defined as $10*\log\left(\frac{SNR_{IN}}{SNR_{OUT}}\right)$, where SNR_{IN} and SNR_{OUT} are the signal-to-noise ratios of the input and output nodes respectively.

- **Linearity** (IIP3 or 1-dB compression point, typically specified in dBm): IIP3 (input-referred intercept point) is defined as the input power at which the output power curves of both the fundamental and the third harmonic components intercept each other. This is a theoretically extrapolated value.

For the numerical analysis, design values for a 1.9 GHz LNA (used in this work) designed in the IBM6RF process have been used. From the LNA schematic of Figure 3.1, various components that impact these specifications, their values used in this analysis and the tolerances[7] considered in this work are listed:

- L_G(gate coil): 9.0 nH, tolerance of 30%

- L_S (source coil): 0.6 nH, tolerance of 30%

- C_{GS} (gate-source capacitance of M_1): 0.73 pF, tolerance of 10%

- *W/L* (W/L ratios of the transistors): 324/0.24 for M_1 and M_2, tolerance in (W/L) ratio of 4% is modeled by varying W from 318 μm to 330 μm. This variation accounts for tolerances of both length and width of the transistor, and variations in the current mirroring ratio between transistors M_3 and M_1.

- g_m (transconductance of input transistor): 60.9 mS

[7] The tolerance values are traced from the Process Design Kit (PDK) of the IBM 6RF CMOS process. In cases where the data was not available in the PDK, best estimated values have been used.

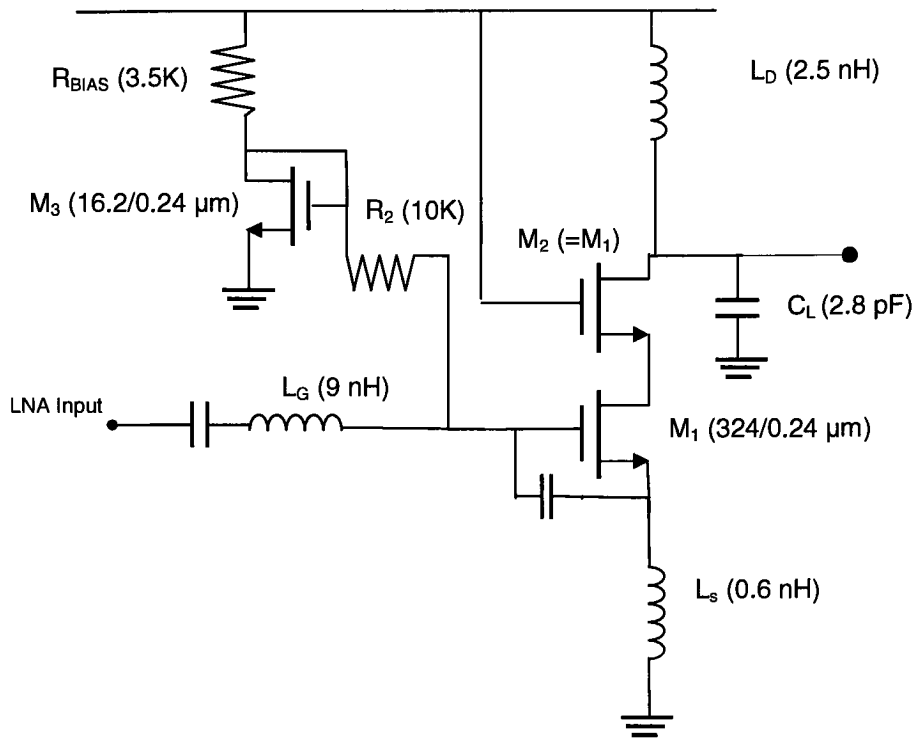


Figure 3.1 Single-ended Cascode LNA schematic. The indicated component values are used in the analysis of this work.

- I_{BIAS} (bias current): 9.6 mA, tolerance of 30%
- L_D: 2.5 nH, tolerance of 30%
- R_{BIAS} (bias resistor): 3.5 KΩ, tolerance of 25%
- V_{TH} (threshold voltage): 0.6 V, tolerance of 3.3 %
- V_{DD} (supply voltage): 2.5 V, tolerance of 20%
- C_L (load capacitance): 2.8 pF, tolerance of 15%

Unless otherwise mentioned, the above-mentioned tolerance values are assumed throughout this work. It must be mentioned that variations parameters such as mobility

and noise correlation factor have not been analyzed, since this work considers components that can be modified by the circuit designer. These factors are dependent on environmental conditions such as temperature, and correcting for such variations is beyond the scope of this work.

3.2 INPUT MATCH

3.2.1 S_{11} frequency

The input match frequency of the LNA is given by [11]:

$$f_{in} = \frac{1}{2\pi\sqrt{(L_G + L_S)C_{gs}}} \tag{3.1}$$

$$\text{where } C_{gs} = \frac{2}{3}WLC_{ox} \tag{3.2}$$

The input match frequency is dependent on L_G, L_S, C_{gs}, and W/L of the input transistor. For the 1.9 GHz LNA used in this work, variation of f_{in} for a 30% variation in the gate coil is shown in Figure 3.2. The sensitivity of L_G to S_{11} frequency is given by:

$$\frac{\partial f_{in}}{\partial L_G} = -\frac{C_{gs}}{4\pi[(L_G + L_S)C_{gs}]^{3/2}} \tag{3.3}$$

and for the design values of the LNA, this equates to 9.902E16, or 0.099 GHz/nH. The total possible deviation in S_{11} frequency due to variations in L_G (ΔL_G is the tolerance of the gate coil and 30% of 9 nH translates to 2.7 nH) is given by[8]:

[8] With the assumption that the variation of S_{11} frequency with L_G is monotonic, and can be approximated to be linear (as can be verified by Figure 3.2). In more complex cases, it will be necessary to perform piecewise linearity approximations, or evaluate the integral of the curve.

$$\frac{\partial f_{in}}{\partial L_G} * \Delta L_G = 9.902E16 * 2.7nH = 0.27GHz \quad (3.4)$$

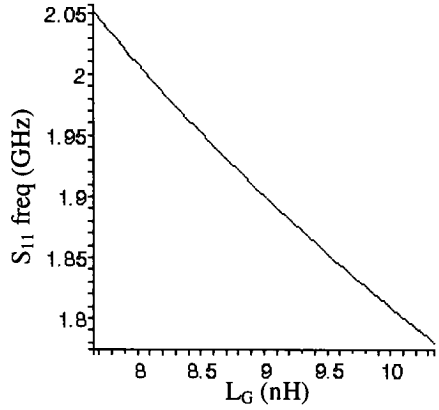


Figure 3.2 Variation in S_{11} frequency (in GHz) as the value of the gate-coil (L_G) is varied

Components	Affects S_{11} freq?	Sensitivity	Δ freq (GHz)
L_G	√	0.99/nH	**0.27**
L_S	√	0.1/nH	0.018
C_{GS}	√	1.3/pF	0.095
g_m	X		
V_{TH}	X		
W	√	0.005/μm	0.06
L_D	X		
C_L	X		
R_{BIAS}	X		
V_{DD}	X		
Q_{LG}	X		
Q_{LD}	X		

Table 3.1 Sensitivity-table for S_{11} frequency

Following a similar process for L_G, C_{GS} and W, the sensitivity-table of S_{11} frequency (Table 3.1) is constructed. The sensitivity equations are realized by computing the partial differential of the equation governing the performance metric with respect to each component (as in equation 3.3). These equations have not been explicitly listed in

this work due to their complexity. The user should be able to readily compute them using any standard Math software using the equations mentioned in this work.

The process is summarized in Figure 3.3, where S_{11} frequency is plotted against all three components: L_G, L_S and C_{GS}. The deviation for all cases is monotonic and almost linear. It is also clearly seen that the deviation is greatest for variations in L_G. Further, since L_G has little or no impact on other specifications (as is seen in the following sections), it is an ideal candidate to use for achieving input-match adaptability.

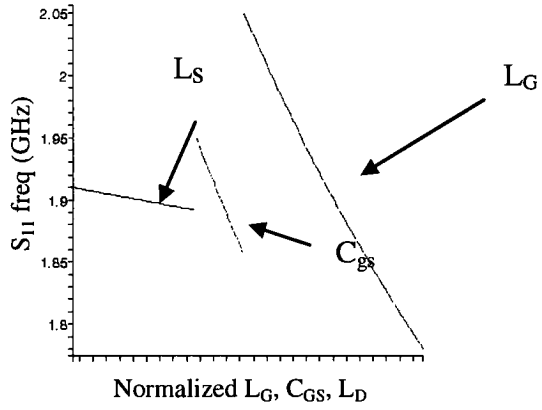


Fig. 3.3 S_{11} frequency (GHz) versus normalized values of L_G, L_S and C_{gs}

The actual variation considered for each component is based on the tolerances and variations specified by the technology process being used. For example, the variation/tolerance of a bond-wire is much higher (up to 40%) compared to an on-chip coil (up to 30%). Hence the variation considered for the gate coil will depend on the choice of coil used.

3.2.2 Input Impedance

The magnitude of input impedance Z_{IN}[9] is given by:

[9] The input match is designed such that the ideal value of Z_{IN} = 50 ohms

$$|Z_{IN}| = \sqrt{\left(\frac{g_m L_S}{C_{gs}}\right)^2 + \left(\omega(L_S + L_G) - \frac{1}{\omega C_{gs}}\right)^2} \tag{3.5}$$

$$\text{where } g_m = \sqrt{2K'\frac{W}{L} I_{BIAS}} \tag{3.6}$$

and K' is the product of C_{ox} and effective mobility, μ_{eff}

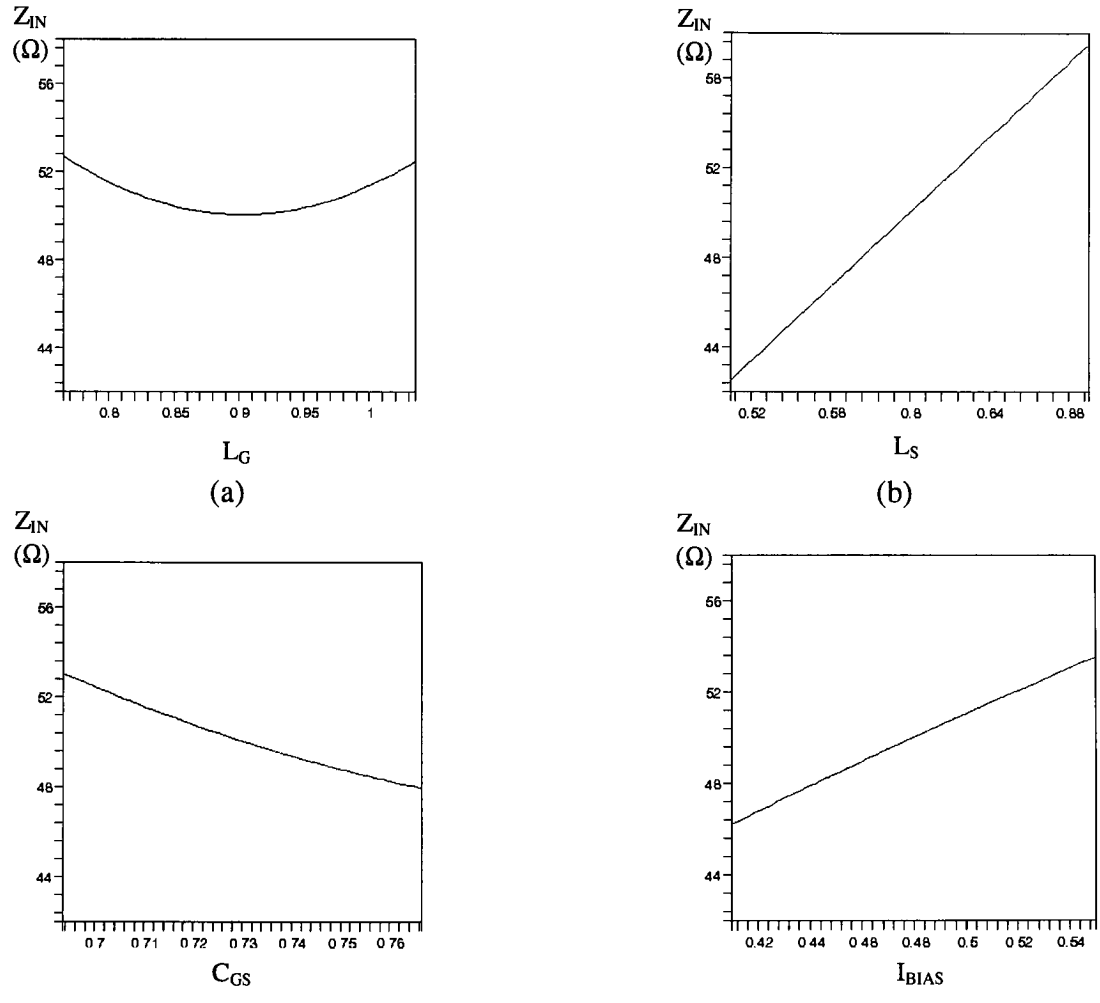


Figure 3.4 Input impedance variation versus (a) L_G (b) L_S (c) C_{GS} and (d) I_{BIAS}

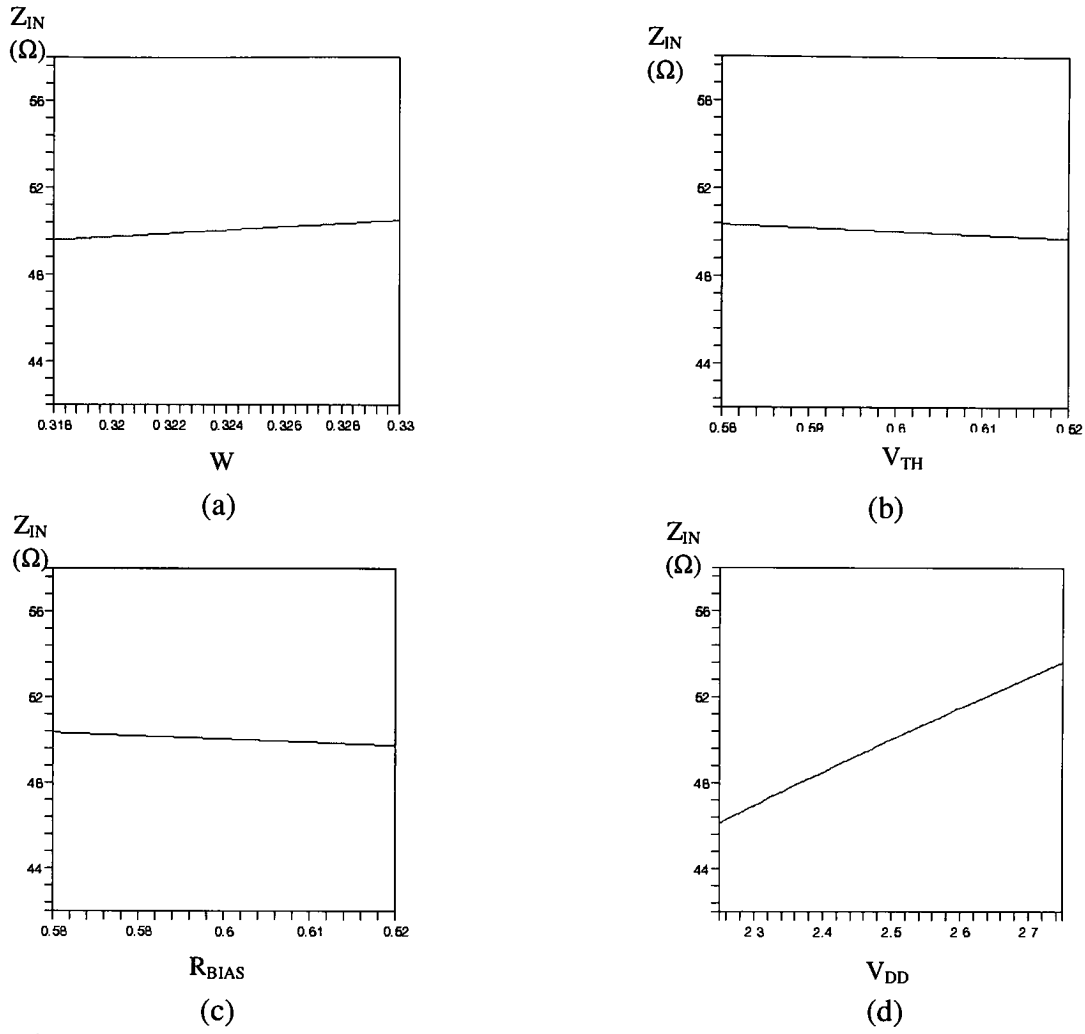


Fig. 3.5 Input impedance (in ohms) versus various components (a)W (b)V_{TH} (c)R_{BIAS} (d)V_{DD}

Figures 3.4 and 3.5 show a plot of the input impedance versus all the components that impact Z_{IN}. For the tolerances chosen, it is seen that L_S has maximum impact on the input impedance magnitude.

The sensitivity of L_S on input impedance is given by:

$$\frac{\partial|Z_{IN}|}{\partial L_S} = \frac{\frac{2g_m{}^2 L_S}{C_{gs}{}^2} + 2\left(\omega(L_S + L_G) - \frac{1}{\omega C_{gs}}\right)\omega}{2\sqrt{\left(\frac{g_m L_S}{C_{gs}}\right)^2 + \left(\omega(L_S + L_G) - \frac{1}{\omega C_{gs}}\right)^2}} \qquad (3.7)$$

and for the design values used, it is evaluated at 8.335E10 (ohms per henry). Following a similar procedure for all other dependent components, we arrive at Table 3.2.

Components	Affects Z_{11}?	Sensitivity	ΔZ_{11} (Ω)
L_G	√	0.358/nH	2.6
L_S	√	83/nH	**14.9**
C_{gs}	√	69.5/pF	5.1
W	√	0.077/μm	0.924
I_{BIAS}	√	2.6/mA	7.28
V_{TH}	√	14.9/V	0.6
R_{BIAS}	√	7.1/kΩ	**6.25**
L_D	X		
C_D	X		
V_{DD}	√	14.9/V	**7.45**
Q_{LG}	√	1/pΩ[10]	4
Q_{LD}	X		

Table 3.2 Sensitivity-table for input-impedance of LNA

3.3 GAIN

An alternate view of the LNA schematic (the cascode transistor has been omitted for simplicity purposes) is shown in Figure 3.6. Here R_L is the parallel equivalent resistance of the load network – the parasitic resistance (R_{par}) of the coil L_D is the main contributor to this resistance. At the resonant frequency, L_D and C_D resonate with each other, with the resistance R_L forming the effective load resistance.

The gain analysis in this section uses voltage gain compared to power gain; the power gain depends on the terminating impedance of the LNA, which is dependent on the circuit/termination that follows the LNA. Since this termination is both application and architecture specific, voltage gain has been considered.

[10] pΩ refers to 'parasitic ohm' – the parasitic resistance of the inductor. This notation is consistent for all cases where 'pΩ' is encountered in this work.

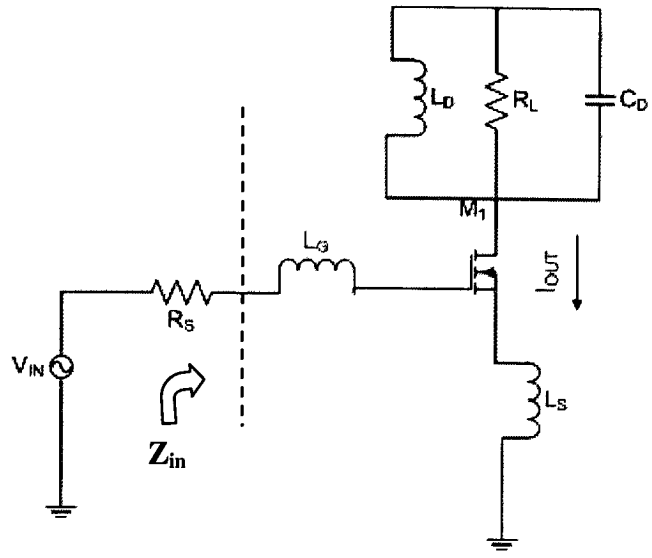


Figure 3.6 Alternate view of the LNA with cascode transistor eliminated

With the output load impedance denoted by Z_{out}, we arrive at the following equations:

The input impedance Z_{in} is given by $$Z_{in} = \frac{g_m L_s}{C_{GS}} + j\left(\omega(L_s + L_g) - \frac{1}{\omega C_{GS}}\right) \quad (3.8)$$

The output impedance Z_{out} is given by $$Z_{out} = \frac{j\omega L_D + R_{par}}{1 - \omega^2 L_D C_D + j\omega R_{par} C_D} \quad (3.9)$$

where R_{par} is the series parasitic resistance of L_D.

The gate-source voltage v_{gs} is given by[11] $$v_{gs} = \frac{v_{in}}{(R_s + Z_{in})}\left(\frac{1}{j\omega C_{gs}}\right) \quad (3.10)$$

The voltage gain G is given by $$G = \frac{g_m v_{gs} Z_{out}}{v_{in}} = \frac{g_m Z_{out}}{(R_s + Z_{in}) j\omega C_{gs}} \quad (3.11)$$

The sensitivity of G to R_{par} is given by $$\frac{\partial G}{\partial R_{par}} = \frac{g_m}{(R_s + Z_{in}) j\omega C_{gs}}\left(\frac{\partial Z_{out}}{\partial R_{par}}\right) \quad (3.12)$$

[11] R_S is this equation is the impedance of the source that drives the LNA, which is typically the impedance presented by the antenna or the filter preceding the LNA. The termination is set to be 50 Ω in almost all designs, which is also equal to the characteristic impedance of the system. Variations in R_S are thus not considered, since it is a fixed parameter as far as the LNA is concerned.

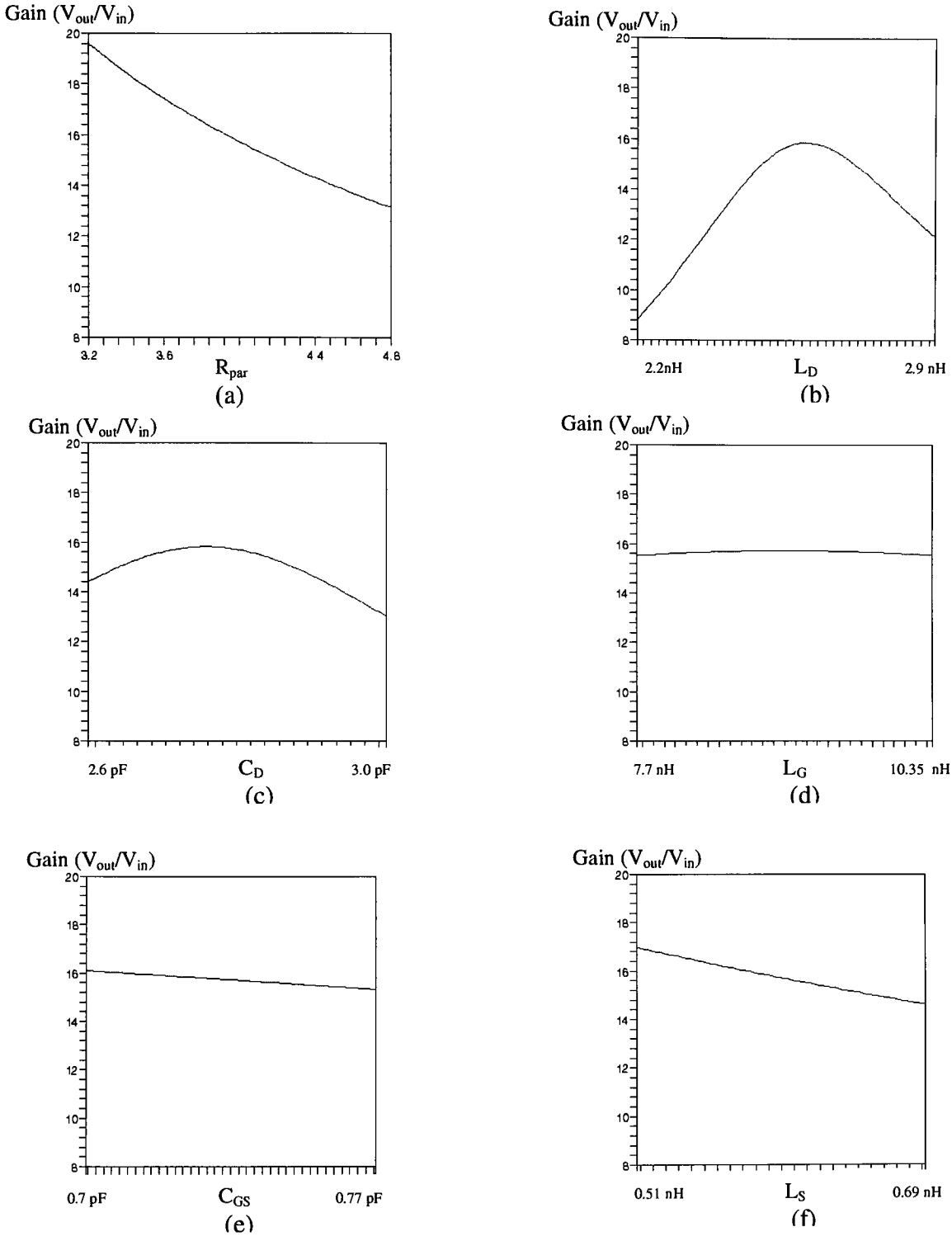


Figure 3.7 Deviation in gain versus various components (a)Q_{LD} (b)L_D (c)C_D (d)L_G (e)C_{GS} (f)L_S

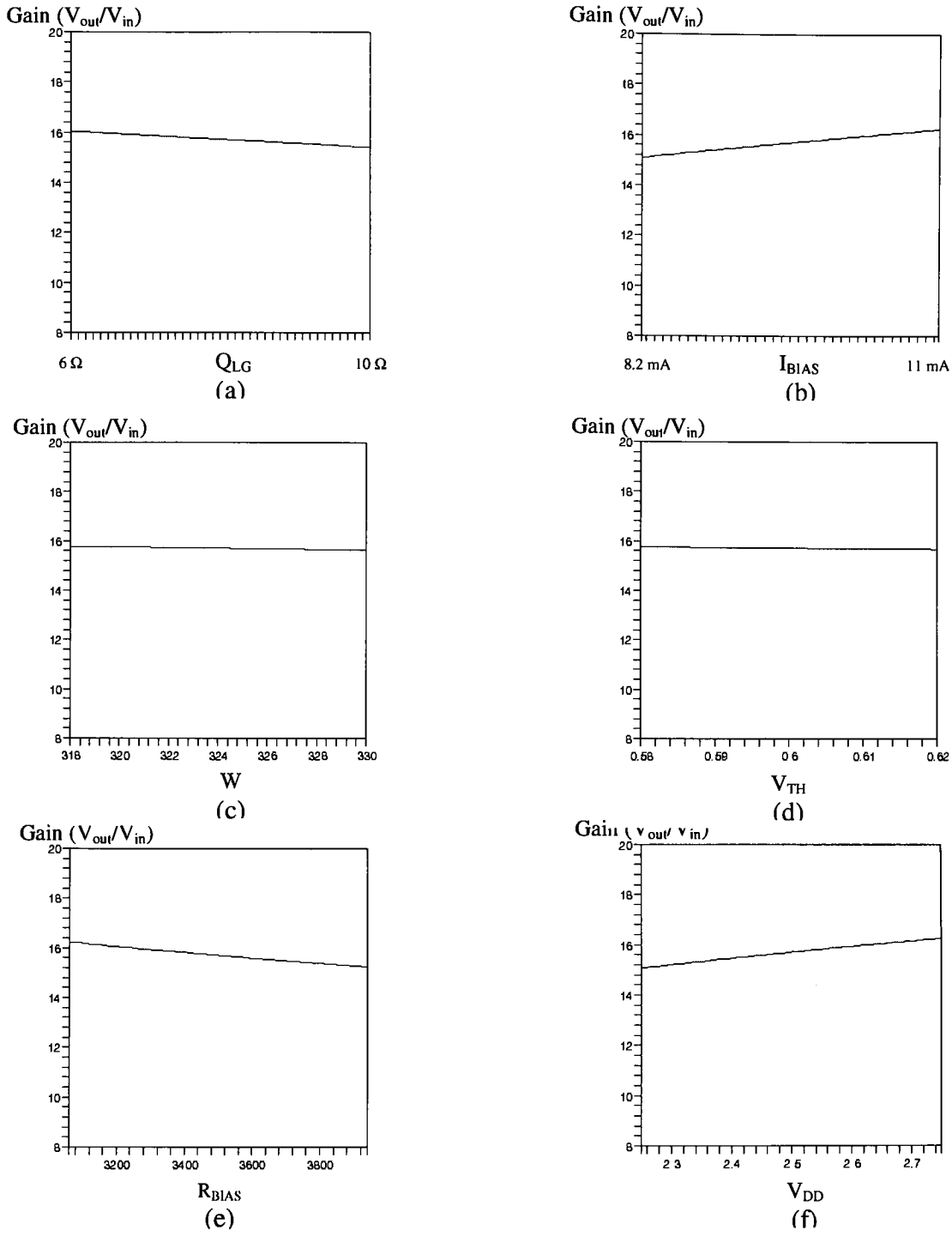


Figure 3.8 Deviation in gain versus various components (a)Q_{LG} (b)I_{bias} (c)W (d)V_{th} (e)R_{bias} (f)V_{DD}

The variations in gain for the LNA under consideration, when the components are subject to variations are shown in Figures 3.7 and 3.8. Following a process similar to that of Section 3.2, the sensitivity grid of Table 3.3 is generated.

Component	Affects G?	Sensitivity	ΔG
L_G	√	0.002/nH	0.26
L_S	√	13.11/nH	2.4
C_{gs}	√	10.74/pF	0.78
W	√	0.0122/μm	0.146
I_{BIAS}	√	0.41/mA	1.15
V_{TH}	√	2.34/V	0.094
R_{BIAS}	√	1.1/kΩ	0.97
L_D	√	6.9/nH	**7.1**
C_D	√	5.0/pF	**3.9**
V_{DD}	√	2.34/V	1.17
Q_{LD}	√	3.86/pΩ[12]	**6.2**
Q_{LG}	√	0.16/pΩ[7]	0.64

Table 3.3 Sensitivity-table for Gain

The three major contributors to gain variation are, predictably, the load network components of L_D, C_D and Q-factor of L_D. While the variation with respect to Q_{LD} is almost linear, C_D and L_D have a non-monotonic response; the sensitivity to gain at their ideal designed values is significantly lower compared to values that have deviated from the ideal designed value.

3.4 REVERSE ISOLATION

Use of cascoding in LNAs has been ubiquitous primarily for the input-output isolation it offers by decoupling the gate-drain capacitance. Due to this, cascode LNAs have more than adequate reverse-isolation in almost all applications. While they have

[12] parasitic ohm

zero reverse-coupling in theory, there exists some minor, but tolerable amount in practice. This section uses simulation results to show that the S_{12} of cascode LNAs remain well within acceptable limits even when process variations and faults are induced. Consequently, their sensitivity to performance specifications is either zero or a negligible finite amount.

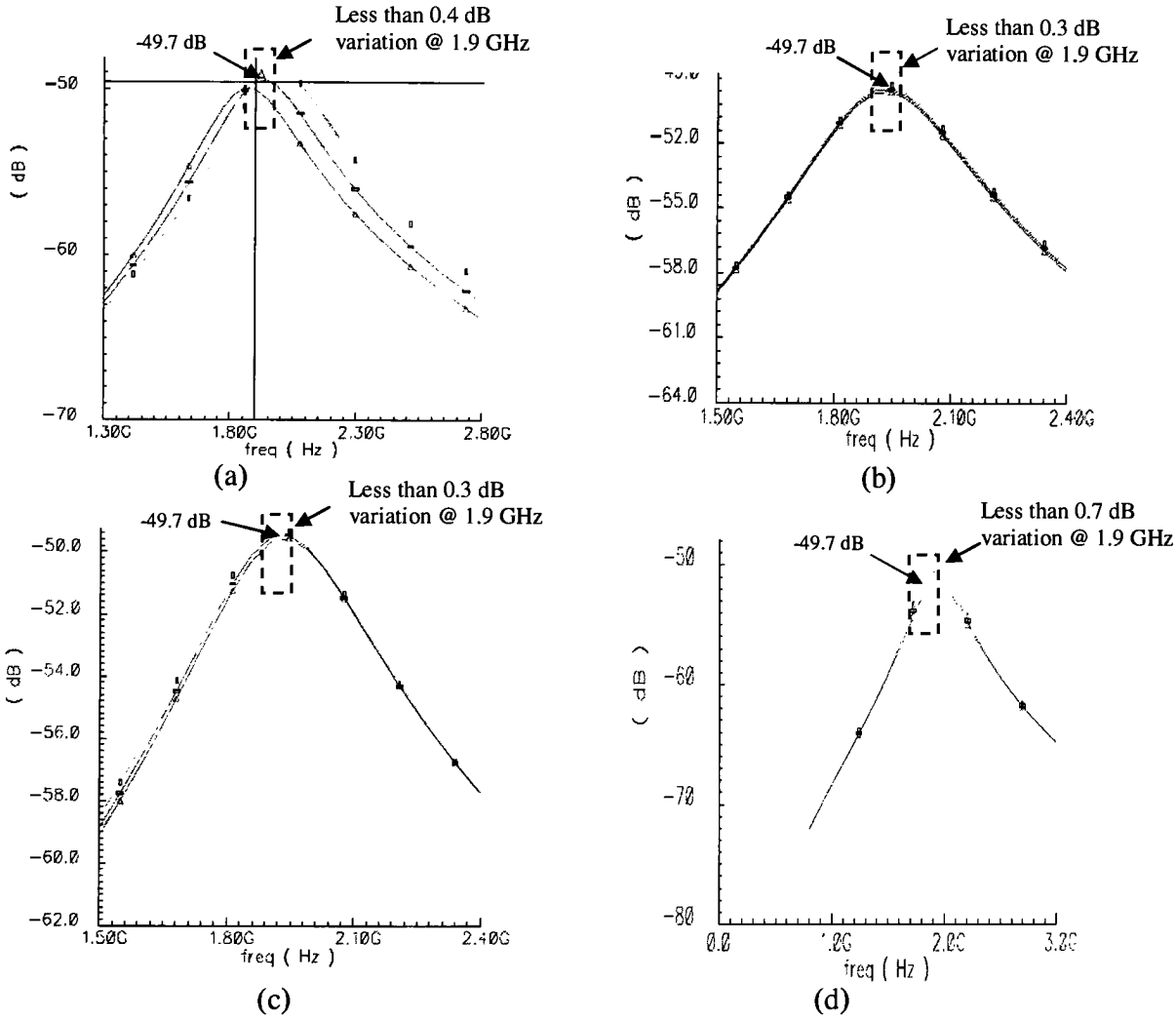


Figure 3.9 Deviation in S_{12} versus variations in (a) C_D (b) C_{GS} (c) V_{DD} (d) Q_{LD}. The deviation for all other components remain less than 0.4%.

Figure 3.9 shows the negligible impact on S_{12} when numerous component values are varied across their tolerance limits for a 1.9 GHz cascode LNA. It is seen that S_{12}

remains below -49 dB in all cases (the measured results for S_{12} from the fabricated chip also remained below -38 dB), and the variations are within 1.5%. The S_{12} deviation for other components (not shown in Figure 3.9) was absent or negligibly minor (less than 0.4%). The above results indicate that the sensitivity is zero or near zero, and also imply that it is realistically not necessary to design S_{12} sense-and-correct mechanisms.

3.5 NOISE FIGURE

The noise figure of a LNA is often a critical specification, and studying its sensitivity to various component deviations allows the designer to make intelligent trade-offs. The Noise Factor[13] (NF) is given by [11]:

$$NF = 1 + \frac{\omega_0 \gamma g_{d0} (1 - 2c\chi_d + (4Q^2 + 1)\chi_d{}^2)}{2.\omega_t g_{m.} Q} \tag{3.13}$$

$$\text{where } \omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \text{ (input match frequency)} \tag{3.14}$$

$$\omega_t = \frac{g_m}{C_{gs}} \tag{3.15}$$

$$g_m = \sqrt{2K' \frac{W}{L} I_{bias}} \tag{3.16}$$

$$Q = \frac{\sqrt{L_g + L_s}}{2R_s \sqrt{C_{gs}}} \tag{3.17}$$

$$\chi_d = \frac{g_m}{g_{d0}} \sqrt{\frac{\delta}{5\gamma}} \tag{3.18}$$

g_{d0} is the device transconductance when the drain-source voltage is zero, i.e, in the triode region of operation. It is modeled as

[13] 10*log(Noise Factor) = Noise Figure

$$g_{d0} = K\frac{W}{L}(V_{gs} - V_{th}) \qquad (3.19)$$

where K is a constant extracted from simulation. γ is the empirically derived excess noise factor, and its value ranges between 2-3 for short-channel processes, and δ is typically valued at 2 γ. c is the correlation factor between the transistor gate and drain noise. For the 0.25 μm process, γ is valued at 3. Figures 3.10 and 3.11 show the deviation in noise figure versus various components. Using the above equations, the sensitivity of each component is evaluated as before and tabulated in Table 3.4. The nominal noise figure value for this design was 1.94 dB.

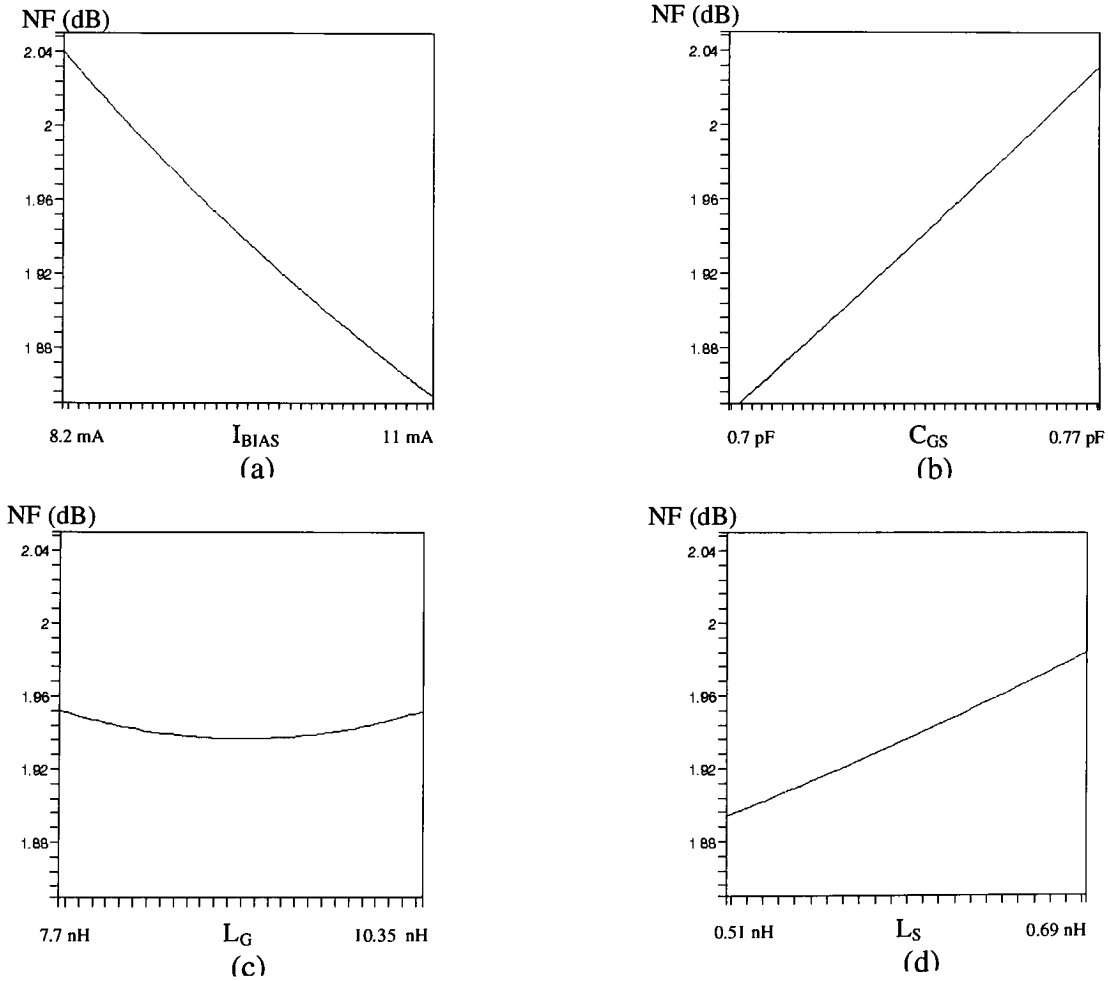


Figure 3.10 Variations in noise figure (dB) versus (a) I_{bias} (b) C_{gs} (c) L_G (d) L_S

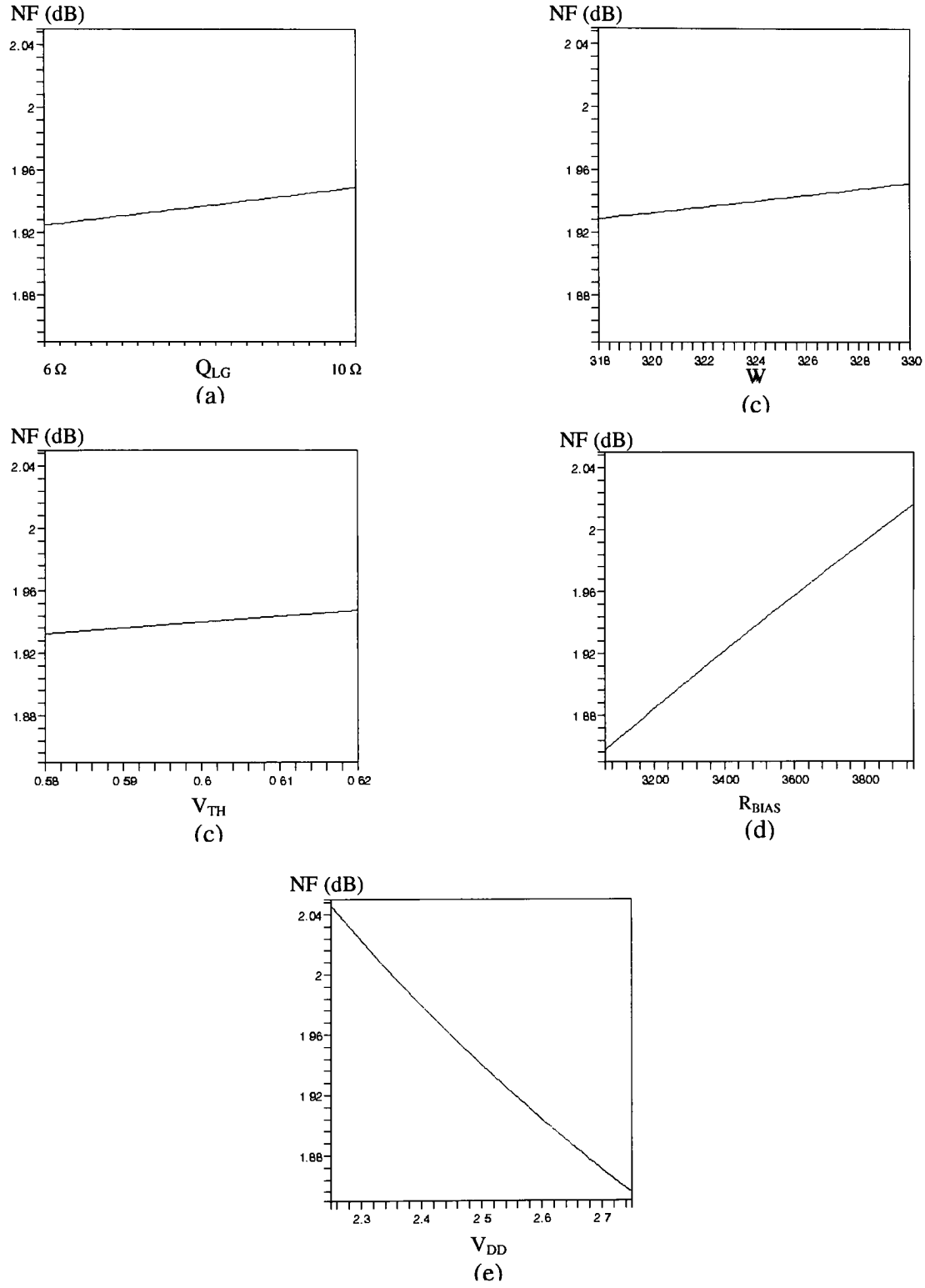


Figure 3.11 Variations in noise figure (dB) versus (a) Q_{LG} (b) W (c) V_{TH} (d) Rbias and (e) V_{DD}

Component	Affects NF?	Sensitivity	ΔNF(dB)
L_G	√	0.001/nH	0.017
L_S	√	0.5/nH	0.09
C_{gs}	√	2.5/pF	**0.18**
W	√	0.004/μm	0.048
I_{BIAS}	√	0.066/mA	**0.185**
V_{TH}	√	0.38/V	0.015
R_{BIAS}	√	0.18/kΩ	**0.16**
L_D	X		
C_D	X		
V_{DD}	√	0.38/V	**0.19**
Q_{LG}	√	0.006/pΩ	0.024
Q_{LD}	X		

Table 3.4 Sensitivity table for Noise Figure

The three biggest contributors for NF degradation are bias-point, C_{GS} and power-supply variations. Increasing power consumption or decreasing the gain (gain-NF trade-off) can lead to better noise figures. The analysis also highlights a power-noise trade-off, where higher power consumption can lead to lower noise figures.

3.6 OUTPUT MATCH

3.6.1 S_{22} frequency

The output side of the LNA is depicted in Figure 3.12, where R_{par} is the parasitic resistance of the load coil. The output impedance of the LNA is often not transformed (down-converted), since the mixer that follows can be designed with the appropriate input-impedance network.

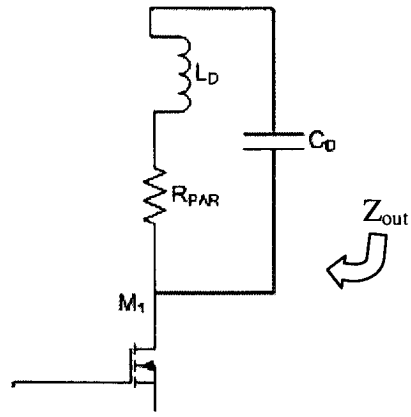


Figure 3.12 Output side of the cascode LNA

The output resonant frequency is given by $f_{out} = \frac{1}{2\pi\sqrt{L_d C_d}}$ (3.20)

The variation in f_{out} due to deviations in L_D and C_D is shown in Figure 3.13, and the sensitivity of L_D is given by:

$$\frac{\partial f_{out}}{\partial L_D} = -\frac{C_D}{4\pi[L_D C_D]^{3/2}} \quad (3.21)$$

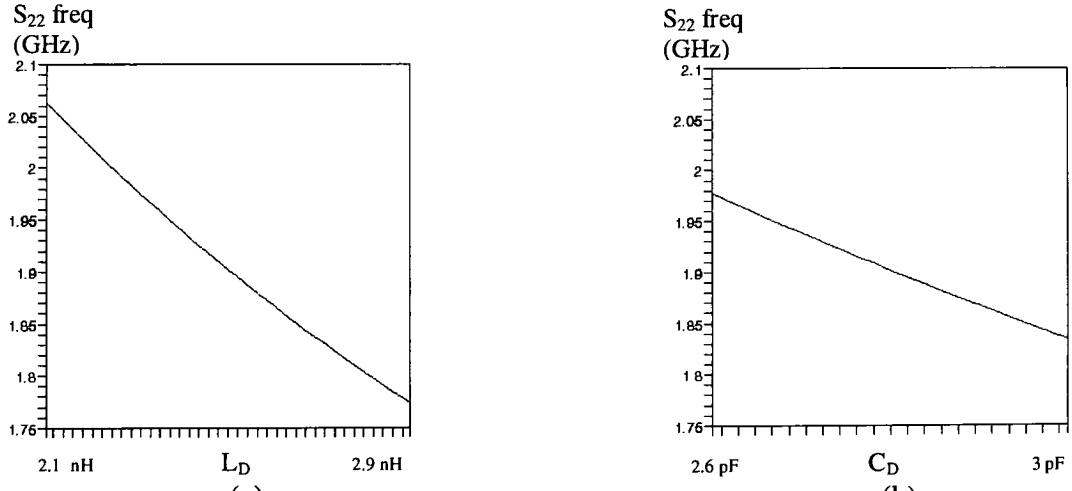


Figure 3.13 Deviation in S_{22} frequency versus (a) L_D and (b) C_D

The sensitivity of Table 3.5 is created as before.

Component	Affects f_{out}?	Sensitivity	Δf_{out} (GHz)
L_G	X		
L_S	X		
C_{gs}	X		
W	X		
I_{BIAS}	X		
V_{TH}	X		
R_{BIAS}	X		
L_D	√	0.38GHz/nH	**0.29**
C_D	√	0.34GHz/pF	**0.143**
V_{DD}	X		
Q_{LD}	X		
Q_{LG}	X		

Table 3.5 Sensitivity table for S_{22} frequency

While both L_D and C_D are candidates for tuning the output-match, toggling L_D with switches potentially impacts gain (through higher parasitic resistance of L_D), as shown in the gain sensitivity table. Hence the practical choice is to replace C_D with a bank of varactors.

3.6.2 Magnitude of Z_{out}

The output impedance Z_{out} is given by (Figure 3.12):

$$Z_{OUT} = \frac{j\omega L_D + R_{par}}{1 - \omega^2 L_D C_D + j\omega R_{par} C_D} \tag{3.22}$$

For the 1.9 GHz LNA under consideration, the sensitivity of Z_{out} to the Q of the load coil is given by[14] $\frac{\partial Z_{out}}{\partial R_{par}}$, and Figure 3.14 shows the impact of Q-variation and other components on the output impedance. Following a process similar to that of section 3.6.1, we arrive at the sensitivity Table 3.6.

[14] Quality-factor of a coil is the ratio of $\omega L/R_{par}$, where R_{par} is the parasitic resistance. Due to ease of computation, *Q-sensitivity* has been replaced with R_{par} *-sensitivity.*

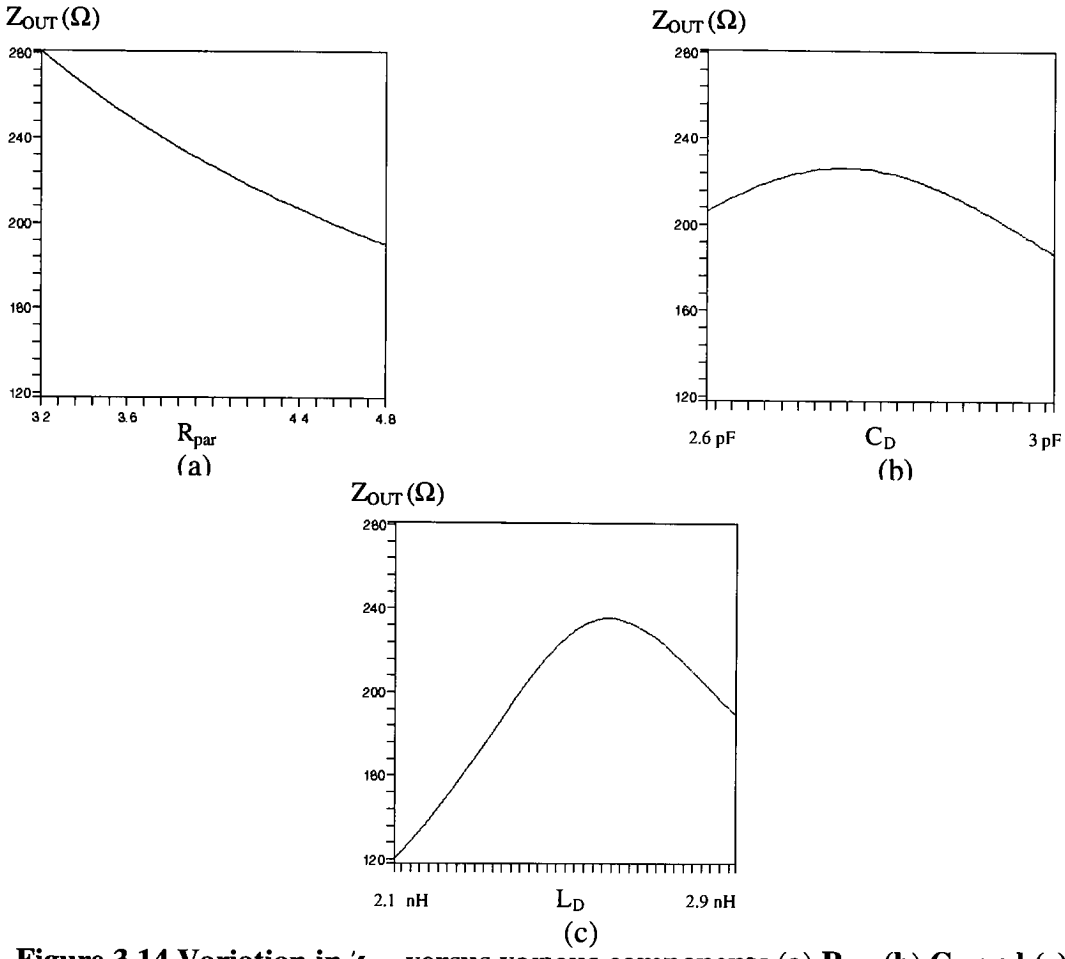


Figure 3.14 Variation in Z_{out} versus various components (a) R_{par} (b) C_D and (c) L_D

Component	Affects Z_{out}?	Sensitivity	ΔZ_{out} (Ω)
L_G	X		
L_S	X		
C_{gs}	X		
W	X		
I_{BIAS}	X		
V_{TH}	X		
R_{BIAS}	X		
L_D	√	98.8/nH	**59.5**
C_D	√	71.2/pF	34
V_{DD}	X		
Q_{LD}	√	55.3/pΩ	**88**
Q_{LG}	X		

Table 3.6 Sensitivity table for magnitude of Z_{out}

3.7 LINEARITY

Intercept-point and 1-dB compression point are the two accepted metrics to quantify linearity of RF circuits. This section discusses the sensitivity of the input-referred intercept point (IIP3) of the third harmonic for the cascode LNA. To the first order (neglecting all higher harmonics above the 3rd) there exists a simple relationship between IIP3 and 1-db compression point[15] [12]:

$$1\text{-dB} = \text{IIP3} - 9.6\ \text{dB} \tag{3.23}$$

The IIP is quantified by the three-point method [11], as it is computationally more efficient compared to the power-series expansion method [13]. In this method, there is no necessity of computing double and triple derivatives in this approach. IIP3 is thus given by:

$$\text{IIP3} = \frac{4V^2}{Q^2 R_S}\left(\frac{g_m(0)}{g_m(V)+g_m(-V)-2g_m(0)}\right) \tag{3.24}$$

where $g_m(F)$ is a function of the input amplitude[16], R_S is the source resistance, V is a DC bias increment, and Q is the input stage Q-factor given by:

$$Q = \frac{1}{(R_S + |Z_{in}|)\omega C_{gs}} \tag{3.25}$$

The transconductance $\left(\frac{\partial I_d}{\partial V_{gs}}\right)$ is calculated from the following current equation [14]:

$$I_d = \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}\frac{(V_{gs}-V_t)^2}{1+\theta(V_{gs}-V_t)} \tag{3.26}$$

---

[15] This relationship is true only to the first-order, and the difference tends to increase for short-channel processes (as gate lengths scale from the 0.25 μm towards sub-100 nm nodes). There does, however, exist a one-on-one correlation between 1-dB point and IIP3 for any given process.

[16] The incremental gain is computed at three different input amplitudes, with 0 being the reference and +V and –V being the other two voltages. For this work, V has been chosen as 50 mV.

where θ is known as the mobility degradation factor. Owing to the dependence of mobility on the bias conditions, this effect has to be accounted for accurate IIP3 computations. θ is empirically extracted for a given process; for the IBM 0.25 μm process, it was extracted to a value of 2.5.

For the LNA design being considered, the variation in IIP3 versus various components is shown in Figures 3.15 and 3.16, and the sensitivities are summarized in Table 3.7. The nominal IIP3 was 5.40 dBm[17]. It is seen that linearity exhibits a huge dependency on bias voltage (current). This fact is exploited later, when IIP3 needs to be made variable in incremental steps. By adjusting the bias current in minor increments, the IIP3 can be varied over an appropriate window of values.

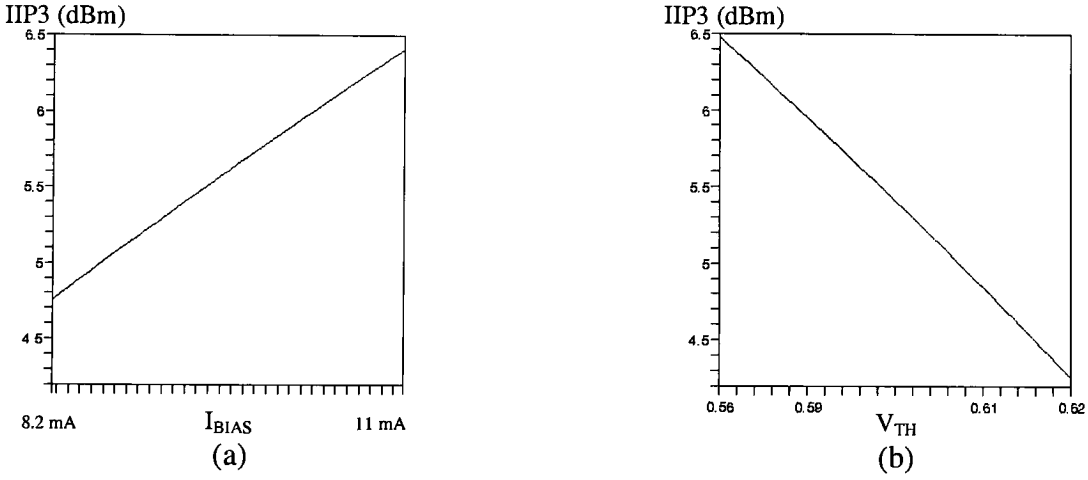


Figure 3.15 Deviations in IIP3 versus component variations (a) I_{BIAS} (b) V_{TH}

[17] This value is higher when compared to simulation or experimental results, since all harmonics above the 3rd have been ignored. The sensitivity values and the net deviation due to component variations, however, remain within 5% of simulated values.

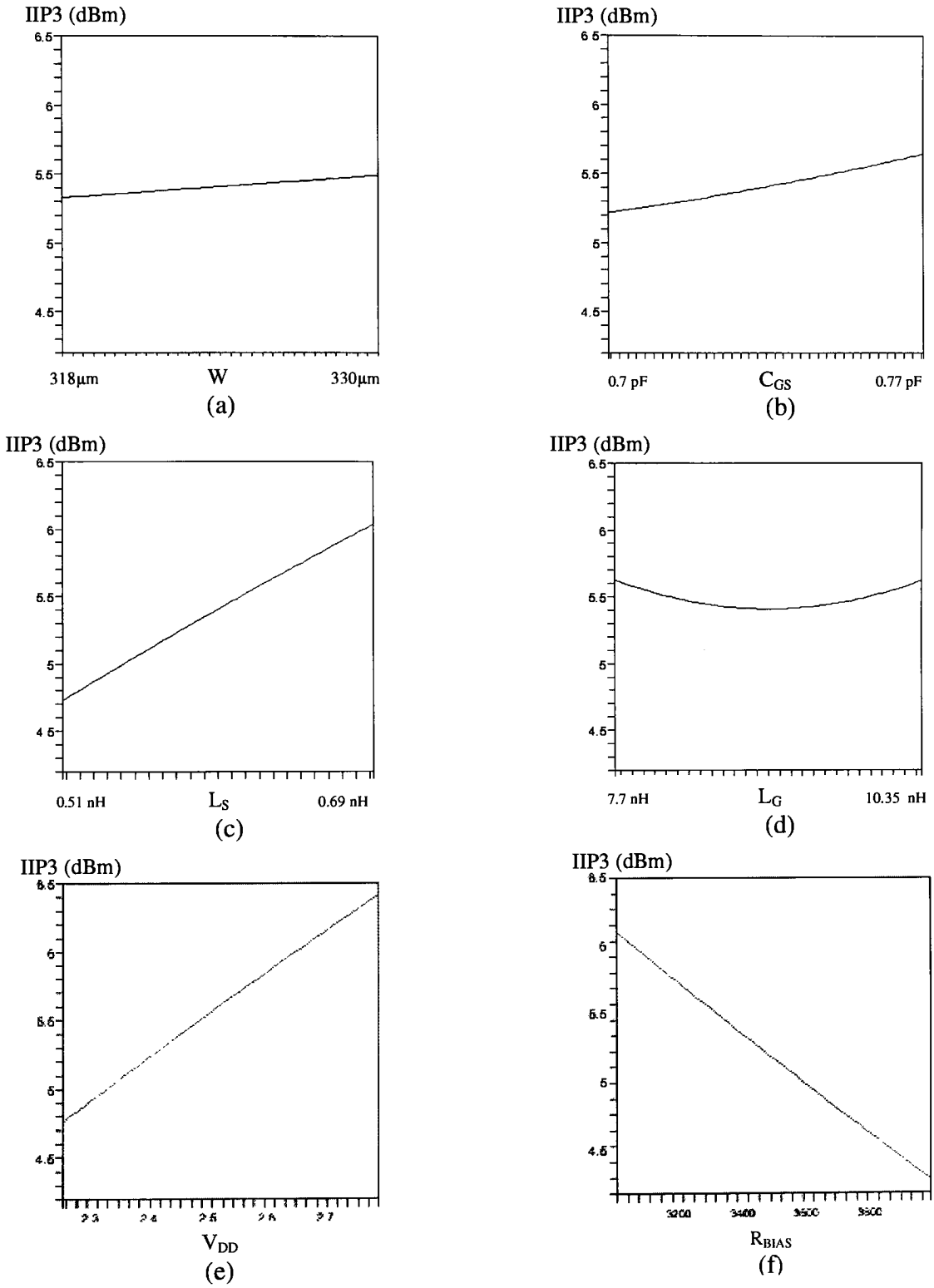


Figure 3.16 Deviations in IIP3 versus component variations (a) W (b) C_{GS} (c) L_S (d) L_G (e) V_{DD} (f) R_{BIAS}

Component	Affects IIP3?	Sensitivity	ΔIIP3 (dBm)
L_G	√	0.002/nH	0.19
L_S	√	7.24/nH	1.3
C_{gs}	√	5.92/pF	0.43
W	√	0.013/μm	0.156
I_{BIAS}	√	0.59/mA	**1.65**
V_{TH}	√	55.34/V	**2.21**
R_{BIAS}	√	1.76/KΩ	**1.55**
L_D	X		
C_D	X		
V_{DD}	√	3.28/V	**1.64**
Q_{LD}	X		
Q_{LG}	X		

Table 3.7 Sensitivity table for IIP3

3.8 SUMMARY

The input-match frequency is most sensitive to the gate inductor (L_G). Further, the sensitivity of other specifications to L_G is very low, making it an ideal target for varying its value to achieve adaptability in input-match frequency. The use of switches to vary the inductance of L_G (section 7.1.1) does impact its Q-factor, and negatively affects the Noise Figure of the LNA, increasing it by about 10-12%. This is an overhead of the adaptable-S_{11} method used in this work.

The two components that affect S_{22} frequency are the load coil (L_D) and the load capacitance (C_D). While it is possible to make L_D variable similar to the adaptability achieved in S_{11}, this severely degrades the gain of the LNA. This effect is due to the high sensitivity of gain on the Q-factor L_D, as is borne out it table 3.3. It is therefore less intrusive to make C_D variable by using a bank of varactors instead of a fixed capacitance. This approach does not degrade other performance specifications.

Misalignment in the S_{22} frequency (variations in load-coil or capacitance) degrades gain significantly. Hence calibrating the output-match also improves gain. Gain is also sensitive to Q-factor of load-coil and the source-coil. While the Q-factor of the coil is not in the designer's control to make it adaptive, reducing the value of the source-coil improves gain but degrades linearity (as shown in figure 3.16). Varying the width of the cascode transistors can be a possible solution, but the corresponding change in gate-source capacitance degrades the input-match, as is borne out in table 3.1. Hence the ideal solution will be varying the widths, while keeping gate-source capacitance constant. The current-splitting transconductance array developed in this work (section 7.1.3) achieves this objective.

It has been shown with the help of simulations that the sensitivity of specifications to reverse isolation is very low (less than 1%), and the cascode topology inherently affords high isolation. Consequently, it is not practically necessary to design mechanisms that sense or correct S_{12}. While sensing noise in an integrated environment is strewn with obstacles (section 6.3 discusses why it cannot be sensed on-chip), its sensitivity analysis has been included to study the impact of the adaptive mechanisms on the noise figure.

The analysis on linearity shows a very high sensitivity to the bias conditions (almost an order of magnitude higher than the other components). Consequently, the approach to achieve adaptability in IIP3 in this work involves varying the bias current. The Gain analysis shows that increasing the bias current to improve linearity also impacts the gain, but in a positive manner. The above conclusions form the basis for the circuit

adaptability techniques discussed in chapter 7, in addition to providing the quantifications necessary to design such an adaptive circuit.

Chapter 4. ARCHITECTURE

4.1 LIMITATIONS OF FEEDBACK IN THE RF DOMAIN

Traditionally, soft-fault degradation in analog circuits has been corrected by using voltage or current feedback, where a part of the output voltage or current is sampled and fed back to the input to achieve increased robustness. However, this technique has several pitfalls when applied to the RF domain. In integrated RF front ends, it is not always possible to have access to the output port of the individual circuit to sample the output signal without influencing the performance of the circuit. Due to the nature of parasitics at these frequencies, any interfacing or sensing circuitry will significantly impact the performance of the RF circuit. In addition to this, feedback components such as transformers, inductors, etc., have wide tolerances making the entire feedback system unreliable. This approach creates significantly complex stability issues. In comparison to low frequency circuits, RF circuits are highly sensitive to layout parasitics and mutual coupling effects. Metal trace parasitics, in the order of a tenth of a nano-henry and tens of femto-farads are no longer negligible due to operations in the GHz domain. While stability is inherently difficult to achieve at these frequencies, such fine sensitivity to parasitics and coupling further complicates the issue, degrading both reliability and predictability. It is thus seen that traditional feedback techniques introduce significant design complexity, creating a need for the complete redesign of the RF circuit in question as a feedback system, with all its associated complexity. Furthermore, RF circuits with no

feedback are pushed to the limit in terms of performance, and it becomes extremely hard to generate any additional power gain to trade-off for increased robustness.

4.2 Alternate Methodology: The 'Locked-Loop' Approach

This work describes an alternate technique that senses the performance of the RF circuit with minimal intrusion while simultaneously removing the constraints associated with feedback. The objective of fault-tolerance was addressed by a four fold approach: firstly, to sense a signal which is indicative of the performance metric; secondly, to process this signal appropriately into a form which quantitatively describes this metric; thirdly, to use this information to send a signal back to the circuit where the metric can be re-calibrated towards the desired value, and finally to provide a mechanism in the circuit which can adaptively change the metric in real time based on the aforementioned signal.

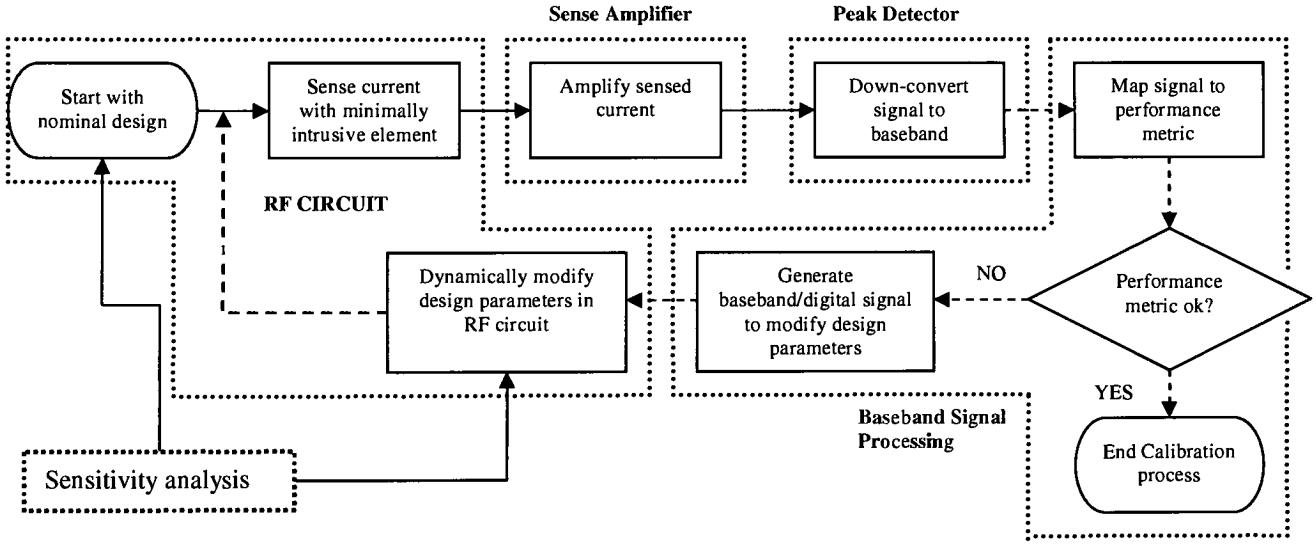


Figure 4.1 Architecture for fault-tolerance [35] [36] [38]

The technique (Figure 4.1) consists of an RF forward path where RF information (in the case of this work, the transient HF current or voltage) corresponding to the circuit

performance is sensed with minimal intrusion and amplified to required levels. As will be described in greater detail in subsequent sections, since this methodology does not pose any noise requirements, simple amplifiers with resistive loads can be used to achieve this gain. Also due to the robustness of the differential techniques used, the actual numerical value of the gain does not influence the self-correction. This amplified information is then down converted to base-band or DC for further processing. The resultant baseband/digital signal quantifies the performance metric under question and can be used (either directly or with additional processing) as a Built-in-Self Test (BiST) readout. This signal is then used, along with the Sensitivity Analysis (Chapter 3) to modify the requisite design parameters in the RF circuit to correct for the variation in performance without requiring any redesign of the original circuit. Since the sense-and-correct mechanism is not necessarily routed from the output node back to the input node, the proposed method lays much greater emphasis on avoiding intrusion into the circuit performance. In addition to this, the entire feedback path functions in the low frequency or DC domain thereby alleviating the stringent noise and stability requirements that plague traditional feedback schemes. Since most of the processing circuitry acts on low frequency signals, these circuits will also present relatively low overheads in the RF front-end. Instead of sampling/summing the input/output nodes of the circuit as in feedback, the performance metric is measured, and a decision is made, dynamically, to modify (if required) a design parameter in the circuit. This 'self-correction' signal is in the form of a digital word, eliminating the potential problems of noise and precision.

The portion of the architecture after the peak detector (figure 4.1) can be placed either on-chip or off-chip. Off-chip processing will not compromise accuracy since low

frequency or DC signals can be transported via pads and probes without the interconnect and contact parasitics (relatively) degrading the signal. These low frequency signals can be processed using a dedicated test-board, and the circuit can be fed instructions on the components to be modified for performance correction. The advantages if keeping the entire architecture on-chip are ease of implementation and use (no external connections, reduced processing times, reduced cost), with the downside being the additional real-estate. This methodology and techniques used in this work are designed re-use the same hardware for all the circuit specifications, and hence minimize the real-estate overheads. Consequently, this work implements the entire architecture on-chip, with the total real-estate overhead (including all components in figure 4.1) is less than 10% of the standard LNA. If lower overheads are desirable for commercial implementations, then all of the low-frequency and digital components can be moved off-chip.

Chapter 5. SENSING MECHANISMS

The objective of this step is to establish a means of sensing some signal(s) from the circuit that, with further processing if required, will ultimately provide information about its performance metrics. Further, this sensing mechanism must be minimally intrusive on the performance of the circuit, and present overheads that make it viable to be practically implemented.

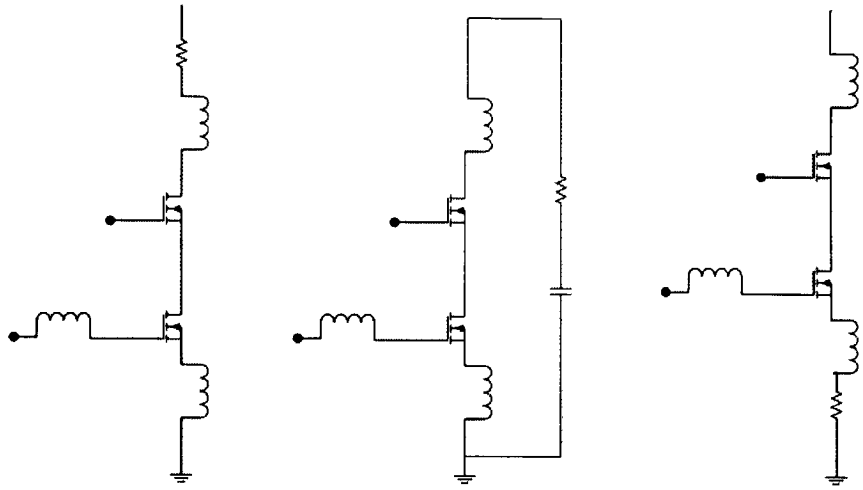
5.1 CURRENT SENSING

RF circuits draw current from the power supply, which provides definite signatures that can be analyzed (with minimal intrusion) to determine circuit attributes.

5.1.1 Resistor as sensing element (R_S)

Some potential placements of the sensing element for a single-ended Cascode LNA are shown in Figure 5.1 [15]. Placing it in series with the drain inductor, as shown in Figure 5.1 (a) degrades gain, S_{22} and noise figure. It can be placed in series with the bypass capacitor (Figure 5.1(b)), which is necessarily present in almost every RF circuit[18]. This placement however, degrades gain and S_{22} significantly. Placing it in series with the source inductor (Figure 5.1(c)), and re-designing the input match along with the sensing resistor results in minimal impact on S_{11} and noise figure.

[18] RF circuits have bypass capacitors to provide the H.F. current, since the power supply path from the outside path will present non-negligible parasitic impedances.



(a) (b) (c)

Figure 5.1 Potential placements for the sensing resistor. Adapted from [30] [29]

From the above discussion it is evident that, in terms of minimal intrusion, placing a small resistor (in the order of a few ohms) in series with the source inductor results in the optimal solution. This approach creates a voltage indicative of the circuit's performance with minimal intrusion on the circuit's behavior.

5.1.2 Source degenerative inductor as sensing element (L_S)

Although minimally intrusive (due to its small value), the sensing resistor still affects certain aspects of the RF circuit performance. It increases the noise figure of the circuit to the extent of 8-12%. In case of the LNA this contribution could be significant in certain extremely low noise applications. Another drawback is the loss of dynamic range by 2-3%. Finally, the circuit under test needs to be co-designed to account for the additional resistance in the equation for input match. Although these trade-offs are necessary to enhance the reliability of the RF circuit in general, this work demonstrates that the resistor can be eliminated for circuits with a source-degeneration coil, which is then used as the sensing element [40]. This approach offers a better solution for RF

communication circuits, which often utilize inductive source degeneration. This class of circuits includes the standard cascode LNA, folded-cascode LNA, most types of differential LNAs, the standard single balanced mixer and some double balanced mixers. The current work uses the voltage dropped across the source degeneration inductor (L_S) to extract and quantify information about the performance of the circuit. This voltage is amplified and peak-detected to DC, and this DC value is processed to quantify the performance. The method eliminates the use of a sense resistor and results in a technique that makes the leap from minimal intrusion to non-measurable intrusion, where the sensing mechanism will have no measurable effect at the operating frequency of the circuit. As the operating frequency is increased, the capacitance presented by the sensor that is interfaced to the LNA will begin to reduce the self-resonant frequency of L_S. In this work, the self-resonant frequency occurs at 26 GHz, an order of magnitude higher than the operating frequencies, which lie in the sub-3 GHz band.

5.1.3 Validity of the L_S approach

In this section we establish the usability of tapping into the source coil instead of using a small valued resistor. In principle, the tones used for sensing (as elaborated in the following sections of this chapter) occur within a narrow frequency range, and more importantly, since discrete single-frequency input stimuli are used, the inductor can be viewed as a frequency-varying resistance. In order to quantify and verify this concept, the voltage equations are presented and the two methods are graphically compared for a source degenerated cascode LNA. The input voltage of the LNA is described by the following equation when the sensing resistor R_S is used (see Figure 5.2) [40]:

$$V_{IN} = i\frac{g_m L_S}{C_{GS}} + i\left(j\omega(L_S + L_G) + \frac{1}{j\omega C_{GS}} \right) + iR_S + i\frac{g_m R_S}{j\omega C_{GS}} \tag{5.1}$$

where i is the input current as shown in figure 5.2. From equation 5.1, i is derived as:

$$i = \frac{V_{IN}}{\left(\frac{g_m L_S}{C_{GS}} + \left(j\omega(L_S + L_G) - \frac{j}{\omega C_{GS}} \right) + R_S - j\frac{g_m R_S}{\omega C_{GS}} \right)} \tag{5.2}$$

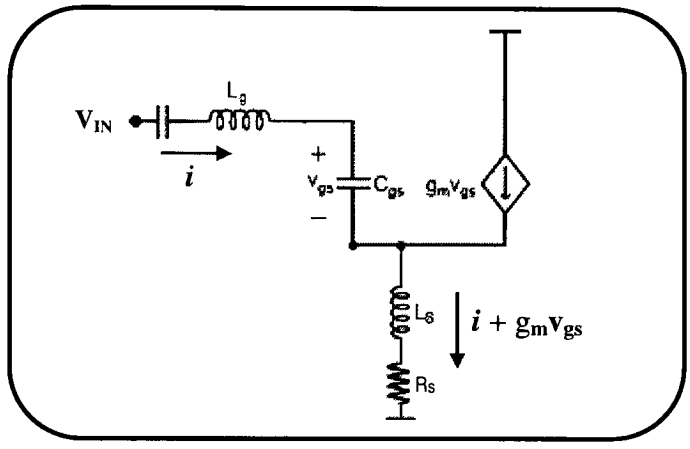


Figure 5.2 Input side of LNA with Sensing resistor. The input-transistor has been replaced with its small-signal model

The voltage across the resistor R_S is described as:

$$V_{RS} = R_S(i + g_m V_{gs}) = \frac{V_{IN} R_S \left(1 - \frac{j g_m}{\omega C_{GS}} \right)}{\left(\frac{g_m L_S}{C_{GS}} + j\left(\omega(L_S + L_G) - \frac{1}{\omega C_{GS}} \right) + R_S - \frac{j g_m R_S}{\omega C_{GS}} \right)} \tag{5.3}$$

When the sensing resistor is eliminated, the voltage across L_S is sensed, and equation (5.3) transforms to (L_S case):

$$V_{LS} = \frac{V_{IN}.L_S.\left(j\omega + \frac{g_m}{C_{GS}}\right)}{\left(\frac{g_m.L_S}{C_{GS}} + j\left(\omega.(L_S + L_G) - \frac{1}{\omega.C_{GS}}\right)\right)} \tag{5.4}$$

By using different gate inductors, five LNAs with differing input-match frequencies were designed (Appendix B shows the circuit schematic and component values. The same design of chapter 3 has been used in this analysis. Appendix A lists the specific device data used in all designs of this work). The five different gate inductors used were valued at 7.4 nH, 8.1 nH, 9 nH, 10 nH and 11 nH.

The voltages developed across the source inductor (L_S case) and the sensing resistor (R_S case) for these five LNAs are compared in Figure 5.3. It is seen that the voltage spectra across the source inductor differentiates different input-match frequencies similar to the R_S case. If the output voltage spectra are sensed at two discrete frequencies (shown by the dotted lines in Figure 5.3), then the voltage values change monotonically as S_{11} changes, thus quantifying changes in input-match frequency. This behavior is true for both R_S and L_S sensing approaches. The width of this region, denoted by dotted lines in Figure 5.3, is slightly higher in the L_S case. Apart from this difference, the two cases differentiate input-match behavior with the same sensitivity and accuracy.

In this example, the value of R_S was 7 ohms and that of L_S was 0.6 nH, and the voltages developed across them were in the same order of magnitude. Hence, the source inductor can replace the sensing resistor, eliminating the need to use a foreign sensing element. There exists a minimum value of L_S below which changes in sensed voltages will be too weak to detect. This value is frequency dependent, and an approximate rule of thumb that defines a value for L_S is to equate the two impedances of L_S and R_S ($\omega L_S = R_S$).

Thus, as the operating frequencies increase, the lower bound for L_S keeps reducing. The operating frequency used in this work is 1.9 GHz, and the impedance of L_S is valued at 7.16 Ω (versus R_S of 7Ω) at this frequency.

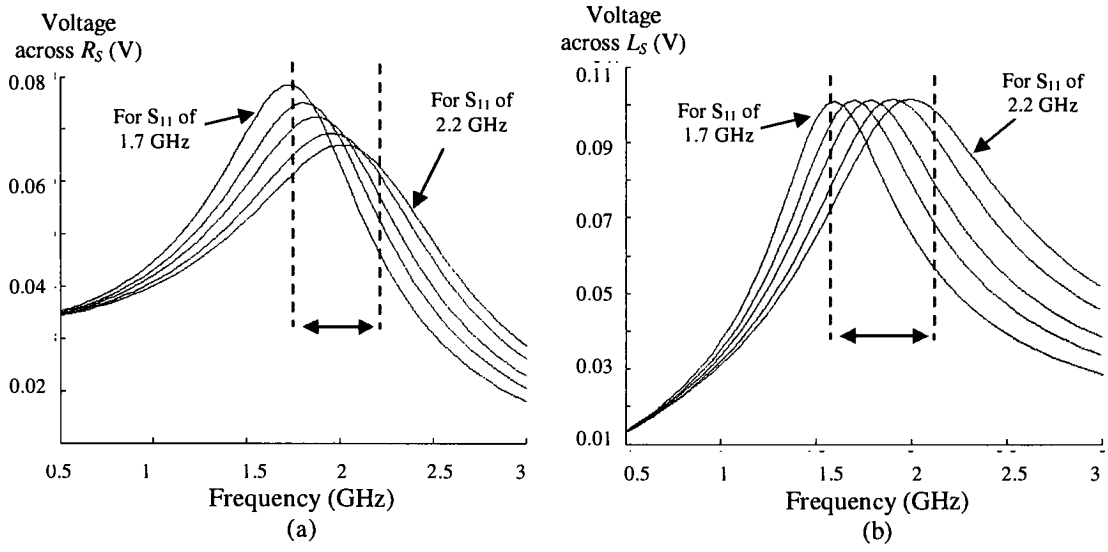


Figure 5.3 Voltage versus frequency across (a) R_S and (b) L_S for 5 different LNAs with input match varying from 1.7 GHz to 2.2 GHz [40] [29]

5.1.4 Advantages of the L_S approach

The intrusion of the L_S approach (voltage sensed across L_S is sensed and processed) compared with the R_S approach (voltage sensed across R_S is sensed and processed), with the performance of the standard LNA (without any sensing circuitry or element) as the ideal state. The circuit details for the R_S approach are listed Appendix B, while that for the L_S case are in Figure 3.1.

The input-match behavior for the three cases is depicted in Figure 5.4 (b). The ideal state from the standard LNA is -38 dB, the degradation due to the sensing resistor is 5 dB (-33 dB), and that due to the sensing inductor is 1 dB (-37 dB). In addition to the above degradation, the use of R_S also degrades Noise Figure (NF), as seen in Figure 5.4

(a). The degradation of NF in the RS case in 0.2 dB, while it remains practically unaltered (it reduces by 0.96%) when the sensing inductor (L_S) is used.

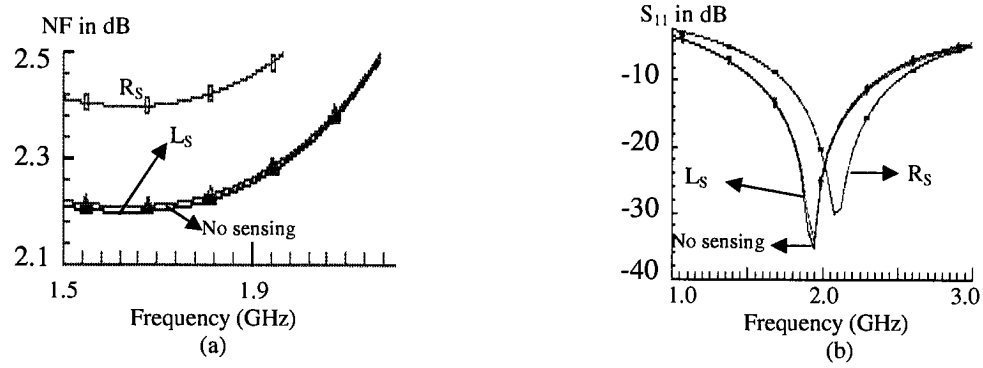


Figure 5.4 (a) Noise Figure for L_S, R_S and stand-alone LNAs and (b) S_{11} for L_S, R_S and stand-alone LNAs [40] [29]

As already discussed in section 3.4, the cascode LNA topology possesses high reverse isolation, and hence changes on the input-side of the circuit do not impact the output side. Thus, adding an additional resistance in the input-side of the circuit does not impact gain or output-match. The gain and output match remain unaffected in the L_S case also, since the entire circuit remains the same as the standard LNA (figure 3.1). Further, the LS method does not suffer from any dynamic range degradation, since no foreign element is added to the circuit (In the R_S approach, adding the extra resistance in the signal path reduces headroom and dynamic range by 1-2%). Therefore, the advantage of this approach lies in the fact that it offers a sensing mechanism with no measurable intrusion on the performance of the circuit. However, one precaution must be observed. The capacitance of the circuit that interfaces to the source-coil, along with the source-coil forms a LC network that can potentially resonate. It is important to keep the value of the capacitance low enough to keep this resonant frequency much higher than the frequency of operation. The source-follower interface used in this work achieves this objective:

60 fF of capacitance, along with 0.6 nH translates to a self-resonant frequency greater than 26 GHz, which is more than an order of magnitude greater than the operating frequency.

The sensor consists of a source-follower and an amplifying section (circuit schematic and description in section 8.2), since the sensed signal is in the order of a few *tens of millivolts.* The amplified signal is then peak-detected to DC for all further processing. It is possible to distinguish changes in the current due to faults on the output side of the circuit by using a similar mechanism at the input side of the next circuit in the RF front-end chain (for example, the LNA is followed by a Mixer). As described in the following chapter, the same sensor can be interfaced with the source degenerative coil of the mixer to sense the output impedance matching of the LNA.

5.2 Voltage Sensing

For specifications such as gain and linearity, peak-to-peak voltage at the output is sensed by using a source-follower as the interface. This method has no measurable impact on the circuit's performance (less than 1% degradation) specifications, as seen in Figure 5.5. The only (minor) variation observed was in S_{22}, due to the added capacitance at the output node. This capacitance will not affect circuit performance under normal conditions because the sensor circuitry, along with the source-follower will be powered down. Furthermore, since S_{22} sensing is carried out at the mixer's input section, the source-follower at the output of the LNA will be powered down during S_{22} sensing and calibration as well, ensuring that no intrusion is possible.

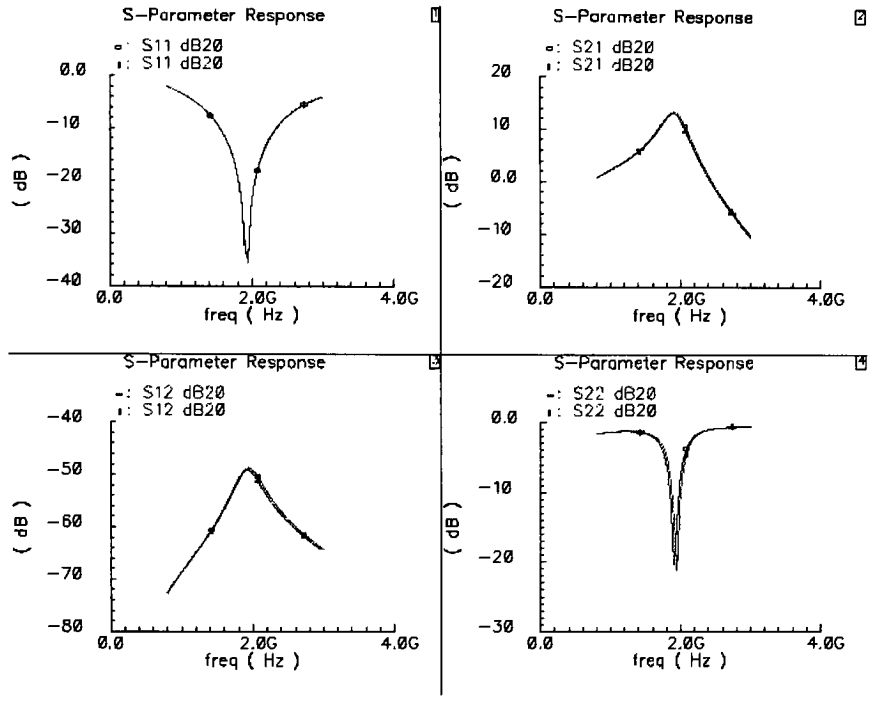


Figure 5.5 Simulated S-parameters before and after the sensor placement at the output node of LNA. The curves overlap, and no measurable degradation was observed

There was no degradation observed in Noise Figure and linearity specifications as well. The simulated values of NF and IIP3 were 2.13 dB and -6.011 dB, respectively, in both cases. The output of the source follower is immediately peak-detected and converted to DC, since no amplification is necessary[19]. Circuit details and description of the sensor are discussed in Chapter 8.

[19] The signal at the output of the LNA will be in the order of 1-2 V (when the appropriate input stimulus is applied), and needs no further amplification

Chapter 6. PERFORMANCE QUANTIFICATION

6.1 SENSING S_{11} AND S_{22}

While S_{11} is sensed at the source coil of the LNA (as discussed in the previous chapter), variations in S_{22} cannot be detected at this node. A traditional cascode LNA is designed to have very little coupling between the input and output side [11]. Therefore any fault in the output side will not be reflected strongly on the input side of the LNA and consequently, on the current through the source inductor of the LNA. However, the LNA will usually feed a mixer either directly or through a filter. If the same scheme is applied at the RF input of the mixer, this can be used to quantify faults in the output side of the LNA in addition to faults on the input side of the mixer. An alternative manner of viewing the technique described previously is that it enables one to essentially quantify the signal entering the gate of the FET through the preceding circuitry. Therefore by quantifying the magnitude of the signal entering the mixer it is possible to detect faults that affect the output match of the LNA. It may be argued that it is not possible to use this technique to distinguish between faults in the input-match of the mixer and output of the LNA. However, if the LNA is connected directly to the mixer, a fault on the output side of the LNA has the same effect on overall performance as a fault on the input side of the mixer this method attempts to correct variation in the RF front-end performance without regard for the actual location of the fault. For example, the signal coming into the RF input of the mixer at the frequency of the mixer may be attenuated either due to a matching mismatch at the LNA's output-side or the input-matching network of the mixer.

However, the effect of both these faults with respect to the magnitude of signal entering the mixer will be the same. Hence S_{11} is sensed at the source of the LNA, and S22 at the source of the mixer. The following sections describe the quantification methods, which are common to both S_{11} and S_{22}

6.2 IMPEDANCE MATCHING (S_{11} AND S_{22}): THE 'TWO-TONAL' APPROACH

The variations in the source current of the LNA (mixer), and hence the peak-peak voltage across the sensing inductor can be used to quantify its input (output) match performance. The voltage across the source coil is amplified (by the Sense Amplifier, SA) and peak-detected (by the peak detector, PD) to DC. To ascertain the exact offset through which the tuning-frequency needs to be shifted and to render this technique independent of process, temperature and power supply variations in the sensing circuitry itself, a novel two-tonal approach was developed [35].

6.2.1 Mapping of match frequency to sensed voltage

At a given frequency, the input/output impedance of the LNA and hence the sensed voltage varies monotonically as the S_{11}/S_{22} match is either increased or decreased. The impedance looking into the input terminal of the LNA (Figure 6.1) is given by [11]:

$$Z_{in} = \frac{g_m L_S}{C_{GS}} + j(\omega(L_S + L_G) - \frac{1}{\omega C_{GS}}) \tag{6.1}$$

With ω_m as the designed match frequency, let the two tones be:

$$\omega_1 = \omega_m - \Delta\omega \text{ and } \omega_2 = \omega_m + \Delta\omega \tag{6.2}$$

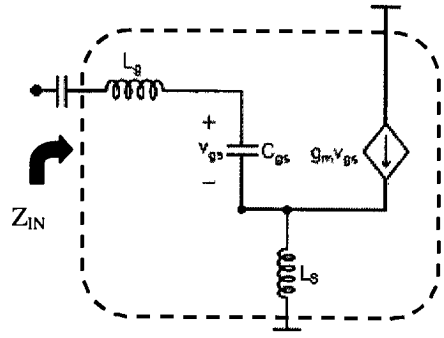


Figure 6.1 Input-section of Cascode LNA

The input impedance at ω_1 is given by:

$$Z_{in}(\omega_1) = j(\omega_m - \Delta\omega)(L_G + L_S) - \frac{j}{(\omega_m - \Delta\omega)C_{GS}} + \frac{g_m L_S}{C_{GS}} \tag{6.3}$$

Since $j\omega_m(L_G + L_S) = \frac{j}{\omega_m C_{GS}}$, (and the input impedance at ω_m is $Z_M = \frac{g_m L_S}{C_{GS}}$), it simplifies to:

$$Z_{in}(\omega_1) = \frac{g_m L_S}{C_{GS}} - j2(\Delta\omega)(L_G + L_S) \tag{6.4}$$

$$\text{Similarly, } Z_{in}(\omega_2) = \frac{g_m L_S}{C_{GS}} + j2(\Delta\omega)(L_G + L_S) \tag{6.5}$$

It is seen that the magnitudes of both $Z_{in}(\omega_1)$ and $Z_{in}(\omega_2)$ are higher than Z_M. Suppose the value of the gate coil (L_G) changes due to a perturbation or fault:

$$L_G' = L_G + \Delta L \tag{6.6}$$

Consequently, the input impedances change to:

$$Z_{in}'(\omega_1) = \frac{g_m L_S}{C_{GS}} - j[2\Delta\omega(L_G + L_S) - (\omega_m - \Delta\omega)\Delta L] \tag{6.7}$$

$$Z_{in}'(\omega_2) = \frac{g_m L_S}{C_{GS}} + j[2\Delta\omega(L_G + L_S) + (\omega_m + \Delta\omega)\Delta L] \tag{6.8}$$

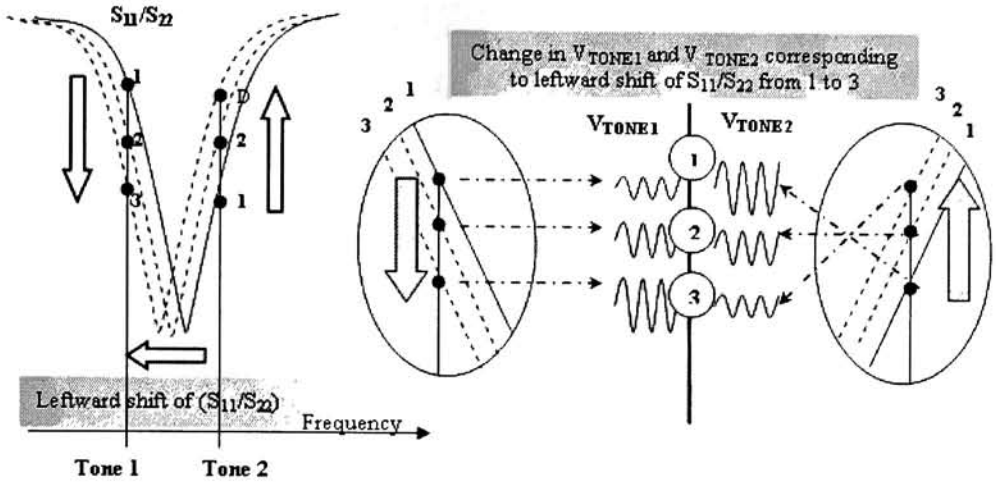


Figure 6.2 The 'two-tonal' approach [36] [39] [29]

The magnitude of $Z_{in}'(\omega_1)$ has dropped due to the increase in L_G, bringing the impedance closer to Z_M (S_{11} has improved, Figure 6.2), while that of $Z_{in}'(\omega_2)$ has increased, moving it further away from Z_M (S_{11} has degraded, Figure 6.2). The difference between these values, $|Z_{in}'(\omega_1)| - |Z_{in}'(\omega_1)|$, is a measure of the change in the input match frequency. This difference also manifests itself as a voltage difference across the source coil of the LNA. The voltage across L_S is given by:

$$V_S = Ij\omega L_S \tag{6.9}$$

where V_S is the peak-peak voltage across L_S, and I is the total current through L_S, given by:

$$I = \frac{v_{in}}{Z_{in}}[1 - \frac{jg_m}{\omega C_{GS}}], \text{ with } v_{in} \text{ being the input stimuli} \tag{6.10}$$

The difference in the sensed voltages then is given by:

$$V_S(\omega_1) - V_S(\omega_2) = jL_S v_{in}[\frac{\omega_1}{Z_{in}'(\omega_1)}(1-\frac{jg_m}{\omega_1 C_{GS}}) - \frac{\omega_2}{Z_{in}'(\omega_2)}(1-\frac{jg_m}{\omega_2 C_{GS}})] \quad (6.11)$$

When an input stimulus at the first tone (*tone1*) is applied, the peak-peak value of the sensed voltage decreases as S_{11} frequency is increases. Similarly, for the second tone (*tone2*), the peak-peak value increases for increase in S_{11} frequency. This behavior is depicted in Figure 6.2 (V_{tone1} and V_{tone2}). The spectra of the sensed voltage for varying input-match frequencies is shown in Figure 6.3 (device and circuit details given in Appendix C), and the corresponding differences in the two tones are shown in Figure 6.4. This difference of the tonal responses (V_{tone1} and V_{tone2}) quantifies the deviation in S_{11} frequency from its ideal case. Consequently, it quantifies the value by which the match-frequency should be moved to compensate for this deviation.

Further, if both tones are made to pass through the same sensing and peak detector circuitry, this method will be inherently insensitive to process variations, temperature and power supply variations[20] since only their difference is processed. This differential method of ascertaining input match frequency renders the technique immune, for example, even to a 50% variation in the gain of subsequent amplifying circuitry, tolerances in the value of the sensing element or the precision of the input test signal itself. Based on the required sensitivity of detecting the input match frequency, this voltage needs to be amplified to provide minimum detectable levels, accounting for offsets and variations in the processing circuitry.

[20] Since the method is not truly differential (the two tones are processed serially), noise can impact measurements. However, this methodology is designed to be applied on a circuit-by-circuit basis, and as such, all other circuits including DSP and digital circuits on the same chip will be powered down or stay in idle mode while the self-correction is initiated. This is possible since no normal operation is possible while self-correction process is in progress. Thus, drastically different noise profiles for the two tones (within a space of a few microseconds) are not anticipated.

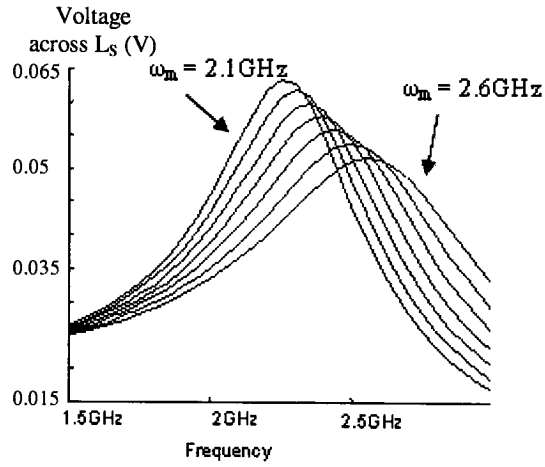


Figure 6.3 Spectrum of peak-peak V_S in V for different input-match frequencies [35].

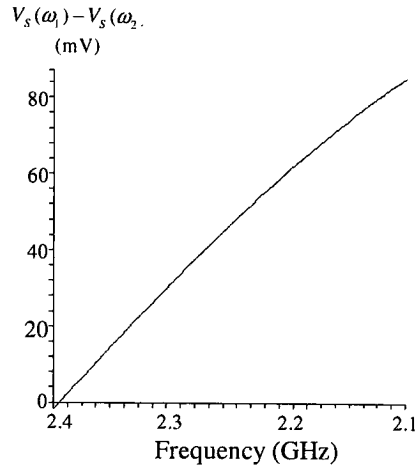


Figure 6.4 Peak-peak value of $V_S(\omega_1) - V_S(\omega_2)$ in mV versus input match frequency. It increases monotonically as the S_{11} frequency is decreased [35].

With proper selection of the two tones (discussed in the following section), it can be ensured that the curve of Figure 6.4 will remain linear for the entire range of S_{11} degradation. In other words, if input-match degradation from 2.4 GHz to 2.1 GHz is anticipated, then the two tones must be chosen such that the entire region of the curve between 2.4 GHz and 2.1 GHz is linear (as is the case in Figure 6.4).

6.2.2 Choice of the two tones

With ω_m being the designed match frequency, ω_m', the perturbed match frequency, can be defined as:

$$\omega_m' = \frac{1}{\sqrt{(L_G + L_S + \Delta L_G + \Delta L_S)(C_{GS} + \Delta C_{GS})}} \qquad (6.11)$$

where ΔL_G, ΔL_S and ΔC_{GS} are the maximum anticipated deviations from their ideal value. To ensure monotonocity in the sensed voltage response, $\Delta\omega$ should be chosen such that (Figure 6.5):

$$\Delta\omega > \omega_m - \omega_m' \tag{6.12}$$

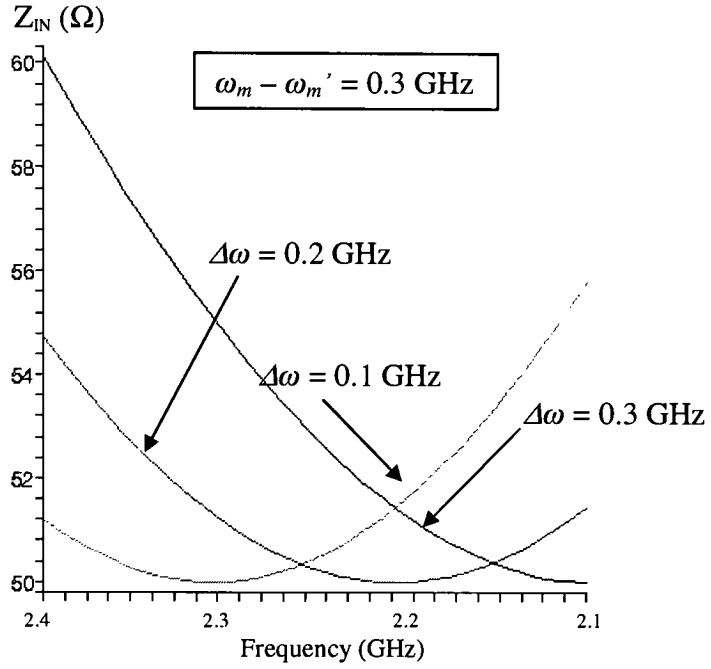


Figure 6.5 $\Delta\omega > \omega_m - \omega_m'$ is necessary for a monotonic response. The y-axis shows variation in Z_{in} versus S_{11} frequency for different $\Delta\omega$, for a 2.4 GHz LNA [35]

Further, to maximize the sensitivity of detecting frequency changes $\Delta\omega$ should be chosen such that it maximizes the voltage difference for various input match frequencies. This optimization problem is the solution to the equation

$$\frac{\partial[V_S(\omega_1) - V_S(\omega_2)]}{\partial(\Delta\omega)} = 0 \tag{6.13}$$

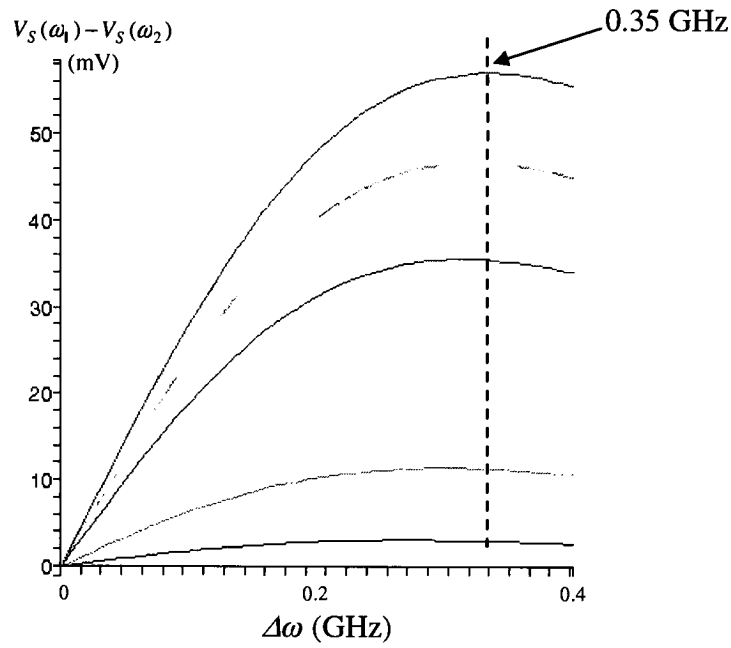


Figure 6.6 Peak-peak value of $V_S(\omega_1) - V_S(\omega_2)$ in *mV* versus $\Delta\omega$ for different input match frequencies. It is seen that optimal $\Delta\omega$ is at 0.35 GHz in this case [35].

For a 2.4 GHz LNA (circuit details in Appendix C), Figure 6.6 shows that the optimal value of $\Delta\omega$ is 0.35 GHz. This process, although described for the input match of a cascode LNA, is applicable in general to any impedance matching segment, including the output match of the LNA. The *tens of mV* range of sensed voltage will be amplified to adequate levels before further processing.

6.2.3 Limitations of the two-tonal approach

It is possible, with the two-tonal approach, to encounter S_{11} shifts similar to that shown in Figure 6.7. In such cases, the approach fails to detect the shift in S_{11} frequency, and one tap in the gate-coil may be missed, leading to a sub-optimal input-match.

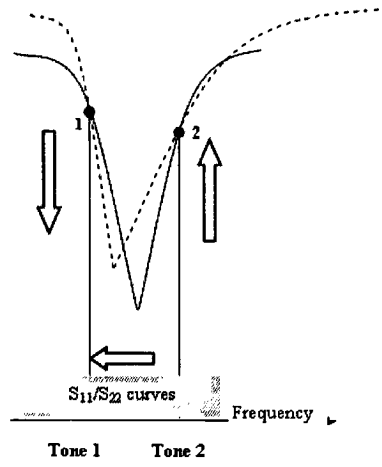


Figure 6.7 Limitation of two-tonal approach

One solution to faultlessly detect such cases is to include a third and, if required, fourth tone to cover for such possibilities. This approach will increase the overheads and processing time of the correction cycle. Another solution is to program redundant taps into the design (more resolution than necessary for the application). With this approach, even if the optimal tap is missed, the redundancy helps in keeping S_{11} within acceptable limits. Although this solution increases processing time of the correction cycle, it does not require additional hardware (real-estate). The limitation of this method is the lower bound on the spacing between taps. Redundancy cannot be built-in if it infringes on the minimum spacing required between taps.

However, extensive Monte Carlo simulations (Section 9.6.1 discusses these results) show that the coverage offered by the two-tonal approach is upwards of 98%, and hence justify their adequacy. In commercial implementations where 100% accuracy is needed to ensure that failed chips do not reach the end-customer, additional testing via ATE will be needed. It should, however, be mentioned, that existing self-test methods (discussed in Chapter 2) do not have accuracies higher than that of this work.

6.3 Sensing Gain and Linearity

While it is possible to sense the gain and linearity of the LNA from the source-coil of the mixer (similar to the output-match), it compromises the robustness of the approach – the gain and linearity variations in the amplifying circuitry (amplification is necessary since the sensed signal from the inductor is small in magnitude) can contribute to errors in the quantification, and may thus necessitate a de-embedding procedure[21].

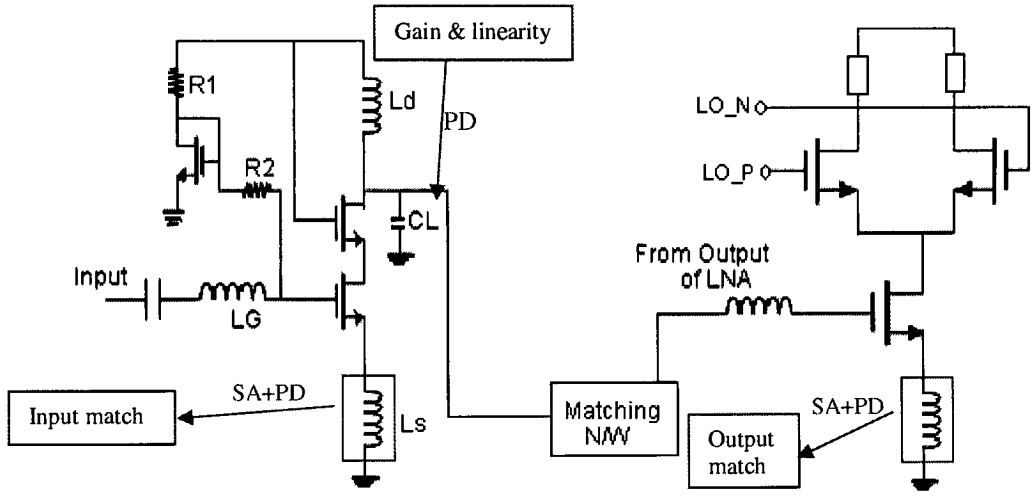


Figure 6.8 Sensing elements and sensor-positions for the LNA

As has already been mentioned in the previous chapter, placing a source-follower and peak-detector at the output node of the LNA has no measurable impact on the LNA's performance, and does not need any amplifying circuitry (Sense Amplifier, SA) in the sensor. The input stimulus for both gain and linearity must have the same frequency as the operating frequency of the front-end system, and can be generated by the VCO of the system. The peak-peak output (Peak Detector, PD) for such a stimulus gives a direct

[21] Gain variations of the amplifying circuitry can be erroneously attributed to the LNA's gain. It thus becomes necessary to de-embed the gain of the amplifying circuitry from the system.

measure of the gain of the LNA. Figure 6.8 summarizes the sensing positions and sensor placements for the LNA.

LNA linearity, often quantified by using IIP3 or 1-dB compression point, provides a measure of the harmonic inter-modulation distortion at its output. In Chapter 2, we have stated the relationship between IIP3 and 1-db compression point. This section explains a process that quantifies the linear behavior of the voltage transfer characteristic of the LNA, thereby presenting a quantitative measure of its linearity. It will also be shown that this quantification has a direct one-on-one correlation to IIP3 of the LNA, thus proving that the sensing mechanism used here does indeed (indirectly) quantify the IIP3, and hence linearity of the LNA.

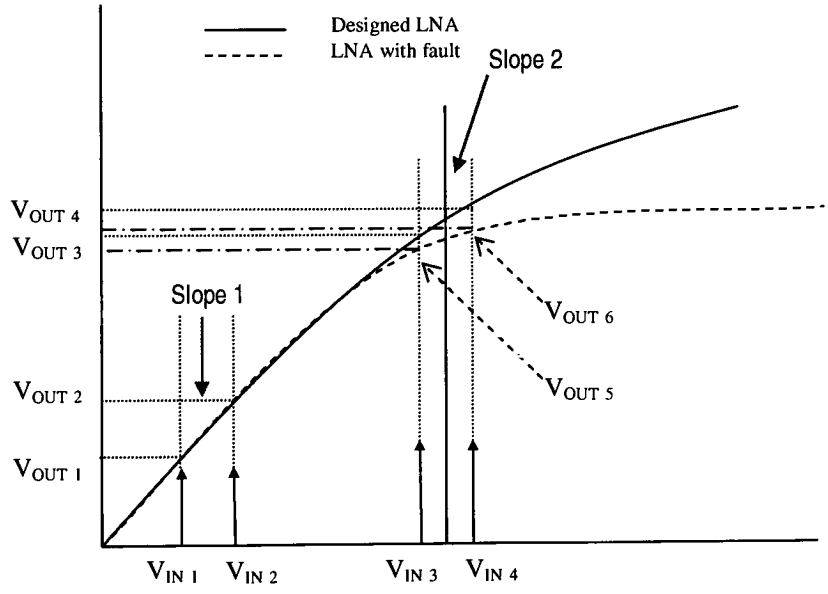


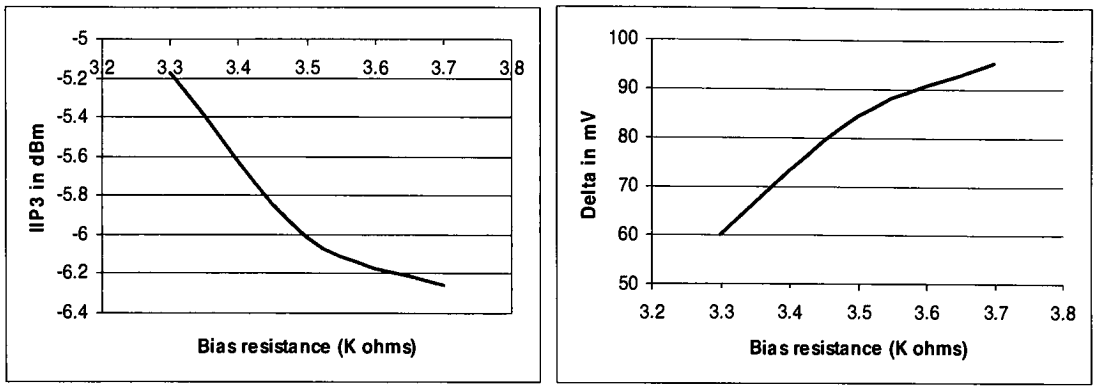
Figure 6.9 Quantifying Linearity. Hypothetical case shown. [41] [29]

Two pre-determined input stimuli, V_{IN1} and V_{IN2} (Figure 6.9) are applied to the LNA at the operating frequency of the front-end system. The output responses for these stimuli, V_{IN3} and V_{IN4} respectively (Figure 6.9), are peak-detected to DC and stored. The

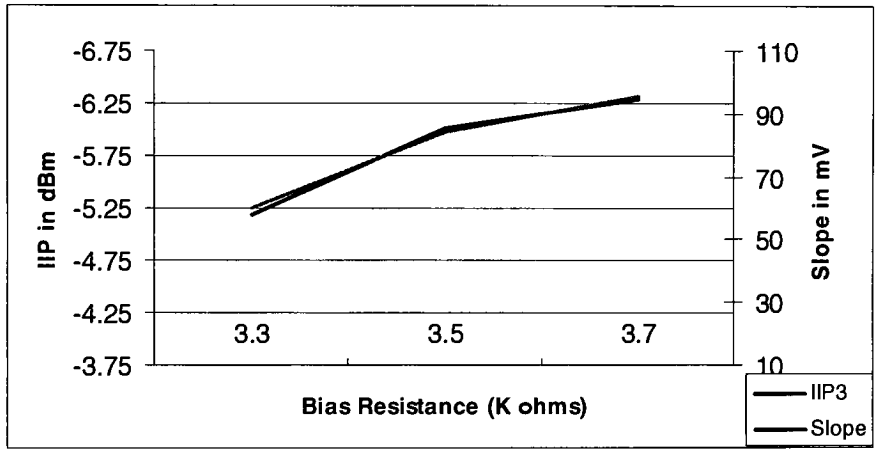
difference between the output responses of these stimuli (V_{IN4}-V_{IN3}) quantifies the slope of the curve about V_{IN1} and V_{IN2}, and is referred to as Slope1. This process is then repeated with a second set of stimuli, V_{IN3} and V_{IN4} (Figure 6.9), about the 1-db compression point of the LNA. The output responses are again peak detected and stored, and their difference (V_{OUT4}-V_{OUT3}) is referred to as Slope2. In a fault-free LNA (ideal case), the difference between Slope1 and Slope2 will be a finite number, and this value (will have to be obtained from measurements with a fault-free LNA) represents the ideal calibration voltage against which all subsequent LNAs will be compared against. Any degradation in LNA linearity (hypothetical case, $V_{OUT\,6} - V_{OUT\,5}$, as shown by the dotted curve in Figure 6.9) will lead to a different Slope1-Slope2 value, thus quantifying this degradation.

To further validate the correlation of this computed signal to IIP3, extensive simulations were executed for different instances of the LNA with varying IIP3s[22] (by varying the bias resistance, R_{BIAS} in Figure 3.1, over 400 Ω). Figure 6.10 depicts simulation sets for LNAs with various IIP3 values in Figure 6.10 (a), and linearity sensing using voltage slopes (Slope1-Slope2) for the same LNAs in Figure 6.10(b). It is seen from Figure 6.10 (c) that the difference between the two slopes (Slope1-Slope2) tracks changes in IIP3 (the two curves of Figure 6.10(a) and 6.10(b) have been plotted on the same x-axis scale, with the IIP3 curve inverted): as IIP3 decreases, the difference increases, signaling an increase in the non-linearity. Once again, since this technique uses two inputs and a differential scheme, it is independent of absolute value of gain, tolerances, etc.

[22] The same design of Figure 3.1 is used.



(a) (b)



(c)

Figure 6.10 (a) shows varying IIP3 as the bias resistance (R_{BIAS}, Figure 3.1) is varied (b) shows the corresponding difference voltage using the slope method (c) superimposes the curves of (a) (inverted) and (b) to illustrate the tracking

6.4 Reverse Isolation and Noise Figure

As has been concluded in Chapter 3, S_{12} has sensitivities of zero or near-zero for most component variations due to the nature of the circuit topology. It therefore does not need any quantification or correction mechanisms. The remainder of this section provides a brief description on the obstacles in the way of sensing noise in an integrated environment.

The IEEE standard definition of the noise factor (F) is given by [17]:

$$F = \frac{N_a + kT_0BG}{kT_0BG} \tag{6.14}$$

where N_a is the noise added by system, T_0 is 290K (standard temperature), B is the system bandwidth, k is the Boltzmann constant and G is the gain of the system. The Noise Figure (NF), expressed in decibels, is given by 10*log(F). Two commonly used approaches [16] exist to ascertain the NF of a given circuit: the direct noise measurement method and the Y-Factor method.

6.4.1 Direct Noise measurement method

This approach involves terminating the input of the circuit by a matched load at a temperature of 290K, and directly measuring the noise power at the output. For use in a completely integrated environment, this approach poses two main obstacles. Firstly, the input pad needs to be connected to a passive load, which involves significant intrusion, with switches toggling different terminations. The switches, in addition to degrading the signal path, will also contribute to a measurement error by adding their own noise. Secondly, the measurement of noise power at the output requires an extremely accurate, highly linear, high sensitivity integrated power detector. It is hard to design and implement such a circuit, given the power levels and process variations involved.

6.4.2 The Y-factor method

The Y-factor approach [16] is employed in most commonly used RF NF meters/analyzers. In this approach, a known noise source is used at the input of the circuit, and the output noise power is measured with the noise source on (N_2) and off

(N_1). The Y-factor is the ratio of these two outputs ($Y=N_2/N_1$). With this measurement, the noise added by the circuit is given by [17]:

$$N_a = kT_0BG(\frac{ENR}{Y-1}-1) \qquad (6.15)$$

where ENR[23] (Excess Noise Ratio) is a pre-calibrated value stored on the internal memory of the NF meter. The calculation of this ENR has to be extremely precise, and involves toggling the noise source between two known noise levels using a programmed attenuator. For use in an integrated self-calibration scheme, this approach poses multiple impediments. The complexity of circuits (noise source, ENR calibration, programmed attenuator, gain amplifier following the circuit-under-test, power detector) required translates to large overheads. Further, the gain and noise characteristics of the additional circuitry must be accurately known, so that it can be de-embedded from the final measurements. This poses a problem, since these circuits are prone to process variations and faults themselves. An additional problem is that the ENR calibration requires external inputs and measurement equipment. The accuracy of the NF measurement depends heavily on the accuracy of the ENR calibration.

Due to these factors, the fault-tolerance architecture of this work[24] cannot sense or calibrate the Noise Figure directly. Indirect optimization of Noise Figure is achieved with

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[23] ENR is a pre-calibrated value for the noise source. Using the programmed attenuator, the equivalent noise temperature is calculated for the two different noise levels (T_h and T_C). ENR in dB is then given by $10\log(\frac{T_H-T_C}{T_0})$

[24] There does not exist any other published literature that captures the noise characteristics of a circuit in an integrated environment

self-calibration of other performance specifications such as gain, output match and linearity.

6.5 SUMMARY

This chapter provides sensing mechanisms, algorithms and sensor placement techniques for four major LNA specifications. The fifth, reverse isolation, does not require any sensing or correction, while Noise Figure remains an elusive metric to quantify. Hence the methodology used in this work can quantify the performance of all LNA specifications except the Noise Figure.

SPECIFICATION	COMMENT
Input-match	Sensed at source-coil of LNA, amplified and peak detected
Output-match	Sensed at source-coil of Mixer, amplified and peak detected
Gain	Sensed at output node of LNA, peak detected
Linearity	Sensed at output node of LNA, peak detected
Reverse isolation	Not necessary to quantify
Noise Figure	Cannot be quantified by this architecture

Table 6.1 Summary of performance quantification techniques for the LNA

Chapter 7. PERFORMANCE CORRECTION

This chapter discusses the processing algorithms, necessary circuit functionality and self-calibration mechanisms for the LNA. The emphasis is on low-overhead solutions – in the three areas of power, area and intrusion. A 1.9 GHz cascode narrow-band LNA has been designed and fabricated in the IBM6RF 0.25 μm process. With the standard cascode LNA of Figure 3.1 as the base, various parameters are made adaptive as discussed in the remainder of the chapter.

7.1 SELF-CALIBRATION MECHANISMS

As described in Chapter 2, the architecture uses a digital self-calibration approach to overcome limitations and complexities of feedback. Hence the self-calibration mechanisms are designed for calibrating the specification in discrete steps (rather than continuous), and use a digital bit-stream as the control signal.

7.1.1 S_{11}

In order to adaptively move the input match of the LNA, the gate inductor (L_G in figure 3.1) value is made variable by tapping it at several points on its outer turn (Figure 7.1) [36]. The sensitivity analysis of Chapter 3 demonstrated that the gate inductor has a high sensitivity towards S_{11}, while having a negligible sensitivity towards other performance specifications. This fact makes it the ideal candidate for use in S_{11} self-calibration. Package parasitics introduce additional inductance (with very large tolerances) at the input pad of the LNA [21] (for example, bond wires). Hence, this

technique allows one to correct for variations in input match due to process faults or package parasitics and also facilitates the use of the LNA in different packages with different parasitic inductances, since the circuit can re-align itself to the original input match.

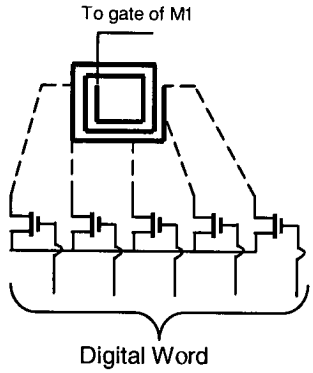


Figure 7.1 Digitally tapped gate coil [36]

The gate coil (L_G) is designed for a nominal value and then tapped off at different intervals in its outer-most turn, with each tap leading to a switch. By including all interconnects and switch parasitics in the design process, this coil can be characterized to give accurate inductance values. This characterization is accomplished using ASITIC [20], a commonly used inductor characterization tool. The inductor coil, interconnects, and NMOS switches are laid out in ASITIC, using the technology file[25] specific to the IBM6RF CMOS process. ASITIC then generates a model for the coil (called the pi-model) that includes the inductance value and all associated parasitics. This model is then exported to the Cadence® Simulation environment, where it is used in the LNA circuit for simulations. The details of the models and parasitics for the specific coil used in this work are described in detail in Chapter 8. Based on which switch is turned on (decided by

[25] The technology file has to be created from data in the IBM6RF PDK documentation. ASITIC documentation explains the process of creation.

a digital word), one and only one tap of the coil will be shorted to the input pad of the LNA, and this tap determines the input match of the LNA. The number of taps and the resolution is determined by the needs of the application, with the aid of the sensitivity analysis of Chapter 3. For example, if the resolution of calibration is set at 0.1 GHz, then the sensitivity analysis determines the spacing in nH for each tap. The input-match frequency is thus made adaptable in increments of ΔL:

$$f_{in} = \frac{1}{2\pi\sqrt{(L_{NOM} + L_S + n.\Delta L)C_{gs}}} \tag{7.1}$$

where n is the number of taps, and

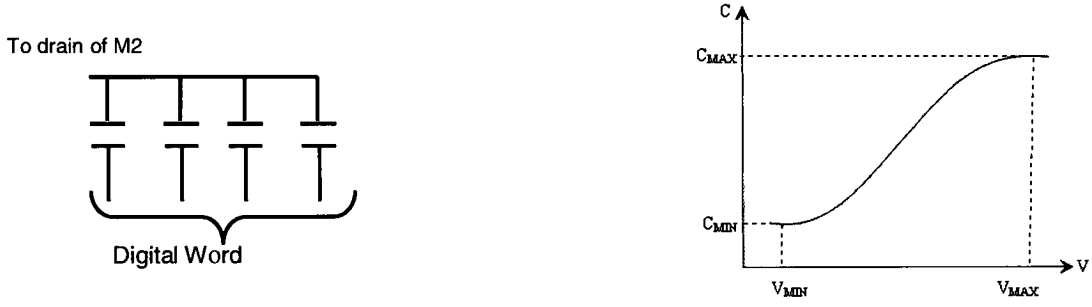
$$L_{NOM} = L_G(designed\ \ value) - (n/2)\ \Delta L \tag{7.2}$$

The overhead of this mechanism is an increase in Noise Figure due to the insertion loss of the MOS switches used. If the process were to be used post-fabrication before packaging (at the wafer level), then one could use laser fuses instead of MOS switches, and the self-calibration process will permanently connect one of the fuses to the inductor. This approach will not add any noise to the system, but loses ability to compensate for package variations or portability.

7.1.2 S_{22}

The S_{22} of the LNA is made variable by using a MOS varactor bank as shown in Figure 7.2 (a) [35]. This bank serves replaces the fixed load capacitance C_L in Figure 3.1. The varactors have a capacitance range of 2.5 (specific to the IBM process being used in this work, $C_{MAX} = 2.5*C_{MIN}$), and are biased to operate in only two modes, at the extreme ends. This method allows the use digital calibration signals (n-bit digital word) to control

S_{22}, and also eliminates the requirement for accurate voltage generation: since the varactors operate only at the two extremes, the sensitivity of the capacitance to control voltage is very low[26] [22], as seen in Figure 7.2(b). This technique also provides immunity to noise, since the control voltages need not be accurate, and noise on the control voltage will not change the capacitance (unless the noise spike is large enough to drive the operating point into the linear region of Figure 7.2 (b)).



(a) (b)

Figure 7.2 (a) Varactor bank for S_{22} adaptability (b) varactor C-V curve [35]

This approach poses no overheads, since a fixed load capacitance is replaced with a bank of varactors. The output resonant frequency is made adaptable in increments of ΔC.

$$f_{out} = \frac{1}{2\pi\sqrt{L_d (C_{NOM} + n\Delta C)}} \tag{7.3}$$

where n is the number of varactors, and

$$C_{NOM}=C_L(designed\ value)-(n/2)\Delta C \tag{7.4}$$

[26] The varactor is extremely sensitive to its control voltage in the mid-ranges, due to a high slope (Capacitance versus control voltage). At the two extremes, the slope is zero, and sensitivity is also near-zero, in addition to having the best possible Q-factor.

Again, the sensitivity analysis authenticates the choice of C_L as the ideal candidate for S_{22} calibration, in addition to forming the basis for determining the number of varactors and their values used. Details specific to the design used in this work are discussed in Chapter 8.

7.1.3 Gain

The gain was made variable by incorporating variable transconductance into the cascode transistors. Figure 7.3(a) depicts one such scheme (The array of transistors replace the cascode pair M_1 and M_2 in Figure 3.1), where the switches connect the cascode transistor either to the DC bias (usually V_{DD}) or ground.

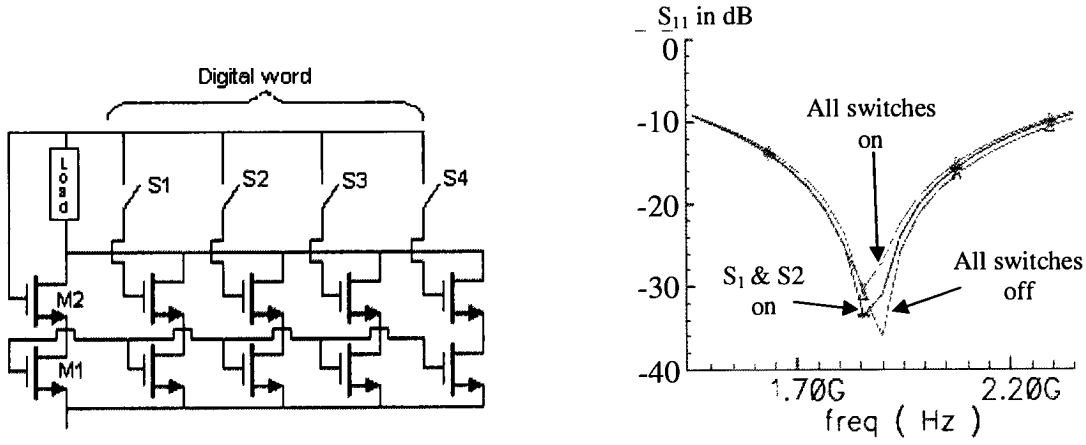


Figure 7.3 (a) Variable-transconductance array, and (b) Impact on S_{11} when the switches are toggled [35]

When connected to V_{DD}, the transistors act as an additional finger for transistors M_1 and M_2, thus increasing the transconductance of the device. This approach, however, has a drawback, as borne out by the sensitivity analysis and simulation results in Figure 7.3(b). Changing transconductance in the abovementioned way also impacts C_{GS}, thus resulting in a minor shift (less than 10%, Figure 7.3(b)) in the input-match characteristics. While this shift could be tolerable for certain applications, the current-splitting transconductance

array of Figure 7.4 overcomes this limitation, albeit at the cost of increased current consumption. Even when the branches are turned off, transient current flows from V_{DD} to ground through an alternate path. This technique of steering current away from the load to vary gain has been used in other applications [32] [33].

When Switch S1 (Figure 7.4(a)) is on, transistor M_{21} is on and M_{22} is off. Hence the current through M_{11} is supplied by M_{21}, which draws current through the load. This increase in the current i_L results in an effective increase in transconductance ($i_L=g_m*V_{gs}$, if V_{gs} remains constant and i_L increases, effective g_m increases). When S1 is off, however, the current through M_{11} is supplied from M_{22}, which bypasses the load and draws the current directly from the supply. Hence the load current (i_L) remains constant, keeping transconductance constant. In both cases, the current through M_{11} remains constant (only the route of the current changes), thus maintaining a constant current on the input-section of the LNA.

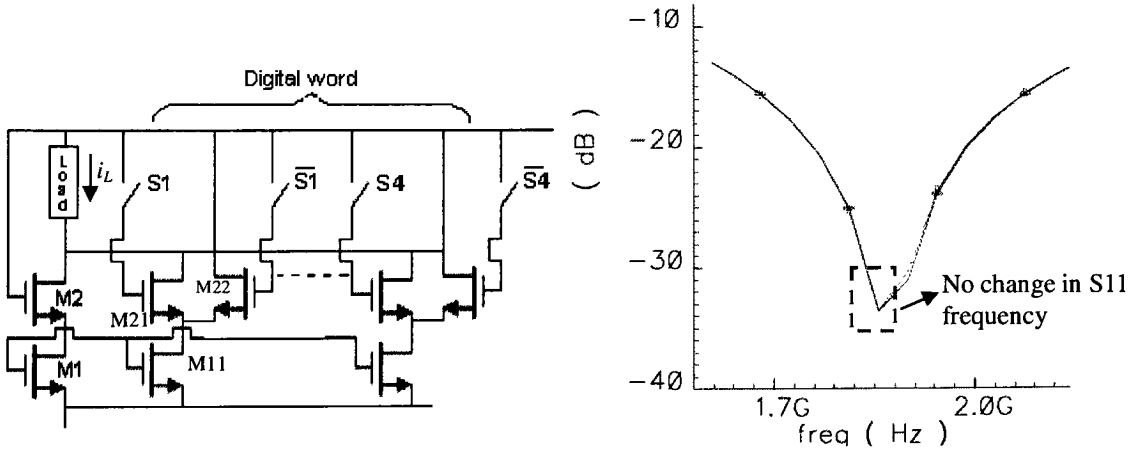


Figure 7.4 (a) current-splitting transconductance array, and (b) Different S_{11} curves as the switches S1-S4 in (a) are toggled. [37]

This approach ensures that there is no change in current or effective W as far as the input-side of the LNA is concerned. It provides variable transconductance as far as

gain is concerned, while not perturbing the S_{11} in any way (since C_{GS} is kept constant), as confirmed by the simulation results of Figure 7.4(b).

The incremental transconductance for gain is given by:

$$g_m = \mu_{eff} C_{ox} \frac{(W_{NOM} + n\Delta W)}{L} (V_{GS} - V_T) \tag{7.5}$$

where n is the number of transconductance branches, and

$$W_{NOM} = W\,(designed) - (n/2)\Delta W \tag{7.6}$$

This equation is valid only for gain, since the input-side of the LNA sees a fixed transconductance throughout. This scheme effectively decouples the influence of g_m on S_{11}. The variable-transconductance on the output side consequently provides the appropriate gain:

$$G = \frac{g_m Z_{out}}{(R_s + Z_{in}) j\omega C_{gs}} \tag{7.7}$$

Thus we have three schemes to dynamically vary S_{11}, S_{22} and gain, with none of the schemes intruding upon the other specifications.

7.1.4 Linearity

While linearity can be sensed using techniques in Chapter 6, non-linearity is an inherent limitation of the MOS device. Consequently, it is extremely hard to directly reduce the non-linearity of the LNA. However, the sensitivity analysis has borne out an interesting dependency that can be exploited. Linearity of the LNA is heavily dependent on the bias current, and the sensitivity of IIP3 is 0.65 dBm per *mA* (increasing current by

1 mA betters IIP3 by 0.65 dBm). Hence it is possible to exploit this high sensitivity on bias current to enhance the linearity of the LNA, within a small window, by increasing the bias current marginally.

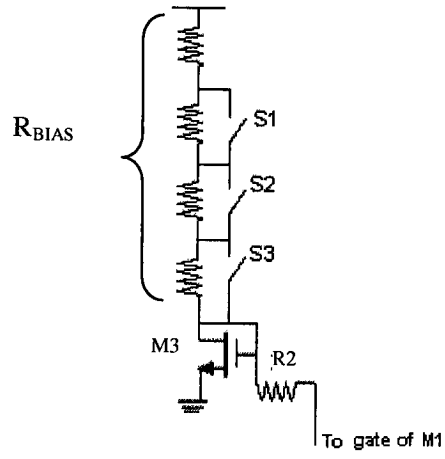


Figure 7.5 Variable bias resistance for IIP3 adaptability

Figure 7.5 depicts a scheme where the bias current is modified in incremental amounts using a digital word that controls the switches[27] [31]. The work in [31] discusses a similar adaptive bias scheme that is digitally controlled by switches for a pipelined ADC circuit. The resistor R_{BIAS} in Figure 3.1 is replaced by a variable resistor array. As the value of the resistor changes (the Switch shorts part of the resistor), the bias current through the transistor M3 changes, thus varying linearity.

The incremental changes in bias current also change the transconductance, which is tied to the gain specification. Hence increasing the bias current to calibrate linearity will also, very marginally (less than 1%), improve the gain specification. It is essential

[27] The switches have a finite on-resistance, and they must be accounted for in the design. The net resistance of each branch when the switches are on is the parallel combination of the resistor and the switch resistance.

that the self-calibration of the specifications follow a specific order, as elaborated in Section 7.3.

7.2 Algorithms and Circuit Architecture

This section describes the algorithms and architecture required for input-match self-calibration in detail. The algorithms for the other specifications are similar to the input-match case, and the same circuitry is re-used in each case. The circuit architecture is depicted in Figure 7.6 and the algorithm for calibration is outlined below [36]:

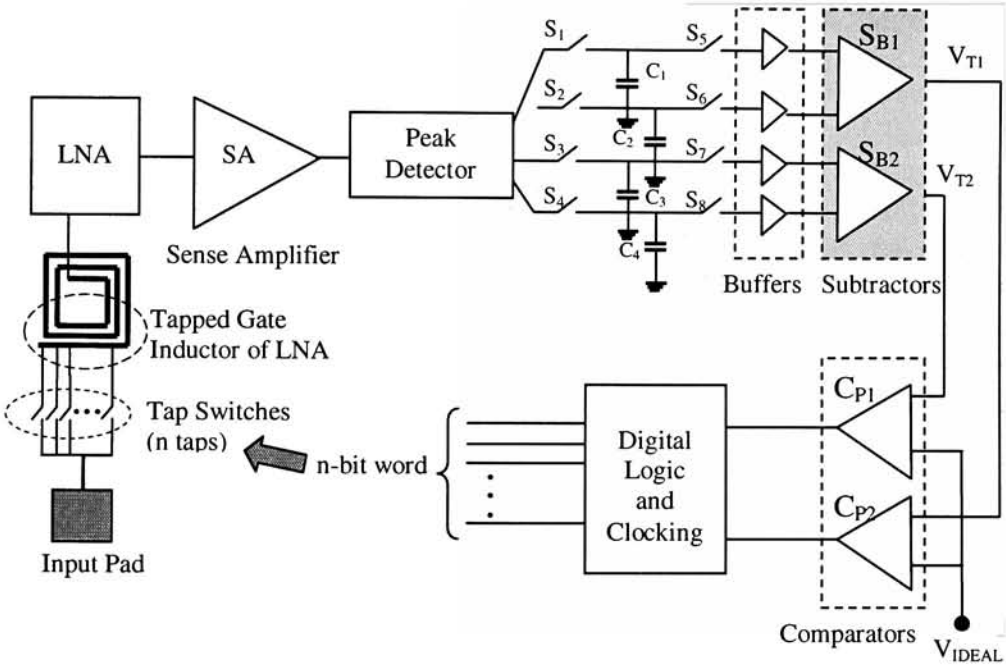


Figure 7.6 Circuit Architecture for self-calibration of LNA input match [36]

Step1: Having chosen the two tones (tone1 and tone2) to be used for the input signals, the switch connecting the first tap of L_G is closed, and a test signal with a frequency of tone1 is applied to the input of the LNA.

Step 2: The resultant output of the Peak Detector (PD) is stored in capacitor C_1 through switch S_1. S_1 is now turned off.

Step 3: Repeat step 1 for tone2, and store the resultant output in capacitor C_2. The switch connecting the first tap of the inductor is now turned off. Since the capacitors have no discharge path, their leakage is minimal and can be reduced to negligible values by choosing appropriate capacitances.

Step 4: The second tap of L_G is now closed (changing the value of L_G and hence moving the input match) and the above process is repeated, storing the PD outputs in different capacitors (C_3 and C_4). At this stage of the process, we have stored the output of the sensor chain for two taps of L_G.

Step 5: Switches S_5 through S_8 are turned on simultaneously, connecting the capacitors to the buffers. For both taps of L_G, the tonal difference amplitudes are calculated by means of two subtractors (V_{T1} and V_{T2}).

Step 6: Now V_{T1} and V_{T2} are compared individually with V_{IDEAL}, where V_{IDEAL} is the voltage difference of the two tones for the desired input match.

Step 7: If V_{T1} is closer to V_{IDEAL} than V_{T2}, the first tap of L_G is connected to the input pad, and self-calibration process is complete. If V_{T2} is closer to V_{IDEAL}, then steps 1 to 6 are repeated, this time for the second and third taps of L_G instead of the first and second taps.

Step 8: The self-calibration will be complete when $V_{T(i)}$ will be closer to V_{IDEAL} than $V_{T(i+1)}$ (this is true since the amplitude of the sensed voltage is monotonic as the input

match frequency is varied). If this condition never occurs, then the last tap of L_G is chosen since it will provide an input match closest to the desired frequency.

The decision-making circuitry includes basic digital logic and a clocking scheme. It is seen that this algorithm follows the linear-search model. Although not maximally efficient in terms of the time taken, this methodology requires minimal overhead circuitry, has no DSP cores or processor requirements, does not require A-D conversion or analog memory cells and consumes little power. The entire time taken for the self-calibration depends on the number of taps in L_G; we show in this work that each tap requires about 3 μs processing time (see Figure 9.10 in Chapter 9). This compares very favorably to times taken by current commercial test schemes [18], wherein the testing period itself is in the order of hundreds of milliseconds.

The algorithms for other specifications are very similar, and require the same circuit blocks. Linearity, for example, requires four voltages (Slope1 and Slope 2 in Chapter 6, Section 6.2) to be stored, their difference computed and compared for a finite difference. The value of this difference triggers the digital logic to create a digital word that changes the bias resistance of the LNA. The same circuitry of Figure 7.6 is re-used for other specifications (circuit details and schematic are discussed in the next Chapter).

7.3 INTER-DEPENDENCIES & OVERHEADS

The overheads of the techniques include a minor increase in Noise Figure (0.22 dB) due to the insertion loss of switches used in the tapped coil, and increase in power consumption due to the current-splitting transconductance array used for gain calibration.

The actual percentage increase in power gain depends on the size of the additional fingers used. For this work, the increase in current was about 10 %.

The self-calibration of each specification will serve to optimize the others, as long as the order of calibration is followed. An improved input and output-match will optimize the gain specification as well, and hence gain calibration must be executed only after both input and output calibration has been performed. The only inter-dependence involved is that of IIP3 and gain, since both are affected by transconductance changes. However, improving either of the two specifications using the techniques mentioned above positively impacts the other. The following order of self-calibration cycles must be followed. Perform input-match and output-match calibration, followed by gain calibration. IIP3 is calibrated last, and if the bias current needs to be reduced (IIP3 is higher than required), no action is taken (since gain can marginally decrease with reduction in bias current). If IIP3 calibration requires increase in bias current, then perform the optimization. This increase in current will only (marginally) enhance the gain. This work uses a scheme where the IIP3 is made adaptive over a 1.1 dBm range. The variations in gain for the bias current changes involved (for 1.1 dBm change in IIP3) is a maximum of 0.15 dB.

It must be reiterated that Linearity is made variable within a window of values (1.1 dBm in this work). The larger the window, the higher the potential power dissipation of the circuit is (and higher will be the increase in gain when IIP3 is improved). This small window is practically acceptable, since the sensitivity of IIP3 on bias (Chapter 3) is much higher compared to other components (only L_S is in the same order of magnitude).

Thus, most variations/faults in those components can be accounted for, as far as IIP3 is concerned, with minor increase in bias current.

Chapter 8. CIRCUIT IMPLEMENTATION

The fault-tolerance methodology has been applied to a 1.9 GHz CMOS Single-ended source degenerated narrow-band cascode LNA. This chapter discusses the implementation of the LNA and the associated processing circuitry. All circuitry has been designed in the IBM 6 Metal layer 0.25 μm RF process (CMOS6RF) with a 2.5 V power supply.

8.1 LNA

The 1.9 GHz LNA schematic designed to demonstrate fault-tolerance is shown in Figure 8.1. For this work, to demonstrate the proof of concept, a digital word of 4-bits has been used, with 4 incremental steps available in each of the four specifications. The number and spacing of these increments is flexible based on the application.

With the nominal values for these increments (half-way between minimum and maximum), the LNA was designed using standard design [11] procedures. The gate inductor was simulated using ASITIC [20] to determine the parasitic inductances and capacitances associated with the structure and the switches. The coil is laid-out, along with the interconnects as shown in Figure 8.2. The switches are implemented using NMOS transistors. This structure is simulated in ASITIC and the PI model obtained as shown in Figure 8.3. This PI model is then simulated in Cadence®, along with the LNA schematic to ascertain the LNA performance. The process is repeated iteratively until the LNA performance meets the application requirements. The design in this work used NMOS switches sized at 68 μm/0.24 μm. The size is a trade-off between

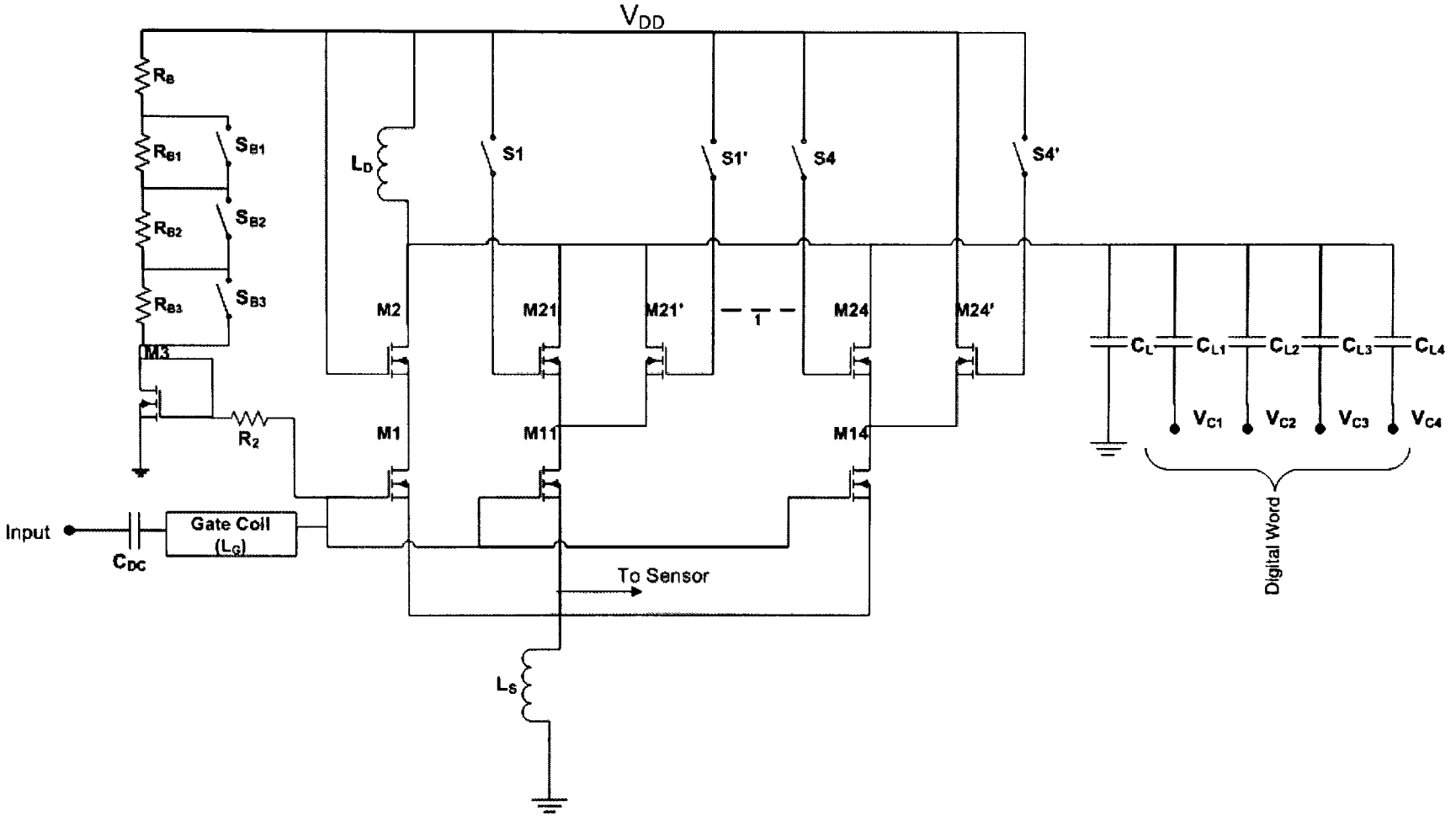


Figure 8.1 Schematic of Fault-tolerant LNA. The gate coil is shown in Figure 8.2

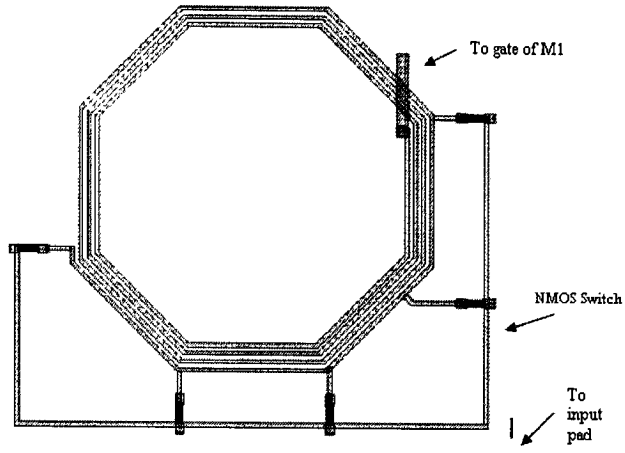


Figure 8.2 The gate inductor structure. The dimensions are: radius = 220 μm, width of metal = 5μm, spacing = 5 μm. It was created on the topmost (Analog metal) layer [36] [38].

Component	Value
M1, M2	300 μm/0.24μm
M3	16.2 μm/0.24 μm
M11-M14	12 μm/0.24 μm
M21-M24	12 μm/0.24 μm
M21'-M24'	12 μm/0.24 μm
S1-S4	NMOS switches, 2 μm/0.24 μm
S_{B1}-S_{B3}	17 μm/0.24 μm
R_{B1}-R_{B3}	200 K Ω
R_2	10 K Ω
R_B	3.3 K Ω
C_{DC}	30 pF
L_S	0.6 nH
L_D	2.5 nH
C_L	1.4 pF
C_{L1}-C_{L4}	MOS Varactors, 0.2 pF – 0.5 pF
V_{DD}	2.5 V

Table 8.1 Design values for components in Figure 8.1

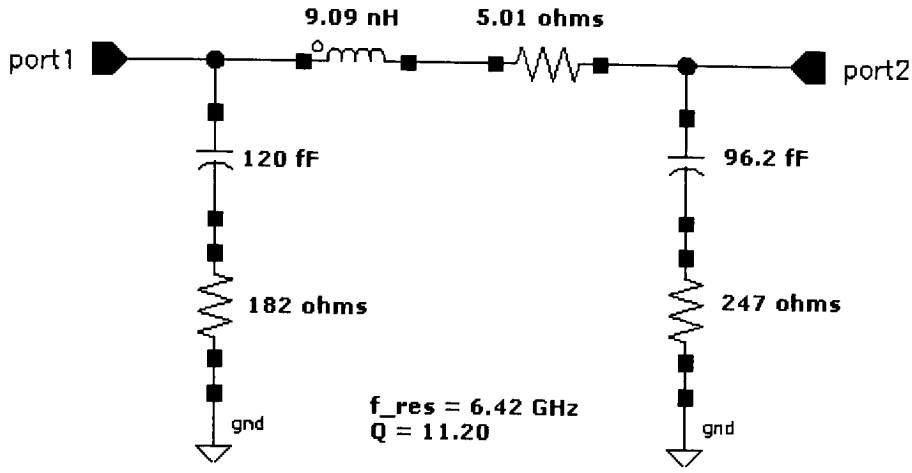


Figure 8.3 PI model of the gate-coil from ASITIC

the channel resistance and transistor capacitance. With higher sizes, the resistance decreases (and hence the Noise Figure degradation), but the increase in parasitic capacitances decreases the self-resonant frequency and Q-factor of the coil. As seen in Fiure 8.3, this choice of size resulted in a Q-factor of 11.20, with a self-resonant frequency of 6.42 GHz. The experimental results match very closely with simulated predictions (Chapter 9), and thus validate this approach. The coil provides inductor values between 7.4 nH and 11nH.

The nominal design uses a fixed load capacitance of 2.8 pF. To make the output-match adaptive, a fixed capacitance of 1.4 pF was retained (C_L in Figure 8.1), and four MOS varactors (range 0.2 pF to 0.55 pF each) were used in a digital mode (operating only at the two extreme ends, C_{L1} –C_{L4} in Figure 8.1). This provided a variable capacitance of 1.4 pF. The sensitivity analysis of Chapter 3 indicated that the sensitivity of output-match frequency to load capacitance was 0.34 GHz per pF (table 3.5), and 1.4 pF provides 0.5 GHz variability in S_{22} frequency.

The power gain was made variable over a range of 1.4 dB in increments of 0.45 dB (corresponding voltage gain is 0.8). The transconductance-splitting transistors (M_{11}-M_{14} and M_{21}-M_{24} in Figure 8.1) were sized at 12 μm/0.24 μm in this design (Table 3.3 in Chapter 3 shows the Sensitivity of Gain to bias current as 0.41 per mA. These sizes route 2 mA of bias current through the additional branches, resulting in a total gain variation of 0.82).

The switches in R_{BIAS} are not in the signal path, and since they only carry DC current, they do not contribute to the noise of the system (the same argument holds true for the switches used in gain calibration). The bias resistor was made variable over a range of 600 Ω (R_{B1}-R_{B3} in Figure 8.1), providing for IIP3 adaptability over a range of 1 dBm (sensitivity analysis of IIP3 in Table 3.7 indicates 1.76 dBm per KΩ of bias resistance, hence 600 Ω translates to 1 dBm). It is seen that mechanisms for dynamic modification of the LNA's design parameters are achieved without significant topological revision or performance degradation. Table 8.1 lists all design values for the schematic of Figure 8.1, and Table 8.2 summarizes the adaptability incorporated in the LNA design used in this work.

SPECIFICATION	ADAPTABILITY
S_{11}	0.5 GHz
S_{21}	1.4 dB
S_{22}	0.5 GHz
IIP3	1 dBm
S_{12}	Not needed
NF	-Nil-

Table 8.2 Adaptability of the LNA

8.2 SENSOR CHAIN

The voltage across the sensing elements (and at the output node) is fed to a source follower. The source follower serves to isolate the LNA (and mixer) from any processing circuitry that might follow and also provides a relatively broad band interface to transfer the sensed signal across the sensing resistor to the processing circuitry. The size of the source follower transistor is kept small so that it presents a negligible capacitance (less than 200 fF for 1.9 GHz operating frequency) at the source node of the LNA. This capacitance is equivalent to adding additional interconnect related parasitics at the source node of the LNA, and it does not affect the LNA performance[28].

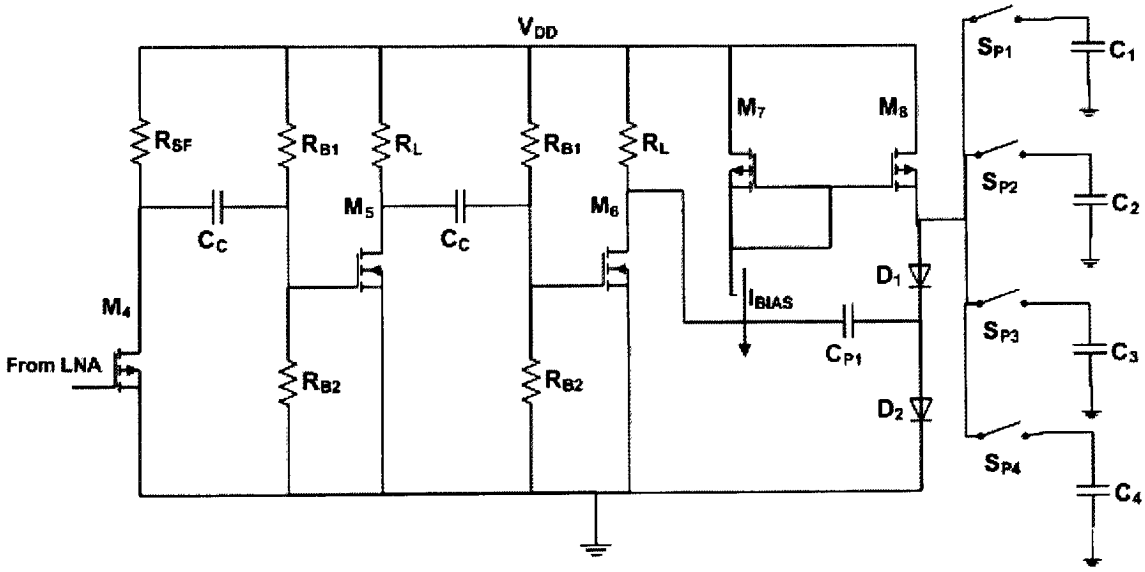


Figure 8.4 Sensor Chain: Sense Amplifier & Peak Detector [36]

The magnitudes of voltage variations across the source degenerative coil (L_S) of the LNA and mixer (corresponding to changes in the impedance match) are relatively small (in the order of a few tens of millivolts). However, since the amplitude of the input

[28] It reduces the self-resonant frequency of the source coil by 10% to 9 GHz. This value has no impact on performance of a 1.9 GHz LNA.

test signal can be considerably higher than typical LNA inputs, the resultant gain requirements of the amplifier are very moderate. In addition to this, due to the absence of any restrictions on Noise Figure of the sensed signal, simple common source amplifiers with resistive loads can be used to achieve the required amplification. Push-pull amplifiers can provide very high gain, but need extensive bias stabilization for a stable operation. Two cascaded common source stages have been used to construct the amplifier because it is possible to AC couple the sensed signal from one stage to another, while providing independent DC biases to each stage. No feedback has been incorporated into the amplifier due to the inherent robustness of the two-tonal approach. As will be shown in succeeding sections, as long as the amplifier can provide a minimal gain at all process, supply and temperature corners, variations in the numerical value of the gain will not affect the successful correction of the RF circuit. The amplifier and the source follower form the sense amplifier (SA, Figure 7.6). The schematic of the sensor chain is shown in Figure 8.4.

A standard half-wave diode (inverting) voltage doubler has been designed to peak detect the sense amplifier's output. Since the P.D output has to be stored on four different capacitors, the output capacitor is replicated four times (C_1 –C_4) and they are connected to node N_2 (Figure 8.4) through transmission gates (S_1-S_4). This eliminates the need for external memory capacitors. The sensor at the output node of the LNA does not have any amplifying circuitry – it is a combination of source follower and peak detector.

The outputs of the peak detector are fed to the two subtractors (S_{B1} and S_{B2}, Figure 7.6) through unity gain buffers. Due to the presence of the buffers, the peak detector capacitors have no discharge path thereby retaining all their charge except

leakage. The buffers, subtractors and comparators have all been designed using standard folded cascode op-amp and comparator techniques.

Component	Value
M_4	8.34 μm/0.24μm
R_{SF}	2000 Ω
R_{B1}	6.86 K Ω
R_{B2}	3.2 K Ω
M_5, M_6	51.6 μm/0.24 μm
R_L	1 K Ω
M_7, M_8	4 μm/0.24 μm
D_1, D_2	25 μm/0.24 μm
I_{BIAS}	4 μA
S_{P1}-S_{P4}	Transmission gates, with W/L of 1.32μm/0.24μm For both PMOS and NMOS
C_C	1 pF
C_1-C_4	3 pF

Table 8.3 Design values for the components of Figure 8.4

The timing for the entire process including the timing for the switches is carried out in integral multiples of a time unit provided by a single low frequency clock which is generated off-chip. This eliminates any dependence on absolute delays and makes the timing scheme process independent. The timing for various switches is derived by decoding the appropriate states of a 32-bit synchronous counter and latching the resultant signal to eliminate glitches. The rest of the digital circuitry constitutes basic gating and logic that creates a digital word. All the digital circuits used in the current work have been constructed using the standard cell library for the IBM 0.25 μm process.

Chapter 9. RESULTS

The entire sensing & post-processing circuitry, along with a cascode LNA (with provision for self-calibrating the input-match) was fabricated in IBM 6RF CMOS 0.25 μm process. This section presents simulation and experimental results for the circuitry [35] [36] [39]. The tapped coil structure and the self-calibration circuitry have been highlighted in the chip micrograph (Figure 9.1). The area overhead of the self-calibration circuitry is under 10% of the area of the single-ended cascode LNA. It should however be mentioned that the same sense amplifier chain can be used for calibrating other circuits in the front-end. The power overheads are very minimal since all the circuitry except for a few logic gates will be powered up only for the self-correction process, which takes less than 200 μs.

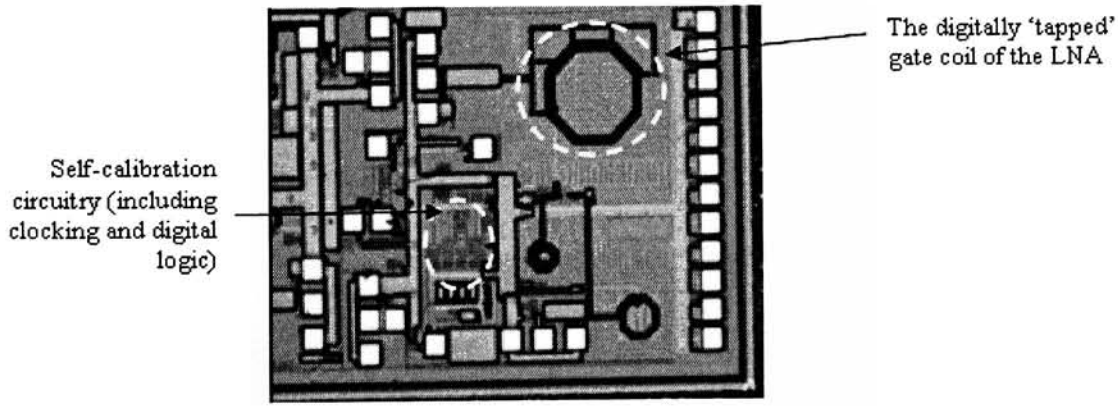


Figure 9.1 Chip micrograph of the system [36] [38]

9.1 MEASUREMENT SETUP

All the testing was carried out using a Cascade RF -1 probe station, in conjunction with an Agilent E8362A network analyzer, an HP 4405B spectrum analyzer and an

Agilent 8648D RF signal generator. Figure 9.2 shows a block diagram of the measurement setup used.

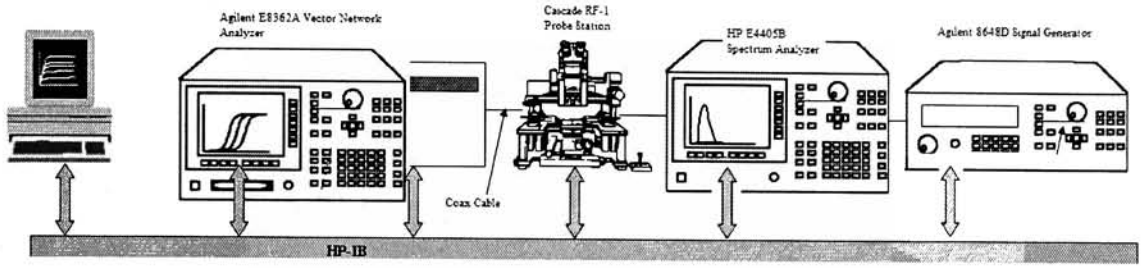


Figure 9.2 Block Diagram of Measurement Setup [42] [29]

9.2 SENSOR CIRCUITRY

For the 1.9 GHz LNA, the two tones for the input stimuli were chosen to be 1.6 GHz and 2.2 GHz (optimal choice of two tones, as discussed in Chapter 6). The sensor gain target was 8 (minimum), and this was ensured by designing for a gain of 8.5 for the weakest corner. The input stimuli for gain had a frequency of 1.9 GHz, the operating frequency of the LNA.

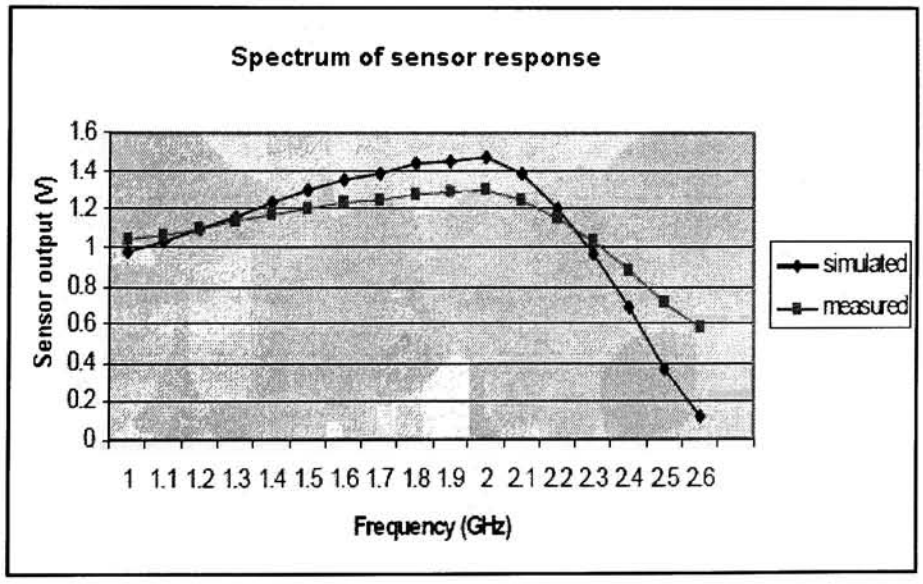


Figure 9.3 Output Spectrum of LNA with sensor – Simulated vs. Experimental [36]

The spectrum of the sense amplifier, when interfaced with the LNA is shown in Figure 9.3 (input applied to LNA). The measured data compares very well with simulated results. While the frequency response from measurements matches very closely with simulations, there is a difference between the magnitudes of the response, due to process variations. The maximum output of the sense amplifier has decreased slightly in the measured data in comparison with simulation. The measured value deviates by 6% from the simulated value, an acceptable change attributed to process variations.

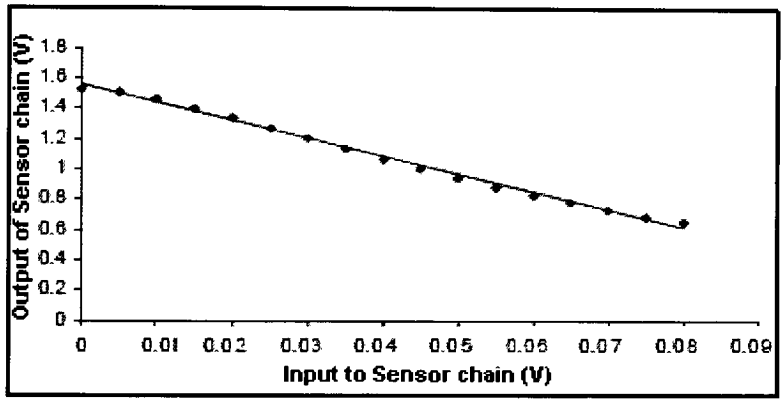


Figure 9.4 Measured transfer curve of the sensor chain [35]

The input stimuli (during correction) to the LNA-sensor chain network is a RF signal, as is the case during normal LNA operation. The output of the sensor chain is the peak-detected DC voltage that is routed appropriately and stored on capacitors. These capacitors also have a discharge path that is activated at the end of every cycle to eliminate any residual charge on them. Figure 9.4 shows the measured amplitude response of the Sensor chain when interfaced with the LNA, when the input stimulus was swept from 0 to 80 mV at 1.9 GHz. It is verified that the response is linear over the full

range of input values, although the actual gain of the sensor is lower than the simulated value (the measured gain was 9.7 as against the designed value of 10.0). It is, however, adequate to ensure successful operation, as is shown by the subsequent sections.

9.3 INPUT-MATCH CORRECTION

Any variation or fault in the gate and source inductors, transistor dimensions, or the gate-source capacitance will impact the input-match of the LNA. In addition, ESD parasitics, external coupling, and package parasitics significantly influence the input-match of a LNA. This section discusses results that show input-match correction independent of the fault or variation affecting the circuit. Figure 9.5 shows the measured S-parameters (S_{11}, S_{22} and S_{21}) of the LNA for the nominal tap of gate coil. At this tap, the measured S_{11} was -22.94 dB at 1.74 GHz. The Noise Figure (NF) overhead due to the presence of a switch (that taps the gate coil) in the signal path was 0.22 dB.

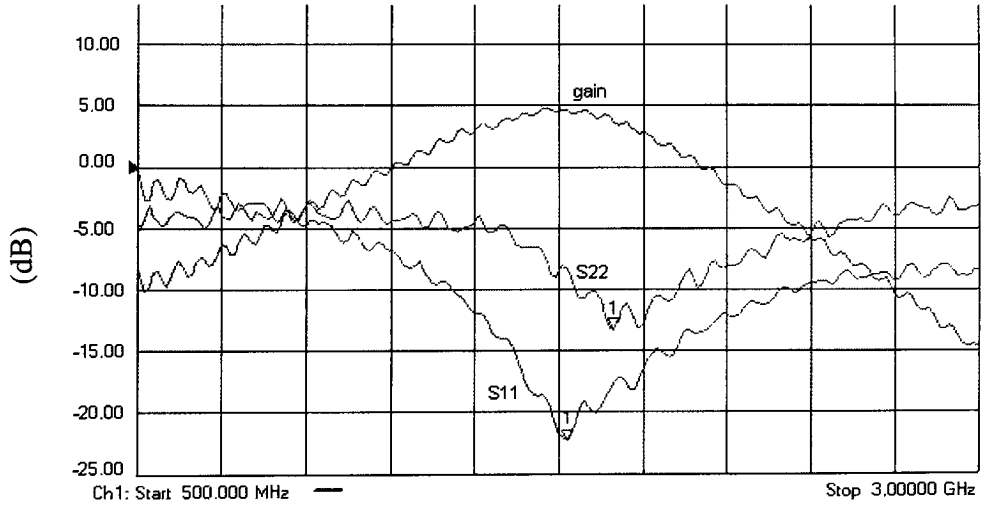


Figure 9.5 Measured LNA S-parameters for the first tap. S_{11} frequency was 1.74 GHz, and value was -22.94 dB. [35]

Tap no.	Inductance value	Simulated S_{11} freq	Digital word input to coil	Measured S_{11} freq
1	7.4 nH	1.7 GHz	00	1.7375 GHz
2	9 nH	1.91 GHz	01	1.925 GHz
3	10 nH	2.0 GHz	10	2.03 GHz
4	11 nH	2.11 GHz	11	2.125 GHz

Table 9.1. Tapped coil performance in simulation and measurement. Excellent agreement is observed.

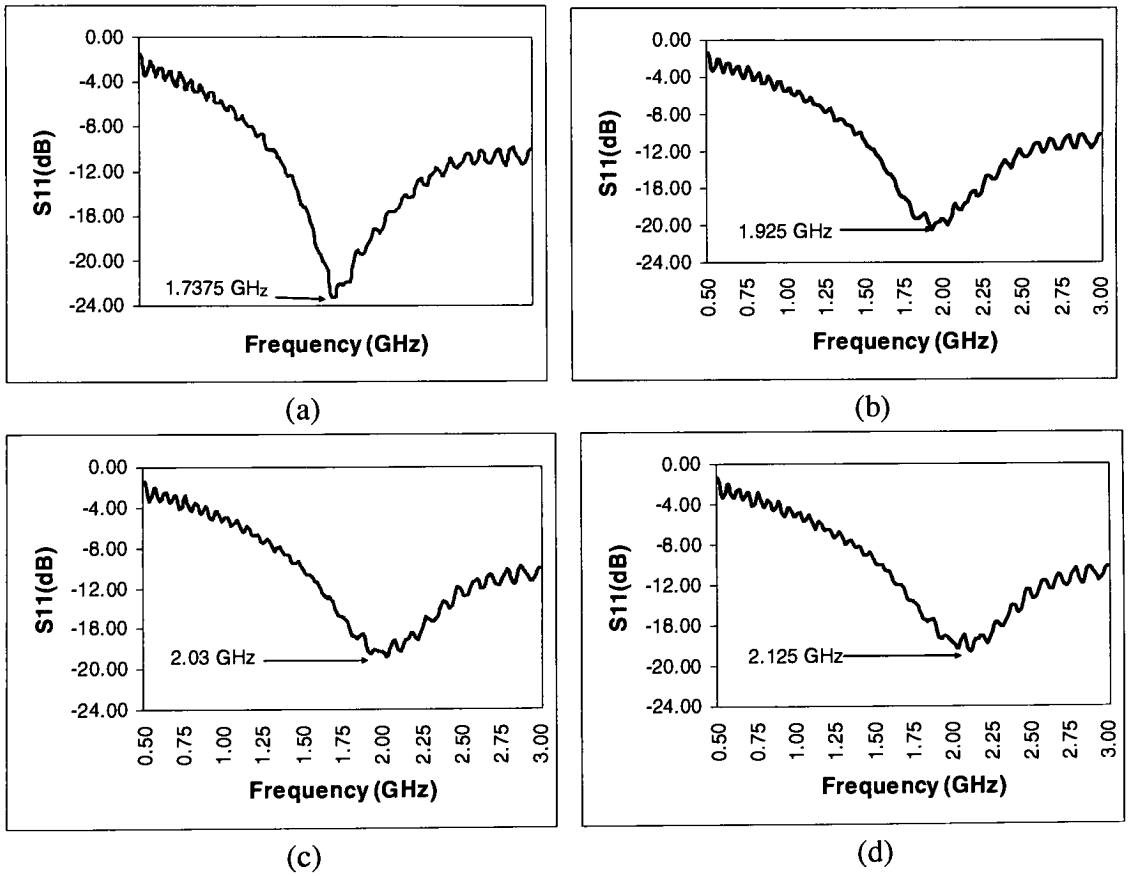


Figure 9.6 Measured S_{11} results for all 4 taps of the gate coil. S_{11} magnitude stayed below -18 dB for all taps, and the different match frequencies were: 1.737 GHz, 1.925 GHz, 2.03 GHz and 2.125 GHz. [35] [38]

Table 9.1 compares the behavior of the tapped coil as modeled in ASITIC with measurement results. Excellent agreement is seen between the frequencies of S_{11} in simulation and measurement. Good match between simulation and measured data was observed with S_{22} (1.9 GHz and 1.91 GHz respectively) and Gain (5.3 dB and 4.95 dB respectively) as well. Figure 9.6 shows the different measured S_{11} curves for all 4 taps. The different frequencies of match were 1.737 GHz, 1.925 GHz, 2.03 GHz and 2.125 GHz, and the magnitude stayed below -18 dB in all cases[29].

Figure 9.7 shows the measured output of the sensor chain for the two tones, for different input-match frequencies of the LNA. As the S_{11} frequency increases, it is seen that the output for the first tone increases, while that for the second decreases, as expected. Figure 9.8 plots the output of the subtractor (difference of the two tones taken at the output of the subtractor, i.e. difference of the two curves in Figure 9.7) for different S_{11} frequencies, and compares it with simulation values.

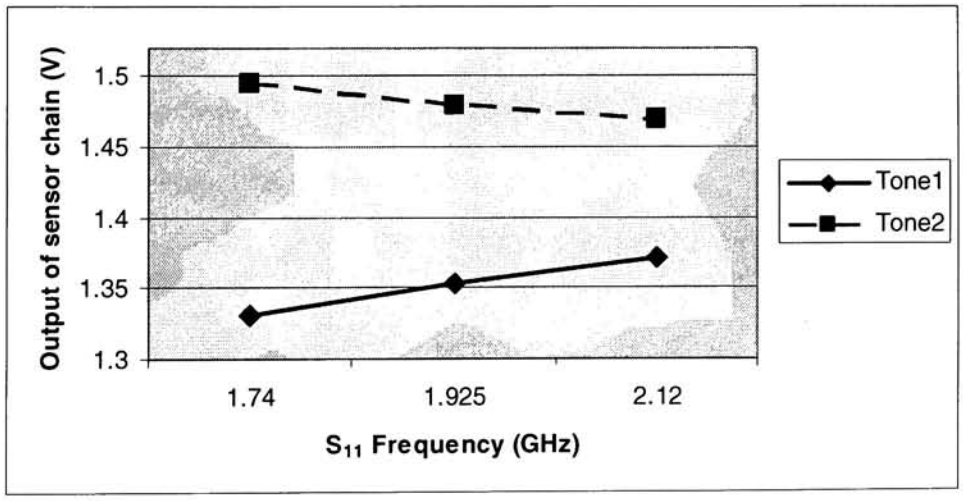


Figure 9.7 Sensor chain output (measured) for the two input tones for different S_{11} frequencies

[29] Most LNA applications require S_{11} to be less than 12-15 dB.

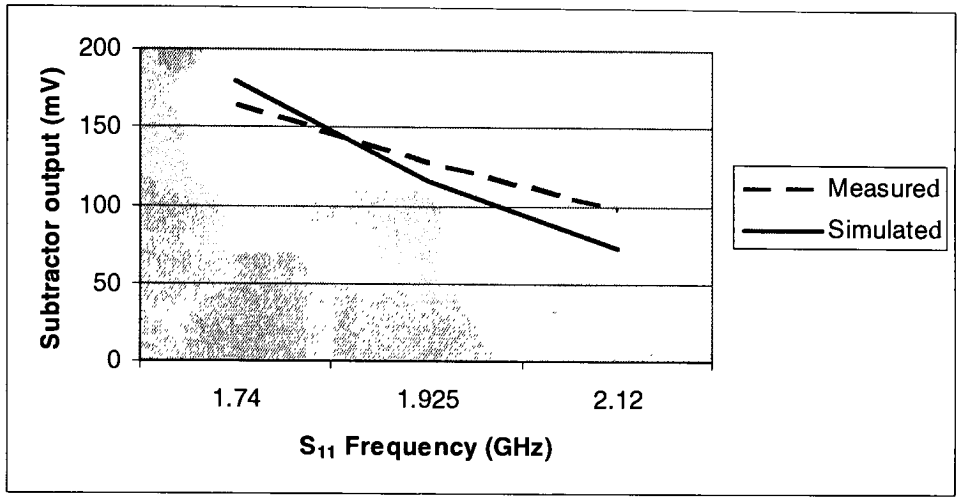


Figure 9.8 Output of subtractor (measured and simulated) for different S_{11} frequencies [35]

It is confirmed that the sensor response accurately (up to 98%, as discussed in Section 9.7.1) captures and quantifies variations in S_{11} frequency. As predicted by the experimental results of the (stand-alone, Figure 9.3) sensor chain, there is a difference in the gain of the sensor circuitry due to variations in process. This variation, however, does not compromise the integrity of the sensing technique due to the differential nature of sensing. Thus it is possible to accurately quantify the change in S_{11} frequency using the DC voltage at the output of the sensor chain.

The self-correction loop was validated by manually setting the inductor tap for an S_{11} frequency of 2.125 GHz, and at the end of the correction cycle, the LNA corrected S_{11} to 1.925 GHz, against the desired value of 1.9 GHz. (Figure 9.9). The entire correction cycle can[30] be completed in 30 μs.

[30] The cycle takes 30 μs when the clock speed is 2 MHz. Due to measurement setup and equipment limitations, the clock speed was reduced to one-fifth of 200 MHz for the data collected.

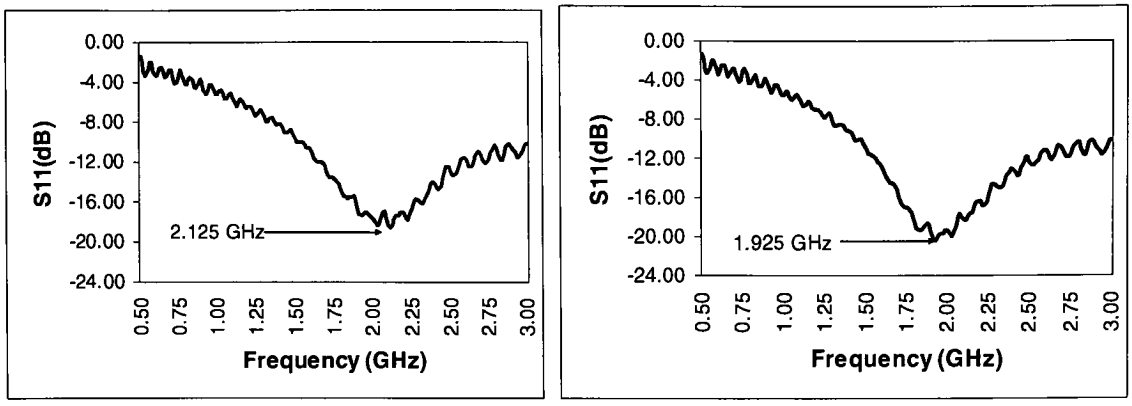


Figure 9.9 S_{11} frequency (measured) was corrected from 2.125GHz (a), (before the self-correction cycle) to 1.925 GHz (b), by the self-correction loop.

Figure 9.10 shows the self-calibration loop waveforms in simulation. The entire process halts when the optimal match has been decided upon (this particular case runs for three taps), and the power to the sensor circuitry is cut-off. All component nomenclature refers to Figure 7.6 in Chapter 7. Figure 9.10(a) shows the voltage sensed across source inductor of LNA (a gap of 3 μs is provided after each cycle to allow the analog processing circuitry, such as the subtractors and comparators, to settle to its final value). Figure 9.10 (b)(c)(d) & (e) show the peak-detected value held by capacitors C_1-C_4 and their discharge (controlled by the discharge pulse in Figure 9.10 (h)) to 0 V after every cycle, to ensure that every new cycle starts with zero charge on the capacitors. Figure 9.10 (f) & (g) show voltages V_{T1} and V_{T2}, which are the differences between voltages across C_1-C_2 (difference in the two tones for a tap of the gate-coil) and C_3-C_4 (difference in the two tones for the subsequent tap) respectively. Figure 9.10(i) shows the power-control to the calibration circuitry. These circuits are powered-down once the optimal match has been set.

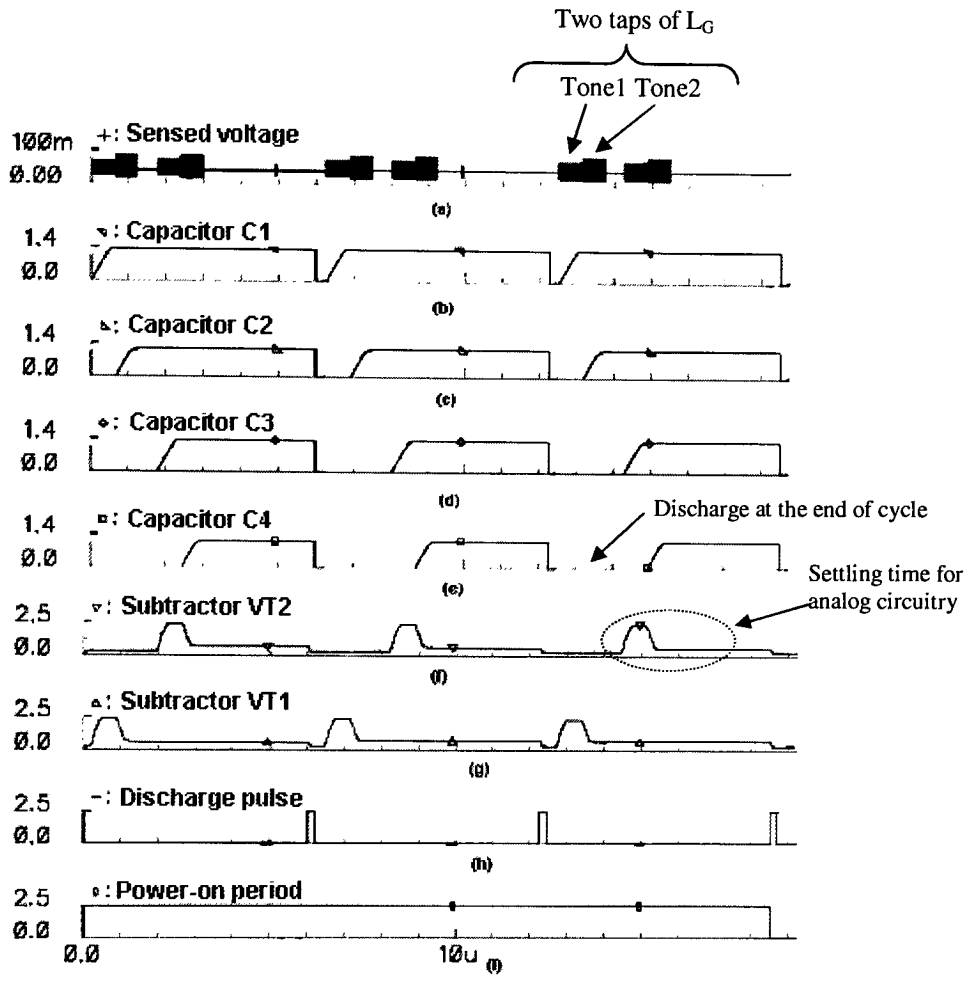


Figure 9.10 Output voltages of various stages over entire correction process in simulation. [36]

Figure 9.11 illustrates the waveforms for the case where the gate-source capacitance is reduced by 15%. The waveform behavior follows the same pattern as in Figure 9.10. Since in this case the reduction of C_{GS} shifted S_{11} to a higher frequency, the effective gate inductance was reduced, and the correction process was completed in 12.2 μs. The input match frequency changes to 2.04 GHz from 1.9 GHz due to the reduction in gate-source capacitance. At the end of the self-correction process, it is re-aligned at 1.925 GHz.

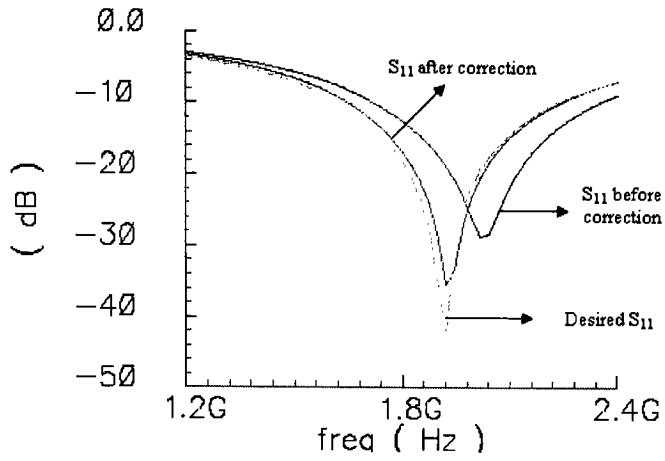


Figure 9.11 Self-correction of input-match (simulation) for a 15% variation in C_{GS} [36]

9.4 S_{22} AND GAIN CORRECTION

The output match can change due to variations or faults in the load inductor, load capacitance, or gate-drain capacitance of the cascode transistor, in addition to interconnect related parasitics. The varactor bank has a capacitance range of 2.5 (the maximum capacitance achievable is 2.5 times the minimum capacitance).

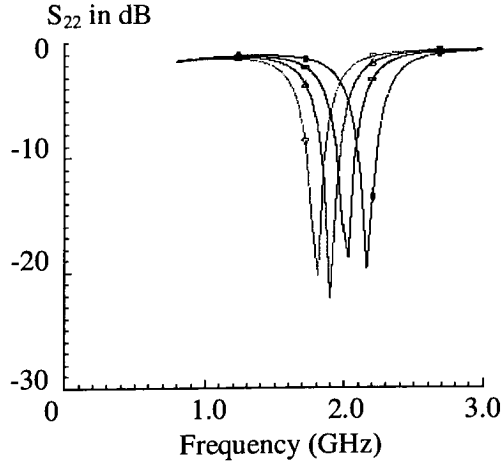


Figure 9.12 S_{22} frequency varies as the digital word to the varactor bank is varied in simulation. The same two-tonal approach used for input match can sense and correct the output match too. [35]

Figure 9.12(a) shows the variation in S_{22} as the varactor voltages are switched by the digital word input. The same two-tonal approach, sensor and post-processing circuitry are re-used for S_{22} self-correction.

Figure 9.13(a) shows the various gain curves when the drain inductance is varied to simulate a soft-fault. The gain curves change since the output match frequency and frequency of maximum gain follow each other. Consequently, faults of this kind impact both output match and gain. Figure 9.13(b) shows the difference in the two-tones as the gain frequency (and S_{22}) varies. This voltage is used to modify the digital word feeding the varactor bank, thus restoring the desired match.

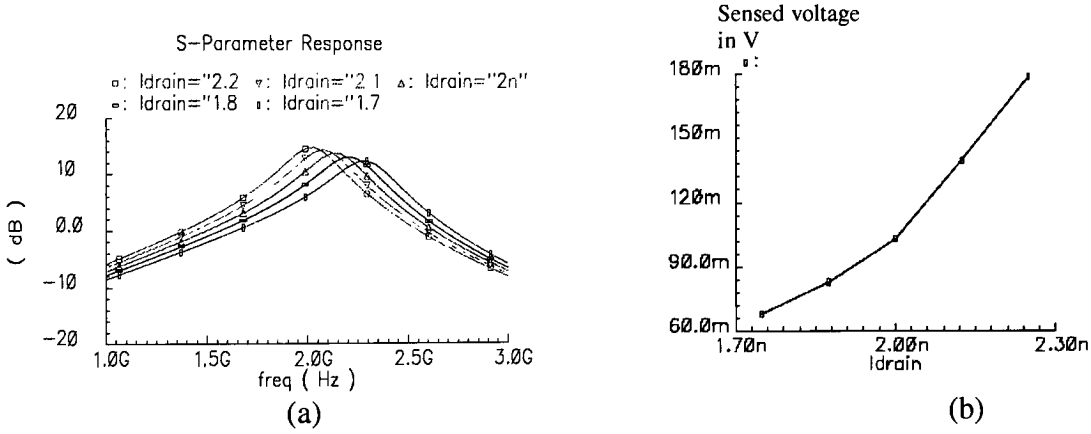


Figure 9.13 Variation in output resonant frequency with 20% variation in drain inductance (in simulation) L_D (b) Difference in the two-tones for the S_{22} variations in (a) [35]

Figure 9.14 illustrates the self-correction process. A 7% variation in the load coil (possible by a soft fault or process variations) was corrected for by changing the digital word feeding the varactor bank, realigning the output match of the LNA.

There can exist faults that modify only the magnitude of gain of the LNA, and these faults are corrected by introducing additional transconductance in the LNA. The current-splitting transconductance array described in Chapter 8(Figure 8.1, transistors

M_{11}-M_{14} and M_{21}-M_{24}) provides increments of gain based on the number of additional fingers activated. Figure 9.15 shows these gain increments.

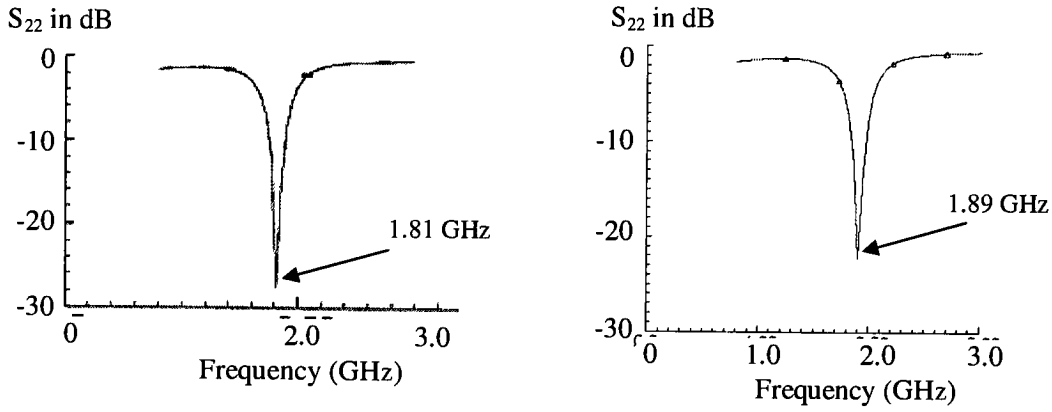


Figure 9.14 A 7% change in the drain inductance (in simulation) shifts the output match from 1.9 GHz to 1.81 GHz. At the end of the self-correction process, the match aligned itself back at 1.89 GHz. [35]

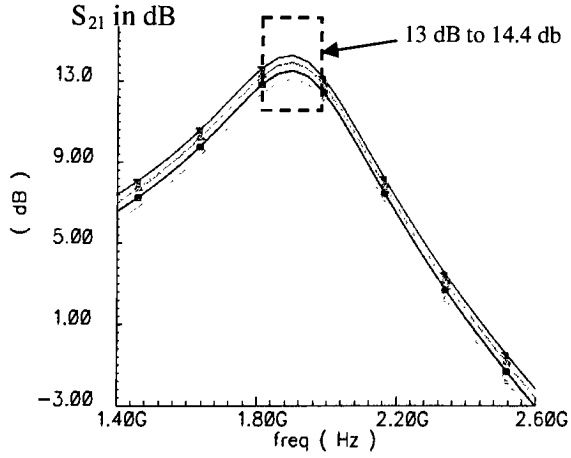


Figure 9.15 Different gain curves as the digital word to the cascode array is changed, in simulation. The gain varies from 13 dB to 14.4 dB [35]

The gain can be varied from 13 dB to 14.4 dB. For a class of faults that degrade the gain magnitude (for example, a small increase in the resistive loss of the load coil or degradation in Q), additional fingers can be activated, restoring the gain back to its desired value.

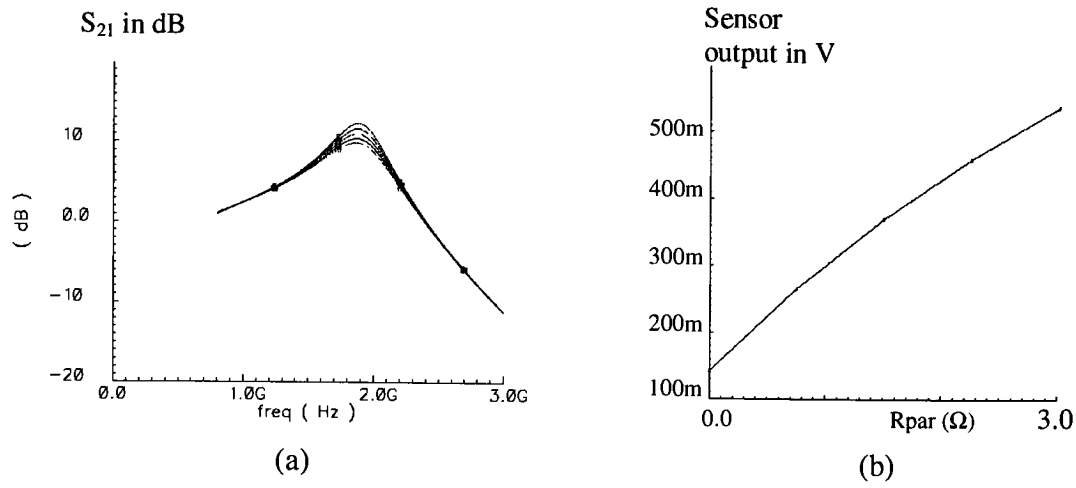


Figure 9.16 Variation in gain S_{21} with variation in parasitic resistance of drain inductance (in simulation) L_D (b) Output of sensor for input stimuli at 1.9 GHz [35]

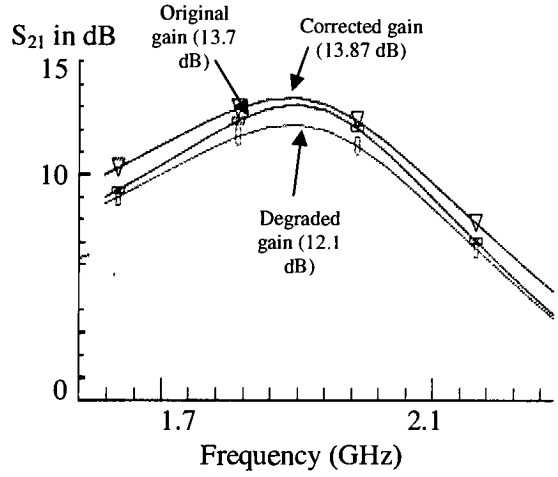
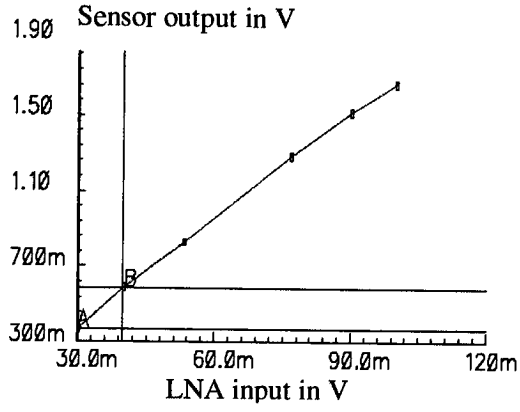


Figure 9.17 Gain self-correction (simulation) [35]

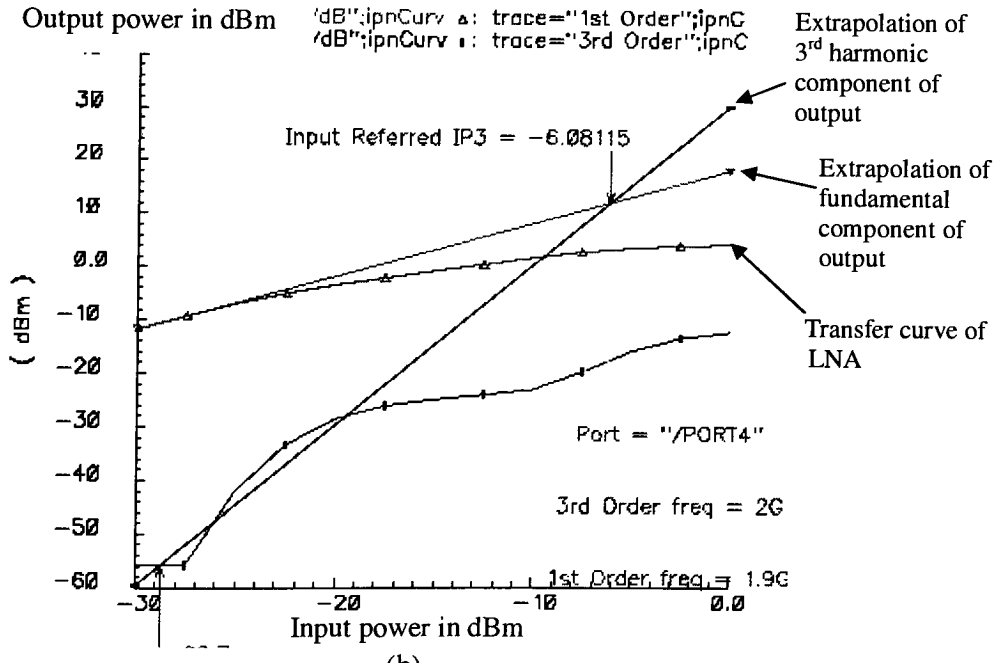
Figure 9.16(a) shows the decrease in gain as the parasitic resistance of the load coil is increased, and Figure 9.16(b) shows the sensor output for the input tone, quantifying gain magnitude. This sensor output is passed through the same post-processing circuitry and it modifies the digital word feeding the array of transistor fingers, thus activating more fingers and restoring gain back to its desired value. This self-correction (for a 1 ohm increase in parasitic resistance of the load coil) is depicted in Figure 9.17.

9.5 LINEARITY

Once the gain calibration is completed, linearity is optimized using the slope comparison technique developed in this work. The correlation between this technique and IIP3 has already been established (Chapter 6), and this section discusses simulation results.



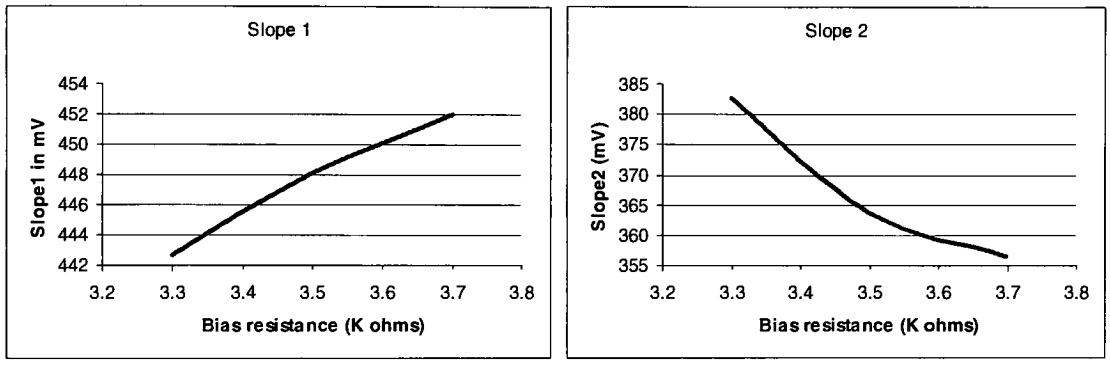
(a)



(b)

Figure 9.18 (a). Transfer curve of sensor at output node (simulation) for input ranging from 30 mV to 100 mV and (b) Nominal IIP3 simulation for the LNA

For a bias resistance variation of 600 ohms (the on-resistance of the MOS switches used in the bias network have been accounted for in designing the bias variations), the bias current varies by 1.4 mA, providing 1 dBm variation in IIP3. Figure 9.18(a) shows the transfer curve of the sensor, Figure 9.18(b) shows the nominal IIP3 simulation curve of the LNA, and Figure 9.19 shows the two slopes calculated for the four input stimuli applied. To compute Slope 1, input stimuli of 20 mV and 40 mV was applied, while stimuli of 80 mV and 100 mV were applied for Slope 2.



(a) (b)

Figure 9.19 (a) Slope 1 (difference in the sensor output for a input stimuli of 20 mV and 40 mV) for different bias currents, and (b) Slope 2 (difference in the sensor output for a input stimuli of 80 mV and 100 mV) for different bias currents (in simulation)

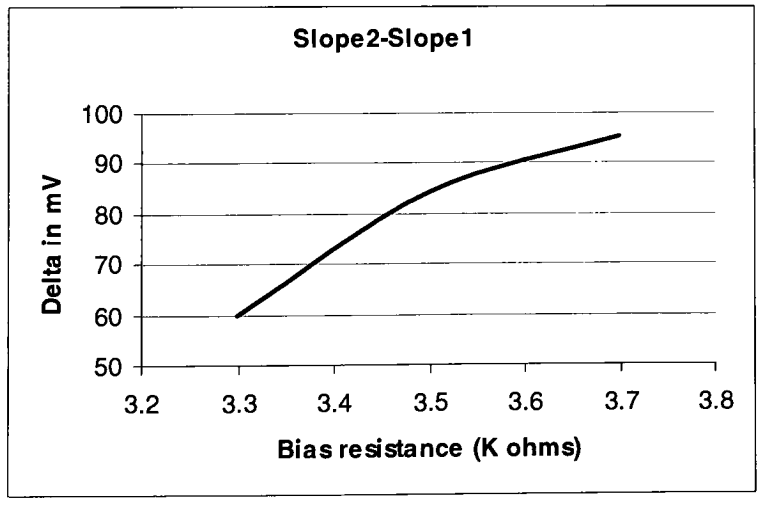


Figure 9.20 Slope1-Slope2 (Delta, in simulation) quantifies the degrading linearity with drop in DC bias current

The curves in the Figures are the peak-detected values of the sensor at the output node of the LNA. Figure 9.20 shows the values of Slope1-Slope2 for different bias currents – as the current increases (R_{BIAS} decreases) and improves linearity, the difference between the slopes drops, quantifying the linearity improvement.

To demonstrate the self-correction process, consider a variation in the bias resistance (5%) of the LNA. Table 9.2 shows the various voltages before and after the self-calibration process, along with the respective IIP3 values. Its value is realigned back to -6.019 dBm. Due to the gain of the subtractors involved, the difference of a few millivolts will be magnified further before the comparator stage. The input stimuli and the subtractor gain can be set appropriately to ensure that the difference is compared to an available reference voltage (or even zero volts).

DESIGN	SLOPE1	SLOPE2	SLOPE1-SLOPE2	IIP3
Nominal LNA	448.14 mV	363.78 mV	84.36 mV	-6.08 dBm
LNA with degraded linearity	451.09 mV	356.22	94.87 mV	-6.47 dBm
LNA after calibration	446.58 mV	358.97 mV	87.61 mV	-6.013 dBm

Table 9.2 Self-calibration of IIP3 in simulation

9.6 MULTIPLE FAULTS

To verify calibration sequencing and the validity of the entire process for multiple faults, the nominal LNA was simultaneously perturbed with:

- Parasitic (or bond-wire) package inductance varied by 1 nH
- 7% variation in drain inductor value

- 1 ohm increase in the parasitic resistance of the drain inductor
- 5% variation in bias resistance of the bias network

At the end of the calibration cycle (the specific sequence followed was S_{11}, S_{22}, gain and Linearity), the specifications had realigned themselves to their nominal (with resolution errors) values. Table 9.3 summarizes the process.

Design	Input match	Output match	Gain	IIP3	Reverse isolation	Noise Figure
Nominal LNA	1.9 GHz, -33.1 dB	1.9 GHz, -27.1 dB	13.7 dB	-6.011 dBm	-41 dB	2.13 dB
LNA with multiple faults	1.82 GHz, -27.4 dB	1.84 GHz, -18.8 dB	12.8 dB	-6.76 dBm	-43 dB	2.15 dB
LNA after calibration	1.894 GHz, -32.2 dB	1.892 GHz, -27.3 dB	13.81 dB	-6.017 dBm	-41 dB	2.12 dB

Table 9.3 Self-calibration of LNA (simulated)

The results of this section prove that the LNA can self-correct its performance specifications for a wide range of variations and faults. The technique is specification-centric, and largely independent of the source of the fault or variation itself. In each of the cases, some uncertainty exists due to the processing circuitry, such as op-amp resolution, charge leakage, DC offsets, etc. However, these offsets are in the order of a few milli-volts, and at worst, may result in the non-detection of very minor performance deviations. These deviations cannot be corrected due to another reason as well, since there will exist a minimum resolution due to the calibration being digital in nature. For example, a IIP3 that has been degraded to -6.017 dBm (from -6.011 dBm) may not be detected by the

sensing circuitry (the difference signals are masked by the offsets, etc.), but such a minor degradation cannot be corrected either, since it falls outside the resolution incorporated for linearity calibration. In essence, the calibration scheme (gain of sense amplifiers, input stimuli, DC offsets of circuitry, etc.) must be designed such that the offsets generated by the calibration circuitry are smaller than the difference signals generated by the smallest performance deviation (resolution) that needs to be corrected.

The methodology presents very low overheads in terms of area, intrusion, and processing. It occupies less than 10% of the LNA area, with a 0.22 dB increase in Noise Figure being the only measurable impact on the circuit. It also achieves processing times of under 200 μs, with no DSP cores or off-chip processing required.

9.7 ADDITIONAL RESULTS

9.7.1 Accuracy of two-tonal approach

Chapter 6 discusses the limitation of the two-tonal approach, and lists possible eventualities where an impedance-match shift might not be detected. With the two tones appropriately chosen, Monte-carlo simulations[31] of both S_{11} and S_{22} were executed. The S_{11} curves are shown in Figure 9.21 and the corresponding sensor outputs (difference of the two tones, output taken at subtractor) for those curves are shown in Figure 9.22. The sensor outputs were compared against the S_{11}/S_{22} plots to ascertain if they had detected (and subsequently corrected) impedance match shifts.

[31] The process parameters varied in this simulation are determined by the IBM PDK provided 'input-file'.

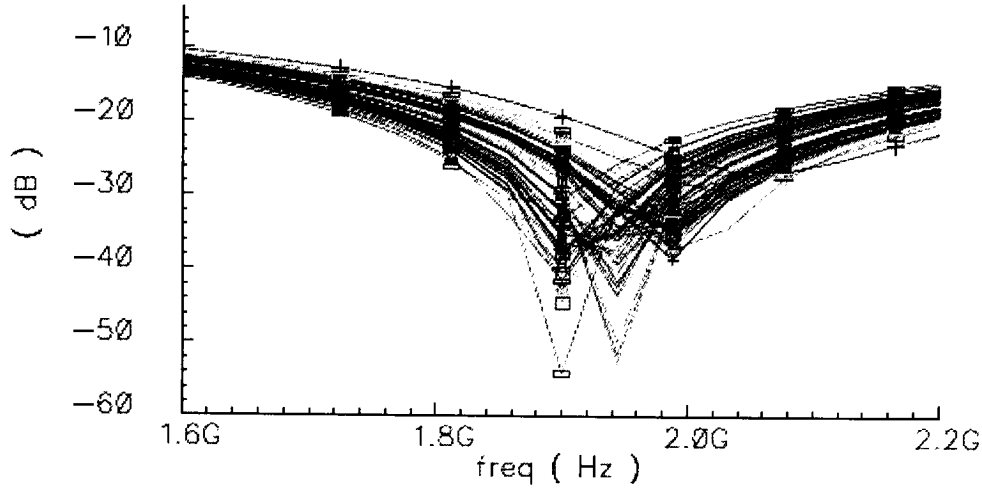


Figure 9.21 S_{11} curves from the 3-sigma Monte-carlo run

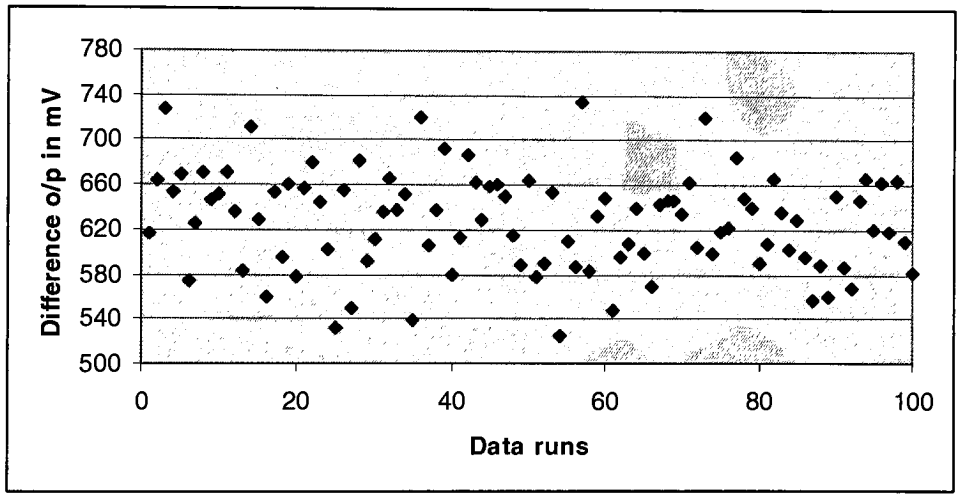


Figure 9.22 Subtractor output for the S_{11} curves of Figure 9.22

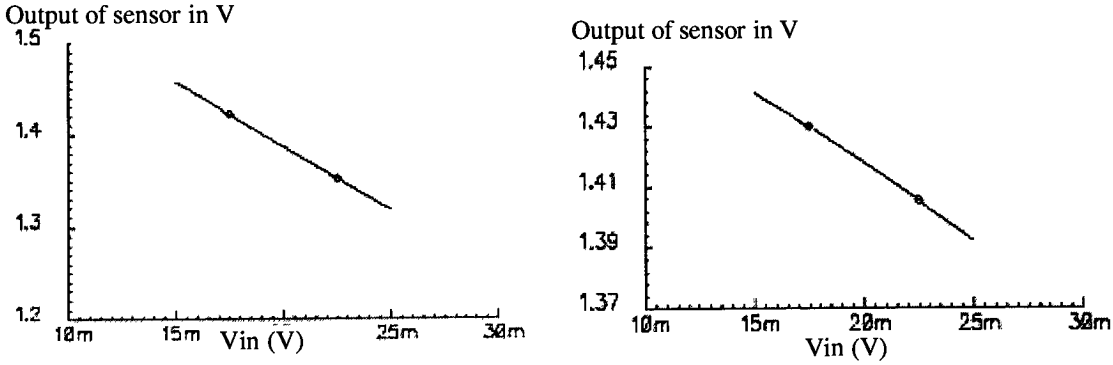
The accuracy of detection was greater than 98% (98.5% for S_{11} and 99% for S_{22}) in both cases. The accuracy can be further improved with additional tones, but this poses the downsides of increased processing times and overheads.

9.6.2 Robustness

The circuit was simulated for process variations using Monte-Carlo and Corners (3-sigma variation of process parameters) analysis. For this work, the two extreme

temperature values were chosen to be 10°C and 50°C and power supply variation was assumed to be 10%. The gain of the sense amplifier varied between 12.3 and 8.6 (at 1.9 GHz) over the weakest and strongest corners, but due to the differential approach adopted, this variation will not affect the outcome as long as sufficient gain is ensured at the weakest corner and headroom is ensured at the strongest corner. This variation was due to the fact that resistive bias networks are used. Most RF systems, especially if they are part of a SoC, will necessarily have a band-gap or stable reference, and the bias can be derived from such a reference. In such cases, the deviation over corners will be significantly less than what has been observed in this work.

Figure 9.23 plots the gain of the sensor chain at both the corners. The curve remains linear and stable.



(a) Strongest corner **(b) Weakest corner**

Figure 9.23 Transfer function Sensor Chain over process, temperature and power supply corners.

The entire self-correction circuitry presented in Chapter 3 was re-simulated at the weakest corner. It was observed that although the absolute values have changed, calibration process is successful (Figure 9.24), demonstrating the robustness of this process.

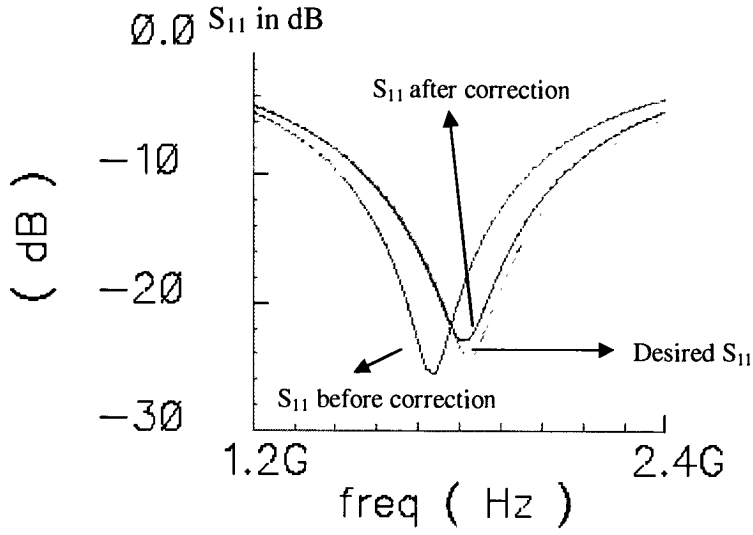


Figure 9.24 S_{11} curves before and after correction for the weakest corner (simulation).

9.6.3 Charge leakage by storage capacitors

While the kT/C noise of the capacitors are in the order of a few microvolts at best (and thus do not impact the calibration), resistive leakage paths can lead to a steady RC decay of the voltage across capacitors. Buffers were used in these paths to minimize this charge leakage (which is proportional to voltage). The capacitors lost less than 1% of their charge in 2 μs (Figure 9.25), thus ensuring accurate decision making further down the signal chain.

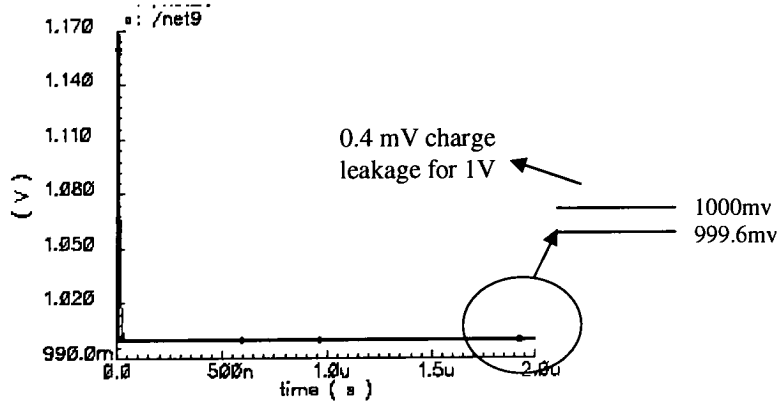


Figure 9.25 Charge leakage is negligible due to the presence of buffers [29]

9.6.4 Power-supply rejection of the adaptive-bias network

The adaptive-bias network used for IIP3 correction (Section 7.1.4) uses NMOS switches to control the bias current. The impact of this network on the sensitivity of bias-current to power-supply variations is discussed here.

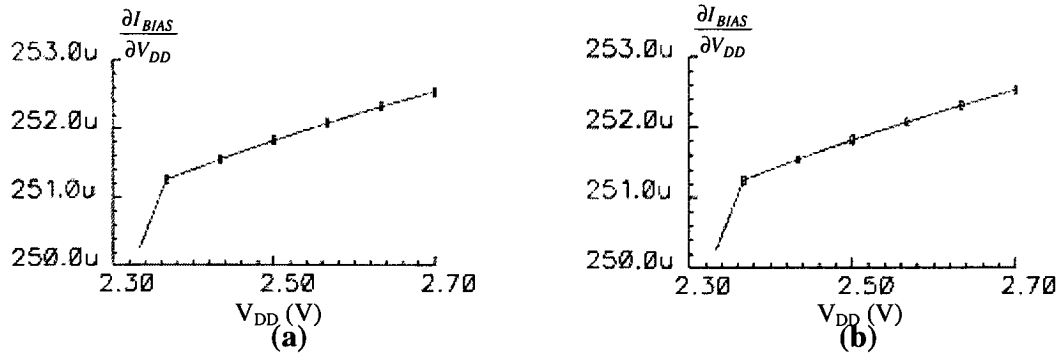


Figure 9.26 Sensitivity of Bias current versus Supply voltage for a V_{DD} variation of 2.30 V-2.70 V, with (a) and without (b) adaptive bias network.

Figure 9.26 plots the sensitivity of the bias current ($\frac{\partial I_{BIAS}}{\partial V_{DD}}$) in simulation, for both adaptive and nominal bias configurations. It is seen that the sensitivity is identical in both cases, thus proving that the adaptive bias network has not impacted variations with respect to power-supply voltage fluctuations.

Figure 9.27 plots the PSRR for both cases, and it is seen that the PSRR of the adaptive bias network[32] is marginally better than the nominal case. These results confirm that the adaptive bias network does not degrade power supply rejection.

[32] The two curves shown in Figure 9.27 for the adaptive-bias network include the two extreme cases: when switches S_{B1}-S_{B3} (Figure 8.1) are all in off-state, and when they are all in on-state.

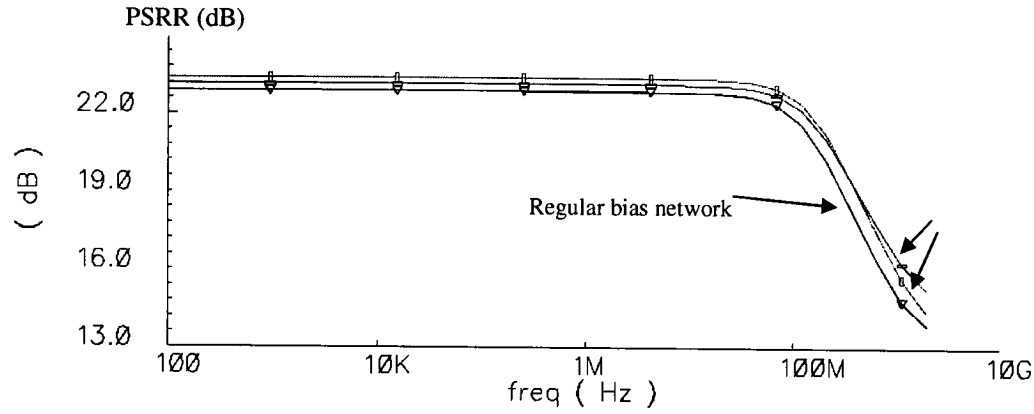


Figure 9.27 PSRR of the bias network with and without adaptive network

9.7 OVERHEADS

The total area of all additional circuitry was less than 10% of the LNA area (including the current-splitting transconductance branches, MOS varactors and the adaptive bias network), and the same circuitry can be used for other circuits in the front-end too. The current drawn by the additional circuitry was 10 mA, but these circuits need to be on for only the correction cycle, which takes less than 200 μs. During 'normal' operation, only a few logic gates need be turned on, which draw negligible or no current in their static state. The current-splitting transconductance branches used for Gain calibration and the bias adjustments used for Linearity calibration can lead to additional power consumption if the end results of both calibration mechanisms use up more current than allocated in the nominal design (sometimes the calibration may re-align the currents back to their nominal values) , then this extra current is a power overhead. Hence there

exists a reliability-power consumption trade-off. For this work, the maximum potential overhead was 1.7 mA[33] of additional current for a nominal current of 9.6 mA (17.7%).

In terms of intrusion, the on-resistance of the switches used to tap the inductor contributes to noise, and the overall degradation to the LNA was 0.22 dB. This overhead is due to the use of MOS switches. If laser-fuses were used (post-fabrication, wafer level self-calibration), then the impact on noise figure will be near-zero. The sensor at the source-inductor of the LNA marginally degrades the self-resonant frequency of the coil, but since the degraded value is about three-four times the operating frequency of the circuit, this intrusion will have no measurable impact on the circuit performance. Additionally, due to the digital nature of self-correction employed, there exists a minimum resolution for correction of each specification. This resolution is a trade-off between application requirements, process limitations and design complexity. Use of higher resolution entails the generation of larger digital words (more bits).

[33] Each transconductance branch takes 0.5 mA, and four such branches mean 2mA – 1 mA on either side of the nominal current of 9.6 mA, translating to a potential maximum 1 mA overhead. Similarly, for the Linearity bias adaptability, there is a potential 0.7 mA overhead.

Chapter 10. CONCLUSIONS

The concept of fault-tolerant RF design has great relevance and applicability in an RFIC world of increasing complexity and massive integration. One of the foremost challenges in the RFIC domain, as we scale beyond the 90 nm node, is reliability and yield. Traditional methods of increasing reliability in the digital and analog domain are not applicable to design in the gigahertz regime. An alternative methodology for incorporating fault-tolerance in RF circuits with minimal overheads and no topology revision has been developed. This methodology and its application towards a fault-tolerant LNA is the first of its kind, to the author's knowledge.

The sensor and associated circuitry are all re-used for self-correction of different performance metrics such as gain, linearity, input-match and output-match. The method has an inherently high fault-coverage, since it senses and corrects circuit performance rather than focusing on individual faults. In addition, the circuitry poses minimal overheads in terms of power and real-estate, characterized by absence of any DSP processing and extremely fast correction times.

The sensitivity analysis described in Chapter 3 provides a basis for the self-calibrating system. It is simulation independent, and lends itself well to multiple iterations and different designs. It provides valuable pre-simulation information to the designer in choosing the components that will be made variable, in addition to defining the range of variations and the number of discrete steps of variation. The analysis provides insight into the constraints and dependencies of component values to the circuit specifications, thus providing information useful for trade-offs and performance.

With the sensitivity analysis providing the basis, robust algorithms and post-processing techniques for typical RF front-end performance specifications have been developed, and have been demonstrated on a single-ended LNA. The techniques are inherently robust and their integrity will not be affected by variations in process or temperature. The input stimuli used in the correction methodology need only moderate precision to test and calibrate the front-end circuit with correction times lesser than 200 μs. The entire sensing and processing circuitry along with the LNA have been fabricated in IBM 0.25 μm 6RF process and the experimental results have successfully verified the methodology.

The methodology's strengths lie in their minimal intrusion, robustness, fast processing times, and low overheads in terms of power and area. It requires negligible power since the system will be switched on only during the correction cycles, and the area overhead is less than 10% that of a standard LNA. It must be mentioned that the same circuitry can be re-used for other circuits in the front-end chain as well. The end-result is superior to even existing test strategies, which usually requires off-chip computing, DSP cores, and high-test times (order of hundreds of milliseconds). The digital nature of self-correction sidesteps obstacles and disadvantages of feedback, and the number of bits used is application dependent. Among the downsides, Noise Figure is the only specification that cannot be addressed by this methodology. In addition, the discreteness of the technique involves a quantization error after self-correction, the

switches in the tapped coil lead to a marginal Noise Figure degradation, and the methodology requires control over the input-stimuli[34] during correction.

Future directions for this work can include extending the techniques to other front-end circuits, investigating methods to eliminate the Noise Figure degradation, and to develop sense-and correct (low-overhead) mechanisms for the Noise Figure of the circuit. This work can also be extended to compensate for environmental conditions such as temperature changes.

[34] Provided by the on-chip VCO

REFERENCES

[1] B. Razavi, "RF CMOS transceivers for cellular telephony", *IEEE Communications Magazine*, Vol. 41, No. 8, pp.144 – 149, August 2003.

[2] B. A. Floyd, C.-M. Hung, K. K. O, "Intra-Chip Wireless Interconnect for Clock Distribution Implemented With Integrated Antennas, Receivers, and Transmitters", *IEEE Journal of Solid-State Circuits,* vol. 37, no. 5, pp. 543-552, May 2002.

[3] M.-C. F. Chang, V. P. Poychowdhury, L. Zhang, H. Shin, Y. Qian, "RF/Wireless Interconnect for Inter- and Intra-Chip Cpmmunications", *Proceedings of the IEEE*, vol. 89, no. 4, pp.456-466, April 2001.

[4] J.M.V. Santos Dos, J.M.M. Ferreira, "Fault-tolerance: new trends for digital circuits" *IEEE International Conference on Electronics, Circuits and Systems*, Vol 3, pp. 237 – 240, Sept. 1998.

[5] Michael S. Heutmaker, Duy K. Le, "Architecture for self-test of a wireless communication system using sampled IQ modulation and boundary scan", *IEEE Communications Magazine*, Vol. 37, No. 6, pp. 98-102, June 1999.

[6] M. Jarwala, Duy Le, M. Heutmaker, "End-to-end test strategy for wireless systems" *Proceedings of the IEEE International Test Conference (TC)*, pp. 940-946, 1995.

[7] N. Nagi, A. Chatterjee, H. Yoon, J. A. Abraham, "Signature analysis for analog and mixed-signal circuit test response compaction", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 17, No. 6, pp. 540-546, June 1998.

[8] Rajsuman R., "Iddq testing for CMOS VLSI", *Proceedings of the IEEE*, Vol.88 No. 4, pp. 544 –568, April 2000.

[9] Isern E., Figueras J., "Test generation with high coverages for quiescent current testing of bridging faults in combinational systems", *Proceedings of the International Test Conference*, pp. 73 -82, October 1993.

[10]A. Gopalan, T. Das, C. Washburn and P.R. Mukund, "An ultra-fast on-chip BiST for RF CMOS LNAs", *Proceedings of 18th International conference on VLSI Deign,* January 2005, pp.485 – 490.

[11]Thomas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", *Cambridge University Press,* 1998.

[12] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ: Prentice-Hall, 1998.

[13] V. Aparin and L.E. Larson, "Modified Derivative Superposition Method for Linearizing FET Low-Noise Amplifiers", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 53, No. 2, pp. 571 581, Feb 2005.

[14] M.T. Terrovitis and R.G. Meyer, "Intermodulation Distortion in Current-Commutating CMOS Mixers", *IEEE Journal of Solid-state Circuits,* Vol. 35, No. 10, pp.1461 - 1473 ,Oct 2000.

[15] Anand Gopalan, P.R.Mukund and Martin Margala, "A Non-Intrusive Self-Test Methodology for RF CMOS Low Noise Amplifiers", *IEEE Mixed-signal Test workshop,* Portland, June 2004.

[16] M. Negreiros, L. Carro, A.A. Susin, "Towards a BIST. Technique for Noise Figure Evaluation", *European Test. Symposium*, ETS'04, 2004.

[17] "Fundamentals of RF and Microwave Noise Figure Measurements", *Agilent Application note 57-1.*

[18] John Ferrario, Randy Wolf, Steve Moss, Mustapha Slamani, "A low-cost test solution for wireless phone RFICs", *IEEE Communications Magazine*, v 41, n 9, September, 2003, pp. 82-89.

[19] S. Sridharan, G. Nayak, P.R. Mukund, "LNA design optimization with reference to ESD protection circuitry", *International Symposium on Circuits and Systems*, Bangkok, Thailand, May 2003.

[20] A. M. Niknejad, R G. Meyer, "Design, Simulation and Applications of Inductors and Transformers for Si RF ICs", *Kluwer Academic Publishers, Boston*, c2000.

[21] P. *Khandelwal, K. Chinnaswamy, K. Shenai,* "RF package characterization and modeling", *Proceedings of the Thirteenth Biennial University/Government/Industry Microelectronics Symposium*, June 20-23 1999, Pages:182 – 185.

[22] IBM 0.25 μm CMOS 6RF process PDK data.

[23] R. Voorakaranam, S. Cherubal, A. Chaterjee, "A signature test framework for rapid production testing of RF circuits", *Proceedings of Design, Automation and Test in Europe Conference and Exhibition*, pp.186 – 191, March 2002

[24] A. Haider, S. Bhattacharya, G. Srinivasan, A. , A. Chaterjee, "System-level alternate test approach for specification test of RF transceivers in loopback mode", *Proceedings of 18th International Conference on VLSI Design*, pp. 289 – 294, Jan 2005

[25] Lupea.D, Pursche.U, Jentschel.H.-J, "RF-BIST: loopback spectral signature analysis", *Design, Automation and Test in Europe Conference and Exhibition,* pp. 478 – 483, 2003

[26] Dabrowski.J, Bayon.J.G, "Mixed Loopback BiST for RF Digital Transceivers", *Proceedings of the 19th IEEE International Symposium* on *Defect and Fault Tolerance in VLSI Systems,* pp.220 – 228, Oct. 2004

[27] Arabi, Karim, Kaminska, Bozena," Oscillation built-in self test (OBIST) scheme for functional and structural testing of analog and mixed-signal integrated circuits", *IEEE International Test Conference (TC),* pp. 786-795, 1997

[28] R. Jee-Youl, D. Kadam, T. Alex, B.C. Kim, "Design of a new RF BIST circuit for 5.25GHz low noise amplifiers", Proceedings of the 2004 Meeting of Bipolar/BiCMOS Circuits and Technology, pp. 257 – 260, Sept. 2004

[29] A. Gopalan, "Built-in Self-test of RF front-end circuitry", *Doctoral Dissertation,* Rochester Institute of Technology, 2005

[30] A. Gopalan, M. Margala, P.R. Mukund, "A current based self-test methodology for RF front-end circuits", *Microelectronics Journal,* Vol. 36, pp. 1091-1102, 2005

[31] H. Matsui, M. Ueda, M. Daito, K. Iizuka, "A 14bit digitally self-calibrated pipelined ADC with adaptive bias optimization for arbitrary speeds up to 40MS/s", *Symposium on VLSI Circuits, Digest of technical Papers,* pp. 330 – 333, June 2005

[32] R.G. Meyer, W.D.Mack, "A DC to 1-GHz differential monolithic variable-gain amplifier", *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 11, pp.1673 – 1680, Nov. 1991

[33] K.W. Kobayashi, K.T. Ip, A.K. Oki, D.K. Umemoto, S. Claxton, M. Pope, J. Wiltz, "GaAs HBT 0.75-5 GHz multifunctional microwave-analog variable gain amplifier", *IEEE Journal of Solid-State Circuits*, Vol. 29, No. 10, pp.1257 – 1261, Oct. 1994

[34] P.R. Mukund, "Chip-Package Co-Design of Integrated RF Microsystems", *SRC Technical report, Annual Review 2003*

[35*] **Tejasvi Das**, A. Gopalan, C. Washburn and P.R. Mukund, "Towards Fault-tolerant RF front-ends", *Journal of Electronic Testing (JETTA),* Accepted for publication, Sep.06

* Publications generated by this work and authored/co-authored by the author of this dissertation.

[36*] **Tejasvi Das**, A. Gopalan, C. Washburn and P.R. Mukund, "Self-Calibration of Input-Match in R.F. Front-end Circuitry", *IEEE Transactions on Circuits and Systems II,* Dec. 2005, Vol.52, No. 12, pp. 821-825, Dec. 2005

[37*] **Tejasvi Das** and P.R. Mukund, 'Self-calibration of gain and output-match in LNAs", *Proceedings of IEEE International Symposium on Circuits and Systems,* May 2006

[38*] **Tejasvi Das**, A. Gopalan, C. Washburn and P.R. Mukund, "Towards Fault-Tolerant RF Front-Ends: On-Chip Input Match Self-Correction of LNAs", *Proceedings of the IEEE Mixed-signal Test Workshop,* June 2005

[39*] **Tejasvi Das**, A. Gopalan, C. Washburn and P.R. Mukund, "Dynamic Input match correction in RF Low Noise Amplifiers", *19th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems,* pp. 211-219, Oct. 2004

[40*] A. Gopalan, **Tejasvi Das**, C. Washburn and P.R. Mukund, "Use of Source Degeneration for Non-Intrusive BIST of RF Front-end Circuits", *Proceedings of IEEE International Symposium on Circuits and Systems,* Vol. 5, pp.4385-4388, May 2005

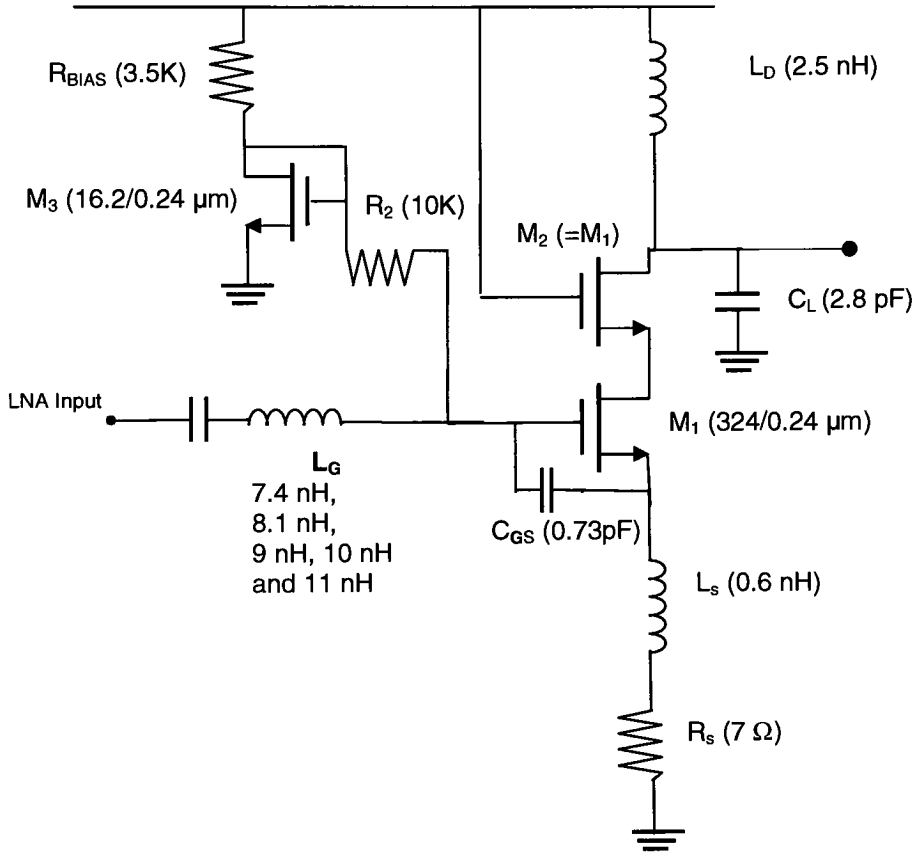
[41*] Anand Gopalan, **Tejasvi Das**, Clyde Washburn and P.R.Mukund, "An Ultra-Fast, On-chip BiST for RF Low Noise Amplifiers", *in the proceedings of the 18th International Conference on VLSI Design*, Jan. 2005.

[42*] Jay Fukumoto, **Tejasvi Das**, Ken Paradis, Jeff Burleson, J.E Moon and P.R. Mukund, "Impact of Asymmetric Metal Coverage on High Performance MOSFET Mismatch", *Journal of Solid-State Electronics,* Oct-Nov 2004, vol.48, pp 1667-1670

* Publications generated by this work and authored/co-authored by the author of this dissertation.

APPENDIX A

The circuit diagram shown below was used for the analysis of Chapter 5.



APPENDIX B

The following devices from the IBM 6RF CMOS 0.25 μm process were used in this work. The details pertain to the Process Design Kit (PDK) offered by IBM.

1. All RF transistors were 2.5 V, thick-oxide transistors with guard-rings and substrate contacts along their perimeter. All LNA, sensor, Peak detector circuits used in this work used these transistors.
2. All analog transistors were 2.5 V, thick-oxide transistors without guard rings. All op-amps, buffers, comparators and subtractors used these devices.
3. All digital gates and flip-flops were devices from the Standard digital library provided in the PDK
4. All capacitors were Metal-on-Metal capacitors.
5. All inductors except the tapped gate-coil were PDK characterized coils from the library.
6. The gate-coil was characterized in ASITIC [20], and details are provided in Chapter 8.
7. Characteristic impedance of 50 Ω has been used for the input and output ports.
8. Power-supply was 2.5 V – 0 V.
9. Diodes in the peak detector were N-well diodes from the RF library.
10. Unsalicided Polysilicon resistors were used due to their low parasitics and leakage characteristics.

The PDK documentation provides all data and details about components and their characteristics.

APPENDIX C

The circuit diagram shown below was used for the analysis of Chapter 6.