Rochester Institute of Technology

RIT Digital Institutional Repository

Theses

3-7-2014

High Efficiency Silicon Photonic Interconnects

Liang Cao

Follow this and additional works at: https://repository.rit.edu/theses

Recommended Citation

Cao, Liang, "High Efficiency Silicon Photonic Interconnects" (2014). Thesis. Rochester Institute of Technology. Accessed from

This Dissertation is brought to you for free and open access by the RIT Libraries. For more information, please contact repository@rit.edu.

R.I.T

High Efficiency Silicon Photonic Interconnects

by

Liang Cao

A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctorate of Philosophy in Microsystems Engineering

Microsystems Engineering Program
Kate Gleason College of Engineering

Rochester Institute of Technology
Rochester, New York
March 7, 2014

High Efficiency Silicon Photonic Interconnects
By
Liang Cao

Committee Approval:

We, the undersigned members of the Faculty of the Rochester Institute of Technology, certify that we have advised and/or supervised the candidate on the work described in this dissertation. We further certify that we have reviewed the dissertation manuscript and approve it in partial fulfillment of the requirements of the degree of Doctor of Philosophy in Microsystems Engineering.

Stefan F. Preble 03/10/2014
Dr. Stefan F. Preble Date
Advisor, Associate Professor, Microsystems Engineering Program

Seth Hubbard 03/12/2014
Dr. Seth Hubbard Date
Associate Professor, Microsystems Engineering Program

Zhaolin Lu 03/10/2014
Dr. Zhaolin Lu Date
Associate Professor, Microsystems Engineering Program

Christiaan Richter 03/10/2014
Dr. Christiaan Richter Date
Assistant Professor, Microsystems Engineering Program

Muhammad Shaaban 03/10/2014
Dr. Muhammad Shaaban Date
Associate Professor, Computer Engineering Program

Certified by:

Brice W. Smith 03/10/2014
Dr. Bruce W. Smith Date
Director, Microsystems Engineering Program

Harvey J. Palmer 03/19/2014
Dr. Harvey J. Palmer Date
Dean, Kate Gleason College of Engineering

ABSTRACT

Kate Gleason College of Engineering
Rochester Institute of Technology

Degree: Doctor of Philosophy **Program:** Microsystems Engineering
Author Name: Liang Cao
Advisor Name: Stefan Preble
Dissertation Title: High Efficiency Silicon Photonic Interconnects

Silicon photonic has provided an opportunity to enhance future processor speed by replacing copper interconnects with an on chip optical network. Although photonics are supposed to be efficient in terms of power consumption, speed, and bandwidth, the existing silicon photonic technologies involve problems limiting their efficiency. Examples of limitations to efficiency are transmission loss, coupling loss, modulation speed limited by electro-optical effect, large amount of energy required for thermal control of devices, and the bandwidth limit of existing optical routers. The objective of this dissertation is to investigate novel materials and methods to enhance the efficiency of silicon photonic devices. The first part of this dissertation covers the background, theory and design of on chip optical interconnects, specifically silicon photonic interconnects. The second part describes the work done to build a 300mm silicon photonic library, including its process flow, comprised of basic elements like electro-optical modulators, germanium detectors, Wavelength Division Multiplexing (WDM) interconnects, and a high efficiency grating coupler. The third part shows the works done to increase the efficiency of silicon photonic modulators, unitizing the $\chi(3)$ nonlinear effect of silicon nanocrystals to make DC Kerr effect electro-optical modulator, combining silicon with lithium niobate to make $\chi(2)$ electro-optical modulators on silicon, and increasing the efficiency of thermal control by incorporating micro-oven structures in electro-optical modulators. The fourth part introduces work done on dynamic optical interconnects including a broadband optical router, single photon level adiabatic wavelength conversion, and optical signal delay. The final part summarizes the work and talks about future development.

For my parents,

for many years of encouragement, love, and support,

and for emphasizing the importance of education.

For my wife

and my son

for everything

forever

ACKNOWLEDGMENTS

I felt so fortunate to be surrounded by many loving people and now it is my pleasure to thank all of them for their love, encouragement, support and blessing.

First of all, I would like to express my sincere gratitude to my advisor Professor Stefan Preble, for his valuable guidance and generous support throughout my entire graduate studies at RIT. His pioneering vision in optical science, abundance of knowledge and hardworking spirit inspired and motivated me. Without his insightful suggestions and persistent help, this dissertation would not have been possible.

I would like to thank Dr. Yenwen Lu, and Dr. Bruce Smith for taking me into the area of Microsystems and reminding me that there is a lot more room at the bottom scale. I would like to thank Dr Zhaolin Lu for his support and valuable discussion during my research. In addition to Dr. Zhaolin Lu, I would like to thank Dr. Seth Hubbard, Dr. Christiaan Richter and Dr. Muhammad Shaaban for serving as my dissertation committee, willing to share their valuable opinions and their useful critiques on my research.

I would like to thank the staff members at Cornell NanoScale Science and Technology Facility (CNF), and the staff members in the Semiconductor and Microsystems Fabrication Laboratory (SMFL), without them, I could not get my work done at all.

I want to express my gratitude to my colleagues Dr. Karthik Narayanan, Dr. Ali Elshaari, Dr. Donald Adams, Dr. Abdelsalam Aboketaf, Zihao Wang, Dr. Ruoxi Yang, Andrew Estoff, Dr. Peng Xie, Dr. Zhonghua Yao, Xiang Li, Dr. Wangshi Zhao for their help in offering me useful technical discussions.

I would like to thank DARPA, SEMATECH, AFOSR, SRO, ACS PRF and NSF for funding me for my research.

And finally, I would like to express my thanks to my parents, my wife and my son for their unlimited support.

Table of Contents

ABSTRACT iii

List of Tables ix

List of Figures x

List of Symbols xxii

1 Introduction 1

1.1 Dissertation Overview 2

2 Silicon Photonic Interconnect 5

2.1 Silicon Photonic Where and How 5

2.2 Current Problems with Silicon Photonic Research 12

2.3 Basic Structure of Silicon Photonics 13

2.3.1 Silicon Waveguide 14

2.3.2 Directional Coupler 15

2.3.3 Ring Resonator 17

2.3.4 Mach-Zehnder Interferometer 20

2.4 Modulation Mechanisms in Silicon 21

2.5 Numerical Simulation Methods 24

2.5.1 Fine Difference Time Domain Method 24

2.5.2 Beam Propagation Method 25

3 Design of 300mm Silicon Photonic Library 27

3.1 300mm Process Flow Design 27

3.2 Ring Resonators 33

3.3 Electro-Optical Modulators 36

3.4 Germanium PIN Detector 42

3.5 Germanium Laser 49

3.6 Wavelength Division Multiplexing (WDM) Interconnect 55

3.7 High Efficiency Optical Coupling by Grating Coupler 58

3.7.1 Introduction of Off-Chip Packaging 58

3.7.2 Grating Fiber Coupler Design.. 61

3.7.3 Introduction of Chip to Chip Packaging 69

3.7.4 Design of Chip to Chip Packaging.. 73

3.8 Summary 81

4 Increase the Efficiency of Silicon Modulators 83

4.1 Observation of DC Kerr Modulation from Silicon Nanocrystals 83

4.1.1 Introduction.. 83

4.1.2 Total Internal Reflection 86

4.1.3 Experimental Setup.. 88

4.1.4 Testing Results... 91

4.2 Hybrid Si- $LiNbO_3$ Modulator 94

4.2.1 Introduction.. 94

4.2.2 Device Design and Simulation... 97

4.2.3 Fabrication 101

4.2.4 Result and Discussion 103

4.3 Efficient Thermal Control of Silicon Photonic 108

4.3.1 Introduction.. 108

4.3.2 Design and Simulation 109

4.3.3 Fabrication and Results.. 112

4.3.4 Discussion and Conclusion 119

5 Dynamic Control of Photonics 121

5.1 Optical delay Storage 121

5.1.1 Introduction.. 121

5.1.2 Simulation 123

5.1.3 Optical Loss Study and Device Fabrication.. 124

5.1.4 Experiment Setup 128
5.1.5 Result and Discussion 131
5.2 Broadband Optical Router 135
5.2.1 Introduction 135
5.2.2 Design and Simulation 137
5.2.3 Device Fabrication and Experiment Setup 141
5.2.4 Results and Discussion 143
5.3 Single Photon Adiabatic Wavelength Conversion 148
5.3.1 Introduction 148
5.3.2 Adiabatic Wavelength Conversion Experiment Setup 149
5.3.3 Experiment Result 151
5.3.4 Summary 156
6 Conclusion 157
6.1 Photonic Library Building 157
6.2 Modulator Device Enhancement 158
6.3 Dynamic Control of Photonics 159
6.4 Future Work 160
Appendices 162
Appendix I 162
1-Basic Ring Resonator Matlab Code 162
2-ATR Simulation Matlab Code 163
3-Optical Delay Simulation Matlab Code 165
Appendix II 169
References 174

List of Tables

Table. 2.1 Gate and Wire Delay for scaled Technology Nodes.. 6

Table. 2.2. Gap between current status and requirement... 13

Table. 3.1. Mask Setting 28

Table. 4.1. Sample preparation 93

Table. 4.2. a-Si:H deposition parameter 102

Table. 4.3.Comparison of traditional heater with single wire oven and double wire oven in rings with radius of 2.5 microns and 10 micron 118

List of Figures

Fig. 1.1. PC-board photonic interconnects build by Intel 1

Fig. 1.2. Main components in silicon photonic interconnects 2

Fig. 2.1. Intel Nehalem four-core processor 8

Fig. 2.2. Through Silicon Via interconnects 8

Fig. 2.3. Optical Interconnect connect with CMOS through TSV 10

Fig. 2.4. Imagine of artists about future network on chip 11

Fig. 2.5. Passive devices of silicon photonics 14

Fig. 2.6. SEM of Silicon waveguide and its supporting mode at 1550nm wavelength ... 15

Fig. 2.7. Transmission coefficient for through and cross ports of a directional coupler .. 16

Fig. 2.8. (a) Configuration of duel port ring resonator, (b) SEM of duel port ring resonator 19

Fig. 2.9. MZI (a) Basic idea of MZI in free space optical path (b) Integrated MZI 20

Fig. 2.10. Field evolution order in 1D-FDTD problem 25

Fig. 3.1. Process flow #1: 1. Begin with 300mm SOI wafer, deposit very thin Oxide and 170nm polysilicon, and then patten the polysilicon, etching away both polysilicon and

thin oxide. 2. Pattern and implant Boron for Pwell doping. 3. Pattern and implant phosphorous for Nwell doping. 4. Pattern and implant phosphorous for deep N doping. 5. Pattern (450nm Wide) and etch 175nm Silicon to form optical waveguide. 6. Pattern and implant boron for p+ doping. 7. Strip off oxide hard mask over waveguide. 8. Pattern and implant phosphorous for n++ doping. 9. Pattern and implant boron for p++ doping...... 30

Fig. 3.2. Process Flow #2: 10. Rapid thermal anneal for implant activation. 11. Clad SiO2 hard mask and pattern holes to epitaxial Germanium. 12. CMP for form flat Germanium and then wet etch hard maks. 13. P+ doping over Germanium. 31

Fig. 3.3. Process Flow#3: 14.Pattern grating etch and do multiple etches to form the grating. 15. Pattern and deposit Nickel for contact and thermally grow Nickel-Silicide. 16. Deposit 1microns of oxide for cladding. 17 Etch channels in oxide for heaters. 18. Deposit TiN and CMP. 19. Pattern and etch oxide for Germanium contact. 31

Fig. 3.4. Process Flow #4: 20. Pattern and etch oxide for Silicon level contact. 21. Pattern and etch oxide for Silicon Modulator contact. 22. Deposit Copper and CMP. 23. Pattern oxide channel for metal pad. 24. Deposit Copper and CMP 33

Fig. 3.5. (a) Ring resonator (b) Quality factor Vs Ring radius 34

Fig. 3.6. (a) Ring resonator with through port (b) Extinction and Quality factor at different gap and width 35

Fig. 3.7. (a) Ring resonator with dual ports (b) Extinction and Quality factor at different gap and width 36

Fig. 3.8. (a) Forward biased PIN diode (b) Spectrum of through port and drop port of switch based on forward biased PIN diode 37

Fig. 3.9. PIN diode CAD design 38

Fig. 3.10. Doping level of PN depletion modulator 39

Fig. 3.11. Carrier concentration at (a) 0.7V (b)-1V (c) -3V 39

Fig. 3.12. Ring resonator with PN modulator at different condition 40

Fig. 3.13. CAD Design of PN depletion mode modulator 41

Fig. 3.14. Cross-section view of layer stack for the direct hetero-epitaxial growth of Ge on Si 43

Fig. 3.15. (a) basic configuration of lateral detector. (b) Cross-section of PIN detector. (c)Test setup (c) Dark current performance. (d) Time response performance 44

Fig. 3.16. Germanium detector simulation (a)Configuration of simulation (b)Transmission VS coupling length at different wavelength (c) Transmission VS Germanium thickness (d) Ttransmission Vs width variation 47

Fig. 3.17. (a) Metal block absorption setup (b) Spectrum comparing with metal and without metal 48

Fig. 3.18. Comparison of Vertical PIN detector and Lateral PIN detector....................... 49

Fig. 3.19. CAD design of germanium detector 49

Fig. 3.20. (a) Band structure of bulk Ge have 136meV difference between direct gap and indirect gap (b)Decrease difference between direct and indirect gaps by introducing tensile strain (c)fill electrons in indirect valley to fill the rest of difference..................... 50

Fig. 3.21. Schematic of first integrated Ge laser.. 51

Fig. 3.22. Possible Fabry Perrot Ge Laser configuration and simulation of coupling...... 52

Fig. 3.23. Disc Resonator Ge laser 54

Fig. 3.24. Disc Resonator Ge laser 55

Fig. 3.25. Basic idea of WDM system 56

Fig. 3.26. (a)40Gbit/s WDM system (b) 80Gbit/s WDM system (c)160Gbit/s WDM system 57

Fig. 3.27. (a) Comparison of dimension of silicon waveguide to dimension of fiber (b) Inverse taper configuration 59

Fig. 3.28. Operation principle of a nanowire waveguide grating coupler 59

Fig. 3.29. (a) Principle of grating diffraction, (b) Principle of grating coupler 60

Fig. 3.30. Process Flow of Grating Coupler 61

Fig. 3.31. 2D FDTD simulation of grating coupler 63

Fig. 3.32. Simulation of optimizing the grating coupler (a)Vary total thickness from 320nm to 410nm, (b) Vary filling factor from 0.31 to 0.51, (c)Vary Period from 550nm to 670nm, (d) Vary etch depth from 300nm to 180nm 65

Fig. 3.33. Simulation of grating coupler (a) Compare of coupler with and without 20nm buffer oxide (b) Compare of coupling efficiency at different incidence angle..... 65

Fig. 3.34. Simulation of grating coupler (a) misalignment tolerance (b) With and without index matching fluid 67

Fig. 3.35. 3D FDTD simulation of focusing grating coupler (a) Configuration of focusing grating coupler (b) X-Y plane and X-Z plane view of coupling efficiency...................... 68

Fig. 3.36. Alignment tolerance study of focusing grating coupler 69

Fig. 3.37. (a) Photonic multichip based on photonic wire-bonding (b) Inverse-taper transition between an SOI nanowire waveguide and a polymer Photonics Wire Bonding interconnects. (c) SEM of Photonics Wire Bonding chip to chip interconnects 70

Fig. 3.38. Schematic of chip to board connection with inverse taper and wide polymer waveguide 71

Fig. 3.39. Grating to grating coupling with Indium reflow self-alignment method (a)Configuration of chip to chip grating coupling (b) Indium reflow self-alignment (c)basic principle of grating to grating coupling (d) grating to grating coupling loss (e) misalignment error tolerance 72

Fig. 3.40. 2D simulation of chip to chip grating coupling: (a) Configuration of grating to grating coupling (b)Cross section view of optical transportation of chip to chip coupling (c)Coupling spectrum for different overlap distance (d) Coupling loss tolerance............ 74

Fig. 3.41. (a) Chip to chip coupling efficiency at different period. (b) Chip to chip coupling efficiency with different overlap length... 75

Fig. 3.42. 3D simulation of chip to chip grating coupling: (a) Configuration of 3D focusing grating to focusing grating coupling (b) Cross section of chip to chip coupling (c) Photon transmission of input plane (d) Photon transmission at receiving plane 76

Fig. 3.43. (a) Configuration of chip to chip coupling. (b) Chip to chip coupling efficiency at different receiving place. (c) Chip to chip coupling efficiency with different gap. 77

Fig. 3.44. Cross-section of flip chip bonding and electric and optical packaging 78

Fig. 3.45. Comparison of misalignment tolerance between focused grating structure and flat grating structure 78

Fig. 3.46. (a)Flat grating coupling setting (b) coupling with 4 microns width grating (c) coupling with 6 microns width grating 79

Fig. 3.47. CAD of basic flip chip design 79

Fig. 3.48. Electric Vernier used to measure misalignment 80

Fig. 3.49. Flip-chip packaging design... 80

Fig. 3.50. Test structures designed for a 300mm process 81

Fig. 4.1. Schematic of ATR (a) Sample structure and basic construction of ATR setup (b) Simulated modulation of refractive index change to resonance angle shift 86

Fig. 4.2. Schematic of the experimental setup: (a)Sample structure and prism coupled ATR setup. (b) Simulated ATR resonance for two different SiNcs refractive indices (c) Detailed experiment set up.. 89

Fig. 4.3. Experimental results (a) detector intensity signal. (b) lock-in amplifier signal (c) fitted modulation curve.. 92

Fig. 4.4. Photoluminescence of different sample: The red dot curve is the PL of HSQ sample, the brown dash curve is the PL of PECVD sample with 1100C annealing, and the blue solid curve is the PL of PECVD sample with 800C annealing................................ 94

Fig. 4.5. Schematic cross-section of the hybrid silicon-$LiNbO_3$ modulator. The light is confined to the $LiNbO_3$ substrate by a thin a-Si:H waveguide. The metal electrodes provide an RF electric field that is used to induce the Pockels effect in the $LiNbO_3$....... 98

Fig. 4.6. Optical mode of a-Si:H waveguide on a $LiNbO_3$ substrate (a) Waveguide thickness 200nm, (b)waveguide thickness 100nm, (c) waveguide thickness 80nm, (d) waveguide thickness 70nm.. 99

Fig. 4.7. (a)Relative index change efficiency for a 700nm wide waveguide for different a-Si:H thicknesses. (b) Waveguide width dependence on index change efficiency.......... 101

Fig. 4.8. Fabrication process of silicon electro-optical modulator 102

Fig. 4.9 (a). Microscope image of the hybrid Si-$LiNbO_3$ modulator integrated into a Mach-Zehnder interferometer. The total size of the device is only 1mm. 103

Fig. 4.10. Experimental Setup used to characterize the MZI modulator 104

Fig. 4.11. Spectrum shifting driving by DC electric field 106

Fig. 4.12. RF response of the modulator at different frequencies. The inset shows an open eye-diagram for a 4.5Gb/s PRBS 2^7-1 signal.. 107

Fig. 4.13. FEM simulation of heating efficiency of (a) traditional top heater, (b) thermal contact on one side of the waveguide, (c) micro-oven heater consisting of two thermal contacts, (d) thermal contact at one side of the waveguide with a 300 nm electrical isolation gap, (e) micro-oven heater with electric isolation gaps and (f) micro-oven heater used in the experiment 110

Fig. 4.14(a) Traditional heater (b) Micro-oven heater... 113

Fig. 4.15. CAD design and microscope image of 2.5 microns radius ring with (a) Traditional Heater design (b) Single wire micro-oven heater design (c) Double wire micro-oven heater design. The ring resonators in all of the designs are coupled to two waveguides in order to ensure near-critical optical coupling. 115

Fig. 4.16. (a) Spectrum response of 2.5 microns radius micro-oven heater (b) Resonance wavelength shifting as function of input power 117

Fig. 4.17. Cross section view of Oven heater (a) without modulator (b) with isolation to modulator (c) Design CAD of PN depletion mode modulator with micro-oven design 120

Fig. 5.1. Schematic the 4 ring system and its operation principle, (Step 1) shows the acceptance state of the system. Bits are stored as shown in (Steps 2 and 3) then released in (Steps 4 and 5). 122

Fig. 5.2. Optical mode and structure of shallow etched silicon waveguide on SOI platform 125

Fig. 5.3. SEM images of shallow etched rib SOI waveguides, with etch depths of: 50nm , 75nm, and 100nm. Photoresist remains on top of the waveguides in these images. 126

Fig. 5.4. Intrinsic quality factor vs. bend radius for 100nm, 75nm, and 50nm shallow etched SOI ring resonators. 127

Fig. 5.5. Layout of optical delay 128

Fig. 5.6. Experimental setup used .The stored pulses are generated in an OPO crystal from 830nm Ti-Sapphire laser, while SHG is used to generate 415nm storage and release signals 129

Fig. 5.7. Stage control for delay of delay pulse 130

Fig. 5.8. Optical Delay Result at changing the time of release pulse 132

Fig. 5.9. Design of Electro-optical delay 133

Fig. 5.10. (a)Optical switch without bias (b)Optical switch with bias 134

Fig. 5.11. (a) ONoC configuration (b) 2x2 Ring resonator router (c) 2x2 MZI routers . 135

Fig. 5.12. A basic adiabatic coupler structure 138

Fig. 5.13. Rsoft BeamProp Simulation of (a) directional coupler (b) adiabatic coupler 139

Fig. 5.14. (a) Simulation of coupler with different gap. (b) Performance under different wavelength. 140

Fig. 5.15. MZI with adiabatic coupler 141

Fig. 5.16. Testing setup 143

Fig. 5.17. Spectrum of 80 microns adiabatic coupler compared with spectrum of directional coupler and Y splitter 144

Fig. 5.18. Spectrum of adiabatic coupler 145

Fig. 5.19. (a)Thin side without phase shift (b) Thin side with Phase shift (c) Wide side without phase shift (d) wide side with phase shift 147

Fig. 5.20. 4x4 Hitless router with 2x2MZI routers 148

Fig. 5.21. Schematic of experimental setup 151

Fig. 5.22. Measured spectra as the relative delay between the pump and probe pulse. The left panel is when the probe is at the original wavelength of the cavity. The right panel is when the probe is at the new wavelength of the cavity. 152

Fig. 5.23. Observed adiabatic wavelength conversion at single photon level compared with classical light at different converted wavelengths (a) 0.21nm (b) 0.29nm (c) 0.37nm (d) 0.59nm (e) 0.78nm 153

Fig. 5.24. (a) Relative reduction in conversion efficiencys due to free-carrier absorption vs. wavelength change. (b) Wavelength conversion efficiency as a function of time offset between the pump and the probe 154

List of Symbols

SMT	Simultaneous Multithreading
AFM	Atomic Force Microscope
ATR	Attenuated Total Reflection
BPM	Beam Propagation Method
CMOS	Complementary Metal–Oxide–Semiconductor
CMP	Chip Multi Processor
CMP	Chemical Mechanical Polishing
CVD	Chemical Vapor Deposition
DBR	Distributed Bragg reflector
DUV	Deep Ultra Violet
EDFA	Erbium Doped Fiber Amplifier
FDTD	Finite-Difference-Time-Domain
FEM	Finite Element Method
FSR	Free Spectral Range
HSQ	Hydrogen Silsesquioxane

MZI	Mach–Zehnder interferometer
NoC	Network on Chip
PECVD	Plasma Enhanced Chemical Vapor Deposition
Q	Quality factor
RF	Radio Frequency
RTA	Rapid Thermal Annealing
SiNcs	Silicon Nanocrystals
SOI	Silicon on Insulator
SPP	Surface Plasmon Polaritons
SRAM	Static Random Access Memory
TE	Transverse Electric
TM	Transverse Magnetic
TSV	Through Silicon Vias
VCSEL	Vertical Cavity Surface Emitting Lasers
WDM	Wavelength Division Multiplexor

1 Introduction

Since the invention of the laser 50 years ago [1], photonic interconnects have proven to be a technology for robustly moving information around. With the speed of light, the distance between USA and China has been shortened to be within 24ms by photonic interconnects, and "Fiber to the Home" is bringing high speed internet into neighborhoods [2]. Replacement of copper wire with photonic fiber enables lower power consumption, dramatically increased bandwidths and significantly lower latency. And these advantages are becoming more and more important at smaller length scales. In recent years, the Photonics group at IBM Research – Zurich has developed an integrated optical interconnects on printed circuit board in order to reduce the energy consumption of future IT systems [3]. And Intel researchers have created a prototype of 50G-bps silicon photonic transmit module for chip to chip interconnects [4].

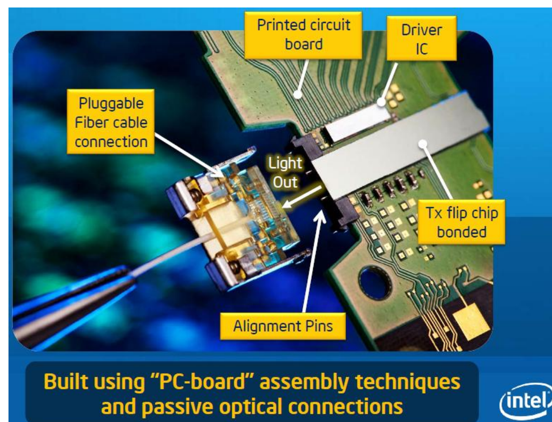


Fig. 1.1. PC-board photonic interconnects build by Intel

Now it is coming to the point where it is necessary to replace the last millimeter of copper wire with photonic waveguide, which is now commonly known as On-Chip Photonic Interconnects.

1.1 Dissertation Overview

This work has developed some building blocks for silicon photonic interconnects in order to enhance the efficiency of current silicon photonic devices and to make it a more promising platform of future on chip interconnect. Fig. 1.2. shows the main components in the silicon photonic interconnects.

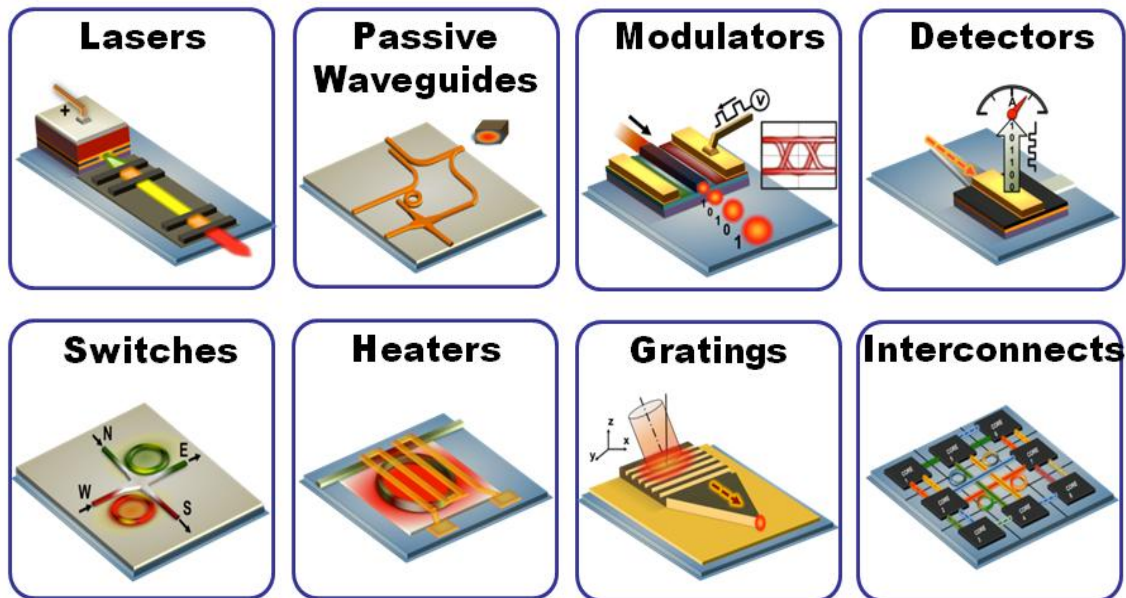


Fig. 1.2. Main components in silicon photonic interconnects

The dissertation is organized as follows:

Chapter 2 starts by introducing the development of computer processors, the architecture of chip multiple processor and the possibility and need for developing on chip optical networking. Then it introduces some basic silicon photonic concepts including basic elements, fabrication method and simulation methods.

Chapter 3 introduces my work on building a 300mm Silicon Photonic Library including its process flow, and basic elements like electro-optical modulator, Ge detector and WDM interconnects. Section 3.1 introduces high efficiency optical grating coupler design and its implementation for chip to chip coupling.

Chapter 4 introduces the work done to increase the efficiency of Silicon Modulators. Section 0 introduces the work done on utilizing the $\chi^{(3)}$ nonlinear effect for a high efficiency electro-optical modulator, where we observe DC Kerr effect in Silicon Nanocrystals. Section 3.2 introduces the work done on achieving $\chi^{(2)}$ nonlinear effect on Silicon, where we realize hybrid Silicon -$LiNbO_3$ integration and demonstrate high efficiency electro-optical modulator. Section 4.3 then introduces a way to efficiently control the thermal problems encountered with the operation of electro-optical modulators.

Chapter 5 introduces the dynamic control of photonic circuits. Section 0 introduces experimental demonstration of long time optical signal delay. Section 5.2 introduces a

design of broadband optical router. Section 5.3 introduces an experimental demonstration of single photon level adiabatic wavelength conversion.

Chapter 6 summarizes the work and also talks about the future development.

2 Silicon Photonic Interconnect

Silicon photonic is an exciting new frontier that has captured the imaginations of people worldwide. It's important to know its development background and its basic research method. This chapter starts with the history introduction of development of computer processors and architecture of chip multiprocessors and the possibility and necessity for developing on-chip optical networking based on silicon photonics. Then introduction of some basic silicon photonic concepts and common research methods including basic elements, fabrication methods and simulation methods are followed. And finally, the current research status of silicon photonic presents the large picture and goals in the development of silicon photonics.

2.1 Silicon Photonic Where and How

The clock speed of computer processors has remained around 5GHz for a long while because the amount of power that can be dissipated per cm^2 on a die is limited to be nearly $100W/cm^2$ [5]. Consequently, the main method to improve processor performance is by increasing transistor density, which is achieved by minimizing feature size. However, while the performance and energy consumption of transistors have greatly improved, copper interconnect performance is not keeping up even after optimized low k dielectric techniques [6] and repeater insertion method, as shown in Table. 2.1.

Table. 2.1 Gate and Wire Delay for scaled Technology Nodes

Delay Types	Technology Node		
	45nm	32nm	22nm
FO4(Gate Delay) (ps)	9	5.5	3.6
Global Wire(RC-Delay) (ps/mm)	280	300	760
Global Wire(repeared) (ps/mm)	61	65	75
Global Wire(optimized+repeatered) (ps/mm)	31	33	36

This trend will become even more severe in the future when feature size scales down to the 10nm level. At the same time, to handle more and more transistors on the same chip, new micro-architectures are developed to execute many instructions within single, sequential program in parallel [7], such as simultaneous multithreading (SMT) and chip multiprocessors (CMP) [8]. SMT is based on superscalar processors which implement a form of parallelism called thread level parallelism within a single processor [9]. SMT allows processors to execute instructions from multiple threads of control simultaneously and can dynamically select and execute instructions from many active threads at the same time. Even when multithread is not available it still can work as conventional wide-issue superscalar [10]. However, SMT requires short interconnect delay which is already lagging behind gate delay as mentioned before. The large interconnect delay requires micro-architecture to be divided into smaller, localized processing elements. CMP as the competitor to SMT uses multiple single thread processor cores; multiple threads can be

executed simultaneously across multiple cores. It requires applications to be decomposed into multiple threads to fully utilize the multi core system. The CMP, composed of small, localized processing cores, has a relaxed interconnect delay requirement and is relatively simple, thus becoming the favorite of both hardware and software developers.

Regarding CMP development, a communication network subsystem between cores and memory needs to be developed [11]. The NoC (Network on Chip) approach applies networking theory and methods of on-chip communication by replacing large number of low activity dedicated wires with fewer multiplexed communication links, which brings great improvement over conventional bus and crossbar interconnections [12]. Although CMP requires less delay in a core than STM, enhancing the networking performance between cores and memory will still enhance the total performance dramatically.

CMP chips normally locate significant memories on chip in static random access memory (SRAM) cache [13]. As we can see from Fig. 2.1, about one third of the chip area is used to provide 8MB of L3 cache. The L2 cache is not shown as it is integrated into each core where it can occupy 80% of the space.

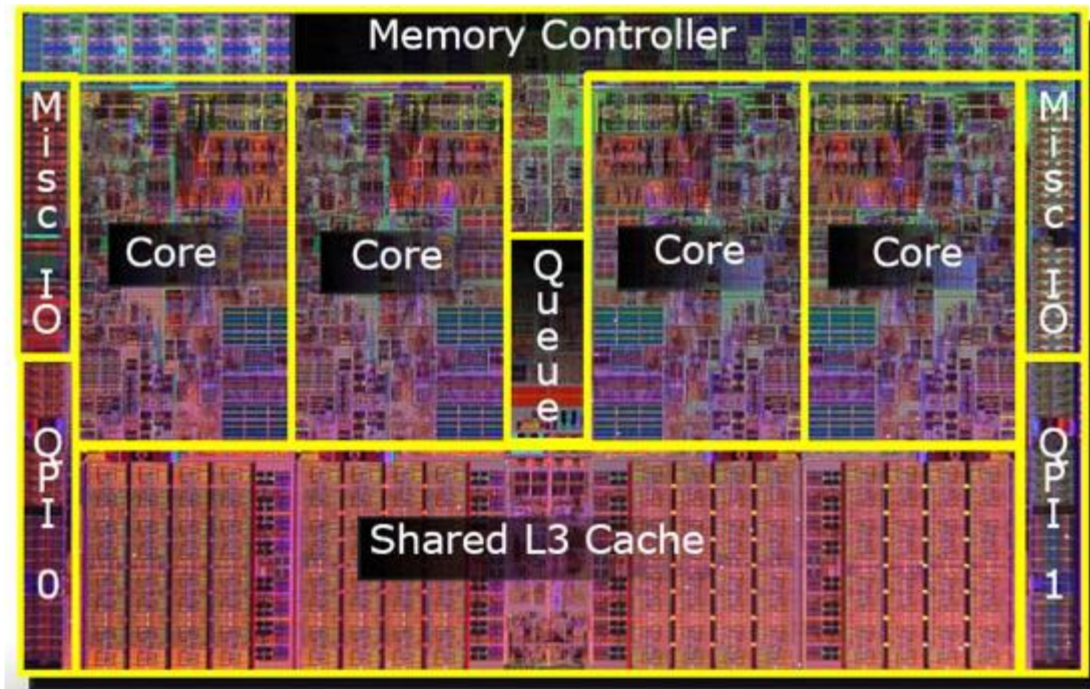


Fig. 2.1. Intel Nehalem four-core processor[14]

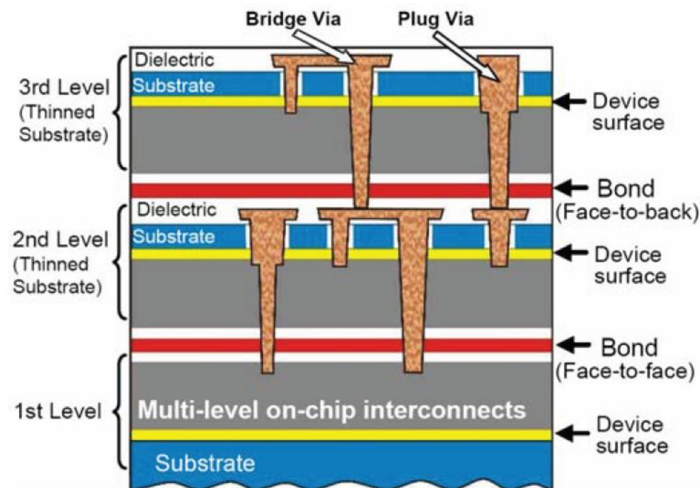


Fig. 2.2. Through Silicon Via interconnects [15]

Recent development of 3D interconnects like TSV (Through Silicon VIA) enables stacking of chips that shorten the distance between chips[16] as seen in Fig. 2.2. As TSV technology develops, it is possible that TSV can be similar in length to existing VIA,

resulting in the distance between chips to be even shorter than on the same chip[17]. Consequently, cache can be moved to other chips on top or below the core chip. This opens up significantly more area on the actual core chips for even more transistor density for processing.Therefore, by stacking memory and processing chips, with the same size of die, and even same scale node technology, we can theoretically build much higher transistor density chips with many more processing cores. However, with this archetecture, we still need a way to efficiently enhance the communications among cores that is located at the same plane.

As people have replaced the copper wire with fiber photonics for the network outside of the chip and have achieved great success, people are now thinking of replacing the last millimeter of copper in the chip creating an Optical Network-on-Chip (ONoC) [18]. The size of silicon waveguides, due to the high contrast of silicon and silicon dioxide, has reached the range of ~400nm in width, which is similar to the current global interconnects size. As mentioned before, scaling down would not enhance performance of copper connections, therefore, future copper global interconnects will have a similar size as Silicon waveguides (~400nm pitch). However, optical waveguides have the key advantage that they can carry much broader bandwidth than copper wire, by using wavelength division multiplexing (WDM). Therefore, one optical waveguide can realize the same performance

as multiple copper interconnects, which in turn, minimizes the interconnects footprint. In addition, optical waveguides themselves don’t s the problems of latency and power dissipation. Most of the latency and power consumption in photonic interconnect happens at the end-devices and the total effect can be much lower than that of copper interconnects. This trend is more obvious in super-computers where thousands of processors need inter communication, which requires large bandwidth and low loss. With development of Vertical Cavity Surface Emitting Lasers (VCSEL’s), chip to chip optical interconnects have already been integrated in supercomputers like Blue Gene L in 2004 at Lawrence Livermore Labs[19][20]. And we expect as commercial processors contain more and more cores in one chip, the requirement for low loss and large bandwidth interconnects will inevitably force the transition to on-chip optical interconnects.

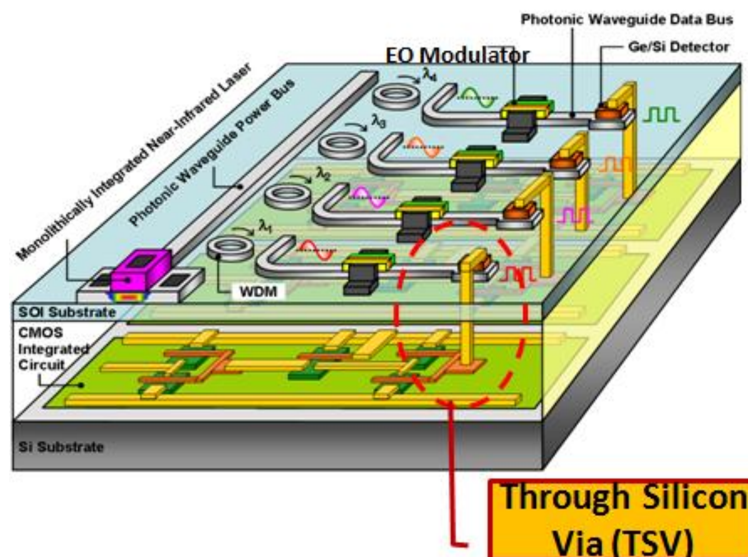


Fig. 2.3. Optical Interconnect connect with CMOS through TSV

Furthermore, while TSV's are currently a competitor to photonic interconnects they will eventually serve a supporting role. This is because it is currently challenging to integrate photonics and electronics together due to differences in processing technologies. However, using TSV's it is possible to stack optical and electrical chips as in Fig. 2.3. Therefore, the physical distance between photonic interconnects to electronic devices can be reduced by the TSV technology.

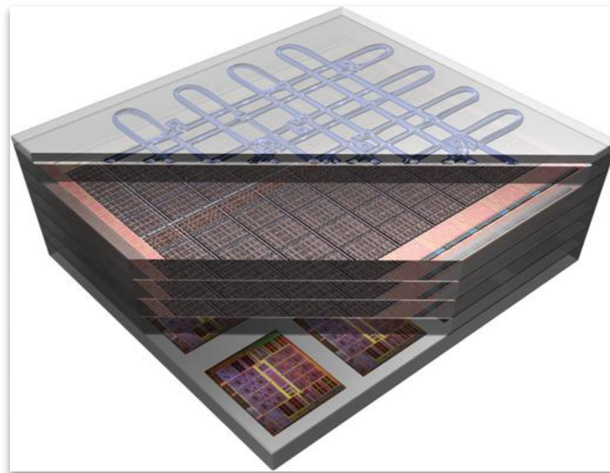


Fig. 2.4. Imagine of artists about future network on chip[21]

Lastly, another possible future stacking architecture of CMP's is shown in Fig. 2.4. Cores are located in one layer, with stacks of memory TSV connected to the cores, while a layer of optical interconnects are TSV connected to cores vertically, taking care of intercommunication among the cores. The processor can have the most transistor density and best efficiency in this way.

2.2 Current Problems with Silicon Photonic Research

The current silicon photonic research still has gaps before commercialization. For example, the current mainstream chip fabrication is based on 300mm wafers. However, before our work is launched, there is no report of 300mm Fab Photonic fabrications. This is mainly because of the processing substrate: 300mm SOI with thick buried oxide has not been ready until very recently. The main SOI wafer manufacturer, SOITEC, has developed a prototype of 300mm SOI wafer with 2 microns of thick buried oxide. Although high speed modulator and Ge detector have been reported to have integrated on Silicon waveguide, major issues still exist with the laser source on silicon substrate. Table. 2.2 gives a basic idea of the existing gaps between current developments of optical interconnects and the requirement for on-chip interconnects.

Table. 2.2. Gap between current status and requirement

Critical Needs	Target	Status	Gap?	Infrastructure Ready?	Reference
Material: 300mm SOI Uniformity	< 5nm	>10nm		Device Design Countermeasures	SOITEC
Material: Ge defects density	<1e6/cm^2	1e7~1e8/cm^2		Metrology, buffer strategy	[46]
Material: III-V (InGaAs, InP) defects density	<1e6/cm^2	>1e8/cm^2		III-V epi	[47]
Test Structures: Waveguide Loss	< 1dB/cm	Typical: 2-3 dB/cm <1dB/cm (Tradeoffs)		Yes (good etch tool)	[48]
Test Structures: Resonator Wavelength Uniformity	< 1nm	~1.5nm (in local areas on wafer)		Thermal Control	[49]
Test Structures: Electro-optic Modulator	E < 10fJ/bit B > 10 Gbit/s Mod. Depth >10dB	E = 5-50fJ/bit B > 10 Gbit/s Mod. Depth 3-10dB		Scaled CMOS Process and Device Design	[50]
Test Structures: Ge Photodetector	I_{dark} < 1nA/ m^2 B > 10GHz R > 0.9 A/W	I_{dark} < 1nA/ m^2 B > 40 GHz R > 0.8 A/W		Ge Growth and Process Development	[51]
Test Structures: Ge Laser	P > 1mW E < 100 fJ/bit	P ~ 1 mW E > 100 pJ/bit		Process and Device Optimization	[52]
Test Structures: III-V on Silicon Laser (Monolithic)	P > 1mW E < 100 fJ/bit	Bonded Lasers: P > 1mW, <3 pJ/bit		III-V Epi Required	[53]
Test Structures: Interconnects	>100 Gb/s	80Gbit/s (>0.6pJ/bit) 3Gbit/s (<200 fJ/bit)		Scaled CMOS Process and Device Design	[54]
Manufacturability Electronic-Photonic Integration	Monolithic / Heterogeneous	Hybrid		Not ready Material/Process	[54]

2.3 Basic Structure of Silicon Photonics

Silicon photonic is the ideal candidate for optical interconnects on chip for a variety of technological and economic reasons [22]. The compatibility to current CMOS industry and the low cost compared to III-V compounds or Lithium Niobate ($LiNbO_3$) are the main driven force for the development of silicon photonics.

Considerable work has been done on realizing silicon photonic devices. Passive devices have been demonstrated like splitters [23], ring resonators[24][25], disk resonators [26], and slot waveguide. Some examples of SOI based passive devices are shown as Fig. 2.5

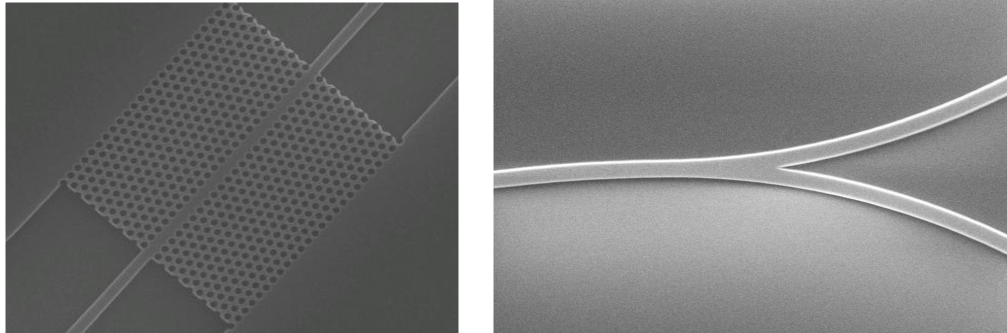


Fig. 2.5. Passive devices of silicon photonics

2.3.1 ***Silicon Waveguide***

A SEM picture and optical mode of standard Silicon waveguide are shown in Fig. 2.6. The waveguide is consisting of a Silicon core and silicon dioxide substrate and cladding. The refractive index of silicon is about 3.5 for photons with communication wavelength, while the index of silicon dioxide is about 1.5 [27]. This huge index contrast allows a compact optical mode as small as comparable to 400nm. In many cases, the height of the core is typically around half of the width. The high index contrast also allows lower radiation loss in sharp bending waveguide.

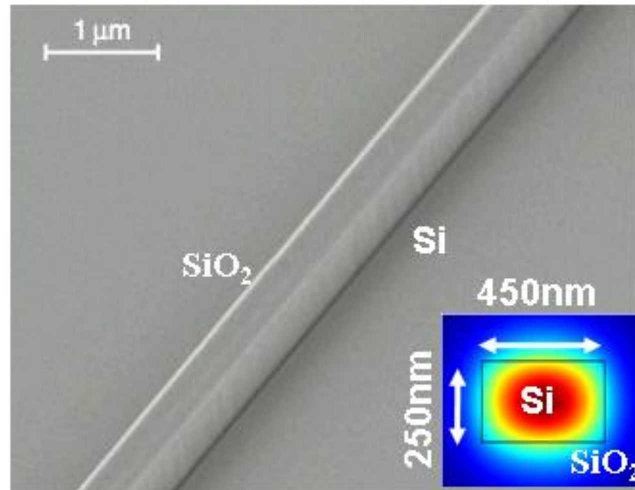


Fig. 2.6. SEM of Silicon waveguide and its supporting mode at 1550nm wavelength [28]

A silicon photonic waveguide is typically fabricated on SOI substrate. The Soitec SOI made with smart-cut technology have 3 microns of silicon dioxide between the substrate bulk silicon and top thin crystal silicon. The thickness of top thin crystal silicon ranges from 200nm to 300nm. The waveguide structure is patterned with - beam lithography or DUV lithography. After RIE etch is performed and silicon is fully or partially removed, 1-2 microns of silicon dioxide would be deposited on top as cladding for physical protection and supporting of optical mode.

2.3.2 *Directional Coupler*

Two waveguides that are close to each other will have interaction of their optical mode. Due to this property, directional coupler is developed as a basic element to combine and split signals in integrated photonic. A standard directional Coupler as shown in Fig. 2.7 is

composed by two waveguides that stay very close to each other in the coupling region, and two input ports and two output ports that is separated at each ends.

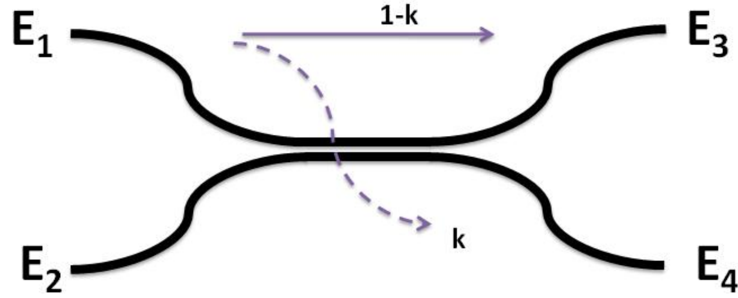


Fig. 2.7. Transmission coefficient for through and cross ports of a directional coupler

Assume the input electrical field of the two ports is E_1 and E_2, and the output electrical field of two ports is E_1 and E_2, the power cross coupling efficiency from one port to another is κ, then the power transmission efficiency of one waveguide from input to output becomes 1-κ. Then a matrix explains the electric field can be written as

$$\begin{bmatrix} E_3 \\ E_4 \end{bmatrix} = \begin{bmatrix} \sqrt{1-\kappa} & -j\sqrt{\kappa} \\ -j\sqrt{\kappa} & \sqrt{1-\kappa} \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \end{bmatrix} \tag{2.1}$$

It can also be written as

$$\begin{bmatrix} E_3 \\ E_4 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -j\sin(\theta) \\ -j\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \end{bmatrix} \tag{2.2}$$

If we assume $\kappa=\sin^2(\theta)$

If light is coupled into port 1 and then after transmission in the coupling region with a length Lc (power transfer length) the light energy will be fully coupled into the other waveguide. Then we can build relationship of output and input as:

$$E_3(x) = E_1 \cos(\theta(x)) = E_1 \cos(\frac{\pi}{2L_c} x)$$
$$E_4(x) = -jE_1 \sin(\theta(x)) = -jE_1 \sin(\frac{\pi}{2L_c} x) \qquad (2.3)$$

Then we can see if the coupling region length is odd times of the Lc, power will be fully transferred to the other waveguide, if the coupling region length is even times of Lc, power will maintain in the original waveguide. And if twice of coupling region length is an odd number, the directional coupler is a 3dB coupler.

2.3.3 ***Ring Resonator***

The ring resonator is basically a directional coupler which has feed back by closing a loop in one of the waveguides. The feedback causes the input optical signal to interfere with the delayed replica of itself [29].

Power coupling constant κ, round trip loss factor r and the feed delay time T, free spectrum range are the important quantities that determine their response. Power coupling constant is same as directional coupler mentioned in previous section.

The feedback delay is simply time of the light wave transport through total round trip length of the ring and it can be expressed as

$$T = \frac{Ln_g}{c} \tag{2.4}$$

Where L is total round trip length, n_g is group refractive index, and c is speed of light. Then if the waveguide loss is α in dB per unit length, then electrical field transmission after one round trip becomes

$$\gamma = 10^{\frac{-\alpha L}{20}} \tag{2.5}$$

Free spectral range (FSR) is the spectral size of each repetition of the periodic spectrum in frequency domain. It is simply the inverse of the feedback delay time of the ring:

$$FSR = \frac{1}{T} = \frac{c}{Ln_g} \tag{2.6}$$

The ring resonator is commonly used in digital filter due to its periodic nature. Here we model the ring resonator in z-domain with digital filter theory. A standard dual port ring resonator is shown in Fig. 2.8(a) where X_1 is the input, and Y_1 is the through port of the structure and Y_2 is the drop port of the structure [30]. And Fig. 2.8 (b) shows the SEM image of it.

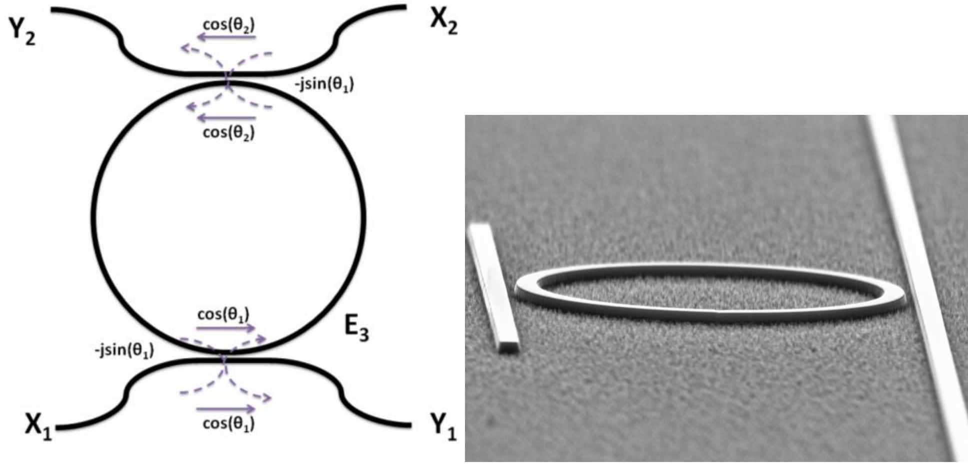


Fig. 2.8. (a) Configuration of duel port ring resonator, (b) SEM of duel port ring resonator

If we take $z=e^{j\omega T}$ then the output equation for Y_2 becomes

$$Y_2(z) = -\sin(\theta_1)\sin(\theta_2)\sqrt{\gamma z^{-1}}(1+\cos(\theta_1)\cos(\theta_2)\gamma z^{-1}+\cdots)X_1(z) \tag{2.7}$$

This transfer function can be simplified as

$$H_{21}(z) = \frac{Y_2(z)}{X_1(z)} = \frac{-\sin(\theta_1)\sin(\theta_2)\sqrt{\gamma z^{-1}}}{1-\cos(\theta_1)\cos(\theta_2)\gamma z^{-1}} \tag{2.8}$$

Likewise, equation for Y_1 becomes

$$Y_1(z) = \left[\cos(\theta_1) - \sin^2(\theta_1)\cos(\theta_2)\gamma z^{-1}(1+\cos(\theta_1)\cos(\theta_2)\gamma z^{-1}+\cdots)\right]X_1(z) \tag{2.9}$$

And can be simplified as

$$H_{11}(z) = \frac{Y_1(z)}{X_1(z)} = \frac{\cos(\theta_1)-\cos(\theta_2)\gamma z^{-1}}{1-\cos(\theta_1)\cos(\theta_2)\gamma z^{-1}} \tag{2.10}$$

And equation for one port ring resonator can be expressed as

$$H_{11}(z) = \frac{Y_1(z)}{X_1(z)} = \frac{\cos(\theta_1) - \gamma z^{-1}}{1 - \cos(\theta_1)\gamma z^{-1}} \tag{2.11}$$

Where $\cos(\theta_2)$ is simply 1.

2.3.4 ***Mach-Zehnder Interferometer***

The Mach-Zehnder interferometer, as an invention a hundred years ago, is a classic experiment in free space optics. The same theory can be applied in silicon photonic as shown in Fig. 2.9.

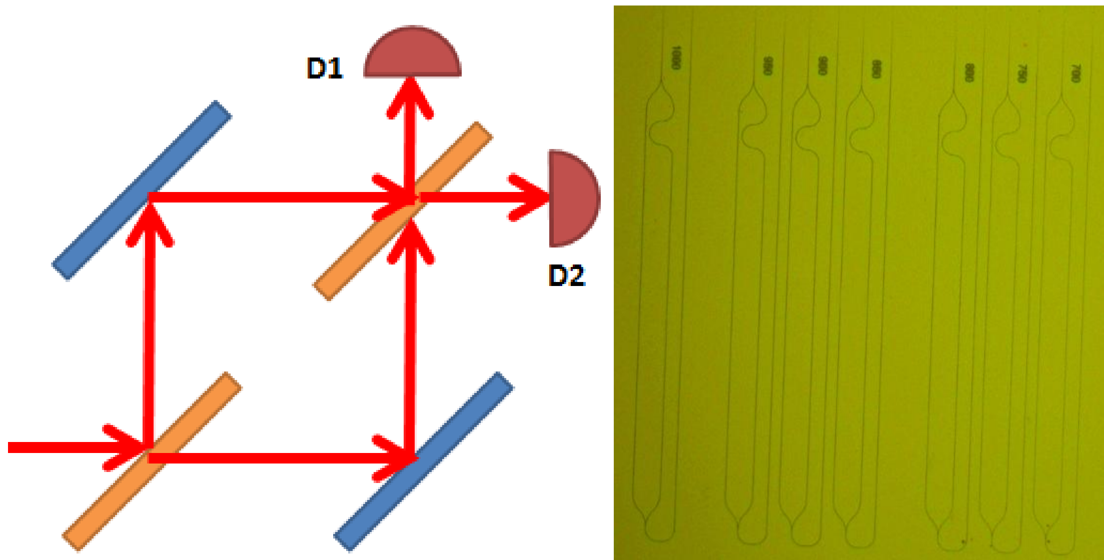


Fig. 2.9. MZI (a) Basic idea of MZI in free space optical path (b) Integrated MZI

Waveguide splitter (Y splitter) can divide the input waveguide evenly. We can express the propagating modes in the two arms as E_1 and E_2 respectively as:

$$E_1 = E_0 \sin\left(\omega t - \beta_1 z\right) \tag{2.12}$$

$$E_2 = E_0 \sin\left(\omega t - \beta_2 z\right) \tag{2.13}$$

The two arms in phase at the moment when they are just split, after transmitted for certain length, there phase might be different due to optical patch difference. Then the intensity at output waveguide would be

$$S_T = S_0\left\{E_0^2 \sin^2\left(\omega t - \beta_1 L_1\right) + E_0^2 \sin^2\left(\omega t - \beta_2 L_2\right) + 2E_0^2 \sin\left(\omega t - \beta_1 L_1\right)\sin\left(\omega t - \beta_2 L_2\right)\right\} \tag{2.14}$$

They can be rewritten as

$$\begin{aligned} S_T = \quad & S_0\left\{\frac{E_0^2}{2} + \frac{E_0^2}{2} + E_0^2\left[\cos(\beta_2 L_2 - \beta_1 L_1)\right]\right\} \\ & = S_0\left\{E_0^2\left[1 + \cos\left(\beta_2 L_2 - \beta_1 L_1\right)\right]\right\} \end{aligned} \tag{2.15}$$

Thus, intensity at output of MZI can be manipulated to be maximum or minimum by changing the phase difference of the two arms.

2.4 Modulation Mechanisms in Silicon

Modulating light using an electrical signal is an important functionality in any interconnects platform. Optical modulation can be applied to silicon photonic interconnects platform by changing the refractive index in three ways: Thermal-Optical Effect, Electric Field Effects and Plasma dispersion effect (free carrier injection or depletion).

Applying an electric field to a material can result in a change of the real and imaginary part of optical refractive index. Common electric field effects used in semiconductor materials include the Pockels effect, Kerr effect and Franz-Keldysh effect [31]. Due to the symmetric crystal structure of silicon, silicon doesn't have Pockels effect unless the symmetry of the crystal lattice is broken by stress [32]. Franz-Keldysh effect is an electro-optic absorption effect that the band gap of the silicon (Eg=1.12 e.V.) shifts with an applied electric field. However, band gap wavelength of silicon is around 1.1 μm, it makes that no pronounced change at the desirable telecom wavelength of 1.3 μm or 1.55 μm. Kerr effect as a second order electric field effect presents in the silicon although it is relatively weak [33]. The refractive index change by Kerr effect can be expressed as

$$\Delta n = s_{33} n_0 \frac{E^2}{2} \tag{2.16}$$

Where s_{33} is the Kerr Coefficient, n_0 is the unperturbed refractive index, and E is the applied field.

Changing the concentration of free charges can change the refractive index of material through what is known as the plasma dispersion effect. Drude-Lorenz equation gives the relation of concentration of electron and holes to absorption and refractive index as [34]

$$\Delta\alpha = \frac{e^3\lambda_0^2}{4\pi^2 c^3 \varepsilon_0 n}\left(\frac{N_e}{\mu_e\left(m_{ce}^*\right)^2} + \frac{N_h}{\mu_h\left(m_{ch}^*\right)^2}\right) \tag{2.17}$$

$$\Delta n = \frac{-e^2\lambda_0^2}{8\pi^2 c^2 \varepsilon_0 n}\left(\frac{N_e}{m_{ce}^*} + \frac{N_h}{m_{ch}^*}\right) \tag{2.18}$$

For communication wavelength (1550nm) light in silicon, the equation becomes

$$\Delta n = -\left[8.8\times10^{-22}\times\Delta N + 8.5\times10^{-22}\times\Delta P^{0.8}\right] \tag{2.19}$$

$$\Delta\alpha = -\left[8.5\times10^{-18}\times\Delta N + 6\times10^{-18}\times\Delta P\right] \tag{2.20}$$

The plasma dispersion effect is important in silicon photonic mainly because it provides direct connection between electronics and optics by simple structures as P-I-N diode [35][36][37], Schottky diode [38], or MOS Capacitors [39].

Thermo-optic effect is another way to tune the refractive index of silicon [40]. The thermo-optic coefficient in silicon at room temperature is

$$\frac{dn}{dT} = 1.84\times10^{-4}K^{-1} \tag{2.21}$$

In this way, large refractive index change of 0.001 can be achieve in a broadband wavelength by simply warm up the waveguide by 6 ℃. The only drawback is the slow modulation speed because of the slow dissipation of thermal energy. Need to point out that during carrier injection modulation, thermo energy would be generated to heat up the

waveguide region. And instead of decreasing refractive index offered by carrier injection modulation, thermo-optical effect will increase the refractive index. Therefore, a good design is required when making the modulator.

2.5 Numerical Simulation Methods

2.5.1 *Fine-Difference-Time-Domain Method*

Finite-Difference-Time-Domain (FDTD) is a powerful simulation technique for solving electromagnetic problems by numerical approximations to Maxwell's equations. A basic algorithm used in 1D FDTD simulation is shown as below [41].

Assume one dimensional TEM wave propagating along the *x* axis. Point form of Maxwell's equations can be written as follows.

$$\mu \frac{\partial H_y}{\partial t} = \varepsilon \frac{\partial E_z}{\partial x} \tag{2.22}$$

$$\varepsilon \frac{\partial E_z}{\partial t} = \mu \frac{\partial H_y}{\partial x} \tag{2.23}$$

After nodes in time and space is created, numerical derivatives can be used to calculate the field evolution at a point *m* in space with time *(n+1)* from the spatial information of the surrounding fields *(k+1/2)*,*(k-1/2)* at times *n*,*(n+1/2)*. Repeat the same algorithm for

different nodes can update fields in both time and space. Fig. 2.10 shows the order for calculating different fields in one dimensional problem.

$$E_z^{n+1}\left[k\right]=E_z^{n}\left[k\right]+\varepsilon\frac{\Delta t}{\Delta x}\left[H_y^{n+\frac{1}{2}}\left[k+\frac{1}{2}\right]-H_y^{n+\frac{1}{2}}\left[k-\frac{1}{2}\right]\right]$$ `(2.24)

$$H_y^{n+1}\left[k\right]=H_y^{n}\left[k\right]+\frac{1}{\mu}\frac{\Delta t}{\Delta x}\left[E_z^{n+\frac{1}{2}}\left[k+\frac{1}{2}\right]-H_z^{n+\frac{1}{2}}\left[k-\frac{1}{2}\right]\right] \quad (2.25)$$

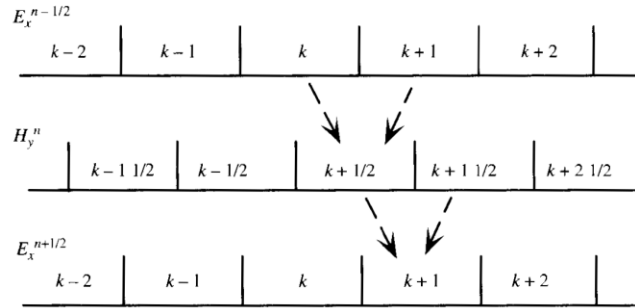


Fig. 2.10. Field evolution order in 1D-FDTD problem [42]

The algorithm can be used to solve 2D and 3D problems by considering their respective derivatives in space. Commercial software like Lumerical is used to do all the 2D or 3D FDTD simulations in this work.

2.5.2 ***Beam Propagation Method***

Beam Propagation Method is another simulation method that is applied to solve guiding wave problems [43]. A general form of optical wave can be expressed as Helmholtz equation

$$\left(\nabla^2 + k_0^2 n^2\right)\psi = 0 \tag{2.26}$$

A solution of this equation can be

$$E\left(x, y, z, t\right) = \psi\left(x, y, z\right)\exp\left(-jwt\right) \tag{2.27}$$

Spatial dependence of the field can be written as

$$\psi\left(x, y\right) = A\left(x, y\right)\exp\left(+jk_0 vy\right) \tag{2.28}$$

Here we approximate that the envelope A(x,y) follows a slowly varying approximation

There for the solution becomes

$$\left[\frac{\partial^2}{\partial x^2} + k_0^2\left(n^2 - v^2\right)\right]A\left(x, y\right) = \pm 2jk_0 v\frac{\partial A_k\left(x, z\right)}{\partial z} \tag{2.29}$$

By computing the function A(x,y) for all space, the $\psi\left(x, y\right)$ can be reconstructed. And because the method is based on time-harmonic Helmholtz equation, calculation only needs to be done in one time period, and the field along transportation direction and be visualized easily[44]. This method can be used to give a quick idea of one direction propagation structure with slow changing like MMI, directional coupler and Y splitters. Commercialized tool based on BPM like RSoft BeamPROP [45] is used in this work.

3 Design of 300mm Silicon Photonic Library

As discussed in chapter 2, current copper interconnects have a fundamental limit of latency and bandwidth and cannot meet the future requirement of semiconductor chip production. There is an urgent demand to develop on-chip optical interconnects. While Through Silicon Via (TSV) can shorten the distance from layer to layer, there is still demand for interconnects on the same layer of the chip, which we propose as a key strength of optical interconnects.

This chapter mainly talks about the work done to introduce silicon photonic fabrication to the state-of-the-art 300 mm processes. A CMOS compatible process flow is introduced in the beginning. And then, important elements like ring resonators and modulators are presented. Germanium based detectors and lasers are also included. WDM systems with both detector and modulator integrated are presented. And finally optimized grating coupler and a high efficiency chip to chip packaging design is demonstrated.

3.1 300mm Process Flow Design

As mentioned in section 2.2, the current silicon photonic research is still far away from real commercialization with multiple problems including the SOI substrate, integration of detector and laser, among others. We had a chance to collaborate with SEMATECH to develop

silicon photonic in the state-of-the-art foundry using newly developed 300mm SOI wafer with thick buries oxide. A process flow that integrates germanium detector and laser with active silicon devices is presented.

The process flow is based on the standard CMOS process flow with three metal layers in SEMATECH. A basic mask setting is shown in Table. 3.1, where 17 masks are used in total. Additionally, Fig. 3.1-Fig. 3.4 tell the detail of the fabrication process.

Table. 3.1. Mask Setting

ITEM #	0	1	2	3	4	5
Description	Zero level	PolyMesaEtch	Pwell	Nwell	DeepNwell	Active
Field Tone	DK	CL	DK	DK	DK	CL
CD on Tape	0.5	0.2	0.2	0.5	0.2	0.2
GDS#	2	55	23	1	33	22
ITEM #	6	7	8	9	10	11
Description	N+ Implant	P+ Implant	Active-2	P+ Implant-2	Poly gate	Silicide Blocking
Field Tone	DK	DK	DK	DK	DK	DK
CD on Tape	0.5	0.5	0.5	0.5	0.2	0.5
GDS#	7	8	25	82	5	59
ITEM #	12	13	14	15	16	
Description	Metal-2 (Heater)	ContactP	ContactN	SiMContact	Metal-1	
Field Tone	DK	DK	DK	DK	DK	
CD on Tape	0.2	0.5	0.5	0.2	0.2	
GDS#	12	13	9	11	10	

The fabrication process starts from a SOITEC 300mm SOI wafer. Mask#0 is used to make alignment marks for future patterning. Very thin oxide (10nm-20nm) is deposited after 170nm of polycrystalline silicon. The thin oxide is deposited here for protection of

crystal silicon while etching the polysilicon. Mask #1 is used to pattern the polysilicon. The polysilicon is mainly used as additional height for grating structures (Section 3.7.2), and it is also exploited as transfer media between lasers and waveguides (Section 3.5). After the pattern of photoresist, polysilicon is etched by plasma, and the thin oxide is wet etched to leave smooth crystal silicon. In most areas, screening Si_3N_4 of 50A is then deposited as the passivation for future ion implantation. From step 2 to 4, ion implantation of boron and phosphorus of different doses and powers will be implanted with pattern masks #2, #3, and #4. Then, the screening Si3N4 is removed by wet etches, and hard mask of thicker Si_3N_4 with SiO_2 is deposited. Mask # 5 is used to pattern the crystal silicon part. Crystal silicon is the main role here that composes the main part of the waveguide and growth substrate of Germanium. After the patterning of crystal silicon, the hard protection mask is kept there. Mask #2 is used again for additional doping of Boron implant for the electric connection between the contact region and the active region. After stripping off all photoresist and depositing silicon nitride, Masks #6 and #7 are used to dope the N+ and the P+ regions.

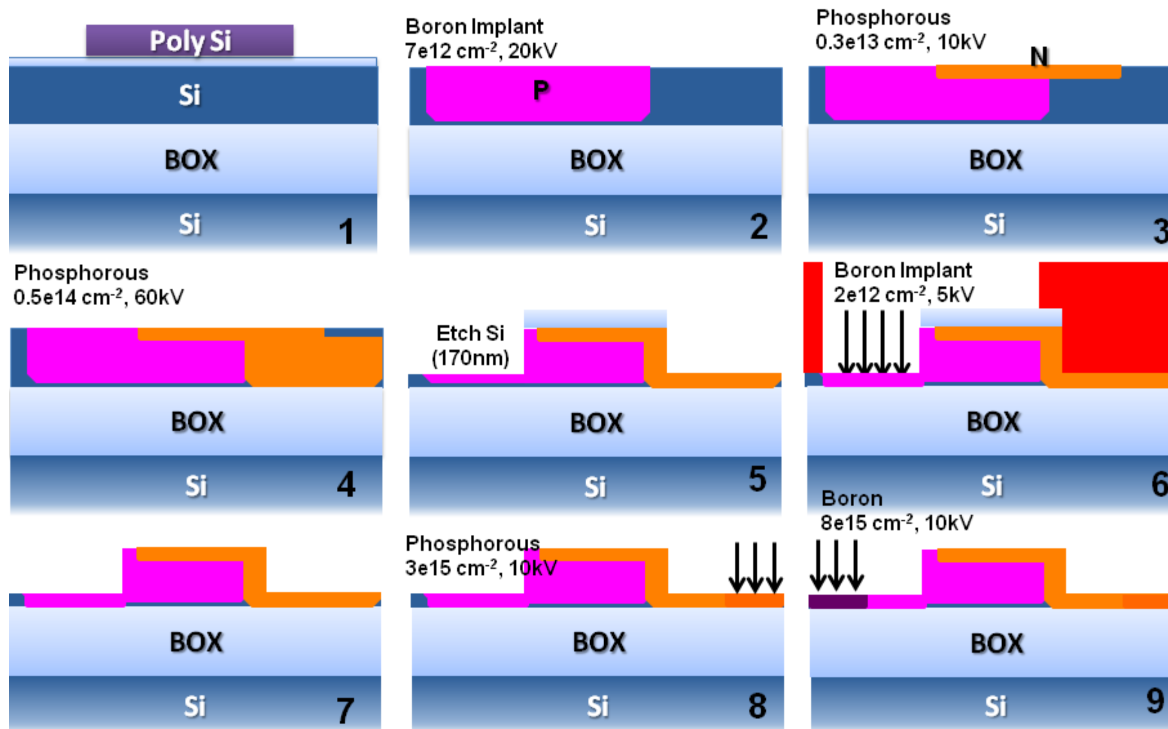


Fig. 3.1. Process flow #1: 1. Begin with 300mm SOI wafer, deposit very thin Oxide and 170nm polysilicon, and then patten the polysilicon, etching away both polysilicon and thin oxide. 2. Pattern and implant Boron for Pwell doping. 3. Pattern and implant phosphorous for Nwell doping. 4. Pattern and implant phosphorous for deep N doping. 5. Pattern (450nm Wide) and etch 175nm Silicon to form optical waveguide. 6. Pattern and implant boron for p+ doping. 7. Strip off oxide hard mask over waveguide. 8. Pattern and implant phosphorous for n++ doping. 9. Pattern and implant boron for p++ doping

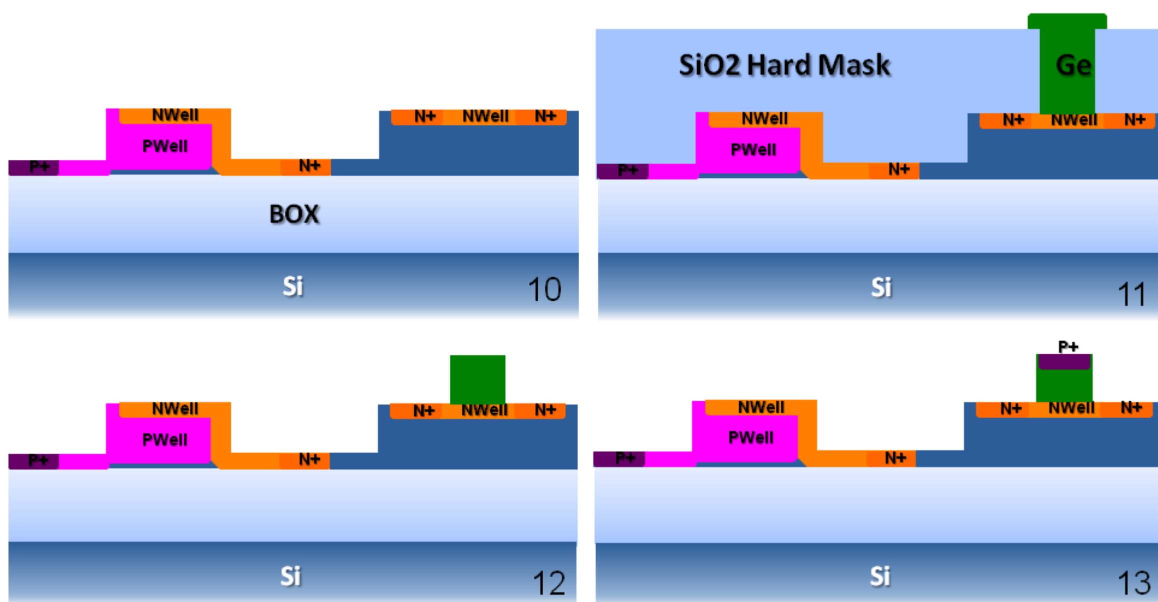


Fig. 3.2. Process Flow #2: 10. Rapid thermal anneal for implant activation. 11. Clad SiO2 hard mask and pattern holes to epitaxial Germanium. 12. CMP for form flat Germanium and then wet etch hard maks. 13. P+ doping over Germanium.

After stripping off all the photoresist and screening layer in step 10, an oxide hard mask of 500-600 microns is deposited and Chemical Mechanically Polished (CMP) , followed with 30 sec of Rapid Thermal Annealing with target temperature of 1100 ℃ to activate all the dopings in silicon. Mask #8 is used to pattern holes for Germanium growth. The uncovered oxide will be etched away leaving crystal Silicon substrate. Then 500nm Germanium is deposited in Ultra High Vacuum CVD with 50nm of SiGe buffer layer to avoid lattice mismatch. The Mask #9 is then applied to dope Boron on Germanium in step 13 after CMP. Another rapid thermal annealing at 450 ℃ is applied to activate the doping in Germanium.

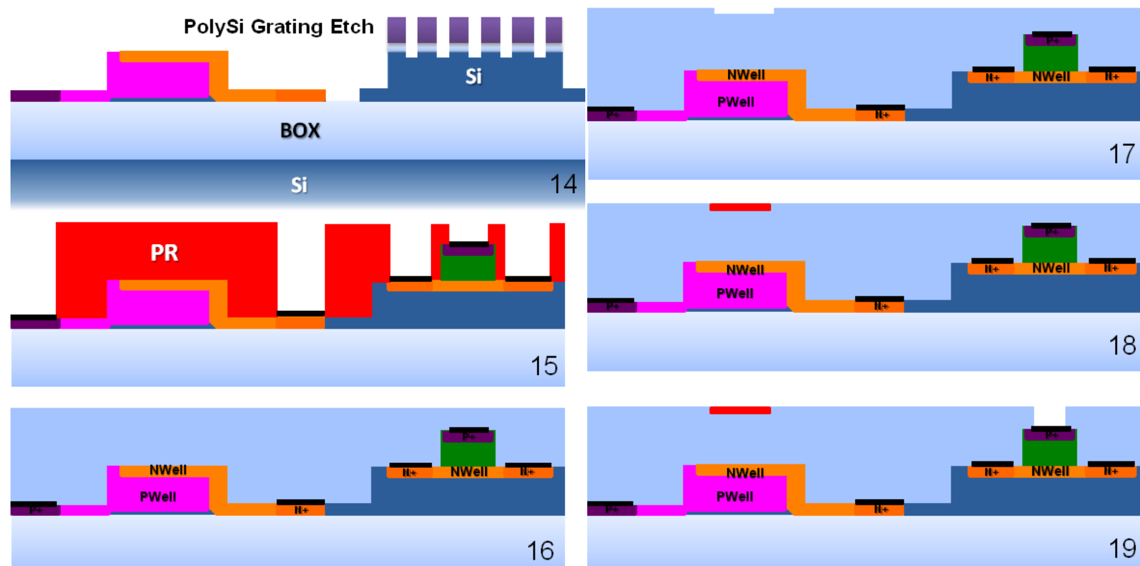


Fig. 3.3. Process Flow#3: 14.Pattern grating etch and do multiple etches to form the grating. 15. Pattern and deposit Nickel for contact and thermally grow Nickel-Silicide. 16. Deposit 1microns of oxide for cladding. 17

Etch channels in oxide for heaters. 18. Deposit TiN and CMP. 19. Pattern and etch oxide for Germanium contact.

In step 14, a poly-oxide-silicon step etch is used to etch the grating structures with Mask # 10. In many areas, this process is also used to etch the crystal silicon to make electric or thermal isolations. Mask # 11 is then used to open the contact areas. 10-15nm Nickel is deposited in the open areas. Rapid thermal annealing at 400 is used here to make Silicide or Germenide for Ohmic contact. The inactivated Nickel is then etched away with wet chemicals. After step 15, 1-1.5 microns of oxide is deposited on the whole wafer and followed by a CMP process. Mask # 12 is used to open 100nm channels on the thick cladding oxide. After depositing of TiN, CMP process is applied to leave TiN only at the channel region. Then thin oxide is used to cover the TiN. TiN is used to form the heaters due to their high resistivity.

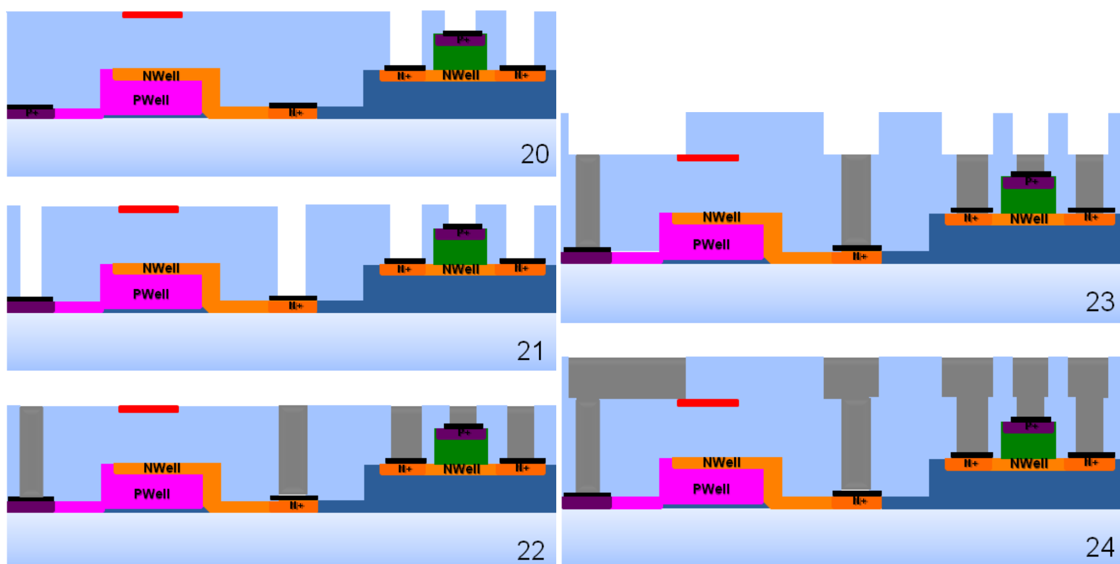


Fig. 3.4. Process Flow #4: 20. Pattern and etch oxide for Silicon level contact. 21. Pattern and etch oxide for Silicon Modulator contact. 22. Deposit Copper and CMP. 23. Pattern oxide channel for metal pad. 24. Deposit Copper and CMP

A standard Damascene [55] [56] process is used here for copper interconnects. In this process, the Masks # 13-15 are used to pattern the open trench where the conductor should be. Thick copper overfills the trenches. After that, chemical-mechanical planarization (CMP) is used to remove the additional copper to level the oxide surface. Finally, another Damascene process is used to define the big contact pads and all the connection wires.

3.2 **Ring Resonators**

As the basic building block of modulators, switches and filters, small size rings are important in the photonic interconnects system. Not only can smaller individual ring create a more dense interconnects system, but also power consumption of modulators can be reduced with the smaller size of the ring, and an important factor is that the smaller ring will offer larger free spectral range (FSR), which makes it easier to fit more wavelength channels in the micro-ring based WDM systems. Researchers have demonstrated 1.5microns radius ring resonators[57]. However, this work is done based on a fully etched waveguide system, which cannot be used to make modulators, and the thickness of the SOI wafer is slightly different (from 250nm to 220nm).

The total quality factor (Q) of the ring is determined by various issues including bending loss, intrinsic loss, coupling loss, etc., as the following equation demonstrates:

$$\frac{1}{Q} = \frac{1}{Q_{\text{int}\,rinsic}} + \frac{1}{Q_{bend}} + \frac{1}{Q_{coupling}} + \cdots \tag{3.1}$$

The ridge waveguide, as the foundation of modulators, will suffer more bending loss than the fully etched waveguide. Therefore, a series of FDTD simulation is done to learn the bending loss as shown in Fig. 3.5(b). Obviously, when the radius is smaller than 4 microns, the loss mainly comes from bending; when the radius is larger than 4 micron, other issues start to play a more major role. From the loss study, a 4 microns ring can both have high Q and small size. The 5 microns ring is a safer choice for high Q, while the 3 microns ring is still possible to achieve a Q of 10000.

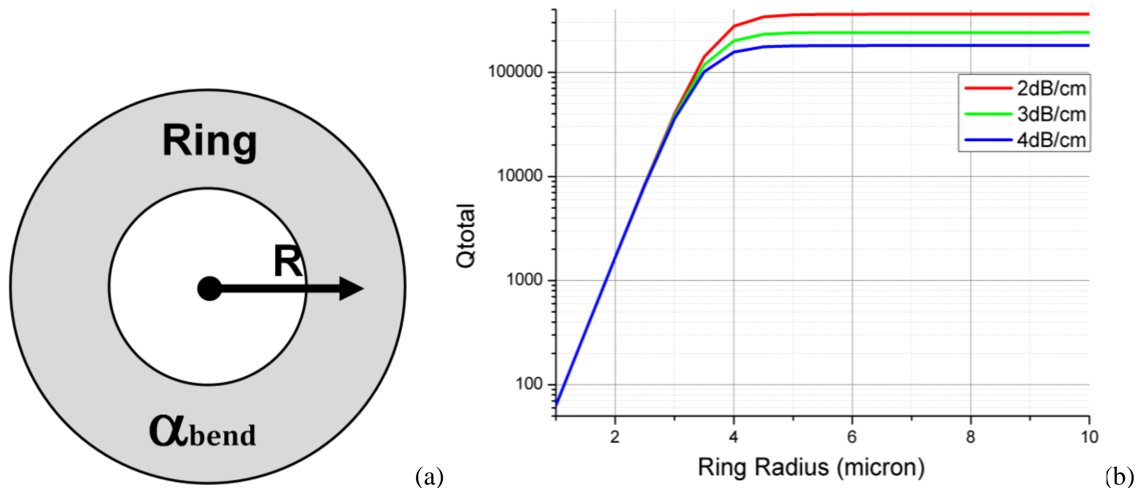


Fig. 3.5. (a) Ring resonator (b) Quality factor Vs Ring radius

The good modulator should have high extinction coefficient and high Q at the same time. We can tune the $Q_{coupling}$ by controlling the gap between the ring and waveguide; we can also tune it by changing the width of waveguide width. Simulation is done based on the simulated intrinsic Quality factor, and coupling efficiency for 3 microns ring resonator. The basic code of the simulation is attached in Appendix I. As we noticed in Fig. 3.6(b), with a larger gap there is a higher quality factor. However, the high extinction only happen when the coupling loss is equal to the transmission loss; therefore, the fabrication need to be very accurate to get high extinction.

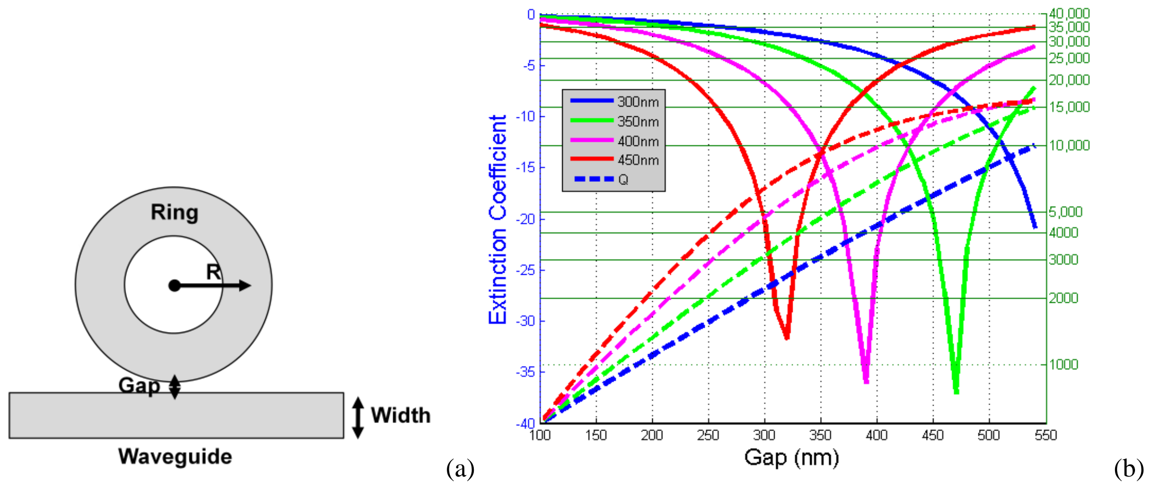


Fig. 3.6. (a) Ring resonator with through port (b) Extinction and Quality factor at different gap and width

A Ring resonator with dual port is then simulated in Fig. 3.7. The additional waveguide has an identical gap to the first waveguide for easier design. As mentioned before, the best extinction happens when coupling loss equals the other loss. When we think about transmission in one waveguide, the coupling loss caused by the other waveguide now

belongs to the other loss. Therefore, the other loss is always larger than the coupling loss. And the other loss can match the coupling loss better if the coupling loss is larger, and this can bring a higher extinction value. And we can see in Fig. 3.7(b) that in a broad gap tuning region, we can maintain high extinction and good quality factor. This would be a very good start point of a modulator design. And for the dual port ring resonator, when it is on resonance, the drop port will have a signal while the through port will not, and behavior will be reversed as it is not on resonance. Thus, the high extinction dual port ring resonator is the perfect candidate for routers or switches.

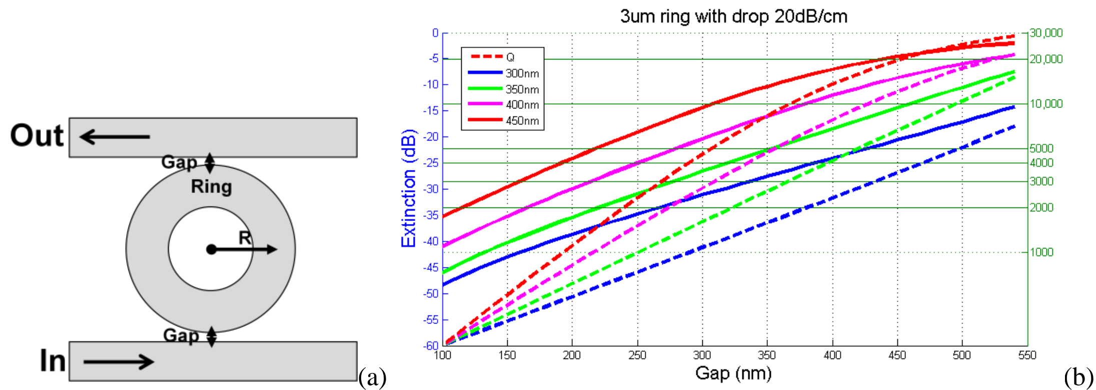


Fig. 3.7. (a) Ring resonator with dual ports (b) Extinction and Quality factor at different gap and width

3.3 Electro-Optical Modulators

As mentioned in section 3.3, plasma dispersion effect can be the only realistic effect that can make modulators in this project. A standard forward biased PIN diode modulator is shown in Fig. 3.8. The ridge waveguide area is the intrinsic region while the slab has high

doping with holes or electrons on each side. When the diode is forward biased, the injected carrier density in the ridge region can be several orders of magnitude higher than intrinsic level. Therefore, a larger refractive index change in the ridge region can be achieved. However, with the large carrier concentration on forward biased status, a very large absorption is unavoidable. And the slow recombination efficiency makes that it can hardly recover from the "ON" status, therefore, there is always a speed limit for modulator of this kind.

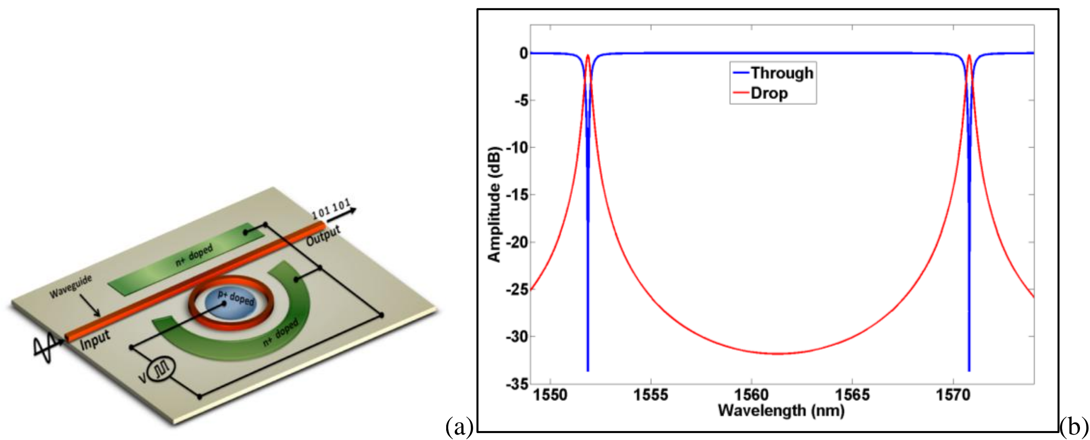


Fig. 3.8. (a) Forward biased PIN diode (b) Spectrum of through port and drop port of switch based on forward biased PIN diode

Although the speed limit exists, with proper design, the forward biased PIN modulator can still reach a speed of 10-50GHz. And a forward biased PIN modulator based on dual port ring resonator can be a good switch or router. If we keep the resonator to be "ON" when no carriers are injected, photons can pass to the "drop port" without getting much absorption in

the cavity. And when carriers are injected, the resonator is on “OFF” status, then photons will pass to the "through port" without getting trapped and experiencing carrier absorptions in the cavity as shown in Fig. 3.8(b). According to the designed process flow, modulators based on forward biased PIN diode with different ring sizes, gaps and doping regions are designed, and a basic PIN modulator design is shown as Fig. 3.9, where only the P+ and N+ doping levels are used.

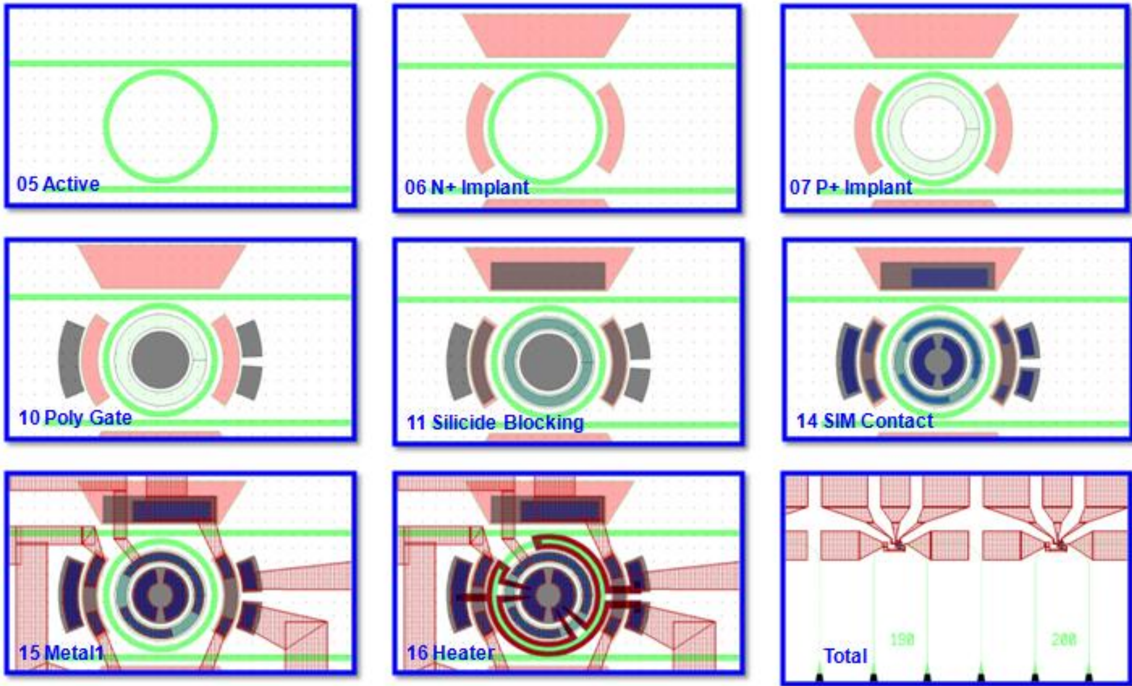


Fig. 3.9. PIN diode CAD design

Reverse biased PN diode modulator, can ideally run at a higher speed than forward biased PIN diode modulator mainly because that the carriers are driven by voltage depletion instead of diffusion. Because holes have much stronger effect on refractive index than

electrons, this design mainly focuses on deplete the holes in Ridge region of the waveguide. And five levels of doping design would form the doping effect as Fig. 3.10. The simulation is run on commercial software Silvaco Atlas.

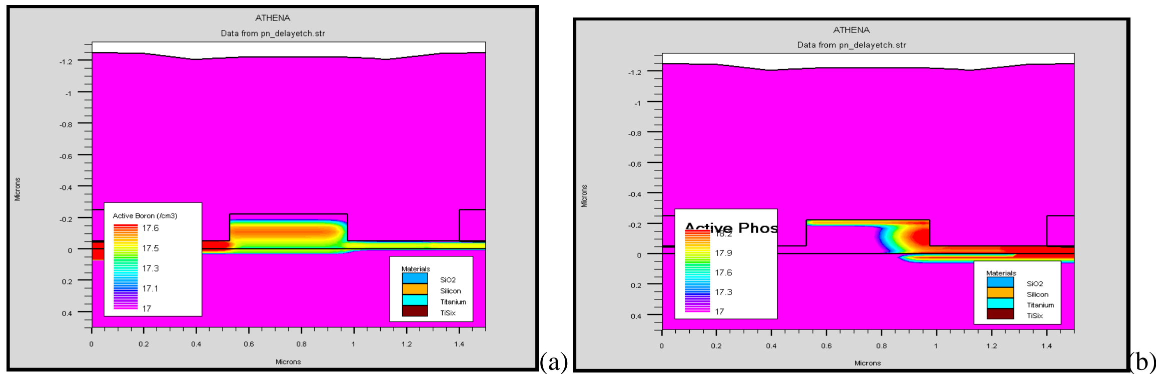


Fig. 3.10. Doping level of PN depletion modulator

Here Pwell mask is used both before and after the etching of waveguide structure with different dose and energy to make sure a good electro connection between the ridge region and contact region.

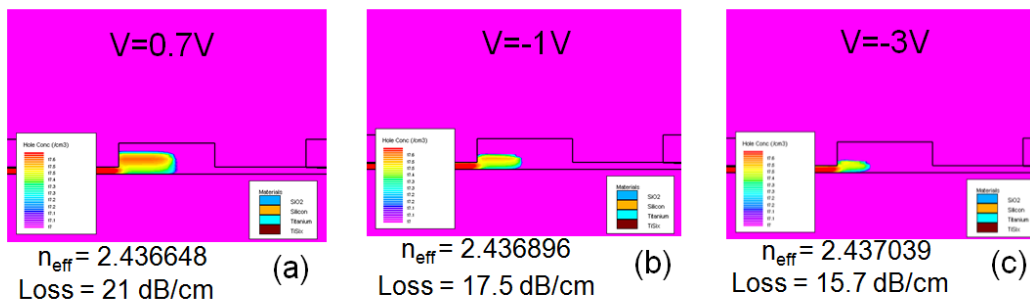


Fig. 3.11. Carrier concentration at (a) 0.7V (b)-1V (c) -3V

Then Silvaco simulations of carrier concentrations under different driving voltages are shown as Fig. 3.11. The distributions of carriers are then exported to Lumerical, through

Matlab for mesh condition matching. The effective refractive index and loss is shown in Fig. 3.11.

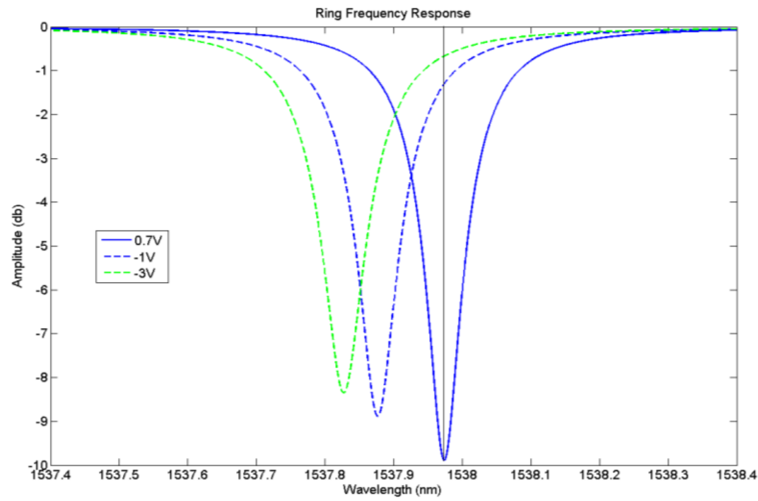


Fig. 3.12. Ring resonator with PN modulator at different condition

Finally, the effective refractive index and loss information can be used in the ring resonator spectrum simulation. Result in Fig. 3.12. shows an 8dB extinction and 1dB insertion loss can be achieved when we apply -1V bias voltage.

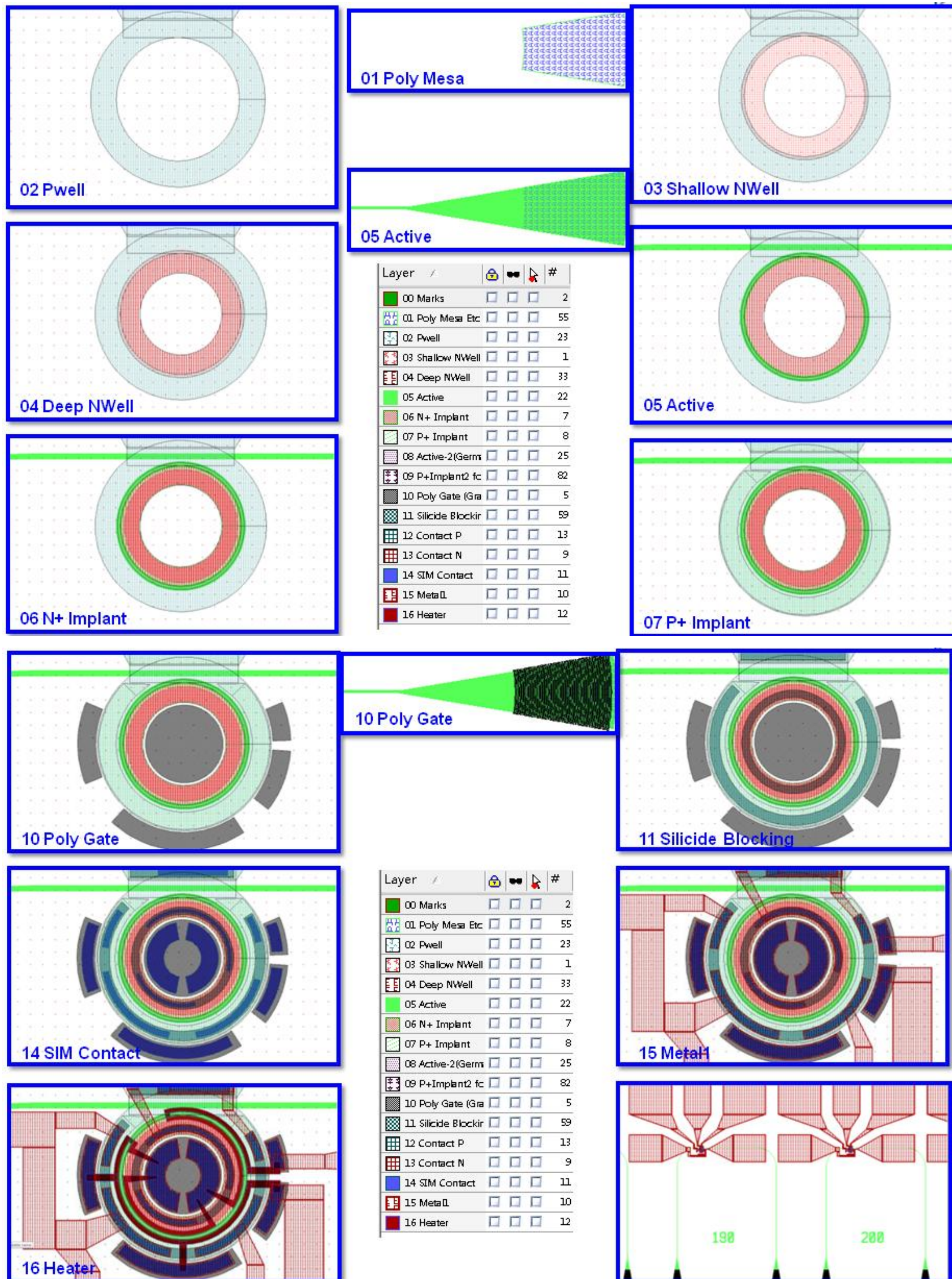


Fig. 3.13. CAD Design of PN depletion mode modulator

Based on the designed process flow, reverse biased PN diode modulators with different ring sizes, gaps and doping regions are designed. In addition, a basic reverse biased PN diode modulator design is shown as Fig. 3.13.

3.4 Germanium PIN Detector

Due to its large band gap, silicon can be a perfect guiding material at telecom wavelengths. For the same reason, silicon cannot be used as a detecting material at same wavelengths. Conventional optical detectors are made by III-V compound materials due to their excellent absorption properties [58]; however, integration of III-V materials to silicon platforms is still a lion in the way. Germanium, an IV group material with pseudo-direct band-gap energy of ~0.66eV, is another excellent material for detecting optical signal at fiber communication wavelengths [59]. And people have successfully integrated Germanium detectors over SOI platforms [60].

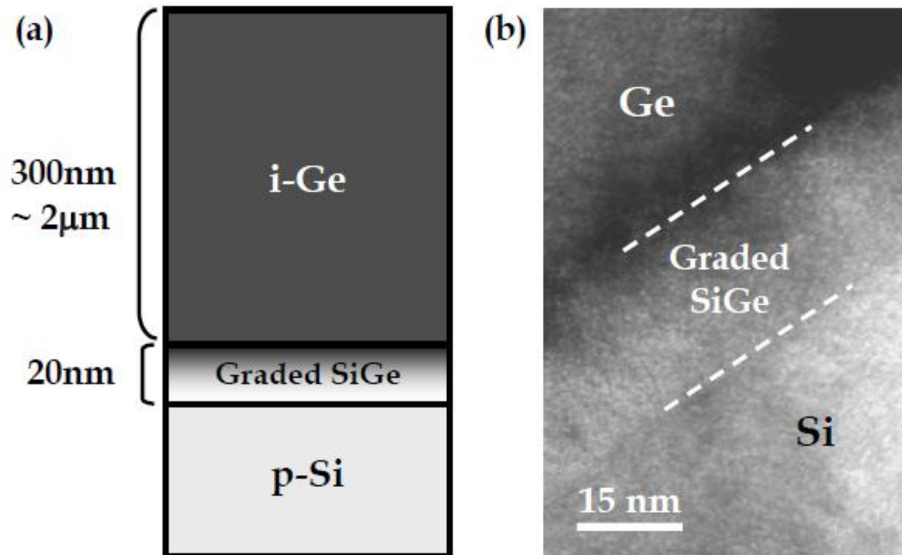


Fig. 3.14. Cross-section view of layer stack for the direct hetero-epitaxial growth of Ge on Si[61]

Integrate germanium over silicon has two challenges: (1) huge lattice mismatch between silicon and germanium, (2) low processing temperature is required for not bring bad affects over done processes. The best solution is performed by an ultra-high vacuum chemical vapor deposition (UHVCVD) reactor. In this process, a 20nm thick grading (Ge mole fraction grade from 10% to 50%) SiGe buffer is firstly deposited to relieve large lattice mismatch stress between silicon and germanium. Then 30nm of Ge seed layer is grown on the SiGe buffer under process temperature of 370 ℃. After getting the smooth Ge seeding layer, faster speed epitaxial of Ge can be processed under higher temperature (400C to 550C) [61]. The TEM image of the buffer SiGe can be seen in Fig. 3.14.

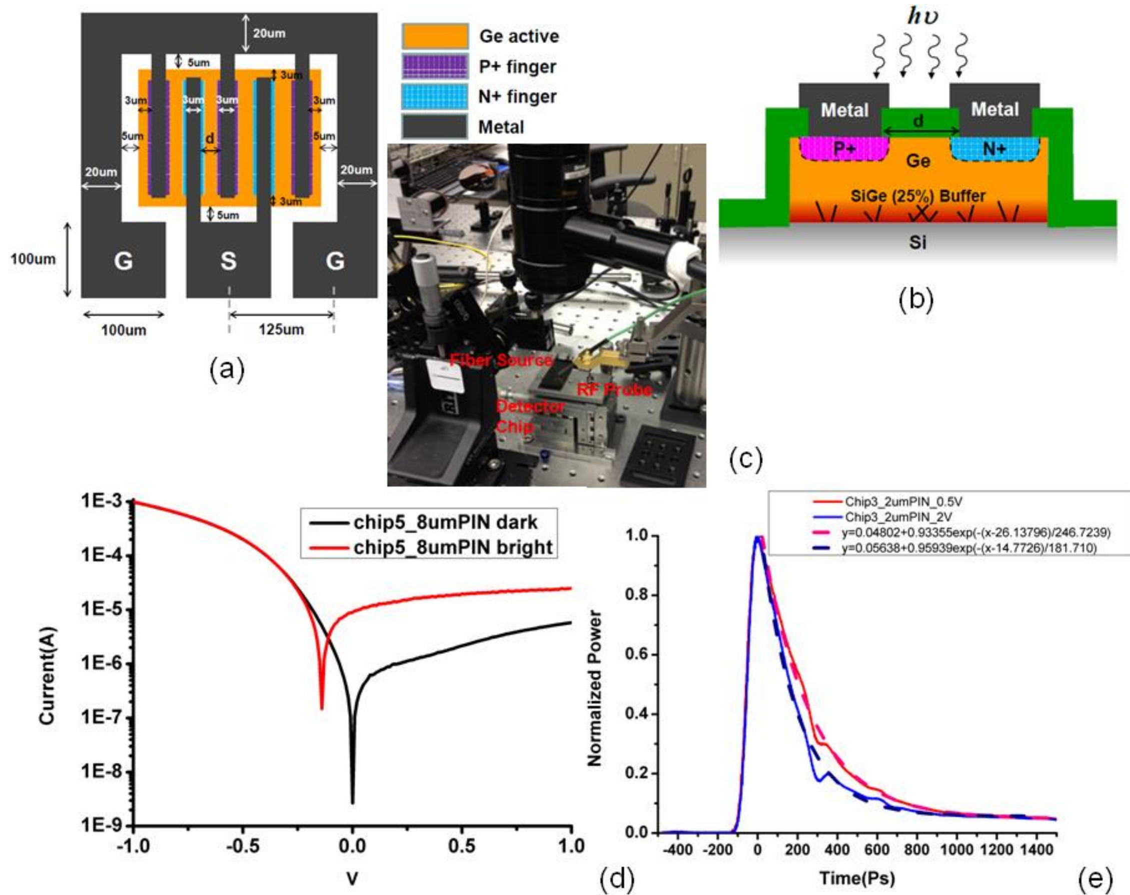


Fig. 3.15. (a) basic configuration of lateral detector. (b) Cross-section of PIN detector. (c)Test setup (c) Dark current performance. (d) Time response performance

To prove the quality of the low thermal budget Germanium integration technique, an experiment is launched based on a bland silicon wafer. After epitaxial of 280nm Germanium over the 300mm silicon wafer with 50nm buffered SiGe, the wafer is then broken into small pieces. And then lateral PIN photo detectors are made in CNF on these pieces with contact lithography technique as shown in Fig. 3.15. The PIN diodes are tested under an 1550nm wavelength fiber source (increasing coupling efficiency) with applied bias of 0.5V. The lowest measured dark current is 1.5μA with 100 x 100 microns Mesa

($0.15nA/um^2$). Optical input of 1mW can yield a current of 50μA, given that there is at least 3dB loss due to fiber coupling reflection and polarization, and 280nm is not sufficient to fully absorb the photons came in. Time response is performed as Fig. 3.15(e), where 250ps response time is achieved under 0.5V (4GHz). Several issues both exist and limit the performance of the fabricated devices including large misalignment due to manual alignment, and large minimum features (2-3microns) due to limited resolution of contact lithography. Better performance can be achieved with advanced lithography techniques. In addition, if we integrate germanium detectors with SOI waveguides, better quantum efficiency can be achieved due to much longer coupling lengths.

The benefit of the in-plane coupling detector is that you can always get 100% coupling efficiency if you make the coupling region long enough. However, there is a tradeoff between high speed and high coupling efficiency. So we need to optimize the device to get optimum coupling in relatively shorter distance and smaller width. A basic configuration of the FDTD simulation is shown in Fig. 3.15(a) where a germanium block is placed over 220nm silicon block and a standard 450nmX220nm silicon waveguide is connected to them. We use a straight waveguide here instead of mode expanding taper based on simulation results that straight waveguide always have better coupling efficiency than the tapered version. And because germanium (~4) has higher refractive index than silicon (~3.5), the

optical mode of the designed structure would gradually transfer from silicon region to germanium region and finally be absorbed by germanium and generate electric current in the circuit. Fig. 3.16(c) shows the transmission spectrums at different wavelengths. As we noticed, transmission at larger wavelengths is higher. This explains the fact germanium has a larger absorption coefficient at a lower wavelength at communication wavelength range. Fig. 3.16(d) shows the different spectrums when we vary the thickness of the germanium block. The thicker germanium block designs have better absorption performance. However, this enhancement is not dramatic, so the thickness of germanium block is not our main concern in the device design. And here we choose 500nm as our thickness parameter. Then spectrums of different germanium block widths with 0.45micron, 0.8micron, 1micron, 1.5microns, 2microns and 2.5microns are shown in Fig. 3.16(e). We notice a big absorption enhancement at 1.5microns. With 1.5 microns width, 90% of light is absorbed within 30microns at the wavelength of 1550nm. And device width thicker than 1.5microns has comparatively less enhancement at spectrum performance.

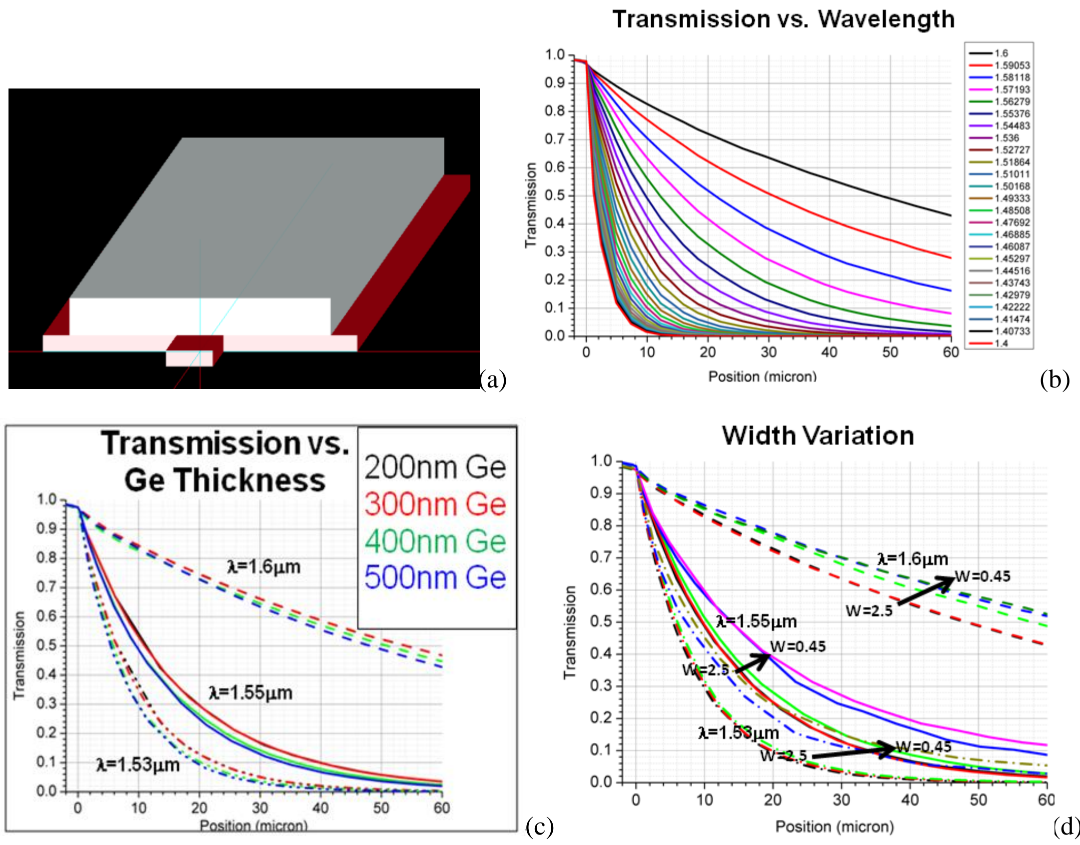


Fig. 3.16. Germanium detector simulation (a)Configuration of simulation (b)Transmission VS coupling length at different wavelength (c) Transmission VS Germanium thickness (d) Ttransmission Vs width variation

We also need to investigate the metal influence of absorption performance since most metals are also good absorbers of photon. To estimate this effect, another simulation is done by putting a 1micron long copper piece over the 0.45 micron germanium block as shown in Fig. 3.17(a). Result shows that the metal piece can bring 15% additional absorption. To avoid this additional absorption by metal, smaller size metal blocks are preferred. In addition, structure of wider and thicker germanium block with smaller metal blocks on top can also help to reduce additional metal absorption.

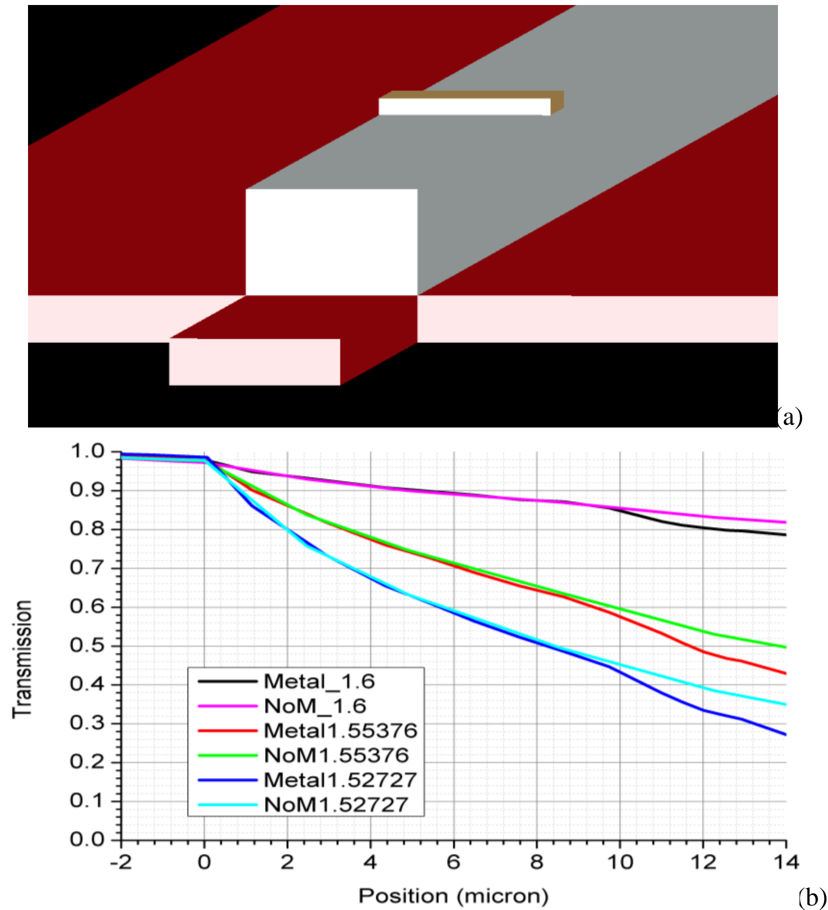


Fig. 3.17. (a) Metal block absorption setup (b) Spectrum comparing with metal and without metal

There are two kinds of PIN detector structures as shown in Fig. 3.18. The vertical structure is experimentally proved to have better performance due to thinner width and height of the intrinsic germanium region. Additionally, the vertical structure requires less doping levels which means less mask and fabrication cost. Therefore, the vertical PIN detector becomes the final choice in this project.

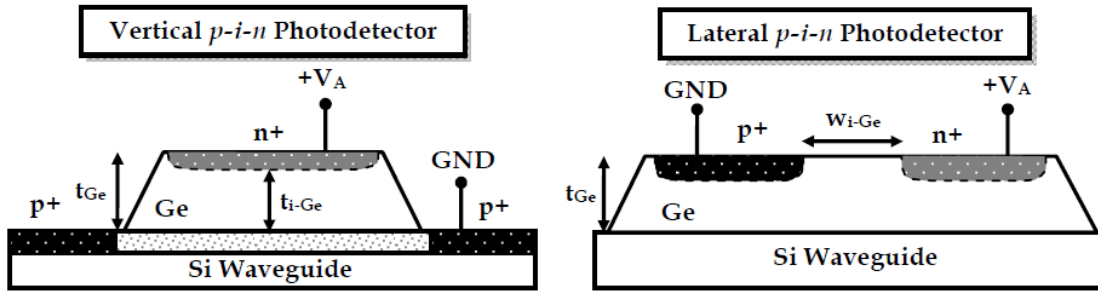


Fig. 3.18. Comparison of Vertical PIN detector and Lateral PIN detector[62]

The basic CAD design is shown as Fig. 3.19 where the shallow Nwell is used to dope bottom silicon, and the N+ implant helps to make contact on silicon.

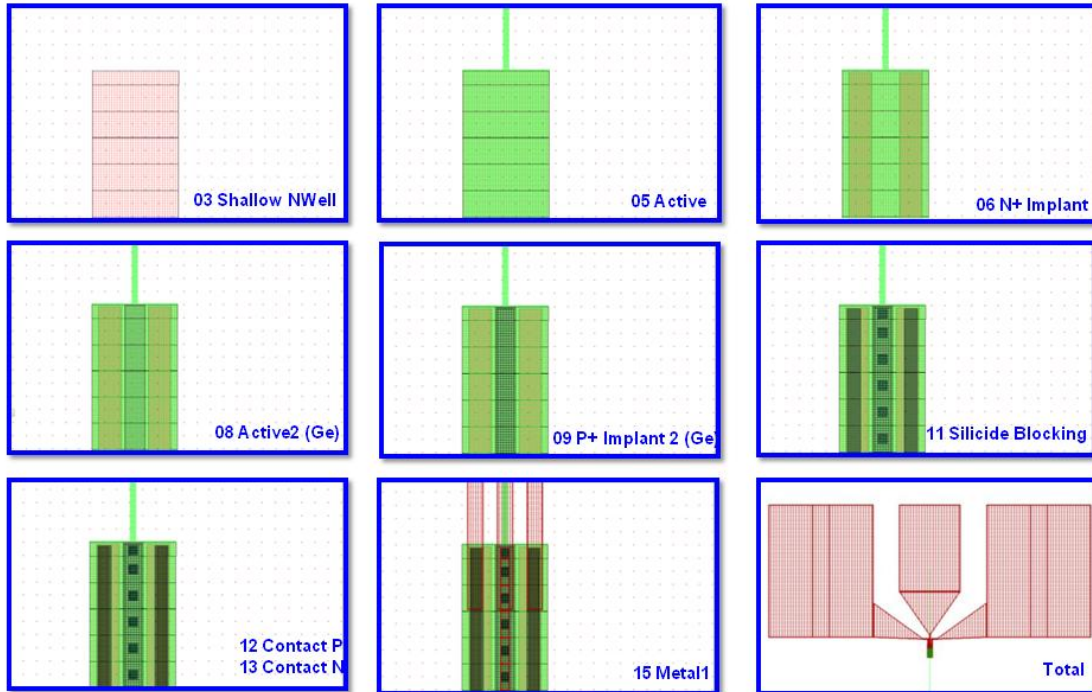


Fig. 3.19. CAD design of germanium detector

3.5 Germanium Laser

Telecom wavelength Silicon compatible electro pumping laser is always a dream of all silicon photonic researchers. It is listed as the most wanted for achievement of silicon based

chip level photonic interconnects. Researchers have tried porous Si [63], Si nanocrystals [64], Er doped Si [65][66], SiGe nano structures [67], GeSn [68], Si Raman laser [69], and III-V laser grown on or bonded to Si [70][71] to make it happen. However, none of these devices can truly meet the requirements.

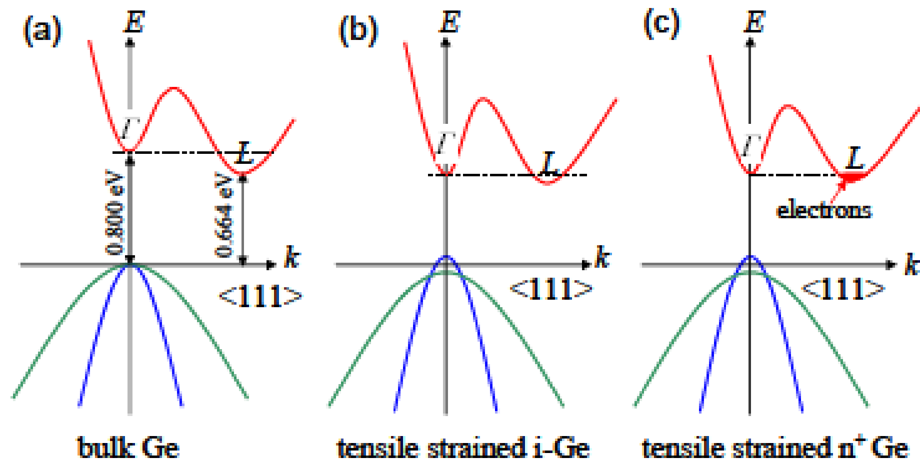


Fig. 3.20. (a) Band structure of bulk Ge have 136meV difference between direct gap and indirect gap (b)Decrease difference between direct and indirect gaps by introducing tensile strain (c)fill electrons in indirect valley to fill the rest of difference[74].

As mentioned in previous section, UHVCVD deposited germanium on silicon has already started working well as the photo detector. And the band gap of germanium is 0.8eV which exactly corresponds to the telecom wavelength 1550nm; it would be perfect if we can use germanium as the laser source on silicon platform. Researchers in MIT have already introduced tensile strains to decrease the energy differences between direct and indirect conduction band valley. And at the same time [72], they used n-type doping to fill

electrons into indirect valley to compensate the rest energy differences as shown in Fig. 3.20 [73].

And based on this work, electrically pumped germanium diode laser has been monolithically integrated into a CMOS process. The first laser device (Fig. 3.21) produces more than 1mW of output power and exhibits germanium gain spectrum of over 200nm [52].

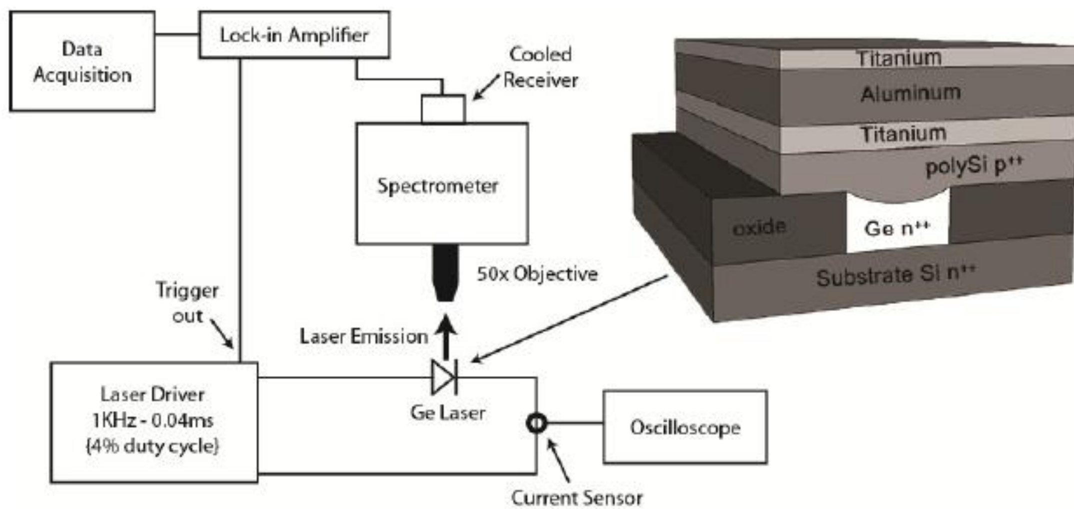


Fig. 3.21. Schematic of first integrated Ge laser

In our fabrication process flow, we have highly doped tensile strained germanium as the detector, and all the contacts and doping levels required for germanium laser are ready. So we naturally included some germanium laser designs in the final CAD.

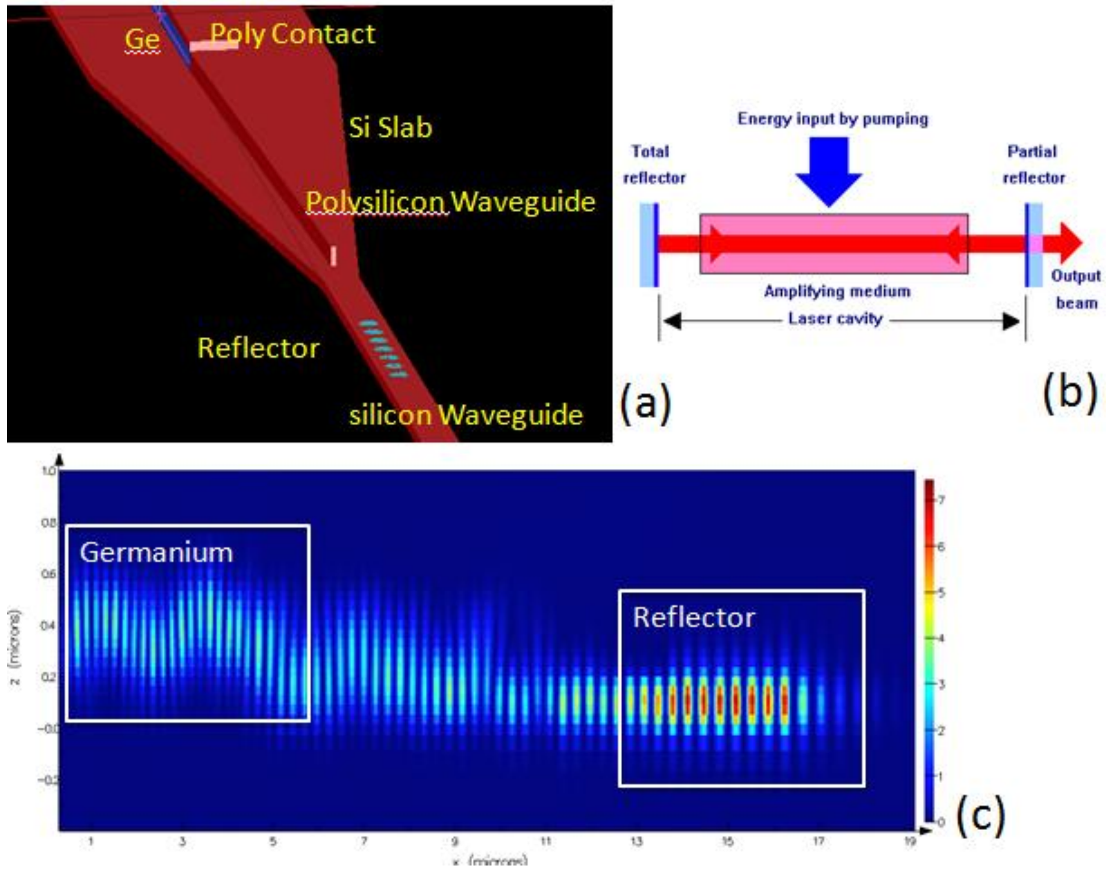


Fig. 3.22. Possible Fabry Perrot Ge Laser configuration and simulation of coupling

A basic construction of the germanium laser is shown as Fig. 3.22(b). A laser requires a good cavity and gain materials in the cavity. Assuming our processed germanium is good gain medium for electro pumping, a good cavity with two 'mirrors' is important. An identical design of Fabry Perot laser is included in the CAD layout, where mechanically polished germanium facets could be option of reflectors. However, the reflection coefficient is not as great as silicon based reflectors. In additional, to integrate the laser with other photonic circuit, a good coupling of mode from silicon layer to germanium layer is necessary. A FDTD simulation of coupling between germanium layer and silicon

waveguide is shown as Fig. 3.22.(c). Because germanium, polysilicon and crystal silicon are located at different height level, mode matching among them becomes really hard. This can cause huge loss each time it bounce back and forth, and therefore cannot form efficient cavity of a laser.

A disc resonator is proposed here as the resonator cavity. When photons are generated by the electric pump in the germanium disc, the photons that meet the disc resonance frequency can survive much longer in the cavity than other photons, and during their stay in the cavity, they can continuously stimulate more photons at the same frequency. After rounds and rounds of amplifying in the disc, partial of the stimulated photons would be emitted to the waveguide and guided to the outer photonic circuit as the source. A FDTD simulation of the disc resonator is shown in Fig. 3.23. As we can see, although the vertical position of germanium and poly silicon varies greatly, there still exists a peak frequency that wins over all other frequencies.

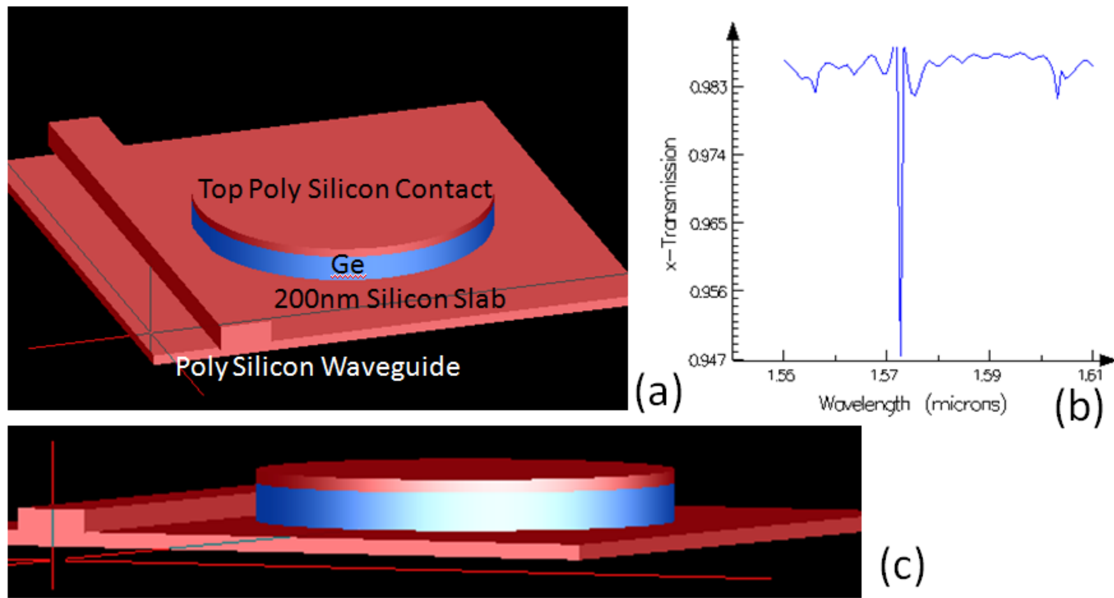


Fig. 3.23. Disc Resonator Ge laser

The CAD design is shown as Fig. 3.24 where bottom crystal silicon and germanium top are highly doped as the two electrodes for electric pumping. Germanium is patterned as a disc to perform as the disc cavity, poly silicon bar is patterned close to germanium disc to emit the lasing photons, and then a long polysilicon taper will guide photons to silicon waveguide.

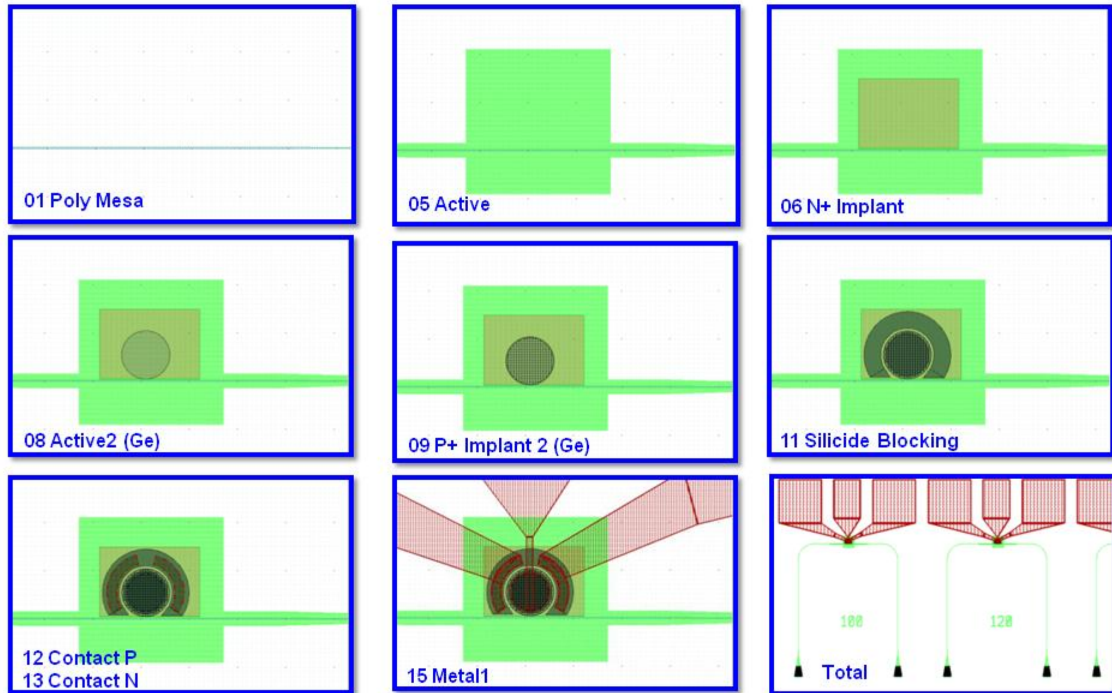


Fig. 3.24. Disc Resonator Ge laser

3.6 Wavelength Division Multiplexing (WDM) Interconnect

The wavelength- division multiplexing (WDM) technique that multiplexes a number of optical signals with different wavelength onto a single optical fiber to enhance the communication capability is used greatly in fiber-optical interconnects. Modern fiber optics can handle up to 160signals to expand basic 10Gbit/s capability to 1.6Tbit/s capability [75].

The WDM is also an important element that enhances the signal communication ability in Optical Network on Chip or other on chip photonic interconnects. As we have developed the detectors and modulators, switches, a full WDM system that integrates lasers, modulators, switches and detectors with fairly high speed is our best hope in this project.

Ring resonator, as we talked about in section 2.3.3 and 3.2, is an idea element for WDM systems. The basic idea of WDM in silicon photonic is shown in Fig. 3.25. It has lasers that can give signals of different channels. Then cascaded ring resonators that resonate at different wavelength can modulate signals from different channels. The waveguide can carry the modulated signals to the demultiplexing end. Then another set of ring resonators with drop ports would demultiplex the signals. And finally, detectors at each end would receive the signals. Unfortunately, the laser module is far from being ready, we have to use external laser sources in our actual WDM system.

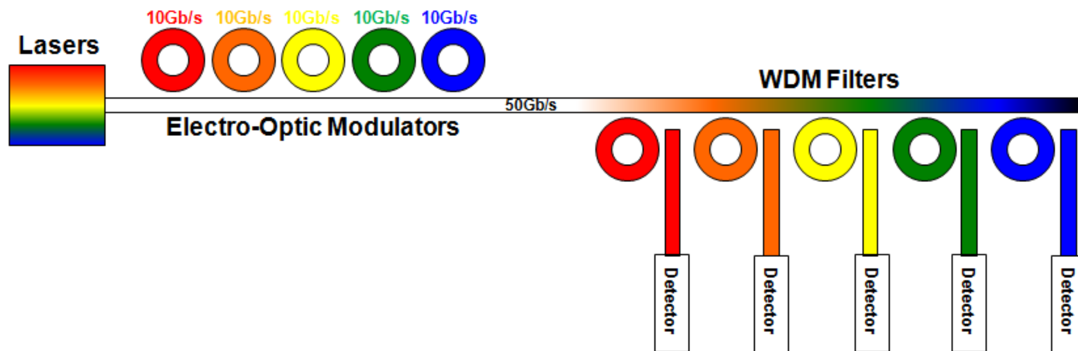


Fig. 3.25. Basic idea of WDM system

Ring resonators with 5 microns and 4 microns radius are chosen to be the basic elements in the WDM system. The 5 microns radius ring has an FSR of 22nm. The cascaded 5 microns radius ring resonators have 5 nm differences in radius and therefore give resonance wavelengths with 1nm difference. In one FSR, 20 channels system is applicable which means 200Gbit/s WDM system based on 10Gbit/s basic capability. The

basic 40Gbit/s WDM systems are built as shown in Fig. 3.26(a). And based on that, the 80Gbit/s WDM and 160Gbit/s WDM systems are built as shown in Fig. 3.26(b)&(c).

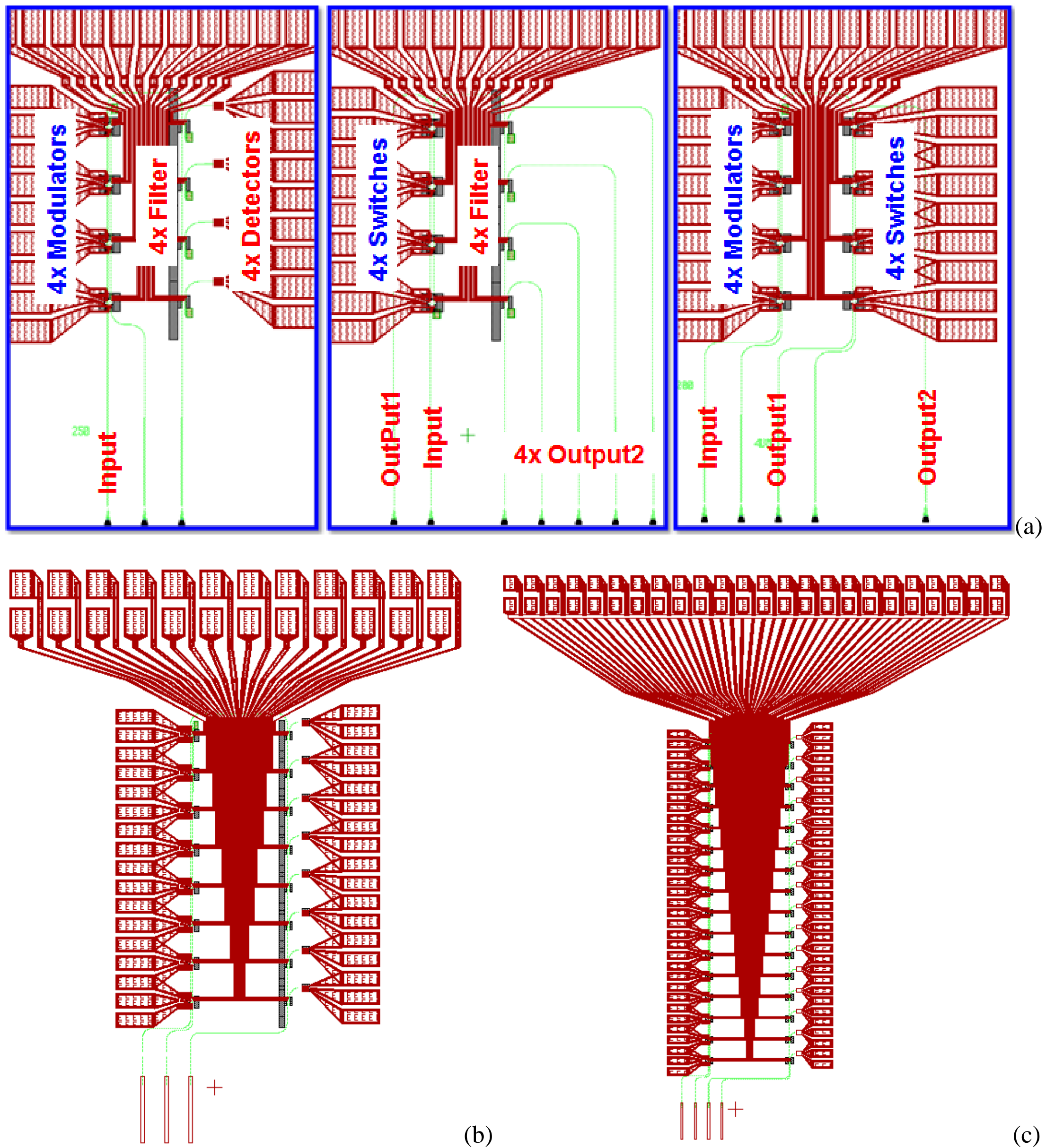


Fig. 3.26. (a)40Gbit/s WDM system (b) 80Gbit/s WDM system (c)160Gbit/s WDM system

One weakness of the ring resonators in WDM system is that the rings are very sensitive to fabrication errors. The thickness difference of 1nm can cause the drifting of

resonance wavelength. Because silicon is thermal sensitive; the temperature difference will also cause problems for the working WDM systems. The solution for this is adding additional heaters on each individual ring. The thermal balance would be necessary during the testing period, and a high efficiency thermal control method is explained in 4.3.

3.7 High Efficiency Optical Coupling by Grating Coupler

3.7.1 *Introduction of Off-Chip Packaging*

The high refractive index contrast of silicon photonic allows a tighter bend radius and smaller dimensions of optical waveguides compared to other photonic integrated circuits. However, this makes the coupling both to and from optical fiber non trivial because of huge size difference (450nm width compared to 10microns of diameters as described in Fig. 3.27(a)). As shown in Fig. 3.27(b) inverted taper is exploited to expand the optical mode of silicon waveguide to match the mode of silica fiber for good optical coupling [76]. But it requires a long transition length which means a larger footprint on the chip. And most importantly, the coupling of signals can only happen at the polished smooth edge of the photonic chip, which makes the sample preparation more difficult.

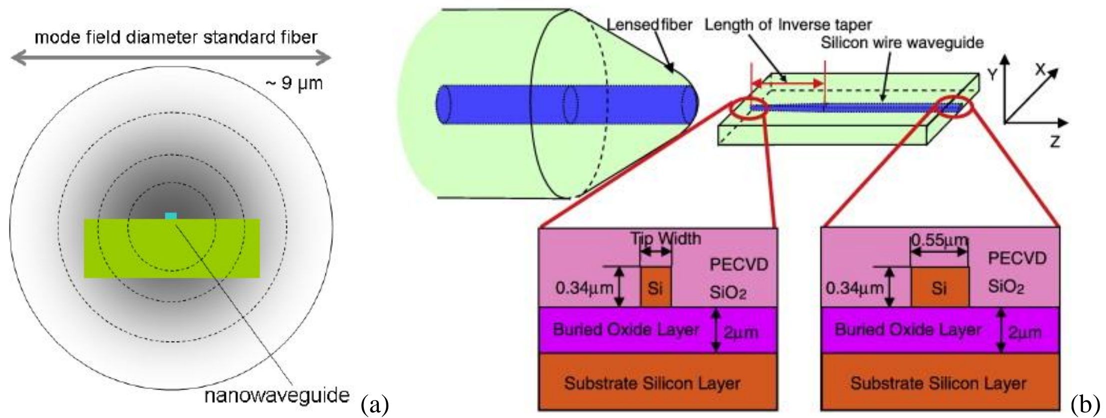


Fig. 3.27. (a) Comparison of dimension of silicon waveguide to dimension of fiber (b) Inverse taper configuration

Grating coupler is another option for fiber to chip coupling. As shown in Fig. 3.28, the greatest advantage of grating coupler is that, it's an out of plane coupling. Thus, we can test the wafer scale photonic circuits without dicing and polishing the edge. In addition, it allows a denser design of photonics circuits.

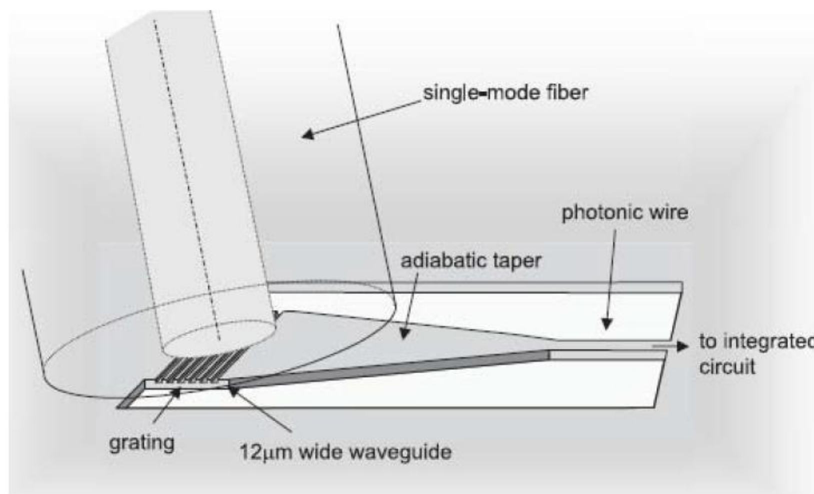


Fig. 3.28. Operation principle of a nanowire waveguide grating coupler [77]

The basic principle of grating diffraction is shown as Fig. 3.29(a). Two optical beams diffract upon a grating surface. And the constructive interference would happen when the

optical beam path difference is multiple of the wavelength. This can be explained in a basic equation:

$$AB - CD = \Lambda(\sin(\theta) + \sin(\theta_m)) = m\lambda \tag{3.2}$$

In the case of grating coupler, $\sin(\theta_m)$ is 1, and the beam path of CD have to consider the effective refractive index n_{eff}. To achieve the first order constructive interference in the waveguide, m=1. The theory equation of getting constructive interference in waveguide then becomes

$$\Lambda = \frac{\lambda}{n_{eff} - \sin\theta} \tag{3.3}$$

Where Λ is period of grating, λ is wavelength, θ is the incidence angle, and n_{eff} is the effective refractive index of the grating coupler.

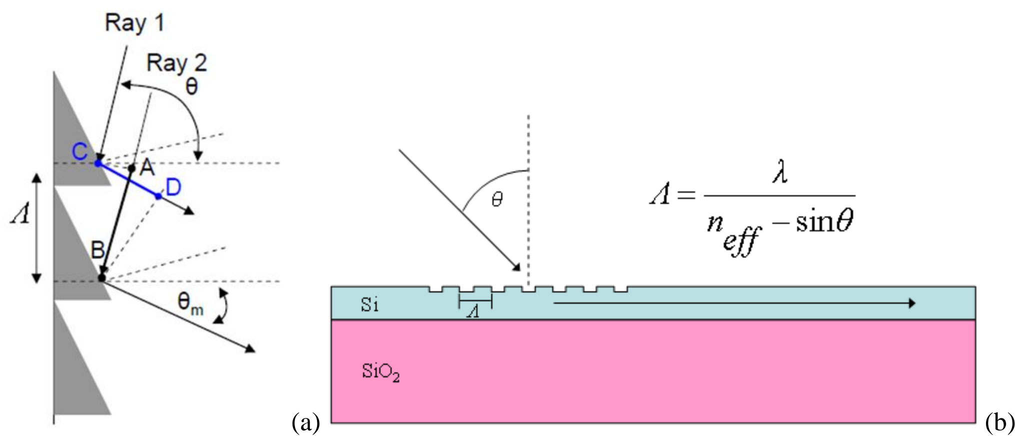


Fig. 3.29. (a) Principle of grating diffraction, (b) Principle of grating coupler

Several strategies have been applied to get better coupling efficiency. Some researchers put bottom mirror (gold film [78] or DBR type mirror[79]) to redirect downwards diffracted light. Optimize the individual grating periods and dimension can also help to match the mode of diffracted light to the fiber mode, and therefore enhance the coupling efficiency [79][80]. So far, the best coupling efficiency is achieved by adding an additional poly-silicon layer on top of the crystal silicon with deep grating etch during the patterning [81]. Our study of optical packaging would be based on the poly-silicon enhanced grating coupler.

3.7.2 *Grating Fiber Coupler Design*

A process flow of the grating coupler is shown as Fig. 3.30.

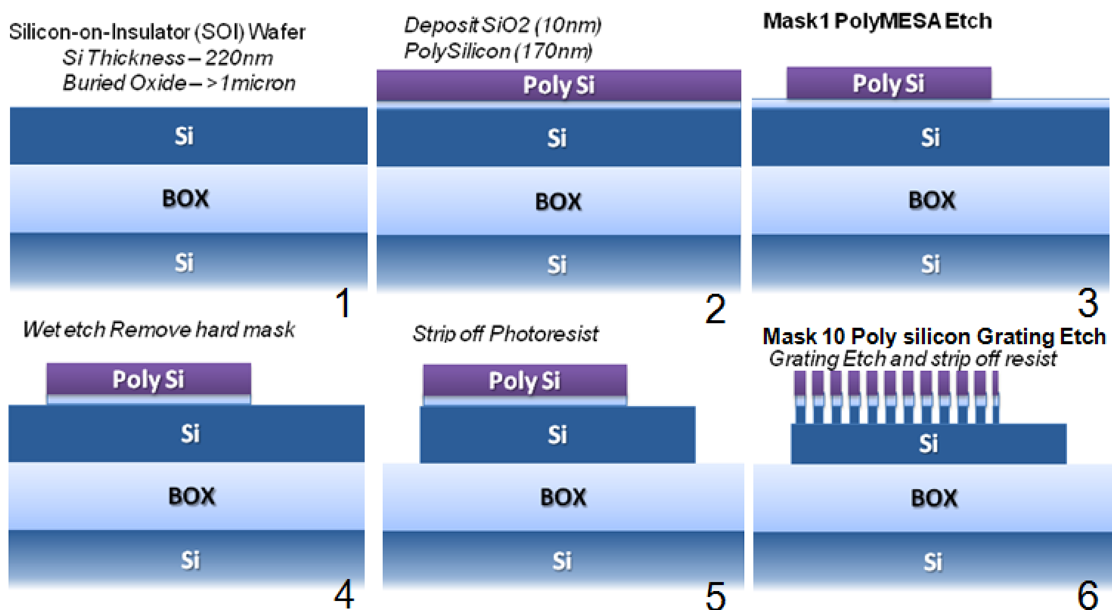


Fig. 3.30. Process Flow of Grating Coupler

This process flow is part of the full 300mm silicon photonic process flow as described in 3.1. It starts with a SOI wafer with 220nm Silicon and thick buried oxide (2 microns). SiO2 of 10nm to 20nm is deposited on top of the SOI followed by 170nm of poly silicon deposition. The SiO_2 plays an important role as the hard mask of crystal silicon during poly silicon etching. And the thin oxide with thickness of 10nm to 20nm would not affect the optical mode too much based on FDTD simulation. Mask #1 is used to pattern the grating area that requires deep silicon etch. After the thin oxide is removed by wet etching without harming the quality of crystal silicon, silicon waveguide is patterned by mask #5. Mask #10 is used to pattern the grating structures. And finally the grating etching will be applied to etch the top poly silicon layer, the thin oxide layer and small portion of the crystal silicon. It is important to leave the grating etching process after most of the etching process because the thin oxide layer can hardly survive under any other wet etching processes that remove the hard masks.

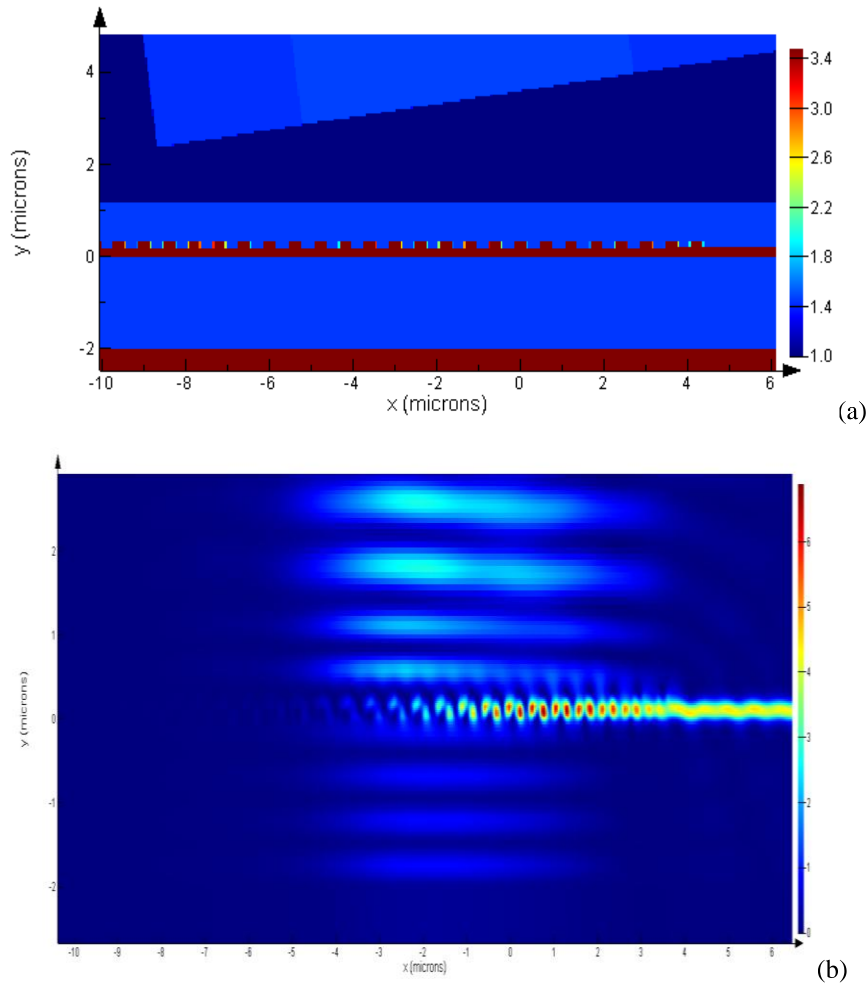


Fig. 3.31. 2D FDTD simulation of grating coupler

To optimize the coupling efficiency, a series of 2D FDTD simulations are done with Lumerical as shown in Fig. 3.31. Here we assume the 1550nm wavelength light is launched to the 200nm thick waveguide by a 10microns diameter fiber with 9 degree incidence angle.

Initially, we assume the grating period is 630nm with a filling factor of 0.35, and the total etching depth is 220nm. Thus we vary the total thickness of waveguide from 320nm to 410nm. The result in Fig. 3.32(a) shows that, the optimum coupling can be achieved with

total thickness of 390nm, and thinner total thickness can make blue shift of optimum spectrum. Then we fix the total thickness to be 390nm, period to be 630nm and etching depth to be 220nm period, and only vary the filling factor. The result in Fig. 3.32(b) shows, there is only small change in coupling power for filling factor, and smaller filling factor can give blue spectrum. In the third simulation, we keep 390nm as the total thickness, 220nm as the etching depth, 0.39 as the filling factor, and vary the period from 550nm to 670nm. Result in Fig. 3.32(c) shows that, there is large spectrum shift during period vary, and an optimum coupling is achieved nearly 1.6microns wavelength with period of 630nm. In the forth simulation, period is fixed to be 630nm, filling factor to be 0.39, total thickness to be 390nm, and we only vary the etching depth. As shown in Fig. 3.32(d), optimum coupling is achieved at 220nm etching depth, and larger etching depth gives blue shift of the spectrum.

Finally, the relatively optimized coupling efficiency can be achieved when we set total thickness to be 390nm, period to be 630nm, etching depth to be 220nm, and filling factor to be 0.39. And this particular optimum coupling is displayed as shown as Fig. 3.32 (b).

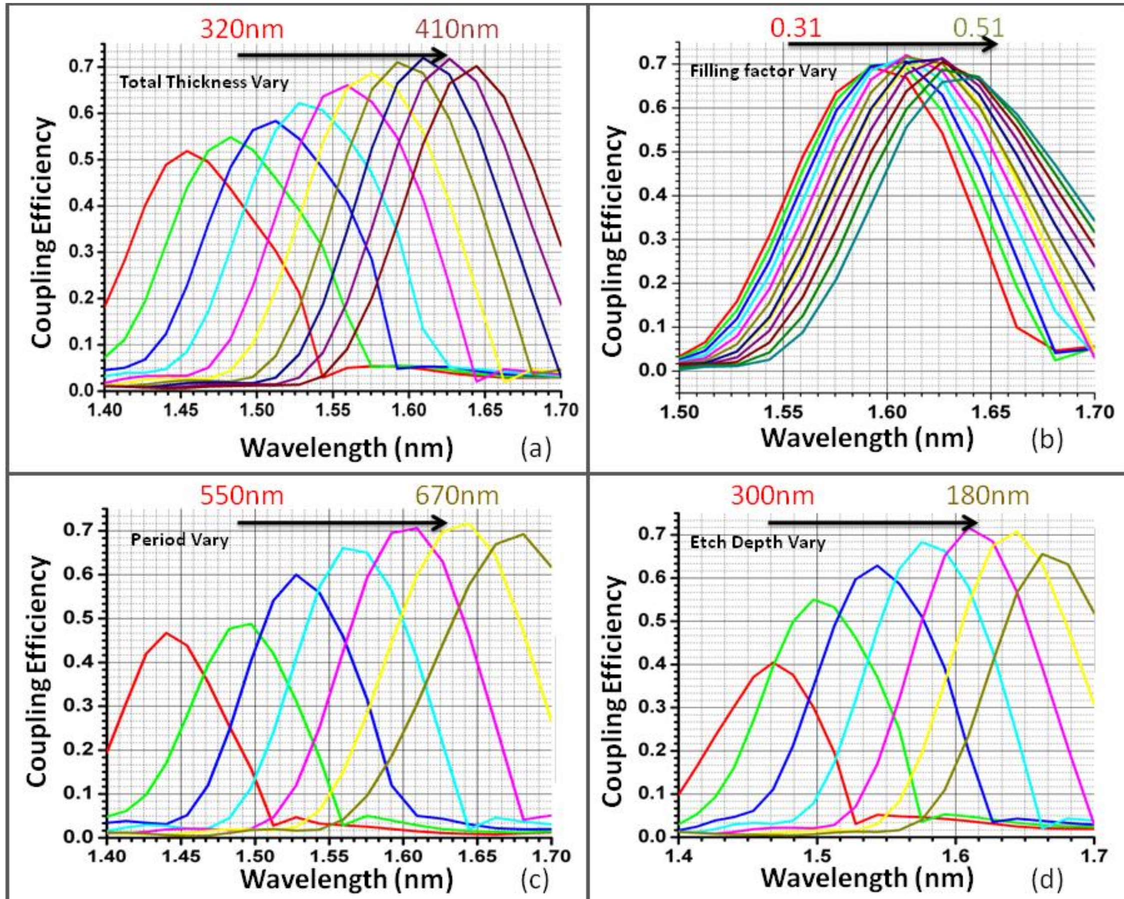


Fig. 3.32. Simulation of optimizing the grating coupler (a)Vary total thickness from 320nm to 410nm, (b) Vary filling factor from 0.31 to 0.51, (c)Vary Period from 550nm to 670nm, (d) Vary etch depth from 300nm to 180nm

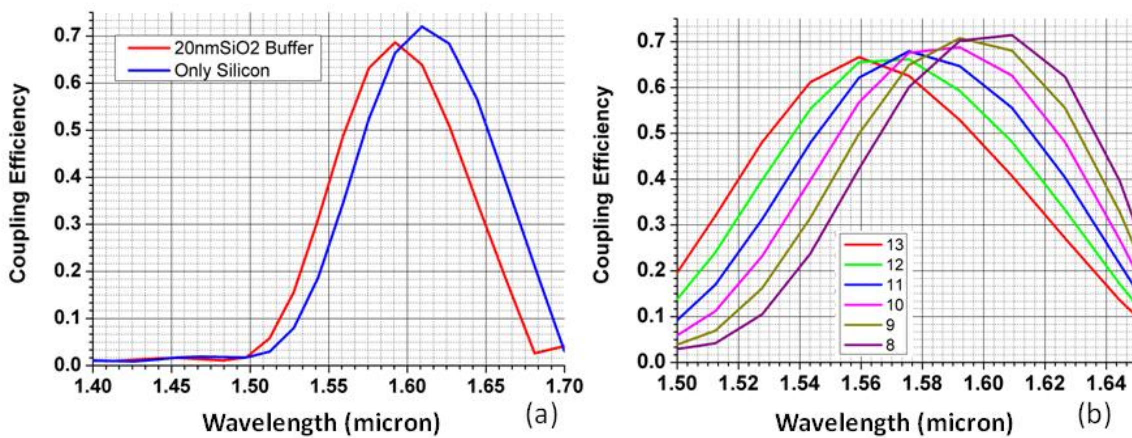


Fig. 3.33. Simulation of grating coupler (a) Compare of coupler with and without 20nm buffer oxide (b) Compare of coupling efficiency at different incidence angle.

Since during the real fabrication process we will add an additional 10nm or 20nm silicon oxide as hard mask of silicon protection, it is meaningful to run a simulation and make a comparison between grating couplers with and without thin oxide. Simulation result in Fig. 3.33(a) shows no big difference in coupling efficiency, and there is a little bit blue shift when we add the thin oxide. This convinced the process of adding thin oxide hard mask. Incidence angle study is also demonstrate in Fig. 3.34 (b) and result shows blue shift can be achieve when we use larger incidence angle. This means we can optimize the coupling coefficient for certain wavelength by simply optimizing the incidence angle of the testing fiber.

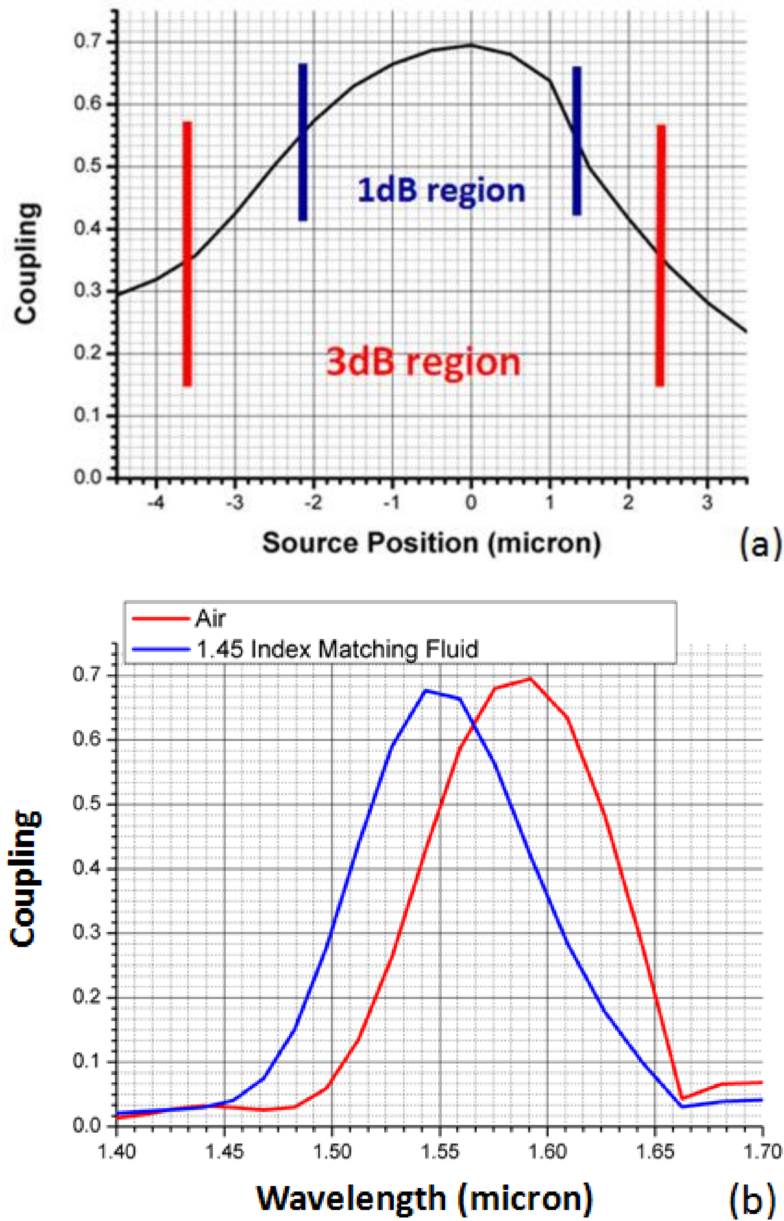


Fig. 3.34. Simulation of grating coupler (a) misalignment tolerance (b) With and without index matching fluid

After the grating structure and incidence angle is fixed, a misalignment error study is made by moving the input fiber at different position. Simulation result in Fig. 3.35(a) shows it has quite high tolerance in position misalignment. And finally a simulation in Fig. 3.35(b) shows that, with proper index matching fluid, we can get blue shift of the spectrum. In the

actual experiment, index matching fluid might be helpful because it will reduce the reflection due to the refractive index difference between air and silica fiber or silicon oxide cladding of the chip.

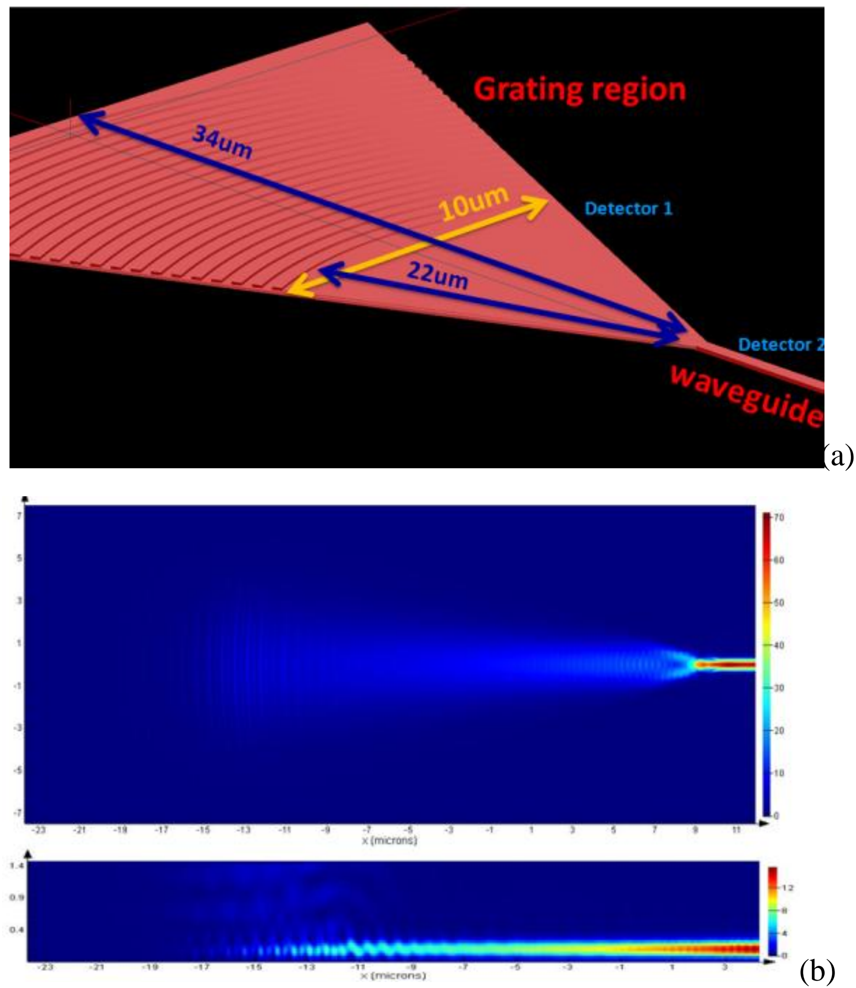


Fig. 3.35. 3D FDTD simulation of focusing grating coupler (a) Configuration of focusing grating coupler (b) X-Y plane and X-Z plane view of coupling efficiency

Fig. 3.36. Alignment tolerance study of focusing grating coupler

After optimizing the basic parameters of the grating coupler by 2D simulation, a 3D simulation is done on focusing grating coupler structures as shown as Fig. 3.37. A tolerance study displays at Fig. 3.36 demonstrate quite high misalignment tolerance in both x and y direction.

3.7.3 *Introduction of Chip to Chip Packaging*

Photonic integration has experienced tremendous development in recent years. For photonics to replace the on chip copper interconnects, great challenges still remain on chip to chip and chip to board packaging.

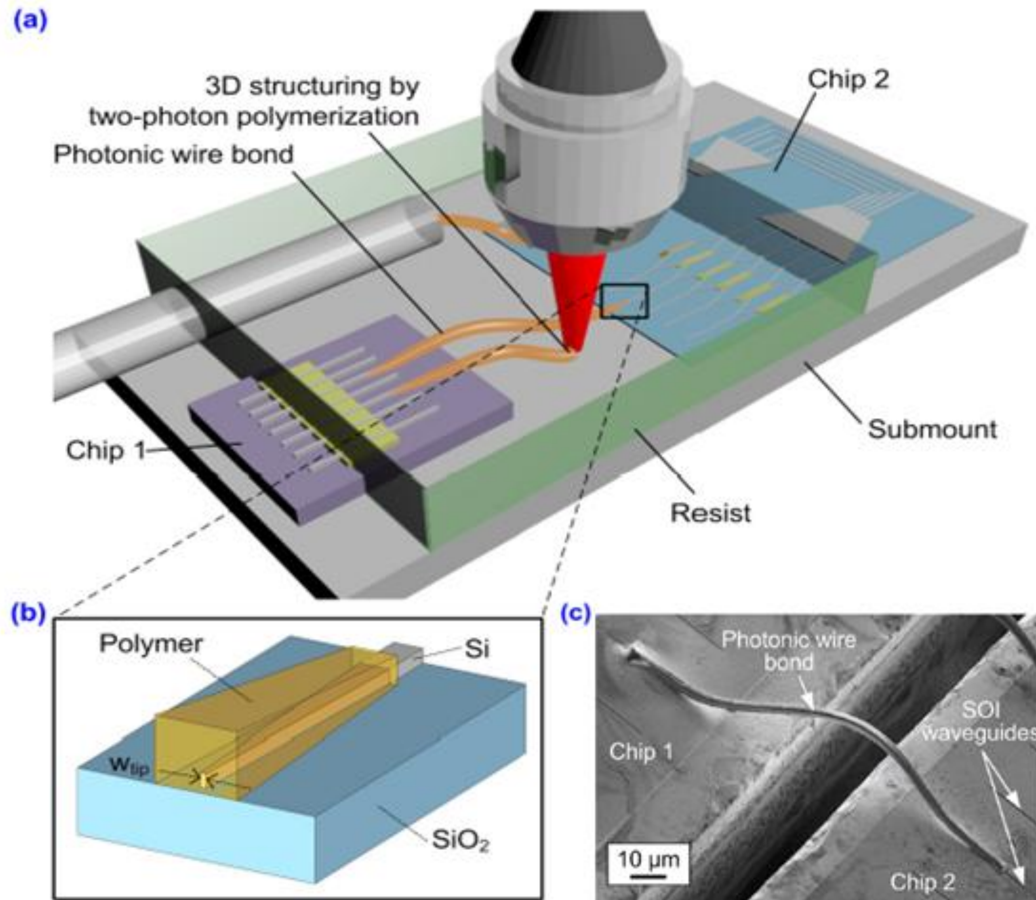


Fig. 3.37. (a) Photonic multichip based on photonic wire-bonding (b) Inverse-taper transition between an SOI nanowire waveguide and a polymer Photonics Wire Bonding interconnects. (c) SEM of Photonics Wire Bonding chip to chip interconnects[82]

People has already exploited inverse taper to expand the optical mode of silicon waveguide to match optical fiber mode [83]. Polymer waveguide is also introduced as the media of optical transmission [84] on silicon photonics. Researchers in German used two photon absorption lithography technique [85][86] to pattern 3D polymer wires between inverse tapers from different chips. This can be viewed a photonic version of wire bonding as shown as Fig. 3.37. However, this cannot solve all the problems in integrated photonics. Similar to the electric wire bonding, photonic wire bonding can only be applied at the edge

of chips, and requires large footprint for each one of the connections since polymer wires have low refractive index contrast. In addition, it requires more accurate alignment on each individual connect. Therefore, it's not an ideal solution for high throughput fabrications. Another way of using the polymer – inverse silicon taper coupler is proposed for flip chip bonding between chip to board as shown in Fig. 3.38 [87].

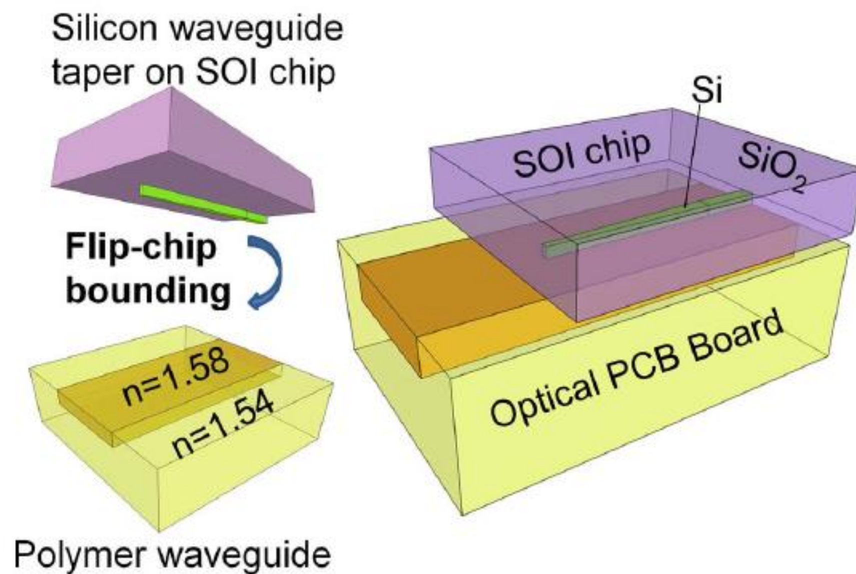


Fig. 3.38. Schematic of chip to board connection with inverse taper and wide polymer waveguide [87]

This flip-chip method is great for high throughput fabrication, and the polymer waveguide turned the lateral transmission vertically to another lateral transmission. But this method requires the silicon to be exposed to air without cladding protection. This may not be an ideal solution for chip to chip packaging.

And flip chip grating to grating coupling with self aligned indium bump is demonstrated as shown as Fig. 3.39.

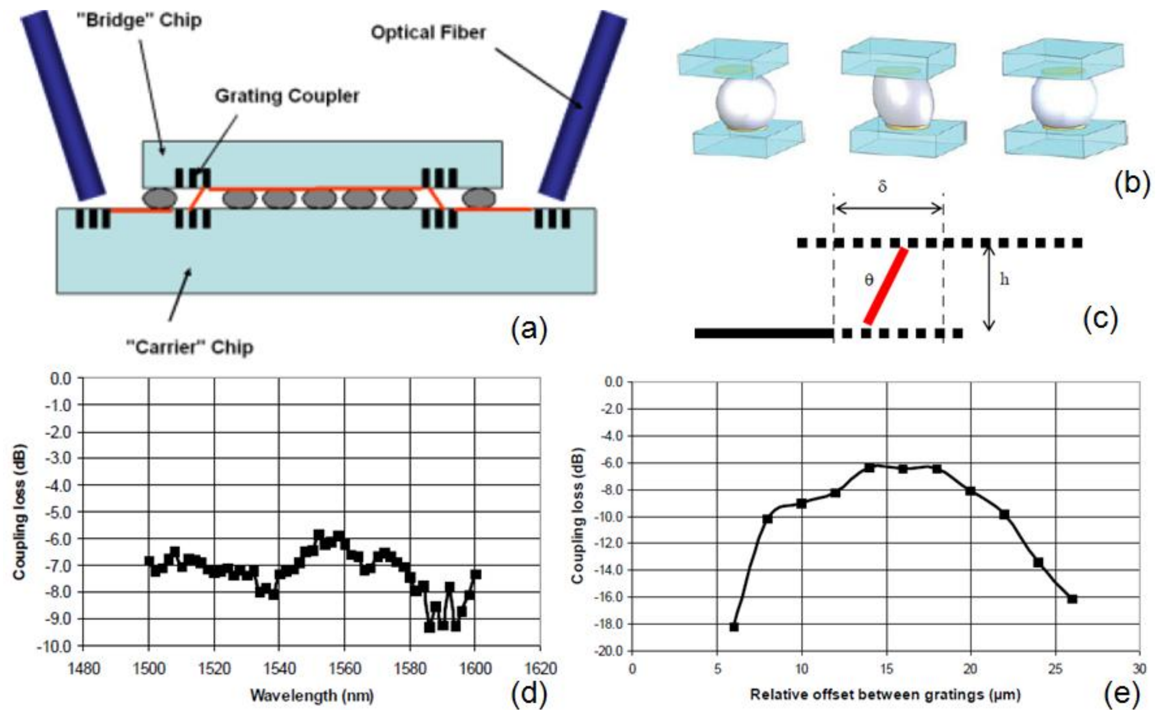


Fig. 3.39. Grating to grating coupling with Indium reflow self-alignment method (a)Configuration of chip to chip grating coupling (b) Indium reflow self-alignment (c)basic principle of grating to grating coupling (d) grating to grating coupling loss (e) misalignment error tolerance [88]

This chip bonding method fully used the self align property of indium bump, and is proved to be a great high volume manufacture packaging solution. By further investigate their result, the grating to grating configuration has very high misalignment tolerance, but the indium bumps they used is normally 35 microns [89] thick. Therefore, huge large may actually come from the far distance between chips. And it may not be necessary to keep perfect alignment during the packaging. And a better grating structure is required to

optimize the grating to grating coupling. Here we propose our chip to chip optical packaging based on thermal compressed copper bonding.

3.7.4 *Design of Chip to Chip Packaging*

We start from grating structures that we have already optimized for fiber to chip coupling. In the actual fabrication, we will have oxide cladding of 1 micron to 1.5 microns over the silicon layer. So when the actual gap between bottom grating and top grating to be is at the range between 2microns to 3microns as shown as Fig. 3.40(a). A TE mode 1550nm wavelength source is launched to the top waveguide. The light will be diffracted by the grating structure and collected by the bottom grating coupler as shown in Fig. 3.40(b). From the equation of grating coupler, shorter wavelength will have larger transmission angle. Therefore, the collection coupler needs to stay farther away. And also during the coupling, light will suffer of the loss during transmission on the grating structure. So 2D simulations of different overlap length between the gratings are done and are shown in Fig. 3.40 (c). Result shows that, the best coupling efficiency of nearly -2dB happens with overlap length of 13 microns. The best coupling efficiency and coupling efficiency at 1550nm from all positions are demonstrated in Fig. 3.40 (d). The result shows that, this coupling method has

really high tolerance. And it has almost 9 microns tolerance range with coupling efficiency difference of only 1dB.

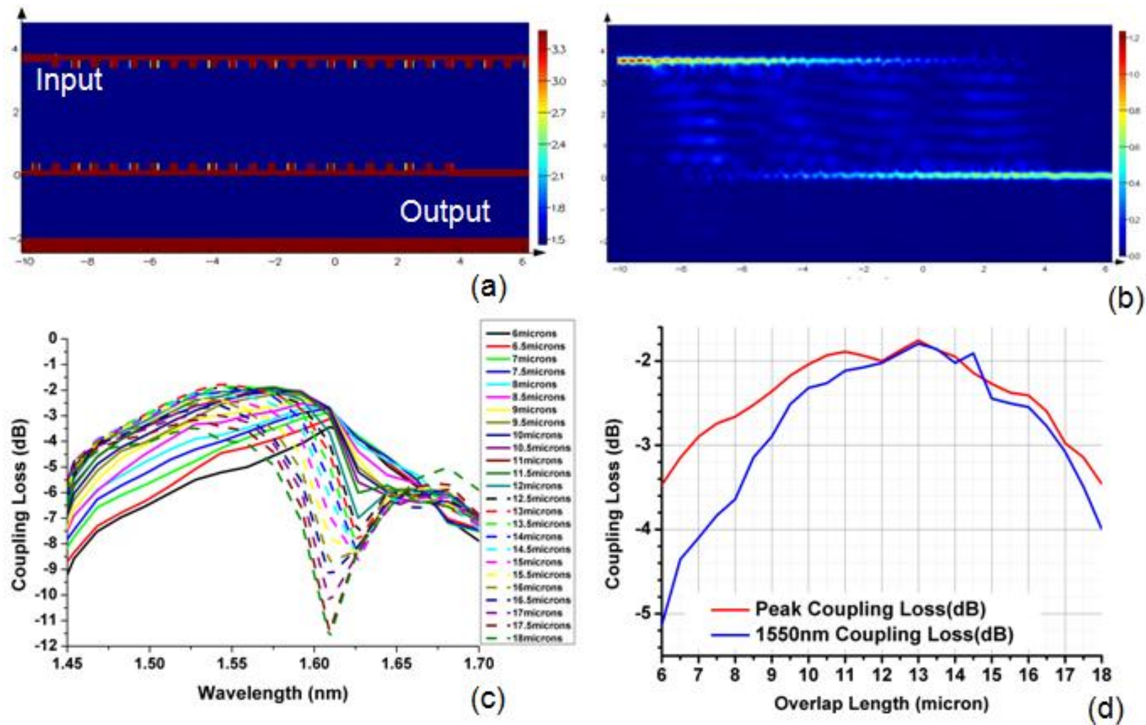


Fig. 3.40. 2D simulation of chip to chip grating coupling: (a) Configuration of grating to grating coupling (b)Cross section view of optical transportation of chip to chip coupling (c)Coupling spectrum for different overlap distance (d) Coupling loss tolerance

As shown in 3.7.2, the grating coupler fabrication parameters like etching depth, total thickness is fixed. And we have learnt that filling factor would not change too much for the coupling. The only parameter that can be optimized for better chip to chip coupling is the period. Simulation results of chip to chip coupling efficiency at different periods are shown in Fig. 3.41(a). The optimum results are achieved at period from 610nm - 630nm. During the simulation, the overlap region of the two couplers might slightly shift due to changing of

period. Another simulation of different overlap with same period is shown in Fig. 3.41(b). The result tells that small change of overlap doesn't affect too much of the total coupling efficiency. Therefore, the result in Fig. 3.41(a) is true. We are certain the optimum period is 610nm - 630nm.

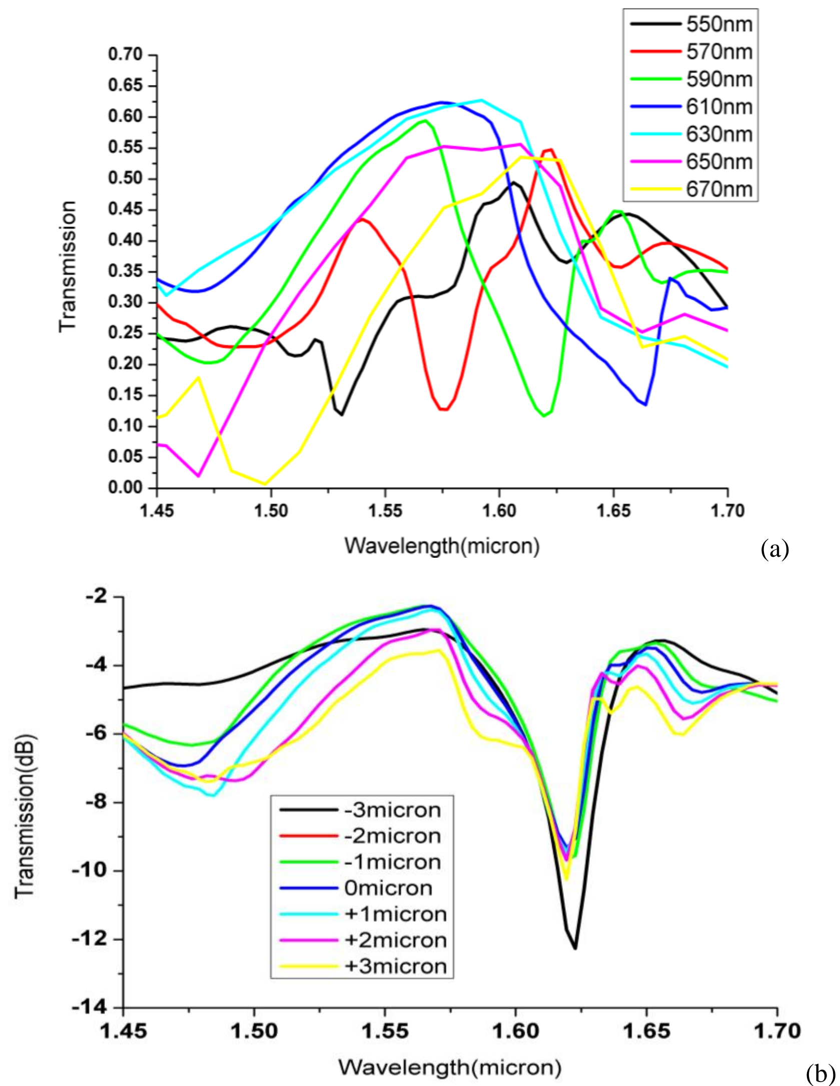


Fig. 3.41. (a) Chip to chip coupling efficiency at different period. (b) Chip to chip coupling efficiency with different overlap length.

The 3D focusing coupler has been proved working well at fiber to chip coupling. The 3D simulation of chip to chip coupling based on the focus grating structure is demonstrated in Fig. 3.42. Fig. 3.43 (b)-(d) demonstrates the electric field at their plane of transmission. A set of simulations (Fig. 3.43(b)) at different locations shows not much change from the taper part to the waveguide part.

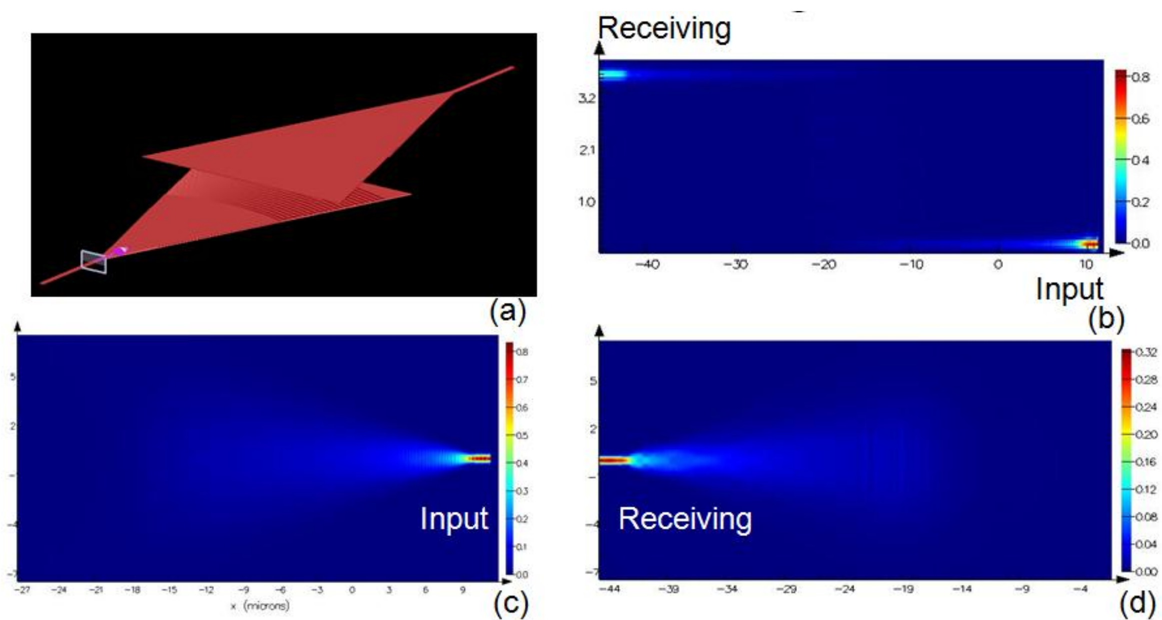


Fig. 3.42. 3D simulation of chip to chip grating coupling: (a) Configuration of 3D focusing grating to focusing grating coupling (b) Cross section of chip to chip coupling (c) Photon transmission of input plane (d) Photon transmission at receiving plane

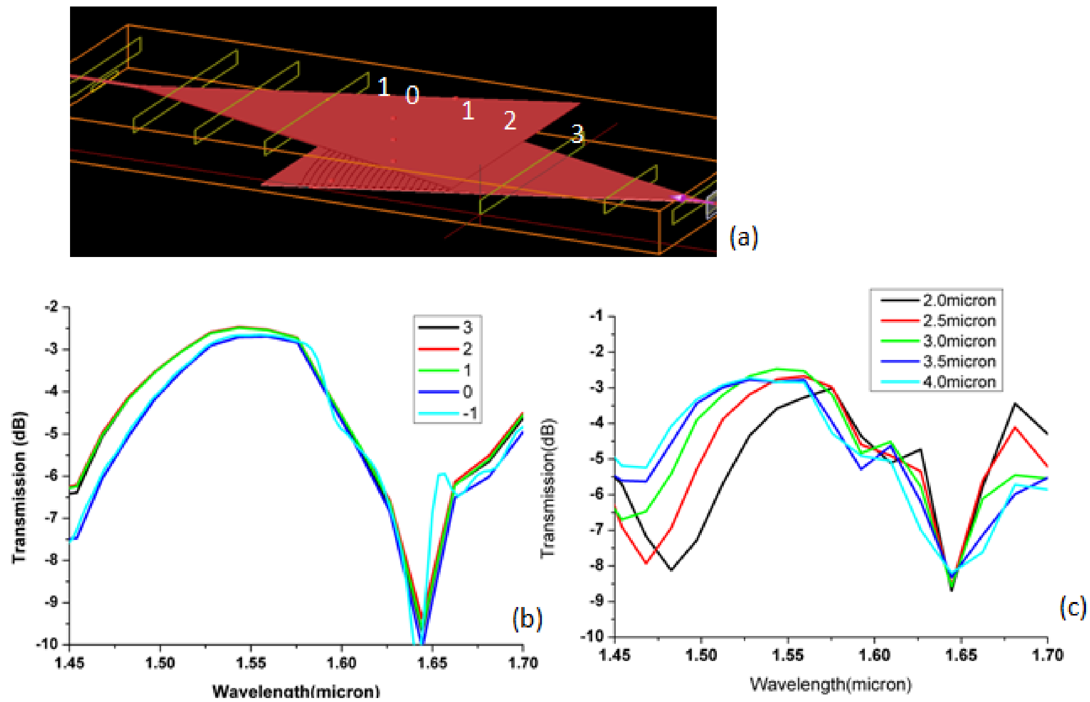


Fig. 3.43. (a) Configuration of chip to chip coupling. (b) Chip to chip coupling efficiency at different receiving place. (c) Chip to chip coupling efficiency with different gap.

The final cross section view of the chip to chip alignment is shown in Fig. 5.2.18. The thermal compressed copper to copper bonding technology is recently greatly improved because TSV development. There is uncertainty of final cladding of oxide and actual metal thickness; therefore, the final gap between the gratings is unknown. It's important to learn the influence of gap difference to the coupling efficiency. So another set of simulations of coupling efficiencies at different gaps between the gratings are shown in Fig. 3.43(c). Result shows a good tolerance of gap differences. This gives greater flexibilities during the fabrication.

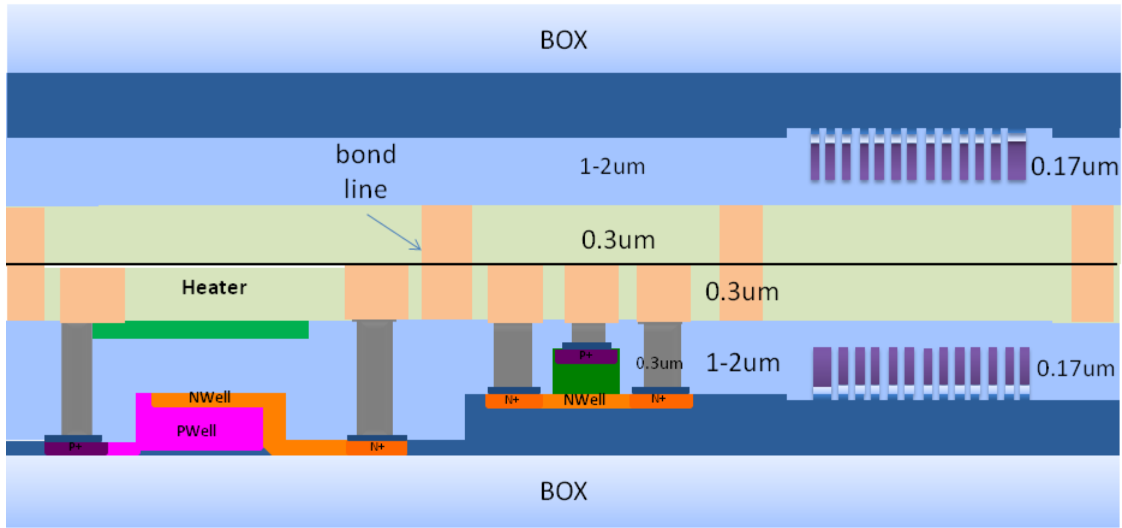


Fig. 3.44. Cross-section of flip chip bonding and electric and optical packaging

Beside of focused grating structure, the flat grating design is also simulated here as shown in Fig. 3.44. The thinner design has better performance because of the better transmission of the adiabatic changing taper. However, thinner coupler has less alignment tolerance simply because of smaller playing field. And a final comparison of focus structure and flat structure shows a great advantage of focus grating structure as shown in Fig. 3.45.

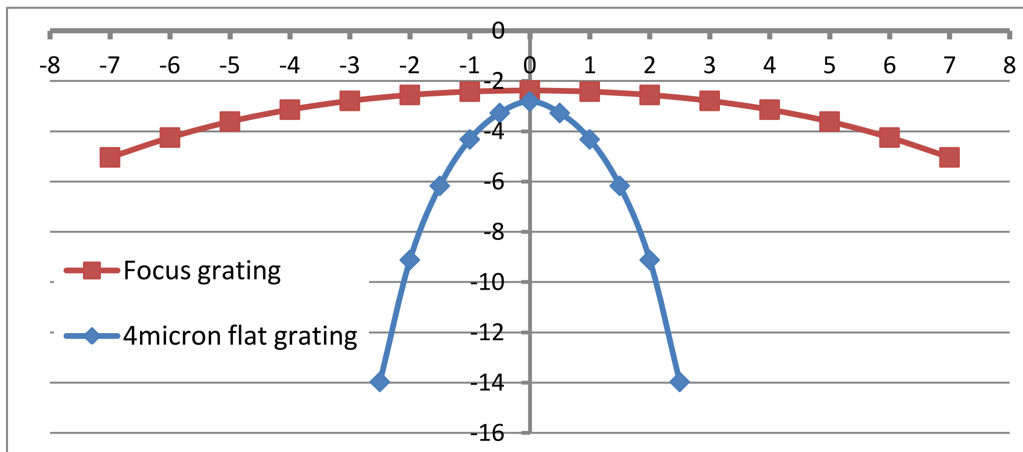


Fig. 3.45. Comparison of misalignment tolerance between focused grating structure and flat grating structure

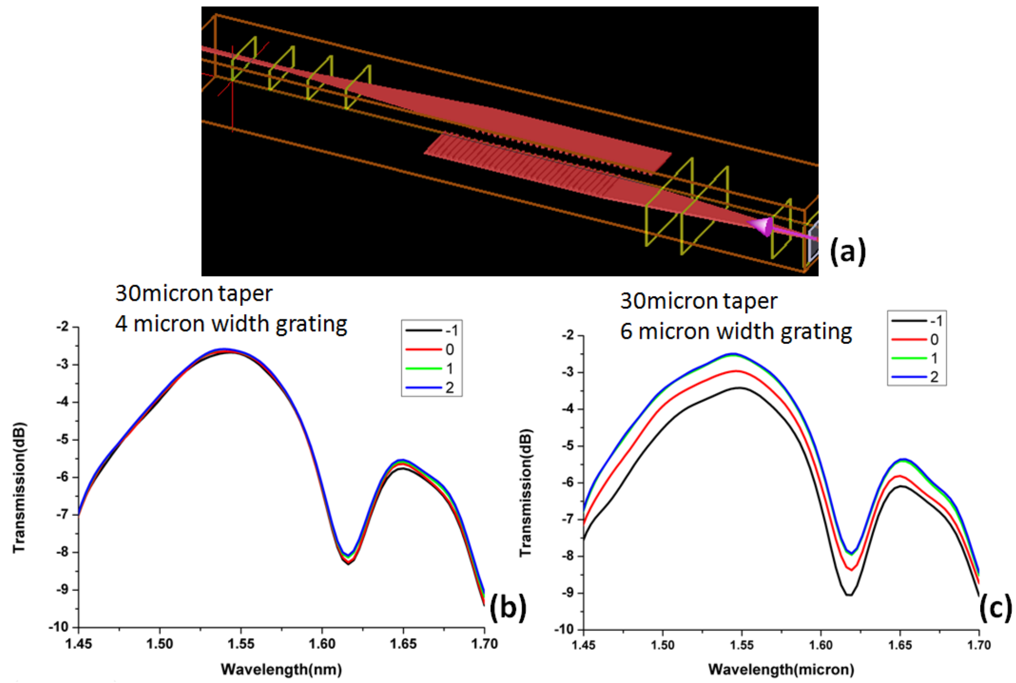


Fig. 3.46. (a)Flat grating coupling setting (b) coupling with 4 microns width grating (c) coupling with 6 microns width grating

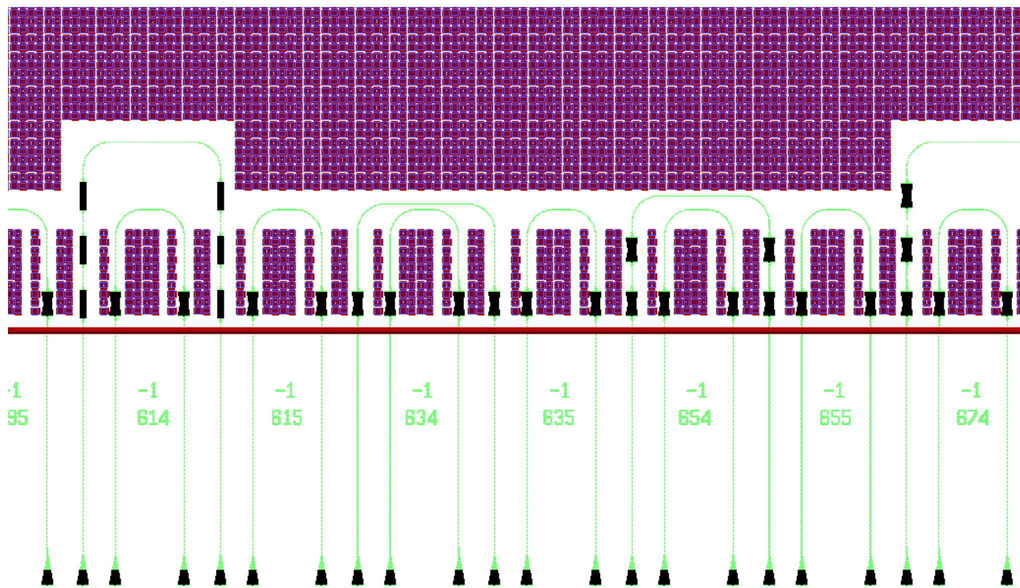


Fig. 3.47. CAD of basic flip chip design

After all the simulations, parameters of grating couplers are determined, a basic the copper bonded flip chip design CAD is shown as Fig. 3.47.

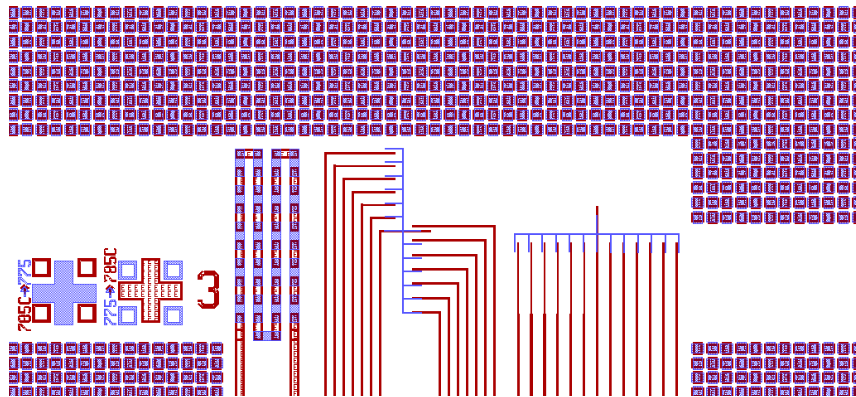


Fig. 3.48. Electric Vernier used to measure misalignment

The coupling efficiency can be tested by comparing none coupled devices and double coupled or even triple coupled devices. Alignment error is purposely brought in to further study the misalignment tolerances. And to test the actual misalignment, electric verniers are designed as show in Fig. 3.48 to measure the actual misalignment.

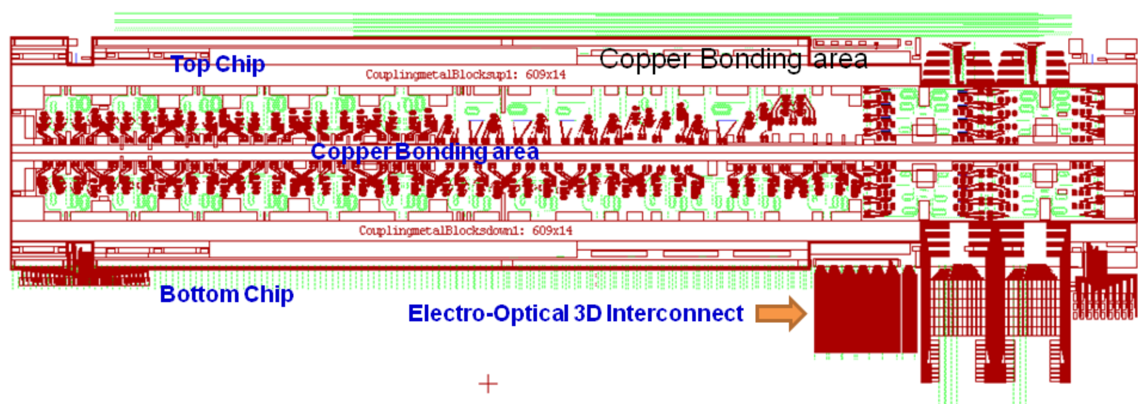


Fig. 3.49. Flip-chip packaging design

The full design block of the flip-chip packaging is shown as Fig. 3.49 where the bonding area is 5mm wide and 25 mm long. This large bonding area makes the copper to copper compressed bonding to be stable enough. This design actually included both the

upper chip and bottom chip in one mask set to save cost. Achieving of packaging requires two fabricated wafers. One of the will be dice to be a small chip, and then aligned and bonded to the wafer (chip to wafer bonding). The copper bonding offers electric connection between top and bottom chips. And above all, full 40Gbit/s WDM systems based on 3D electric and optical interconnects are designed and shown in the right region of Fig. 3.49.

3.8 Summary

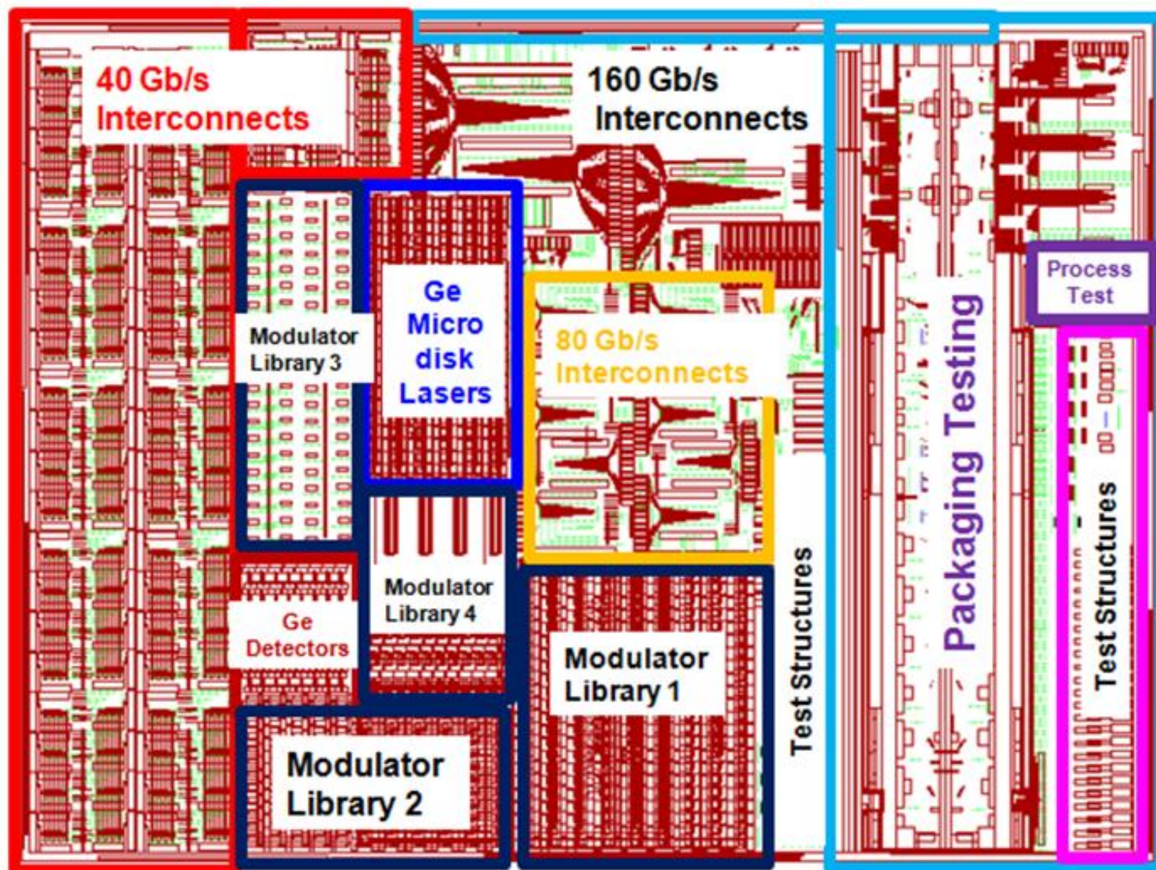


Fig. 3.50. Test structures designed for a 300mm process

This chapter mainly introduces the work done to build up silicon photonic library based on the state-of-the-art 300 mm fabrication conditions. A mask design is shown in Fig. 3.50. The CMOS compatible process flow is developed based on current available process flow in CNSE. Individual elements like silicon ring resonators, modulators, Ge detectors and Ge lasers, grating couplers and full WDM systems are included in the CAD. And finally, chip to chip packaging of both electric and optical interconnects are demonstrated.

4 Increase the Efficiency of Silicon Modulators

Modulation is a basic functional requirement for any interconnects technology. Although the current free-plasma-dispersion effect based silicon electro-optic modulator can run at a speed up to 40GHz, there is still speed limitations or thermal tuning issues existing. This chapter mainly introduces efforts to increase the efficiency of silicon modulators. First the DC Kerr modulation effect of silicon nanocrystals is observed as a candidate for developing future high speed modulators; then a hybrid silicon lithium niobate modulator is demonstrated, which does not have the carrier loss and RC delay issues that limit silicon modulators; and finally a micro-oven design is invented for increasing the thermal tuning efficiency of existing silicon electro-optic modulators.

4.1 Observation of DC Kerr Modulation from Silicon Nanocrystals

4.1.1 *Introduction*

As mentioned in Section 2.4. The only practical fast electro-optical modulation on silicon photonic is based on free-carrier plasma dispersion (FCPD) effect, and it has been demonstrated with speed up to 40Gbit/s. It comes with inherent tradeoffs in free-carrier lifetime, device footprint, power consumption and temperature stability [90].

Although the third order nonlinearity in crystal silicon is comparatively weak. Low dimensional Si (porous silicon or SiNcs) have been proved to be very promising material for nonlinear application [91]. In comparison with porous silicon, SiNcs embedded in amorphous silica are better candidates for photonics, because of their robustness, stability and their fully compatibility with the mainstream CMOS technology [92]. And it has been shown in several studies that the AC Kerr coefficient of silicon nanocrystals is enhanced by two-to-four orders of magnitude over crystalline silicon[93]. And ultra-fast all-optical modulation in slot waveguides embedded with silicon nanocrystals oxide has been demonstrated on 1550nm wavelength [94].

Present SiNcs researches are focused on the preparation of SiNcs embedded in an oxide host. Methods applied for preparation inlcude Si ion implantation into high quality oxide [95], sputtering of Si rich Oxide [96], reactive evaporation of Si rich oxide [97], amorphous Si/SiO2 super lattices approach [98], solution processable Hydrogen Silsesquioxane (HSQ) [99]. All of them have different behaviors due to differences in size, surface passivation and shape distortion. Many parameters like gas ratio, pressure, temperature, process time during the fabrication would influence the effect dramatically. To make the best electro-optic SiNcs modulator, we need to find a proper method to

fabricate the SiNcs with highest Kerr coefficient. Thus, we need a direct and convenient method to measure the nonlinear property of fabricated sample.

Z-scan method is popularly used to measure the third order nonlinearity of SiNcs [100]. However we still lack of a method to directly provide the DC Kerr effect information[101] since our purpose is making electro-optic modulators. Here we demonstrated a new method by exploiting the attenuated total reflection setup to measure the DC Kerr effect of the fabricated SiNcs.

4.1.2 *Total Internal Reflection*

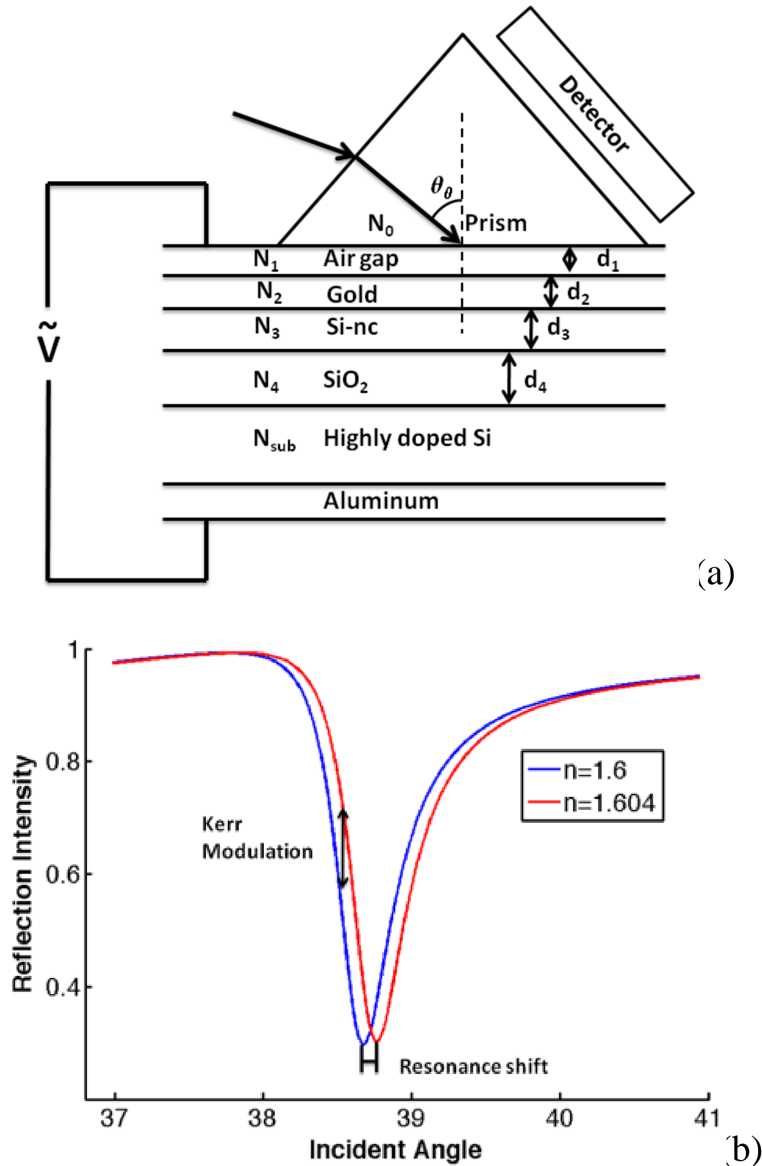


Fig. 4.1. Schematic of ATR (a) Sample structure and basic construction of ATR setup (b) Simulated modulation of refractive index change to resonance angle shift

A basic attenuated total reflection structure used in this work is shown as Fig. 4.1(a), and the detail of Matlab code is attached in the Appendix I. Since our sample is actually an

assembly of many thin films with different thickness d_j where the refractive index of each film is

$$N_j = n_j - ik_j \tag{4.1}$$

The reflectance of the sample can be calculated by the concept of optical admittance [102] as

$$\begin{bmatrix} B \\ C \end{bmatrix} = \left\{ \prod_{j=1}^{q} \begin{bmatrix} \cos\delta_j & \frac{i\sin\delta_j}{\eta_j} \\ i\eta_j \sin\delta_j & \cos\delta_j \end{bmatrix} \right\} \begin{bmatrix} 1 \\ \eta_{sub} \end{bmatrix} \tag{4.2}$$

Where q is number of layers above substrate, η_{js} is the tilted optical admittance calculated for s polarization as

$$\eta_{j_s} = N_j \cos\theta_j = \sqrt{N_j^2 - N_j^2 \sin^2\theta_j} \tag{4.3}$$

According to Snell's law and the parallel properties of the film stack

$$N_0^2 \sin^2\theta_0 = N_j^2 \sin^2\theta_j = N_{sub}^2 \sin^2\theta_{sub} \tag{4.4}$$

Where $\theta_0$is the incidence angle, θ_j is the angle in the other films. So

$$\eta_{j_s} = \sqrt{N_j^2 - N_0^2 \sin^2\theta_0} = \sqrt{N_j^2 - n_0^2 \sin^2\theta_0} \tag{4.5}$$

And tilted optical admittance for p-wave is

$$\eta_{j_p} = \frac{N_j^2}{\eta_{j_s}} \tag{4.6}$$

And

$$\delta_j = \frac{2\pi N_j d_j \cos\theta_j}{\lambda} = \frac{2\pi d}{\lambda}\sqrt{N_j^2 - N_j^2 \sin^2\theta_j} = \frac{2\pi d}{\lambda}\sqrt{N_j^2 - n_0^2 \sin^2\theta_0} \quad (4.7)$$

Finally the reflectance can be calculated as

$$\rho = \frac{\eta_0 B - C}{\eta_0 B + C} \quad (4.8)$$

$$R = \rho\rho^* \quad (4.9)$$

By plotting the reflection of TM mode incidence light as a function of incidence angle in Fig. 4.1(b), we can see a resonance angle where the reflection is attenuated. This is because the light is guided into the gold film and forms a Surface Plasmon guiding mode.

4.1.3 ***Experimental Setup***

The samples are fabricated based on a highly doped silicon wafer (4mΩ-cm). Then 2.75μm of wet oxide is deposited on top of the silicon wafer as substrate for SiNcs growth.

Samples of three kinds of conditions are made as shown in Table 4-1. One micron of silicon rich oxide film was deposited on the silicon dioxide substrate by plasma enhanced chemical vapor deposition (PECVD) using N_2O and SiH_4 at a ratio of 13.8:1 as precursor gas. After the deposition, 3 minutes of rapid thermal annealing (RTA) is performed in N_2 environment at two different temperatures (800C and 1100C). Consequently, SiNcs is developed.

In another sample, Hydrogen Silsesquioxane (HSQ) solution (XR1461) was spin coated at 500rpm on the same substrate, and 3 minutes of RTA at 1100C is done to develop SiNcs.

After SiNcs are developed, the back side of the sample is deposited with Aluminum as one of the electrodes. And 35nm of gold is evaporated on top of the SiNcs layer as both the other electrode of the sample and the guiding layer of surface Plasmon.

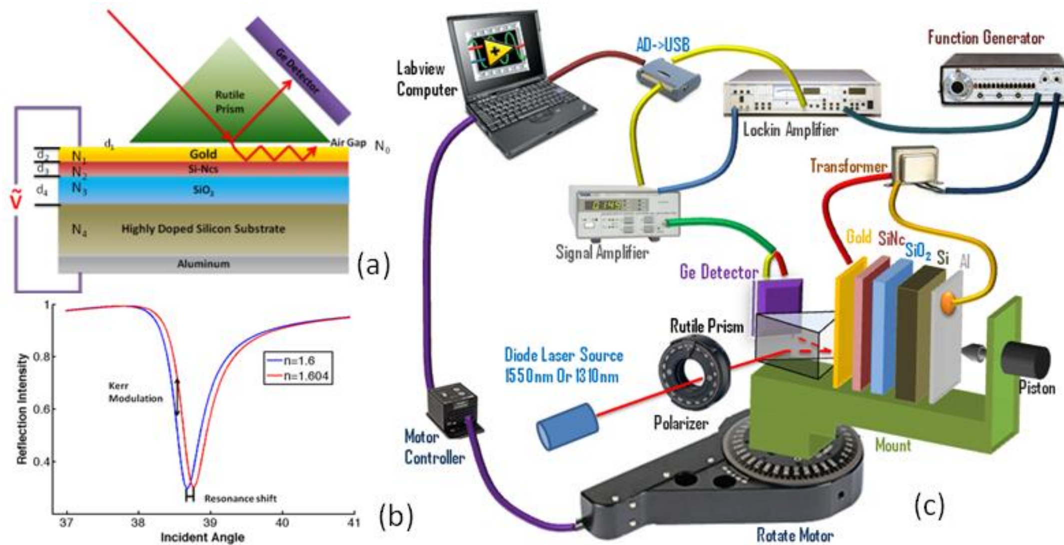


Fig. 4.2. Schematic of the experimental setup: (a)Sample structure and prism coupled ATR setup. (b) Simulated ATR resonance for two different SiNcs refractive indices (c) Detailed experiment set up

In order to directly measure the DC Kerr effect of the deposited silicon nanocrystals, an attenuated total reflectance (ATR) setup is used as seen in Fig. 4.2(a). In the ATR setup, the surface Plasmon resonance is excited in a thin gold metal film. This resonance only occurs at a very specific evanescent wave vector, which is excited by using a prism with

light incident at the Plasmon resonance angle. In our setup, a gold film is deposited on top of the wafer before being pressed into the prism using an air-piston, seen in Fig. 4.2(c). A plot of total reflected power, blue line of Fig. 4.2(b), shows the attenuation versus incidence angle, where the sharp Plasmon resonance is seen. In the testing setup, a rotation stage allows precise control of the incident angle, and a germanium detector attached to the output of the prism collects the reflected power.

The ATR resonance is very sensitive to the refractive index of the silicon nanocrystals film, as seen in Fig. 4.2(b). Therefore, it can be used to directly measure refractive index changes caused by the DC Kerr effect. This is realized by applying a voltage (kHz frequency) to the sample. Since the sample is simply a capacitor, the electric field will be applied to the SiNcs. The change of the index can be derived as:

$$\square = \varepsilon\square^{(1)}(\omega)\square(\omega) + 3\varepsilon\square^{(3)}(\omega;\omega,0,0)\square(\omega)\square(0)\square(0) \qquad (4.10)$$

From this equation, the actual refractive index change can be expressed as:

$$\Delta n = \frac{3}{2n(\omega)}\chi^{(3)}(\omega;\omega,0,0)[E(0)]^2 \qquad (4.11)$$

In order to determine the refractive index change experimentally, we measure the power changes in the light intensity at different applied voltage. Based on the slope of the curve, the resonance shift can be obtained by $\Delta I/(dI/d\theta) = \Delta\theta$. Using thin film optical

simulations, we obtain the change in resonance angle over refractive index change, $d\theta/dn$. Finally, the refractive index change is obtained using $\Delta\theta/(d\theta/dn)= \Delta n$. Thus, the DC Kerr constant K is obtained, knowing the applied electric field.

4.1.4 ***Testing Results***

The measurement results of a typical silicon nanocrystals sample are seen in Fig. 4.3. The detector signal is shown in Fig. 4.3(a); along with the lock-in amplifier signal (Fig. 4.3 (b)), which is proportional to the intensity change. From the model, we obtain the refractive index modulation as a function of applied electric-field. The fitting is conspicuously quadratic, proving that the observed modulation is due to the DC Kerr effect.

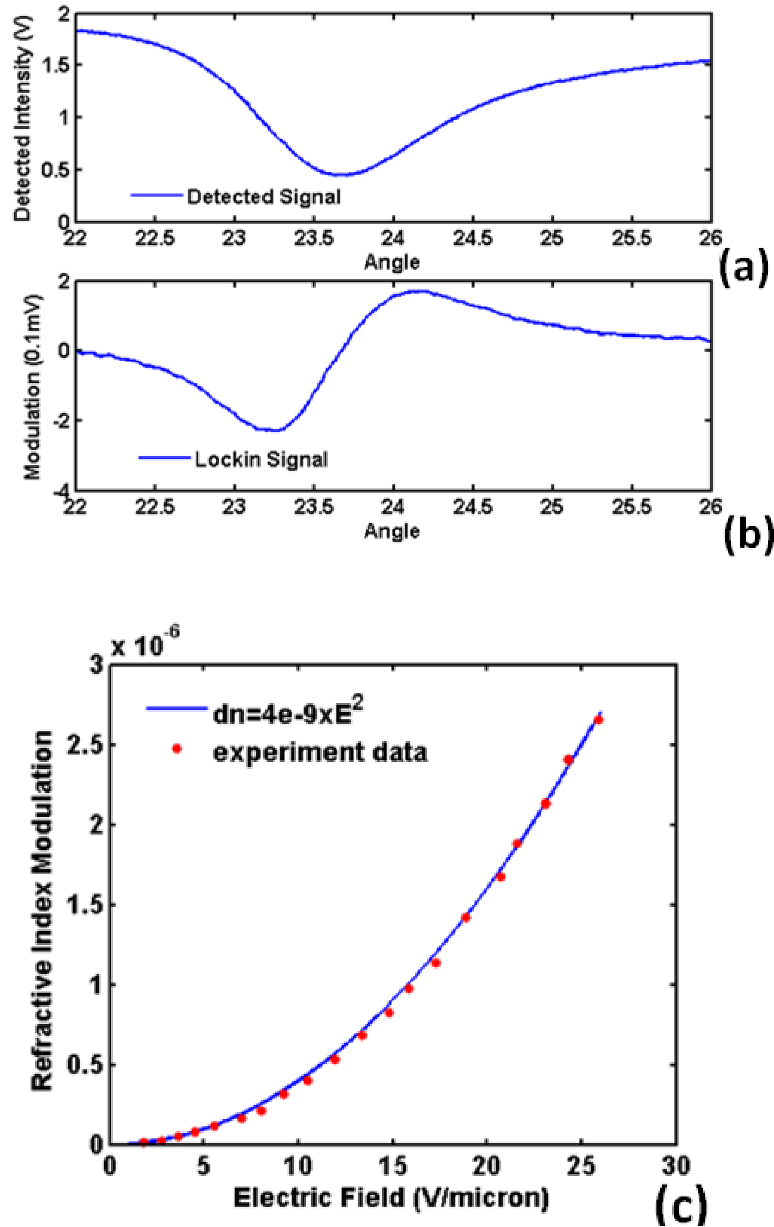


Fig. 4.3. Experimental results (a) detector intensity signal. (b) lock-in amplifier signal (c) fitted modulation curve

For comparison, we measured a sample without silicon nanocrystals and did not observe any modulations. And the measurement results of all samples are presented in detail as Table. 4.1.

Table. 4.1. Sample preparation

Sample #	Process	Thickness	Annealing temperature	K(m/V^2,)
S1	PECVD	1000nm	800 ℃	2.6e-15
S2	PECVD	1000nm	1100 ℃	8.3e-16
S3	HSQ Spin coat	400nm	1100 ℃	1.4e-16

Then a photoluminescence is then done on the sample (without gold film) as Fig. 4.4. The oscillation of the spectrums because the SiO2 layer under SiNcs is working as resonance cavity. The HSQ sample gives very small amount of PL which tell not many SiNcs exist, and that's why it didn't give good modulation. PECVD+1100C sample peaks at 860nm wavelength and have the most amount of photons at PL, this tells the SiNcs crystallized well at large size. PECVD+800C sample peaks at 750nm wavelength and have a bit lower amount of photons at PL which means the SiNcs crystallized at smaller sizes than 1100C sample.

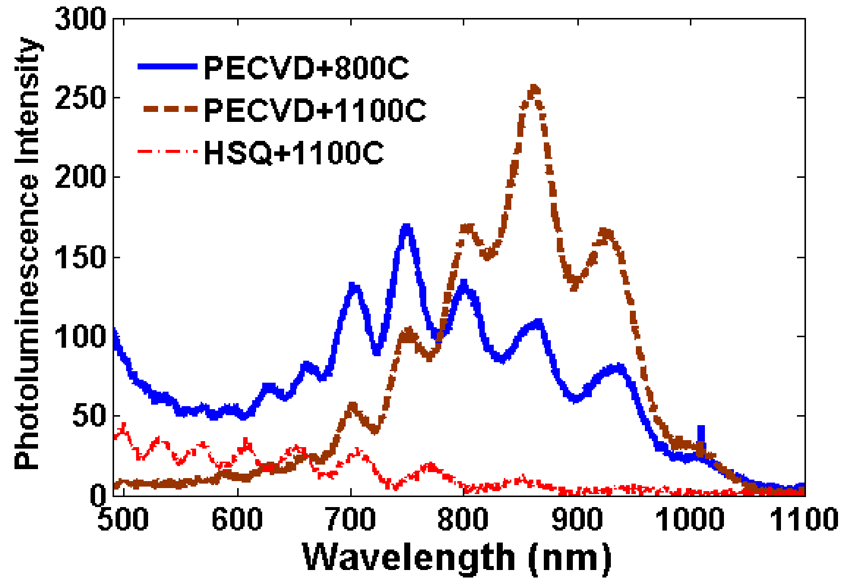


Fig. 4.4. Photoluminescence of different sample: The red dot curve is the PL of HSQ sample, the brown dash curve is the PL of PECVD sample with 1100C annealing, and the blue solid curve is the PL of PECVD sample with 800C annealing.

Since the nonlinear effect of SiNcs results from the quantum confinement and refractive index mismatching, a better DC Kerr effect should happened at a smaller size SiNcs. And the PL results fit the DC Kerr effect results well.

4.2 Hybrid Si- $LiNbO_3$ Modulator

4.2.1 *Introduction*

As mentioned in Section 2.4, due to the symmetric property of the silicon crystal lattice, we cannot observe the $\chi(2)$ nonlinear effect from silicon. We have to use free carrier plasma dispersion effect to make electro-optical modulators even though its relatively small in effect. Lithium Niobate modulators, on the other hand, have high speed and large

modulation effect based on the second-order nonlinear Pockels effect. However, $LiNbO_3$ modulator is normally ~cm scale size due to its low refractive index contrast and large optical mode. There has been lots of efforts to achieve strong $\chi(2)$ nonlinear optical effects in the CMOS compatible silicon photonic platform. For example, a significant Pockels effect was realized in silicon by using strain to break the crystal symmetry [103][32]. In other cases, $\chi(2)$ materials, such as nonlinear polymers [104][105] or Aluminum Nitride [106] have been deposited and used to enable electro-optic modulation. And several groups have bonded $LiNbO_3$ films onto silicon waveguides or substrates [107][108][109]. On the other hand, the major drawback of Lithium Niobate ($LiNbO_3$) platform is the low index contrast of standard Titanium diffused Lithium Niobate waveguides (Ti: $LiNbO_3$). Consequently, it is challenging to realize densely integrated photonic circuits on the $LiNbO_3$ platform. Some work has been done to either etch $LiNbO_3$ [110][111] or deposit high index chalcogenide glasses [112]. However, the devices are still an order of magnitude larger than their silicon photonic counterparts. In order to overcome this, some groups have recently bonded $LiNbO_3$ films onto silicon waveguides or substrates [107][108][109][113][114]. However, these approaches require a complicated ion implant and bonding process. In contrast, here we combine the best of silicon photonic and $LiNbO_3$ by simply depositing high index hydrogenated amorphous silicon (a-Si:H) on $LiNbO_3$ substrates to realize a

compact and efficient active hybrid silicon:$LiNbO_3$ platform. This platform will enable a multitude of ultra-high performance photonic integrated circuits for communications and RF signal processing. In addition, the $\chi(2)$ nonlinearity can be leveraged for quantum and nonlinear optics applications.

Our group has previously shown that, the loss of plasma enhanced chemical vapor deposited (PECVD) hydrogenated amorphous silicon (a-Si:H) waveguides is less than 3dB/cm [115]. Furthermore, the waveguides have nearly the same refractive index as crystalline silicon waveguides (~3.45). Therefore, it is possible to realize very compact photonic circuits by simply depositing a-Si:H at temperatures lower than 400 ℃. Here, we present our results on a hybrid a-Si:H-$LiNbO_3$ modulator where the same a-Si:H material is deposited on a $LiNbO_3$ substrate. We have optimized the a-Si:H waveguide dimensions in order to maximize the overlap of the optical mode with the electro-optically active $LiNbO_3$ material. As a result, it is possible for ~75% of the mode to sense an electrically induced refractive index change in the $LiNbO_3$ material. Furthermore, since the optical mode is strongly confined to the a-Si:H waveguide width (<1 m), the electrodes can be placed very closely to each other, significantly enhancing the applied electric field. Therefore an electro-optic modulator with less than 2V-cm response is possible, which is nearly an order of

magnitude smaller than typical. Here we show a proof of concept and demonstrate >4GHz modulation in a small footprint of <1mm.

4.2.2 *Device Design and Simulation*

A schematic of the proposed hybrid a-Si:H/$LiNbO_3$ waveguide modulator is shown in Fig. 4.5, where an a-Si:H waveguide core is patterned on top of a $LiNbO_3$ substrate. The optical mode for this a-Si:H waveguide (700nm wide, 90nm thick) is superimposed in the image along with the simulated electric field induced by applying a voltage to the metal electrodes. The strong lateral optical confinement of the a-Si:H waveguide ensures that the metal electrodes can be spaced closely together (3microns in this case). Furthermore, the thin a-Si:H material allows a significant amount of the optical mode to strongly sense the $LiNbO_3$ substrate. Therefore, it is possible to obtain both low voltage and compact electro-optic modulation in this hybrid platform.

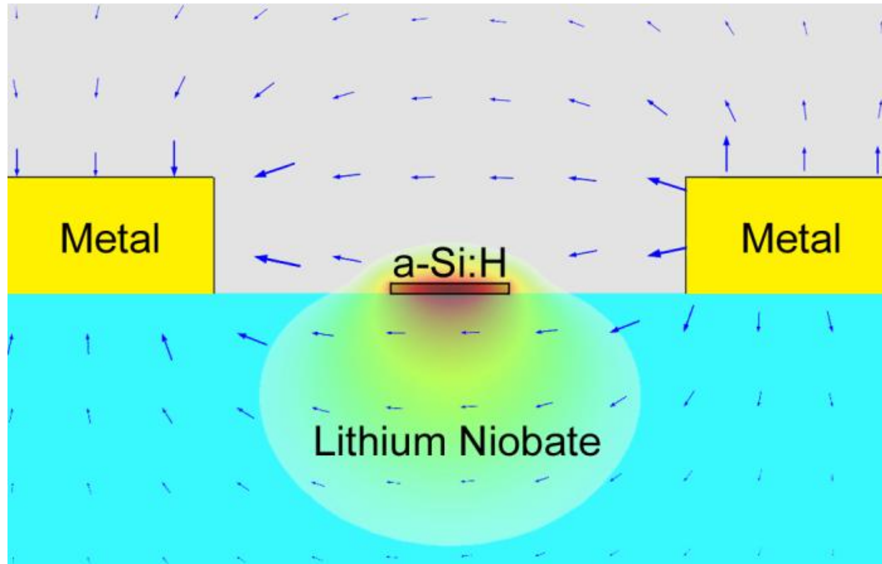


Fig. 4.5. Schematic cross-section of the hybrid silicon-$LiNbO_3$ modulator. The light is confined to the $LiNbO_3$ substrate by a thin a-Si:H waveguide. The metal electrodes provide an RF electric field that is used to induce the Pockels effect in the $LiNbO_3$.

In order to enhance the overall Pockels modulation effect we need to ensure as much of the optical mode is in the $LiNbO_3$ region as possible. At the same time, we need to make sure that the optical mode is compact, so that devices can be realized with significantly smaller footprints. This can be well understood from the mode simulations shown in Fig. 4.6 (a-d). In all cases the waveguide has a 700nm width but it is clearly seen that in order to realize an appreciable amount of light in the $LiNbO_3$ substrate the a-Si:H must be relatively thin, approximately less than 100nm.

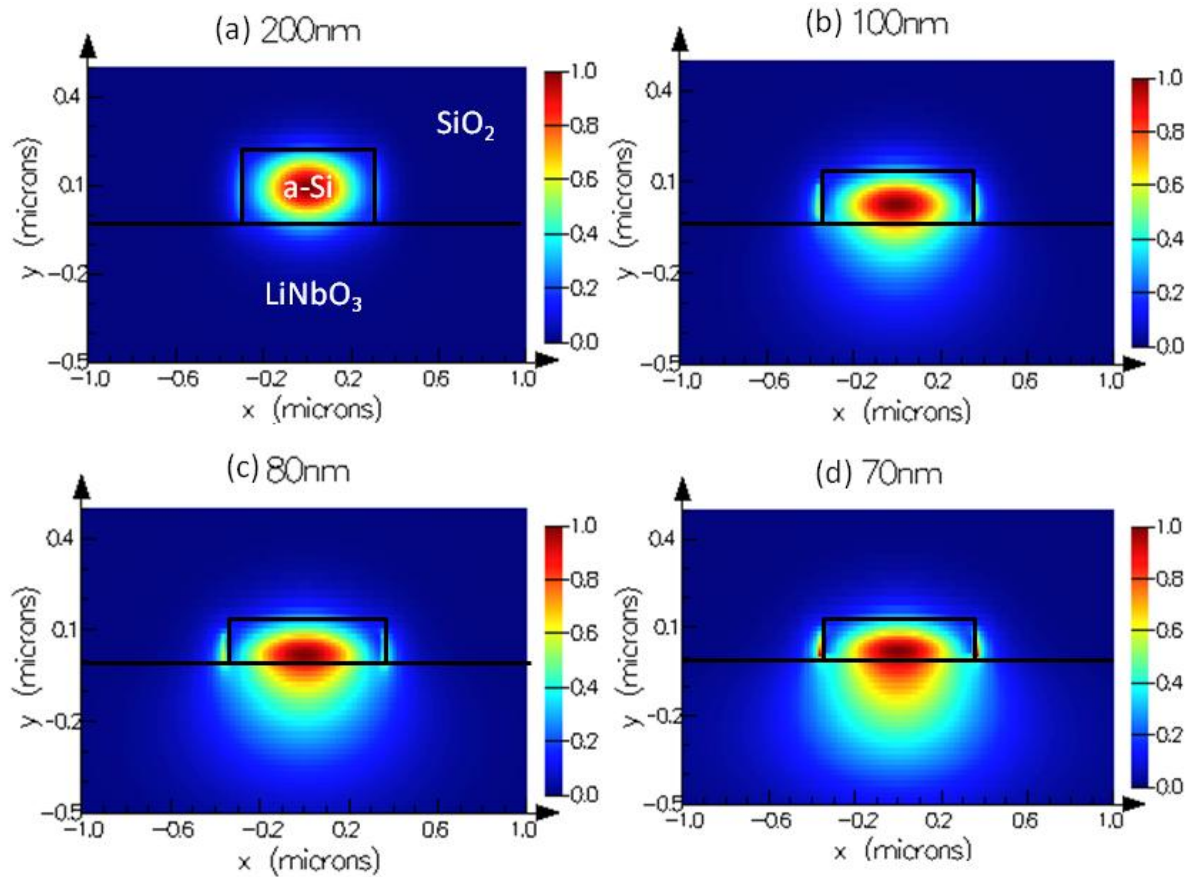


Fig. 4.6. Optical mode of a-Si:H waveguide on a $LiNbO_3$ substrate (a) Waveguide thickness 200nm, (b)waveguide thickness 100nm, (c) waveguide thickness 80nm, (d) waveguide thickness 70nm

To further investigate the influence of the profile of optical mode on the modulation strength, a series of simulations are summarized in Fig. 4.7(a). We have once again fixed the width of the waveguide to be 700nm and varied the a-Si:H thickness from 80nm to 200nm. At each thickness, we calculate the efficiency of the effective refractive index change in the $LiNbO_3$ material, which is simply obtained by applying a small change to the $LiNbO_3$ refractive index and seeing the net change in the overall effective index of the mode. As we can see from the blue curve in Fig. 4.7 (a) the effective index change from the $LiNbO_3$ modulation increases as the

waveguide becomes thinner. This is simply because the amount of light in the $LiNbO_3$ increases as the waveguide is thinned. However, there is a limit to how thin it can be made, which in this specific waveguide width is approximately a thickness of 80nm. It is at this point that the effective index (red curve in Fig. 4.7 (a)) reaches the same value as the $LiNbO_3$ substrate, and consequently the mode is no longer strongly confined by the a-Si:H waveguide and will be very leaky. Fig. 4.7 (b) looks at the dependence on the waveguide width for several a-Si:H thicknesses. As we can see, all of the curves follow the same general trend, specifically that thinner waveguides enhance the modulation effect. However, as the waveguides get narrower the required waveguide thickness increases and as a result the ultimate effective index change efficiency that can be obtained is decreased. Therefore, it is better to have wider waveguides to reach the ultimate modulation efficiency. However, there is a tradeoff in device size as the waveguide is made wider. As a result, there inherently is a tradeoff and we have selected the 700nm width as a reasonable tradeoff point.

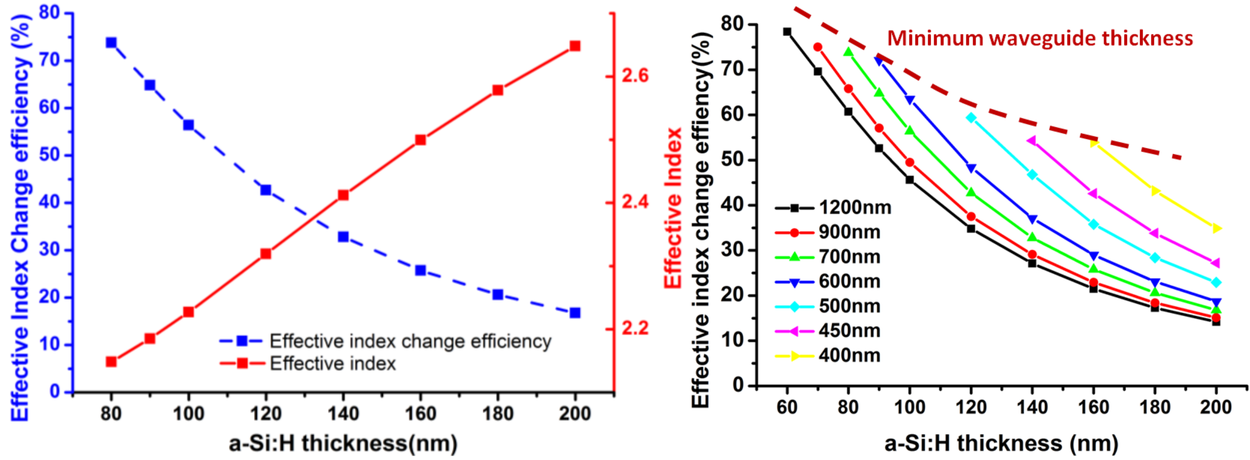


Fig. 4.7. (a)Relative index change efficiency for a 700nm wide waveguide for different a-Si:H thicknesses. (b) Waveguide width dependence on index change efficiency.

4.2.3 *Fabrication*

The fabrication starts from an x-cut $LiNbO_3$ wafer, which will yield the maximum Pockels coefficient (r_{33}) for the lateral metal electrode configuration presented in Fig. 4.5. Then a-Si:H is deposited using plasma enhanced chemical vapor deposition (PECVD) at 200C, as depicted in Fig. 4.8(a). The deposition parameters of the film are given in Table. 4.2 [115]. Then the strip waveguides, 700nm wide, are patterned using electron beam lithography followed by inductively coupled plasma (ICP) chlorine etch similar to our standard silicon waveguide fabrication process[116]. After the a-Si:H is fully etched, 1 micron of SiO2 is deposited over the structure also using PECVD at a temperature of 400C as shown in Fig. 4.8 (c). Next, contact holes are patterned using contact lithography as shown in Fig. 4.8 (d) and followed by RIE etching of SiO2. Then the contact hole is filled

with 100nm of gold. Finally, lift-off of the electrode metal is performed in an acetone bath (Fig. 4.8(f)).

Table. 4.2. a-Si:H deposition parameter

Hydrogen (H2) flow	700sccm
Silane (SiH4) flow	60sccm
RF Power	100W
Substrate temperature	200C
Pressure	4Torr

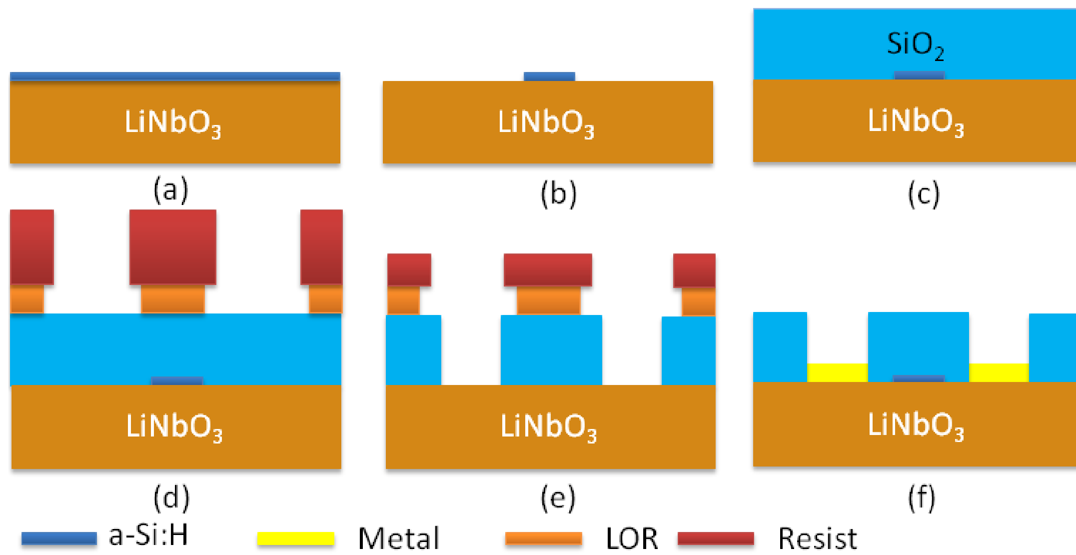


Fig. 4.8. Fabrication process of silicon electro-optical modulator

In order to convert the electric field induced refractive index change into an optical intensity change, the waveguides are patterned into a Mach-Zehnder Interferometer (MZI) configuration as shown in Fig. 4.9. The modulation region of the device is ~700 microns long which is smaller than traditional $LiNbO_3$ MZI modulators. Furthermore, there is ~100

microns length difference in one branch of the MZI in order to directly obtain the modulation induced phase change from the wavelength-dependent transmission of the MZI, as shown in the results section.

Fig. 4.9 (a). Microscope image of the hybrid Si-$LiNbO_3$ modulator integrated into a Mach-Zehnder interferometer. The total size of the device is only 1mm.

4.2.4 *Result and Discussion*

The experimental setup used to measure the modulation efficiency is shown in Fig. 4.10. Optical measurements are performed using a tunable infrared laser that passes through a polarization controller, a collimator and a lens focused on the chip facet. Light is efficiently coupled in and out of the chip via nano-taper mode converters [83]. The output from the chip is collimated by the lens and is collected by another collimator. The light is detected by a photo-detector in order to obtain the transmission spectrum of the MZI by scanning the tunable lasers wavelength. Alternatively the output signal is amplified by an Erbium Doped Fiber Amplifier (EDFA) and measured by an optical detection module in a

sampling oscilloscope. The modulator is electrically biased by DC probes and an RF probe that is driven by a tunable RF source.

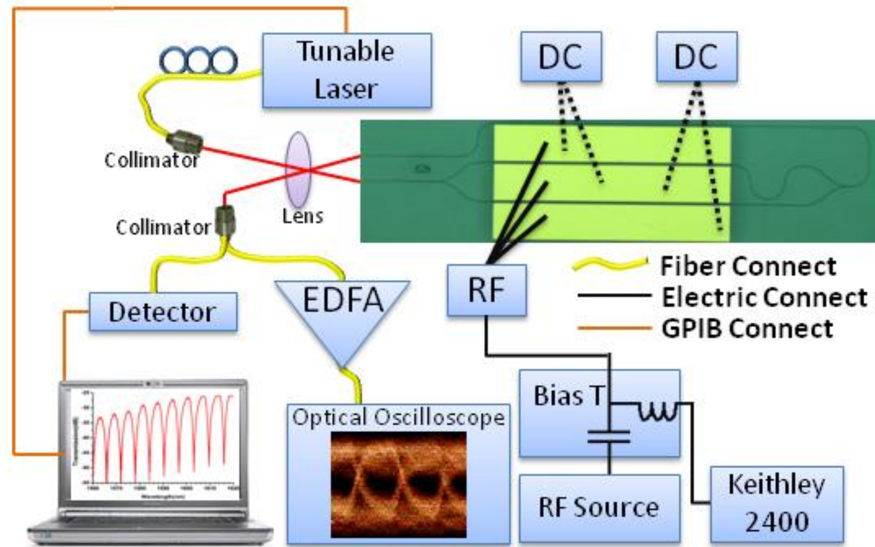


Fig. 4.10. Experimental Setup used to characterize the MZI modulator

DC analysis is performed by measuring the devices spectral response for various applied electric fields. The DC bias is operated in a push and pull configuration, where the DC voltage is applied to the center electrode and the two outside electrodes are grounded. Since the Pockels effect induces either a positive or negative index change based on the direction of the electric field, the effective phase change of the MZI is doubled in this configuration. The spectral response at various electric fields is shown in Fig. 4.11, where the blue line is the spectrum without bias. It is seen that the MZI has a high extinction of 20dB and the 100 microns length difference yields a Free-Spectral-Range of 6.2nm. It is also seen that there is a linear shift in the wavelength spectra for different Electric fields as

expected from the $LiNbO_3$ Pockels effect. However, the overall switching field (defined as the field required to obtain a phase shift) of the modulator is relatively high, approximately 10V/micron. From this we determined that the effective Pockels coefficient of our waveguide configuration is only ~10pm/V, whereas bulk $LiNbO_3$ material has an r_{33}=33pm/V. The primary reason we do not reach the optimal efficiency is because the deposited a-Si:H was found to be 150nm thick, significantly thicker than anticipated. As seen in Fig. 4.7(a), only ~30% of the optical mode is sensing the $LiNbO_3$ refractive index change, which confirms the measured 10pm/V efficiency. In the future, by reducing the waveguide thickness to <100nm it will be possible to realize a doubling in modulation efficiency. In turn, the overall performance of this new hybrid modulator can be calculated using the standard $V\pi L$ figure of merit. Specifically, assuming the electrodes are conservatively spaced 3um apart, which induces negligible optical loss, then the switching voltage is approximately $V\pi L$~1.6V-cm, which is significantly smaller than typical $LiNbO_3$ modulators [117]. Therefore, with this new hybrid waveguide approach it is possible to realize significantly smaller modulators with a simple silicon deposition waveguide process.

Optical measurements are performed using a tunable infrared laser coupled through a polarization controller, a fixed focus collimator to a lens focused on the chip facet. Light is coupled in and out of the chip via nano-taper mode converters. Output from the chip is converted to parallel beam by the same lens, and finally detected by a photo-detector.

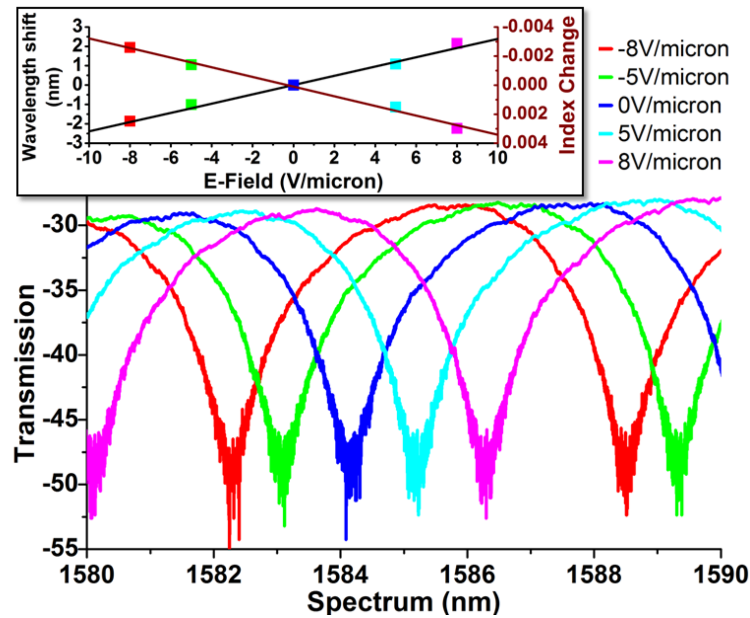


Fig. 4.11. Spectrum shifting driving by DC electric field

We have also measured the RF response of the modulator as seen in Fig. 4.12 by sweeping an RF source from 100MHz to 13GHz. The modulated optical signal is measured as a function of frequency using a sampling oscilloscope with a 30GHz bandwidth photo-receiver module. The resulting data is given in Fig. 4.12, which shows that the MZI modulator has a 3-dB roll-off frequency of ~2.5GHz. The RF speed is limited mainly because we haven't optimized the electrode design for high frequency signals. In the future

we will optimize the coplanar electrode design to yield both optimal impedance and phase difference between the optical and electrical signals. Regardless, we are still able to achieve an open eye diagram at 4.5Gb/s by applying a Non-Return-to- Zero (NRZ) 2^7-1 Pseudo Random Bit Sequence using an RF signal with a ±5V swing as shown in the bottom left inset of Fig. 4.12.

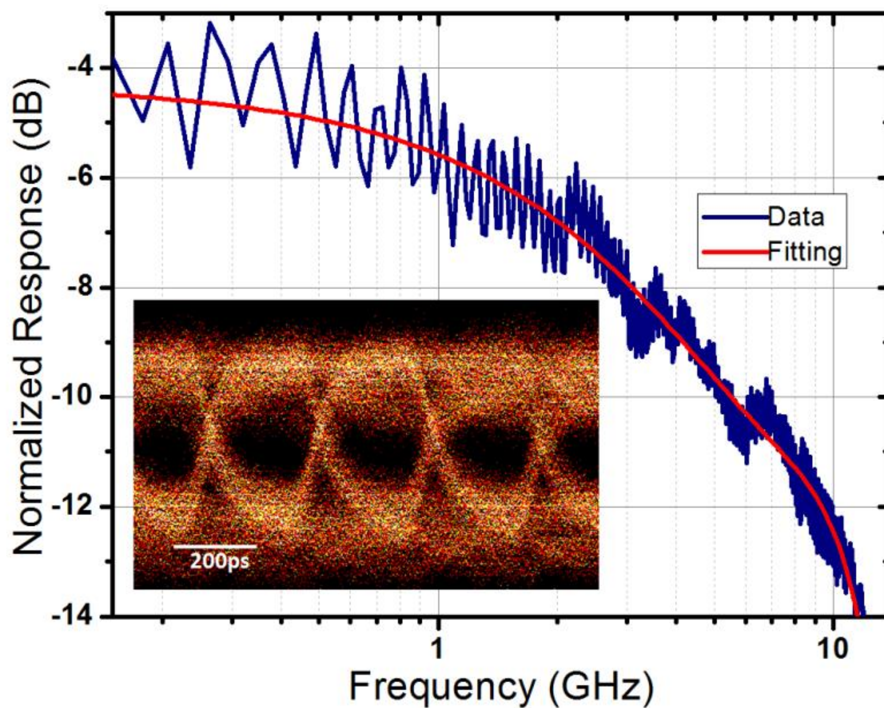


Fig. 4.12. RF response of the modulator at different frequencies. The inset shows an open eye-diagram for a 4.5Gb/s PRBS 2^7-1 signal.

We have demonstrated a hybrid silicon-LiNO3 modulator that utilizes a simple amorphous silicon deposition process to realize both tight confinement of the optical mode and strong modulation efficiency. Consequently, this work has proven that it is possible to realize significantly smaller $LiNbO_3$ modulators that operate with low voltages (<2V-cm).

In addition, the integration approach can be used to realize a multitude of compact and low loss devices that are seamlessly integrated on a single platform.

4.3 Efficient Thermal Control of Silicon Photonic

4.3.1 *Introduction*

As mentioned in section 3.3, one challenge for chip level high speed interconnects with silicon photonic is the robustness. Silicon photonic devices are highly sensitive to temperature changing and fabrication defects. Therefore, an efficient thermal control is necessary to stable the silicon photonic platform. This brings another problem, if we want to exploit silicon photonic in super computer system, the power consumption from thermal control part could add up quickly. Therefore, it becomes important to minimize energy consumption for individual thermal control.

The most traditional way of realizing thermal control is flowing current through a metal resistor over the cladding oxide of silicon [118]. However, heating efficiency in this form is very low (<50%). In order to improve the performance researchers have integrated air trenches to confine the thermal energy around the silicon waveguide [119]. However, the integration of air trenches, especially underneath the waveguide, is challenging in a traditional CMOS process, and it may bring the problem of unstable. Other approaches have

been taken where the heaters are directly integrated into the Silicon with minimal impact on the optical mode, resulting in high efficiencies [120]. However, this comes with a tradeoff in real estate when the heater must be integrated with an electro-optic modulator, reducing overall efficiency of both the modulator and the thermal control.

Here we present a new silicon photonic heater based on micro-oven structure to enhance heating efficiency of silicon photonic devices. The micro-oven is seamlessly integrated in a CMOS photonic fabrication flow since it does not require additional process steps or even materials. It directly makes use of the standard metal contacts/via's used to connect upper Metal layers to the active silicon devices. Furthermore, the metal contacts effectively form "oven" around the silicon waveguide, in turn, confining the thermal energy.

4.3.2 *Design and Simulation*

The traditional approach for achieving thermal control is with a high resistivity metal. To avoid optical loss the resistor is normally separated from the silicon waveguide by a thick cladding oxide (>1 µm). Unfortunately, the poor thermal conductivity of silicon oxide (k=1 Wm^{-1} K^{-1}) results in a low thermal efficiency (η=34.1%), defined as the temperature of the silicon waveguide relative to the temperature of the heater, as seen in the 2D Finite-Element-Method (FEM) simulation in Fig. 4.13(a). In a modified approach, we channel heat

to the slab region of the silicon waveguide without affecting the optical mode by using a high thermal conductivity metal contact (k=400 Wm^{-1} k^{-1}), such as Copper, placed 1 μm away from the silicon waveguide. Furthermore, since the silicon slab has a higher thermal conductivity (k=149 Wm^{-1} k^{-1}) than oxide the heat is transferred relatively efficiently (η=82.6%), to the silicon waveguide, as seen in Fig. 4.13(b). We note that the metal thermal contact can be simply realized in a standard CMOS process by making use of standard via's that normally connect different layers electrically in a CMOS chip.

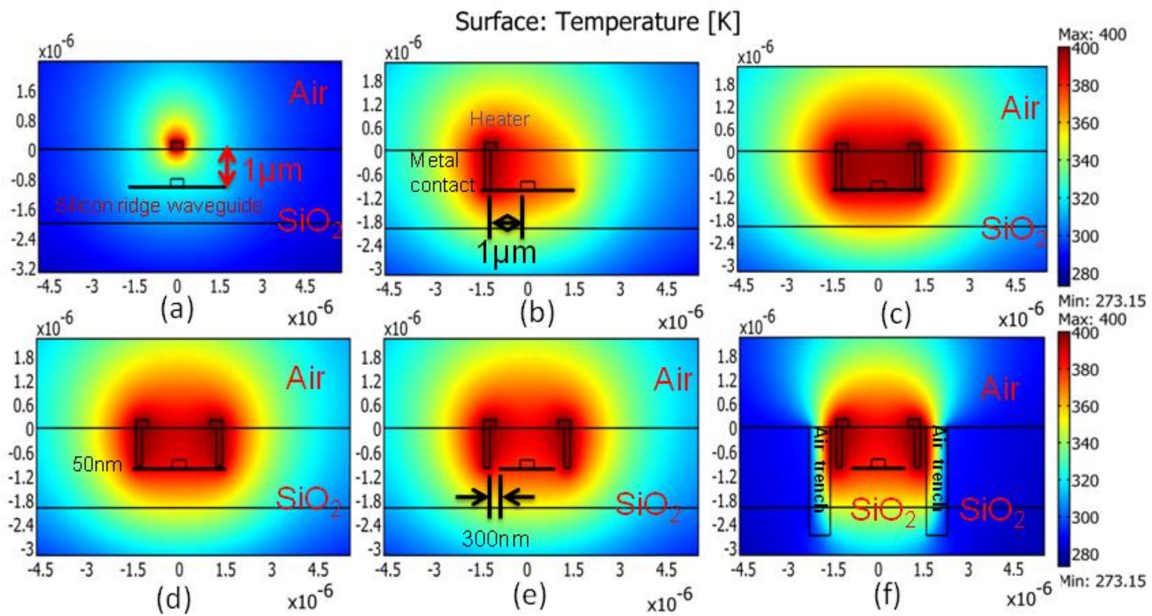


Fig. 4.13. FEM simulation of heating efficiency of (a) traditional top heater, (b) thermal contact on one side of the waveguide, (c) micro-oven heater consisting of two thermal contacts, (d) thermal contact at one side of the waveguide with a 300 nm electrical isolation gap, (e) micro-oven heater with electric isolation gaps and (f) micro-oven heater used in the experiment

To enhance the thermal efficiency further we add an identical thermal metal contact at the other side of the waveguide. This strongly confines the thermal energy in the central

region as seen in Fig. 4.13(c). As a result we achieve a very high efficiency of η=94%. We have named this heater design a "micro-oven" due to the similarity to any oven used in a kitchen (i.e. an oven consists of high thermal conductivity walls surrounding a low thermal conductivity region). Specifically, the device efficiently conducts and confines heat through the low thermal resistivity thermal contacts that completely surround the central waveguide region.

One of the primary goals of this work is to realize both high thermal efficiency and the ability to integrate the heater with electro-optic modulators. Unfortunately the micro-oven in Fig. 4.13(c) effectively introduces an electrical short across the waveguide; especially if the silicon has low resistance (i.e. is heavily doped as in a modulator). Therefore, the electric contact of the heater and the silicon waveguide has to be broken. We can either introduce a thin oxide insulating film between the contact and the silicon slab layer vertically or we can etch the silicon slabs surrounding the contact region. Here we do the latter by introducing a 300 nm gap between metal contact and silicon slab to ensure electrical isolation, as seen in Fig. 4.13(d). However, the thermal efficiency is reduced to η=76% in the case of the single thermal contact. However with the introduction of the micro-oven configuration, the overall heating efficiency is increased back to η=85.6% (Fig. 4.13(e)). Lastly, as seen in Fig. 4.13(f), we have simulated an un-optimized micro-oven

design that was used in the experimental results presented below. This design has an efficiency of only 59.1% because of limitations in the fabrication process we used. First, the thermal contacts were placed farther away (~2 microns instead of ~1 micron) due to lithography limitations. Secondly, we used a metal with a lower thermal conductivity [Aluminum (k=160Wm^{-1}k^{-1})] since Copper was not available for our process. Lastly, the heater was connected to the thermal contact using low thermal conductivity NiCr (k=30Wm^{-1}k^{-1}) and the slab region of silicon waveguide was not fully etched which dissipated heat away. Regardless, as we show below, this micro-oven design still doubles heating efficiency over a traditional top heater.

4.3.3 *Fabrication and Results*

To prove the micro-oven concept experimentally devices were fabricated at the Cornell Nanoscale Science & Technology Facility (CNF) including two sets of ring resonators, one with radius of 2.5 microns and another with 10 µm radius. Both ring resonator sets have either a traditional heater or a micro-oven heater. The fabrication starts from 250 nm thick silicon on a SOI wafer with a 3 microns of buffer oxide. Waveguides with a width of 450 nm are patterned with HSQ resist by electron beam lithography. After developing, the unprotected area is etched down by 200 nm by reactive ion etching under inductively

coupled plasma (ICP) chlorine chemistry, leaving 50 nm silicon slab next to the waveguide. Then 1.5 μm of PECVD Oxide is deposited over the waveguide as a cladding; and 80 nm thick NiCr is patterned over the ring resonator region with width of 1.5 microns as the heater source. The traditional heater configuration is then formed as shown in Fig. 4.14(a). After that, thermal contact holes are patterned and etched 1.5 microns away from the silicon waveguide. Aluminum is then deposited and lifted-off to fill the contact holes to serve as the thermal conductor and micro-oven chamber as shown in cross section view of micro-oven heater in Fig. 4.14(b). And finally 50 nm of gold is patterned as the contact pads for both types of heaters.

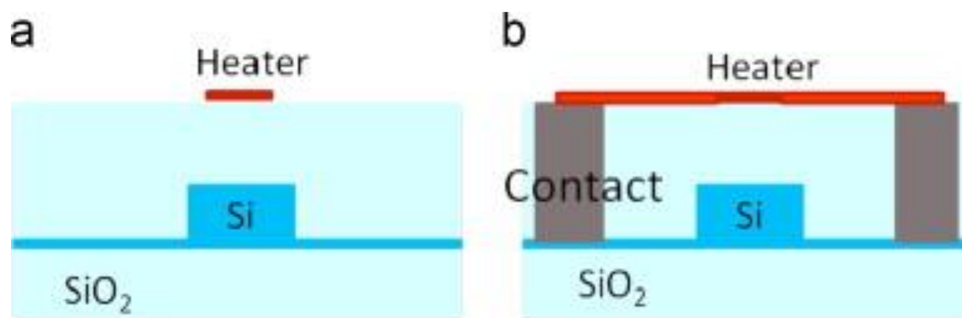


Fig. 4.14. (a) Traditional heater (b) Micro-oven heater

Fig. 4.15 shows the CAD design and corresponding fabricated ring resonator devices with either a traditional heater structure (Fig. 4.15(a)) or micro-oven design (Fig. 4.15(b)). Both designs use an identical omega heater structure that follows most of the ring resonator. The micro-oven is formed by adding thermal contacts that are thermally connected to the

heater structure with additional NiCr wire. These connections ensure relatively low thermal resistance but high electrical resistance, which is important to maintain so that most of the electrical current flows only through the omega heater and not the low electrical resistance Aluminum contacts. In Fig. 4.15(c) we have adapted the micro-oven to use a double wire heater, which has two round trips instead of single wire omega shape. The double wire provides both higher electrical resistance and flexibility in future implementations of electro-optic modulator designs.

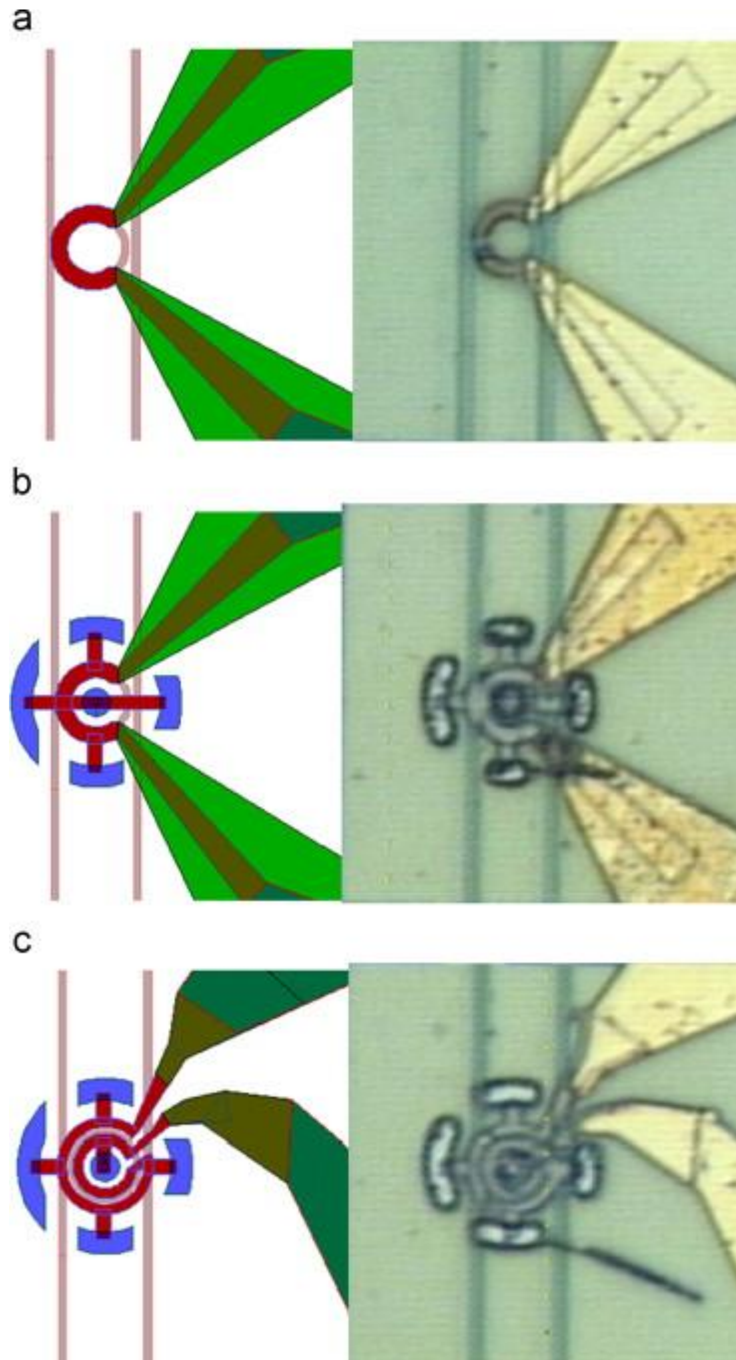
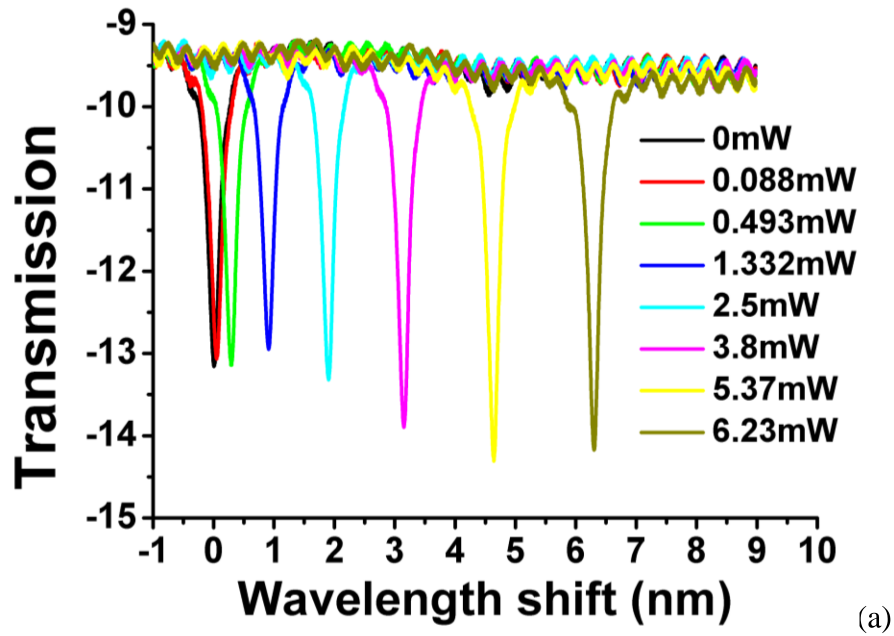
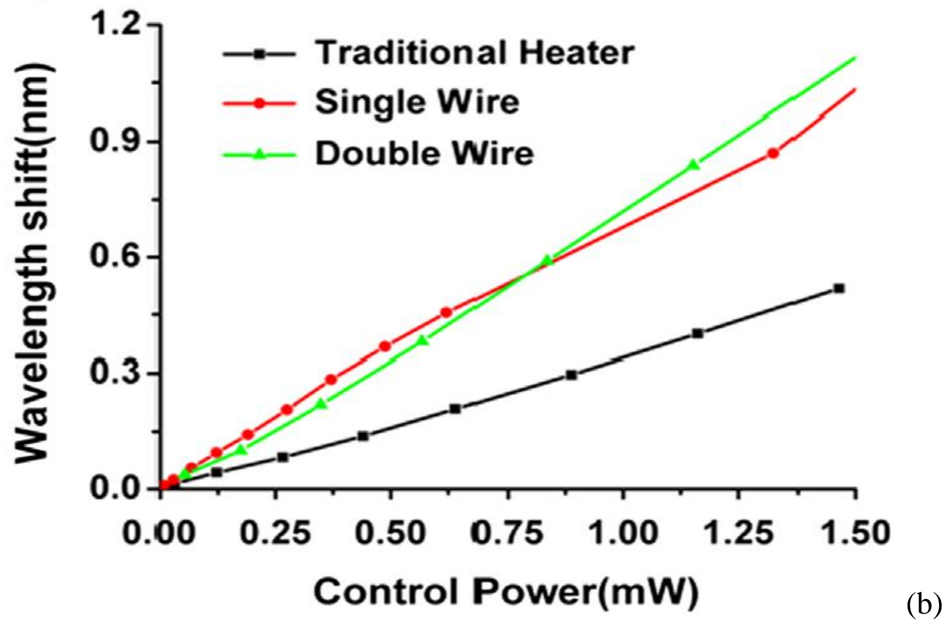


Fig. 4.15. CAD design and microscope image of 2.5 microns radius ring with (a) Traditional Heater design (b) Single wire micro-oven heater design (c) Double wire micro-oven heater design. The ring resonators in all of the designs are coupled to two waveguides in order to ensure near-critical optical coupling.

The measured spectral response of a 2.5 microns radius ring resonator with a micro-oven heater under different heating powers is seen in Fig. 4.16(a). The spectral behaviors of 2.5 microns radius devices with traditional heater design and double ring oven design is also extracted in Fig. 4.16(b) for comparison. We see that both micro-oven heater designs exhibit a wavelength shift of ~0.8 nm/mW while the traditional heater has a wavelength shift of only 0.35 nm/mW. Consequently, we see that the micro-oven doubles the heater efficiency.



(a)



(b)

Fig. 4.16. (a) Spectrum response of 2.5 microns radius micro-oven heater (b) Resonance wavelength shifting as function of input power

Additional testing is done on group of devices with 10 μm radius as well, and the comparison of their performance is shown in . We notice that the efficiency is four times

smaller in the 10 microns device than the 2.5 microns device. This is because for a given amount of heater power the thermal energy must be distributed over a four times larger area, effectively reducing the wavelength change. Regardless we still observe that the micro-oven configuration doubles heating efficiency over a traditional device. Lastly, in order to compare the measured results with our simulations we note that in the CAD design for the micro-oven, seen in Fig. 4.15(b), around 80% of the ring is covered by the oven design while 20% of the ring is covered by traditional heater. From the simulations we know that the traditional heater has an efficiency of η=34.1% while the un-optimized oven heater has efficiency of η=59.1%. Based on this we can estimate that the expected enhancement in efficiency is ~2 times as high, in good agreement with our measurements and within the uncertainty of the 2D simulations.

Table. 4.3.Comparison of traditional heater with single wire oven and double wire oven in rings with radius of 2.5 microns and 10 micron

Ring radius	**2.5 µm**	**10 µm**
Normal heater	0.35 nm/mW	0.07 nm/mW
Single wire oven	0.83 nm/mW	0.19 nm/mW
Double wire oven	0.80 nm/mW	0.19 nm/mW

4.3.4 *Discussion and Conclusion*

We have proposed a unique micro-oven heater to enhance the performance of traditional heater for silicon photonic devices. Both simulation results and experimental result confirm at least a doubling in thermal efficiency. We note that while we have not achieved the highest reported heating efficiencies (~1.8 nm/mW) this is primarily because we did not use an optimal micro-oven design. Specifically, we did not use metals with the highest thermal conductivities to connect the heater to the thermal contact and within the contact. And the thermal contacts were unnecessarily far away from the actual silicon waveguide. Consequently, thermal energy was not perfectly conducted through to the silicon waveguide as clearly seen in the simulations in Fig. 4.13 (c) and (f). Regardless, we still have proven that the micro-oven is a novel approach for enhancing heater performance. Furthermore, the design can be efficiently integrated with electro-optic modulators as seen in the schematic in Fig. 4.17. We note that an electric isolation gap is added between the silicon slab and the heater conductor, as seen in Fig. 4.13(b). The top down view of the design shown in Fig. 4.13(c) also uses the double wire micro-oven design in order to ensure efficient use of the entire ring for heating and modulation.

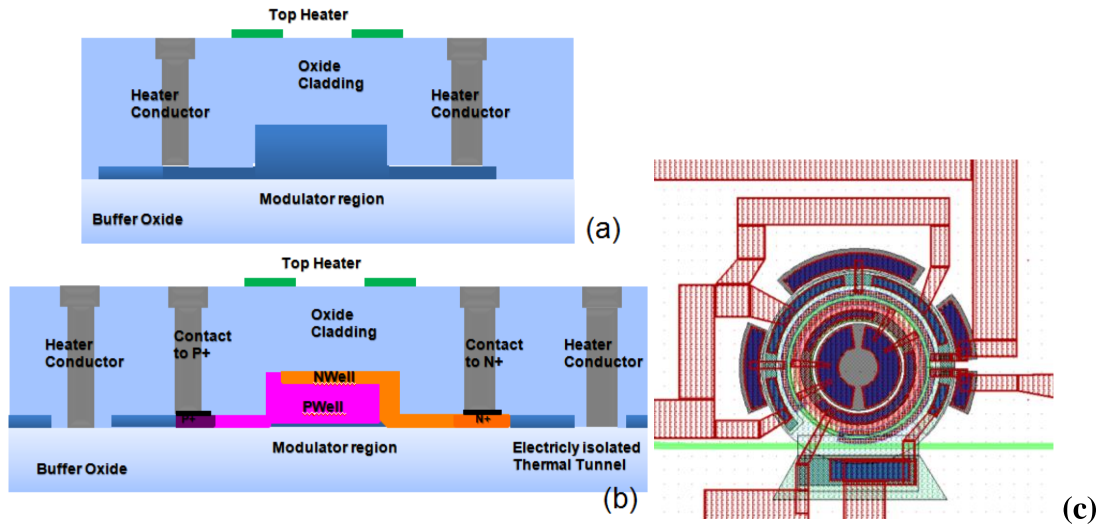


Fig. 4.17. Cross section view of Oven heater (a) without modulator (b) with isolation to modulator (c) Design CAD of PN depletion mode modulator with micro-oven design

5 Dynamic Control of Photonics

This chapter mainly introduces some dynamic control of photonic circuits. An optical storage experiment is firstly presented, then a broadband optical router based on adiabatic coupler is proved, and finally a single photon level adiabatic wavelength conversion is experimentally demonstrated.

5.1 Optical delay Storage

5.1.1 *Introduction*

Storing light on chips with delays is an important function in optical signal processing [121][122], optical network on chip and especially quantum computing [123][124]. It requires to break the structure bandwidth limit [125][126][127]. An all-optical analogue of electromagnetically induced transparency (EIT) is initially demonstrated on a silicon chip [128]. However, the amount of delay demonstrated was limited to be less than 100 picoseconds due to free carrier absorption loss during the storage. Then, a 4 ring or 3 ring design is demonstrated to split the input and output control of optical signals from the super-mode ring; therefore, the optical loss due to free carrier absorption is greatly reduced and the optical storage is greatly enhanced to be 300 picoseconds [129] .

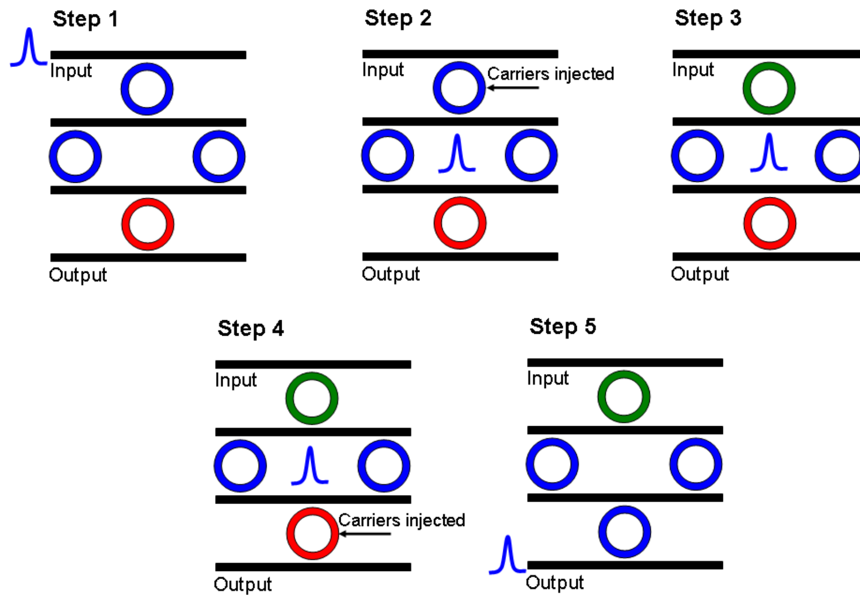


Fig. 5.1. Schematic the 4 ring system and its operation principle, (Step 1) shows the acceptance state of the system. Bits are stored as shown in (Steps 2 and 3) then released in (Steps 4 and 5).

The 4 ring system for tunable delay is shown in Fig. 4.1. It is consisted of 4 rings in 3 rows in total. The top row and bottom rows are used to storage and release an optical pulse in the system. And the two rings in the central row formed an equivalent EIT-storage cavity structure.

Initially, the storage cavity has the same resonant wavelength as the store control ring, so that optical signal with that wavelength will automatically couple into the storage EIT cavity. Then after the pulse is completely coupled in, free-carriers will be injected to the storage control ring to change its resonance wavelength (color of the top ring is changed from blue to green as in Fig. 5.1). At the same time, the resonance frequency of the release ring is different from the storage cavity. In this way, the optical signal can be stored in this

cavity. Finally, the release pulse will inject free-carriers into the release ring to make it match the resonance wavelength to the storage cavity. In this manner, the optical pulse can be released to the output. A three ring structure is similar to the four ring structure except that its release ring is chosen as one of the two rings in the storage cavity.

5.1.2 ***Simulation***

Here we mainly used the optical-mode-solution described in Chapter 2.3.3 for simulation of optical delays. And the following equations [130] are used to describe the time evolution of the field of the add/drop ring resonator.

$$\frac{da}{dt} = (j\omega_o - \frac{1}{\tau_{int}} - \frac{1}{\tau_{through}} - \frac{1}{\tau_{drop}})a + j\kappa_1 E_{In}^{through} + j\kappa_2 E_{In}^{drop} \tag{5.1}$$

$$E_{Out}^{through} = E_{In}^{through} - j\kappa_1^* a \tag{5.2}$$

$$E_{Out}^{drop} = E_{In}^{drop} - j\kappa_2^* a \tag{5.3}$$

Where ω_o is the resonance wavelength of the ring and $\kappa_{1,2}$ are the coupling coefficient from through/drop waveguides to the cavity. These equations can be applied to each cavity used in the system, and then they are coupled to each other to compose the whole system. Here we let k1=k2 for simplicity of design and calculation.

To model effects of free-carriers during the store/release steps, we use the following equations [90] :

$$a(l) = a_o e^{-j\Delta\beta l + 0.5\Delta\alpha l} \tag{5.4}$$

$$\Delta\beta = \frac{2\pi}{\lambda}\Delta n_{neff} = \frac{-2\pi}{\lambda}(8.8\times10^{-22}\Delta N + 8.5\times10^{-18}\Delta P^{0.8}) \tag{5.5}$$

$$\Delta\alpha = 8.5\times10^{-18}\Delta N + 6.0\times10^{-18}\Delta P \tag{5.6}$$

Where ΔN is the injected electron density, ΔP is the injected hole density, Δβ and Δα is respectively the propagation constant and the attenuation constant of a waveguide with length l and effective index n_{eff}.

One thing we need to take in consideration is that the carriers injected in the cavity will gradually recombine. Therefore, the previous calculated propagation constant and attenuation constant becomes various with time. The detailed Matlab code of optical delay simulation is shown in Appendix I.

5.1.3 *Optical Loss Study and Device Fabrication*

A fundamental problem that precludes the delay system to store optical pulse for a longer time is the optical transmission loss of the waveguide, especially the transmission loss of ring resonators. Therefore, an optical loss study is made to overcome this problem.

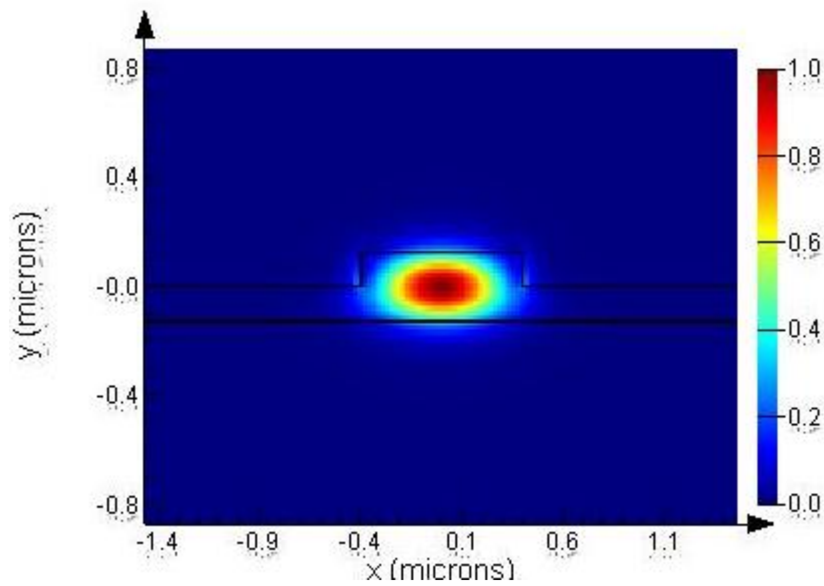


Fig. 5.2. Optical mode and structure of shallow etched silicon waveguide on SOI platform

A ridge waveguide based on SOI is shown in Fig. 5.2. The ridge waveguide is composed by partially etched silicon with ridge looking waveguide on top of the flat silicon surface. The optical mode is located inside the ridge region. The optical loss of waveguide is mainly attributable to scattering, absorption and radiation [131]. The radiation loss is only obvious when the waveguide is bending as a sharp curve. And absorption of 1550nm wavelength photon can be trivial in SOI platform. The main loss here has to be the surface scattering given that the top silicon crystal layer of SOI has limited defect. This surface scattering is mainly because the relative unsmooth surface after RIE etches during the fabrication process of the ridge waveguide. The unsmooth can be because of a mix of the nonuniform exposure during Ebeam writing and the unsmooth of plasma etching.

Therefore, to reduce the surface scattering loss, we can smooth the exposure during Ebeam writing. And in addition, we can reduce the etching depth of the waveguide, to reduce to the overlap of optical mode and unsmooth etching surface in order to reduce the surface scattering loss.

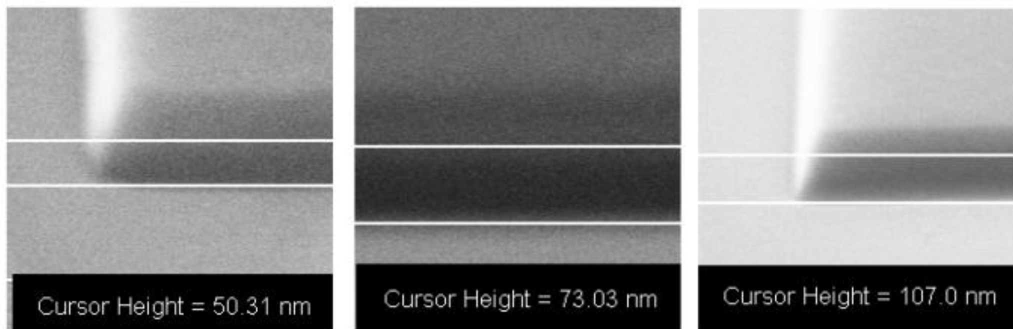


Fig. 5.3. SEM images of shallow etched rib SOI waveguides, with etch depths of: 50nm , 75nm, and 100nm. Photoresist remains on top of the waveguides in these images.

An experiment is then done to study the influence of etching depth to surface scattering loss. The substrate is Soitec's 6" SOI wafers with 3µm thick buried oxide and 250nm thick silicon layer on top. Then waveguides are patterned with JEOL 9300 Ebeam lithography system with X1541 resist. The waveguides are then etched using ICP RIT chlorine-based recipe(CL2/BCL3) to three different etching depths: 50nm, 75nm and 100nm as shown in Fig. 5.3. Waveguide widths are set to be 700nm, 800nm and 900nm to ensure near single mode in each case. And finally, 2 microns thick oxide is deposited by PECVD for protection of the device.

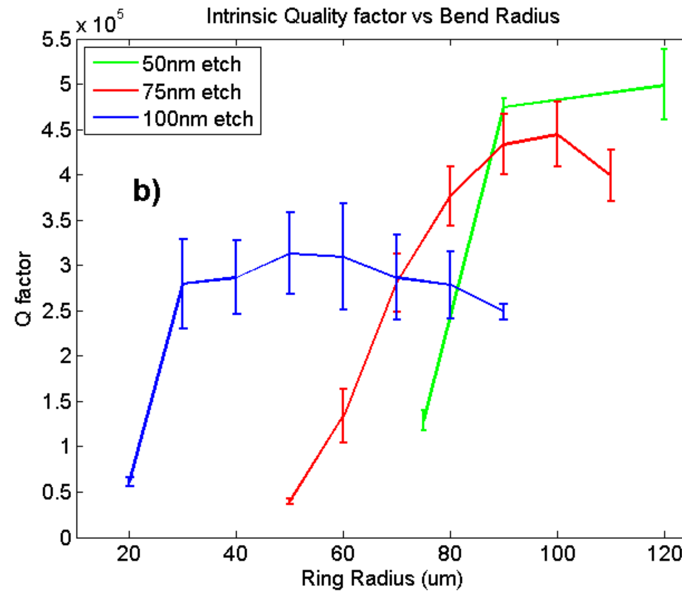


Fig. 5.4. Intrinsic quality factor vs. bend radius for 100nm, 75nm, and 50nm shallow etched SOI ring resonators.

The result of this experiment is close to the theory, that the shallower the etching is, the less loss the waveguide will suffer. However, it also comes with a tradeoff that the shallow etch has less bending radius tolerance as shown in Fig. 5.4 [132]. In the real device fabrication, we want the device to be as compact as possible. Therefore, we would also need the waveguide structure to have better performance at sharp bending. A waveguide with 100nm etching depth and 30microns bending radius is finally selected during the device fabrication.

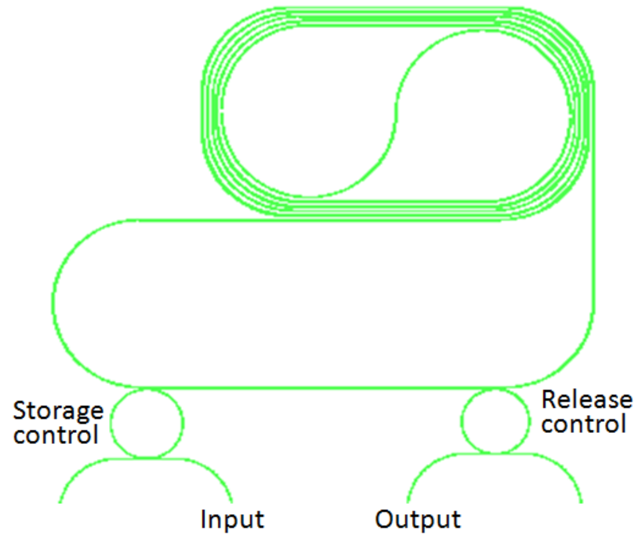


Fig. 5.5. Layout of optical delay

Then a new design of optical delay is shown as in Fig. 5.5. The storage unit here is changed to a big spiraled ring. In this design, optical pulse will experience less of coupling loss region during its stay in storage unit. We kept the storage control ring and release control ring for controlling of optical pulse signals. The storage unit is set to be a big ring.

5.1.4 ***Experiment Setup***

The experiment setup is shown as Fig. 5.6. A Ti: Sapphire laser generates 100fs pulses at a repetition rate of 80MHz with 830nm center wavelength. Then the pulse meets a 50:50 beam splitter. Half of the pulse is turned into 1550nm communication wavelength through Optical Parametric Oscillator (OPO). After this communication pulse is coupled into a fiber, it goes through an 0.25nm bandwidth tunable grating filter (JDS Uniphase TB3) and an

EDFA (Erbium Doped Fiber Amplifier), and another 0.5nm bandwidth tunable filter and a tunable delay system to narrow down its bandwidth from ~20nm to ~0.5nm and tune it at required wavelength and time. Finally it is coupled into the silicon photonic chip at TM (E-field perpendicular to the chip) mode and working as the signal pulse.

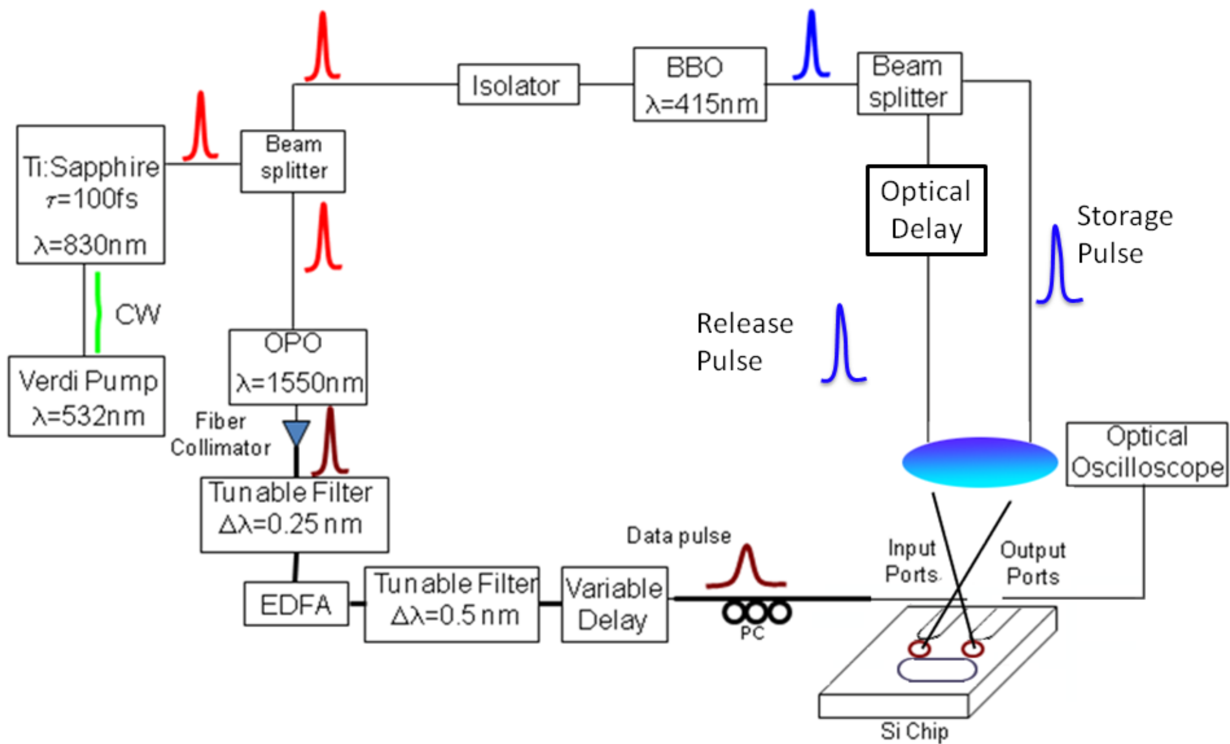


Fig. 5.6. Experimental setup used .The stored pulses are generated in an OPO crystal from 830nm Ti-Sapphire laser, while SHG is used to generate 415nm storage and release signals

The other half of the 830nm pulse will go through a BBO crystal to form a 415nm wavelength blue pulse to tune the resonance cavity of the silicon photonic device. This pulse is first split into a storage pulse and a release pulse by a beam splitter. And a motor driven linear stage is placed in the beam path of the release pulse to control the time of

delay as in Fig. 5.7. The beam path on the linear stage has to be kept perfectly straight to make sure that moving of the stage doesn't affect the focus spot location and coupled energy on the chip. Both delay and release pulses are focused on the ring resonator through a 10X long working distance microscope lens.

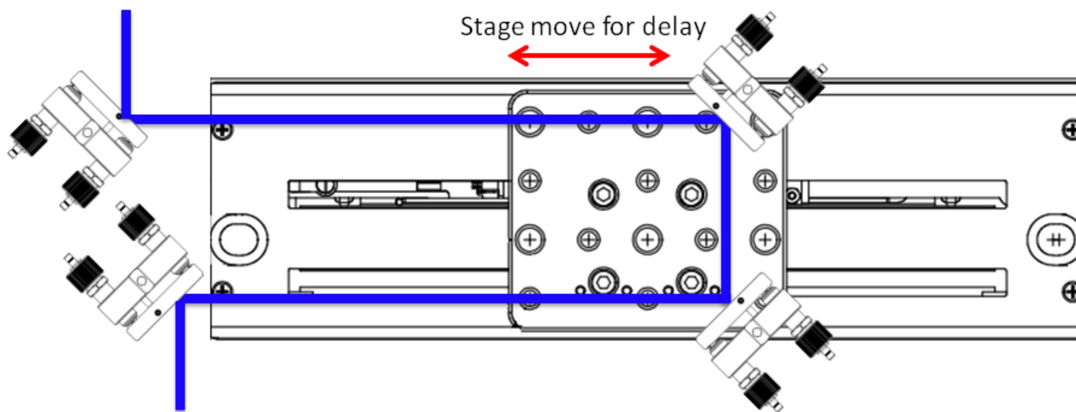


Fig. 5.7. Stage control for delay of delay pulse

During the experiment, the near 1550nm signal pulse is firstly aligned to the resonance frequency of storage control ring, this way the pulse can enter the storage unit. The storage control pulse need to pump the storage control ring immediately after this. This pulse injects sufficient amount of carriers to blue shift the resonance wavelength at least 0.6nm away to break the coupling between the big storage ring and the storage control ring. Meanwhile, the original release control ring resonance wavelength is away from the signal pulse wavelength to avoid the leakage of the signal pulse into the release ring. Then at required release time, the release pulse will pump the release ring to shift the resonance wavelength to match the

wavelength of signal pulse, this way, the storage pulse will leak out through the release ring to the output. The output signal will finally go through an additional EDFA and be tested by an optical oscilloscope.

In this experiment, the beam path of the storage pulse is fixed. The signal pulse will go through an electric driven fiber delay device before entering the chip for the purpose of synchronizing. And the release pulse goes through a linear stage for delay time control. The linear stage can vary within 100mm range, which means a controllable delay within about 300ps range.

5.1.5 ***Result and Discussion***

The result of all optical delay is demonstrated in Fig. 5.8. Where delay signal from 150ps to 450ps is demonstrated. This is the record of tunable on-chip optical delay demonstrated so far. We didn't demonstrate the signal before 150ps mainly limited by the 100mm range control stage.

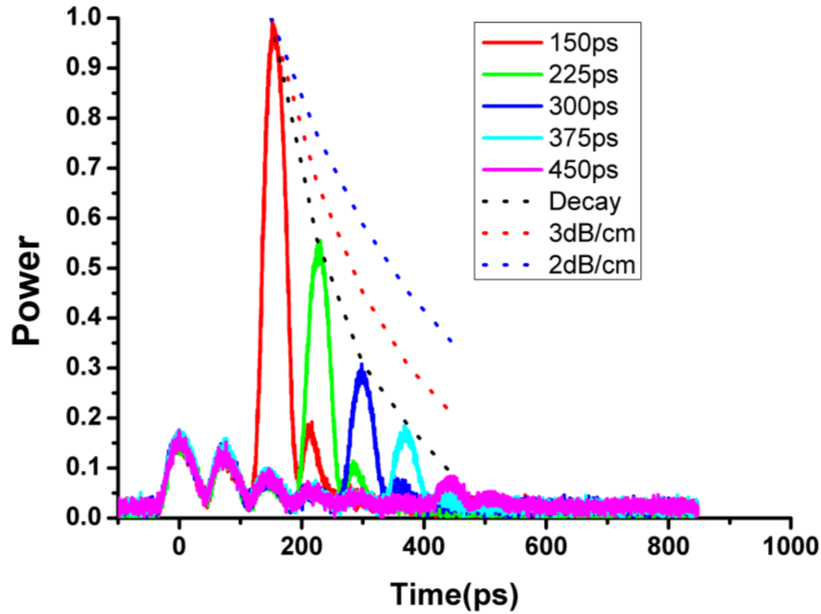


Fig. 5.8. Optical Delay Result at changing the time of release pulse

However, we still notice that the pulse signal is decaying faster than what we estimate. For example, the blue and red dot lines are the assumption behavior of 2dB/cm and 3dB/cm transmission loss, while our measured transmission loss of this device is actually about 1.5dB/cm to 2dB/cm. The result behaves worse than the estimated transmission loss. This is mainly because that the carrier life time is limited to be around 500ps in this case. The storage control ring cannot maintain large enough (0.6nm) blue shift from its resonance wavelength, and then the optical signal will gradually leak to the storage control ring and cause additional loss.

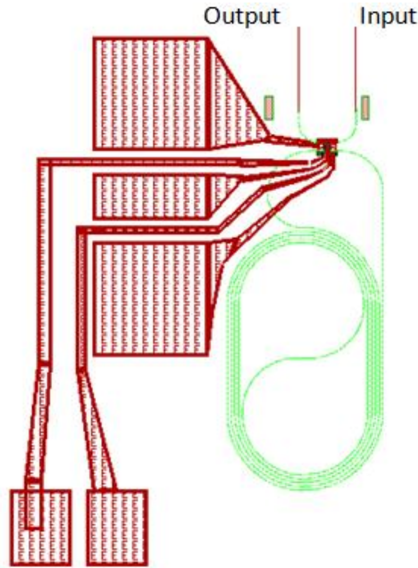


Fig. 5.9. Design of Electro-optical delay

Solution of this problem is an electro-optical delay device as seen in Fig. 5.9. In the all-optical solution, we can only inject carriers, and then have to wait for the carriers to recombine themselves. While in electro-optical systems, we can control the injection of carriers and depletion of carriers by simply change the bias voltage. Therefore the storage control and release control of the optical delay can use the same ring with PIN modulator.

The fabrication of the electro-optical delay device actually goes along with other projects in our group. The design and fabrication of these device can be seen as an smaller scale multi-project wafer (MPW) service. We developed our own way of silicon photonic MPW in our group by unify the design and process, so that we can yield multiple projects at the same time. A more detailed description of this design is included in Appendix II. And a double pattern method is also presented in the fabrication process in Appendix II which can

avoid the mask resolution limit and optical diffraction limit to silicon photonic fabrication, and at the same time reduce the cost of high resolution mask.

The working sequence of the electro-optic delay can be as following: the control ring resonance wavelength is originally same as the pulse signal wavelength. When the signal pulse enters the input port, it will enter the delay storage without loss as seen in Fig. 5.10(a). Once it enters the storage unit, the control bias will be turned ON; carriers are injected in the ring to shift the resonance wavelength. Then the stored signal pulse will keep staying in the through port without experiencing loss through the ring (Fig. 5.10(b)) and leak to the output. Once the electric bias is off, the resonance wavelength is the same as signal pulse, and then the optical pulse will leak to the output port without loss.

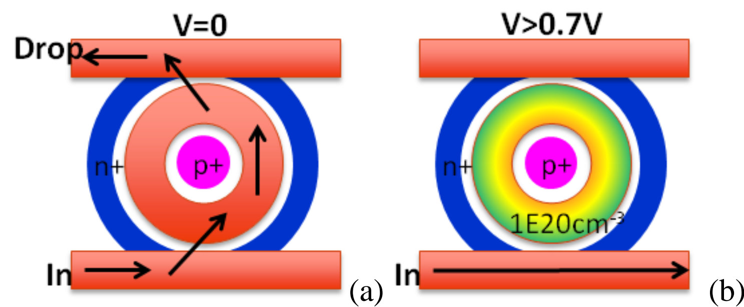


Fig. 5.10. (a)Optical switch without bias (b)Optical switch with bias

5.2 Broadband Optical Router

5.2.1 *Introduction*

Optical Network on Chip, as the replacement of current copper interconnect, must have the property of broadband, low power consumption and low latency [133].

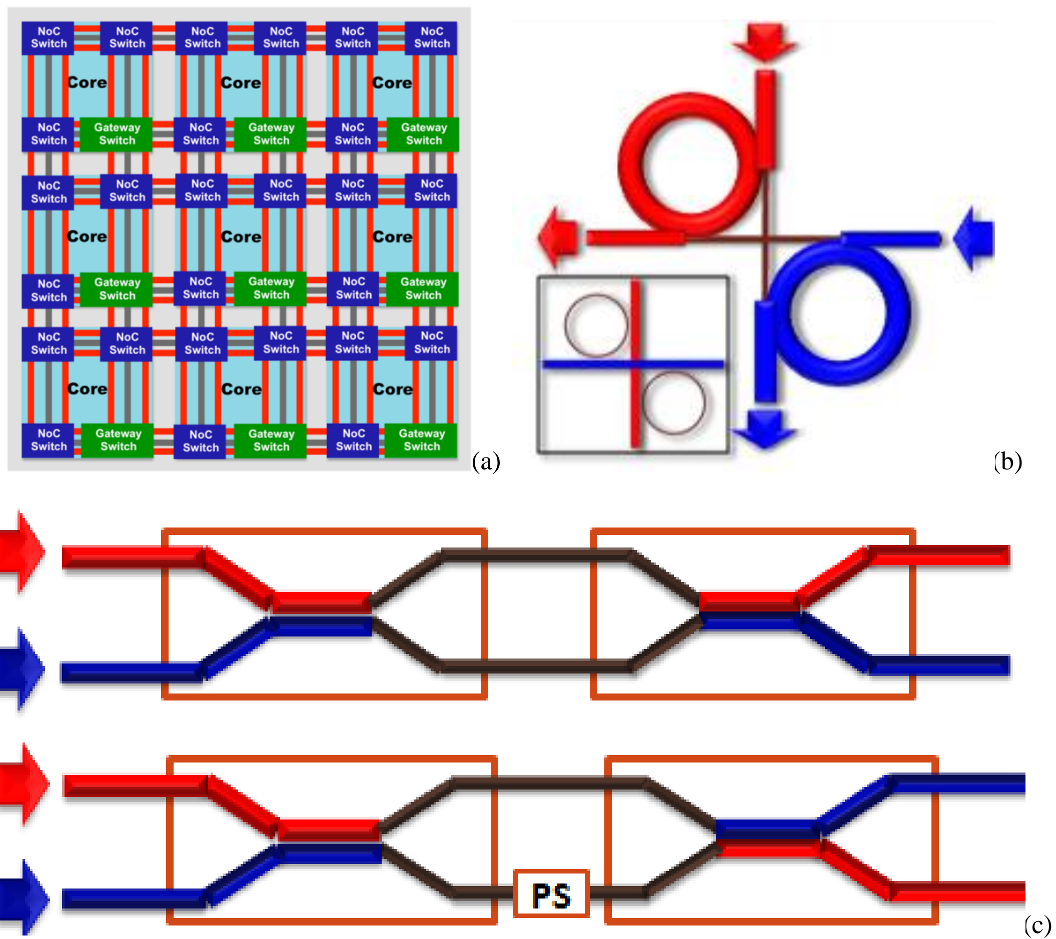


Fig. 5.11. (a) ONoC configuration (b) 2x2 Ring resonator router (c) 2x2 MZI routers

As shown in the Fig. 5.11(a), based on the Manhattan architecture of Network on Chip, the basic element of ONoC must have ability to communicate both in and out at all four

directions. Therefore, a 2x2 optical router is required as an fundamental element. The ring resonator with both drop port and though port have been proved to be efficient as a switch or router in changing the transport direction of optical signal [134]. However, the spectrum of ring resonator is sharp at certain wavelengths. Therefore, it can hardly maintain the broad bandwidth property that optical network should have; more specifically, it cannot be use in the WDM systems. A 2x2 Mach Zehnder interferometer (MZI) router design is a better choice which could route more signals with a fairly broadband performance. A key of 2x2 MZI is the 3dB coupler which can well perform in a broadband region.

The symmetric directional couplers as introduced in section 2.3.2 are used in the integrated optic circuits to couple light between waveguides. The power transfer length (L_c) is the main part that affects the coupling condition. However the directional couplers are too sensitive to wavelength and have very low fabrication tolerances. A small change in gap, width or height can vary the power transfer length greatly and therefore would affect the final coupling condition. The adiabatic coupler with an asymmetric structure is developed to overcome these drawbacks. There have been reports of adiabatic couplers on $LiNbO_3$ [135], and polymeric [136] waveguide materials. Results show that adiabatic coupler is not sensitive to the total coupling length, and they are performing robust to fairly broad

wavelength range. However, all the adiabatic couplers requires a long coupling length (usually millimeters), makes it hard to integrate in a chip.

Silicon photonic platform provides possibility of achieving large scale integration of photonic circuits [137] due to the high refractive index contrast between the silicon core and the silicon dioxide cladding. This section mainly focuses on simulation and fabrication results of 3-dB adiabatic couplers in silicon photonic platform, and its application in the broadband optical routers.

5.2.2 *Design and Simulation*

The adiabatic coupler looks really similar to the directional waveguide except for its asymmetric. A basic adiabatic coupler shown in Fig. 5.11 consists of three parts [138]. Region 1: two widely separated asymmetric waveguides converge closer with very narrow gap (~200 nm). Region 2: two asymmetric waveguides tapers to a same width while keeping a same gap between each other. Region3: the two symmetric waveguides diverge to wider separation (>1µm).

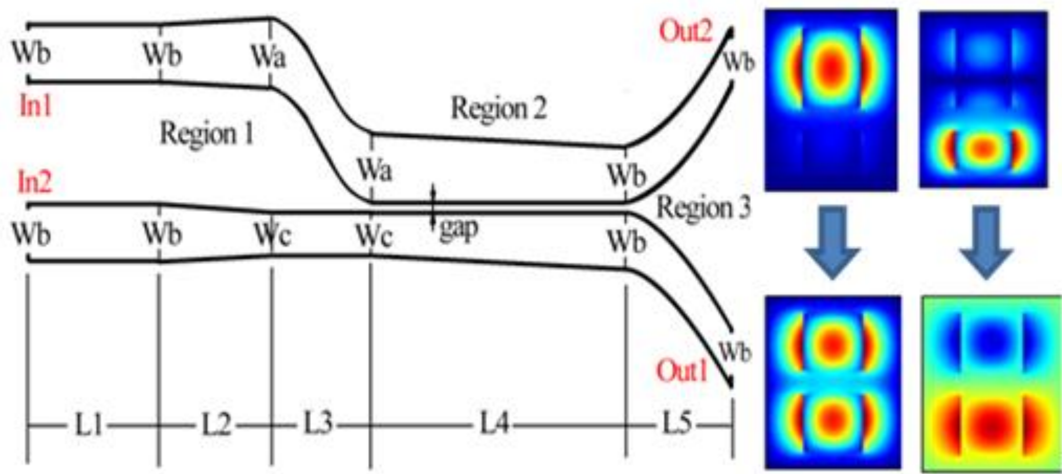


Fig. 5.12. A basic adiabatic coupler structure

A directional coupler will launch two modes (even and odd mode), and later will oscillate between the two modes. The coupled result is a combination of the two modes. As a contrast, in adiabatic couplers, you only launch one fundamental mode (either even or odd) with exciting the input waveguide with the fundamental mode, the power slowly transfers to the adjacent waveguide without exciting higher order modes. The two branches of a 3-dB coupler should have similar dimensions to enable equal transfer of power. A direct comparison of power transfer of a directional coupler and an adiabatic coupler with same coupling length in Rsoft BeamProp simulation is shown in Fig. 4.1.3.

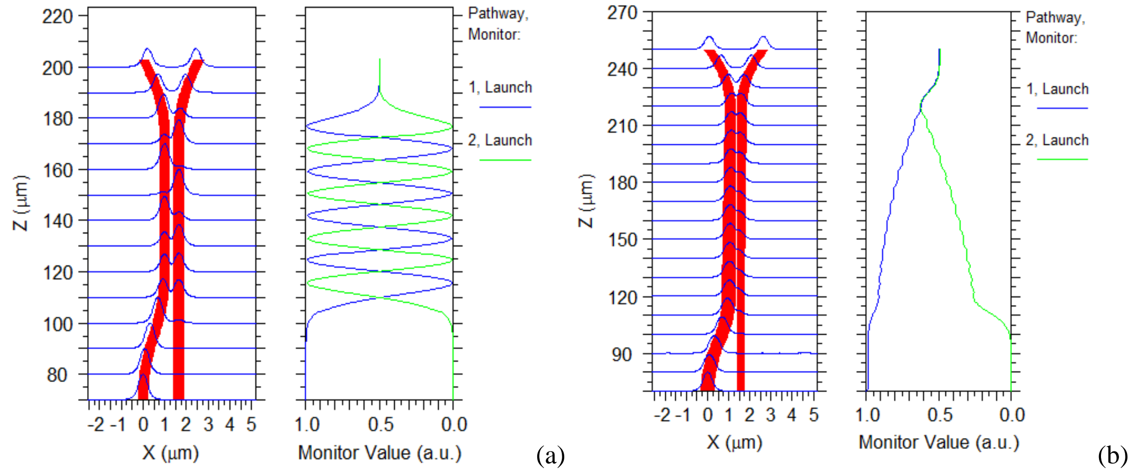


Fig. 5.13. Rsoft BeamProp Simulation of (a) directional coupler (b) adiabatic coupler

To optimize the coupling performance, a series of simulations based on Beam Propagation Method (BPM) are performed on the layout shown in Fig. 5.13. We set the waveguide height to be 250nm, and the standard waveguide and symmetric side of coupler width to be 450nm. And the core index is 3.5 and the cladding index is 1.5 just as then standard silicon photonic platform. The asymmetric sides of coupler have width of 300nm and 600nm respectively, and the total length of L4 is 200 micron. The simulation results are shown in Fig. 4.1.4.

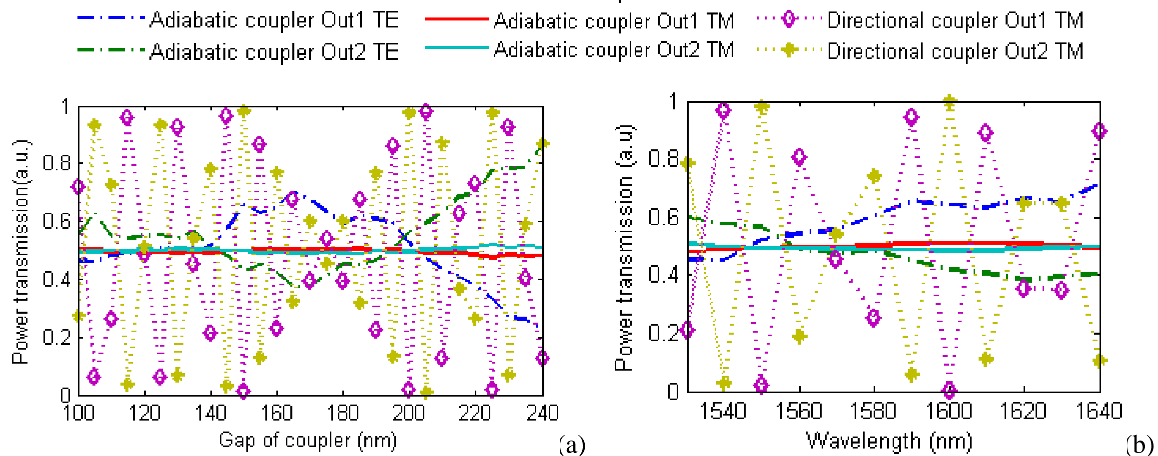


Fig. 5.14. (a) Simulation of coupler with different gap. (b) Performance under different wavelength.

In the first simulation [139], the gap between two asymmetric waveguides varies from 100nm to 240nm. The wider input port of the adiabatic coupler is excited with TE or TM mode light and result is compared to directional coupler with the same condition. From comparison in Fig. 5.14 (a), the adiabatic coupler is robust with different gaps. Therefore a reasonable guess of 10nm fabrication error would not affect the performance of adiabatic coupler. One difference of this short adiabatic coupler from the other published adiabatic couplers is that it's polarization dependable device. The coupler can work much better on TM mode than TE mode. The situation keeps the same in the second simulation as will be talked about later. A main reason is that the power transfer length in TE mode is longer than TM mode, therefore, for the same coupling length, it have more power transfer lengths on TM mode than TE mode. While adiabatic coupler normally requires large number (>20) of power transfer length, TE mode in this condition cannot meet the requirement under this condition here. TE mode performance can be enhanced by either shortened the coupling length (minimize the gap) or extend the coupling length. However, that is either pushing the fabrication limit or against the rule of shrinking footprint size.

In the second simulation, the gap of the coupler is fixed at 200 nm , performances of the coupler under different wavelengths are simulated and shown in Fig. 5.14(b). The

results are compared with directional coupler. And we have confirmed that, under TM mode, the adiabatic coupler have really stable performance on outputting equal power.

5.2.3 *Device Fabrication and Experiment Setup*

Then an asymmetric Mache-Zehnder Interferometer (MZI) is fabricated to test the performance of adiabatic coupler. The symmetric side of the adiabatic coupler goes with arms with different length, and finally would be combined by a Y splitter. Path difference of the arm is 135micron, and as the standard MZI structure mentioned in section 2.3.4, the output power will be either 0 (destructive interference) or 1 (constructive interference) based on different phase change caused by path difference under different wavelength.

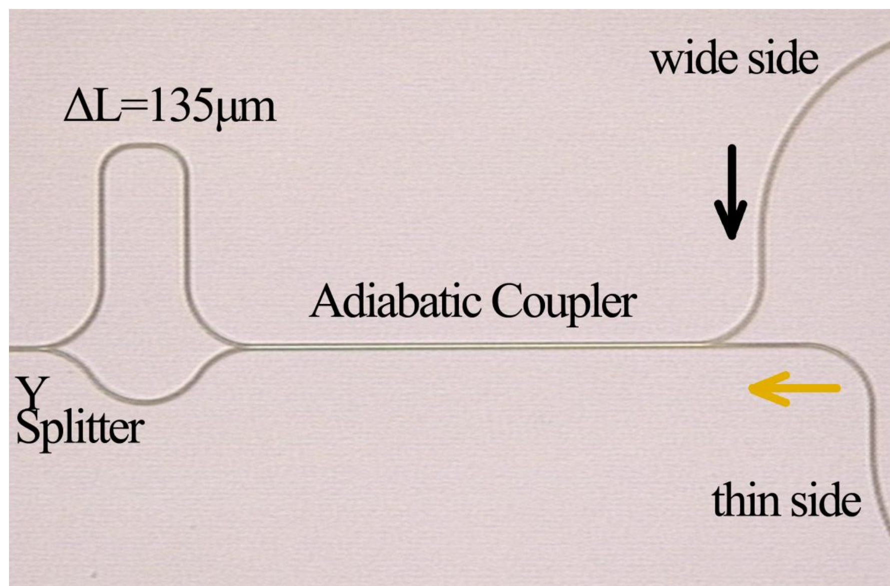


Fig. 5.15. MZI with adiabatic coupler

Difference between the constructive interference and destructive interference is the extinction ratio which is caused by equality of the input power offered by 3dB coupler. If the adiabatic coupler makes perfect 3dB coupling, then we are supposed to be able to achieve really high extinction ratio.

The testing devices are fabricated based on the standard silicon photonic SOI platform with a U shape. All the inverse taper couplers are positioned in one side of the chip and can be mechanically polished in one time. Both the input and output coupling of the chip to the fibers are achieved with one single lens. This lens can focus the free space parallel beams from the input collimator to the waveguide tip and can parallel the output light from output waveguide tip to a free space detector. A Labview program collects and plots the final spectrum of output. The experiment flow is described as Fig. 5.16.

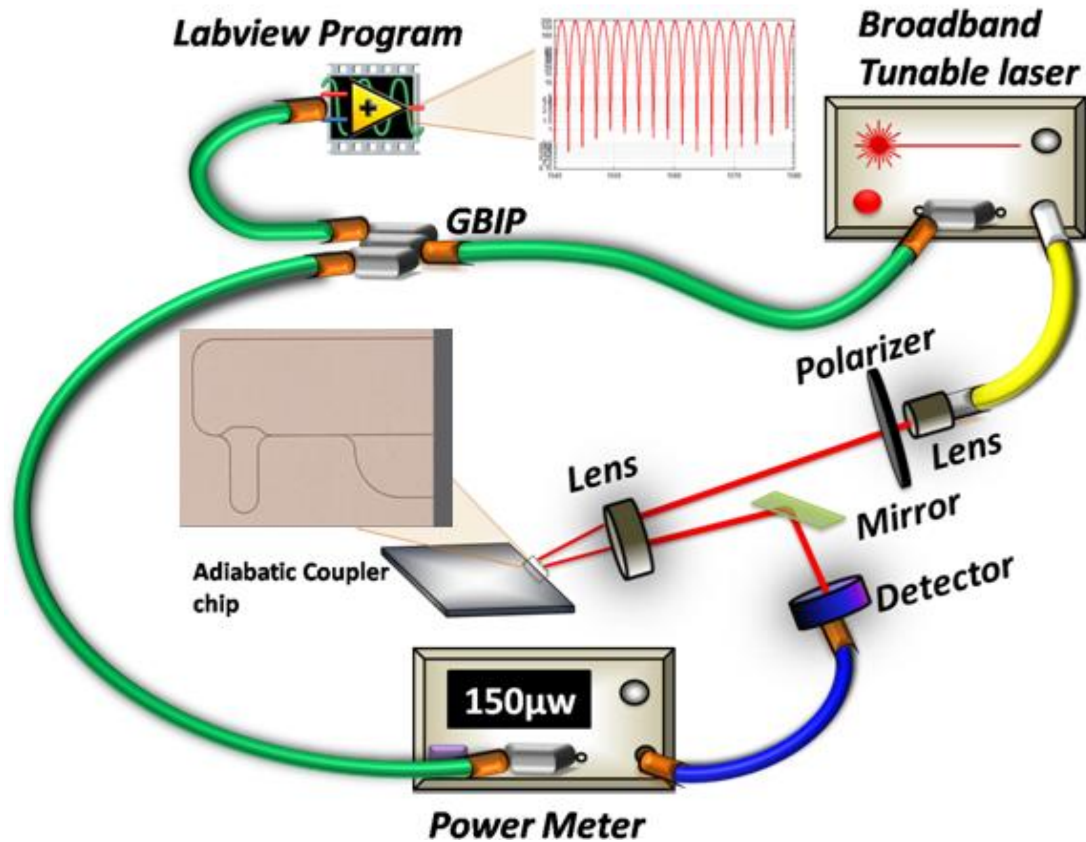


Fig. 5.16. Testing setup

5.2.4 *Results and Discussion*

During the experiment, both ports of the MZI are tested under quasi TM mode, and the transmission spectrum is compared with directional coupler and Y splitter as shown in Fig. 5.17. The MZI devices have very high extinction ratio (16-30dB) in wavelength range from 1520nm to 1620nm (limited by capability of laser). The Y splitter is supposed to be the best 3dB coupler in theory; the result shows no enhancement over adiabatic coupler. There could be several issues reasoning that. The main reason is the noise background makes it hard to

achieve really high extinction; scattering of input light on the input surface and reflection of light at polished interface of waveguide and air can also be collected by the detector.

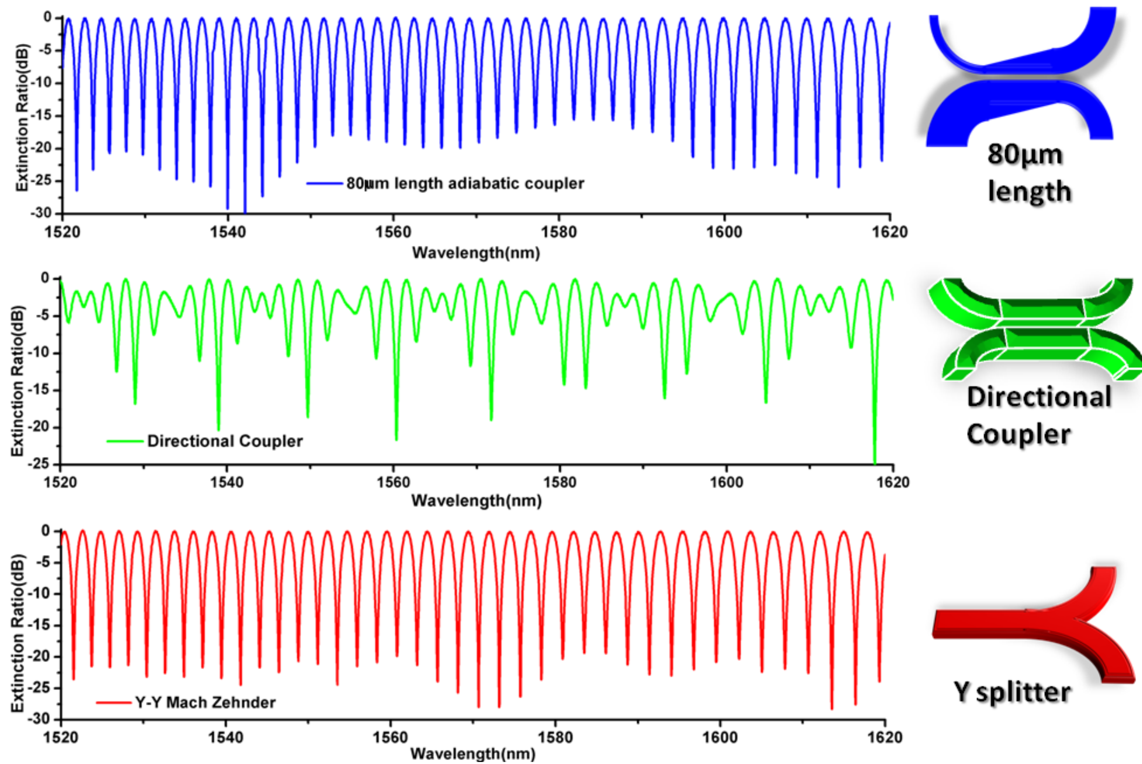


Fig. 5.17. Spectrum of 80 microns adiabatic coupler compared with spectrum of directional coupler and Y splitter

To prove the broadband ability of the adiabatic coupler, two lasers at different wavelength regions are used in the experiment, and results are combined together as shown in Fig. 5.18. The results show a quite stable performance from 1320nm to 1620nm, and both thin side input and wide side input gave robust performance. It proves that the adiabatic coupler can be a good element for the 2x2 broadband routers.

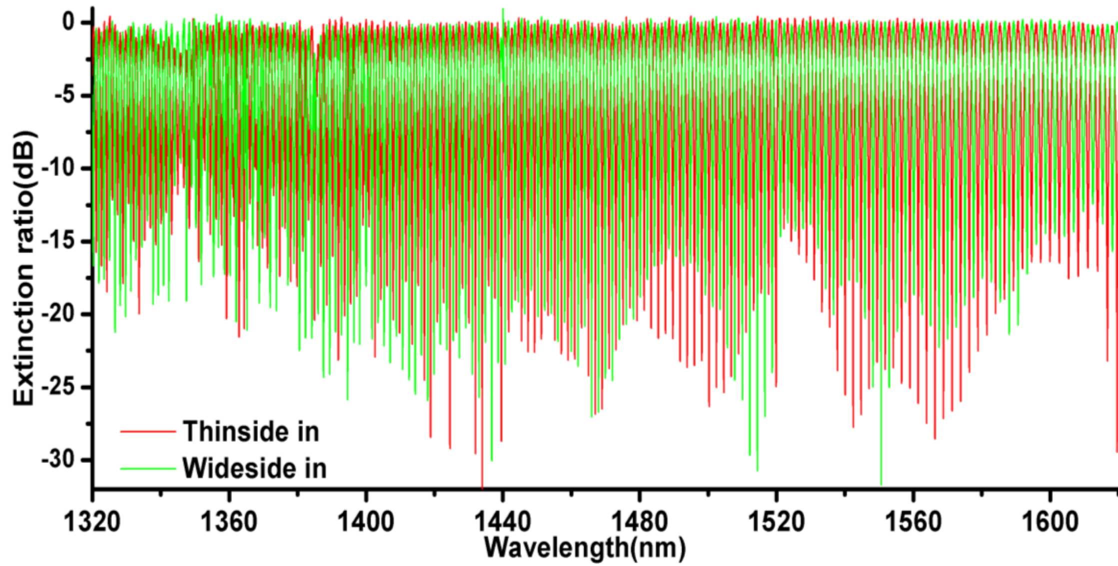


Fig. 5.18. Spectrum of adiabatic coupler

Then a 1x2 router testing is performed on the same chip simply by flipping the input and output. As Y splitter is a perfect 3dB splitter, the direct output from the Y splitter is a good even mode. Then after phase change with two arms, the mode will be converted to either even mode or odd mode which is actually outputting to either wide side or thin side of the adiabatic coupler.

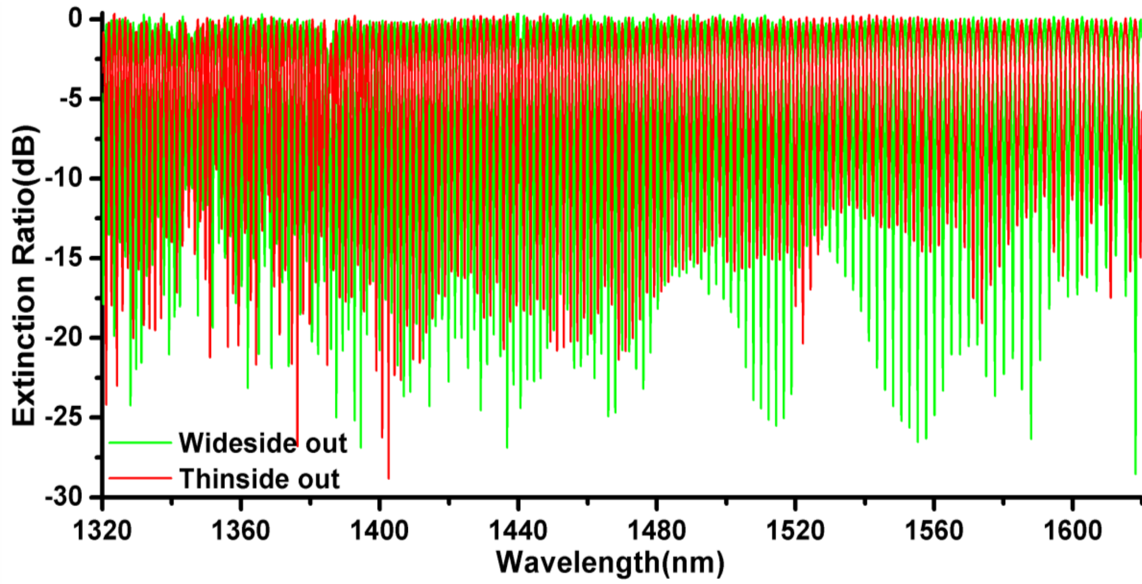


Fig. 4.1.9 Spectrum of 1x2 routers

The result in Fig.4.1.9 shows that a broad band 1x2 optical router is achieved. Thus, to make a 2x2 broadband optical router, we just need to replace the Y splitter with another adiabatic coupler.

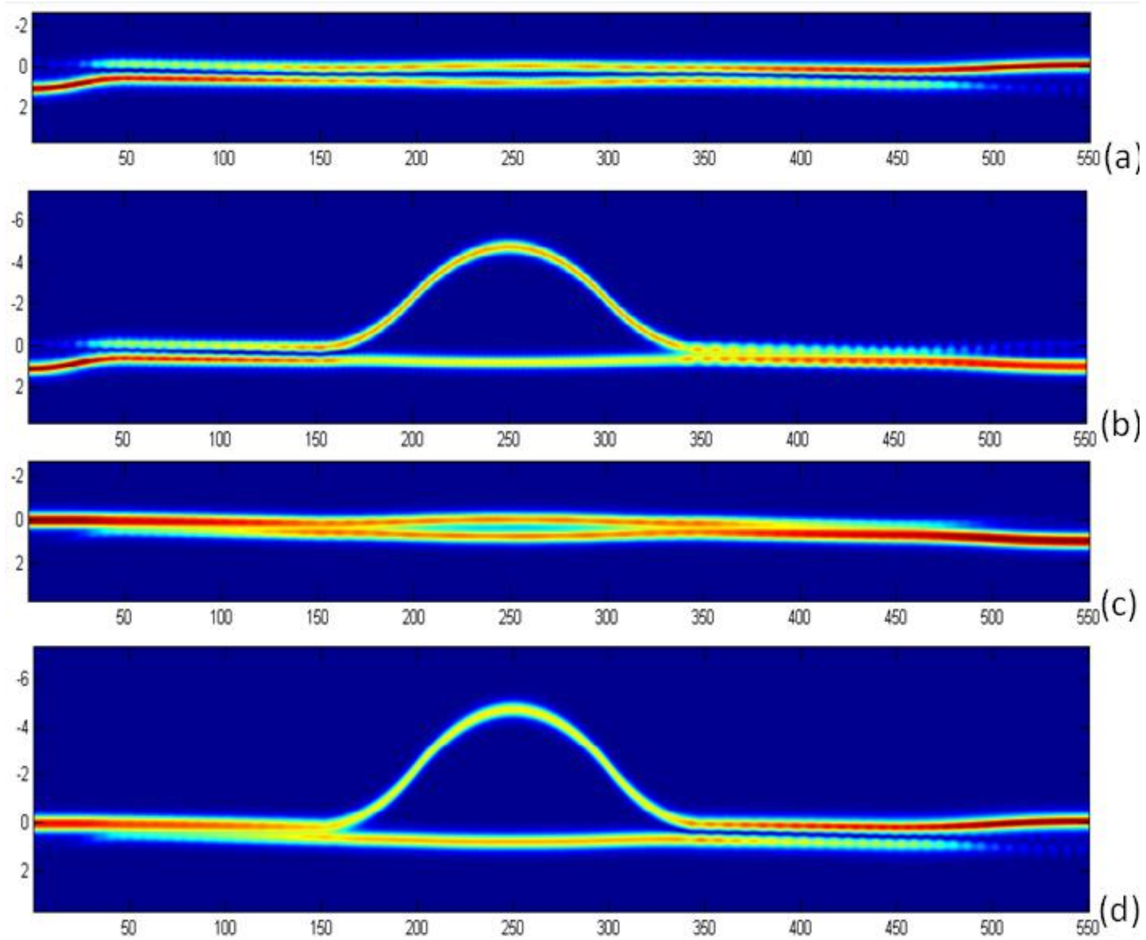


Fig. 5.19. (a)Thin side without phase shift (b) Thin side with Phase shift (c) Wide side without phase shift (d) wide side with phase shift

Fig. 5.19. demonstrates simulations of a 2x2 optical router that can switch directions of input source from two inputs. And then based on this work, a future 4x4 hitless optical router [140] can be made with the 2x2 MZIs as shown in Fig.4.1.11.

		Input			
		N	S	E	W
output	N		M6,M3	M5,M3	M2
	S	M1,M4		M5	M2,M4
	E	M1,M4	M6		M2,M4
	W	M1	M6,M3	M5,M3	

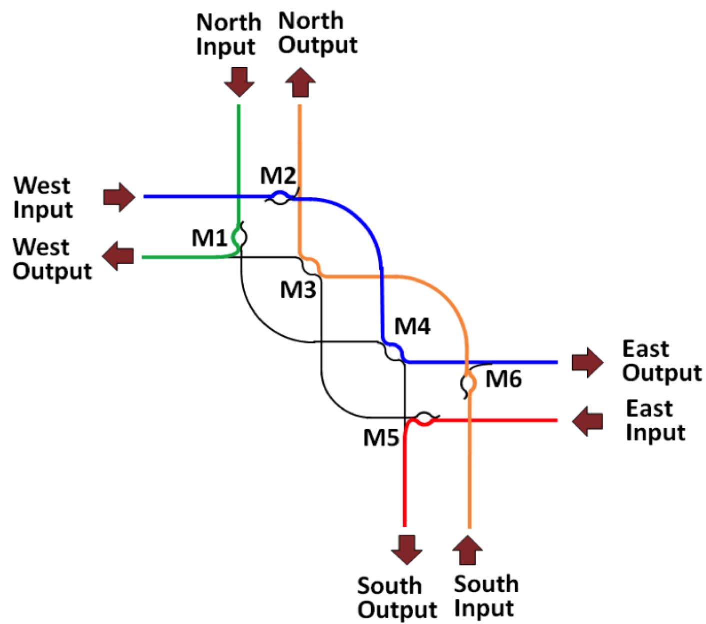


Fig. 5.20. 4x4 Hitless router with 2x2MZI routers

5.3 Single Photon Adiabatic Wavelength Conversion

5.3.1 *Introduction*

Ability of wavelength shifting is going to be an essential technology in future quantum optical communication and computing systems. It can be used to control frequency-bin entanglement [141], and can be used to control channels in wavelength division multiplexed

quantum key distribution networks [142], it can also enable tuning of photon's frequency to match optical cavity resonance [143]. Single photon wavelength conversion has been demonstrated through nonlinear frequency mixing in long crystals or optical fibers [144][145]. However, these approaches require high power pump lasers, and it would be a challenge to filter away from the weak signal, noise is also issue for nonlinear method due to competing nonlinear processes. Therefore, a new approach that is efficient and low noise is necessary.

Here we proposed and demonstrate a single photon adiabatic wavelength conversion based on optical micro cavities. It has been shown theoretically [146] and demonstrated experimentally [147] that during the period when light is trapped in a resonant cavity, if the cavities Eigen state is tuned, the light will undergo an adiabatic shift to the new state. The cavities state tuning can be achieved by either optically [147] electrically [148] or even mechanically [149] . And the efficient of this conversion can reach 100%, even down to the single photon level [150] .

5.3.2 *Adiabatic Wavelength Conversion Experiment Setup*

The experimental setup for adiabatic wavelength conversion is shown in Fig. 5.21. The pump pulse that causes the resonance shift of cavity is generated by a 100fs Ti: Sapphire

laser and converted through nonlinear crystals. The pump pulse (415nm) is focused on the 10 microns silicon ring though a microscope objective, absorption of the pump photons will generate free carriers and will change the refractive index and shift the cavity resonance with free carrier plasma dispersion effect. This shift can cause the adiabatic wavelength conversion of the probe pulse. The probe pulse also comes from the Ti: Sapphire laser; and an Optical Parametric Oscillator (OPO) is used to convert the probe pulse into ~1523nm. To synchronize the probe pulse and pump pulse, the probe pulse is tuned by optical path tuning. It is also filtered (0.14nm bandwidth) to match original resonant frequency of the ring resonator and then attenuated to single photon power level. The average photon number coupled into the ring resonator is about n=0.15, this minimizes the probability for multi-photon excitations and is a good approximation of a true single photon source. The photons coupled across the ring resonator into the drop port are measured by Superconducting Nanowire Single Photon Detector (SSPD from Scontel, Inc.) with a detection efficiency of around 5.6% after a second tunable filter (0.14nm bandwidth). The single photon results are directly compared with a bright coherent source by reducing the applied attenuation and tested by an Optical Spectrum Analyzer (OSA) with 0.05nm bandwidth for spectrum measurement.

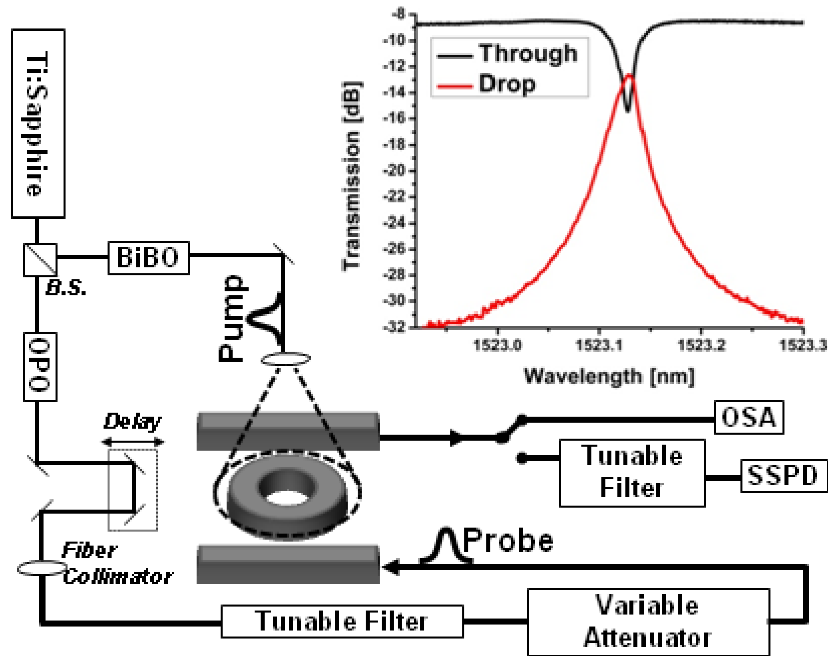


Fig. 5.21. Schematic of experimental setup[150]

5.3.3 *Experiment Result*

Adiabatic wavelength conversion is observed as shown in Fig. 5.22, where light converted to a new wavelength -0.3nm away from original wavelength by tuning the refractive index of the ring resonator. To prove that the new wavelength is generated by wavelength conversion we tuned the wavelength of the input light to be the expected new wavelength of the resonator after tuning. It is observed as right half of Fig. 5.22 that no signal is detected until resonator is tuned to new wavelength (when time=0). Therefore the new wavelengths we have observed before cavity shifting have to be generated by wavelength conversion. Furthermore, we notice that at time -10<t<0ps, there is no light left

at original wavelength, this offers further prove that wavelength conversion has reached 100%.

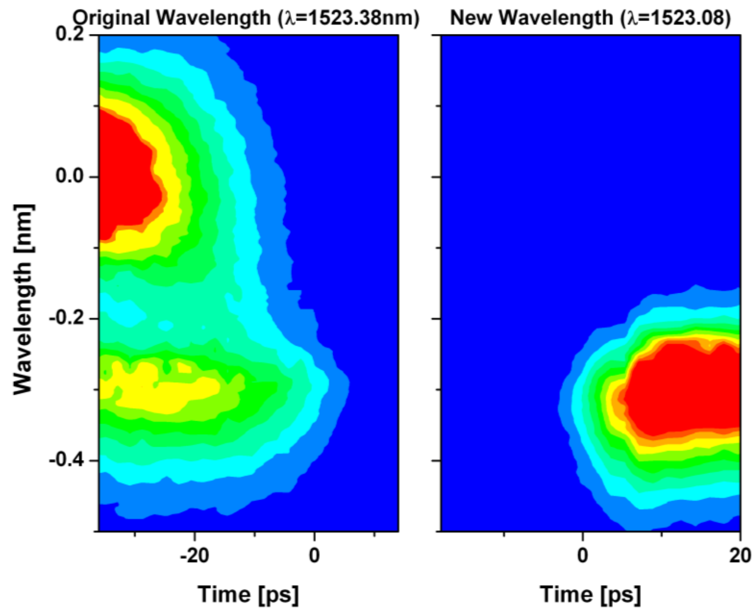


Fig. 5.22. Measured spectra as the relative delay between the pump and probe pulse. The left panel is when the probe is at the original wavelength of the cavity. The right panel is when the probe is at the new wavelength of the cavity.

Direct comparison of adiabatic wavelength conversion at single photon level and at classical level is shown in Fig. 5.23. Wavelength conversion for five different wavelength conversions for different pump power is demonstrated. It is obvious that in all cases the single photon results well match the classical results. The spectrum curves are not exactly identical due to different filters used to obtain the spectral data in the two regimes (0.05nm bandwidth for the classical light using an OSA, and 0.14nm bandwidth using a telecom tunable filter). Need to point out that especially in Fig. 5.23(a) that after conversion there is

almost no signal at the original wavelength. In the other cases the two signals are comparable because the new wavelength is strongly attenuated by free-carrier absorption. Another notice is that light measured at the original wavelength could because that a small amount of it leaves the cavity before the conversion process occurs. An ultrafast detector might help to get more accurate result.

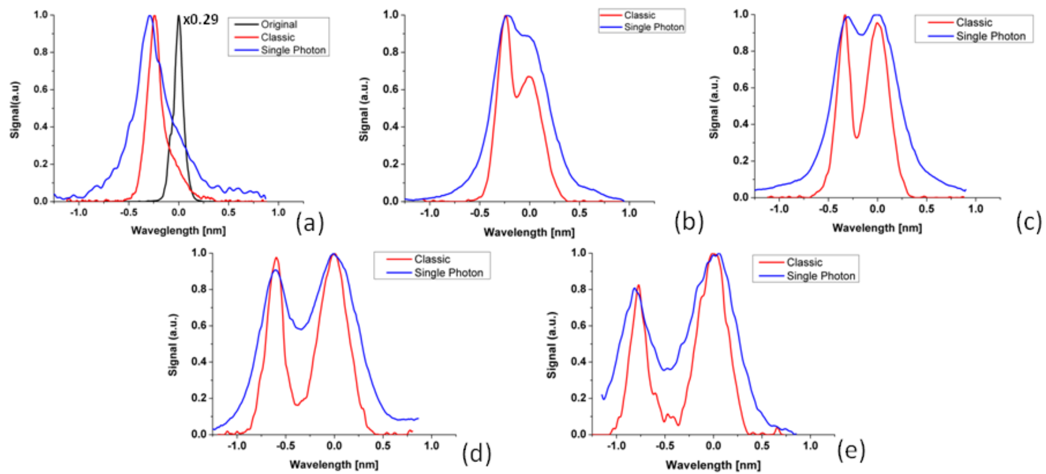


Fig. 5.23. Observed adiabatic wavelength conversion at single photon level compared with classical light at different converted wavelengths (a) 0.21nm (b) 0.29nm (c) 0.37nm (d) 0.59nm (e) 0.78nm

The overall conversion we have observed is ~40%, this is mainly limited by free-carrier absorption. To further study about the efficiency, we have modeled the Free Carrier absorption as shown in Fig. 5.24(a). This model is based on the reduction of cavity quality factor due to increasing of free carriers. This models shows that due to the existing of free carrier absorption, the wavelength conversion is limited to be 1nm where ~70% of photons are lost.

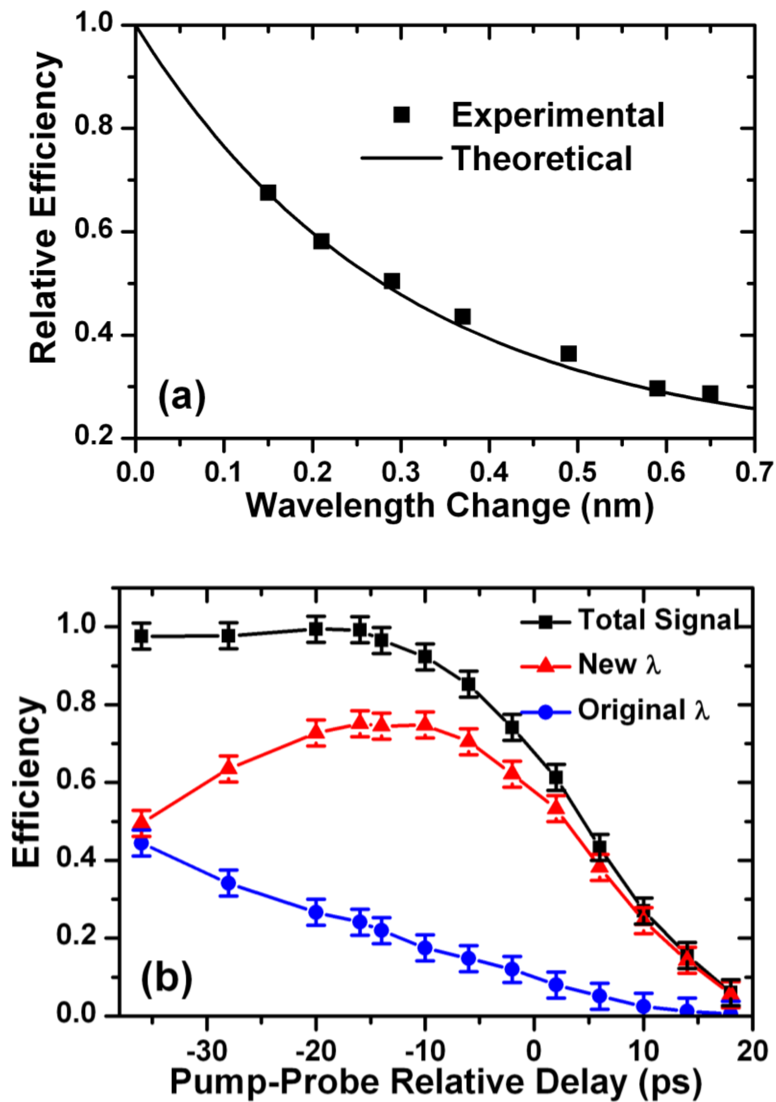


Fig. 5.24. (a) Relative reduction in conversion efficiencys due to free-carrier absorption vs. wavelength change. (b) Wavelength conversion efficiency as a function of time offset between the pump and the probe

We also measured the conversion efficiency as a function of the relative delay between the pump and probe pulse, as shown in Fig. 5.24(b). Here the efficiency is calculated by integrate signal at original wavelength and new wavelength as the relative delay between the pump and probe pulses is varied. The integrated signals are normalized to the original signal obtained at the drop port without wavelength conversion. In addition, effect of free-

carrier absorption is removed by using the model in Fig. 5.24 (a). This allowed us to obtain a statistical measure of the actual conversion efficiency. We notice that the earlier the probe pulse comes than pump pulse (negative pump-probe delay), the signal at original wavelength increases. And the signal will reach its peak at ($t<80ps$) because the light will leave the cavity before conversion process occurs at $t=0$. And since the pump pulse is as short as 100fs, the conversion process can be considered as instant response. When pump-probe delay is near $t=-10ps$, we notice that conversion efficiency reach its peak value (80%). This is the optimal point where the cavity contains the maximum amount of light from the incidence probe pulse during the happening of conversion. We have learnt from Fig. 5.22 that ring can never contain full power of the pulse energy at the same time. In practice the exact time when the maximum pulse power will be wavelength converted is a function of the photon lifetime of the resonator and the duration of the input pulse. Here we used a probe pulse with a bandwidth of 0.14nm, which corresponds to pulse duration of approximately 20ps. This is seen in Fig. 5.24(b) where the total signal reduces from its maximum value to zero in a time approximately equal to the probe pulse duration. As a result by using later delays it is possible to ensure that a minimal signal at the original wavelength exists, but this comes with a tradeoff in that the light from the probe pulse is not coupled into the resonator before the resonator is shifted to the new wavelength. These

inherent tradeoffs dictate the maximum conversion efficiency to approximately 80% in Fig. 5.24.

5.3.4 ***Summary***

As conclusion, adiabatic wavelength conversion at the single-photon power-level is experimentally demonstrated here. The process is very efficient and suffers very low noise. Any wavelength can be converted by simply tuning the refractive index of the resonator and the only limitation is the additional loss due to free-carrier absorption. This loss can be minimized by using a lower quality factor cavity.

6 Conclusion

In this dissertation, several different types of novel designs or materials are investigated and explored analytically, numerically and experimentally for the application of silicon photonic interconnects. Both novel designs and the material studies are done to build up silicon photonic elements for higher efficiency in speed, bandwidth and energy consumption.

6.1 Photonic Library Building

Chapter 3 mainly describes the work done to build up a 300mm reference flow photonic library. With the capability of a more uniform thick dielectric 300mm SOI wafer, we tried for the first time in the world to fabricate silicon photonic devices on 300mm wafers to shorten the distance between photonic research and the state-of-the-art massive electronic fabrication. We built up basic components of photonic interconnect circuit including different kinds of passive waveguides, interleaved modulators, reverse biased depletion mode modulators and forward biased PIN modulators. We combined germanium with silicon and built up low dark current germanium detectors and germanium Lasers on SOI. To solve the coupling loss problem in large scale fabrication, Section 3.1 optimized the grating coupler and its fabrication process. Furthermore, these grating couplers are used in the chip-to-chip optical coupling and have

demonstrated high coupling efficiency in simulation. Finally, these elements are combined to build up full WDM systems on a chip.

6.2 Modulator Device Enhancement

Chapter 4 studies the possibility of enhancing modulator efficiency by using novel material systems.

Section 4.1 focuses on enhancing the $\chi(3)$ nonlinear effect of silicon nanocrystals by quantum confinement. An experiment based on attenuated total reflection was done and for the first time observed the DC Kerr modulation of silicon nanocrystals. We can use this effect to make high speed electro-optical modulator devices in the silicon photonic platform.

Silicon photonic has the advantage of high confinement, while $LiNbO_3$ material has the advantage of large $\chi(2)$ nonlinear effect. Section 4.2 finds a creative way to deposit a-Si:H material over x-cut $LiNbO_3$ material, and uses the a-Si:H to confine optical signals. With specially designed optical waveguides, there is the possibility that the optical mode can partially cover the $LiNbO_3$ substrate. Therefore, the refractive index tuning of $LiNbO_3$ will cause phase changes of the waveguide. Section 4.2.4 demonstrates experimental results of both DC and RF. This method can greatly reduce the fabrication cost and yield of traditional $LiNbO_3$ modulator devices.

The electro-optical modulator in silicon photonic, based on free carrier injection free plasma dispersion cannot avoid the thermal generation issue while running due to the current flow through the device. Section 4.3 creatively uses the electric VIA structure, commonly used in the silicon photonic platform, to create a micro-oven shape and has successfully enhanced the thermal control efficiency by 100%. This invention can reduce the power consumption of silicon photonic platform in terms of thermal control in the future.

6.3 Dynamic Control of Photonics

Section 5.1 reduces the transmission loss of the optical waveguide by reducing the rough scattering surface with the shallow etch method. A newly designed optical delay device based on the low loss waveguide is then demonstrated, and has achieved 450ps optical delay.

Broad bandwidth is always a key advantage of photonics compared to copper interconnects. However, the existing optical router based on ring resonator performs with very narrow bandwidth. Section 5.2 solves this problem by smartly introducing a broadband adiabatic coupler design into silicon photonic platform, and brings useful solution for future broadband interconnects.

With the enhancement of optical transmission efficiency, section 5.3 demonstrates adiabatic wavelength conversion at single photon level through an experiment. This is one of the essential techniques required for future quantum optical communication and computing systems.

6.4 Future Work

The work presented in this dissertation focuses on enhancing the efficiency of silicon photonic devices in terms of speed, power consumption and bandwidth, and make it possible to be implemented in cluster, supercomputing and future processing systems. There is certainly much more to do to enhance the performance of demonstrated devices like optimization of the fabrication process, selection of right material, enhancement of the coupling efficiency, reduction of the transmission loss, and phase matching of the optical signal and RF signals.

Besides enhancing performance of single devices, we also need to consider practical applications as following:

1. The micro-oven design needs to be implemented in the CMOS compatible electro-optical device experimentally. A full thermal feedback system can be developed based on this device for low power consumption real time adaptive thermal control. It can also be directly used on thermal optical tuning systems, like the optical filter optical router and directional coupler, to enhance their performance.

2. Some dynamic photon control systems, like adiabatic wavelength conversion, optical delay and other quantum computing experiments, could be demonstrated with our optimized electro-optical modulation systems.

3. The novel hybrid silicon-$LiNbO_3$ platform has the advantage of a large electro-optical effect and compact size; therefore, it can be used to make low price modulator device or optical transceivers in the market of data communication and telecommunications. Some other novel devices or structures can be designed over this platform like the active broadband router and the modulation of grating cavity. The price of the hybrid $LiNbO_3$ platform can be further reduced by using the $LiNbO_3$ over insulator (LNOI) over silicon substrate.

4. One of the key aspects that should be investigated in the future is the complete integration of these components into actual interconnect, optical signal processing, or optoelectronic systems.

Appendices

Appendix I

1-Basic Ring Resonator Matlab Code

```
% Through-to-Drop RingResonator
function [QQ,Ex,FFSR]=ringring(couple,loss)
% ********************************
% Basic Ring setup
% ********************************
c = 299792458;      % Speed of light (m/s)
R = 2e-6;         % Ring Radius (m)
%ng = 4.1017;          % Ring group index
ng = 4.1;
L = 2*pi*R;
FSR = c/(ng*L) ;       % Ring Free Spectral Range (Hz)
T = 1/FSR    ;      % Ring round trip time (s)
WGloss = loss;     % Ring loss (db/cm)
RingWGloss = WGloss*L*1e2;
ringrtp = 10^(-RingWGloss/10)   ;   % normalized power after one round trip
ringrta = sqrt(ringrtp) ;      % normalized amplitude after one round trip
powercoupling = couple;  % Power coupled into and out of the ring
cs1 = sqrt(1-powercoupling);
ss1 = -1j*sqrt(powercoupling);
cs2 = 1;
ss2 = 0;
% ********************************
% Ring Frequency Response
% ********************************
lambda = 1550:0.0001:1570;
fspec = c./(lambda.*1e-9);

zm1 = exp(-1j.*(2.*pi.*fspec.*T + 0));

ringthrough = (cs1 - cs2.*ringrta.*zm1)./(1 - cs1.*cs2.*ringrta.*zm1);
ringdrop = (ss1.*ss2.*sqrt(ringrta.*zm1))./(1 - cs1.*cs2.*ringrta.*zm1);
powerthrough=10*log10(abs(ringthrough).^2);

% Operational Wavelength search
[m,minidx] = min(powerthrough);
lambda0 = lambda(minidx)*1e-9;
FSRwl = lambda0^2/(2*pi*R*ng);
Qtotal = (2*pi*lambda0)/(FSRwl*(2*powercoupling+(1-ringrtp)));
Qintrinsic = (2*pi*lambda0)/(FSRwl*(1-ringrtp));
QQ=Qtotal;
FFSR=FSRwl;
Ex=m;
```

2-ATR Simulation Matlab Code

```
%ATR setup simulation
clear;
lambda=1525e-9;
theta1=linspace(45*pi/180,55*pi/180,1000); %incident angle
%theta1=0*pi/180;
R_s=zeros(size(theta1));
R_p=zeros(size(theta1));
T_s=zeros(size(theta1));
T_p=zeros(size(theta1));
for z=1:length(theta1)

%Incident medium GGG
n0=1.93508;
k0=0;
y0=n0-i*k0; %characteristic admittance medium 1
eta0_s=y0*cos(theta1(z)); %optical admittance, s/TE pol.
eta0_p=y0/cos(theta1(z)); %optical admittance, p/TM pol.

%Medium 0
n00=1.66;
k00=0.0;
y00=n00-i*k00; %characteristic admittance in medium
d00=100e-9;
%**BELOW CRITICAL ANGLE**
delta00=(2*pi*d00/lambda)*sqrt(n00^2-k00^2-n0^2*(sin(theta1(z)))^2-2*i*n00*k00);
eta00_s=sqrt(n00^2-k00^2-n0^2*(sin(theta1(z)))^2-2*i*n00*k00); %absorbing optical admittance, s/TE pol.
eta00_p=y00^2/eta00_s; %absorbing optical admittance, p/TM pol.
%**ABOVE CRITICAL ANGLE**
BC00_s=[[cos(delta00), i*sin(delta00)/eta00_s];[eta00_s*i*sin(delta00), cos(delta00)]]; %Characteristic matrix of film, s/TE pol.
BC00_p=[[cos(delta00), i*sin(delta00)/eta00_p];[eta00_p*i*sin(delta00), cos(delta00)]]; %Characteristic matrix of film, p/TM pol.

%Medium 1
n1=0.559;
k1=9.81;
y1=n1-i*k1; %characteristic admittance medium 1
theta2=asin(y0*sin(theta1(z))/y1); %angle in medium
d1=35e-9;
%**BELOW CRITICAL ANGLE**
delta1=(2*pi*d1/lambda)*sqrt(n1^2-k1^2-n0^2*(sin(theta1(z)))^2-2*i*n1*k1);
eta1_s=sqrt(n1^2-k1^2-n0^2*(sin(theta1(z)))^2-2*i*n1*k1); %absorbing optical admittance, s/TE pol.
eta1_p=y1^2/eta1_s; %absorbing optical admittance, p/TM pol.
%**ABOVE CRITICAL ANGLE**
BC1_s=[[cos(delta1), i*sin(delta1)/eta1_s];[eta1_s*i*sin(delta1), cos(delta1)]]; %Characteristic matrix, film 1, s/TE pol.
BC1_p=[[cos(delta1), i*sin(delta1)/eta1_p];[eta1_p*i*sin(delta1), cos(delta1)]]; %Characteristic matrix, film 1, p/TM pol.

%Medium 2
n2=1.50;
k2=0.0;
```

```
y2=n2-i*k2; %characteristic admittance in medium
d2=200e-9;
%**BELOW CRITICAL ANGLE**
delta2=(2*pi*d2/lambda)*sqrt(n2^2-k2^2-n0^2*(sin(theta1(z)))^2-2*i*n2*k2);
eta2_s=sqrt(n2^2-k2^2-n0^2*(sin(theta1(z)))^2-2*i*n2*k2); %absorbing optical admittance, s/TE pol.
eta2_p=y2^2/eta2_s; %absorbing optical admittance, p/TM pol.
%**ABOVE CRITICAL ANGLE**
BC2_s=[[cos(delta2), i*sin(delta2)/eta2_s];[eta2_s*i*sin(delta2), cos(delta2)]]; %Characteristic matrix of film, s/TE
pol.
BC2_p=[[cos(delta2), i*sin(delta2)/eta2_p];[eta2_p*i*sin(delta2), cos(delta2)]]; %Characteristic matrix of film,
p/TM pol.

%Medium 3
n3=1.46;
k3=0.00;
y3=n3-i*k3; %characteristic admittance in medium
d3=3134e-9;
%**BELOW CRITICAL ANGLE**
delta3=(2*pi*d3/lambda)*sqrt(n3^2-k3^2-n0^2*(sin(theta1(z)))^2-2*i*n3*k3);
eta3_s=sqrt(n3^2-k3^2-n0^2*(sin(theta1(z)))^2-2*i*n3*k3); %absorbing optical admittance, s/TE pol.
eta3_p=y3^2/eta3_s; %absorbing optical admittance, p/TM pol.
%**ABOVE CRITICAL ANGLE**
BC3_s=[[cos(delta3), i*sin(delta3)/eta3_s];[eta3_s*i*sin(delta3), cos(delta3)]]; %Characteristic matrix of film, s/TE
pol.
BC3_p=[[cos(delta3), i*sin(delta3)/eta3_p];[eta3_p*i*sin(delta3), cos(delta3)]]; %Characteristic matrix of film,
p/TM pol.
 %Substrate
ns=3.46;
ks=0;
ys=ns-i*ks; %characteristic admittance substrate
etas_s=conj(sqrt(ns^2-ks^2-n0^2*(sin(theta1(z)))^2-2*i*ns*ks)); %absorbing optical admittance, s/TE pol.
etas_p=ys^2/etas_s; %absorbing optical admittance, p/TM pol.
BCs_s=[1;etas_s]; %Characteristic matrix, substrate, s/TE pol.
BCs_p=[1;etas_p]; %Characteristic matrix, substrate, p/TM pol.

%Matrix
BC_s=BC00_s*BC1_s*BC2_s*BC3_s*BCs_s; %final stack matrix, s/TE pol.
BC_p=BC00_p*BC1_p*BC2_p*BC3_p*BCs_p; %final stack matrix, p/TM pol.

rho_s=(eta0_s*BC_s(1,1)-BC_s(2,1))/(eta0_s*BC_s(1,1)+BC_s(2,1)); %Amplitude Reflection Coefficient s/TE pol
rho_p=(eta0_p*BC_p(1,1)-BC_p(2,1))/(eta0_p*BC_p(1,1)+BC_p(2,1)); %Amplitude Reflection Coefficient p/TM
pol
R_s(z)=rho_s*conj(rho_s); %Reflectance s/TE pol
R_p(z)=rho_p*conj(rho_p); %Reflectance p/TM pol

end
hold on
plot(theta1*180/pi,R_p,'.g');
```

3-Optical Delay Simulation Matlab Code

```
% Big Ring Delay sim

clc
clear all
% close all
% ********************************
% Waveguide Ring and spectrum setup
% ********************************
c = 299792458;                          % speed of light (m/s)
lambdaspec = (1540:0.001:1560)*1e-9;    % wavelength (m)
fspec = c./lambdaspec;                  % frequency (Hz)
wspec = 2.*pi.*fspec;                   % radian frequency
ng = 3.9;                % waveguide group index
R = 30e-6;               % Ring radius (m)
FSR = c./(2.*pi.*R.*ng);    % Free Spectral Range (Hz)
T = 1/FSR                % Ring Feedback Time (s)
T_ring = T;
% ring loss (alpha/cm)
CarrierLifetime = 500e-12;% Carrier Life time(s)
Ring_dbcm = 2;          % 30 um Rings
WG_dbcm = 1;
alpha_WG = log(10^(WG_dbcm/10));
alpha_ring = log(10^(Ring_dbcm/10));
ring_rt_loss = exp(-alpha_ring.*pi*R*1e2); % ring loss (amp norm)
ring_hrt_loss = exp(-alpha_ring/2.*pi*R*1e2);  % half ring loss (amp norm)
gap_loss = ring_rt_loss;

% Coupling Strength
coup_pow_in = 0.15;    % 30 um rings
coup_pow_out = 0.15;
sin = -1j*sqrt(coup_pow_in);   % amp coupling coeffs
sout = -1j*sqrt(coup_pow_out);
cin = sqrt(1-coup_pow_in);
cout = sqrt(1-coup_pow_out);
ring_response_through = (cin - cin.*ring_rt_loss.*exp(-1j.*wspec.*T))./(1- cin.*cin.*ring_rt_loss.*exp(-
1j.*wspec.*T));
ring_response_drop = (sin.*sin.*ring_hrt_loss.*exp(-1j.*wspec.*T./2))./(1- cin.*cin.*ring_rt_loss.*exp(-
1j.*wspec.*T));

% ********************************
% Pulse and time setup
% ********************************

dt = T./100;        % sample time
tmax = 2e-9;        % simulation time
t = 0:dt:tmax;      % time (s)
tlen = length(t);
tlenhf = round(tlen/2);

[val,l0idx] = min(abs(ring_response_through));
lambda0 = lambdaspec(l0idx)
% lambda0 = 1542.009e-9;          % Pulse center wavelength (m)
```

```
f0 = c./lambda0;                % Pulse center frequency (Hz)

pulsewidth = 30e-12;        % Pulse width (s)
pulsedelay = 100e-12;       % Pulse delay (s)

pulsein = exp(-(t - pulsedelay).^2/(pulsewidth).^2).*exp(1j*2*pi*(f0)*t);

% ********************************
% Waveguide and Ring Modulation
% ********************************
% carriers_max = 21e17;       % 20 um Rings
carriers_in = 3e17;
carriers_out = 3e17;
Carrierout=carriers_in.*exp((-t)./CarrierLifetime);
plot(Carrierout);
hold on;
dng_in = -2.5e-22.*(carriers_in.^1.03) - 8.0e-18.*(carriers_in.^0.8);
dalpha_in = 2e-21.*(carriers_in.^1.2) + 8e-20.*(carriers_in.^1.1);

FSR_mod_in = c./(2.*pi.*R.*(ng+dng_in));    % Free Spectral Range (Hz)
T_mod_in = 1/FSR_mod_in;                  % Ring Feedback Time (s)

ring_rt_loss_mod_in = exp(-(alpha_ring+dalpha_in).*2*pi*R*1e2); % ring loss (amp norm)
ring_hrt_loss_mod_in = exp(-(alpha_ring+dalpha_in).*pi*R*1e2);  % half ring loss (amp norm)

ring_response_through_mod_in = (cin - cin.*ring_rt_loss_mod_in.*exp(-1j.*wspec.*T_mod_in))./(1-
cin.*cin.*ring_rt_loss_mod_in.*exp(-1j.*wspec.*T_mod_in));
ring_response_drop_mod_in = (sin.*sin.*ring_hrt_loss_mod_in.*exp(-1j.*wspec.*T_mod_in./2))./(1-
cin.*cin.*ring_rt_loss_mod_in.*exp(-1j.*wspec.*T_mod_in));
output_ring_shift = -0.135*pi;
ring_response_through_out = (cin - cin.*ring_rt_loss.*exp(-1j.*(wspec.*T - output_ring_shift)))./(1-
cin.*cin.*ring_rt_loss.*exp(-1j.*(wspec.*T - output_ring_shift)));
ring_response_through_mod_out = (cin - cin.*ring_rt_loss_mod_in.*exp(-1j.*(wspec.*T_mod_in -
output_ring_shift)))./(1- cin.*cin.*ring_rt_loss_mod_in.*exp(-1j.*(wspec.*T_mod_in - output_ring_shift)));

% with time
switch_time = 0.5e-12;
n_switch = round(switch_time/dt);
n_switch_off = n_switch;

switch_on = 140e-12;    % 40 ps pulse width
% switch_on = 120e-12;    % 10 ps pulse width
n_on = round(switch_on/dt);
switch_off = 225e-12;
n_off = round(switch_off/dt);
carriers_time_in = [zeros(1,n_on) linspace(0,carriers_in,n_switch) carriers_in.*ones(1,(tlen-n_switch-n_on))];
carriers_time_out = [zeros(1,n_off) linspace(0,carriers_out,n_switch_off) carriers_out.*ones(1,(tlen-n_switch_off-
n_off))];
%plot(t,carriers_time_in)
dng_time_in = -8.8e-22.*carriers_time_in - 8.5e-18.*(carriers_time_in.^0.8);
dalpha_time_in = 8.5e-18.*carriers_time_in + 6e-18.*carriers_time_in;
dng_time_out = -8.8e-22.*carriers_time_out - 8.5e-18.*(carriers_time_out.^0.8);
dalpha_time_out = 8.5e-18.*carriers_time_out + 6e-18.*carriers_time_out;
```

```
ring_hrt_loss_time_in = exp(-(alpha_ring+dalpha_time_in).*pi*R*1e2);  % half ring loss (amp norm)
phase_hrt_time_in = exp(-1j.*2.*pi.*f0.*pi.*R.*dng_time_in/c);
ring_hrt_loss_time_out = exp(-(alpha_ring+dalpha_time_out).*pi*R*1e2);  % half ring loss (amp norm)
phase_hrt_time_out = exp(-1j.*(2.*pi.*f0.*pi.*R.*dng_time_out/c - output_ring_shift));

% *******************************
% Ring feedback sim
% *******************************
Spiral = 5593e-6;
T_spi = (Spiral.*ng)./c;
spi_loss = exp(-alpha_WG*Spiral*1e2);
rhrt_smp = round(T_ring./(dt*2));
gap_smp = round(T_ring./dt);
spi_smp = round(T_spi./dt);
Ea1_in = pulsein;
Eb1_in = zeros(1,tlen);
Ec1_in = zeros(1,tlen);
Ed1_in = zeros(1,tlen);
Ea2_in = zeros(1,tlen);
Eb2_in = zeros(1,tlen);
Ec2_in = zeros(1,tlen);
Ed2_in = zeros(1,tlen);
Eb1_out = zeros(1,tlen);
Ec1_out = zeros(1,tlen);
Ed1_out = zeros(1,tlen);
Ea2_out = zeros(1,tlen);
Eb2_out = zeros(1,tlen);
Ec2_out = zeros(1,tlen);
Ed2_out = zeros(1,tlen);

Ec1_in(1:rhrt_smp) = cin.*Ea1_in(1:rhrt_smp);
Ed1_in(1:rhrt_smp) = sin.*Ea1_in(1:rhrt_smp);
for n = (rhrt_smp + 1):1:gap_smp

    Eb1_in(n) = Ed2_in(n-rhrt_smp).*ring_hrt_loss_time_in(n).*phase_hrt_time_in(n);
    Ec1_in(n) = cin.*Ea1_in(n) + sin.*Eb1_in(n);
    Ed1_in(n) = sin.*Ea1_in(n) + cin.*Eb1_in(n);

    Eb2_in(n) = Ed1_in(n-rhrt_smp).*ring_hrt_loss_time_in(n).*phase_hrt_time_in(n);
    Ec2_in(n) = cin.*Ea2_in(n) + sin.*Eb2_in(n);
    Ed2_in(n) = sin.*Ea2_in(n) + cin.*Eb2_in(n);
end;
for n = (gap_smp + 1):1:spi_smp
    Eb1_in(n) = Ed2_in(n-rhrt_smp).*ring_hrt_loss_time_in(n).*phase_hrt_time_in(n);
    Ec1_in(n) = cin.*Ea1_in(n) + sin.*Eb1_in(n);
    Ed1_in(n) = sin.*Ea1_in(n) + cin.*Eb1_in(n);

    Eb2_in(n) = Ed1_in(n-rhrt_smp).*ring_hrt_loss_time_in(n).*phase_hrt_time_in(n);
    Ec2_in(n) = cin.*Ea2_in(n) + sin.*Eb2_in(n);
    Ed2_in(n) = sin.*Ea2_in(n) + cin.*Eb2_in(n);

    Ea2_out(n) = Ec2_in(n-gap_smp).*gap_loss;
    Eb2_out(n) = Ed1_out(n-rhrt_smp).*ring_hrt_loss_time_out(n).*phase_hrt_time_out(n);
    Ec2_out(n) = cout.*Ea2_out(n) + sout.*Eb2_out(n);
    Ed2_out(n) = sout.*Ea2_out(n) + cout.*Eb2_out(n);
```

```
    Eb1_out(n) = Ed2_out(n-rhrt_smp).*ring_hrt_loss_time_out(n).*phase_hrt_time_out(n);
    Ec1_out(n) = sout.*Eb1_out(n);
    Ed1_out(n) = cout.*Eb1_out(n);

end;
for n = (spi_smp + 1):1:tlen
    Eb1_in(n) = Ed2_in(n-rhrt_smp).*ring_hrt_loss_time_in(n).*phase_hrt_time_in(n);
    Ec1_in(n) = cin.*Ea1_in(n) + sin.*Eb1_in(n);
    Ed1_in(n) = sin.*Ea1_in(n) + cin.*Eb1_in(n);
    Ea2_in(n) = Ec2_out(n-spi_smp).*spi_loss;

    Eb2_in(n) = Ed1_in(n-rhrt_smp).*ring_hrt_loss_time_in(n).*phase_hrt_time_in(n);
    Ec2_in(n) = cin.*Ea2_in(n) + sin.*Eb2_in(n);
    Ed2_in(n) = sin.*Ea2_in(n) + cin.*Eb2_in(n);



    Ea2_out(n) = Ec2_in(n-gap_smp).*gap_loss;
    Eb2_out(n) = Ed1_out(n-rhrt_smp).*ring_hrt_loss_time_out(n).*phase_hrt_time_out(n);
    Ec2_out(n) = cout.*Ea2_out(n) + sout.*Eb2_out(n);
    Ed2_out(n) = sout.*Ea2_out(n) + cout.*Eb2_out(n);
    Eb1_out(n) = Ed2_out(n-rhrt_smp).*ring_hrt_loss_time_out(n).*phase_hrt_time_out(n);
    Ec1_out(n) = sout.*Eb1_out(n);
    Ed1_out(n) = cout.*Eb1_out(n);

end;
% ********************************
% Pulse FFT's
% ********************************

Sin = fftshift(fft(Ea1_in));
% St = fftshift(fft(Ec1));
% Sd = fftshift(fft(Ec2));

df = 1/tmax;
fmax = 1/dt;
f_fft = 0:df:fmax;

[val,fidx] = max(abs(Sin));
lambda_fft = c./(f0 + f_fft(fidx) - f_fft);

% ********************************
% Plots
% ********************************
 figure(1)
set(gca,'fontsize',14)
plot(lambdaspec.*1e9,10*log10(abs(ring_response_through)),'b','linewidth',1.5)
hold on
plot(lambdaspec.*1e9,10*log10(abs(ring_response_drop)),'b--','linewidth',1.5)
plot(lambdaspec.*1e9,10*log10(abs(ring_response_through_mod_in)),'r','linewidth',1.5)
plot(lambdaspec.*1e9,10*log10(abs(ring_response_drop_mod_in)),'r--','linewidth',1.5)
plot(lambda_fft.*1e9,10*log10(abs(Sin)./max(Sin)),'k','linewidth',1.5)
plot(lambdaspec.*1e9,10*log10(abs(ring_response_through_out)),'g','linewidth',1.5)
plot(lambdaspec.*1e9,10*log10(abs(ring_response_through_mod_out)),'g--','linewidth',1.5)
```

```
hold off
title('Ring response')
xlabel('wavelength (nm)')
ylabel('Power (db)')
axis([lambdaspec(1)*1e9 lambdaspec(end)*1e9 -50 0])

figure(2)
set(gca,'fontsize',14)
plot(t.*1e12,10*log10(abs(pulsein).^2),'k','linewidth',1.5)
hold on
plot(t.*1e12,10*log10(abs(Ec2_in).^2),'b','linewidth',1.5)
plot(t.*1e12,10*log10(abs(Ec1_in).^2),'g','linewidth',1.5)
plot(t.*1e12,10*log10(abs(Ec1_out).^2),'r','linewidth',1.5)
hold off
title('Pulse')
xlabel('time (ps)')
ylabel('Pulse Power (norm)')
legend('Input','Store','Pass','Output',4)
axis([t(1)*1e12 t(end)*1e12 -25 0])

figure(3)
set(gca,'fontsize',14)
plot(t.*1e12,(abs(pulsein).^2),'k','linewidth',1.5)
hold on
plot(t.*1e12,(abs(Ec1_out).^2),'r','linewidth',1.5)
hold off
title('Single ring Power Coupling')
xlabel('time (ps)')
ylabel('Pulse Power (norm)')
legend('Input','Output')
axis([t(1)*1e12 700 0 1])
```

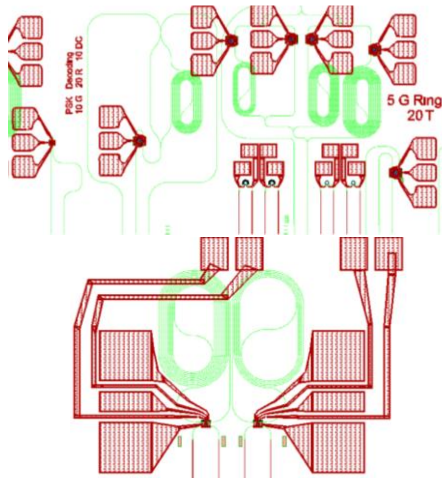
Appendix II

Unified CAD design for multi project wafer and double pattern usage in integrated photonics.

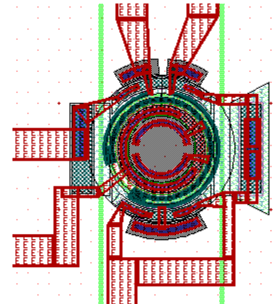
Unified CAD Design

ADDITIONAL PROJECTS

Make working electro-optic modulators for all kinds of devices, reduce fabrication cost for future production



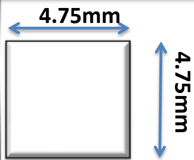
Same Requirements:
Simple modulator



Use Ebeam to pattern different waveguide shape, use Photolithography to pattern all other levels

CAD Design

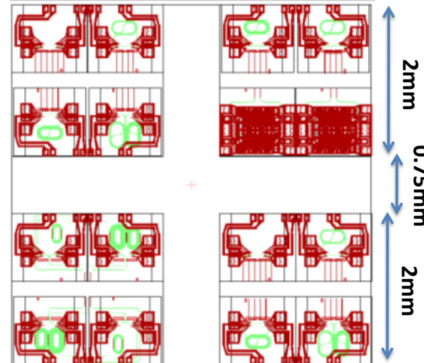
VARIATIONS OF DESIGN



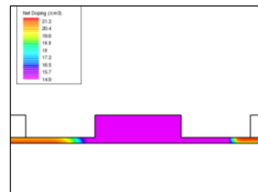
Variations we need:

1. Waveguide gap, waveguide pattern
2. Positive or Negative resist
3. Triple pattern trick
4. Modulator type: PIN, PN, Interleaved
5. Modulator with Micro-oven, without oven
6. Modulator Radius:5um, 10um, 20um
7. Contact doping distance
8. Interleaved device finger size

Waveguide mask sets:



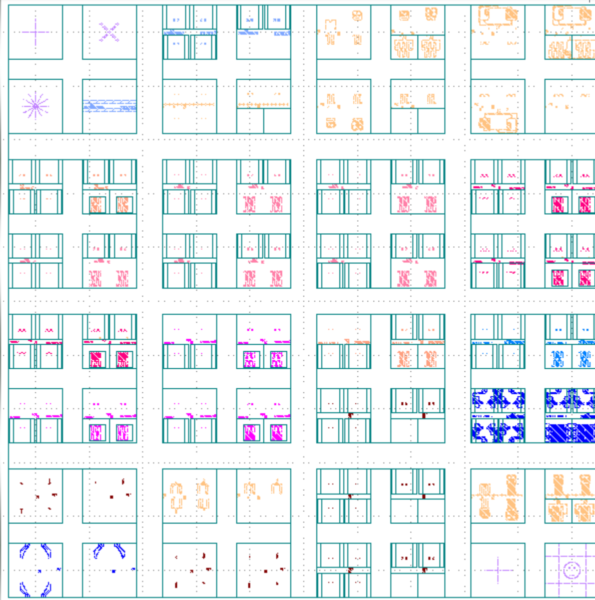
Trade off of speed and loss at defining gap between doping and waveguide

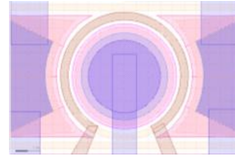


VARIATIONS OF DESIGN

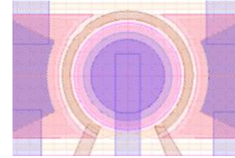
R·I·T Nanophotonics Group

CAD Design

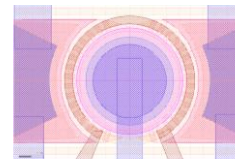




PIN Diode



Depletion PD Diode



Interleaved Modulator

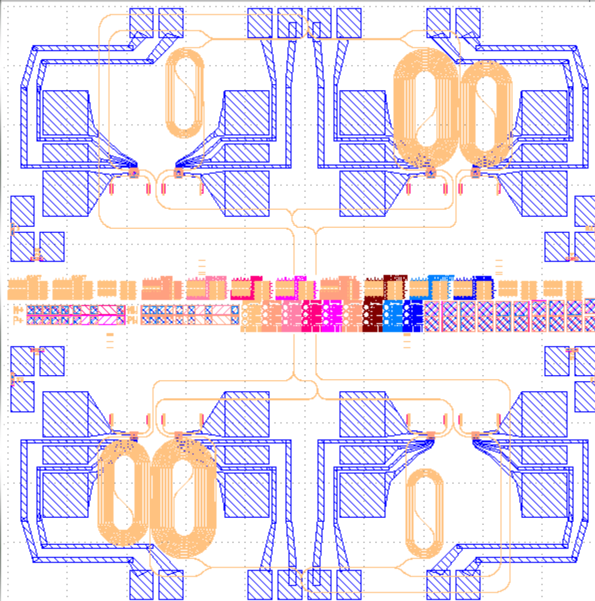
nanophotonics.rit.edu

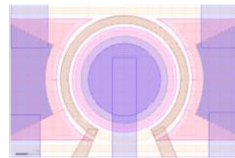
3

VARIATIONS OF DESIGN

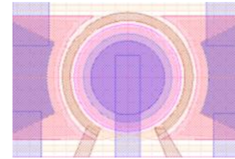
R·I·T Nanophotonics Group

CAD Design

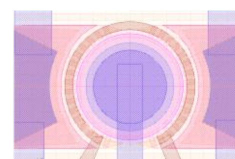




PIN Diode



Depletion PD Diode



Interleaved Modulator

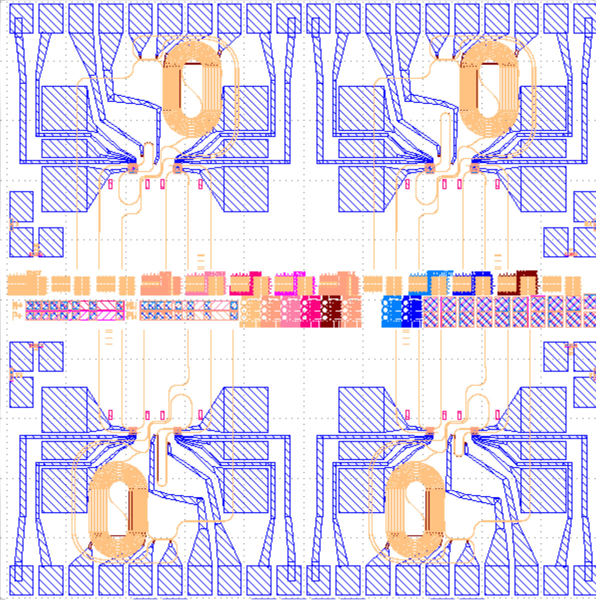
nanophotonics.rit.edu

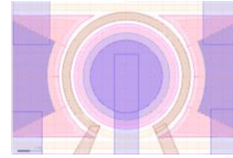
4

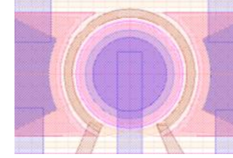
VARIATIONS OF DESIGN

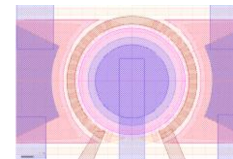
RIT Nanophotonics Group

CAD Design




PIN Diode

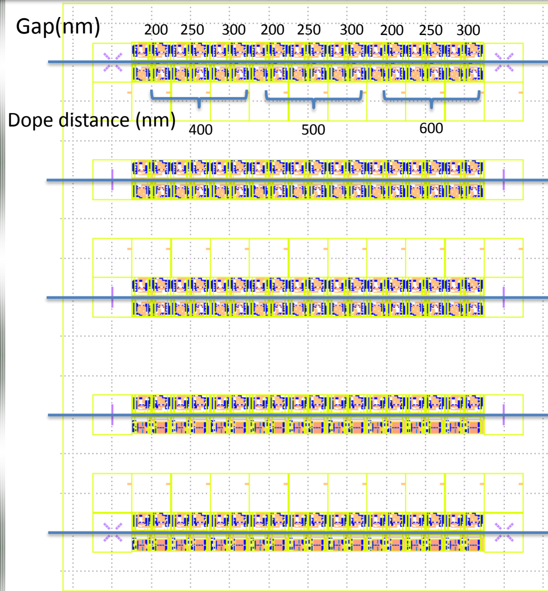

Depletion PD Diode

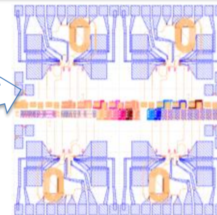

Interleaved Modulator

CHIP SETTING

RIT Nanophotonics Group

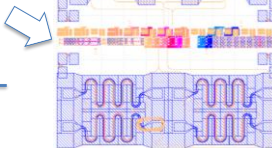
CAD Design

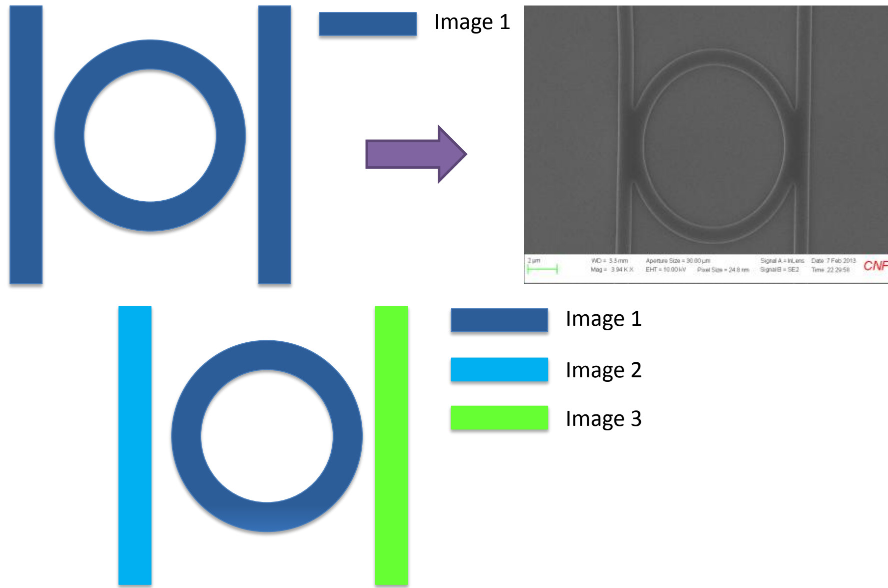


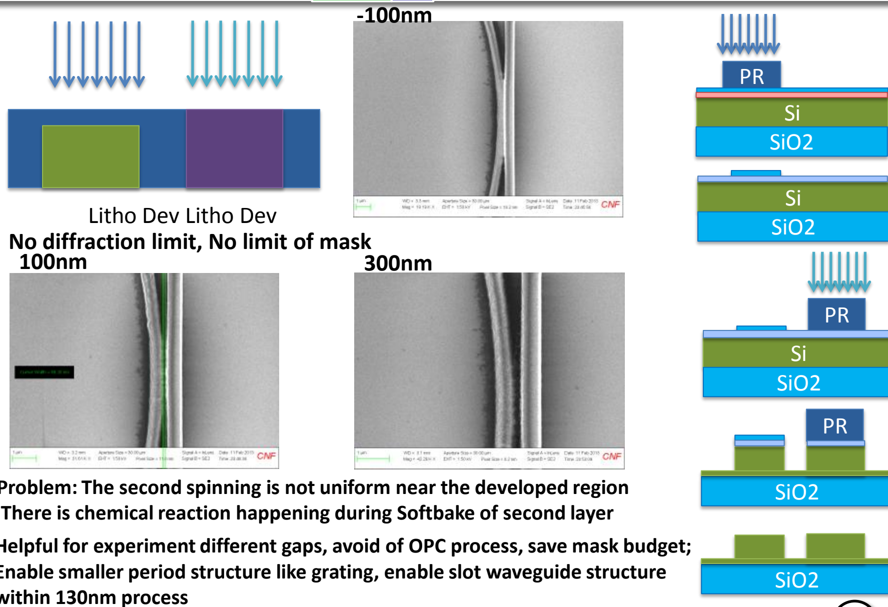


5um 10um ring OTDM

20um ring OTDM




Photolitho Pattern development
R·I·T
Nanophotonics Group
Process Engineer
Image 1
Image 1
Image 2
Image 3
nanophotonics.rit.edu
7


Double pattern of waveguide
R·I·T
Nanophotonics Group
Process Engineer
-100nm
Litho Dev Litho Dev
No diffraction limit, No limit of mask
100nm
300nm
PR
Si
SiO2
Si
SiO2
PR
Si
SiO2
PR
SiO2
SiO2
Problem: The second spinning is not uniform near the developed region
There is chemical reaction happening during Softbake of second layer
Helpful for experiment different gaps, avoid of OPC process, save mask budget;
Enable smaller period structure like grating, enable slot waveguide structure
within 130nm process
nanophotonics.rit.edu
8

References

[1] M. Bertolotti, *The History of Laser*. Taylor & Francis, 2004.

[2] "FTTH Council - Definition of Terms," *FTTH Council*, 2009. [Online]. Available: http://www.ftthcouncilmena.org/documents/FTTHdefinitions/FTTH-Definitions-Revision_January_2009.pdf.

[3] M. B. J. O. K. V. Schmatz, "Optical Interconnects: Intra-system data transfer with light," 2005. [Online]. Available: http://www.zurich.ibm.com/pdf/sys/Optical_Interconnects@IBM-ZRL_2005-04_E.pdf.

[4] M. Paniccia, "The 50Gbps Silicon photonic Link," *Intel.com*, 2010. [Online]. Available: http://blogs.intel.com/intellabs/2010/07/23/50g-link/.

[5] S. Chaudhury, "A Tutorial and Survey on Thermal-Aware VLSI Design: Tools and Techniques," *Int. J. Recent Trends Eng.*, vol. 2, no. 8, 2009.

[6] H. Sanchez, "Design implications of low-K," *Proc. IEEE 2003 Int. Interconnect Technol. Conf. (Cat. No.03TH8695)*, 2003.

[7] M. W. Hall, J. M. Anderson, S. P. Amarasinghe, B. R. Murphy, S.-W. L. S.-W. Liao, and E. Bu, "Maximizing multiprocessor performance with the SUIF compiler," *Computer (Long. Beach. Calif).*, vol. 29, 1996.

[8] K. Olukotun, B. A. Nayfeh, L. Hammond, K. Wilson, and K. Chang, "The case for a single-chip multiprocessor," *ACM SIGPLAN Notices*, vol. 31. pp. 2–11, 1996.

[9] D. M. Tullsen, S. J. Eggers, and H. M. Levy, "Simultaneous multithreading: Maximizing on-chip parallelism," *Proc. 22nd Annu. Int. Symp. Comput. Archit.*, 1995.

[10] B. A. Nayfeh and K. Olukotun, "A single-chip multiprocessor," *Computer (Long. Beach. Calif).*, vol. 30, 1997.

[11] T. Bjerregaard and S. Mahadevan, “A survey of research and practices of Network-on-chip,” *ACM Computing Surveys*, vol. 38. p. 1–es, 2006.

[12] R. P. W. J. Dally and B. Towles, “Not Wires: On-Chip Interconnection Networks,” in *38th Design Automation Conference*, 2001, pp. 681–689.

[13] “Application Note : Understanding Static RAM Operation,” *IBM*, 1997. [Online]. Available: http://www.ece.cmu.edu/~ece548/localcpy/sramop.pdf.

[14] “Processor Architectures.” [Online]. Available: http://www.qdpma.com/CPU/CPU_Nehalem.html.

[15] B. H. K. T. Huang, J.-Q. Lu, D. Popa, “BCB Wafer Bonding Compatible with Bulk Micro Machining,” in *International Electronic Packaging Technical Conference (InterPack)*, 2003.

[16] C. Weis, N. Wehn, L. Igor, and L. Benini, “Design space exploration for 3D-stacked DRAMs,” *2011 Des. Autom. Test Eur.*, pp. 1–6, 2011.

[17] M. Facchini, P. Marchal, F. Catthoor, and W. Dehaene, “An RDL-configurable 3D memory tier to replace on-chip SRAM,” in *Design, Automation and test in Europe Conference and Exhibition*, 2010.

[18] A. Biberman, H. L. R. Lira, K. Padmaraju, N. Ophir, J. Chan, M. Lipson, and K. Bergman, “Broadband Silicon Photonic Electrooptic Switch for Photonic Interconnection Networks,” *IEEE Photonics Technol. Lett.*, vol. 23, pp. 504–506, 2011.

[19] T. Hino, R. Kuribayashi, Y. Hashimoto, T. Sugimoto, J. Ushioda, J. Sasaki, I. Ogura, I. Hatakeyama, and K. Kurata, “A 10 Gbps x 12 channel pluggable optical transceiver for high-speed interconnections,” *2008 58th Electron. Components Technol. Conf.*, 2008.

[20] J. E. Cunningham, D. Beckman, D. Mcelfresh, C. Forrest, D. Cohen, and A. V Krishnamoorthy, “Scaling VCSEL reliability up to 250Terabits / s of system bandwidth,” *OSA/IP*, vol. IThA3, 2005.

[21] A. R. Y.A.Vlasov, S. Assefa, W. M. J. Green, M. Yang, C. L. Schow, "Si Integrated Nanophotonics for on-chip optical interconnects," in *European Conference on Optical Communications*, 2010.

[22] A. P. K. Graham T. Reed, *Silicon Photonics: An Introduction*. Wiley, 2004.

[23] L. H. Frandsen, P. I. Borel, Y. X. Zhuang, A. Harpøth, M. Thorhauge, M. Kristensen, W. Bogaerts, P. Dumon, R. Baets, V. Wiaux, J. Wouters, and S. Beckx, "Ultralow-loss 3-dB photonic crystal waveguide splitter.," *Opt. Lett.*, vol. 29, pp. 1623–1625, 2004.

[24] J. Niehusmann, A. Vörckel, P. H. Bolivar, T. Wahlbrink, and W. Henschel, "Ultrahigh-quality factor silicon-on-insulator microring resonator," *Opt. Lett.*, vol. 29, pp. 2861–2863, 2004.

[25] T. Baehr-Jones, M. Hochberg, C. Walker, and A. Scherer, "High-Q ring resonators in thin silicon-on-insulator," *Appl. Phys. Lett.*, vol. 85, p. 3346, 2004.

[26] C. A. Barrios, Q. Xu, J. Shakya, C. Manolatou, and M. Lipson, "Compact silicon slot-waveguide disk resonator," *2006 Conf. Lasers Electro-Optics 2006 Quantum Electron. Laser Sci. Conf.*, 2006.

[27] P. Knight, "Fundamentals of Photonics," *Journal of Modern Optics*, vol. 39. pp. 1400–1400, 1992.

[28] T. Baba, "Slow light in photonic crystals," *Nature Photonics*, vol. 2. pp. 465–473, 2008.

[29] D. G. Rabus, "Building blocks of ring resonator devices in Integrated Ring Resonators: The Compendium," in *Integrated Ring Resonators:The Compendium*, Springer Berlin Heidelberg, 2007, pp. 111–124.

[30] Christi K. Madsen; Jian H. Zhao, *Optical Filter Design and Analysis: A Signal Processing Approach*. Wiley, 1999.

[31] S.-H. Fang, "Observation of Franz-Keldysh Effect in Silicon," *Chinese J. Phys.*, vol. 4, pp. 41–48, 1966.

[32] R. S. Jacobsen, K. N. Andersen, P. I. Borel, J. Fage-Pedersen, L. H. Frandsen, O. Hansen, M. Kristensen, A. V Lavrinenko, G. Moulin, H. Ou, C. Peucheret, B. Zsigri, and A. Bjarklev, "Strained silicon as a new electro-optic material.," *Nature*, vol. 441, pp. 199–202, 2006.

[33] R. A. Soref, "Silicon-based optoelectronics," *Proc. IEEE*, vol. 81, 1993.

[34] T.S.Moss; G. J. Burrell and B. Ellis, *Semicondcutor opto-electronics*. London, 1973.

[35] Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, "Micrometre-scale silicon electro-optic modulator.," *Nature*, vol. 435, pp. 325–327, 2005.

[36] S. Manipatruni, Q. X. Q. Xu, B. Schmidt, J. Shakya, and M. Lipson, "High Speed Carrier Injection 18 Gb/s Silicon Micro-ring Electro-optic Modulator," *LEOS 2007 - IEEE Lasers Electro-Optics Soc. Annu. Meet. Conf. Proc.*, 2007.

[37] C. A. Barrios, "Electrooptic modulation of multisilicon-on-insulator photonic wires," *J. Light. Technol.*, vol. 24, 2006.

[38] N. K. Hon, L. Z. L. Zhou, and A. W. Poon, "Silicon depletion-type microdisk electro-optic modulators using selectively integrated Schottky diodes," *2007 Conf. Lasers Electro-Optics*, 2007.

[39] A. Liu, L. Liao, D. Rubin, H. Nguyen, B. Ciftcioglu, Y. Chetrit, N. Izhaky, and M. Paniccia, "High-speed optical modulation based on carrier depletion in a silicon waveguide.," *Opt. Express*, vol. 15, pp. 660–668, 2007.

[40] G. Ghosh, *Handbook of thermo-optic coefficients of optical materials with applications*. Academic Press, 1998.

[41] K. Yee, "Numerical solution of initial boundary value problems involving Maxwell's equations in isotropic media," *Antennas Propagation, IEEE Trans.*, vol. 14, pp. 302–307, 1966.

[42] D. M. Sullivan, *Electromagnetic Simulation Using the FDTD Method*. 2000, p. 165.

[43] K. Okamoto, *Fundamentals of Optical Waveguides*. 2006, p. 561.

[44] Clifford R. Pollock; Michal. Lipson, *Integrated Photonics*. Springer, 2003.

[45] "RSoft BeamPROP Manual," *Synopsys*. [Online]. Available: http://optics.synopsys.com/rsoft/rsoft-passive-device-beamprop.html#.

[46] L. Vivien, A. Polzer, D. Marris-Morini, J. Osmond, J. M. Hartmann, P. Crozat, E. Cassan, C. Kopp, H. Zimmermann, and J. M. Fédéli, "Zero-bias 40Gbit/s germanium waveguide photodetector on silicon," *Optics Express*, vol. 20. p. 1096, 2012.

[47] M. Heyns, A. Alian, G. Brammertz, M. Caymax, Y. C. Chang, L. K. Chu, B. De Jaeger, G. Eneman, F. Gencarelli, G. Groeseneken, G. Hellings, A. Hikavyy, T. Y. Hoffmann, M. Houssa, C. Huyghebaert, D. Leonelli, D. Lin, R. Loo, W. Magnus, C. Merckling, M. Meuris, J. Mitard, L. Nyns, T. Orzali, R. Rooyackers, S. Sioncke, B. Soree, X. Sun, A. Vandooren, A. S. Verhulst, B. Vincent, N. Waldron, G. Wang, W. E. Wang, and L. Witters, "Advancing CMOS beyond the Si roadmap with Ge and III/V devices," *2011 Int. Electron Devices Meet.*, pp. 13.1.1–13.1.4, 2011.

[48] G. Li, J. Yao, H. Thacker, A. Mekis, X. Zheng, I. Shubin, Y. Luo, J. Lee, K. Raj, J. E. Cunningham, and A. V. Krishnamoorthy, "Ultralow-loss, high-density SOI optical waveguide routing for macrochip interconnects," *Optics Express*, vol. 20. p. 12035, 2012.

[49] A. V. Krishnamoorthy, X. Zheng, G. Li, J. Yao, T. Pinguet, A. Mekis, H. Thacker, I. Shubin, Y. Luo, K. Raj, and J. E. Cunningham, "Exploiting CMOS Manufacturing to Reduce Tuning Requirements for Resonant Optical Devices," *IEEE Photonics Journal*, vol. 3. pp. 567–579, 2011.

[50] W. A. Zortman, D. C. Trotter, and M. R. Watts, "Silicon photonics manufacturing.," *Opt. Express*, vol. 18, pp. 23598–23607, 2010.

[51] C. T. DeRose, D. C. Trotter, W. A. Zortman, A. L. Starbuck, M. Fisher, M. R. Watts, and P. S. Davids, "Ultra compact 45 GHz CMOS compatible

Germanium waveguide photodiode with low dark current," *Optics Express*, vol. 19. p. 24897, 2011.

[52] R. E. Camacho-Aguilera, Y. Cai, N. Patel, J. T. Bessette, M. Romagnoli, L. C. Kimerling, and J. Michel, "An electrically pumped germanium laser," *Optics Express*, vol. 20. p. 11316, 2012.

[53] M. Lamponi, S. Keyvaninia, C. Jany, F. Poingt, F. Lelarge, G. de Valicourt, G. Roelkens, D. Van Thourhout, S. Messaoudene, J.-M. Fedeli, and G. H. Duan, "Low-Threshold Heterogeneously Integrated InP/SOI Lasers With a Double Adiabatic Taper Coupler," *IEEE Photonics Technology Letters*, vol. 24. pp. 76–78, 2012.

[54] X. Zheng, F. Liu, J. Lexau, D. Patil, G. Li, Y. Luo, H. D. Thacker, I. Shubin, J. Yao, K. Raj, R. Ho, J. E. Cunningham, and A. V. Krishnamoorthy, "Ultralow Power 80 Gb/s Arrayed CMOS Silicon Photonic Transceivers for WDM Optical Links," *Journal of Lightwave Technology*, vol. 30. pp. 641–650, 2012.

[55] A. Pratt, "Overview of the use of copper interconnects in the semiconductor industry." .

[56] J. Reid, S. Mayer, E. Broadbetrt, E. Klawuhn, and K. Ashtiani, "Factors influencing damascene feature fill using copper PVD and electroplating," *Solid State Technol.*, vol. 43, pp. 86–103, 2000.

[57] Q. Xu, D. Fattal, and R. G. Beausoleil, "Silicon microring resonators with 1.5-μm radius," *Optics Express*, vol. 16. p. 4309, 2008.

[58] J. K. Park and I. Yun, "Modeling of avalanche gain for high-speed InP/InGaAs avalanche photodiodes," *2008 IEEE Int. Conf. Electron Devices Solid-State Circuits*, 2008.

[59] K.-W. A. K.-W. Ang, J. W. Ng, A. E.-J. Lim, M.-B. Y. M.-B. Yu, G.-Q. L. G.-Q. Lo, and D.-L. K. D.-L. Kwong, "Waveguide-integrated Ge/Si avalanche photodetector with 105GHz gain-bandwidth product," *Opt. Fiber Commun. (OFC), collocated Natl. Fiber Opt. Eng. Conf. 2010 Conf.*, 2010.

[60] Z. Huang, J. Oh, and J. C. Campbell, "Back-side-illuminated high-speed Ge photodetector fabricated on Si substrate using thin SiGe buffer layers," *Appl. Phys. Lett.*, vol. 85, p. 3286, 2004.

[61] T.-Y. L. T.-Y. Liow, K.-W. A. K.-W. Ang, Q. F. Q. Fang, J.-F. S. J.-F. Song, Y.-Z. X. Y.-Z. Xiong, M.-B. Y. M.-B. Yu, G.-Q. L. G.-Q. Lo, and D.-L. K. D.-L. Kwong, "Silicon Modulators and Germanium Photodetectors on SOI: Monolithic Integration, Compatibility, and Performance Optimization," *IEEE J. Sel. Top. Quantum Electron.*, vol. 16, 2010.

[62] J. Grym, *Semiconductor Technologies*. InTech, 2010.

[63] F. Namavar, H. P. Maruska, and N. M. Kalkhoran, "Visible electroluminescence from porous silicon np heterojunction diodes," *Appl. Phys. Lett.*, vol. 60, p. 2514, 1992.

[64] L. Pavesi, L. Dal Negro, C. Mazzoleni, G. Franzò, and F. Priolo, "Optical gain in silicon nanocrystals.," *Nature*, vol. 408, pp. 440–444, 2000.

[65] M. F. and C. W. P. A. J. Kenyon, P F Trwoga, "Optical properties of PECVD erbium-doped siliconrich silica: evidence for energy transfer between silicon microclusters and erbium ions," *J. Phys. Condens. Matter*, no. 6, pp. 319–324, 1994.

[66] B. Zheng, J. Michel, F. Y. G. Ren, L. C. Kimerling, D. C. Jacobson, and J. M. Poate, "Room-temperature sharp line electroluminescence at λ=1.54 μm from an erbium-doped, silicon light-emitting diode," *Appl. Phys. Lett.*, vol. 64, p. 2842, 1994.

[67] C. Peng, Q. Huang, W. Cheng, J. Zhou, Y. Zhang, T. Sheng, and C. Tung, "Optical properties of Ge self-organized quantum dots in Si," *Physical Review B*, vol. 57. pp. 8805–8808, 1998.

[68] G. He and H. Atwater, "Interband Transitions in SnxGe1-x Alloys," *Physical Review Letters*, vol. 79. pp. 1937–1940, 1997.

[69] H. Rong, A. Liu, R. Jones, O. Cohen, D. Hak, R. Nicolaescu, A. Fang, and M. Paniccia, "An all-silicon Raman laser.," *Nature*, vol. 433, pp. 292–294, 2005.

[70] A. W. Fang, H. Park, O. Cohen, R. Jones, M. J. Paniccia, and J. E. Bowers, "Electrically pumped hybrid AlGaInAs-silicon evanescent laser.," *Opt. Express*, vol. 14, pp. 9203–9210, 2006.

[71] M. E. Groenert, C. W. Leitz, A. J. Pitera, V. Yang, H. Lee, R. J. Ram, and E. A. Fitzgerald, "Monolithic integration of room-temperature cw GaAs/AlGaAs lasers on Si substrates via relaxed graded GeSi buffer layers," *J. Appl. Phys.*, vol. 93, pp. 362–367, 2003.

[72] S. Jongthammanurak, J. F. Liu, K. Wada, D. Cannon, D. T. Danielson, D. Pan, J. Michel, and L. C. Kimerling, "Large Electro-Optic Effect in Tensile Strained Ge-on-Si Films," *3rd IEEE Int. Conf. Gr. IV Photonics, 2006.*, 2006.

[73] J. Liu, X. Sun, D. Pan, X. Wang, L. C. Kimerling, T. L. Koch, and J. Michel, "Tensile-strained, n-type Ge as a gain medium for monolithic laser integration on Si.," *Opt. Express*, vol. 15, pp. 11272–11277, 2007.

[74] Y. Ishikawa, K. Wada, D. D. Cannon, J. Liu, H.-C. Luan, and L. C. Kimerling, "Strain-induced band gap shrinkage in Ge grown on Si substrate," *Appl. Phys. Lett.*, vol. 82, pp. 2044–2046, 2003.

[75] H. Ishio, J. Minowa, and K. Nosu, "Review and status of wavelength-division-multiplexing technology and its application," *J. Light. Technol.*, vol. 2, 1984.

[76] Y. Z. Guanghui Ren, Shaowu Chen, , Yongpeng Cheng, "Study on inverse taper based mode transformer for low loss coupling between silicon wire waveguide and lensed fiber," *Opt. Commun.*, vol. 284, no. 19, pp. 4782–4788, 2011.

[77] D. Taillaert, F. Van Laere, M. Ayre, W. Bogaerts, D. Van Thourhout, P. Bienstman, and R. Baets, "Grating Couplers for Coupling between Optical Fibers and Nanophotonic Waveguides," *Japanese Journal of Applied Physics*, vol. 45. pp. 6071–6077, 2006.

[78] F. Van Laere, W. Bogaerts, D. Taillaert, P. Dumon, D. Van Thourhout, and R. Baets, "Compact Focusing Grating Couplers Between Optical Fibers and

Silicon-on-Insulator Photonic Wire Waveguides," *OFC/NFOEC 2007 - 2007 Conf. Opt. Fiber Commun. Natl. Fiber Opt. Eng. Conf.*, 2007.

[79] D. Taillaert, P. Bienstman, and R. Baets, "Compact efficient broadband grating coupler for silicon-on-insulator waveguides.," *Opt. Lett.*, vol. 29, pp. 2749–2751, 2004.

[80] G. Roelkens, D. Van Thourhout, and R. Baets, "High efficiency Silicon-on-Insulator grating coupler based on a poly-Silicon overlay.," *Opt. Express*, vol. 14, pp. 11622–11630, 2006.

[81] D. Vermeulen, S. Selvaraja, P. Verheyen, G. Lepage, W. Bogaerts, P. Absil, D. Van Thourhout, and G. Roelkens, "High-efficiency fiber-to-chip grating couplers realized using an advanced CMOS-compatible silicon-on-insulator platform.," *Opt. Express*, vol. 18, pp. 18278–18283, 2010.

[82] N. Lindenmann, G. Balthasar, D. Hillerkuss, R. Schmogrow, M. Jordan, J. Leuthold, W. Freude, and C. Koos, "Photonic wire bonding: a novel concept for chip-scale interconnects," *Optics Express*, vol. 20. p. 17667, 2012.

[83] V. R. Almeida, R. R. Panepucci, and M. Lipson, "Nanotaper for compact mode conversion.," *Opt. Lett.*, vol. 28, pp. 1302–1304, 2003.

[84] F. E. Doany, B. G. Lee, S. Assefa, W. M. J. Green, M. Yang, C. L. Schow, C. V. Jahnes, S. Zhang, J. Singer, V. I. Kopp, J. A. Kash, and Y. A. Vlasov, "Multichannel High-Bandwidth Coupling of Ultradense Silicon Photonic Waveguide Array to Standard-Pitch Fiber Array," *J. Light. Technol.*, vol. 29, pp. 475–482, 2011.

[85] V. Schmid, G. ; Leeb, W.R. ; Langer, G. ; Schmidt, "Gbit/s transmission via two-photon-absorption-inscribed optical waveguides on printed circuit boards," *Electron. Lett.*, vol. 45, no. 4, pp. 219–221, 2009.

[86] S. Maruo, O. Nakamura, and S. Kawata, "Three-dimensional microfabrication with two-photon-absorbed photopolymerization.," *Opt. Lett.*, vol. 22, pp. 132–134, 1997.

[87] J. Shu, C. Qiu, X. Zhang, and Q. Xu, "Efficient coupler between chip-level and board-level optical waveguides," *Optics Letters*, vol. 36. p. 3614, 2011.

[88] S. Bernabé, C. Kopp, M. Volpert, J. Harduin, J.-M. Fédéli, and H. Ribot, "Chip-to-chip optical interconnections between stacked self-aligned SOI photonic chips," *Optics Express*, vol. 20. p. 7886, 2012.

[89] M. Volpert, L. Roulet, J. F. Boronat, I. Borel, S. Pocas, and H. Ribot, "Indium deposition processes for ultra fine pitch 3D interconnections," *Electron. Components Technol. Conf. (ECTC), 2010 Proc. 60th*, 2010.

[90] Q. Xu, S. Manipatruni, B. Schmidt, J. Shakya, and M. Lipson, "12.5 Gbit/s carrier-injection-based silicon micro-ring silicon modulators.," *Opt. Express*, vol. 15, pp. 430–436, 2007.

[91] K. Burke, J. Werschnik, and E. K. U. Gross, "Silicon Nanophotonics: Basic Principles, Present Status and Perspectives," *J. Chem. Phys.*, vol. 123, p. 062206, 2005.

[92] R. T. Lorenzo Pavesi, *Silicon Nanocrystals: Fundamentals, Synthesis and Applications*. Wiley, 2010.

[93] M. F. and S. H. M Ito, K Imakita, "Nonlinear Optical Properties of Phosphorus Doped Silicon Nanocrystals/Nanoclusters," *J. Phys. D. Appl. Phys.*, vol. 43, no. 50, p. 505101, 2010.

[94] A. Martínez, J. Blasco, P. Sanchis, J. V Galán, J. García-Rupérez, E. Jordana, P. Gautier, Y. Lebour, S. Hernández, R. Guider, N. Daldosso, B. Garrido, J. M. Fedeli, L. Pavesi, J. Martí, and R. Spano, "Ultrafast all-optical switching in a silicon-nanocrystal-based silicon slot waveguide at telecom wavelengths.," *Nano Lett.*, vol. 10, pp. 1506–1511, 2010.

[95] E. H. A. Szekeres, S. Alexandrova, E. Vlaikova, "Oxidation of Si Surface Nitrogenated by Plasma Immersion N+ Ion Implantation," *Bulg. J. Phys.*, vol. 39, pp. 178–185, 2012.

[96] S. Hernández, P. Pellegrino, A. Martínez, Y. Lebour, B. Garrido, R. Spano, M. Cazzanelli, N. Daldosso, L. Pavesi, E. Jordana, and J. M. Fedeli, "Linear

and nonlinear optical properties of Si nanocrystals in SiO2 deposited by plasma-enhanced chemical-vapor deposition," *J. Appl. Phys.*, vol. 103, p. 064309, 2008.

[97] M. S. and M. Z. J. Heitmann; R. Scholz; L. Yi, "Syntresis and size-control of Si nanocrystals by SiO/SiO2 superlattices," *Electrochem. Soceity Proc.*, 2002.

[98] M. Zacharias, J. Heitmann, R. Scholz, U. Kahler, M. Schmidt, and J. Bläsing, "Size-controlled highly luminescent silicon nanocrystals: A SiO/SiO[sub 2] superlattice approach," *Appl. Phys. Lett.*, vol. 80, p. 661, 2002.

[99] C. M. Hessel, E. J. Henderson, and J. G. C. Veinot, "Hydrogen Silsesquioxane: A Molecular Precursor for Nanocrystalline Si−SiO2 Composites and Freestanding Hydride-Surface-Terminated Silicon Nanoparticles," *Chem. Mater.*, vol. 18, pp. 6139–6146, 2006.

[100] M. G. Kuzyk, *Characterization Techniques and Tabulations for Organic Nonlinear Materials*. Marcel Dekker, 1998.

[101] L. Cao, A. A. Aboketaf, K. Narayanan, A. Elshaari, S. Kowsz, E. Freeman, S. McDermott, S. Preble, J. Bickford, and N. Bambha, "Direct Observation of DC Kerr Electro-Optic Modulation using Silicon Nanocrystals - OSA Technical Digest (online)," in *Frontiers in Optics Conference*, 2012, p. FTu1A.5.

[102] J. Chilwell and I. Hodgkinson, "Thin-films field-transfer matrix theory of planar multilayer waveguides and reflection from prism-loaded waveguides," *Journal of the Optical Society of America A*, vol. 1. p. 742, 1984.

[103] B. Chmielak, M. Waldow, C. Matheisen, C. Ripperda, J. Bolten, T. Wahlbrink, M. Nagel, F. Merget, and H. Kurz, "Pockels effect based fully integrated, strained silicon electro-optic modulator," *Optics Express*, vol. 19. p. 17212, 2011.

[104] D. Korn, R. Palmer, H. Yu, P. C. Schindler, L. Alloatti, M. Baier, R. Schmogrow, W. Bogaerts, S. K. Selvaraja, G. Lepage, M. Pantouvaki, J. M. D. Wouters, P. Verheyen, J. Van Campenhout, B. Chen, R. Baets, P. Absil, R.

Dinu, C. Koos, W. Freude, and J. Leuthold, “Silicon-organic hybrid (SOH) IQ modulator using the linear electro-optic effect for transmitting 16QAM at 112 Gbit/s.,” *Optics express*, vol. 21. pp. 13219–27, 2013.

[105] L. Alloatti, D. Korn, R. Palmer, D. Hillerkuss, J. Li, A. Barklund, R. Dinu, M. Fournier, J. Fedeli, H. Yu, W. Bogaerts, P. Dumon, and R. Baets, “42.7 Gnit/s electro-optic modulator in silicon technology,” *Opt. Express*, vol. 19, pp. 11841–11851, 2011.

[106] C. Xiong, W. H. P. Pernice, and H. X. Tang, “Low-loss, silicon integrated, aluminum nitride photonic circuits and their use for electro-optic signal processing.,” *Nano Lett.*, vol. 12, pp. 3562–8, 2012.

[107] P. Poberaj, G., Hu, H., Sohler, W. and Günter, “Lithium niobate on insulator (LNOI) for micro-photonic devices,” *Laser Photon. Rev.*, vol. 6, no. 4, pp. 488–503, 2012.

[108] S. Darmawan, L. Y. M. Tobing, and T. Mei, “Coupling-induced phase shift in a microring-coupled Mach-Zehnder interferometer.,” *Opt. Lett.*, vol. 35, pp. 238–240, 2010.

[109] Y. S. Lee, G.-D. Kim, W.-J. Kim, S.-S. Lee, W.-G. Lee, and W. H. Steier, “Hybrid Si-$LiNbO_3$ microring electro-optically tunable resonators for active photonic devices.,” *Opt. Lett.*, vol. 36, pp. 1119–1121, 2011.

[110] H. H. H. Hu, R. R. R. Ricken, W. S. W. Sohler, and R. B. W. R. B. Wehrspohn, “Lithium Niobate Ridge Waveguides Fabricated by Wet Etching,” *IEEE Photonics Technol. Lett.*, vol. 19, 2007.

[111] H. Lu, F. Issam Baida, G. Ulliac, N. Courjal, M. Collet, and M.-P. Bernal, “Lithium niobate photonic crystal wire cavity: Realization of a compact electro-optically tunable filter,” *Appl. Phys. Lett.*, vol. 101, p. 151117, 2012.

[112] M. E. Solmaz, D. B. Adams, W. C. Tan, W. T. Snider, and C. K. Madsen, “Vertically integrated As2S3 ring resonator on LiNbO3.,” *Opt. Lett.*, vol. 34, pp. 1735–1737, 2009.

[113] L. Chen and R. M. Reano, “Compact electric field sensors based on indirect bonding of lithium niobate to silicon microrings,” *Optics Express*, vol. 20. p. 4032, 2012.

[114] L. Chen, M. G. Wood, and R. M. Reano, “12.5 pm/V hybrid silicon and lithium niobate optical microring resonator with integrated electrodes.,” *Opt. Express*, vol. 21, pp. 27003–10, 2013.

[115] K. Narayanan and S. F. Preble, “Optical nonlinearities in hydrogenated-amorphous silicon waveguides.,” *Opt. Express*, vol. 18, pp. 8998–9005, 2010.

[116] L. Cao, A. A. Aboketaf, and S. F. Preble, “CMOS compatible micro-oven heater for efficient thermal control of silicon photonic devices,” *Opt. Commun.*, vol. 305, pp. 66–70, 2013.

[117] D. Janner, D. Tulli, M. Belmonte, and V. Pruneri, “Waveguide electro-optic modulation in micro-engineered LiNbO 3,” *J. Opt. A Pure Appl. Opt.*, vol. 10, p. 104003, 2008.

[118] H.-Y. Ng, M. R. Wang, D. Li, X. Wang, J. Martinez, R. R. Panepucci, and K. Pathak, “1<formula formulatype=‘inline’> <img src=‘/images/tex/353.gif’ alt=‘,\times,’> </formula>4 Wavelength Reconfigurable Photonic Switch Using Thermally Tuned Microring Resonators Fabricated on Silicon Substrate,” *IEEE Photonics Technol. Lett.*, vol. 19, 2007.

[119] P. Dong, W. Qian, H. Liang, R. Shafiiha, N.-N. Feng, D. Feng, X. Zheng, A. V Krishnamoorthy, and M. Asghari, “Low power and compact reconfigurable multiplexing devices based on silicon microring resonators.,” *Opt. Express*, vol. 18, pp. 9852–9858, 2010.

[120] M. R. Watts, W. A. Zortman, D. C. Trotter, G. N. Nielson, D. L. Luck, and R. W. Young, “Adiabatic Resonant Microrings (ARMs) with directly integrated thermal microphotonics,” *2009 Conf. Lasers Electro-Optics 2009 Conf. Quantum Electron. Laser Sci. Conf.*, 2009.

[121] V. R. Almeida, C. A. Barrios, R. R. Panepucci, and M. Lipson, “All-optical control of light on a silicon chip.,” *Nature*, vol. 431, pp. 1081–1084, 2004.

[122] T. Tanabe, M. Notomi, S. Mitsugi, A. Shinya, and E. Kuramochi, "All-optical switches on a silicon chip realized using photonic crystal nanocavities," *Appl. Phys. Lett.*, vol. 87, p. 151112, 2005.

[123] A. Politi, M. J. Cryan, J. G. Rarity, S. Yu, and J. L. O'Brien, "Silica-on-silicon waveguide quantum circuits.," *Science*, vol. 320, pp. 646–649, 2008.

[124] B. Julsgaard, J. Sherson, J. I. Cirac, J. Fiurášek, and E. S. Polzik, "Experimental demonstration of quantum memory for light.," *Nature*, vol. 432, pp. 482–486, 2004.

[125] N. Stefanou and A. Modinos, "Impurity bands in photonic insulators," *Physical Review B*, vol. 57. pp. 12127–12133, 1998.

[126] A. Yariv, Y. Xu, R. K. Lee, and A. Scherer, "Coupled-resonator optical waveguide: a proposal and analysis.," *Opt. Lett.*, vol. 24, pp. 711–713, 1999.

[127] F. Xia, L. Sekaric, M. O'Boyle, and Y. Vlasov, "Coupled resonator optical waveguides based on silicon-on-insulator photonic wires," *Appl. Phys. Lett.*, vol. 89, p. 041122, 2006.

[128] Q. Xu, P. Dong, and M. Lipson, "Breaking the delay-bandwidth limit in a photonic structure," *Nature Physics*, vol. 3. pp. 406–410, 2007.

[129] A. W. Elshaari, A. Aboketaf, and S. F. Preble, "Controlled storage of light in silicon cavities.," *Opt. Express*, vol. 18, pp. 3014–3022, 2010.

[130] C. Manolatou, M. J. Khan, S. Fan, P. R. Villeneuve, H. A. Haus, and J. D. Joannopoulos, "Coupling of modes analysis of resonant channel add-drop filters," *IEEE J. Quantum Electron.*, vol. 35, 1999.

[131] R. G. Hunsperger, "Integrated Optics," *Appl. Opt.*, vol. 7, pp. 399–457, 2009.

[132] D. Adams, G. Madejski, and S. Preble, "High-Q shallow etch silicon micro resonators for optical delay," in *IEEE Photonic Society 24th Annual Meeting*, 2011, vol. 2, pp. 871–872.

[133] A. Shacham, K. Bergman, and L. P. Carloni, "On the Design of a Photonic Network-on-Chip," *First Int. Symp. Networks-on-Chip*, 2007.

[134] B. A. Small, B. G. Lee, K. Bergman, Q. Xu, and M. Lipson, "Multiple-wavelength integrated photonic networks based on microring resonator devices," *Journal of Optical Networking*, vol. 6. p. 112, 2007.

[135] P. W. SMITH, "A digital optical switch," *Optics News*, vol. 13. p. 33, 1987.

[136] W. Y. W. Yuan, S. K. S. Kim, W. H. Steier, and H. R. Fetterman, "Electrooptic polymeric digital optical switches (DOSs) with adiabatic couplers," *IEEE Photonics Technol. Lett.*, vol. 17, 2005.

[137] S. J. Spector, M. W. Geis, G.-R. Zhou, M. E. Grein, F. Gan, M. A. Popovic, J. U. Yoon, D. M. Lennon, E. P. Ippen, F. Z. Kärtner, and T. M. Lyszczarz, "CMOS-compatible dual-output silicon modulator for analog signal processing.," *Opt. Express*, vol. 16, pp. 11027–11031, 2008.

[138] T. A. Ramadan, R. Scarmozzino, and R. M. . J. Osgood, "Adiabatic couplers: design rules and optimization," *J. Light. Technol.*, vol. 16, 1998.

[139] L. Cao, A. Elshaari, A. Aboketaf, and S. Preble, "Adiabatic couplers in SOI waveguides," *Lasers Electro-Optics Quantum Electron. Laser Sci. Conf. (QELS), 2010 Conf.*, 2010.

[140] N. Sherwood-Droz, H. Wang, L. Chen, B. G. Lee, A. Biberman, K. Bergman, and M. Lipson, "Optical 4x4 hitless Silicon router for optical Networks-on-Chip (NoC): erratum.," *Opt. Express*, vol. 16, p. 19395, 2008.

[141] L. Olislager, J. Cussey, A. Nguyen, P. Emplit, S. Massar, J.-M. Merolla, and K. Huy, "Frequency-bin entangled photons," *Physical Review A*, vol. 82. 2010.

[142] K. Yoshino, M. Fujiwara, A. Tanaka, S. Takahashi, Y. Nambu, A. Tomita, S. Miki, T. Yamashita, Z. Wang, M. Sasaki, and A. Tajima, "High-speed wavelength-division multiplexing quantum key distribution system," *Optics Letters*, vol. 37. p. 223, 2012.

[143] D. Englund, A. Majumdar, A. Faraon, M. Toishi, N. Stoltz, P. Petroff, and J. Vucković, “Resonant excitation of a quantum dot strongly coupled to a photonic crystal nanocavity.,” *Phys. Rev. Lett.*, vol. 104, p. 073904, 2010.

[144] M. Notomi and S. Mitsugi, “Wavelength conversion via dynamic refractive index tuning of a cavity,” *Physical Review A*, vol. 73. 2006.

[145] H. J. McGuinness, M. G. Raymer, C. J. McKinstrie, and S. Radic, “Quantum frequency translation of single-photon states in a photonic crystal fiber.,” *Phys. Rev. Lett.*, vol. 105, p. 093604, 2010.

[146] S. F. P. Edwin E Hach III, Ali W Elshaari, “Fully quantum-mechanical dynamic analysis of single-photon transport in a single-mode waveguide coupled to a traveling-wave resonator,” *Phys. Rev. A*, vol. 82, no. 6, p. 063839, 2010.

[147] S. F. Preble, Q. Xu, and M. Lipson, “Changing the colour of light in a silicon resonator,” *Nature Photonics*, vol. 1. pp. 293–296, 2007.

[148] T. Tanabe, E. Kuramochi, H. Taniyama, and M. Notomi, “Electro-optic adiabatic wavelength shifting and Q switching demonstrated using a p-i-n integrated photonic crystal nanocavity.,” *Opt. Lett.*, vol. 35, pp. 3895–3897, 2010.

[149] M. Notomi, H. Taniyama, S. Mitsugi, and E. Kuramochi, “Optomechanical Wavelength and Energy Conversion in High-Q Double-Layer Cavities of Photonic Crystal Slabs,” *Physical Review Letters*, vol. 97. 2006.

[150] S. Preble, L. Cao, A. Elshaari, A. Aboketaf, and D. Adams, “Single photon adiabatic wavelength conversion,” *Appl. Phys. Lett.*, vol. 101, p. 171110, 2012.