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Gate-to-Channel Parasitic Capacitance Minimization and Source-Drain Leakage Evaluation in Germanium PMOS

By

Raymond T. Krom III

A Thesis Submitted

in Partial Fulfillment

of the Requirements for the Degree of

Master of Science

in

Microelectronic Engineering

Approved by:

Prof. _____
Dr. Santosh K. Kurinec (Thesis Advisor)

Prof. _____
Dr. Sean L. Rommel (Committee Member)

Prof. _____
Dr. James E. Moon (Committee Member)

Jerome M. Mitard (IMEC Collaborator)
Dr. Marc Heyns (IMEC Collaborator)
Dr. Marc Meuris (IMEC Collaborator)

DEPARTMENT OF MICROELECTRONIC ENGINEERING

KATE GLEASON COLLEGE OF ENGINEERING

ROCHESTER INSTITUTE OF TECHNOLOGY

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Abstract

This work studies the behavior of both gate-to-channel capacitance (C_{GC}) and source-channel-drain/well leakage in metal-gate/high- κ /Ge PMOS technology ($W = 10 \mu\text{m}$ and $L = 10; 5; 1 \mu\text{m}$) under development at IMEC. The hole drift-mobility of germanium is $\sim 4X$ that of silicon, leading researchers to evaluate germanium as a possible channel material replacement for PMOS expected at the 32 nm technology node. In particular this study focuses on—but is not restricted to—(1) the presence of a parasitic gate-to-channel capacitance (C_{GC}), the large non-ideal trap assisted conductance which contributes to it, and its function versus Ge-PMOS architecture and gate length; (2) the existence of C - V tool compensation error due to C_{GC} measurement technique resulting in conductance measurement error; (3) the presence of large source-channel-drain/well leakages characterized using a new MOS gated-diode measurement technique; (4) extrinsic capacitance (C_{EXT}), flatband voltage (V_{FB}), and effective oxide thickness (EOT) parameter extraction with discussion on inversion layer quantization.

This study found that excessive current leakages from the Ge-PMOS source-and-drain into the channel led to a chuck-dependent parasitic capacitance during C_{GC} measurement. This excessive leakage is identified as a trap-assisted leakage through both AC and DC analysis. The chuck-dependent parasitic capacitance was an unexpected side effect of the PMOS architecture: namely the lack of N-Well isolation. The parasitic capacitance—dependent on both applied bias and frequency—was separated into two main capacitive components: a frequency-dependent source/well and drain/well trap-assisted leakage capacitance (C_{Para_SD}) and a frequency-voltage-dependent gate-induced

junction leakage capacitance (C_{Para_GIII}). A third parasitic capacitance due to interface trap (IT) contribution (C_{IT}) during channel depletion was also identified.

This study also found that the new MOS gated-diode measurement technique designed to separate and evaluate the source, channel, and drain leakage components is superior to typical V_{GS} versus I_{DS} methods when attempting to quantify the C_{GC} measurement. The MOS gated-diode configuration allowed for temperature-dependent analysis and activation energy extraction (E_A), thereby providing a means to confirm individual leakage components: diffusion; Shockley-Read-Hall (SRH); trap-assisted leakage (TAL). TAL components include: Poole-Frenkel (PF); phonon-assisted tunneling (PAT); trap-to-band tunneling (TBT).

In conclusion, it was found that the source-channel-drain/well leakages and hence parasitic capacitances of PMOS built on relaxed germanium-on-silicon can be minimized by reducing the source/drain area, reducing the source/drain-to-gate contact distance, while increasing both the gate length and measurement frequency. The dominance of SRH and TAL during Ge-PMOS operation disagrees with diffusion dominance predicted by theory and as a result opens the door for future research. Future research includes Ge-PMOS fabrication on substrates free of dislocations—to minimize SRH and TAL current leakage contributions—so as to compare leakage performance.

*“The solution is not to be found in the result achieved, but
in the way of achieving it.”*

-André Bazin

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IMEC is a world-leading independent research center addressing the next generation of processes, chips, and systems utilized in nanoelectronics and nanotechnology areas. Housing state-of-the-art 300 mm and 200 mm clean rooms extended in 2006 for electrical characterization, IMEC is evaluating Ge—among other materials—as a channel replacement material for PMOSFET and other advanced technologies expected at the 32 nm technology node. Research at IMEC provided the author with a great degree of resources, flexibility, and creative freedom. The author is extremely grateful to this research center, its employees, faculty, and vision.

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List of Symbols and Abbreviations

<u>Symbol</u>	<u>Unit</u>	<u>Description</u>
A	μm^2	Gate area
ALD	-	Atomic layer deposition
ω	rad/s	Angular frequency ($2\pi f$)
B	S	Susceptance
BF_2	-	Boron difluoride
BTBT	-	Band-to-band tunneling
C_{EXT}	F	Extrinsic capacitance
C_{GC}	F	Gate-to-channel capacitance
C_{GCO}	F	Intrinsic capacitance
C_{IF}	F	Inner fringing field capacitance
C_{IT}	F	Interface trap capacitance
C_M	F	Measured capacitance
C_{MAT}	F	Material capacitance
CMOS	-	Complementary metal oxide semiconductor
C_O	F	Outer capacitance
C_{OF}	F	Outer fringing field capacitance
C_{OV}	F	Overlap capacitance
C_P	F	Parallel capacitance
C_{Para}	F	Parasitic capacitance
C_{Para_SD}	F	Source/well drain/well leakage parasitic capacitance
C_{Para_GJL}	F	Gate-induced junction leakage parasitic capacitance
C_S	F	Substrate capacitance

C_{TOP}	F	Top capacitance
D_{IT}	$\text{cm}^{-2}\text{eV}^{-1}$	Interface trap density
DUT	-	Device under test
E	eV	Energy difference (trap state vs. conduction band)
ΔE	eV	Poole-Frenkel energy difference
E_A	eV	Activation energy
E_G	eV	Energy gap
ϵ_0	pF/m	Permittivity of free space (8.8542)
E_{max}	V/cm	Maximum electric field
E_T	eV	Interface trap level
EMI	-	Electromagnetic interference
EOT	nm	Effective oxide thickness
f	Hz	Frequency
G	S	Conductance/Susceptance
GIDL	-	Gate-induced drain leakage
GIJL	-	Gate-induced junction leakage
G_L	A	Photogenerated recombination-generation current
G_P	S	Parallel conductance
GPIB	-	General purpose interface bus
HDD	-	Highly doped drain
HfO ₂	-	Hafnium-oxide
HPC	-	High probe contacts
I_1	A	P/N junction reverse bias leakage
I_2	A	Subthreshold leakage
I_3	A	Gate-oxide tunneling leakage

I_4	A	Hot carrier substrate-to-gate injection
I_5	A	Gate-induced junction leakage
I_6	A	Punchthrough
I_7	A	Surface generation leakage in channel
I_{DS}	A	Drain-to-source current
IMEC	-	Interuniversitair Micro-Elektronica Centrum
I - V	A- V	Current voltage measurement
$J_{Drift-Diff}$	A/cm ²	Drift-diffusion current density
J_R	A/cm ²	Reverse-bias current density
J_{SRH}	A/cm ²	Shockley-Read-Hall current density
J_{SRH_Chan}	A/cm ²	Shockley-Read-Hall current density in channel
κ	eV/K	Boltzmann's constant (8.617x10 ⁻⁵)
K_{OX}	-	SiO ₂ dielectric relative permittivity
L	μm	Gate length
L_{EFF}	μm	Effective channel length
L_{MAT}	H	Material Inductance
LPC	-	Low probe contacts
ML	-	Monolayer
μ_{eff}	cm ² /Vs	Effective carrier mobility
MOSFET	-	Metal oxide semiconductor field effect transistor
N_A	cm ⁻³	Acceptor doping concentration
N_D	cm ⁻³	Donor doping concentration
n_i	cm ⁻³	Intrinsic carrier concentration
PAI	-	Pre-amorphization
PAT	-	Phonon-assisted tunneling

PF	-	Poole-Frenkel
PMOS	-	P-type metal oxide semiconductor
PMOSFET	-	P-type MOSFET
POR	-	Product of record
PVD	-	Physical vapor deposition
q	C	Elementary charge (1.602×10^{-19})
Q_i	-	Inversion charge
R	Ω	Resistance
RFI	-	Radiofrequency interference
R-G	-	Recombination-generation
R_P	Ω	Parallel resistance
R_S	Ω	Series resistance
SRH	-	Shockley-Read-Hall
SRH	-	Shockley-Read-Hall
T	K	Temperature
TAL	-	Trap-assisted leakage
TBT	-	Trap-to-band tunneling
T_{OX}	nm	SiO ₂ thickness
τ_{S/D_Trap}	s	Time-constant for source/well and drain/well traps
V_A	V	Applied bias
V_{bi}	V	Built-in potential
v_{sat}	cm/s	Saturation velocity
V_{FB}	V	Flatband voltage
V_G	V	Gate voltage
V_{GS}	V	Gate-to-source voltage

V_T	V	Channel threshold voltage
W	μm	Gate width
X	Ω	Reactance
Y	S	Admittance
Z	Ω	Impedance

Chapter 1

Introduction and Motivation

1. The 32 nm Technology Node and Germanium PMOS

Since the invention of the semiconducting transistor nearly 60 years ago, semiconducting technology has grown exponentially in both complexity and application. To date – and in no small way due to ingenious advancements in fabrication technology – semiconductors are utilized in nearly every aspect of daily life from telling the time to using a cell phone. Current research shows, however, that continued growth in this field will encounter many challenges beyond the 32 nm technology node expected between the years 2013 and 2015, the solutions to which will require the implementation of both new materials and advanced non-classical Complementary Metal Oxide Semiconductor (CMOS) capable of higher drive currents while at the same time minimizing current leakages and short channel effects [1-4].

At present most state-of-the-art facilities are capable of 65 nm production, with Intel being the world's first producer of 45 nm consumer technology [5]. Second to Intel is AMD currently deploying its 45 nm pilot line, expected to be available in the second-half of 2008 [6]. These state-of-the-art semiconducting technologies implement process and global induced strain engineering [5,6], high- κ metal gate stacks [5], and in some cases—as in the case of AMD's new 65 nm Barcelona processing technology—SiGe hybrid source/drain replacement [6]. The replacement of SiO₂ as the gate dielectric of choice in favor of high- κ dielectric stacks is a revolution in classical CMOS fabrication.

To meet device requirements at the 32 nm technology node while maintaining a foundation in silicon, renewed interest in silicon-compatible germanium p-type Field Effect Transistor (PFET) and III-V n-type FET (NFET) technologies has begun [1-7]. A device trend-projection by Intel is shown in Fig. 1.1. Note the advanced non-classical CMOS technologies currently in use and projected beyond 2008.

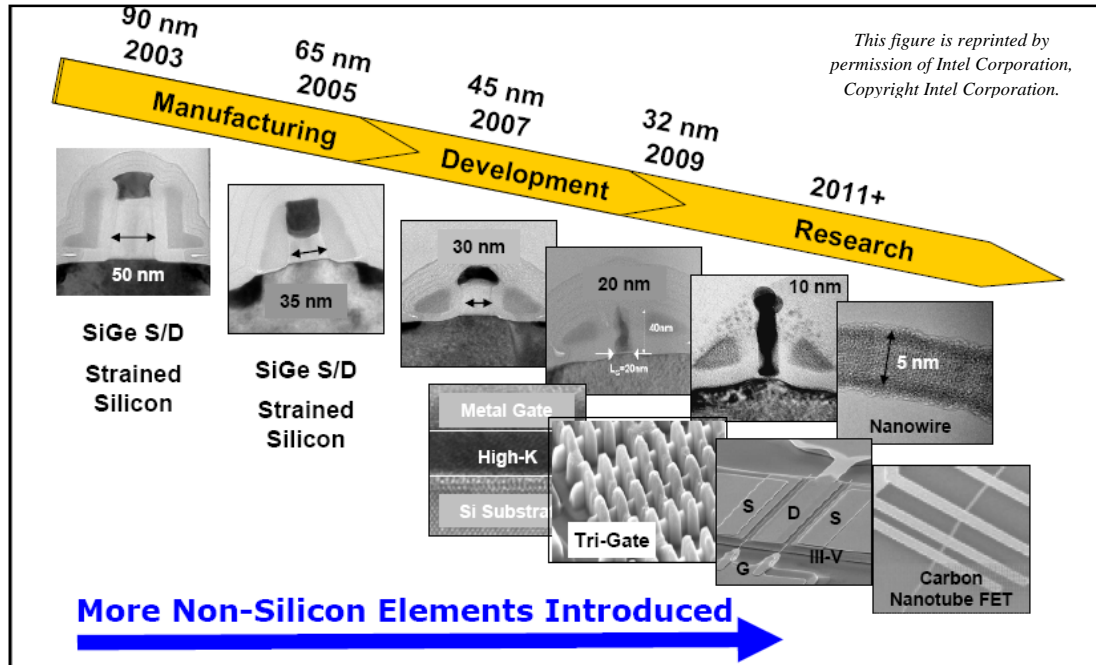


Fig. 1.1: Intel's 2006 device trend-projection adopted from Chau [4]. Note that Intel's research projection is more aggressive than that of the ITRS. Intel plans on researching the 32 nm technology node starting 2009 versus 2013 for ITRS [2].

Most important to such technology and the main focus of this study, are the methods used to characterize their electrical operation. This study focuses on IMEC's Ge-PMOSFET technology and reveals that one must quantify source-drain-channel leakage and its effect on Gate-to-Channel Capacitance (C_{GC}) before using C_{GC} to extract critical device parameters.

1.1. Silicon, Germanium, and III-V

As was briefly mentioned, researchers are interested in Ge and III-V materials for the next generations of semiconducting technology. Such materials provide an extra degree of freedom—mobility enhancement—in the manufacturing of complex semiconducting technologies. With such freedom come complexities such as characterization, fabrication, and integration of these advanced materials. This section discusses the pros of increased electron and hole mobility versus the cons of material density, cost, and the creation of threading dislocations due to lattice mismatch.

The focus of research on Ge and III-V materials resides in their increased hole and electron mobility, when compared to silicon. This is shown in Table 1.1.

Table 1.1: Si, Ge, and GaAs selected property comparison at 300K [1,8].			
	Si	Ge	GaAs
Mobility [cm^2/Vs]			
Electron (μ_n)	1,500	3900	8500
Holes (μ_p)	450	1900	340
Density [g/cm^3]	2.33	5.32	5.32
Bulk Cost in 2007 (approx.) [USD/kg]	2.05	800	460(Ga)2.30(As)
Cost for 2 μm Thick by 200 mm Diameter [USD]	-	0.27	0.15
Lattice Constant [\AA]	5.431	5.646	5.653
Energy Gap [eV]	1.12	0.67	1.42
Intrinsic Carrier Concentration (cm^{-3})	1.0×10^{10}	2.0×10^{13}	2.1×10^6

It is quite clear from Table 1.1, that a 322% hole mobility enhancement exists and a 467% electron mobility enhancement exists when changing the device material from Si to Ge and from Si to GaAs, respectively. Problems reside in the increased density, bulk cost, and creation of threading dislocations due to lattice mismatch of Ge and GaAs when compared to Si. Wafer handling systems of 200 mm and 300 mm tools are calibrated for Si. Both this calibration issue and the high cost of Ge and GaAs bulk materials indicate

that future technologies may not utilize 200 mm bulk Ge or GaAs substrates. Bulk Ge and GaAs are currently impractical from both a manufacturing and cost standpoint.

Researchers are developing solutions to the density, cost, and threading dislocation problems associated with these new materials. There are two main solutions in place: first, the deposition of germanium on silicon wafers and subsequent annealing of threading dislocations created due to the lattice mismatch between the two materials (referred to as relaxed germanium-on-silicon) [9] and second, the deposition of germanium and III-V in/on trenched-silicon-dioxide upon silicon wafers in which the dislocations formed are contained in oxide trenches, resulting in a device layer nearly free of dislocations (referred to as Aspect-Ratio-Trapping) [10, 11]. In both cases silicon is used as the mechanical stabilizer thereby allowing germanium and III-V processing on 200 mm and 300 mm silicon substrates. Since these mobility enhancers are used in the regions of interest only—namely as thin films within the channel regions of MOS technology—wafer handling and expense becomes less of an issue. Table 1.1 shows that 2 μm of Ge and GaAs on a 200 mm wafer yields a bulk material cost of 0.27 USD and 0.15 USD, respectively.

Due to these two solutions, the strength of silicon in the future may reside in its mechanical properties first and its naturally stable SiO_2 second. This was observed during this study in which the devices under test were Ge-PMOS fabricated through the use of a 200 mm silicon stabilizing substrate (the Ge PMOS gate interface was passivated using SiO_2/Si layers). Due to the trap-assisted leakage observed in this study and the known fact that dislocations generate recombination-generation (R-G) centers, this study also indicates that researchers may exploit Aspect-Ratio-Trapping technology more so in the

future so as to minimize threading dislocations, their effect on integration during fabrication, and their effect on both electrical performance and characterization.

1.2. Present Study: Relaxed Germanium-on-Silicon

The devices in this study were fabricated on IMEC's 200 mm silicon pilot line and were the Product of Record (POR) throughout this study. The fabrication details are summarized in Table 1.2 so as to provide background for the following chapters.

1.) Starting Wafers	~2 μm epitaxial undoped Germanium-on-Silicon			
	Diameter	200 mm		
	Orientation	<100>		
	Dislocations	$1 \times 10^7 \text{ cm}^{-2}$ and $1 \times 10^8 \text{ cm}^{-2}$		
2.) Well Implants (P^{31})	V_T Adjust	$1 \times 10^{12} \text{ cm}^{-2}$	90 keV	7° Tilt
	Shallow Well	$2.5 \times 10^{12} \text{ cm}^{-2}$	180 keV	7° Tilt
	Deep Well	$1 \times 10^{13} \text{ cm}^{-2}$	570 keV	7° Tilt
3.) Layer Anneal	600°C 5 min. N_2			
4.) Box Isolation	200 nm CVD SiO_2			
5.) Ge Gate Passivation	Epitaxial Si 6ML=0.8 nm partially oxidized			
6.) Gate Dielectric	4 nm ALD HfO_2			
7.) Gate Metal	10 nm PVD TaN			
	100 nm PVD TiN			
8.) Halos (P^{31})	60 keV $4 \times 10^{13} \text{ cm}^{-2}$ 25° Tilt			
9.) S/D Implant (BF_2)	Extensions	$8 \times 10^{14} \text{ cm}^{-2}$	11 keV	7° Tilt
10.) Spacer	90 nm wide Si_3N_4 with SiO_2 Liner			
11.) S/D Implant (Ge)	Pre-amorphization (PAI)		35 keV	
12.) S/D Implant (Boron)	HDD	$4 \times 10^{15} \text{ cm}^{-2}$	7.5 keV	7° Tilt
13.) Activation Anneal	500°C 5 min. N_2			
14.) Metallization	TiN/Ti/Al/TiN			
15.) Post Metal Anneal	350°C 20 min. H_2 anneal with cool down in H_2			

The device fabrication details discussed in this section are nearly identical and limited to the details published in the works of Nicholas *et al.* [7]. The small differences are insignificant when considering the electrical behavior of the large devices (10 μm , 5 μm , and 1 μm gate lengths with fixed gate width of 10 μm) in this study.

Fabrication started with 200 mm <100> Germanium-on-Silicon wafers obtained from ASM. A Ge threading dislocation density between $1 \times 10^7 \text{ cm}^{-2}$ and $1 \times 10^8 \text{ cm}^{-2}$ is typical of these substrates—as discussed in previous works [7,9]—and as such is assumed for the devices investigated in this study. This epitaxial Ge layer is undoped and approximately 2.0 μm thick [7,9].

The n-well is formed by implanting P^{31} through a 30 nm screening SiO_2 layer in three stages. The first stage consists of a threshold adjustment implant, followed by a shallow well implant, concluded with a deep well implant as shown in Table 1.2. The n-well is annealed at 600°C for 5 minutes in N_2 ambient. Note that the n-well is not counter-doped as is the case with most silicon CMOS technologies: this is important for device isolation and will be discussed in the electrical characterization chapters.

After n-well formation, a 200 nm SiO_2 Box Isolation—field oxide isolation—is formed by chemical vapor deposition (CVD) thereby defining the device active region. The surface of the active region is passivated with six monolayers (6ML) of epitaxially grown silicon ($\sim 0.8 \text{ nm}$ thick). The Si is partially oxidized with ozonated H_2O resulting in a final Si thickness of 0.6 nm and SiO_2 thickness of 0.4 nm [7]. After forming the SiO_2 layer it is immediately capped with 4 nm of HfO_2 [7] using an ASM Pulsar 2000 reactor [9] so as to prevent any further oxidation, which is followed by metal gate formation using physical vapor deposition (PVD) [7]. The metal gate consists of 10 nm of TaN capped by 100 nm of TiN [7]. One should note that active region passivation, Si partial oxidation, and HfO_2 deposition are done without removing the wafer from vacuum.

After defining the gate, halos are formed by implanted P^{31} so as to control short channel effects. The source/drain extensions are formed by implanting BF_2 and the spacers are formed to a width of 90 nm: they consist of Si_3N_4 surrounded by a SiO_2 liner [7] so as to dampen additional stresses as seen by the Ge surface. The highly doped drain is then formed by first preamorphizing the germanium surface through Ge implantation and following it with a boron implantation: implanting Ge roughens the source/drain surface thereby controlling the subsequent boron implant depth. The junctions are annealed at $500^\circ C$ for 5 minutes in N_2 .

Finally, the source drain regions are germanided through nickel deposition and anneal. Back end processing consists of a TiN/Ti/Al/Ti metal contact stack [7]. The devices are concluded with a final anneal at $350^\circ C$ for 20 minutes in N_2 [7]. The final schematic of the fabricated Ge PMOSFET tested in this study is shown in Fig. 1.2.

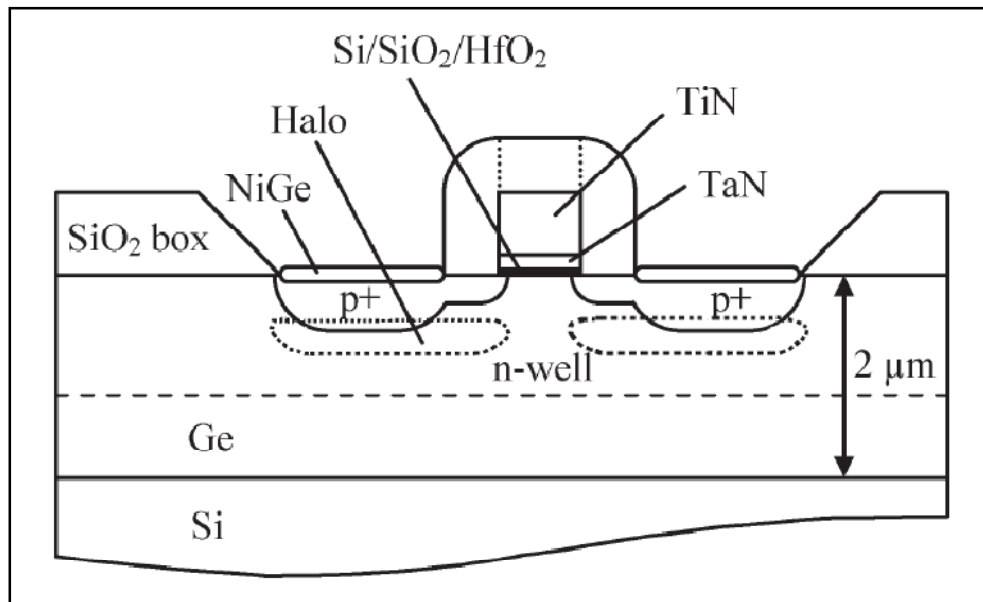


Fig. 1.2: Ge PMOSFET adopted from [7]. Note that backend metallization has been omitted.

According to the work of Nicholas *et al.* [7], the simulated doping concentrations for the Well; Halos; Extensions; HDD are approximately $5 \times 10^{17} \text{ cm}^{-3}$; $5 \times 10^{19} \text{ cm}^{-3}$; $5 \times 10^{20} \text{ cm}^{-3}$; $9 \times 10^{20} \text{ cm}^{-3}$, respectively [7]. For simulated doping concentration profiles the reader is referred to the work of Nicholas *et al.* [7].

1.2.1. Architecture Modules D1, G3, J2

Three architectures were evaluated when conducting this study; they are commonly referred to as D1, G3, and J2: all three have transistors containing $10 \mu\text{m}$ gate widths. All three architectures have the same source/drain contact and gate contact layout as shown in Fig. 1.3.

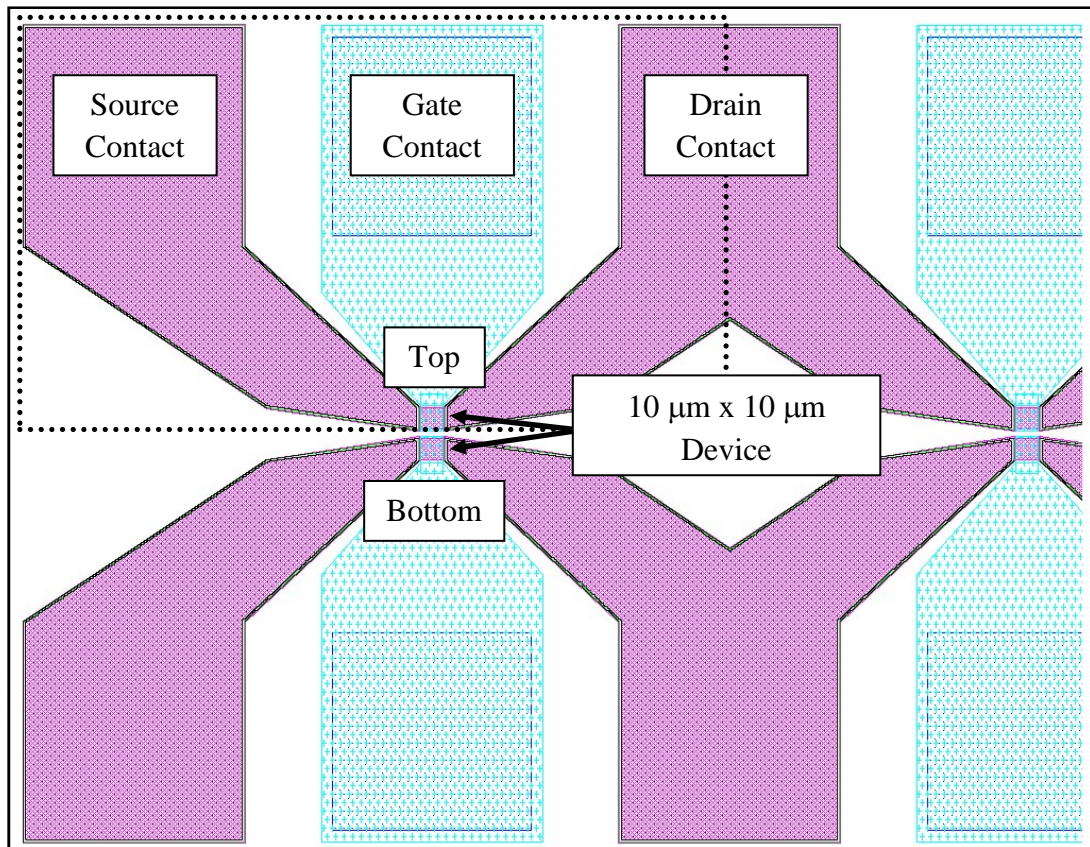


Fig. 1.3: $10 \mu\text{m} \times 10 \mu\text{m}$ ($L \times W$) Ge PMOS source/drain contact and gate contact layout. This layout is the same for D1, G3, and J2 architectures.

The device in the top of Fig. 1.3 is the same as the device in the bottom as noted. As one moves device-to-device from left to right the gate length decreases: 10 μm ; 5 μm ; 1 μm ; 0.8 μm ; etc. Note in Figure 1.3 that the drain contact for this 10 μm x 10 μm (L x W) Ge PMOS is also the source contact for the neighboring 5 μm x 10 μm (L x W) device. This is important when considering the reverse bias source and drain leakages. The 10 μm device has in essence one source and two drains, whereas the 5 μm ; 1 μm ; and 0.8 μm devices have two sources and two drains, indicating possible optimization for MOSFET leakage performance.

The differences between the three architectures are in their source/drain areas, source/drain contact areas, and distance of source/drain metal contact to gate. The differences are listed in Table 1.3. These differences played a significant role in the trap-assisted leakages as observed in the devices. This will be discussed in Chapter 5.

Arch	S/D Area [μm^2]	$S/D_{Contact}$ Area [μm^2]	$S/D_{Contact}$ to Gate Distance [μm]
D1	2.20×10^4	2.10×10^4	1.5
G3	74	43	3.0
J2	74	43	1.5

1.3 Statement of Problem and Thesis Contribution

The investigation presented in this study started in an attempt to identify the source(s) leading to an abnormal behavior in C_{GC} when measuring the devices described in Section 1.2. Specifically, this unknown behavior was observed as a parasitic capacitance during C_{GC} measurement dependent on both applied bias and frequency: this is shown in Fig. 1.4. Not only were the sources identified, but their effect minimized by

minimizing the Ge-PMOS source/drain area and gate to source/drain-contact distance, while maximizing both gate length and measurement frequency.

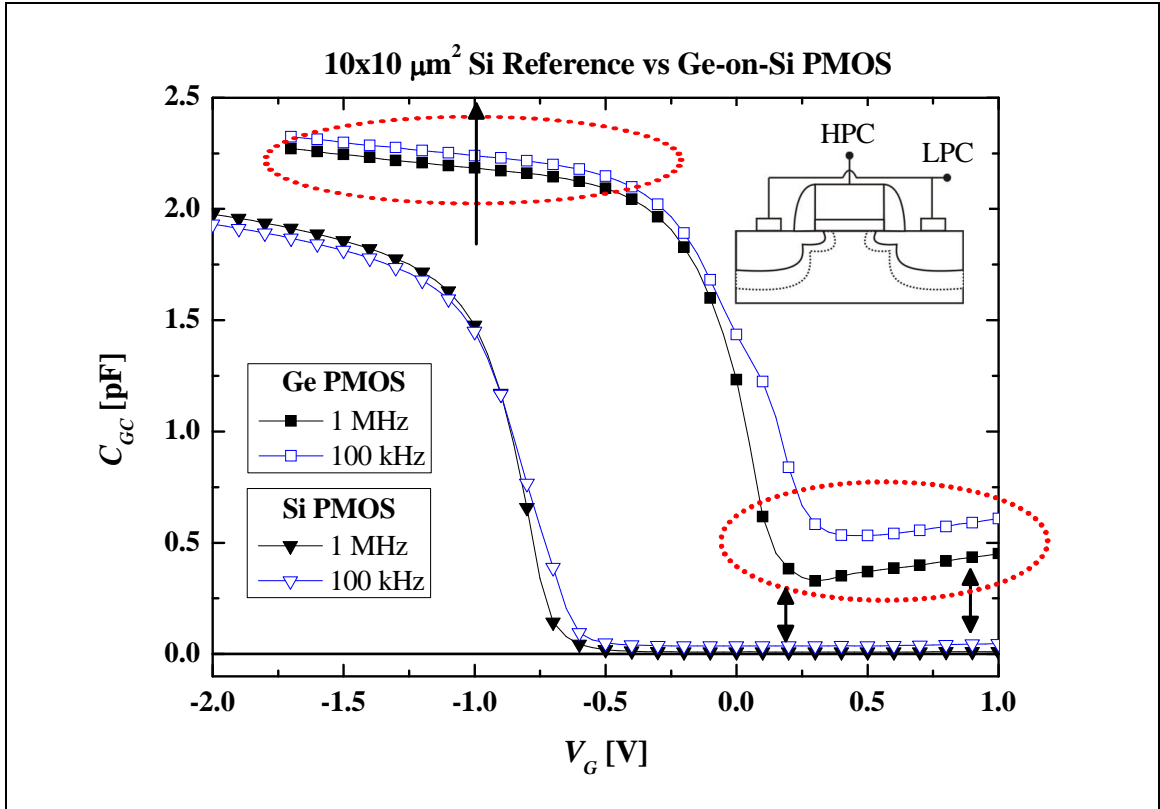


Fig. 1.4: Gate-to-Channel Capacitance (C_{GC}) for two $\sim 10 \mu\text{m} \times 10 \mu\text{m}$ pMOSFETs. Plot reveals a large voltage and frequency-dependent parasitic capacitance in channel-accumulation for the Germanium PMOS resulting in a positive shift in C_{GC} . This behavior is contrary to theory as shown by the Silicon PMOS. The source of this behavior was unknown prior to this study.

Fig. 1.4 shows the measurement of two PMOS technologies containing identical TiN/TaN/HfO₂/SiO₂/Si gate stacks as outlined in Section 1.2. The Si-PMOS technology behaves as predicted whereas the Ge-PMOS technology has a large voltage and frequency-dependent parasitic capacitance resulting in a vertical shift of the C_{GC} curve. This raises concern in Ge-PMOS C_{GC} values obtained in high channel-inversion, such as those used to evaluate effective oxide thickness (EOT) and in Ge-PMOS C_{GC} values obtained in high channel-accumulation, such as those used to quantify overlap

capacitance (C_{OV}). Prior to this study the parasitic capacitance was removed mathematically at each frequency by subtracting the minimum parasitic capacitance observed in accumulation at that frequency from the entire C_{GC} curve of that frequency. This provided questionable EOT results and no C_{OV} information (mathematical subtraction results in a $C_{OV} = 0.0$ F) as observed in Chapter 6.

Initially, during $C-V$ analysis reliable conductance information could not be obtained. In all cases conductance was negative. To determine the Ge-PMOS leakage a new DC measurement technique was created and called a MOS-Gated-Diode measurement. The configuration of this measurement—designed to be similar to the C_{GC} configuration as shown in the inset of Fig. 1.4—shorts the Ge-PMOS source to the drain and reverse biases them to the well, while sweeping the gate. This allowed leakage mechanism evaluation and temperature-dependent analysis. It was found that leakage was architecture-dependent: in terms of reverse bias leakage magnitude (I_R): $I_{R_D1} > I_{R_G3} > I_{R_J2}$.

Using the best device (J2 architecture $10\ \mu\text{m} \times 10\ \mu\text{m}$ device), activation energy extraction at each V_G of the MOS-gated-diode measurement indicated which leakage components were contributing throughout the C_{GC} measurement. When analyzing the J2 architecture, results show that a significant amount of trap-assisted leakage (TAL) and gate-induced-junction leakage (GIJL) existed at source/drain-to-well reverse biases as low as 10 mV. Results also reinforced why conductance information had initially not been obtained.

Obtaining reliable conductance information required the learning of two lessons: first, that the parasitic capacitance was chuck-dependent because there was no counter-

doped well technology and second, that grounding the substrate resulted in conductance measurement error. The MOS-gated-diode measurement led the investigator to the cause of the conductance measurement error. This study reveals that for obtaining reliable conductance information the Ge-PMOS substrate must not be grounded during C_{GC} measurement. It was found that grounding the substrate during AC analysis induced a compensation error in the C - V unit during measurement which remained—for at minimum three re-compensations—thereafter. In extreme cases the capacitance would shift to negative values.

This study links the trap-assisted and gate-induced-junction leakage mechanisms observed during DC analysis to trap-assisted and gate-induced-junction conductance observed during AC analysis. As a result the parasitic capacitance is broken into two main components: a frequency-dependent source/well and drain/well trap-assisted leakage (TAL) capacitance (C_{Para_SD}) and a frequency-voltage dependent gate-induced-junction leakage capacitance (C_{Para_GJL}). A third component due to channel depletion and generation by traps is also identified (C_{IT}). TAL was identified as a major leakage component instead of Shockley-Read-Hall (SRH), because the activation energy extracted during DC analysis was less than half the bandgap of Ge (bandgap of Ge is 0.66 eV).

Furthermore, the Conductance Method—first proposed by Nicollian and Goetzberger in 1967 for use with capacitors but related to the C_{GC} measurement of this study—was used, revealing a Gaussian distribution in conductance versus frequency attributed to trap-conductance. This trap-conductance is found to be geometry and gate-length dependent. Specifically, data suggest that traps are slower for J2 architecture

10 μm x 10 μm devices and become faster for smaller gate lengths throughout all architectures. The trend in trap frequency response also corresponds to the DC leakage evaluation performed.

1.4. Organization of Thesis

This thesis is broken down into seven chapters so as to better communicate the study. Chapter 1 is an introduction and motivation section discussing why researchers are interested in Germanium and III-V semiconducting technology and what this technology actually entails. Chapter 2 describes the PMOS C_{GC} measurement setup used in this study, what equipment was used and why it was configured in the manner it was. This chapter also discusses the parallel model assumption, the role of the high probes, the role of the low probes, the C_{GC} regions of operation, and ideal C_{GC} behavior. The experimental data in Chapter 2 is normalized so as to explain C_{GC} and support the C_{GC} results presented in Chapter 3.

In Chapter 3 the C_{GC} results are presented for the Ge PMOS devices described in Section 1.2 of Chapter 1. The frequency dependence of C_{GC} and conductance are discussed. The capacitance and conductance of architectures D1, G3, and J2 are measured for 10 μm ; 5 μm ; 1 μm gate lengths showing the parasitic capacitance behavior as a function of both architecture and gate length. The Gaussian distribution of conductance versus frequency reveals trap-assisted leakage behavior. Finally, the parasitic capacitance is minimized using J2 architecture with 10 μm gate length. Chapter 4 discusses C - V tool compensation error due to measurement technique: grounding the Ge substrate during C_{GC} measurement.

Chapter 5 begins by discussing the typical leakage components—diffusion, generation/trap-assisted, and gate-induced junction leakage—observed in reverse-biased p/n junctions so as to discuss the MOS-Gated-Diode Measurement used in this study. In Chapter 5 the source/drain to well leakage components are compared between architecture modules and identified on the J2 Module through activation energy extraction of the MOS-Gated-Diode measurement.

Chapter 6 extracts the extrinsic and intrinsic capacitances (C_{EXT}) and (C_{GCO}), respectively. A new definition for C_{EXT} is developed in considering the effect of C_{Para_SD} , C_{Para_GJL} , and C_{IT} . This definition relies on proper determination of V_{FB} . From C_{GCO} the inversion capacitance is determined and the effective oxide thickness (EOT) extracted. This EOT is compared to theoretical. The results do not match. The discrepancy is explained through inversion layer quantization and compared to results published in research. Finally, Chapter 7 is the conclusion of this work in which results are briefly revisited along with a discussion of the future work needed to identify and further minimize the source of the traps in this Ge-PMOS technology.

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Chapter 2

PMOS Gate-to-Channel Capacitance (C_{GC})

Equipment/Measurement

The goal of this chapter is to describe the C - V equipment configuration used in this study, the C - V measurement setup used in this study, and the ideal behavior of PMOS Gate-to-Channel Capacitance (C_{GC}) so as to provide background for the deviation in Ge-PMOS C_{GC} behavior observed and discussed in the next chapter. During this study three equipment configurations were briefly evaluated as shown in Table 2.1. Configuration-3 was found to be the best due to both its open compensation (correcting for stray admittance due to the test fixture) and short compensation (correcting for stray impedance due to the test fixture) capabilities [1]. The Keithley K4200 in Configuration-1 and Configuration-2 allowed for open compensation only. As a result, all C_{GC} measurements presented in this study were performed using Configuration-3.

Table 2.1: The three equipment configurations available to measure C_{GC} .			
Configuration	Probe Station	C - V Meter	C - V Control and Data Acquisition
1	Cascade Microtech Manual Microchamber	Agilent 4284A 20 hz-1 MHz Precision LCR (Agilent 4284A)	Keithley K4200 through General Purpose Interface Bus (GPIB)
2	SUSS MicroTec PA300PS	Agilent 4284A	Keithley K4200 through GPIB
3	SUSS MicroTec PA300PS	Agilent 4284A	Unix System through GPIB

Besides the compensation capabilities of Configuration-3 in Table 2.1, it was found that the lack of a switching matrix—utilized in both Keithley setups—provided a system with less Unknown Terminal to DUT separation. This meant less cable length resulting in better cable calibration. Lastly, the Keithley C_{GC} measurement program of Configuration-1 and Configuration-2 grounded the Ge-PMOS substrate resulting in $C-V$ Meter compensation error. This will be described in more detail in Chapter 4. Configuration-3 did not ground the Ge-PMOS substrate. As a result, Configuration-3 will be the only configuration discussed in this chapter.

2.1. $C-V$ Equipment and Configuration

The Suss MicroTec PA300PS probe station used in Configuration-3 of this study and shown in Fig. 2.1 is a semi-automatic device characterization tool [2]. Consisting of a Semiautomatic Wafer Controller, iVista Microscope, Probe Shield Technology, and PH110 SUSS Microtec Micromanipulators, this station is capable of accurately analyzing devices located on single chips or on wafers as large as 300 mm in diameter.

The Semiautomatic Wafer Controller of the PA300PS allows for both easy movement die-to-die and probe lift/drop during measurement (provided the height and location of the probe tips inside the probe shield housing are set correctly to minimize contact scratching). This allows one to map the die performance of an entire wafer. The iVista Microscope allows one to zoom in on the contacts vertically and view them laterally thereby ensuring connection between the probe tip and device contact. The Probe Shield Technology provides an environment free from both electromagnetic interference (EMI) and radiofrequency interference (RFI) [1, 2], thereby removing the

requirement from an expensive EMI/RFI shielded room. Shielding is extremely important when performing precise noise-free $C-V$ analysis.

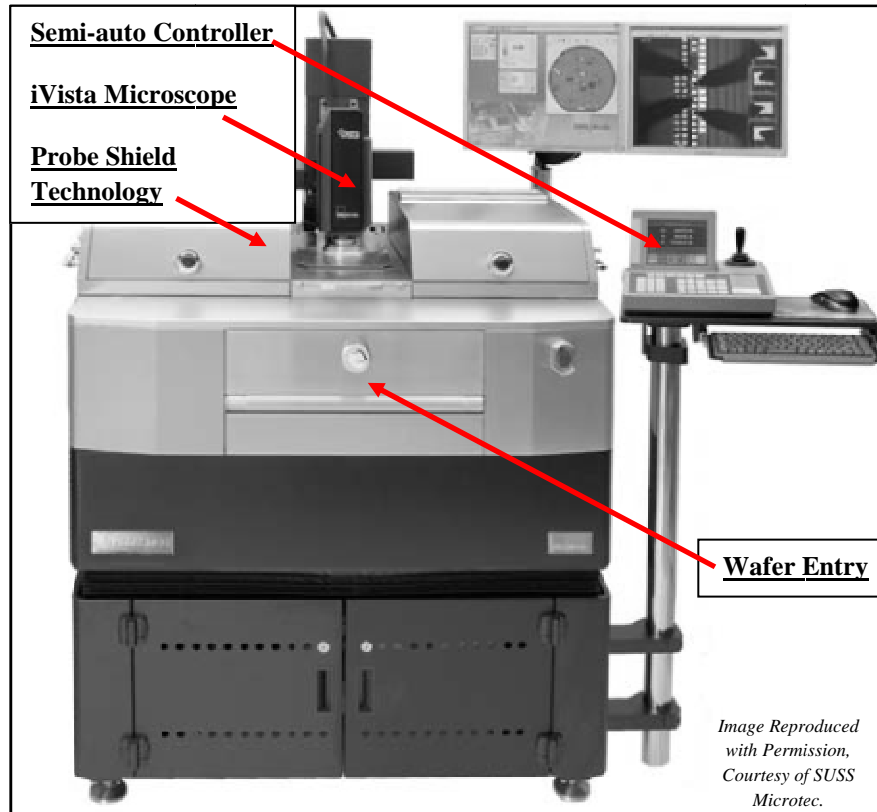


Fig. 2.1: A SUSS Microtec. semiautomatic probe station PA300PS adopted from [2].

Aside from the features above, the Probe Station floats on hydraulic feet, thereby protecting the wafer and probe tips from minor vibrations, such as in those caused by the slamming of a door, making it perfect for time-dependent electrical analysis. A chuck heater and chiller are attached to the station, allowing temperature-dependent measurements. Finally, the wafer handling system is designed for wafer fragility [2] making it perfect for Germanium and III-V devices.

The C-V Meter used in this study consists of an Agilent 4284A 20Hz-1MHz Precision LCR Meter—shown in Fig. 2.2—controlled by a Unix Computer System through a General Purpose Interface Bus (GPIB).

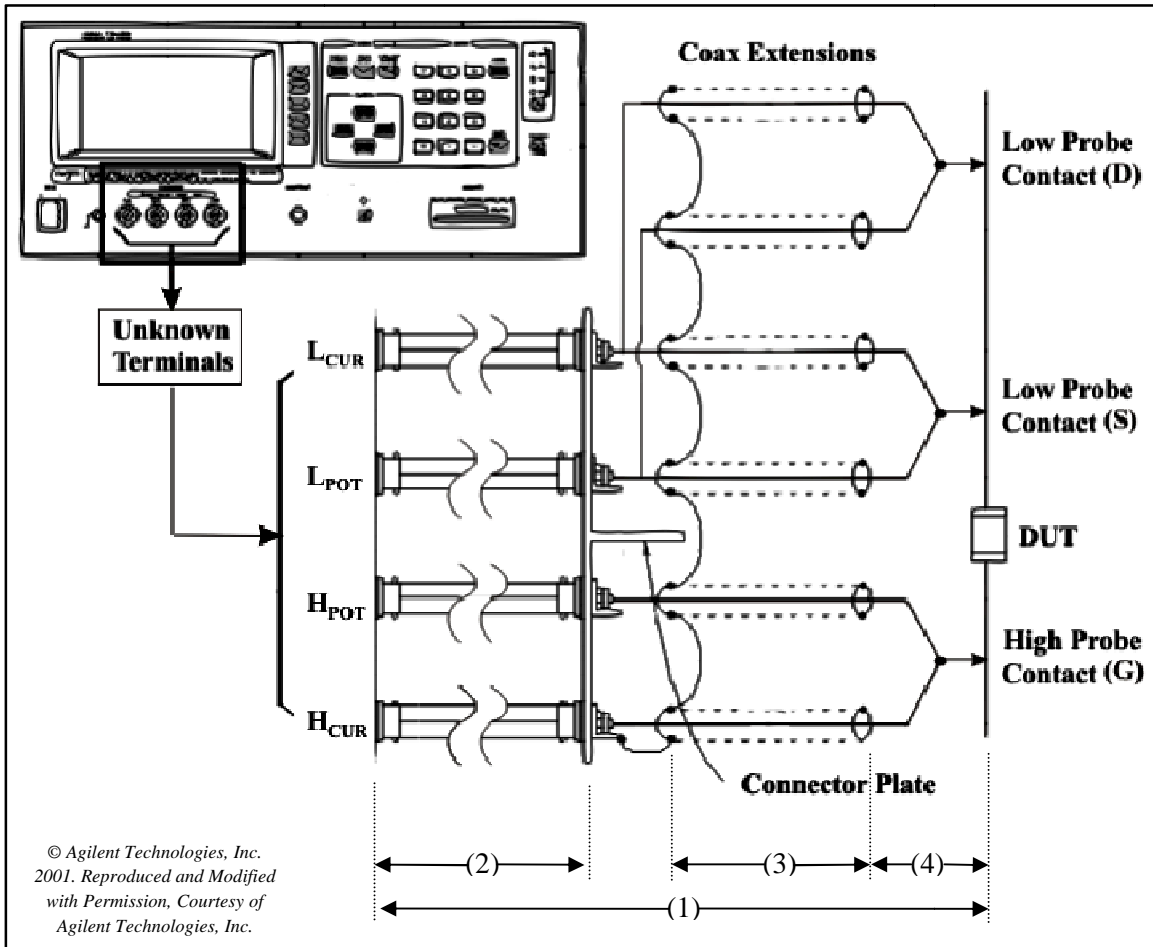


Fig. 2.2: Front Panel of the Agilent 4284A 20 Hz – 1 MHz Precision LCR Meter adapted from [3] showing location of the Unknown Terminals and their connection/configuration with the Connector Plate through the Coax Cable Extensions. The total cable length (1) is composed of the triax cable extensions (2), in connection with the coax cable extensions (3) and the probe tips (4). The cable lengths are not to scale. The cable length between (2-3) is exaggerated here for illustration only.

The configuration of the HP-4284A Unknown Terminals with respect to the probe tips is perhaps the most important aspect of the C-V equipment configuration when considering measurement accuracy at low and high frequencies. This is due to the need for software

calibration of cable length and compensation of stray admittances and impedances due to the testing fixture.

In general the following conditions are sought and labeled in Fig. 2.2 appropriately. The signal path between the 4284A and the probe tips (1) should be as short as possible; High Current (H_{CUR}), High Potential (H_{POT}), Low Potential (L_{POT}), and Low Current (L_{CUR}) coax extension cables (2) should be as short as possible and they should be connected as close as possible to the DUT (3+4); the distance between the DUT and the shields of the coax extension cables (4) should be as short as possible [3]. Following these four conditions minimizes the cable length calibration required. This minimizes stray capacitive, inductive, and resistive components existing between the Unknown Terminals and the probe tips thereby allowing for more accurate open/short compensation. By obtaining better parasitic admittance/impedance compensation, one may obtain an effective capacitance value as close as possible to the true theoretical value of the DUT.

The terminal configuration shown in Fig. 2.2 is close to one known as a 5-Terminal Pair Configuration used in typical frequency measurement ranges of 10 mHz – 100 MHz [1], but different in the fact that, first, it contains two Low Probe Contacts (labeled S and D) and, secondly, it does not contain shield shorting at the end of the coax cables near the DUT (4). Shield shorting at the end of the coax cables near the DUT was not performed in any measurements conducted within the scope of this study due to the 2 kHz – 1 MHz frequency range of interest.

2.2. Measurement Setup of Capacitance and Conductance

To understand how capacitance and conductance are extracted from the DUT, it is important to understand the role of impedance. Impedance (Z) is defined as the measurement of the total opposition of a device or circuit to AC current flow [1]. When measured it exists as a complex quantity containing both real and imaginary quantities known as resistance (R) and reactance (X), respectively. Reactance (X) can take on an inductive or a capacitive form as shown in Eq. 2.1 and Eq. 2.2, respectively where ω is the angular frequency of the applied signal, L_{mat} is the material inductance, and C_{mat} is the material capacitance.

$$X = X_L = 2\pi f L_{mat} = \omega L_{mat} \quad (2.1)$$

$$X = X_C = \frac{1}{2\pi f C_{mat}} = \frac{1}{\omega C_{mat}} \quad (2.2)$$

If resistance and reactance are in series with one another the impedance is measured as the mathematical sum of the two. This is shown as inset (a) of Fig. 2.3.

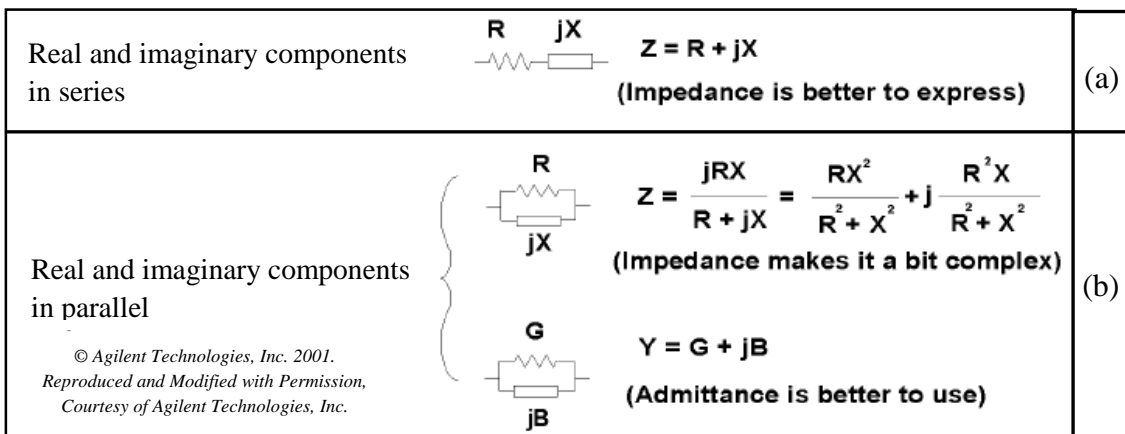


Fig. 2.3: Impedance (Z) and admittance (Y) representations adopted from [1]. (a) Impedance series configuration of resistance (R) and reactance (X). (b) Impedance parallel configuration transformed into a simpler expression known as admittance (Y). Admittance is composed conductance (G) and susceptance (B).

If, on the other hand, these quantities are in parallel to one another—as in the case of gate-to-channel capacitance evaluated in this study—impedance is measured as shown in the top of inset (b) of Fig. 2.3. In this case it is often much more convenient mathematically to consider Admittance (Y) as shown in bottom of this inset.

Admittance, as is shown in the bottom of inset (b) of Fig. 2.3 and in Eq. 2.3, is the inverse of impedance and is measured in Siemens. Admittance is also a complex quantity, composed of both real and imaginary quantities known as conductance (G) and susceptance (B), respectively.

$$Y = \frac{1}{Z} = G + jB \quad (2.3)$$

There are several methods available to measure the impedance or admittance of a DUT. Such include the Bridge, Resonant, I-V, RF I-V, Network Analysis, and Auto-Balancing Bridge methods. Reference is made to the Agilent Technologies Impedance Measurement Handbook [1] for specific details on each of these methods. All have their advantages and disadvantages. The Agilent 4284A used in this study uses the Auto-Balancing Bridge Method.

2.2.1. Auto-Balancing Bridge Method

The Agilent 4284A uses an Auto-Balancing Bridge Method to measure impedance of the DUT. The advantage of this method is that, first, it has wide frequency coverage (20 Hz – 110 MHz provided the $C-V$ meter supports it); second, it has high accuracy over a wide impedance measurement range provided the equipment configuration supports it; and third, it is capable of grounded DUT measurement [1]. The

main disadvantages are 1.) frequency ranges higher than 110 MHz cannot be measured and 2.) grounded DUT measurements—though possible by grounding the DUT as shown in Fig. 2.4—are difficult to perform because the measurement signal current can bypass the Low Probe amplifier network shown in Fig. 2.4, which can provide erroneous capacitance and conductance values [1].

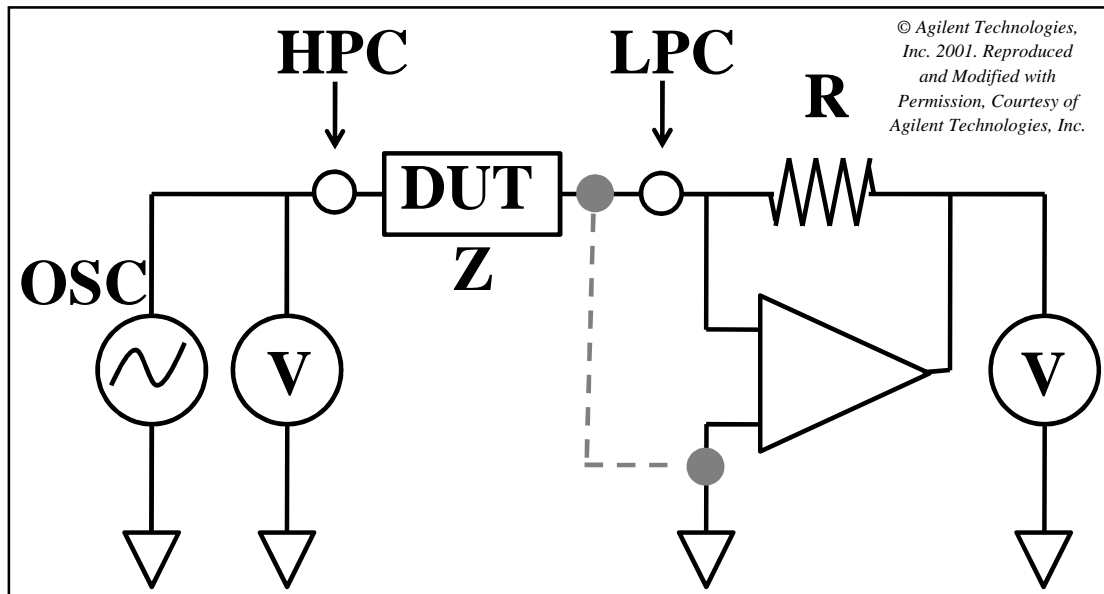


Fig. 2.4: Auto-Balancing Bridge Method impedance measurement adapted from [1]. The potential at the High Probes (HPC) varies through time as it is the input signal (DC sweep with AC signal superimposed). The potential at the Low Probes (LPC) is maintained at zero volts: it is called “virtual ground” for current passing through R is balanced with the current passing through the DUT using the I-V converter amplifier [1]. The impedance is calculated using the voltage at the HPC terminal and the current which crosses the resisting network R [1].

The most important aspect of the Auto-Balancing Bridge method is the fact that the measured impedances—in the case of this study translated to admittance—are only as accurate in value and behavior as the assumptions made about the DUT. In the case of the Auto-Balancing Bridge, it is assumed when using the parallel model—where the conductance and susceptance are parallel to each other resulting in the admittance representation—that, first, little current flows from the High Probes through the DUT to

the Low Probes and, second, that any current flowing into or out of the Low Probe is a result of DUT leakage from the high probe. The first case was found to be true in this study for DC analysis revealed gate leakage in the 1×10^{-11} A to 1×10^{-12} A range. The second case was found not to be true and affected the measured impedance which translated into non-ideal capacitance and non-ideal conductance behavior.

2.3. Purpose of C_{GC} , Regions of Operation, and Ideal Behavior

In order to compare new germanium MOSFET technologies with existing silicon MOSFET technology basic electrical analysis is required. This section will discuss a measurement known as Gate-to-Channel Capacitance (C_{GC}), in common use during both gate stack characterization and the benchmarking of advanced devices. During gate stack characterization, parameters such as Effective Oxide Thickness (EOT), channel threshold voltage (V_T), and Interface Trap Density (D_{it}) [4, 5] are commonly sought. During the benchmarking of advanced devices, parameters such as External Capacitance (C_{EXT}), Effective Channel Length (L_{EFF}), Inversion Charge (Q_i), Effective Carrier Mobility (μ_{eff}), and Saturation Velocity (v_{sat}) [5-9] are commonly sought.

Due to the wide use of C_{GC} as a foundation for Ge MOSFET characterization— μ_{eff} and v_{sat} require MOSFET I_{DS} versus V_{GS} analysis [7,8], also referred to as Split C - V Analysis— C_{GC} accuracy is an extremely important issue. This is especially true at smaller channel lengths where the drain and source regions become a significant contributor to C_{GC} [6]. During this study the investigator observed that Ge MOSFET C_{GC} did not always obey the known behaviors as expected from literature [10], research [4-9, 11], and as observed in Si MOSFETs containing identical gate stacks [12].

In particular, the Ge C_{GC} observed during channel accumulation was frequency-dependent and larger than expected (in the pF range versus the fF range) [12] resulting in a vertical shift in the C_{GC} curve as seen in inversion [12]. The exact reason for this was unknown until this study and will be discussed in Chapter 3. To better understand the C_{GC} measurement let us look at its configuration with a PMOSFET.

2.3.1. Connection to Generic PMOSFET

In this study C_{GC} was measured by connecting the High Probe Contact (HPC) and the two Low Probe Contacts (LPCs) – initially shown in Fig. 2.2 – to the MOSFET DUT as follows: the HPC is connected to the Gate, one of the LPCs is connected to the Source and the other LPC to the Drain. This C_{GC} connection scheme is shown in the (a1; b1; c1; a2; b2; c2) insets of Fig. 2.5. The LPCs are kept at virtual ground, meaning that the C - V meter senses the LPCs and biases them appropriately to maintain a 0 V bias on the Source and Drain. The HPC is swept from accumulation to inversion and vice versa while superimposing an AC voltage signal throughout the biasing range. This AC voltage signal is used to determine the admittance in the parallel model—composed of a conductance (G) and a susceptance (B)—of the gate at each DC bias.

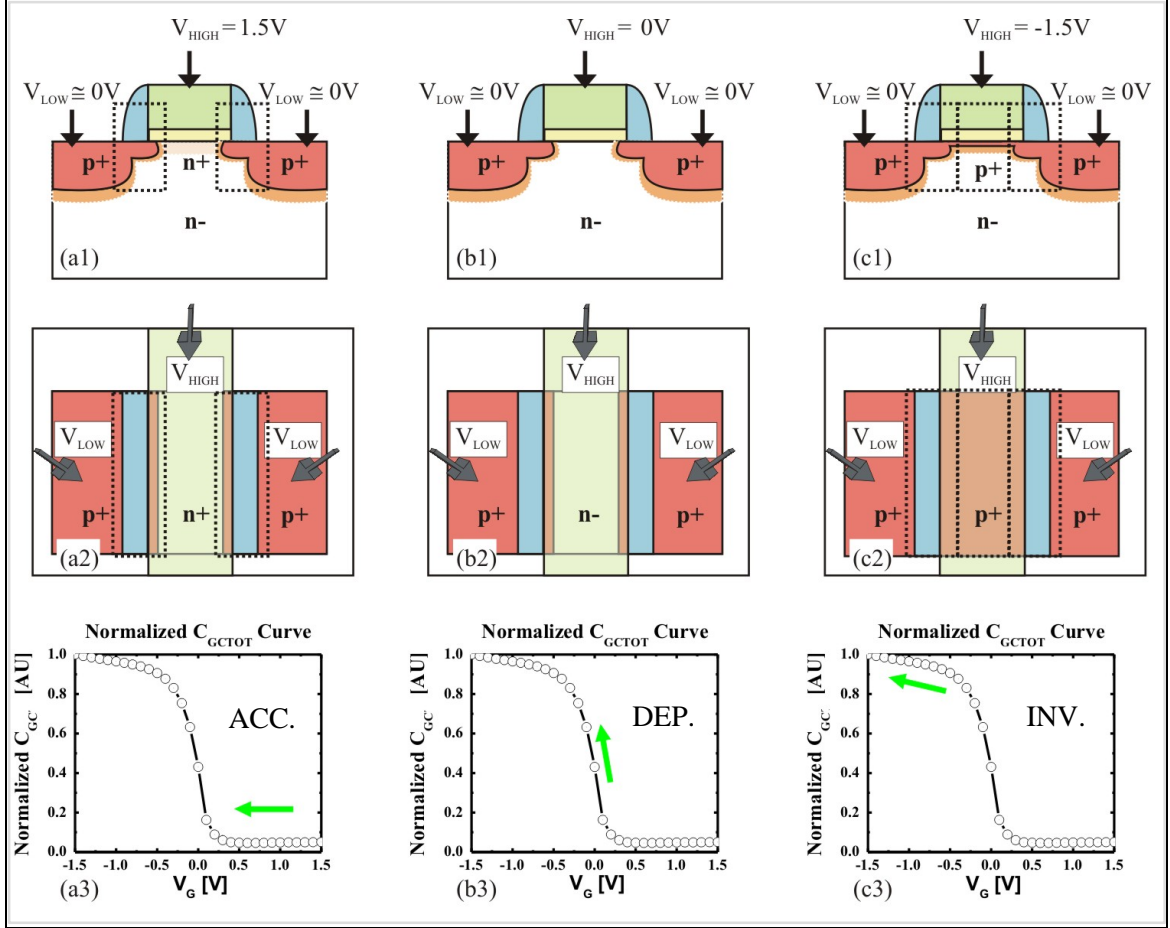


Fig. 2.5: Standard C_{GC} connection and measurement for PMOS. Horizontal (a1, b1, c1) and vertical (a2, b2, c2) illustrations of HPC (V_{HIGH}) and LPCs (V_{LOW}) connections. Normalized C_{GC} Curve (a3, b3, c3) illustrate modes of operation. There are three general C_{GC} modes: that at accumulation, depletion, and inversion.

The result of this C_{GC} connection as measured at accumulation, depletion, and inversion of a Si-PMOS is shown in Fig. 2.5. Notice that the C_{GC} capacitance is normalized to the maximum capacitance as observed in high inversion so as to illustrate the regions of MOSFET operation. In accumulation the capacitance measured between the HPC and LPC is illustrated in insets (a1, a2) and shown in inset (a3) of Fig. 2.5. It is observed that in accumulation the capacitance is extremely small. During depletion (b1-b3) the capacitance increases. It is here that the C_{IT} contributes. As the gate is swept to inversion as illustrated in insets (c1, c2), the capacitance becomes very large. The

capacitance in accumulation is typically referred to as the extrinsic capacitance, for most of it resides near the peripheries of the MOS channel; whereas that in inversion is typically referred to as the intrinsic capacitance, for it resides within the MOS channel.

2.3.2. High Accumulation and High Inversion

Fig. 2.6 can help explain why the accumulation capacitance is very small when compared to the inversion capacitance. Fig. 2.6 illustrates the extrinsic capacitance observed in channel accumulation and the intrinsic capacitance observed in channel inversion. The gate-to-channel capacitance measured in high inversion is the sum of the extrinsic and intrinsic capacitances in parallel.

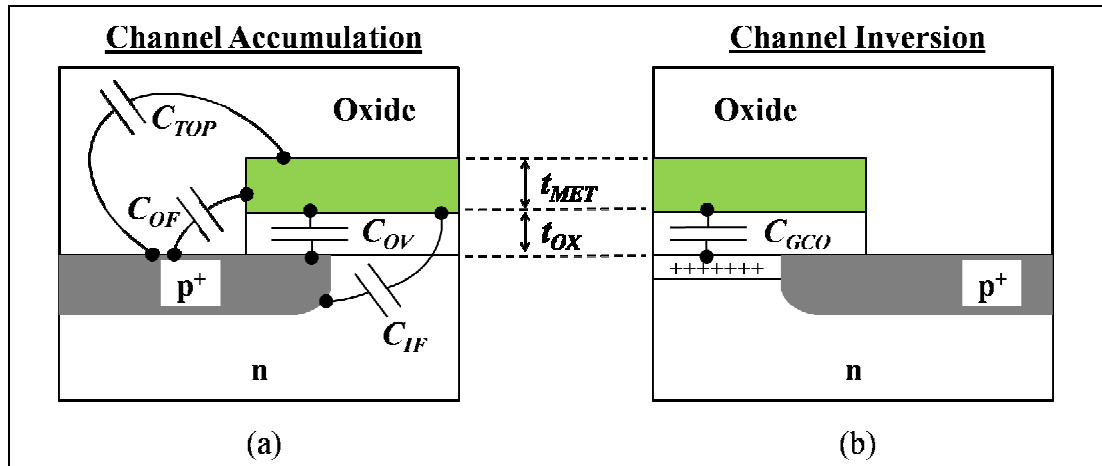


Fig. 2.6: Components of high accumulation and high inversion capacitance. (a) The four components of accumulation capacitance and (b) the component of inversion capacitance as adapted from [10].

Referring to inset (a) of Fig. 2.6, it can be inferred that during accumulation there exists no inversion channel. As a result, in accumulation only the capacitances between HPC and LPCs are observed. These result from gate overlap with the source/drain (C_{OV}), inner fringing fields between the gate and source/drain (C_{IF}), outer fringing fields

between the gate and source/drain (C_{OF}), and top capacitance as seen through the insulator between gate and source/drain contact (C_{TOP}). Likewise, inset (b) of Fig. 2.6 shows that during ideal inversion there exists an inverted channel below the gate connecting source to drain. From this connection an additional capacitance between the HPC and LPCs, known as the inversion capacitance (C_{GCO}), is observed. Assuming the inversion layer is at the channel surface, this inversion channel capacitance is considered a parallel plate capacitance proportional to the gate area and dielectric constant and inversely proportional to the dielectric thickness. This gate-to-channel capacitance (C_{GC}) is the sum of the extrinsic and intrinsic capacitance in parallel.

The ideal C_{GC} —as shown in Eq. 2.4—is the mathematical sum of the ideal extrinsic capacitance (C_{EXT}), the ideal inversion capacitance (C_{GCO}), and the ideal parasitic capacitance (C_{Para}).

$$C_{GC}(V_G, f)|_{\text{Fixed_LxW}} = C_{GCO}(V_G) + C_{EXT}(V_G) + C_{Para}(V_G, f) \quad (2.4)$$

The extrinsic capacitance in Eq. 2.5 is twice the C_{IF} that is gate-bias dependent—meaning that it is decoupled during inversion—and twice the outer capacitance (C_O) that is geometry and material dependent as shown in Eq. 2.6.

$$C_{EXT}(V_G) = 2C_{IF}(V_G) + 2C_O \quad (2.5)$$

$$C_O = C_{TOP} + C_{OF} + C_{OV} \quad (2.6)$$

Due to line calibration and open/short compensation error, a small C_{Para} may exist throughout the test fixture. This parasitic capacitance—if it exists—can be both

frequency and voltage-dependent. It is common to mathematically subtract C_{Para} from C_{GC} after measurement. By subtracting C_{Para} from the C_{GC} curve it is quite obvious that one removes the C_{OV} information while maintaining the C_{GCO} information. Minimizing C_{Para} prior to measurement allows one to approach the effective total capacitance, which provides a near true C_{GCO} and C_{OV} .

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Chapter 3

Germanium PMOSFET C_{GC} Measurement

The Ge-PMOS C_{GC} in this study was measured using Configuration-3 as discussed in the previous chapter. C - V tool calibration was the same for all data presented in this section and is as follows: the HP 4284A cable calibration was set/checked to 4 meters; the low-voltage and low-current triaxial Unknown Terminals (UTs) were split (using two triaxial T-Bars) across two micromanipulators (for separate source and drain connection); the high-voltage and high-current triaxial UT was connected to the gate micromanipulator; open compensation was performed with the probe tips in the air; short compensation was performed using a shorting box. The shorting box required that one disconnect the triaxial cables from the micromanipulators. As a result, the finite cable length between the triaxial cable-ends and probe tips was never included in the short compensated. This can result in small capacitance/admittance error, but that this error was not observed in any of the measurements presented in this chapter.

Ge-PMOS C_{GC} measurement-program setup and data acquisition was the same for all Ge-PMOS C_{GC} presented in this study. The parallel capacitance-conductance circuit mode (Cp - Gp) was selected. The parallel circuit mode was selected knowing that the C_{GC} measured in inversion would be in the pF range and expecting that the parallel resistance (R_p) would be more significant than the series resistance (R_s). This turned out to be a good assumption in inversion. Each Ge-PMOS was measured using a 30 mV signal level with medium integration time: the starting voltage was set at -1.5 V and the ending voltage was set at +1.5 V; a step size of 50 mV was used; hysteresis was not evaluated

for it was not significant in the biasing of this study. Hysteresis evaluation is a source for future research.

3.1. Conductance Method

To identify a conductance signature of interest in this study, the conductance method first proposed by Nicollian and Goetzberger in 1967 [1,2] will be briefly discussed. The circuit diagram of a MOS capacitor when considering the parallel circuit mode used in the conductance method is shown in Fig. 3.1.

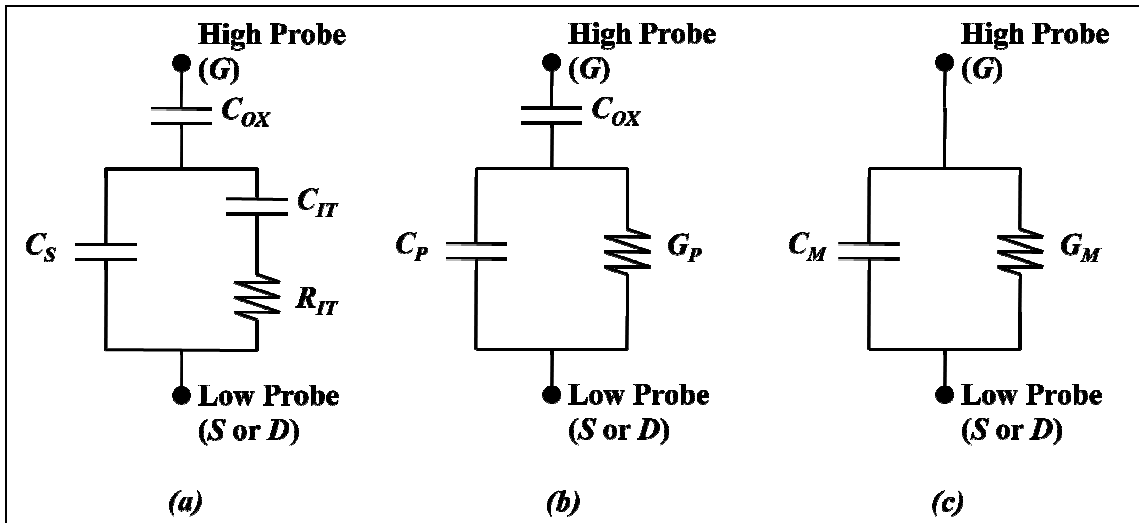


Fig. 3.1: Equivalent circuit for parallel conductance measurements (a) MOS capacitance considering additional capacitance due to interface traps, (b) simplified circuit of (a), (c) measured circuit adapted from [1].

It is obvious from Fig. 3.1 that when measuring the capacitance of a MOS capacitor, the measured capacitance (C_M) consists of the fixed oxide capacitance (C_{OX}) as shown in Eq. 3.1 in series with the parallel capacitance-conductance (C_P-G_P). The parallel capacitance shown in Eq. 3.2 is the mathematical sum of both any additional substrate capacitance in parallel with any additional interface trap capacitance present in depletion and weak inversion of the oxide-semiconductor interface.

$$C_{OX} = \frac{K_{OX}\epsilon_{OX}A}{T_{OX}} \quad (3.1)$$

$$C_P = C_S + \frac{C_{IT}}{1+(\omega\tau_{IT})^2} \quad (3.2)$$

It must be noted that Eq. 3.2 assumes that the interfacial traps contain a single energy level in the bandgap. It is clear from Eq. 3.2 that when dealing with a MOS capacitor, C_P is directly proportional to both C_S and the effective C_{IT} , and that the effective C_{IT} increases as the trap time constant decreases.

When using the conductance method on a MOS capacitor the interface trap density (D_{IT}) can be measured at densities of $10^9 \text{ cm}^{-2}\text{eV}^{-1}$ and lower by evaluating the conductance (G_P) normalized to angular frequency (ω) as shown in Eq. 3.3 [1,2] below. G_P is in units of S/cm^2 .

$$\frac{G_P}{\omega} = \frac{q\omega\tau_{IT}D_{IT}}{1+(\omega\tau_{IT})^2} \quad (3.3)$$

Eq. 3.3 considers the fact that capture and emission of minority carriers—by the traps at a single energy level in depletion and weak inversion—occur a few kT/q above and below the Fermi level [1]. This fact results in a Gaussian distribution of G_P/ω versus ω at fixed gate bias. The peak of this distribution has a maximum at $\omega \cong 1/\tau_{IT}$ and at that maximum $D_{IT} = 2G_P/q\omega$ [1]. This Gaussian distribution was observed in the C_{GC} of this study and is a signature indicating trap-assisted leakage between the high and low probes.

It is important to note that in this study three regions of operation exist—accumulation, depletion, and inversion—and that Fig. 3.1 could be used during depletion assuming low source and drain leakage into the well. In this study, however, large source

and drain leakages into the substrate are observed. As a result this Gaussian distribution of G_p/ω versus ω at fixed gate bias can also occur within the depletion region of the source/well and drain/well junctions, should the LPCs not be exactly 0 V.

3.2. C_{GC} Measured Regions and Observed Behavior

The first Ge-PMOS devices measured contained D1 architecture, gate lengths of 10 μm , and gate widths of 10 μm . The capacitance results are shown in Fig. 3.2 and the conductance results are shown in Fig. 3.3. In reviewing Fig. 3.2 first note the C_{GC} frequency dispersion. The slope of C_{GC} with respect to V_G is negative (nearly zero) at every frequency in high inversion and positive at every frequency in high accumulation. The transition from negative to positive slope occurs within the depletion regime and the C_{GC} increase is more dramatic at lower frequencies than at higher frequencies. The voltage at 1 MHz—where G_{GC} begins to increase due to the transition between depletion and weak inversion—is close to the device threshold voltage and is approximately +0.20 V. This moderate threshold voltage is less certain at lower frequencies where the interface trap capacitance in depletion/weak inversion begins to increase significantly.

It is clear that from Fig. 3.2 that a large parasitic C_{GC} exists. There were three hypotheses regarding its source—in part because reliable conductance data could not be obtained—first, that the parasitic capacitance was due to incorrect compensation; second, that there was current leakage from gate into source and drain; third, that there was current leakage from source and drain into the well. The first hypothesis was ruled out by tedious compensation, the second was ruled out by DC gate leakage analysis confirming leakage in the pA range, and the third was verified by leakage analysis confirming

leakage in the μA range. Conductance verified this leakage analysis and will now be discussed.

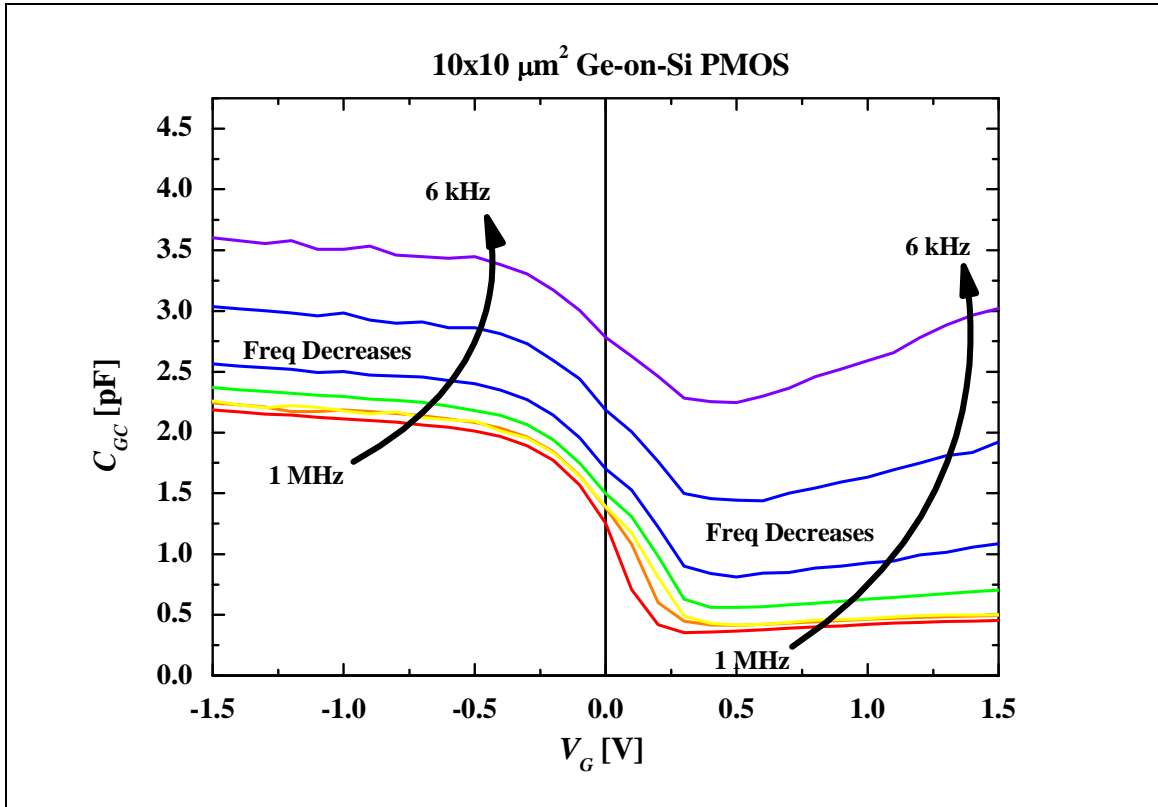


Fig. 3.2: C_{GC} for a $10\ \mu\text{m} \times 10\ \mu\text{m}$ Ge PMOS device containing D1 Module Architecture. Gate voltage (V_G) is swept from inversion to accumulation and frequency is swept from 1 MHz to 6 kHz showing the C_{GC} frequency dispersion.

In reviewing Fig. 3.3, the normalized conductance (normalized to angular frequency) contains frequency dispersion similar to the capacitance case. This makes sense since both capacitance and conductance are derived from admittance. The normalized conductance has approximately no slope in inversion, has a positive slope in accumulation, and starts to approach exponential behavior in high accumulation.

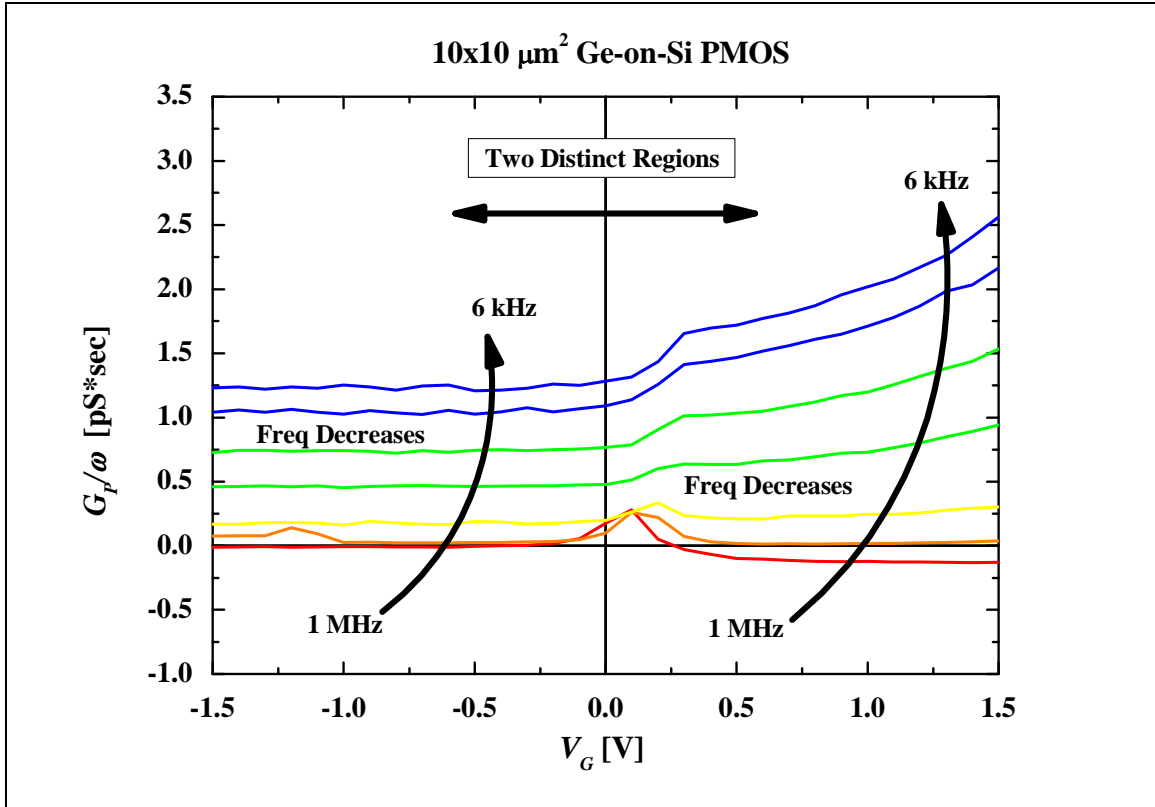


Fig. 3.3: Normalized conductance (G_p/ω) for a $10\ \mu\text{m} \times 10\ \mu\text{m}$ Ge PMOS device containing D1 Module Architecture. Gate voltage (V_G) is swept from inversion to accumulation and frequency is swept from 1 MHz to 6 kHz showing the C_{GC} frequency dispersion.

Fig. 3.3 also contains two distinct regions of operation—in inversion and in accumulation. It is clear that there is a conductance into or out of the low probes in contact with the source and drain leading to a parasitic capacitance observed in C_{GC} . The primary goal of this study was to minimize the parasitic capacitance. This was first done by grounding the substrate and eventually followed by floating the substrate while decreasing the source/drain area; decreasing the source/drain contact distance from the gate; increasing the gate area; maximizing the frequency of measurement. The effect of grounding the substrate will be discussed in the next section.

3.3. Parasitic C_{GC} Chuck Dependence

It was initially found that grounding the substrate to the DUT ground terminal resulted in a C_{GC} free of the parasitic capacitance previously observed while the substrate was floating. This is shown in Fig. 3.4.

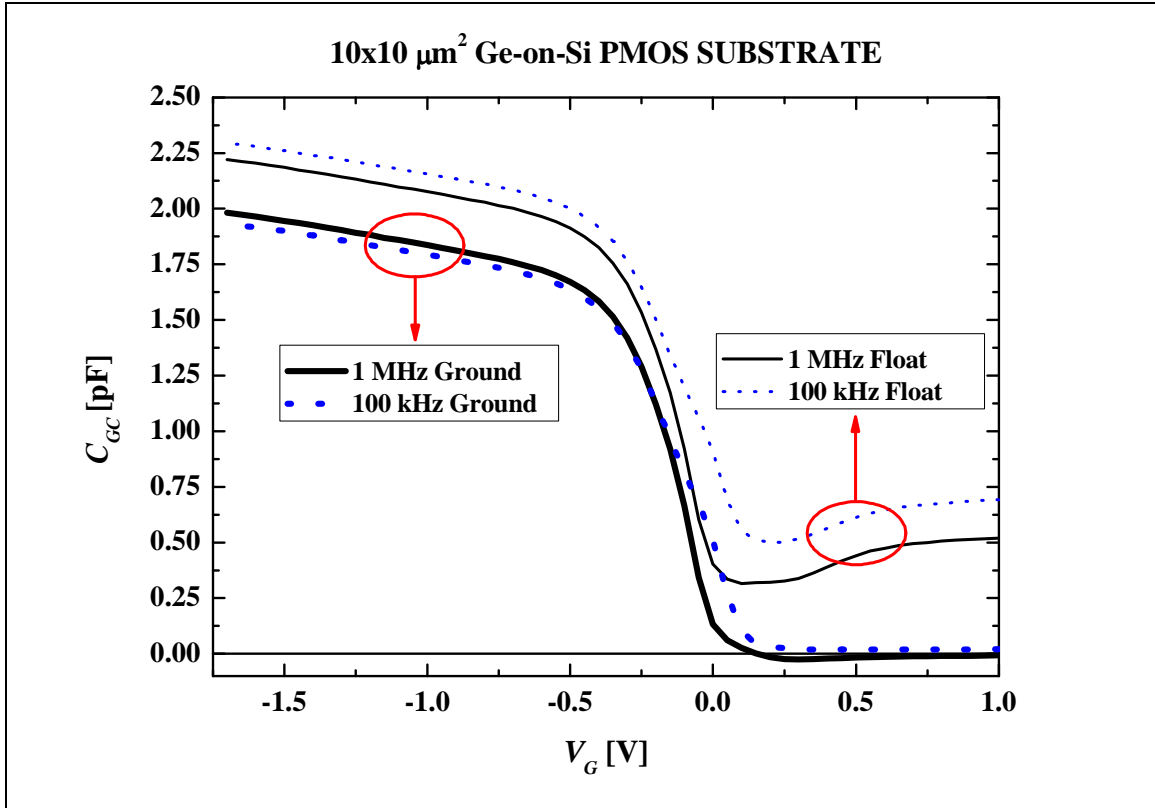


Fig. 3.4: Parasitic C_{GC} removal for a $10\ \mu\text{m} \times 10\ \mu\text{m}$ Ge-PMOS device containing D1 Module Architecture. Comparison of substrate floating versus substrate grounding as observed at 100 kHz and 1 MHz.

From Fig. 3.4 one should note that despite removing the parasitic capacitance through substrate grounding the C_{GC} for 1 MHz as observed in depletion/moderate accumulation is slightly negative. This negative capacitance results in a questionable C_{GC} curve. After discovering this grounding condition it was found that grounding the Ge-PMOS was common. The investigator noted that grounding the substrate resulted in negative and questionable conductance information.

Before moving on, the difference between the grounded and floating conditions for C_{GC} were calculated as shown in Fig. 3.5.

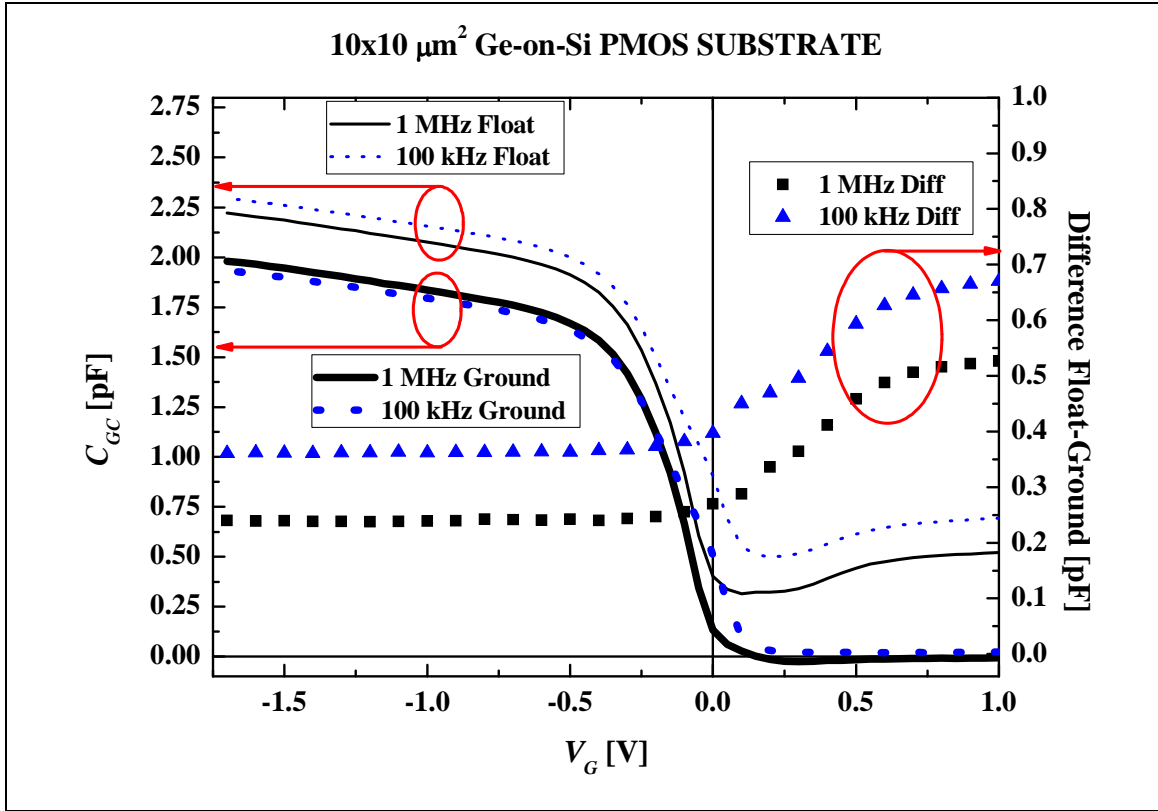


Fig. 3.5: Difference of C_{GC} 1 MHz & 100 kHz (Float-Ground) calculated at each V_G . Note the linear difference in inversion which increases rapidly in depletion/weak accumulation before saturating in high accumulation.

The difference is shown in Fig. 3.5 and a hypothesis was formed. It was believed that current conduction was possible between the well and chuck. To confirm this, the current was measured while applying a bias between the front-side well and chuck contacts. The results are shown in Fig. 3.6 and compared with the results of a Si-PMOS exhibiting n/p well counter-doped isolation, but identical gate stack technology.

As can be observed in Fig. 3.6 the Ge-PMOS device exhibits a resistive behavior between the well (n-layer) area and the chuck, whereas its Si-PMOS equivalent exhibits a diodic characteristic. This was the first indication that the parasitic capacitance (not

observed in the Si-PMOS technology) was not gate stack-related (both Ge and Si-PMOS technologies contain identical gate stacks) but well-related.

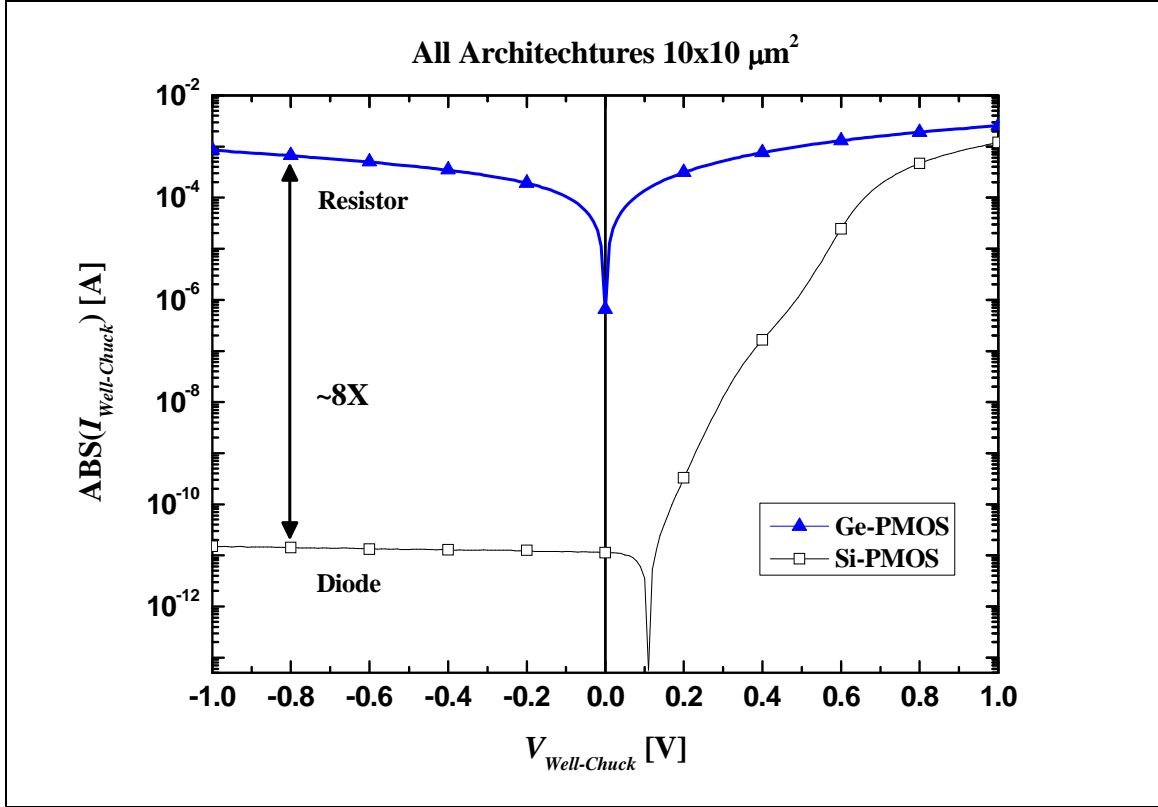


Fig. 3.6: Absolute current leakage from front-side well contact to chuck comparison between Ge-PMOS using n-layer well technology and a Si-PMOS equivalent containing identical gate stack but using n/p well isolation technology.

The results of the grounding effect are summarized in Fig. 3.7. The parasitic capacitance is broken into two regions in Fig. 3.7—a gate-voltage dependent parasitic capacitance (C_{Para1}) and a gate-voltage/frequency dependent parasitic capacitance (C_{Para2}).

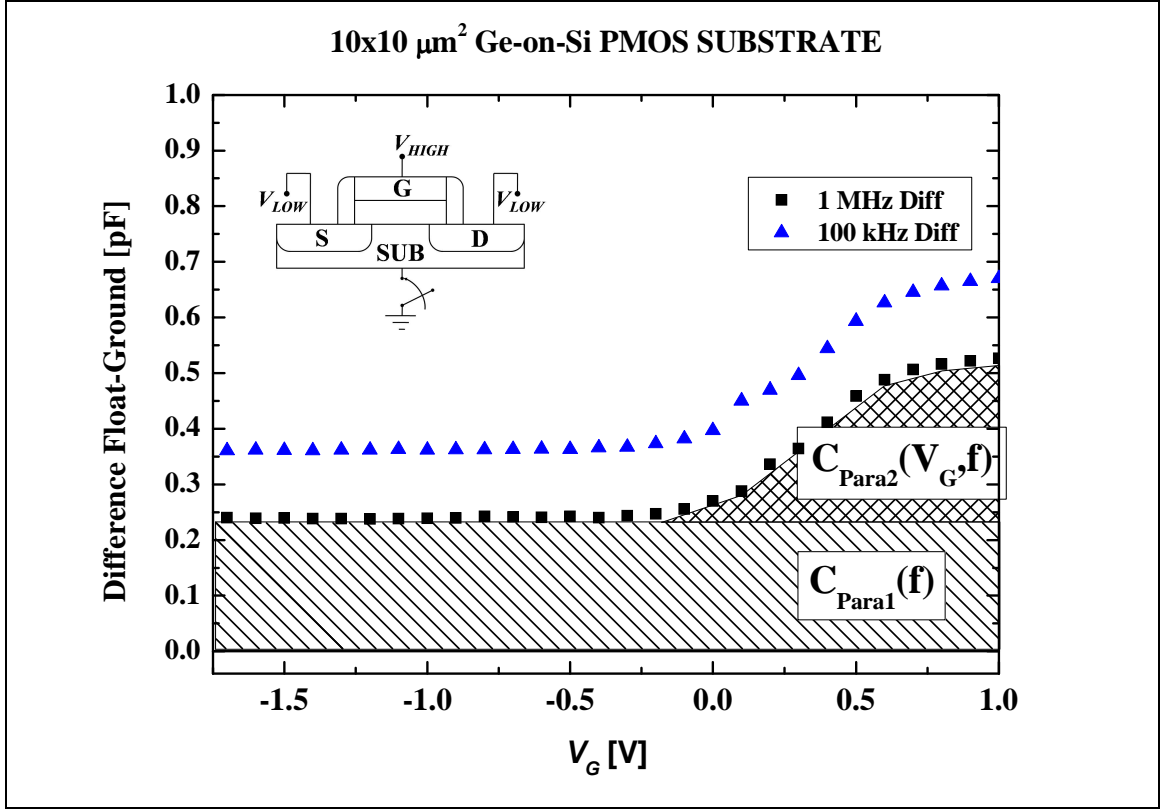


Fig. 3.7: Difference of C_{GC} 1 MHz & 100 kHz breakdown into C_{Para1} & C_{Para2} .

C_{Para1} is due to trap generation leakage current in the space/charge depletion region of the source/well and drain/well p/n junctions and C_{Para2} is due to trap generation leakage current under the depleted gate during depletion and gate-induced-junction leakage during high accumulation. Grounding the substrate dumps these extra carriers to ground, thereby preventing their buildup under the gate and field oxide during C - V measurement.

3.4. Parasitic C_{GC} Source and Drain Geometry Dependence

Due to the effect of substrate grounding on conductance measurement, the Ge-PMOS C_{GC} grounding technique was quickly avoided. This led to the belief that the negative conductance initially observed was in essence due to measurement technique, not the device. Before proving this and obtaining the correct conductance, it was found

that minimizing the source/drain area and source/drain contact distance to gate reduced the parasitic C_{GC} . The minimum C_{GC} for these device was observed at $V_G = 0.4$ V corresponding to depletion/accumulation (close to the flatband voltage) transition and shown in Fig. 3.8.

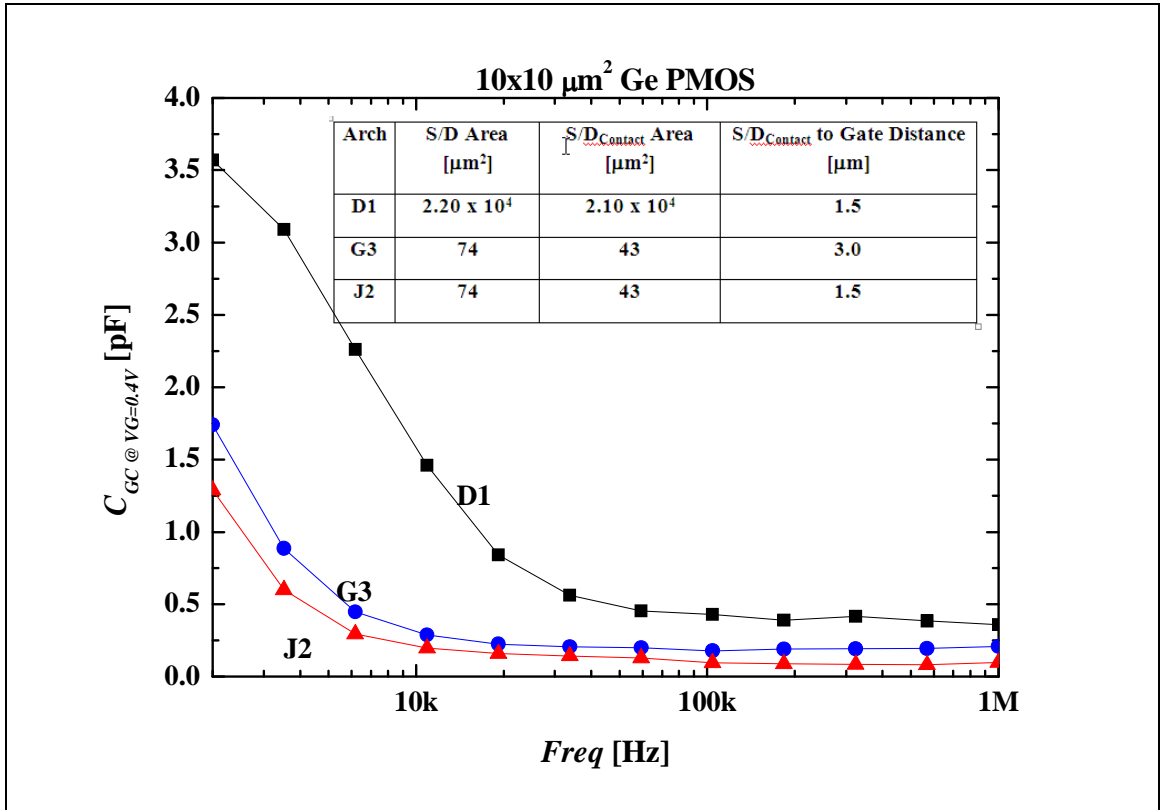


Fig. 3.8: Minimization of C_{GC} Parasitic Capacitance observed at $V_G = 0.4$ V using J2 Architecture.

Fig. 3.8 shows that the J2 architecture contains a minimum parasitic capacitance within an acceptable frequency range. This minimum parasitic capacitance is compared to a silicon equivalent containing an identical gate stack in Fig. 3.9. It is obvious that to measure C_{GC} , the J2 $10 \mu\text{m} \times 10 \mu\text{m}$ device should be selected and measured within a frequency range of 100 kHz to 1 MHz.

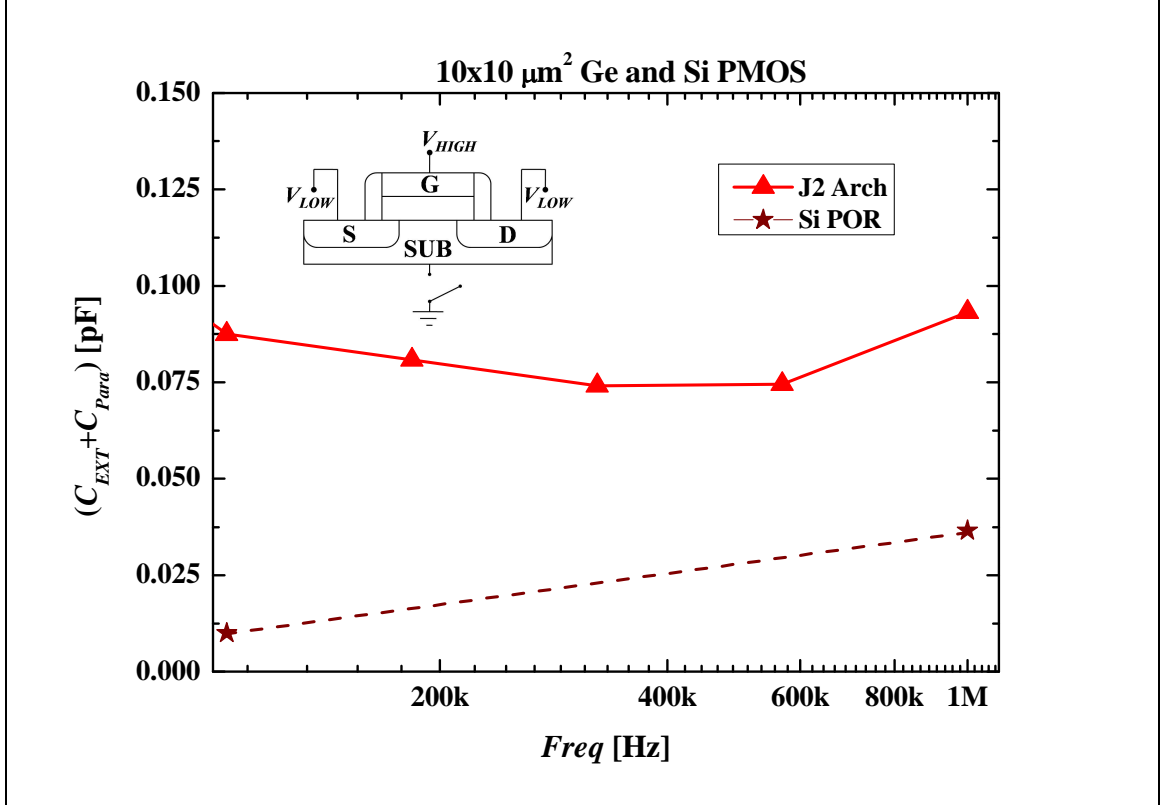


Fig. 3.9: Extrinsic and parasitic capacitance comparison of J2 to Si POR at $V_G = 0.4$ V revealing J2 accumulation capacitance in the fF range.

Minimization of the C_{Para} is one aspect of this study, but to fully understand and ensure that this minimization is truly valid we must understand its origin. The correct capacitance and conductance measurements were conducted using a floating substrate. The results for architecture and gate length are shown in the next section. The signature of the conductance reveals frequency and gate voltage dependent trap-assisted leakage.

3.5 Parasitic C_{GC} & Conductance versus Architecture

Capacitance and conductance measured in the D1 architecture versus gate length is shown in Fig. 3.10. Note that all conductance plots in Fig. 3.10 contain an inset of G_P/ω versus V_G .

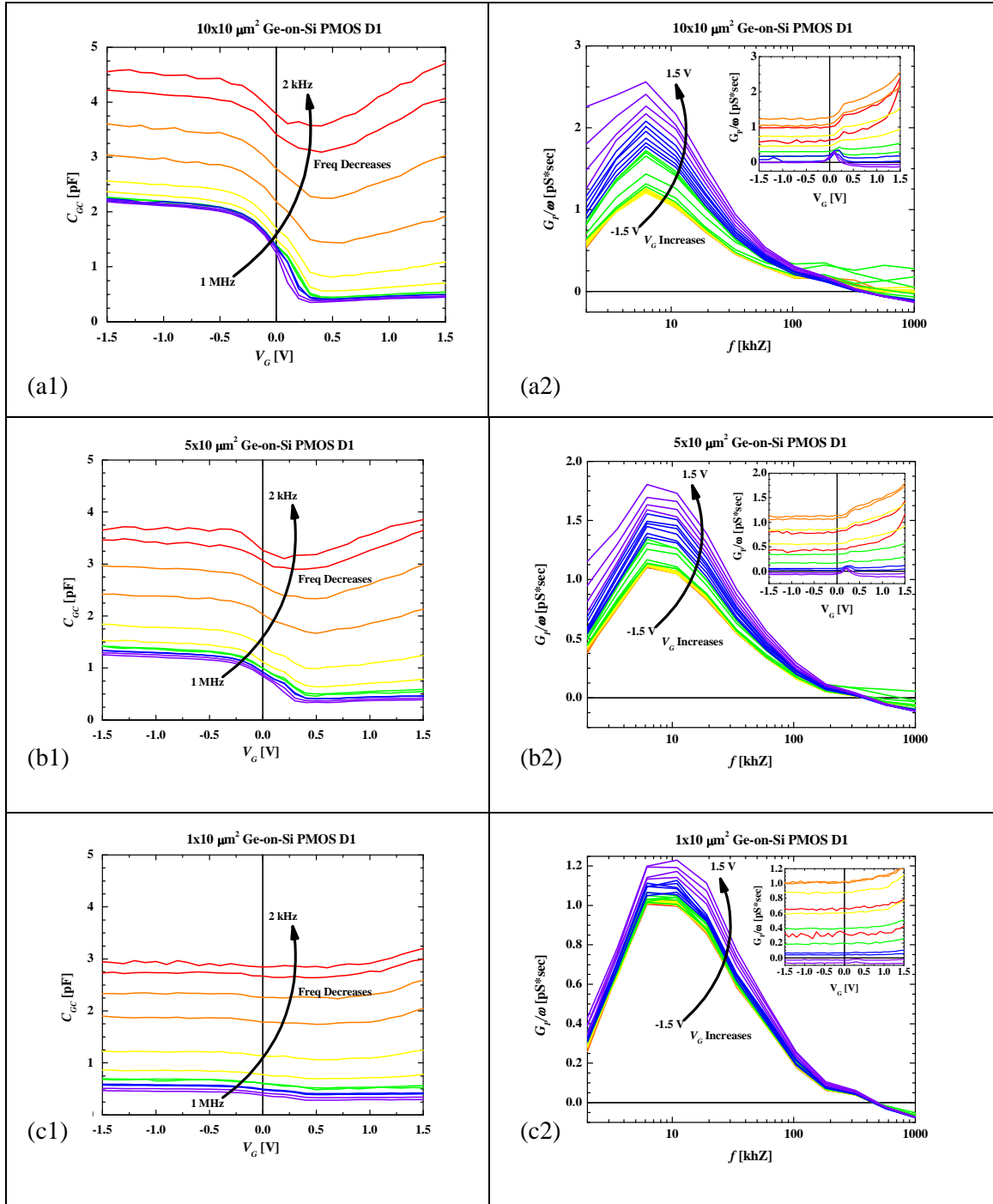


Fig. 3.10: Capacitance and conductance measurement of D1 architecture for gate lengths of (a) 10 μm (b) 5 μm and (c) 1 μm.

A great deal of information can be obtained from Fig. 3.10 in regards to the D1 architecture. First, when looking at the D1 10 μm gate length conductance (a2), note that there is a trap signature (Gaussian distribution). Second, notice that the peak of this

distribution does not vary with V_G , but its magnitude does. Specifically the higher the gate bias in accumulation the greater the normalized conductance as shown in the inset of (a2). The fact that this trap level is independent of V_G indicates that its location is not at the gate/semiconductor interface, but within the source/well and drain/well p/n junction depletion regions. Third, note that the peak of the normalized conductance curve versus frequency compares with the frequency spread of the parasitic C_{GC} : specifically the higher the peak the greater the spread in parasitic capacitance between frequencies. This is better observed in the D1 architecture with gate length of $1\ \mu\text{m}$ (c1-c2). Fourth, note that as the gate length of the D1 architecture decreases the normalized conductance peak both decreases and moves to higher frequencies. It seems that the traps decrease slightly in concentration and become much faster with decreasing gate length. It is noted that the processing parameters are identical regardless of both geometry and gate length leading one to believe that the electric field distribution may be different in each device.

From Fig. 3.10 it seems that the gate length has an effect on the trap assisted conductance out of and/or into the low probes. This same test was performed for G3 and J2 architectures for gate lengths $10\ \mu\text{m}$; $5\ \mu\text{m}$; $1\ \mu\text{m}$ as shown in Fig. 3.11 and Fig 3.12, respectively. Both Fig. 3.11 and 3.12 agree with the observations made in Fig. 3.10 for the D1 architecture. The fact that the trap assisted conductance is geometry dependent is important. There tends to be a decrease in the peak normalized conductance as well as a shift to the right when comparing gate lengths for D1, G3, and J2 architectures. This could be trap or electric field distribution-related due to the identical processing parameters versus gate length and architecture.

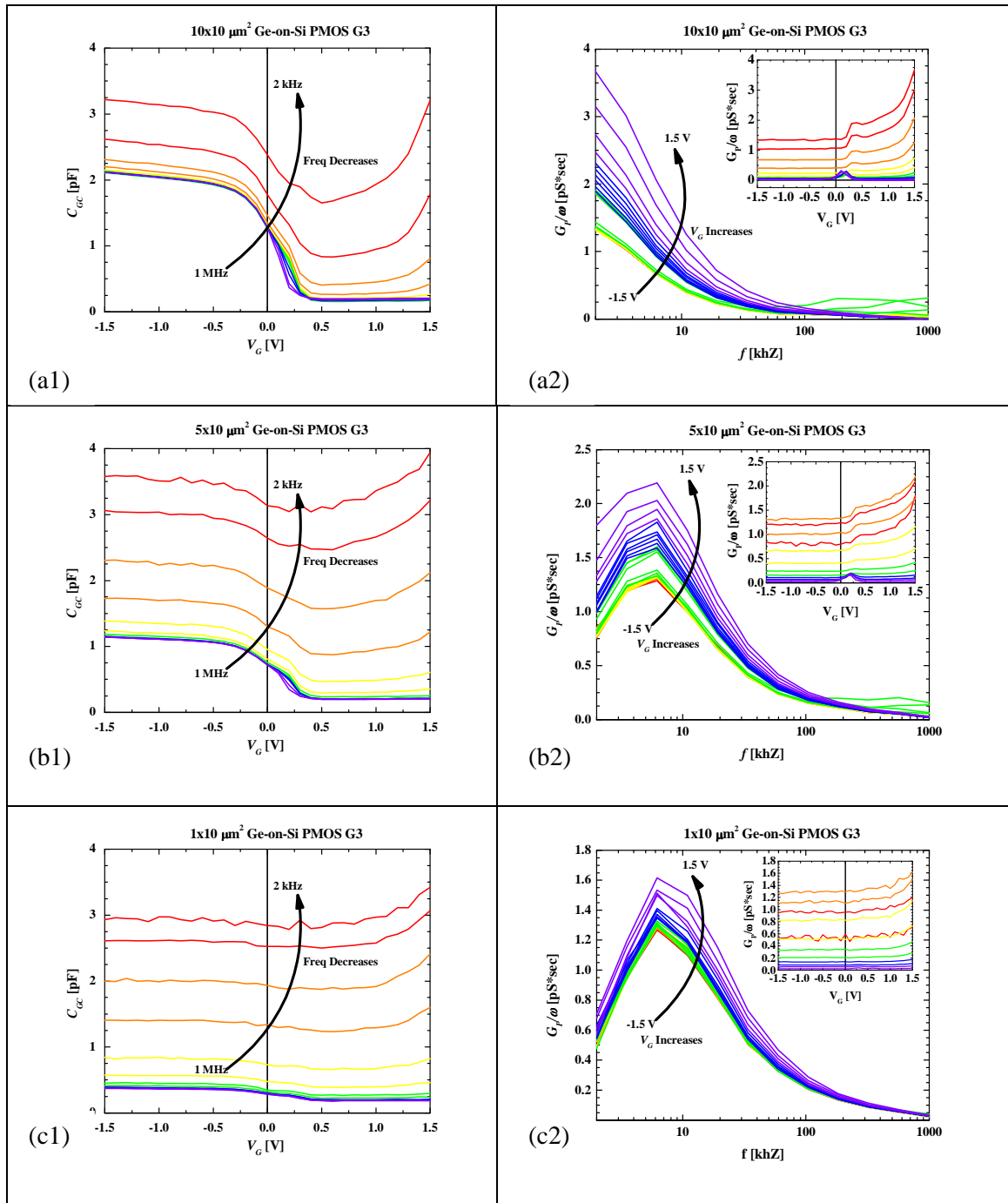


Fig. 3.11: Capacitance and conductance measurement of G3 architecture for gate lengths of (a) 10 μm (b) 5 μm and (c) 1 μm .

In comparing Fig. 3.11 with Fig. 3.10, notice that the normalized conductance peak versus frequency starts farther left at the 10 μm device but begins to travel right and down as gate length is reduced.

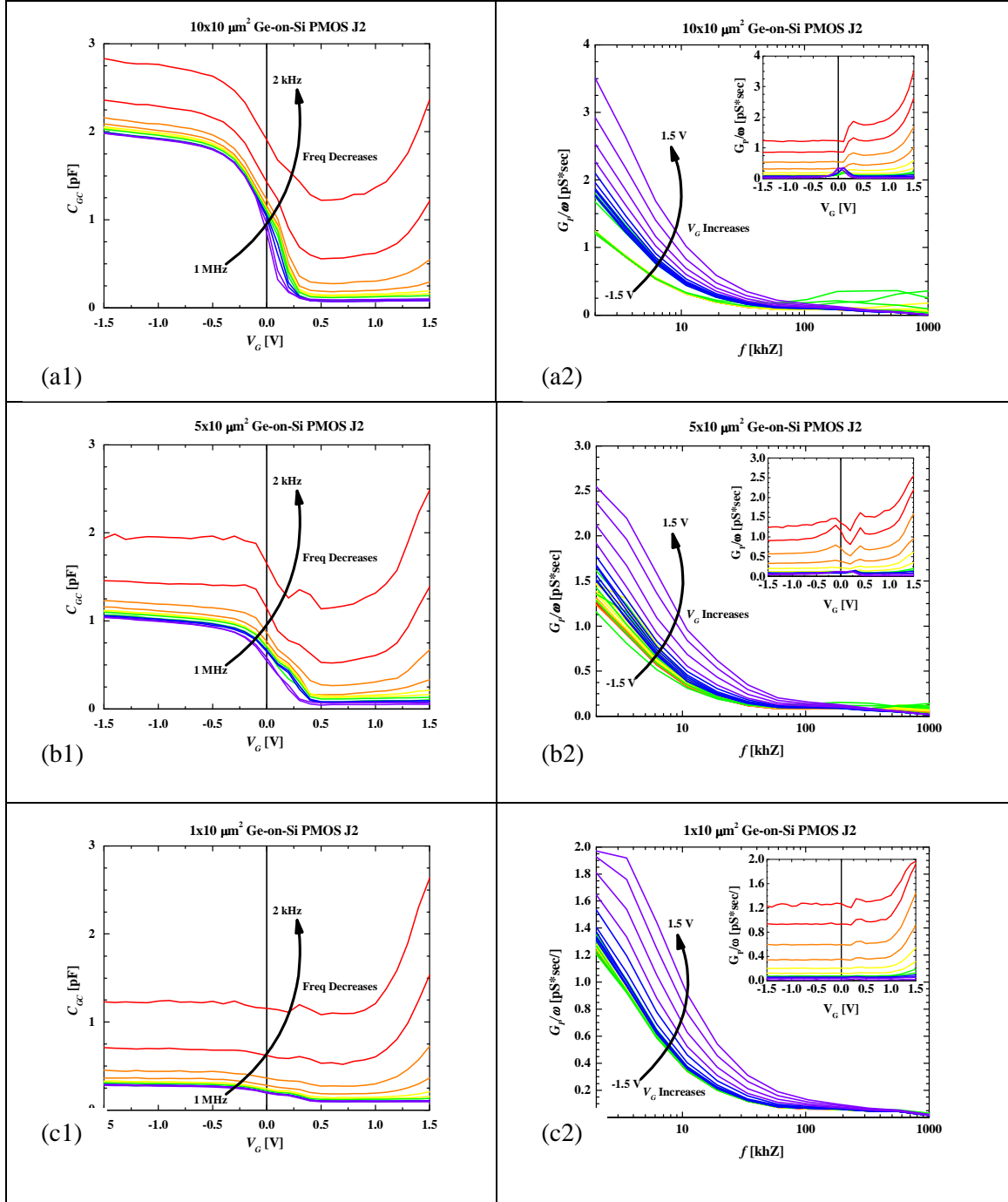


Fig. 3.12: Capacitance and conductance measurement of J2 architecture for gate lengths of (a) 10 μm (b) 5 μm and (c) 1 μm .

In comparing Fig. 3.12 with Fig. 3.11, notice again that the normalized conductance peak versus frequency starts farther left at the 10 μm device but begins to travel right and down as gate length is reduced. This normalized conductance peak for the J2 device does

not appear, however, even at gate lengths as short as 1 μm . In summary of Fig. 3.10-3.12, Table 3.1 reveals that the location of the normalized frequency peak f_{GMAX} is dependent on both architecture and gate length. The magnitude is not included since not all peaks could be found, but it was observed that the normalized conductance tended to decrease with a decrease in gate area.

Table 3.1: Summary of approx. peak conductance location and magnitude for Fig. 3.10-3.12.				
Parameter	L_G [μm]	Architecture		
		D1	G3	J2
f_{GMax} [kHz]	10	6.2	<2.0	<<<2.0
	5	8.6	4.9	<<2.0
	1	10.9	8.6	<2.0
G_p/ω [pS*sec] Taken at f_{GMAX} ; V_G = -1.5 V	10	1.2	NA	NA
	5	1.1	1.3	NA
	1	1.0	1.2	NA

Overall, it is observed that the reason J2 architecture out-performs both D1 and G3 resides in the fact that during C - V analysis f_{GMAX} is farther from the 100 kHz–1 MHz frequency of interest as shown in Table 3.1. There is also a tendency for the peak of this normalized conductance to increase as one fixes the gate length and moves from D1 to G3 to J2. The reason for this is unknown and more data is needed to create a definitive comparison. DC analysis and activation energy extraction will reveal why these trap-assisted leakage components are constant in inversion, increase slightly when $0.0 \text{ V} \leq V_G \leq \sim 0.5 \text{ V}$, and increase rapidly when V_G is in high accumulation.

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Chapter 4

C_{GC} Technique Affecting Conductance

Earlier, the effect of substrate grounding was briefly discussed. Specifically, it was noted that substrate grounding removed the parasitic C_{GC} behavior observed during Ge-PMOS C_{GC} measurement. During C_{GC} evaluation the investigator had a difficult time obtaining well-behaved conductance data. The conductance data was occasionally negative and contained discontinuities when plotted versus both frequency and voltage.

Over a period of time, similarities were noticed when measuring the conductance of MOS InGaAs dot capacitors. During measurement the interfacial quality of the MOS InGaAs dot capacitors was quantified using the conductance method [1] and as a result interested was paid to both the conductance and the capacitance data. It was noticed that discontinuities would occasionally appear in the conductance versus frequency and voltage data, indicating measurement error. The response was to move to a different C - V unit and re-measure the device of interest. This was time consuming—the conductance method for III-V's utilizes temperature-dependent analysis to observe D_{IT} distribution within the semiconductor bandgap—and furthermore did not address the source of measurement error.

A distribution in measurement error with respect to C - V tool was noticed by the investigator. Specifically, it was noted that for C - V units closer to the Keithley setup negative and discontinuous conductance behavior occurred more often than for those farther from the Keithley setup. The Keithley setup C_{GC} program default was to ground the Ge-PMOS substrate during measurement. Around this time the investigator ruled out

parasitic C_{GC} due to gate leakage from the high probe into the low probes, and ruled out $C-V$ calibration error. The only other hypothesis was that leakage from the source and drain into the well induced the parasitic C_{GC} . DC analysis confirmed this. To obtain reliable conductance data during AC analysis the investigator hypothesized that grounding the Ge-PMOS substrate had been inducing the measurement error all along. For this hypothesis to be correct, the induced error would have to be observed and remain for a short time after both removing the substrate ground and after performing short/open compensation: C_{GC} was measured previously while floating the substrate after open/short compensation and negative discontinuous conductance data was observed.

4.1. Grounding Germanium Substrate

To prove this hypothesis the investigator reserved a different $C-V$ unit identical to Configuration-3. The setup and calibration procedures were kept identical to those used to measure C_{GC} as discussed in the previous chapter. The Ge-PMOS $10\ \mu\text{m} \times 10\ \mu\text{m}$ D1 architecture was tested while maintaining a floating substrate. Well-behaved conductance data were obtained. The investigator grounded the chuck and found that doing so induced negative discontinuous conductance data. After this the chuck was left floating and C_{GC} measured again. The negative and discontinuous conductance behavior remained. Open and short compensations were performed and the device measured again. It took three open and short compensations to remove the negative discontinuous conductance behavior. The results of the measurements are shown in Fig. 4.1 (a1) through (c2).

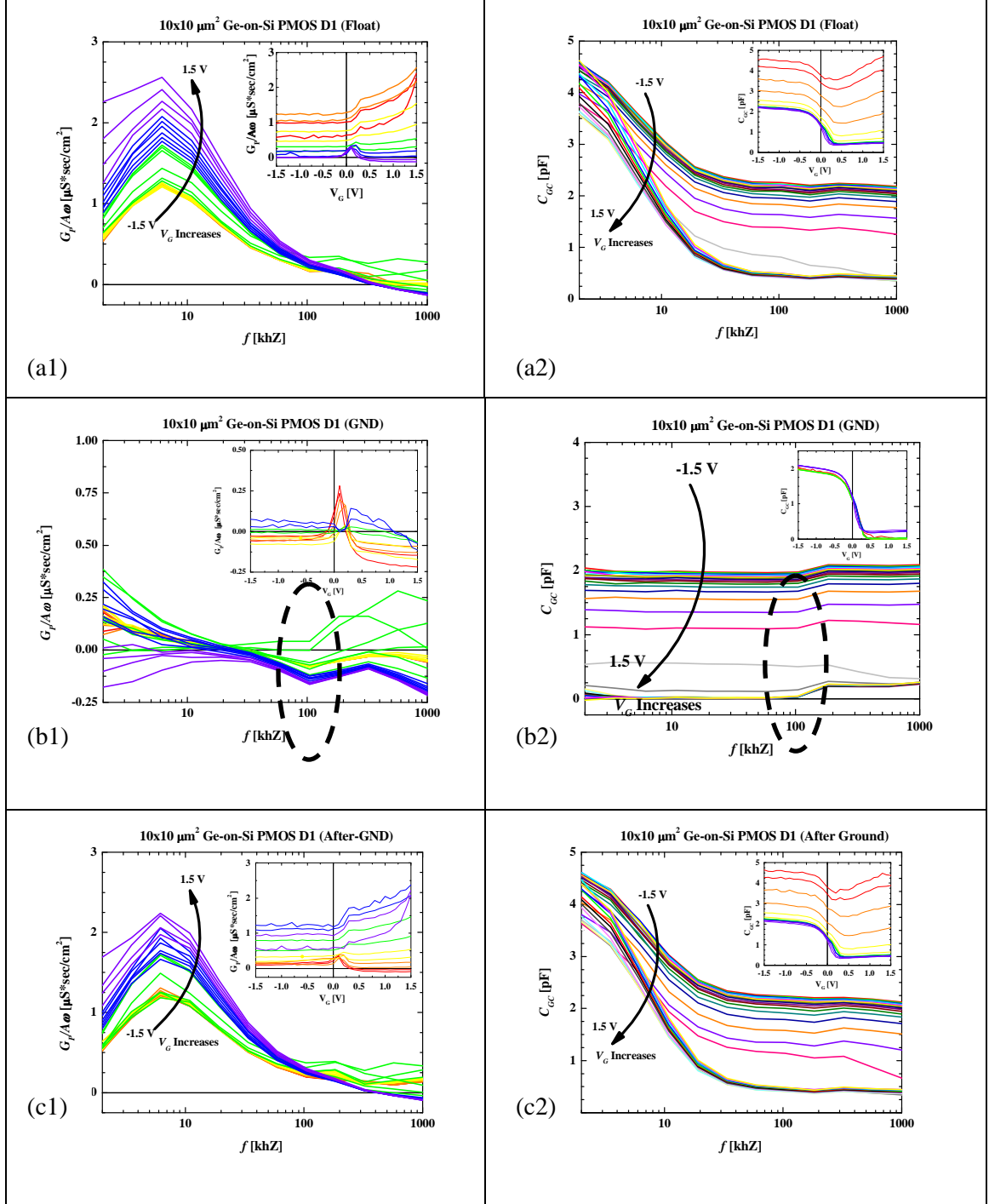


Fig. 4.1: Grounding substrate effect. Measurement of Ge-PMOS with floating substrate (a1) $G/A\omega$ and (a2) C_{GC} ; grounded substrate (b1) $G/A\omega$ and (b2) C_{GC} ; floating substrate after three open/short compensations (c1) $G/A\omega$ and (c2) C_{GC} .

Before moving on to the mathematical difference between the floating substrate after three re-compensations and the floating substrate before substrate ground for both

$G/A\omega$ and C_{GC} , let us review Fig. 4.1 (a1) through (c2). Note first that (a1), (b1), and (c1) are plots of $G/A\omega$ versus frequency; that (a2), (b2), (c2) are plots of C_{GC} versus frequency; and that all contain insets of either $G/A\omega$ versus V_G or C_{GC} versus V_G . Note also that the result trend from top to bottom is the same as the measurement trend discussed in the previous paragraph.

Fig. 4.1 (a1) and (a2) show that when floating the substrate, well-behaved conductance data is obtained despite a large parasitic C_{GC} existing. Fig. 4.1 (b1) and (b2) show that grounding the substrate removes the parasitic C_{GC} yet induces negative conductance especially in high accumulation. Fig. 4.1 (c1) and (c2) show that even after open/short re-compensation the grounding effect induces additional $G/A\omega$ and C_{GC} noise previously not present. This noise is more apparent on the $G/A\omega$ versus V_G and C_{GC} versus V_G plots.

These results show that the measurement technique can influence the results presented by the $C-V$ tool. It affects both the capacitance and conductance results, which last for at least three re-compensations thereafter. One should note that this test was done on the leakiest architecture (D1) and that it was done only once to prove the effect. $C-V$ units closest to the Keithley exhibited this effect. Specifically, the entire conductance curve was shifted negative (not just that in high accumulation and partially in high inversion) and in some cases the $C-V$ curve was shifted towards the negative regime as well. Data shows that this effect tends to be manifested to a greater degree in conductance than in capacitance, indicating that conductance extraction is more sensitive to tool variation than capacitance extraction.

From Fig. 4.1 one should note that the conductance of (b1) changes sharply with both applied frequency, due to the ability of traps to respond to the measurement frequency, and applied gate bias, due to the activation of channel generation ($0 \text{ V} \leq V_G \leq \sim 0.5 \text{ V}$) and gate-induced-junction leakage in high accumulation. The negative conductance indicates the presence of an extremely low impedance as observed by the low probes. Specifically, current is flowing out of the low probes and into ground.

It is believed that the discontinuities observed at 100 kHz for $G/A\omega$ and C_{GC} in Fig. 4.1 (b1, b2) result from a mismatch in the measured verses expected impedance values at the frequency range of interest. Specifically, a low impedance is measured when a high impedance is expected by the ranging resistor at the frequency range of interest, resulting in a slip or discontinuity in the impedance data used to calculate conductance and capacitance [2]. There are 7-10 measurement ranges present in the $C-V$ unit to measure impedance from low to high values as shown in Fig. 4.2 [2].

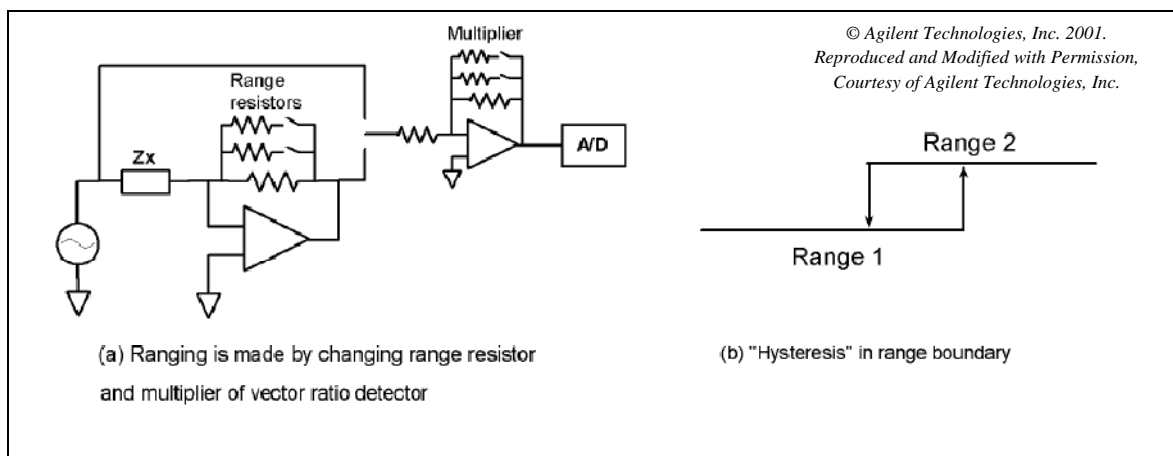


Fig. 4.2: Ranging function adopted from [2]. The ranging function is used to measure impedance from low to high values in the auto-balancing bridge method.

This ranging function is present in this $C-V$ unit and allows the instrument to automatically select the appropriate impedance range of the DUT at each frequency

during measurement [2]. This ensures that the maximum signal level is fed to the analog-to-digital (A/D) converter thereby providing the highest signal-to-noise ratio for measurement accuracy [2]. Its fault during C_{GC} ground helps explain why the data of Fig. 4.1 (c1) and (c2) is more noisy after grounding than before grounding and helps explain why one could observed slips in the conductance data during measurement. Future work is needed to determine if there is a need to correct for any compensation error induced during grounding. The manual indicates one should set the impedance range manually to the range that measures the higher impedance [2]. Further research is required to perform this task.

4.1.1. Negative Conductance-Capacitance Effect

After discovering the source of slips and negative conductance—Ge PMOS substrate grounding during C_{GC} measurement—the investigator sought to determine how much variation existed in $G/A\omega$ and C_{GC} when comparing results before grounding to results after grounding. Fig. 4.3 (a1) was created by subtracting $G/A\omega$ before grounding from $G/A\omega$ after grounding. Fig. 4.3 (a2) was created by subtracting C_{GC} before grounding from C_{GC} after grounding. The insets of each are plotted versus gate voltage. Fig. 4.3 (b1) is a contour plot of (a1) where $G/A\omega$ is in arbitrary units and (b2) is a contour plot of (a2) where C_{GC} is in arbitrary units.

First, note in Fig. 4.3 (a1) that the difference in $G/A\omega$ trends negative to both lower frequencies and higher gate voltage and trends positive to both higher frequencies and negative gate voltages. This artifact results in a stretching of the $G/A\omega$ plot by nearly $0.4 \mu\text{S}\cdot\text{sec}/\text{cm}^2$ tip-to-tip, which is relatively large considering the $0\text{-}3 \mu\text{S}\cdot\text{sec}/\text{cm}^2$ range

observed in Fig. 4.3 (a1). This stretching effect is shown in Fig. 4.3 (b1) using arbitrary units for graphical purposes only.

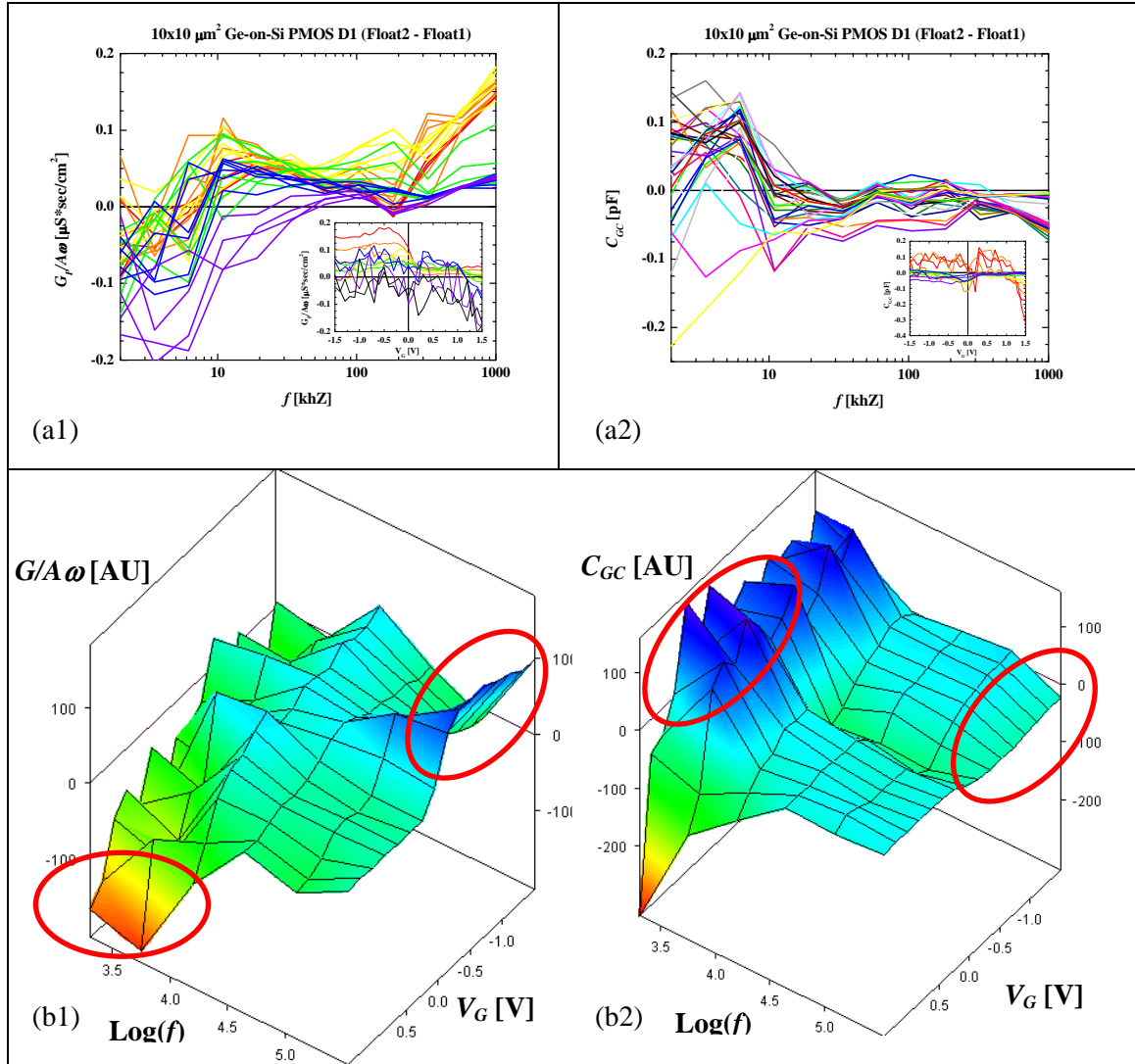


Fig. 4.3: Difference calculation for (a1) $G/A\omega$ and (a2) C_{GC} . Floating substrate data subtracted from floating-substrate-after-grounding. Contour plots (b1) $G/A\omega$ [arbitrary units] and (b2) C_{GC} [arbitrary units] versus $\text{log}(\text{frequency})$ and gate voltage [V].

Second, note in Fig. 4.3 (a2) that the difference in C_{GC} trends positive to both lower frequencies and lower gate voltages and trends negative to both higher frequencies and higher gate voltages. This artifact results in a stretching of the C_{GC} plot by nearly

0.25 pF, which is relatively large when considering both the 0-2 pF range observed in Fig. 4.3 (a2) and the expected fF overlap capacitance magnitude. This stretching effect is shown in Fig. 4.3 (b2) using arbitrary units for graphical purposes only. One should note that these observations are relevant for this study only and further information is needed to quantify the extent and degree of this behavior if any. The results of this chapter show that grounding the Ge-PMOS substrate during C_{GC} measurement should be avoided and also reveals a realm of future work: namely, possible removal of this Ge-PMOS C_{GC} grounding artifact observed as a possible distortion of the conductance and capacitance curves.

References for Chapter 4

- [1] D. Schroder. 1998. *Semiconductor Material Device Characterization Second Edition*. USA: John Wiley & Sons, Inc.
- [2] Agilent Technologies Inc. 2006. *Agilent Technologies Impedance Measurement Handbook July 2006*. USA. Agilent Technologies, Inc. 2000-2006. <http://www.agilent.com> (accessed March 25, 2008).

Chapter 5

IMEC Germanium PMOSFET Source-Drain Leakage

Throughout the last three decades, technological innovation has resulted in a steady reduction in MOSFET dimensions. This came to first light in 1972 when Robert Dennard proposed the Constant Electric Field scaling criterion: a self-consistent methodology for scaling the lateral dimensions, vertical dimensions, doping levels, and operating voltages (keeping the source-to-drain electric field constant) of silicon-based MOSFETs so as to avoid short-channel effects. Officially adopted by industry in 1974—when Robert Dennard demonstrated scaling to the 0.5 μm node—and used to date, this scaling criterion has provided silicon-based CMOS technology of higher density and performance. Current research shows, however, that continued scaling to the nanometer regime is resulting in larger leakage currents, leading to greater power dissipation in CMOS circuit technology [1].

As has been discussed, researchers are investigating the replacement of Si-PMOS with Ge-PMOS in an attempt to achieve the 2109 $\mu\text{A}/\mu\text{m}$ drive current forecast at the 32 nm node [2]. Germanium has half the bandgap of silicon (0.66 eV for Ge versus 1.12 eV), has an intrinsic carrier concentration three orders of magnitude greater than silicon ($2.0 \times 10^{13} \text{ cm}^{-3}$ versus $1.0 \times 10^{10} \text{ cm}^{-3}$), and when utilized in MOS technology often exploits exotic high- κ dielectric gate stacks. This combination makes germanium more susceptible to typical current leakage mechanisms observed in silicon CMOS technology. As a result, current leakage consideration of these new Ge-PMOS devices is of great concern.

In this study, the reverse bias p/n junction leakage mechanism of the Ge-PMOS source-and-drain are compared between D1, G3, and J2 architectures containing gate lengths of 10 μm and gate widths of 10 μm . A MOS-Gated-Diode measurement is developed and the leakage mechanisms are compared (in inversion, depletion, and accumulation) for these devices. Low gate-oxide tunneling leakage (in the pA range) was confirmed for all architectures and was subsequently ignored. The MOS-Gated-Diode current leakage mechanisms are confirmed for the best device through activation energy E_A extraction. Extraction of E_A indicated which current components dominated each mechanism. To better understand the Ge-PMOS current leakages observed in this study, one must first identify the seven transistor leakage mechanisms and understand why three of them are of interest.

5.1. Transistor Leakage Mechanisms

Research indicates that there are six main transistor leakage mechanisms as shown in Fig. 5.1: p/n junction reverse-bias current leakage (I_1); subthreshold leakage (I_2); gate-oxide tunneling leakage (I_3); hot carrier substrate-to-gate injection (I_4); gate-induced drain leakage (I_5); punchthrough (I_6) [1]. In this study there are seven main transistor leakage mechanisms. The seventh is due to surface generation leakage under the gate during channel depletion.

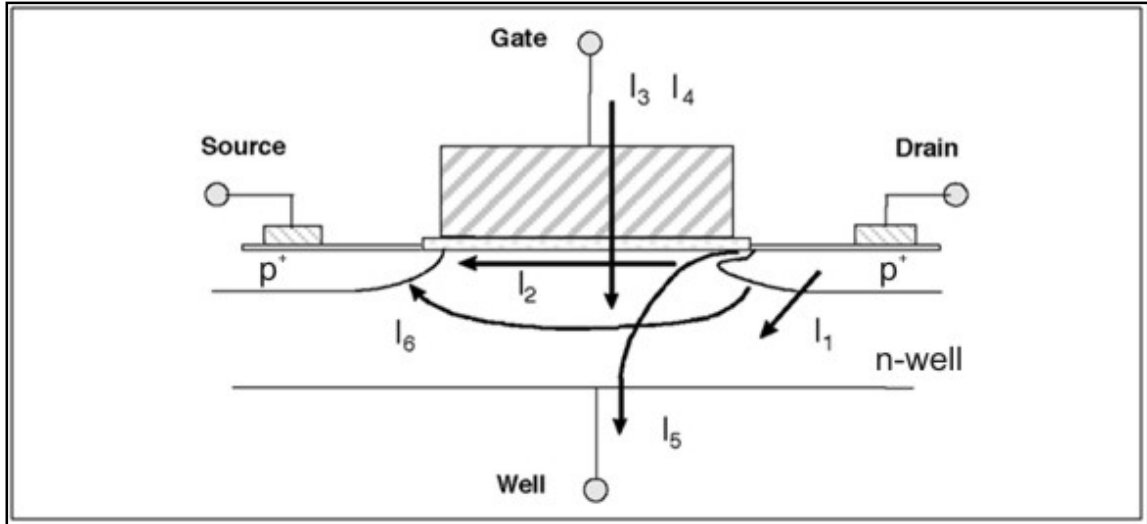


Fig. 5.1: The six transistor current leakage mechanisms according to research adapted from [1].

This study focuses on the primary leakage mechanisms observed in Ge PMOS while performing the gate-to-channel capacitance (C_{GC}) measurement. During the C_{GC} measurement the source and drain are shorted together and kept at ~ 0 V while the gate is swept from accumulation to inversion and vice versa. The C_{GC} is measured between the gate-contact and source/drain-contact regions. As a result the leakage mechanisms of interest do not involve current transport from source to drain. A DC MOS configuration equivalent to the AC MOS configuration used during C_{GC} analysis has been developed in this study and is called a MOS Gated Diode configuration. In the MOS Gated Diode configuration, the source and drain are shorted together and reverse-biased to the well while sweeping the gate. Current is measured from both the gate probe and source/drain probe into the well.

The MOS Gated Diode configuration in conjunction with the fact that gate-oxide tunneling leakage was found to be in the pA range results in three main leakage mechanisms of concern: the reverse bias p/n junction (source/well and drain/well)

leakage due to generation ($2I_1$), surface generation leakage under the gate (I_7) during channel depletion, and field induced junction leakage ($2I_5$) during channel accumulation.

These leakage mechanisms are shown in Fig. 5.2.

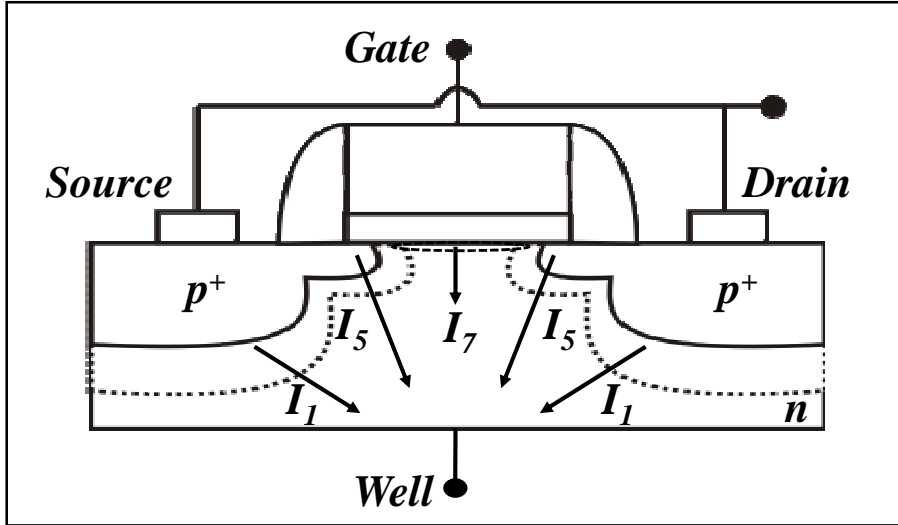


Fig. 5.2: The three primary transistor current leakage mechanisms observed in this study using the MOS Gated Diode configuration. Figure is based on [1].

To better understand the leakage components present in each mechanism, this section will focus on individual explanation of reverse-bias current leakage (I_1), surface generation leakage (I_7) during channel depletion, and gate-induced drain leakage (I_5) during channel accumulation. These are the dominant leakage mechanisms (in and beyond the μA range) examined in this study which contributed to the observed C_{GC} deviations.

5.1.1. P/N Junction Reverse Bias Leakage (I_1)

During typical MOSFET operation, the drain and source junctions are reverse biased to the well [1]. This results in a reverse-bias p/n junction leakage (I_1). Let us assume that each p/n junction contains moderate doping and reverse bias (so as to avoid tunneling and avalanche), is dominated by area leakage, and exhibits no photogenerated

recombination-generation (G_L) current. Such a p/n junction will contain two main leakage components in reverse bias: the first, according to ideal diode theory, is a minority carrier drift-diffusion leakage current ($J_{Drift-Diff}$) near the edge of the p/n junction depletion region [1, 3-7], and the second, according to Shockley-Read-Hall (SRH) theory, is a thermal electron-hole pair recombination-generation leakage current (J_{SRH}) within the p/n junction depletion region [1, 3-7]. This is shown below in Eq. 5.1, Eq. 5.2, and Eq. 5.3, respectively.

$$J_R = J_{Drift-Diff} + J_{SRH} \quad (5.1)$$

$$J_{Drift-Diff} = J_{Diff} \left(e^{V_A/\varphi} - 1 \right); \quad \varphi = \frac{kT}{q} \quad (5.2)$$

$$J_{SRH} = \frac{qn_i}{2\tau_G} W \left[\frac{\left(e^{V_A/\varphi} - 1 \right)}{\left(1 + \frac{V_{bi} - V_A \sqrt{\tau_N \tau_P}}{\varphi} e^{V_A/2\varphi} \right)} \right] \quad (5.3)$$

where,

$$J_{Diff} = q \left(\frac{D_N n_i^2}{L_N N_A} + \frac{D_P n_i^2}{L_P N_D} \right) \quad (5.4)$$

$$\frac{D_N}{L_N} = \sqrt{\frac{\left(\frac{kT}{q}\right)\mu_N}{\tau_N}} \quad \frac{D_P}{L_P} = \sqrt{\frac{\left(\frac{kT}{q}\right)\mu_P}{\tau_P}} \quad (5.4a)$$

$$n_i = \sqrt{N_C N_V} \exp\left(-E_G/2kT\right) \quad (5.4b)$$

$$\tau_G = \frac{1}{2} \left[\tau_P e^{(E_T - E_i)/kT} + \tau_N e^{(E_i - E_T)/kT} \right] \quad (5.4c)$$

$$W = \left[\frac{2K_S \epsilon_0}{q} \left(\frac{N_A + N_D}{N_A N_D} \right) (V_{bi} - V_A) \right]^{1/2} \quad (5.4d)$$

$$V_{bi} = \phi \ln \left(\frac{N_A N_D}{n_i^2} \right) \quad (5.4e)$$

In reviewing Eq. 5.1-5.4e, J_{Diff} is the diffusion current density, V_A is the applied bias, k is Boltzmann's constant, T is temperature in Kelvin, q is electronic charge, A is the diode area, D_N and D_P are the electron and hole diffusion coefficients, respectively, L_N and L_P are the minority carrier diffusion lengths for electrons and holes, respectively, N_A and N_D are the total number of acceptors and donors, respectively, n_i is the intrinsic carrier concentration, E_i is the intrinsic energy level, E_G is the bandgap, μ_P and μ_N are the minority carrier hole and electron mobilities, respectively, τ_P and τ_N are the minority carrier hole and electron lifetimes respectively, N_C and N_V are the effective density of states for the conduction and valance band, respectively, τ_G is the generation lifetime, W is the depletion width, V_{bi} is the built-in potential, and E_T is the interface trap level energy.

Reverse biasing Eq. 5.2-5.3 beyond $-3kT/q$ results in a reverse bias current density dependent on diffusion as shown in Eq. 5.5 and on generation as shown in Eq. 5.6.

$$J_{Driff-Diff} = J_{Diff} \left(e^{V_A/\phi} - 1 \right) \xrightarrow{V_A < -3\phi} -J_{Diff} = -qn_i^2 \left(\frac{D_N}{L_N N_A} + \frac{D_P}{L_P N_D} \right) \quad (5.5)$$

$$J_{SRH} = \frac{qn_i}{2\tau_G} W \left[\frac{\left(e^{V_A/\phi} - 1 \right)}{\left(1 + \frac{V_{bi} - V_A \sqrt{\tau_N \tau_P}}{\phi} e^{V_A/2\phi} \right)} \right] \xrightarrow{V_A < -3\phi} -J_{Gen} = -\frac{qn_i}{2\tau_G} W \quad (5.6)$$

The final simplified expression for reverse-bias p/n junction leakage is shown in Eq. 5.7.

$$J_R|_{V_A < -3\phi} = J_{Diff} + J_{SRH} = -qn_i^2 \left(\frac{1}{N_D} \sqrt{\frac{(kT/q)\mu_P}{\tau_P}} + \frac{1}{N_A} \sqrt{\frac{(kT/q)\mu_N}{\tau_N}} \right) - qn_i \frac{W}{2\tau_G} \quad (5.7)$$

From simplification it is quite obvious that the drift and recombination currents decay to zero when sufficient reverse bias is applied ($V_A < -3kT/q$ for the Ge p/n diodes). In reviewing Eq. 5.7 one should note the following:

- i. J_R is highly semiconductor type-dependent due to the $J_{Diff} \propto n_i^2$ and $J_{SRH} \propto n_i$ dependence
 - a. At 300K the n_i of Si is $1 \times 10^{10} \text{ cm}^{-3}$ and that of Ge is $2.0 \times 10^{13} \text{ cm}^{-3}$
 - b. The reverse bias diffusion current density J_{Diff} for Ge diodes is expected to be 10^6 times larger than that observed in Si diodes [3]
- ii. The relative significance of J_{Diff} and J_{SRH} tends to be semiconductor-type dependent due to $J_{Diff} \propto n_i^2$ versus $J_{SRH} \propto n_i$
 - a. Theoretically, for Si and GaAs p/n diodes with low n_i , J_{SRH} should dominate
 - b. Theoretically, for Ge p/n diodes with high n_i , J_{Diff} should dominate
- iii. J_R is inversely proportional to τ_N ; τ_P ; τ_G
- iv. Since $J_{Diff} \propto n_i^2 \propto \exp(-E_G/kT)$ and $J_{SRH} \propto n_i \propto \exp(-E_G/2kT)$
 - a. One can determine the dominant leakage component by measuring the reverse bias leakage current versus temperature

- b. Extracting the slope of $\ln|J_R/|$ versus $1/kT$ at low and high temperatures results in activation energy extraction of the dominant leakage current component
- c. At higher temperatures J_{Diff} is expected to dominate due to n_i^2

Of main interest is the non-ideal generation current component present in the p/n junction depletion region of I_1 and present during channel depletion (I_7).

5.1.2. Surface Generation Leakage (I_7)

Surface Generation Leakage (I_7) during channel depletion is dominated by a generation component ($J_{SRH-Chan}$) and requires that the source or drain be reverse biased to the well. An explanation of generation leakage is needed. In an ideal case, the energy band diagram of a perfect single crystal semiconductor consists of a conduction and valance band with no energy levels in between. Practically, however, single crystal semiconductors contain foreign atoms and crystalline defects—metallic impurities; crystal imperfections; dislocations; stacking faults; precipitates; vacancies; interstitials—which perturb the crystal periodicity. As has been discussed, dislocations exist in the relaxed-germanium on silicon substrate used to fabricate the Ge-PMOS of this study. When this occurs, discrete energy levels are introduced into the bandgap as shown in Fig. 5.3.

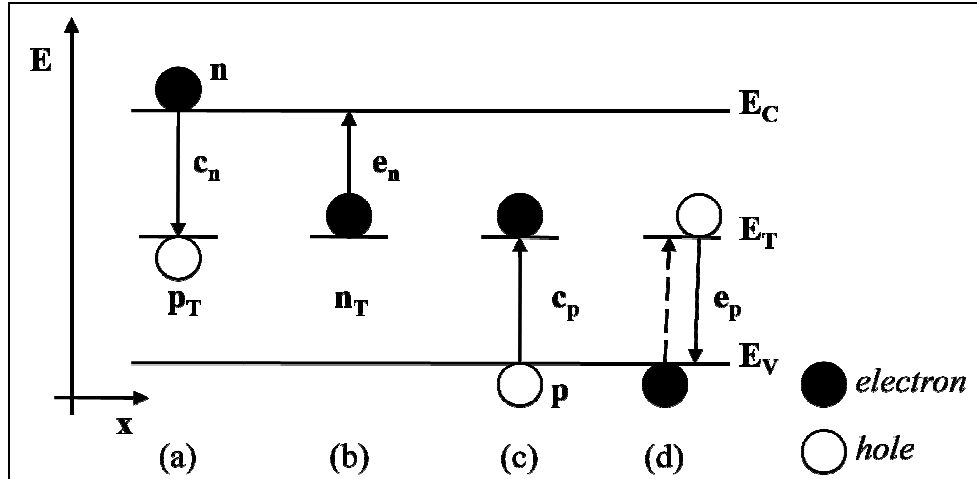


Fig. 5.3: Electron energy band diagram for Ge with deep-level impurities detailing: (a) electron capture; (b) electron emission; (c) hole capture; (d) hole emission. Adapted from [8].

Each of the four lines at the discrete energy level E_T in Fig. 5.3 represents a defect. When such defects exist close to mid gap they are referred to as recombination-generation (R-G) centers. These R-G centers tend to lie deep within the bandgap, acting as recombination centers when there are an excess of carriers in the semiconductor and as generation centers when there are a depletion of carriers in the semiconductor. When the carrier density drops below its equilibrium value n_i ($np < ni^2$)—such as in the reverse-biased space-charge region of a p/n junction or as in the depleted semiconductor-surface of a MOS capacitor—generation dominates.

Ideally in Fig. 5.3 one may view recombination as event (a) followed by event (c) and generation as event (b) followed by event (d) [5]. A third event exists in which neither generation or recombination occurs: this is called a trapping event and is considered event (a) followed by (b) or event (c) followed by (d) [5]. The ease in which this process occurs can be affected by the presence of large electric fields common in

highly doped and abrupt p/n junctions ($E_{max} > 1 \times 10^6$ V/cm) [1,6]. Generation current enhancement is shown in Fig. 5.4.

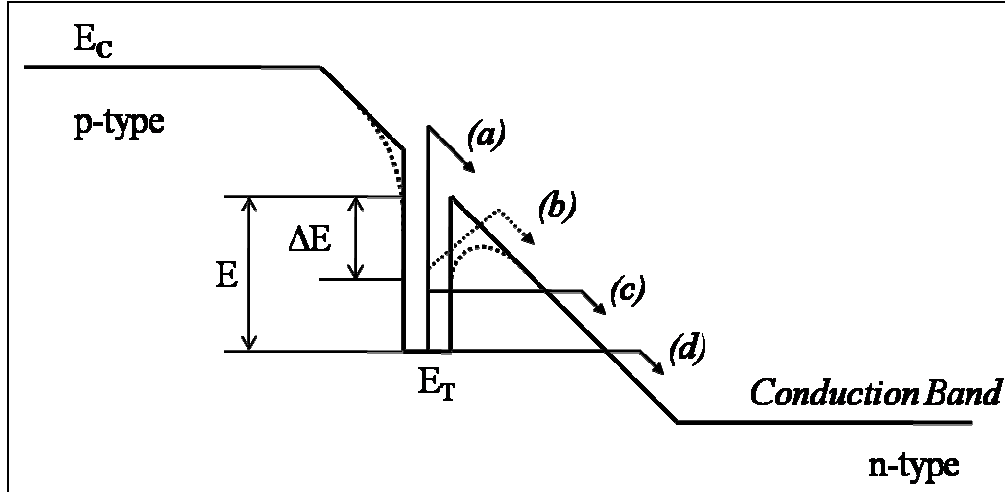


Fig. 5.4: Electron generation mechanisms adopted from [8] for (a) SRH, (b) Poole-Frenkel (PF), (c) Phonon-assisted tunneling (PAT), (d) Trap-to-band tunneling (TBT). The dashed line indicates the Coulombic Well and the solid line the Dirac well [8]. The energy difference E is the energy difference between the trap state and the conduction band; ΔE is the energy difference due to Poole-Frenkel barrier lowering [8].

In this study a SRH generation current J_{SRH} will be identified when it occurs approximately $E_G/2$ within the bandgap (activation energy extraction will help determine this). R-G centers behave as discussed when near mid gap. When a generation current occurs at less than $E_G/2$ it will be identified as a trap assisted leakage (J_{TAL}) for it could be assisted by the Poole-Frenkel effect (lowering of the Coulombic well), phonon-assisted tunneling (PAT), or trap-to-band tunneling (TBT). TBT requires a larger electric-field than PAT [8].

5.1.3. Gate Induced Drain Leakage (I_5)

Gate-induced drain leakage (GIDL) I_5 is a leakage mechanism that results from inversion of the drain extension by the gate overlap region during channel accumulation resulting in the conduction of minority carriers from the drain to the channel through

PAT, TBT, BTBT, and in the extreme case avalanche [1,10]. A figure illustrating GIDL is shown in Fig. 5.5 in inset (b): Gate-Induced-Junction leakage (GIJL) is expected to be twice the GIDL.

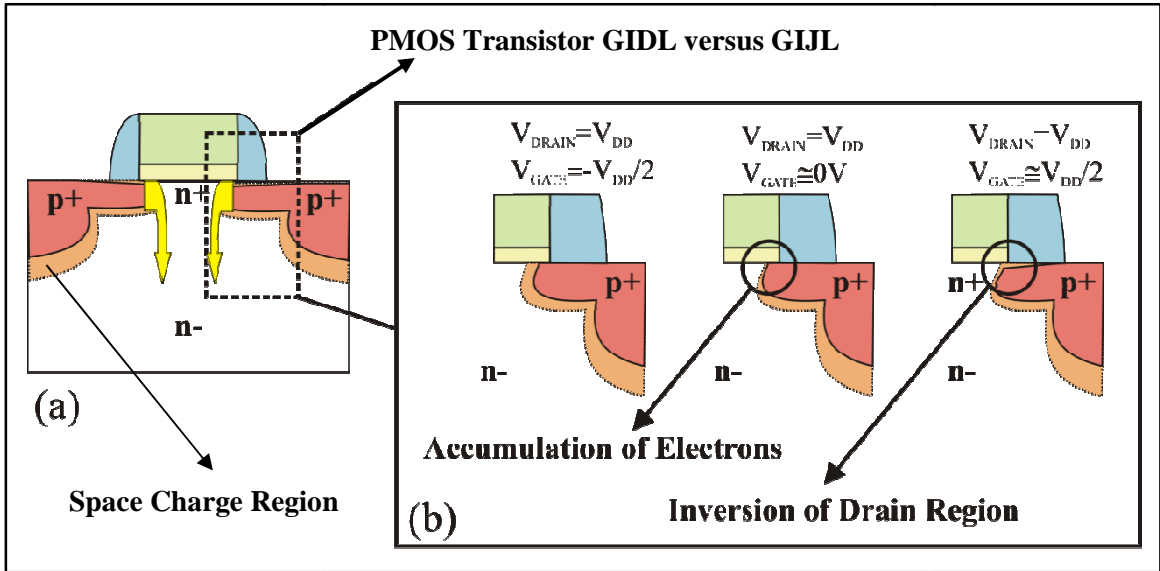


Fig. 5.5: Gate-Induced Junction Leakage (GIJL) versus Gate-Induced Drain Leakage (GIDL). (GIJL) inset (a) is twice the gate-induced drain leakage (GIDL) of inset (b) provided the source and drain are shorted to one another and considered identical in nature. Adapted from [10].

For GIDL to happen the drain must be reverse biased to the well. In the case of Ge-PMOS, as the gate is biased to form an accumulation layer in the channel, majority carrier electrons are attracted to the channel surface forming a n+ region. This n+ region behaves as a region more highly doped than the underlying substrate [1]. As majority carriers continue to accumulate at the channel surface the depletion width at the surface separating the channel from the drain begins to decrease as shown in Fig. 5.5: GIDL is highlighted in inset (a) and shown in detail in inset (b). This can be shown through Eq. 5.4d with fixed applied bias. As either side of the p/n junction appear more highly

doped, the $N_D N_A$ product in the denominator increases rapidly resulting in a rapid decrease in the depletion width W .

As majority carriers continue to accumulate in the channel, the surface-depletion width separating the channel from the drain continues to decrease resulting in an increase in the electric field between them [1]. While this is occurring the gate region begins to deplete the drain region directly below it. This overlap region can become inverted in the worse case, which causes even more field crowding, thereby increasing the possibility of tunneling and in the extreme case avalanche [1]. When the drain is inverted enough and the tunneling probability great, the minority n^{++} electrons created in the drain tunnel or avalanche laterally to the n^+ region in the channel after which they are swept to the n -region of the well.

The effect of GIDL with respect to drain/well doping is complicated. Research shows that GIDL is worse for devices containing moderate doping where the electric field between the drain-well and the depletion width tunneling volume are considerable [1]. This occurs for moderately doped non-abrupt p/n junctions. In this study, the source and drain are shorted together and swept through reverse bias, while stepping the gate to high accumulation. The observed effect is called Gate-Induced-Junction Leakage (GIJL) as shown in Fig. 5.5 (a) because it occurs at the surface of both the source/well and drain/well junctions. Both source and drain are identical and as a result GIJL (J_{GIJL}) is considered to be twice the GIDL (J_{GIDL}) of each device.

5.2. MOS-Gated-Diode and Expected Trend

Now that p/n junction leakage (I_1), surface generation leakage (I_7) during channel depletion, and GIDL (I_5) during channel accumulation have been discussed, the reverse-bias leakage mechanisms expected during MOS-Gate-Diode measurement as a function of V_G and, as a result, expected during C_{GC} can be listed. One should note that to effectively model the devices in this study, one would have to modify the multiplication coefficient of each component so as to account for the multiple source and drain contacts due to metallization as was discussed in Chapter 1. The devices in this study will not be modeled. As a result, MOSFETs containing a single source and single drain are considered for simplicity.

$$J_R(V_G)|_{V_A < -3\phi} = 2J_{Diff} + 2J_{SRH}\Gamma + J_{SRH-Chan}(V_G) + J_{GIDL}(V_G) \quad (5.8)$$

Notice from Eq. 5.8 at fixed V_A ($V_A < -3\phi$ and one would expect all leakage components to increase in absolute magnitude with increasing reverse bias) that the J_{DIFF} and J_{SRH} are independent of V_G ; that a multiplication factor Γ has been used to account for additional generation current due to high electric field inducing FP, PAT, and TBT mechanisms [8]; that $J_{SRH-Chan}$ is dependent on V_G and will only occur during channel depletion; that J_{GIDL} is dependent on V_G and will only occur in high accumulation. The MOSFET in inversion, depletion, and accumulation and the resulting current is illustrated in Fig. 5.6 at fixed reverse bias.

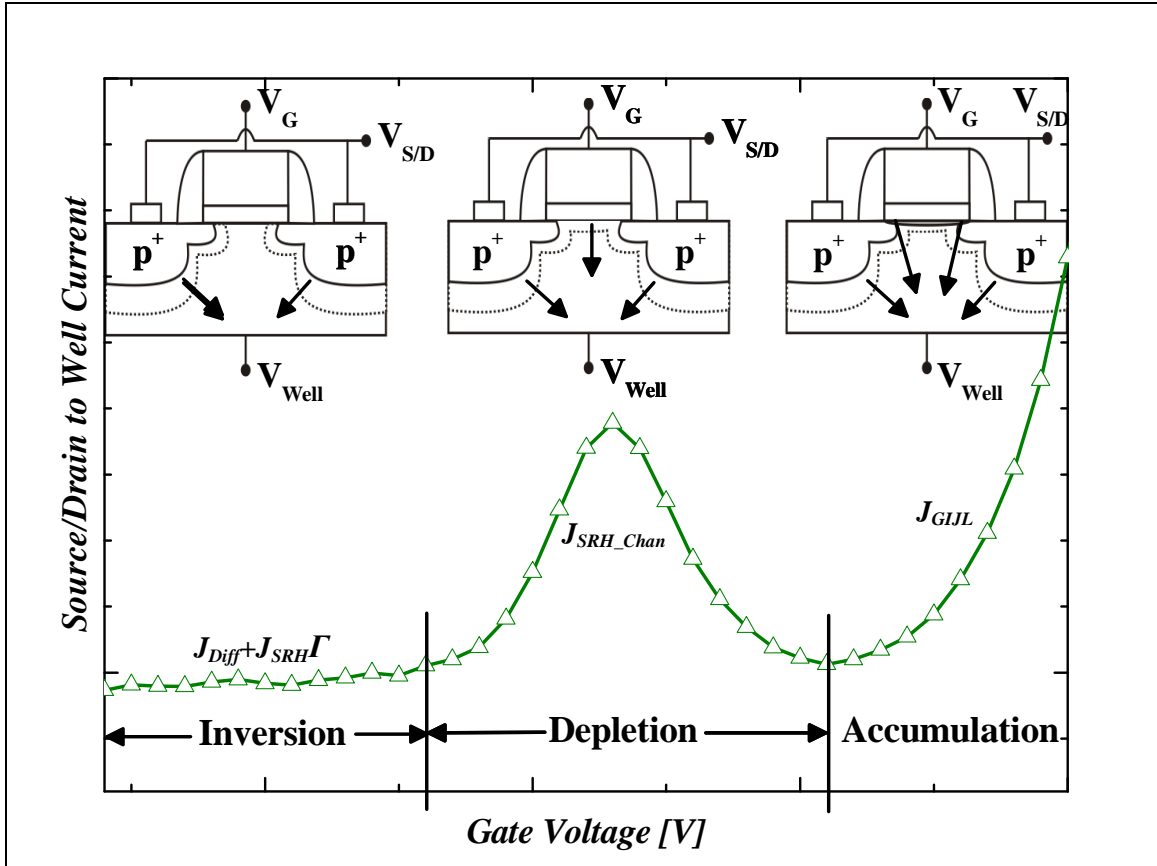


Fig. 5.6: Three regions of operation for MOS-Gated-Diode leakage.

5.3. Experimental Results

5.3.1. Source/Drain-to-Well Reverse Bias Leakage ($2I_1$)

Experimentally, the reverse bias diode current I was evaluated for three $10 \mu\text{m} \times 10 \mu\text{m}$ Ge PMOS architectures (D1; G3; J2) by shorting the source and drain together, sweeping the source/drain-to-well from 0.2 V to -1.0 V in increments of 20 mV, and measuring the resulting $I_{D\&S\text{-}Well}$ current using a Keithley K4200 parameter analyzer. The results of this analysis are shown in Fig. 5.7.

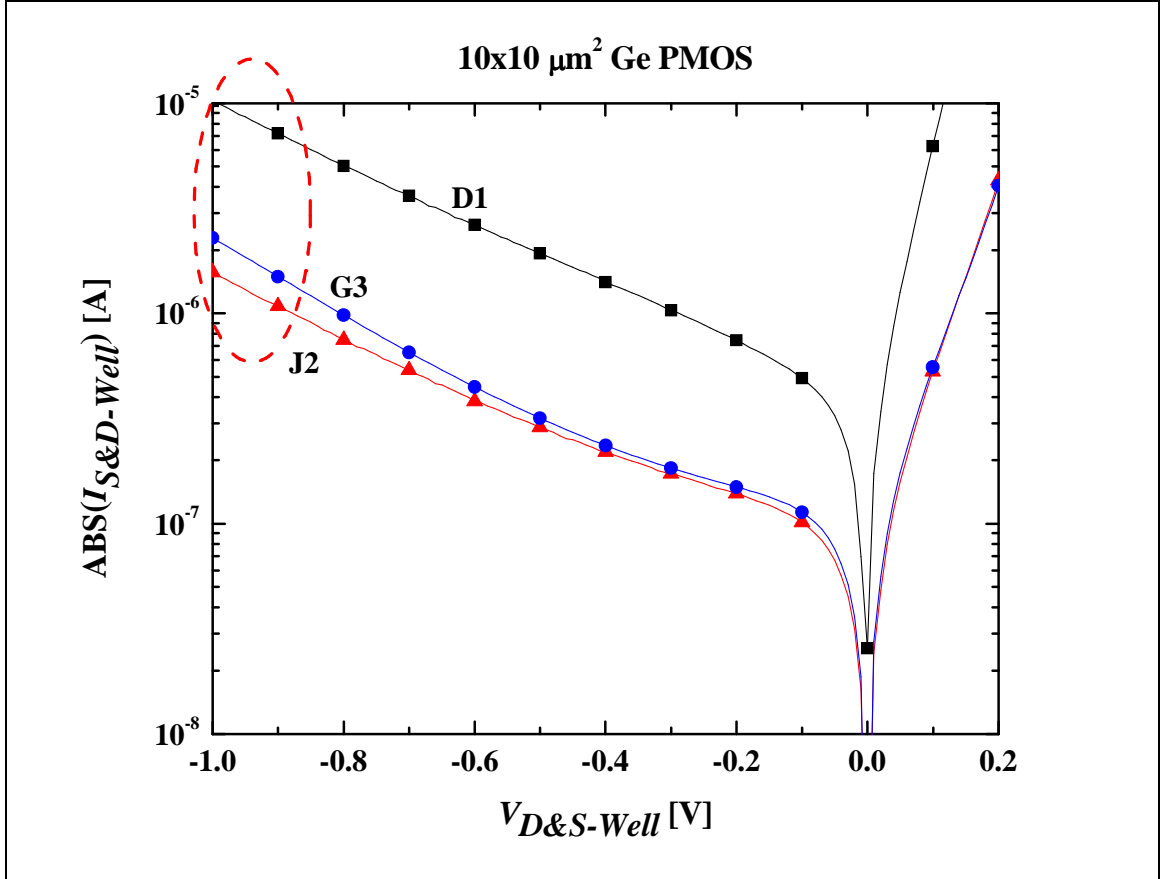


Fig. 5.7: Reverse-bias source/drain-to-well leakage of three 10 $\mu\text{m} \times 10 \mu\text{m}$ Ge PMOS architectures D1, G3, and J2.

Note that the absolute reverse bias $I_{S\&D-Well}$ current, is approximately one order of magnitude lower for the J2 architecture than the D1 architecture. It also shows that the leakage is more than source/drain area-dependent: the G3 and J2 architectures have the same source/drain area and perimeter, and the same contact area. The only difference between J2 and G3 is the source/drain contact distance from the gate region—1.5 μm for J2 versus 3.0 μm for G3 as illustrated in Chapter 1.

The reverse-bias source/drain-well leakage current of J2 is slightly greater than 1 μA in magnitude at a reverse bias of -1.0 V. This is six orders of magnitude greater than similar silicon CMOS technologies, which tend to exhibit reverse-bias leakage

currents in the pA range. Fig. 5.7 reveals that when performing typical C_{GC} analysis, the J2 architecture should be sought. This figure also raises a question: what is the dominant leakage component of the J2 architecture? Why does the source/drain contact distance from the gate affect the reverse bias leakage?

5.3.2. Gate-Induced Junction Leakage ($2I_5$)

Gate-induced-junction leakage analysis was performed on the worse and best architectures observed in the leakage results shown in Fig. 5.7 of this study: architectures D1 and J2, respectively. Similar $10\ \mu\text{m} \times 10\ \mu\text{m}$ Ge PMOS devices as shown in Fig. 5.7 were analyzed. The source and drain were shorted together and swept from 0.2 V to -1.0 V in increments of 20 mV while stepping the gate voltage from 0 V to 1.5 V in increments of 0.5 V using a Keithley K4200 parameter analyzer. The results are shown in Fig. 5.8.

The reverse-bias leakage of each device increases as gate voltage increases. This behavior is easily observed at reverse biases as low as 100 mV. Second, the fact that the GJL increase is more rapid for the J2 architecture than the D1 architecture indicates that the D1 architecture may already contain a significant amount of tunneling or avalanche leakage. Third, at a high source/drain-to-well reverse bias of 1.0 V the observed leakage currents for D1 and J2 are very close at 935 μA , and 769 μA , respectively indicating that J2 barely outperforms D1 in extreme reverse bias case. One should note that typical MOS operation of these devices occurs at a drain/well reverse bias of 1.5 V [9]!

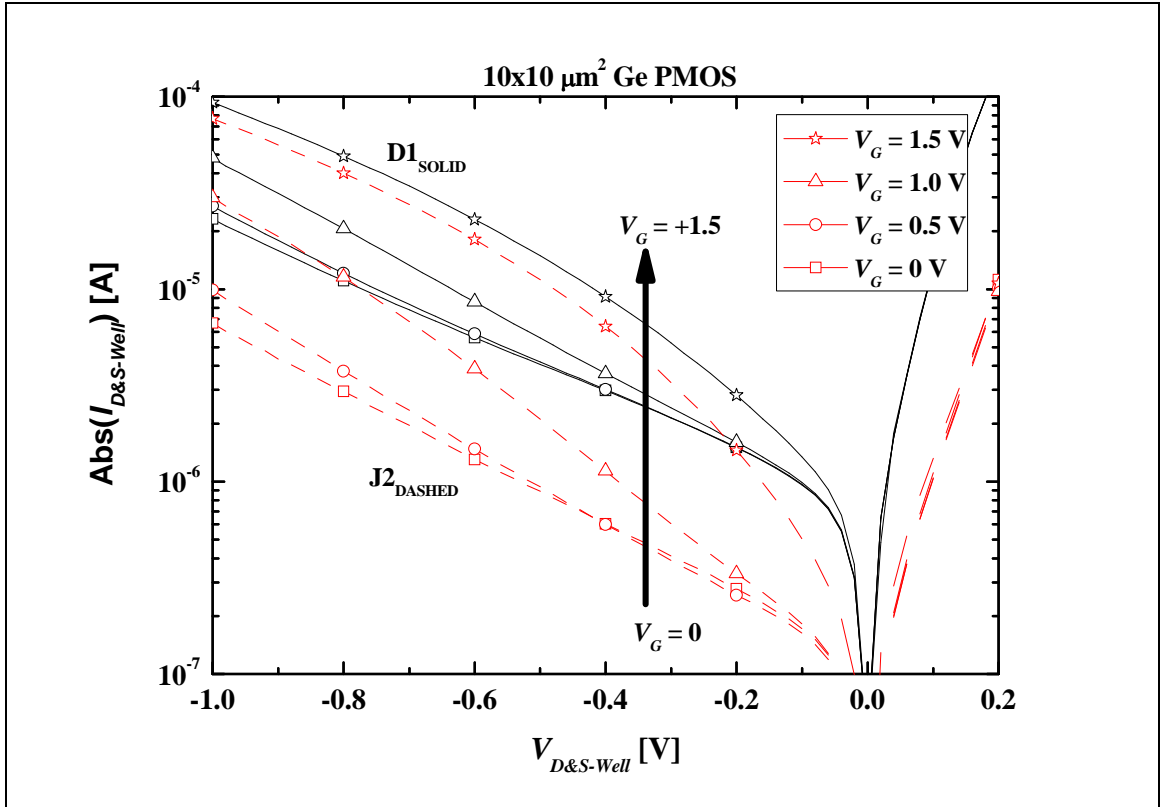


Fig. 5.8: GIJL of two $10\ \mu\text{m} \times 10\ \mu\text{m}$ Ge PMOS devices: D1 and J2. The source and drain are shorted together and swept from $-1.0\ \text{V}$ to $0.2\ \text{V}$ while stepping the gate from $0\ \text{V}$ to $1.5\ \text{V}$. Note that as the V_G increases the reverse bias source/drain-to-well leakage increases.

5.3.3. MOS-Gated-Diode Results

Gate-induced-junction leakage has been identified in Fig. 5.8. Of interest is the source-and-drain leakage at fixed $V_{D\&S\text{-}Well}$ as a function of gate bias. This was evaluated on $10\ \mu\text{m} \times 10\ \mu\text{m}$ Ge PMOS devices architectures D1, G3, and J2. The source and drain were shorted together and reverse biased at $100\ \text{mV}$ while sweeping the gate voltage from $-1.5\ \text{V}$ to $1.5\ \text{V}$ in increments of $0.1\ \text{V}$ using a Keithley K4200 parameter analyzer. The results are shown in Fig. 5.9.

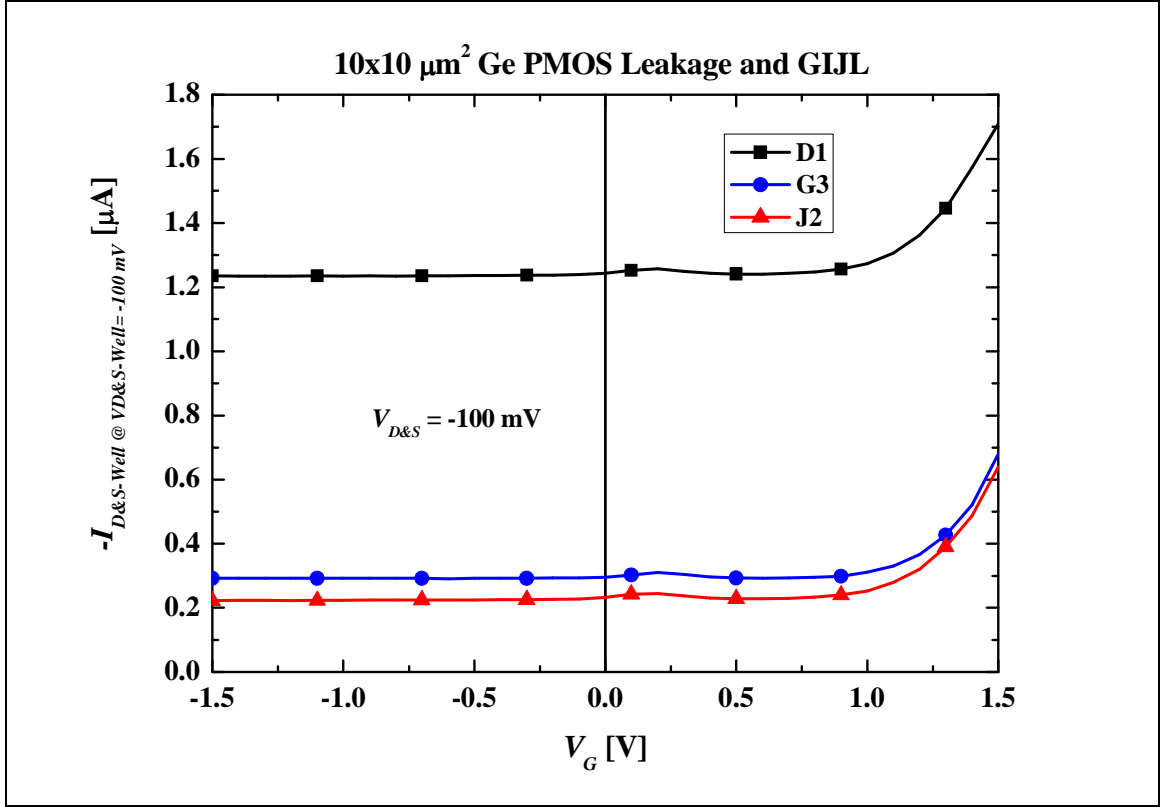


Fig. 5.9: MOS-Gated-Diode configuration showing $I_{D\&S-Well}$ leakage and GIJL.

Note again from Fig. 5.9 that the $I_{D\&S-Well}$ leakage for $D1 > G3 > J2$ for all values of V_G . When comparing J2 architecture to D1 architecture the leakage difference is again about one order of magnitude. Note that the spread between G3 and J2 is greater in inversion and decreases in the GIJL region as V_G approaches 1.5 V. From Fig. 5.9 one can observe the constant leakage trend from high inversion ($V_G = -1.5$ V) to $V_G = 0$ V after which the leakage tends to increase rapidly due to channel depleted surface generation and to drop when entering accumulation. The location of the peak within this transition indicates the beginning of transition from inversion-to-depletion/depletion-to-accumulation: $V_{Peak} = \sim 0.15$ V. Flatband voltage can be determined to be $V_{FB} = \sim 0.5$ V. GIJL takes off rapidly after 1.0 V for all architectures. It is clear that much leakage exists

between the source-well and drain-well junctions. One should ask: how little reverse bias is needed to avoid this leakage effect? Is a reverse bias of 100 mV too much?

To answer this question the most stable (less leaky) J2 architecture was analyzed. The source and drain were shorted together and reverse biased to the well. The reverse bias was then stepped from 100 mV to 10 mV in steps of 10 mV while sweeping the gate voltage from -1.5 V to 1.5 V in increments of 0.1 V using a Keithley K4200 parameter analyzer. The results are shown in Fig. 5.10.

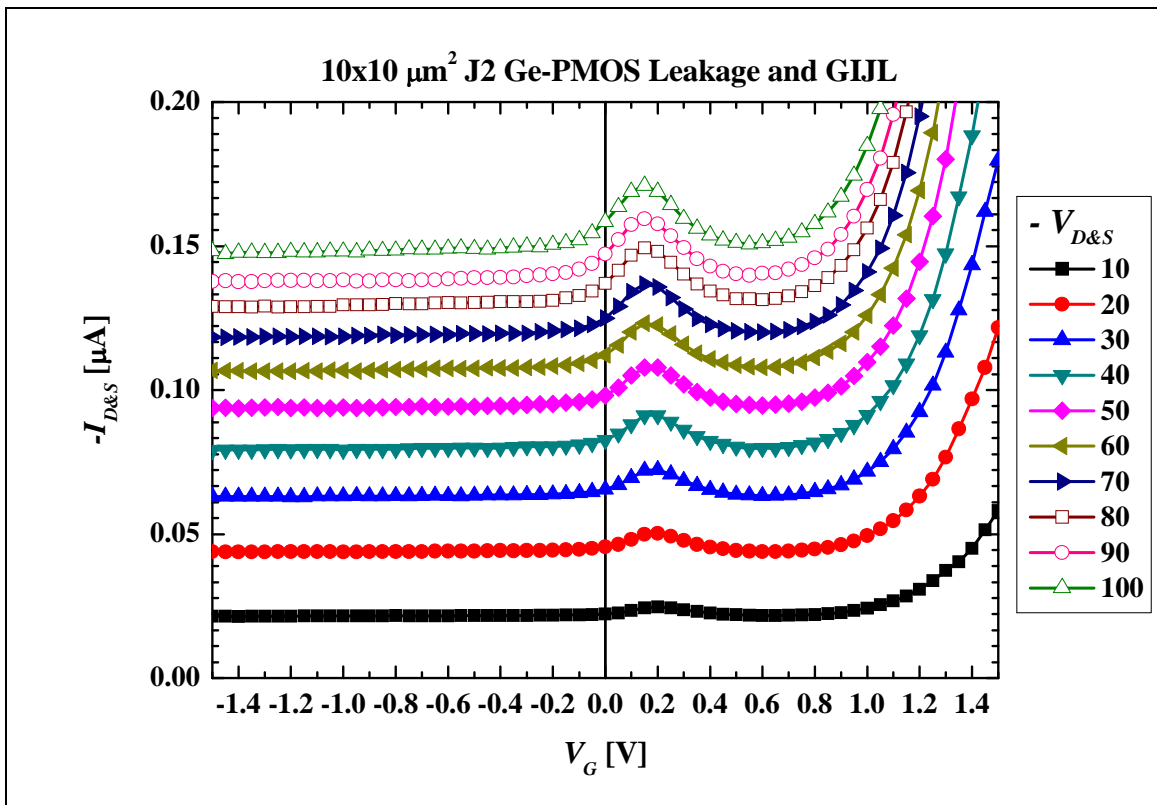


Fig. 5.10: MOS-Gated-Diode configuration showing $I_{D\&S\text{-}well}$ leakage and GIJL stability. Substantial $I_{D\&S\text{-}well}$ leakage and GIJL occurs as low as 10 mV reverse bias.

Fig. 5.10 reveals that substantial $I_{D\&S\text{-}well}$ leakage, channel depleted surface generation, and GIJL occur for $V_{D\&S\text{-}well}$ reverse biases as low as 10 mV. Special note should be paid to the apparent spike in leakage at $V_G = 0.15$ V indicating the transition

from inversion-to-depletion/depletion-to-accumulation. To place this leakage in perspective one should note that typical Ge-MOS transistor operation occurs while reverse biasing the drain at 1.5 V [9]! Activation energy extraction of the J2 leakage at each V_G will indicate which components (J_{DIFF} , J_{SRH} , J_{TAL}) dominate at $V_A = -100$ mV.

5.3.4. Activation Energy Extraction

As one may recall from Eq. 5.7 in this chapter: $J_{DIFF} \propto n_i^2$ and $J_{SRH} \propto n_i$. As a result one may write the temperature dependence proportionalities as shown in Eq. 5.9 and Eq. 5.9a.

$$J_{DIFF} \propto \exp\left(\frac{-E_G}{kT}\right) \quad (5.9)$$

$$J_{SRH} \propto \exp\left(\frac{-E_G}{2kT}\right) \quad (5.9a)$$

The proportionalities in Eq. 5.9 and Eq. 5.9a combined with Eq. 5.7 indicate that temperature analysis during reverse bias will provide activation energies of the dominant leakage current. It is expected that J_{DIFF} will dominate at higher temperatures due to ni^2 . It is known that if high electric fields exist ($E_{max} > 1 \times 10^6$ V/cm) the energy required for a generated carrier to surmount the potential barrier can be less than half the band gap. The leakage involved in such a case is trap-assisted and can exhibit PF, PAT, or TBT behavior. The nature of each reveals that $E_{A_PF} > E_{A_PAT} > E_{A_TBT}$, but since their effects cannot be separated by E_A extraction alone, any value less than $E_G/2$ will be considered TAL. One therefore expects the following conditions during E_A extraction as shown in Eq. 5.10 where E_{GO} is the band gap (0.66 eV for Ge) at room temperature.

$$\{J_{DIFF}: E_A \geq E_{GO}\}; \{J_{SRH}: E_A = \frac{1}{2}E_{GO}\}; \{J_{TAL}: E_A < \frac{1}{2}E_{GO}\} \quad (5.10)$$

To determine the activation energies of the dominant current leakage component at each gate potential the MOS-Gated-Diode configuration was used on a $10\ \mu\text{m} \times 10\ \mu\text{m}$ Ge PMOS with J2 architecture. The source/drain-to-well was reverse biased to $-100\ \text{mV}$ while sweeping the gate voltage from $-1.5\ \text{V}$ to $1.5\ \text{V}$ in increments of $0.1\ \text{V}$ using a Keithley K4200 parameter analyzer. This measurement was performed at low temperature ($25; 30; 35; 40; 50; 60^\circ\text{C}$) and high temperature ($70; 80; 100; 125; 150^\circ\text{C}$). The results are shown in Fig. 5.11.

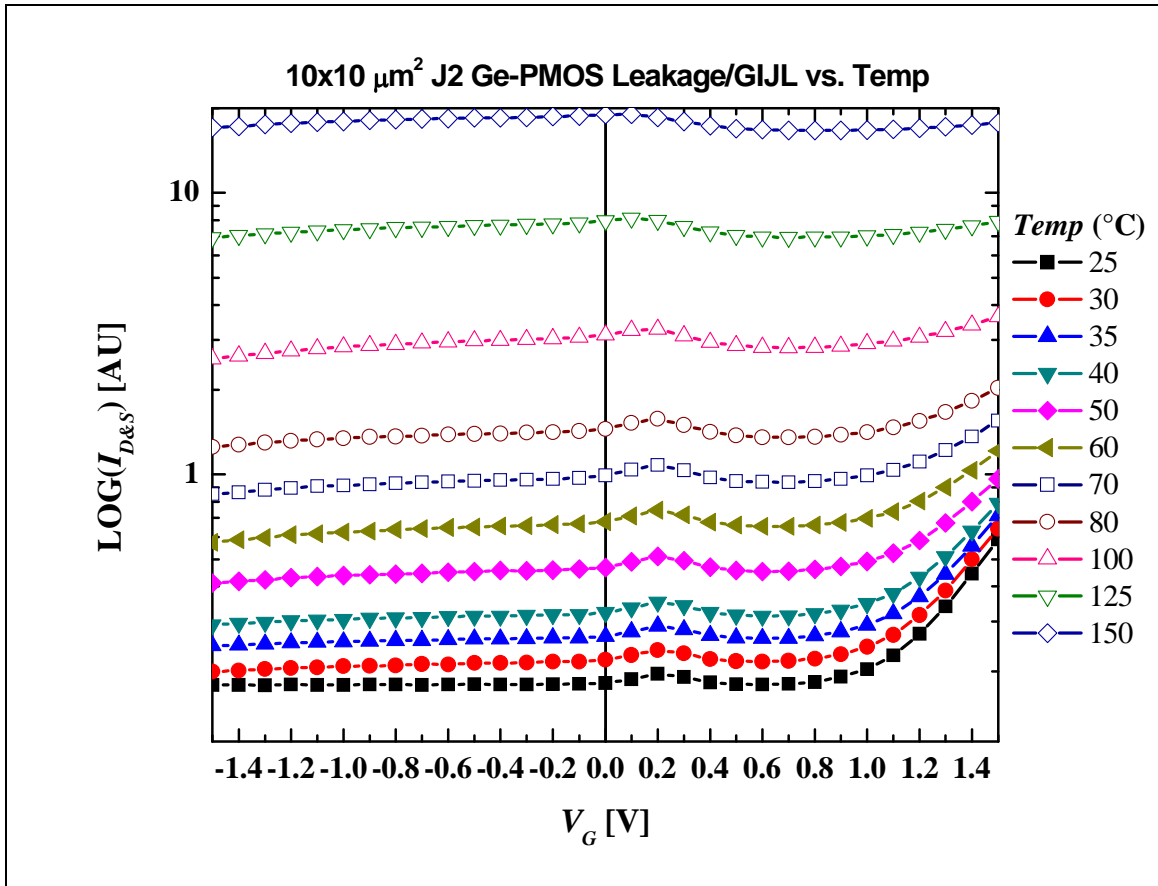


Fig. 5.11: Temperature dependence of $I_{D\&S\text{-}well}$ for $10\ \mu\text{m} \times 10\ \mu\text{m}$ Ge PMOS J2 Architecture using the MOS-Gated-Diode configuration.

Note first from Fig. 5.11 that at lower temperatures the GIJL region does not vary much with increased temperature. Only as the temperature surpasses $60^\circ\ \text{C}$ does the

leakage level in the GIJL region begin to increase sharply. Also note that the increase in temperature tends to shift the entire leakage curve up. The dominant leakage component at each gate potential may be extracted at high and low temperatures. Fig. 5.12 confirms the domain of the low temperature region and the domain of the high temperature region by fitting the leakage current density at $V_G = 0$ V to two exponentials.

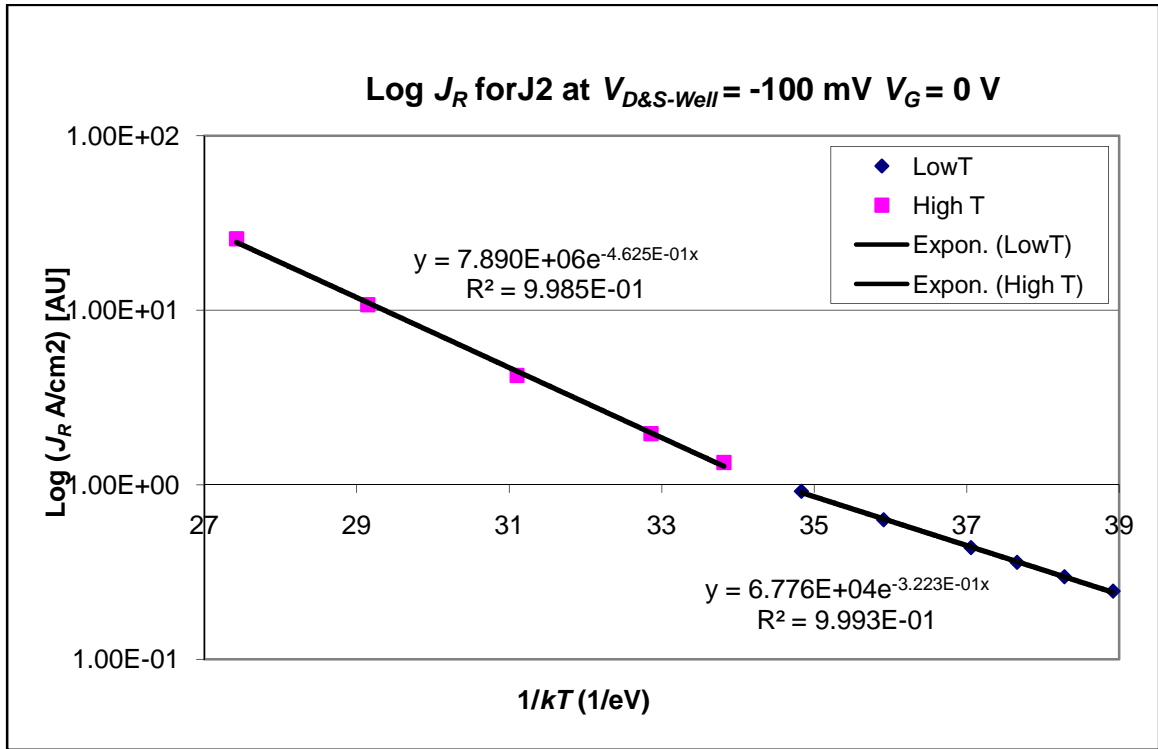


Fig. 5.12: Log of J_R at $V_G = 0$ V for $10 \mu\text{m} \times 10 \mu\text{m}$ Ge PMOS J2 architecture using the MOS-Gated-Diode configuration. Low temperature (25; 30; 35; 40; 50; 60°C) and high temperature (70; 80; 100; 125; 150°C) domains are confirmed.

Fitting two exponentials to Fig. 5.12 reveals the low temperature and high temperature domains and reveals that the J_{DIFF} does not dominate for the high temperature domain ($0.33\text{eV} < E_{A_High_T} < 0.66$ eV). J_{SRH} does tend to dominate at $V_G = 0$ V for $E_A = 0.32$ eV. To get a better idea of which component dominates at each V_G one can perform this extraction at each gate potential. This has been done and is shown in Fig. 5.13.

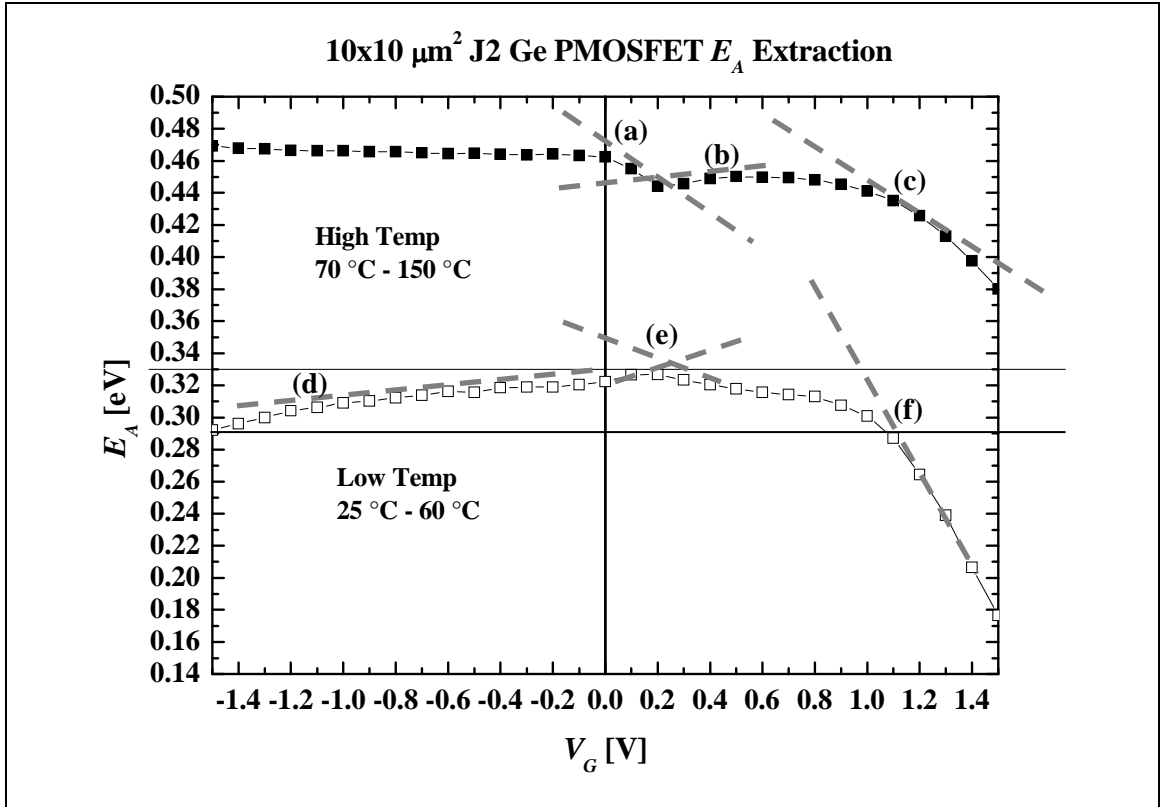


Fig. 5.13: Energy extraction at each gate potential revealing the J_{DIFF} , J_{R-G} , J_{BTBT} , and J_{AV} dependence.

Figure 5.13 reveals that at higher temperatures J_{DIFF} does not dominate the overall p/n junction leakage as expected. It is true that the leakage E_A tends to increase at higher temperatures (when compared to the low temperature case) and this can be attributed to an increase in the J_{DIFF} contribution. When looking at high temperature extraction one can see that the dominant leakage component changes with applied gate bias. In high temperature extraction, there is a great shift downward (a) when the channel passes into depletion ($V_G = 0.15 - 0.2$ V as hypothesized) which can be attributed to an increase in J_{SRH_Chan} leakage. This is followed by a decrease in generation (b) due to channel accumulation (up to $V_G = 0.6$ V) and finally a roll-off (c) when entering the TAL GIJL regime.

Looking at the lower temperature extraction one sees that the J_{TAL} component dominates in inversion (d) and tends to increase in contribution as the gate is reverse biased to -1.5 V. This was not expected. The low temperature extraction also shows that J_{SRH_Chan} dominates at a gate potential between 0 V and 0.2 V (e) as expected. The E_A extracted decreases with higher accumulation (f) due to high electric field effects (PR, PAT, TBT) representative of GIJL. Furthermore it looks as if the TBT mechanism does not activate: E_A does not equal 0 eV at $V_G = 1.5$ V.

To explain why TAL dominates throughout most of the Fig. 5.13 one may use Eq. 5.11 below and the simulated doping concentrations of Nicholas *et al.* [9].

$$E = \sqrt{\frac{2qN_A N_D (V_A + V_{bi})}{\epsilon_{ge}(N_A + N_D)}} \quad (5.11)$$

Calculating E_{max} , at an applied voltage of -100 mV for Extension-Well; HDD-Well; Extension-Halo; HDD-Halo results in 3.01×10^5 V/cm; 3.01×10^5 V/cm; 2.87×10^6 V/cm; 2.96×10^6 V/cm, respectively. These calculations are an over estimate since the applied potential is expected to drop throughout the device in approach to these regions. Despite such over estimation however, one can see that TAL is probable ($E_{max} > 1 \times 10^6$ V/cm) in the Extension-Halo and HDD Halo regions due to their large doping concentrations. The presence of TAL at -100 mV reverse bias is confirmed through E_A extraction and is an unfortunate side effect of the doping required to prevent short-channel effects in these Ge devices.

An aspect of further research includes the effect of dislocation-free substrates on the leakage current mechanisms presented in this chapter. As was discussed in theory, the J_{DIFF} leakage component should dominate the Ge-PMOS reverse-bias p/n junction

leakage. The nature of SRH theory suggests that fewer crystal perturbations (through the reduction of dislocations formation) should decrease the apparent trap density and thereby reduce the J_{SRH} component. This should also reduce the J_{TAL} observed in inversion. Besides providing devices containing lower power dissipation, dislocation-free substrates may also provide devices with superior drive current. As a result, the investigator is interested in fabricating this technology on dislocation-free substrates currently available to research.

References for Chapter 5

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Chapter 6

Germanium PMOSFET C_{GC} Parameter Extraction

Now that the behavior of the parasitic capacitance observed during C_{GC} measurement has been characterized and minimized by identifying its main sources—source/drain leakage from the low probes into the well during reverse bias (virtual ground during AC is not absolute ground); surface generation during channel depletion; GJL during high accumulation—gate characterization can take place. Gate characterization incorporates—and is certainly not limited to—the extraction of extrinsic capacitance (C_{EXT}), intrinsic capacitance (C_{GCO}), and flatband voltage (V_{FB}) from the C_{GC} measurement.

This chapter will discuss the extraction of C_{EXT} , C_{GCO} , and V_{FB} as well as the determination of EOT using the J2 architecture containing gate lengths of 10 μm , 5 μm , and 1 μm . Extrinsic and intrinsic capacitances non-idealities will be discussed first. Identifying them prior to extraction will help quantify the accuracy of the parameters determined in accumulation and inversion.

6.1. Extrinsic and Intrinsic Capacitance Non-idealities

Recall that C_{GC} behavior as defined in Chapter 2 Eq. 2.4 was comprised of the ideal intrinsic capacitance, ideal extrinsic capacitance, and the parasitic capacitance due to measurement setup. In reality this study shows that C_{GC} behavior at fixed $L \times W$ is represented by Eq. 6.1.

$$C_{GC}(V_G, f)|_{\text{Fixed}_{L,W}} = C_{GCO}(V_G) + C_{IT}(V_G, f) + C_{EXT}(V_G, f) + C_{Para}(V_G, f) \quad (6.1)$$

The realistic extrinsic capacitance C_{EXT} in Eq. 6.1 now includes a voltage and frequency-dependent parasitic capacitance component due to source/drain GIJL into the well during high accumulation (C_{Para_GIJL}). This study shows that the GIJL parameter is minimized at the onset of accumulation. This is shown in Eq. 6.2.

$$C_{EXT}(V_G) = 2C_{IF}(V_G) + 2C_O + C_{Para_GIJL}(V_G, f) \quad (6.2)$$

The realistic parasitic capacitance C_{Para} in Eq. 6.1 now includes both a frequency-dependent capacitance component due to source/drain leakage into the well throughout all V_G (C_{Para_SD}) and a voltage/frequency-dependent parasitic capacitance due to system compensation and calibration throughout all V_G (C_{Para_Meas}). This is shown in Eq. 6.3.

$$C_{Para}(V_G, f) = C_{Para_Meas}(V_G, f) + C_{Para_SD}(f) \quad (6.3)$$

The realistic intrinsic capacitance in Eq. 6.1 is the inversion capacitance. There is no additional parasitic capacitance due to channel inversion. This is shown in Eq. 6.4.

$$C_{GCO}(V_G) = C_{INV}(V_G) \quad (6.4)$$

Of final note, notice that there is an additional component in Eq. 6.1: the existence of capacitance due to interface traps— C_{IT} , a function of both voltage and frequency. This study shows that these traps are observed during trap-generated current leakage at the channel surface. They begin responding at the onset of depletion and stop responding at the onset of strong inversion. As a result their signature on the C_{GC} measurement allows for easy determination of V_{FB} (accumulation/depletion transition) and V_T (depletion/inversion transition) for the largest channel devices (10 μm x 10 μm).

6.1.1 Extrinsic and Intrinsic Capacitance Extraction of J2

C_{GC} measured for J2 architecture of gate lengths of 10 μm , 5 μm , and 1 μm have been plotted together as show in Fig. 6.1.

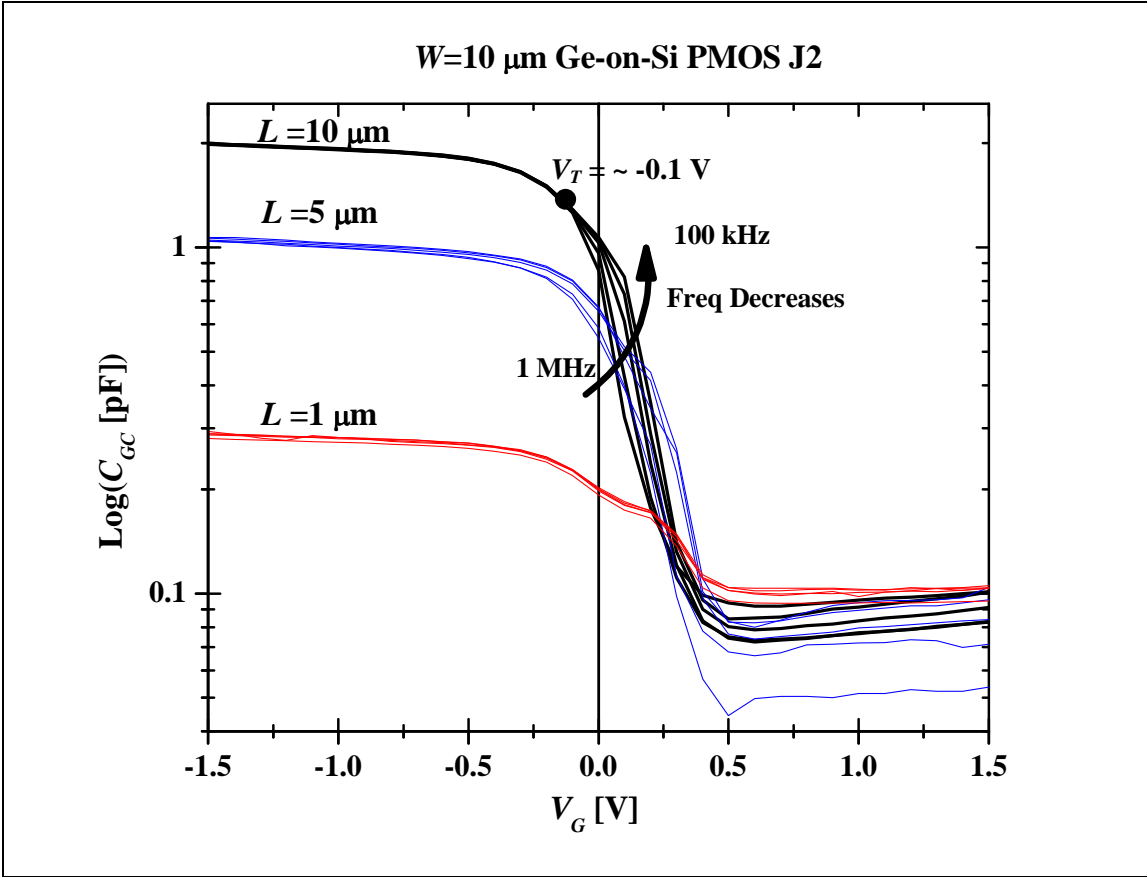


Fig. 6.1: Log of C_{GC} for J2 architecture containing gate lengths of 10 μm ; 5 μm ; 1 μm at frequencies of 100; 185; 323; 568; 1000 kHz.

Notice first that the C_{GC} curve shifts up at the gate length of 1 μm . The source of this upward shift has been identified as an increase in the reverse-bias source/well and drain/well leakages resulting in an increase in C_{Para_SD} . In order to obtain C_{EXT} one cannot subtract this C_{Para_SD} component.

According to theory, plotting C_{GC} as a function of V_G for multiple gate lengths—of the same architecture and frequency—reveals an intersection of each C_{GC} curve [2]. This intersection first occurs at the depletion/accumulation transition and reveals C_{EXT} . C_{OV} may dominate C_{EXT} at this point [2]. As was shown by this study, however, trap conductance is a function of gate length in these devices. Due to the C_{IT} contribution, the C_{Para_SD} existence, and their dependency on gate length this definition cannot be used to determine C_{EXT} in these devices.

As a result, C_{EXT} is extracted at the transition between accumulation and depletion. This point is referred to as the flatband voltage [2]. At this point C_{IT} does not exist, C_{Para_SD} is minimum (as observed during DC analysis), and C_{Para_GIJL} does not yet take over. The only source of parasitic capacitance comes from tool compensation/calibration and that of C_{Para_SD} . The C_{EXT} and V_{FB} for the 10 μm , 5 μm , and 1 μm devices have been extracted for frequencies containing the smallest C_{Para_SD} (100; 185; 323; 568; 1000 kHz): the results are shown in Table 6.1.

Table 6.1: Summary of C_{EXT} and V_{FB} from Fig. 6.1.

Gate Length	Parameter	Frequency [kHz]					Mean	% Std Dev
		100	185	323	568	1000		
10 μm	C_{EXT} [fF]	84.6	78.4	72.4	73.2	92.0	80.1	10.2
	V_{FB} [mV]	500	600	600	600	600	580	7.8
5 μm	C_{EXT} [fF]	79.9	82.3	73.8	44.4	66.2	69.3	22.1
	V_{FB} [mV]	600	600	600	500	600	580	7.8
1 μm	C_{EXT} [fF]	98.0	101.9	99.7	93.7	102.3	99.1	3.5
	V_{FB} [mV]	1000	700	700	700	1100	840	23.2

Table 6.1 reveals that C_{EXT} for the 10 μm and 5 μm devices resides within 88.3–54 fF. The 1 μm device has been omitted due to the large percent standard deviation in flatband

voltage. The exact value of C_{EXT} could be less than 54 fF since source/well and drain/well leakages still exist. It is clear, however, that this value is more accurate than those attainable using the D1 and G3 architectures. Also note that the V_{FB} is 580 +/- 45 mV for the 10 μm and 5 μm devices which confirm the DC results shown Fig. 5.9 of Chapter 5.

To determine the intrinsic capacitance and hence the inversion capacitance, one can mathematically subtract C_{EXT} and C_{Para} from the entire C_{GC} curve as shown in Eq. 6.1. This results in Fig. 6.2.

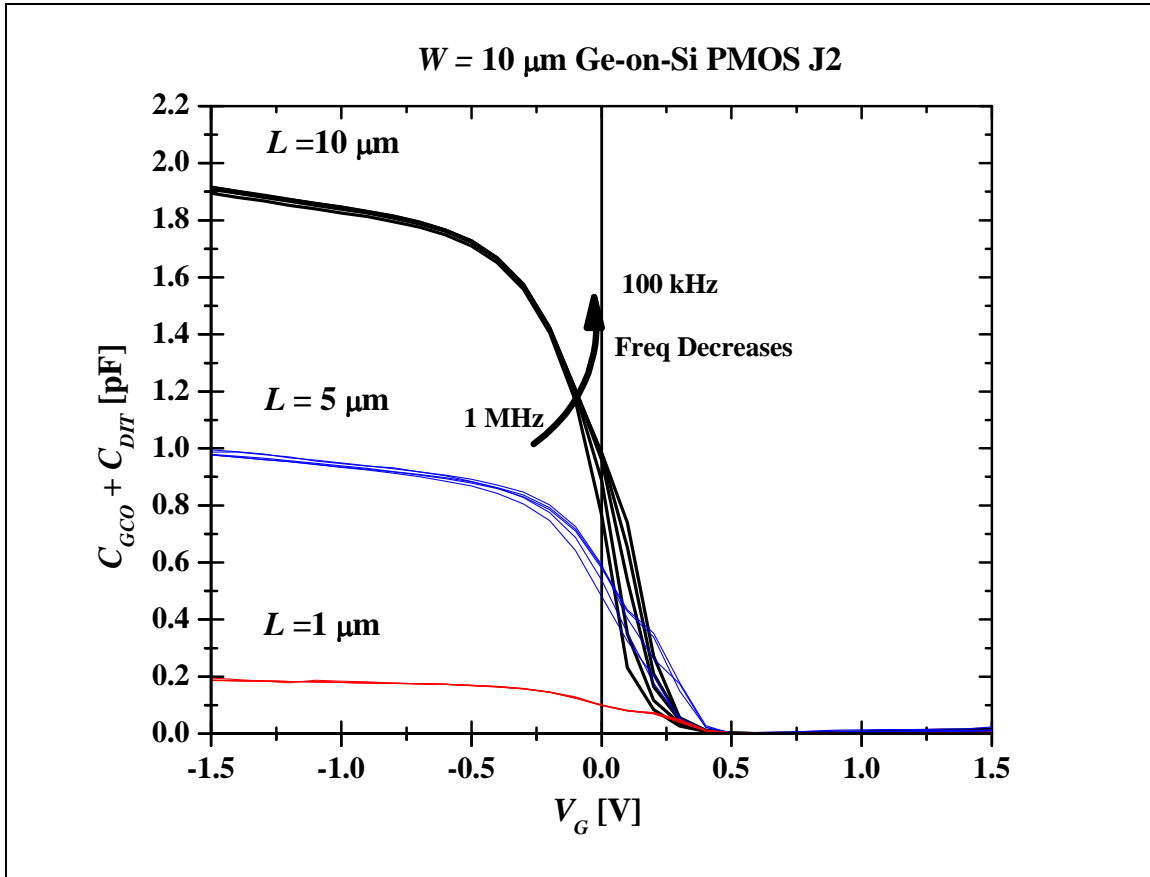


Fig. 6.2: C_{GCO} for J2 architecture containing gate lengths of 10 μm ; 5 μm ; 1 μm at frequencies of 100; 185; 323; 568; 1000 kHz.

Note from Fig. 6.2 that the capacitance due to interface traps does not exist in inversion.

Also note that the inversion capacitance increases slightly as the gate voltage decreases.

The source of this will be discussed shortly. The inversion capacitance C_{INV} is determined far from V_{FB} . In this case C_{INV} will be taken at -1.5 V from V_{FB} . The results are shown in Table 6.2.

Gate Length	Parameter	Frequency [kHz]					Mean	% Std Dev
		100	185	323	568	1000		
10 μm	C_{INV} [fF]	1843	1830	1830	1824	1812	1828	0.6
	V_{INV} [mV]	-1000	-900	-900	-900	-900	-920	4.9
5 μm	C_{INV} [fF]	939	930	927	949	924	934	1.1
	V_{INV} [mV]	-900	-900	-900	-1000	-900	-920	4.9
1 μm	C_{INV} [fF]	170	177	177	176	164	173	3.5
	V_{INV} [mV]	-500	-800	-800	-800	-400	-660	29.5

6.2. Effective Oxide Thickness Calculation J2

Effective oxide thickness (EOT) can be calculated theoretically and extracted from C_{INV} as shown in Eq. 6.5 and Eq. 6.6 respectively. K_{OX} is the dielectric permittivity of SiO_2 , K_{HfO_2} is the dielectric permittivity of HfO_2 , K_{Si} is the dielectric permittivity of Si, ϵ_0 is the permittivity of free space, A is the gate area, and C_{INV} is the extracted inversion capacitance from C_{GC} .

$$EOT_{Classical} = t_{HfO_2} \left(\frac{K_{OX}}{K_{HfO_2}} \right) + t_{OX} \left(\frac{K_{OX}}{K_{OX}} \right) + t_{Si} \left(\frac{K_{OX}}{K_{Si}} \right) \quad (6.5)$$

$$EOT_{Actual} = \frac{K_{OX}\epsilon_0 A}{C_{INV}} \quad (6.6)$$

EOT is a commonly used parameter to compare advanced high- κ gate dielectric stacks to the existing classical SiO_2 gate dielectric technology. The Ge-PMOS in this study have theoretical $EOT_{Classical}$ of 1.2 nm as shown in Eq. 6.7.

$$EOT_{Classical} = 4nm \left(\frac{3.9}{25}\right) + 0.4nm + 0.6nm \left(\frac{3.9}{11.9}\right) = 1.2nm \quad (6.7)$$

The actual EOT using the C_{INV} values obtained in Table 6.2 are shown in Table 6.3.

Gate Length	Parameter	Frequency [kHz]					Mean	% Std Dev
		100	185	323	568	1000		
10 μm	EOT [nm]	1.87	1.89	1.89	1.89	1.91	1.89	0.6
5 μm	EOT [nm]	1.84	1.86	1.86	1.82	1.87	1.85	1.0
1 μm	EOT [nm]	2.03	1.95	1.95	1.96	2.11	2.00	3.0

As one can see the classical EOT is 0.69 nm lower when compared to the extracted EOT of the 10 μm device and 0.65 nm lower when compared to the extracted EOT of the 5 μm device. This average EOT difference of 0.67 nm is due to the inversion layer quantization effect [3].

6.2.1 Inversion Layer Quantization

During C_{GC} measurement of these devices in inversion the channel experiences a large gate-oxide electric field. This electric field, if high enough, can result in inversion layer quantum confinement due to band bending at the germanium-Si/SiO₂ interface. When this occurs the inversion carriers behave quantum-mechanically (as a 2D gas quantized in energy and location) resulting in an inversion layer recession from the Ge/Si-SiO₂ interface [3]. This is becoming a significant problem in advanced gate stack technology requiring even thinner effective oxide thicknesses. This inversion layer recession increases with increasing electric field (proportional to the absolute magnitude of the gate bias). It is for this reason that we observe an increase in C_{GC} as the channel

becomes more inverted. As a result the theoretical EOT considering this quantum confinement is shown in Eq. 6.8.

$$EOT_{Quantum} = EOT_{Classical} + t_{Ge} \left(\frac{K_{Ox}}{K_{Ge}} \right) \quad (6.8)$$

The new quantum EOT calculation allows us to account for inversion layer quantization. Assuming that this quantization begins at the Ge/Si-SiO₂ interface and taking the average 0.67 nm EOT difference, one can calculate the depth of the inversion layer within the Ge channel as shown in Eq. 6.9.

$$t_{Ge} = 0.67nm \left(\frac{K_{Ge}}{K_{Ox}} \right) = 0.67nm \left(\frac{11.9}{3.9} \right) = 2.04nm \quad (6.9)$$

Theoretically, calculating the thickness of inversion layer quantization as a function of applied voltage and technology requires that one iteratively solve the Schrödinger-Poisson equations. This can be a numerically intensive task. Instead of doing this, the 2.04 nm hole quantization thickness is compared against the 3 nm hole quantization of the Ge PMOS device reported by Low *et al.* [4] in 2003. The well of this work was simulated at $1 \times 10^{18} \text{ cm}^{-3}$ with an EOT of 1 nm allowing comparison to the devices in this study. When compared to the work of Low *et al.* [4]—after considering the lower well doping ($\sim 1 \times 10^{17} \text{ cm}^{-3}$) of the devices in this study—a 2.04 nm quantization thickness is an acceptable approximation of the mismatch in theoretical and measured EOT . Solving the Schrödinger-Poisson equations iteratively is required for an in-depth analysis of the correction accuracy.

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Chapter 7

Conclusions

This study has characterized the gate-to-channel capacitance (C_{GC}) behavior and its relationship to source-channel-drain/well leakage of Ge-PMOS built on relaxed germanium-on-silicon technology. Specifically, it was found that connecting the low probes of the C - V unit to the source and drain induced a reverse-bias source/well and drain/well leakage into the channel. This was unexpected due to the virtual grounding condition reported in the C - V user manual. This reverse-bias leakage was found to be a function of gate potential, source/drain area, source/drain contact distance from gate, gate length, and measurement frequency.

The parasitic C_{GC} observed in this Ge-PMOS technology has been minimized. Results show that further optimization is possible, for reverse-bias p/n junction leakage of the J2 architecture ($10\ \mu\text{m} \times 10\ \mu\text{m}$) occurs at reverse biases as low as 10 mV. This was observed using the MOS gated-diode configuration. To the investigator's knowledge, this is the first time in which a gated-diode configuration has been used to characterize the leakage components and mechanisms of a MOSFET and later to explain the non-idealities observed during C_{GC} measurement. The MOS gated-diode configuration revealed the leakage components and mechanisms of interest in this study and helped identify a seventh leakage component of concern, previously ignored during typical MOSFET operation [1]: channel generation current during channel depletion.

During parameter extraction it was revealed that threshold voltage extraction using C_{GC} data is unreliable due to the contribution of C_{IT} . As a result, flatband voltage

(V_{FB}) was targeted. At this voltage (~ 0.580 V) the parasitic capacitance (C_{Para_SD}) was minimum resulting in accurate V_{FB} extraction. Using V_{FB} , V_{INV} ($V_{INV} = V_{FB} - 1.5$ V) and hence inversion capacitance (C_{INV}) was found. Using this inversion capacitance, effective oxide thickness (EOT) was calculated. The average EOT for $10\ \mu\text{m}$ and $5\ \mu\text{m}$ gate lengths was extracted—using the inversion capacitance of C_{GC} —as 1.87 nm. This value is 0.65 nm greater than the 1.2 nm expected EOT . This difference revealed the presence of a 2.04 nm inversion layer quantization which was confirmed by similar devices published by Low *et al.* [2].

This study revealed the correct method of C_{GC} measurement and opened many doors for further research. Such include C - V unit conductance and capacitance correction due to error induced from Ge-PMOS grounding; architecture optimization so as to reduce trap assisted leakage; source and drain doping optimization so as to avoid gate-induced junction leakage; evaluation of trap-assisted leakages in devices fabricated upon substrates free of dislocations; source and drain contact optimization so as to reduce reverse-bias leakage.

The investigator wishes to determine—with further research—the exact source of these trap-assisted leakages. Are they created by the relaxed dislocations from the Ge-on-Si substrate? Are they by the addition of impurities during device fabrication? It is clear from research that these devices exhibit excellent performance [3-5]. The investigator believes that better performance can be obtained using substrates free of threading dislocations [6]. It is quite clear that power dissipation will be a limiting factor in the implementation of these devices at the 32 nm node [7]. As a result full characterization of

these leakage components, their mechanisms, and sources must be determined. This will be investigated by the investigator during PhD studies to begin at IMEC in January 2008.

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