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Development of plasma enhanced chemical vapor deposition (PECVD) gate dielectrics for TFT applications

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Development of Plasma Enhanced Chemical Vapor Deposition (PECVD) Gate Dielectrics for TFT Applications

By

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Abstract

This study investigated a variety of electrically insulating materials for potential use as a gate dielectric in thin-film transistor applications. The materials that were investigated include silicon dioxide and oxynitride films deposited using PECVD and LPCVD techniques. Silicon source materials included tetraethylorthosilicate (TEOS) and silane (SiH_4). Oxygen sources included diatomic oxygen (O_2) and nitrous oxide (N_2O). The optical, electrical, and material properties of the dielectrics were analyzed using Variable Angle Spectroscopic Ellipsometry (VASE), Fourier Transform Infrared Spectroscopy (FTIR), Capacitance-Voltage (C-V) analysis and current-voltage (I-V) analysis. Transistors were also fabricated at low temperatures with different gate dielectrics to investigate the impact on device performance. While a deposited gate dielectric is intrinsically inferior to a thermally grown SiO_2 layer, an objective of this study was to create a high quality gate dielectric with low levels of bulk and interface charge (Q_{it} & Q_{ot}~$1x10^{10}$ cm^2); this was achieved.

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Chapter 1

Introduction

There is an increasing interest in developing low temperature deposition processes that provide a high quality dielectric on semiconductor materials that do not provide a chemically stable oxide (e.g. germanium), or for non-traditional substrate applications (e.g. glass), [1]. The thin film transistor (TFT) industry is limited in processing temperature because of the strain point of the substrate, which is either a plastic or glass material. A high temperature (T~1000°C) thermal oxide cannot be used, and the industry typically relies on a plasma enhanced chemical vapor deposition (PECVD) gate dielectric. TFTs are used in Organic Light Emitting Diode (OLED) displays and Liquid Crystal Displays (LCD); as switches to activate a pixel cell. A typical TFT cross-section is shown below in Figure 1.1.

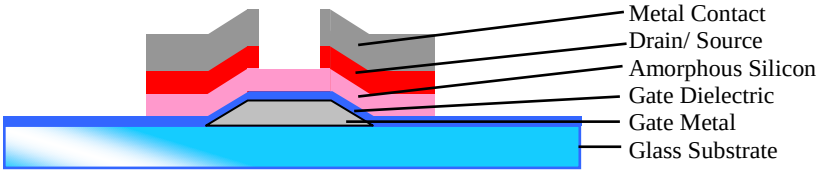

Figure 1.1: Bottom gate LCD TFT cross-section.

Several methods can be used to deposit a dielectric, such as physical vapor deposition (PVD) - sputtering or evaporation, PECVD, atmospheric chemical vapor

deposition (AMCVD), and low pressure chemical vapor deposition (LPCVD). For TFT applications the dielectric must have high thickness uniformity; glass substrates are on an area scale of square meters. The flat panel display (FPD) industry is currently tooled for PECVD deposition tools, which can meet the uniformity and performance requirements.

There are many parameters that are important in quantifying the gate dielectric quality, which will affect the transistor operation and circuit performance, as well as product reliability. Breakdown field, oxide charge, transparency, density, and composition are among the parameters that will be measured directly or indirectly to determine the quality of the dielectrics that are being investigated. The scope of this project focused on the development of PECVD based dielectrics; results of which are compatible with the FPD industry.

This thesis reviews the concepts of CVD in Chapter 2. A review of oxide non-idealities will be reviewed in Chapter 3. Chapter 4 will discuss the different measurement techniques used in this study. Chapter 5 will review the concepts of the 2 and 3 terminal MOS device. Chapters 6 & 7 will present the fabrication steps of the MOS transistors and capacitors as well as MOS results. Chapter 8 will present the optical and physical characterization results.

Chapter 2

Chemical Vapor Deposition for Thin-Film Dielectrics

Chemical vapor deposition is the formation of a solid film on a substrate by the reaction of vapor-phase chemicals (reactants) that contain the required constituents [2]. CVD processes do not react with or consume the substrate. There are five types of CVD reactions: thermal decomposition, reduction, oxidation, compound formation, and disproportionation. In this study the primary concern will be the oxidation and decomposition reactions. The reactions that will be of interest in this study are listed in Equations (2.1), (2.2), and (2.3).

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2 \quad (2.1)$$

$$SiH_4 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2H_2 \quad (2.2)$$

$$Si(OC_2H_5)_4 + O_2 = SiO_2 + byproducts \quad (2.3)$$

Often oxygen is added to the tetraethylorthosilicate {$Si(OC_2H_5)_4$} reaction to increase the deposition rate and to fully react with carbon in the reaction. The growth rate of a CVD film is governed by the partial pressure of the reactants and temperature of the reaction. If the reaction function of the transport of reactants from main gas flow to the substrate surface is less than the reaction rate function of the surface reaction, then the

reaction is mass transport limited. If the opposite is true then the reaction is reaction rate limited. The deposition is usually mass transport limited at higher temperatures and reaction rate limited at lower temperatures. In a PECVD reaction, the incoming source gas is broke into radicals by electron bombardment is an RF plasma, since the plasma is excited by a 13.56 MHz frequency, only electrons can respond, allowing the temperature of the radicals in the reaction to remain relatively low. For PECVD reactions most radicals are electrically neutral so their transport to the wafer surface is by gas phase diffusion and radical concentration gradient drives this diffusion process and not the temperature of the radicals as in other CVD reactions. There are some source molecules that are ionized; these ions are accelerated by the plasma bias toward the substrate. Table 2.1 shows the advantages, disadvantages and applications of PECVD, LPCVD, and APCVD reactors. Figure 2.1 shows three types of CVD reactors commonly used today, belt APCVD, batch hot-wall reactor LPCVD, and parallel plate PECVD reactor. Table 2.2 shows the properties of various CVD films.

Table 2.1: Characteristics and applications of CVD reactors [2].

Process	Advantages	Disadvantages	Applications
APCVD	Simple Reactor, Fast Deposition, Low Temperature	Poor Step Coverage, Particle Contamination	Low Temperature Oxides, both doped and undoped; Epi films, Trench Fill
LPCVD	Excellent Purity and Uniformity, Conformal Step Coverage, Large Wafer Capacity	High Temperature Low Deposition Rate Source Depletion	High Temperature Oxides, both doped & undoped, Silicon Nitride, Poly-Si, W, WSi_2
PECVD	Low Temperature, Fast Deposition, Good Step Coverage, Large Area Deposition possible	Chemical (e.g., H_2) and Particulate Contamination	Low Temperature Insulators over Metals, Passivation (Nitrides)

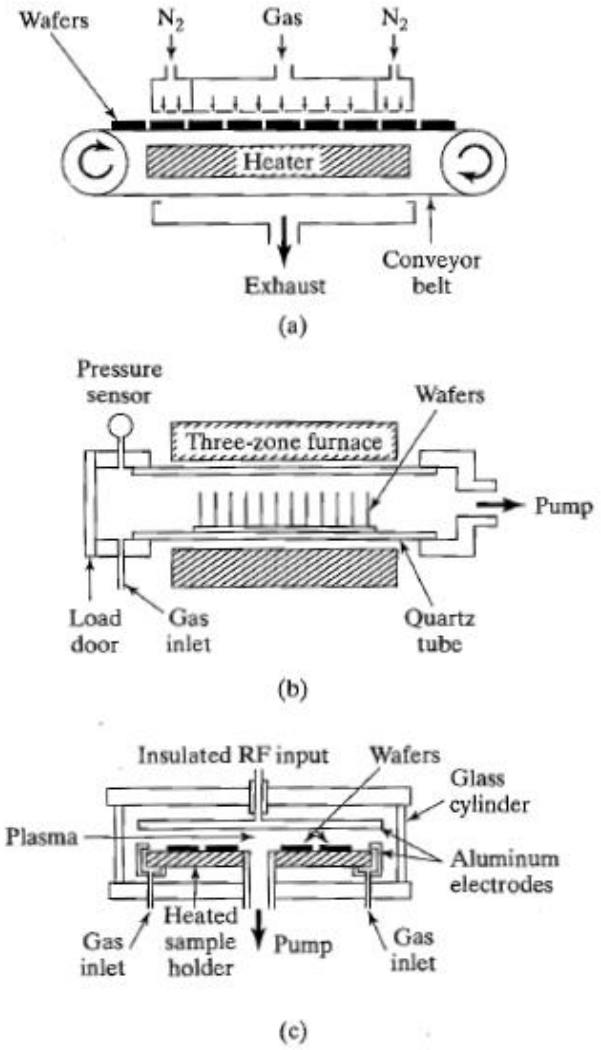

Figure 2.1: Three types of chemical vapor deposition (CVD) systems. (a) Atmospheric-pressure reactor; (b) hot-wall LPCVD system using a three-zone furnace tube; (c) parallel-plate plasma-enhanced CVD system [3].

Table 2.2: Properties of Various Deposited Oxides [3].

Source	*Deposition Temperature (˚C)*	*Composition*	*Conformal Step Coverage*	*Dielectric Strength (MV/cm)*	*Etch Rate (Å/min) [100:1 H_2O:HF]*
Silane	450	SiO_2(H)	No	8	60
Dichlorosilane	900	SiO_2(Cl)	Yes	10	30
TEOS	700	SiO_2	Yes	10	30
Plasma	200	$SiO_{1.9}$(H)	No	5	400

2.1. Low Pressure Chemical Vapor Deposition, LPCVD

LPCVD systems are usually hot-wall reactor systems, meaning the chamber walls are heated to the deposition temperature. A major disadvantage of a hot wall reactor system is that films deposit on the chamber wall as well as on the substrate, and the chamber will need to be periodically cleaned. The operating temperatures of typical LPCVD reactions are 300 to 1150°C and pressures from 0.2 to 2 Torr [4]. There are two types of reactions that take place in an LPCVD reactor, homogeneous and heterogeneous reactions. In a homogeneous reaction the reactants react in the atmosphere of the reactor and not on the heated surfaces in the reactor. This causes gas phase nucleation in the plasma or particulates to 'rain' on the substrate causing a high defect count. This phenomenon is more common in silane based reactions. In a heterogeneous reaction the reactants diffuse to the substrate and are adsorbed on the substrate. Adatom migration takes place. The by-products desorb from the surface and diffuse into the main gas flow.

2.2. Plasma Enhanced Chemical Vapor Deposition, PECVD

Plasma Enhanced Chemical Vapor Deposition (PECVD) is a deposition method that uses plasma to disassociate, excite or ionize reactants as opposed to a hot-wall reactor that uses temperature. Most PECVD systems use temperatures less than 400°C.

A parallel plate reactor shown in Figure 2.1.c, uses a radio frequency (13.56 MHz) bias applied to an electrode ~1 cm above the substrate, while under vacuum in the Torr range to create a plasma. Electrons are accelerated, colliding with the reactants. The inelastic collisions cause the reactants to dissociate, excite or ionize and diffuse or ions to accelerate toward the substrate. The reactants adsorb to the substrate and any by-products are desorbed from the substrate. PECVD reactions often have high energy electrons and excited radicals, these high energy particles are prone to create electrical defects in solid state devices.

2.3. Dielectric Materials for TFTs

The flat panel display (FPD) industry uses several different dielectrics for thin film transistor (TFT) processes. Silicon dioxide, silicon nitride, high-k gate dielectrics and silicon oxynitride materials have been used for the gate dielectric in current thin film transistors [5]. The scope of these experiments will focus on silicon dioxide and silicon oxynitride materials. The deposition method for these dielectrics is typically plasma enhanced chemical vapor deposition (PECVD). This chapter will discuss the material and electrical characteristics of silicon dioxide, and silicon oxynitride.

Silicon dioxide is the standard gate dielectric for the IC industry for the last several decades. This is due to the excellent interface quality, creating low interfacial charge with a silicon substrate. In the demand for faster switching speeds, high-k gate materials have been investigated in the IC industry, but they suffer from a poor interface. A result is that SiO_2 is still being used as an interfacial layer in some applications [6]. However high-k dielectric materials are not in high demand from the display industry, because device geometries and required switching speeds are not as challenging as the IC industry. Therefore if a silicon dioxide film can be created at temperatures appropriate for the display industry (T~600 ºC) and has electrical properties close to thermally grown oxide, this will satisfy the display industry's needs.

Studies have shown that using a PECVD process for a MOS gate insulator has yielded devices with a performance comparable to a thermally grown oxide [7]. In this study the silicon precursor was SiH_4 and the oxygen source was N_2O. By adding helium to the reaction, of the source molecules are more completely dissociated into their fundamental elements, resulting in a more complete reaction. Other studies have shown that using a TEOS/O_2 precursor with inert argon gas molecules can create a dense oxide with good electrical properties [8]. Several variations on these input parameters were investigated and are discussed in Chapter 5.

Chapter 3

Oxide and Interface Trapped Charges

Oxide charge is the main parameter of a gate dielectric that is of interest in the operation of a transistor, and circuit. There are four types of charges in the silicon-silicon dioxide system; they are interface trapped charge, fixed oxide charge, mobile oxide charge, and oxide trapped charge. Figure 3.1 shows the location of the different charges found in a Si-SiO_2 system.

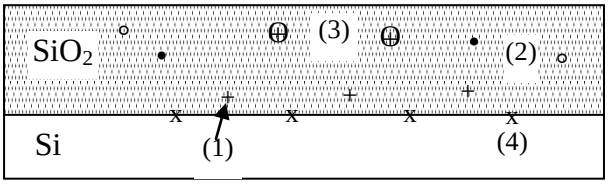

Figure 3.1: Charges and their location for thermally oxidized silicon. (1)-Fixed Oxide Charge, (2) - Oxide Trapped Charge, (3) - Mobile Oxide Charge, (4) – Interface Trapped [9].

3.1. Fixed Oxide Charge (Q_f)

Fixed oxide charge is typically a positive charge, primarily caused by structural defects within 2 nm of the oxide silicon surface and typically seen in thermally grown oxide. Fixed oxide charge is affected by the silicon orientation, final annealing temperature and ambient. The fixed charge has been show to be reversible and is modeled by the "Deal triangle" shown in Figure 3.2.

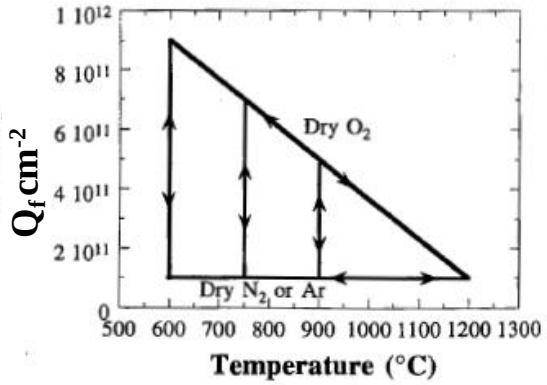

Figure 3.2: "Deal triangle" showing the reversibility of heat treatment effects on Qf for a (111) oriented silicon wafer [10].

3.2. Oxide Trapped Charge (Q_{ot})

Oxide trapped charge can be positive or negative and is caused by the trapping of hot carriers in the bulk of the oxide from Fowler-Nordheim tunneling, ionizing radiation, avalanche injection, or other mechanisms. Oxide trapped charge can be mitigated by annealing at low temperatures (<500 ˚C) unlike fixed charge. Oxide trapped charge is usually characterized by their capture cross sections. Electron traps with capture cross sections in the range of 10^{-14} to 10^{-12} cm^2 are usually Coulomb-attractive traps. Electron traps with capture cross sections on the order of 10^{-18} to 10^{-14} cm^2 are usually due to neutral traps. Electron traps with a cross section smaller than 10^{-18} cm^2 are usually associated with Coulomb-repulsive traps [11].

3.3. Mobile Oxide Charge (Q_m)

Mobile oxide charge, typically a positive charge, is caused by alkaline ions such as Na^+, K^+, Li^+, and possibly H^+. These ions are typically mobile in the temperature range of a transistor operation and can reduce the reliability of a device. Figure 3.3 shows the mobility of Na^+, K^+, Li^+, and Cu^+ vs. temperature.

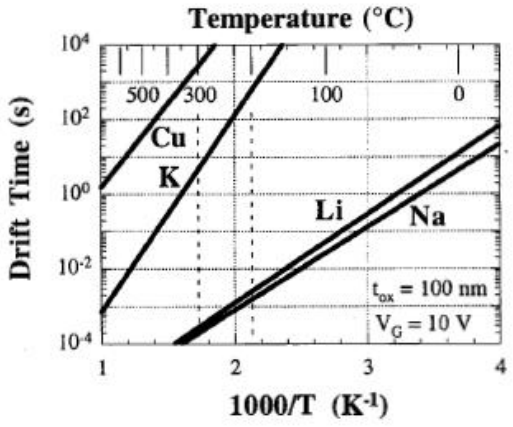

Figure 3.3: Drift time for Na, Li, K, and Cu for an oxide electric field of 106 V/cm and tox=100 nm [12].

3.4. Interface Trapped Charge (Q_{it}, D_{it})

Interface trapped charge are positive or negative charges that are caused by structural defects at the interface between the silicon and silicon-dioxide, metal impurities, or caused by other bond breaking processes—e.g.: hot electrons, radiation, ect. Interface trapped charge can be charged or discharged depending on the surface potential of the silicon. Most interface trapped charge can be neutralized by a low

temperature anneal ~450 ˚C in a dilute H_2 ambient ~5%, and N_2. Figure 3.4 shows the ranges of different techniques used to detect interface traps.

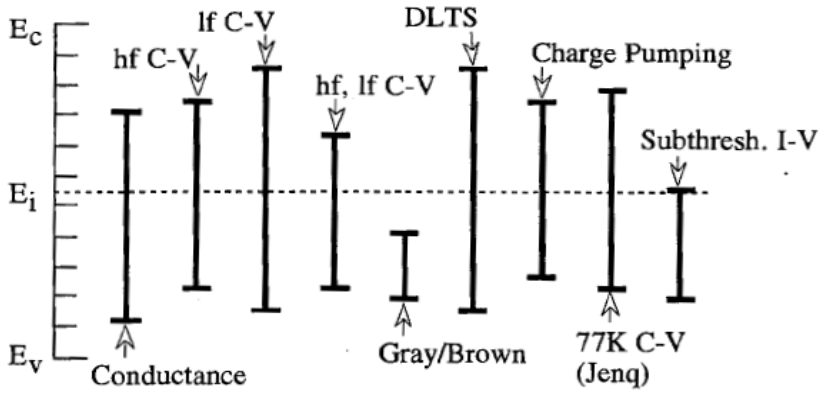

Figure 3.4: Ranges of energy in the band gap of a silicon p-type substrate over which interface trap charges are determined by various characterization techniques [12].

These fundamental understandings of the charge densities in a dielectric are essential for the understanding of a MOS device. These imperfections in a gate dielectric can lead to performance degradation in NFET and MOS devices. In the next chapter the different methods to characterize these defects are presented.

Chapter 4

Measurement and Analysis Techniques

There are several methods and techniques to characterize a dielectric film. The techniques that are discussed here are variable angle spectroscopic ellipsometry (optical constants), prism coupler, Fourier Transform infrared spectroscopy (bonding configurations, stoichiometry), stylus profilometry (film stress), time-of-flight secondary ion mass spectrometry (element composition), and chemical etch rates. Electrical measurements such as capacitance–voltage measurements (dielectric and interface charge), gate dielectric integrity measurements (electric field breakdown, charge to breakdown), and transistor drain current–gate voltage measurements will be discussed in chapter 6.

4.1. Optical Materials Characterization

Variable Angle Spectroscopic Ellipsometry, VASE

Ellipsometry is a technique used to characterize both thin films and bulk materials properties. Some useful parameters that can be measured by ellipsometry are optical constants such as index of refraction and extinction coefficient (n, k or ε_1, ε_2) in the UV, visible and IR wavelengths, surface roughness, composition, and optical anisotropy.

Ellipsometry measures the ratio of Fresnel reflection coefficients $\tilde{R}_p$ and $\tilde{R}_s$ for p- and s-polarized light, respectively [13]. The measured values are expressed as psi (ψ) and delta (Δ). The relationship between the Fresnel reflection coefficients and delta and psi is given in equations (4.1) & (4.2). Figure 4.1 shows the geometrical representation of an ellipsometry system.

$$\rho = \frac{R_p}{R_s} = \tan(\psi)e^{i\Delta} \tag{4.1}$$

$$\Psi = \tan^{-1}|\rho| \tag{4.2}$$

where Δ is the differential phase change, Δ_p- Δ_s.

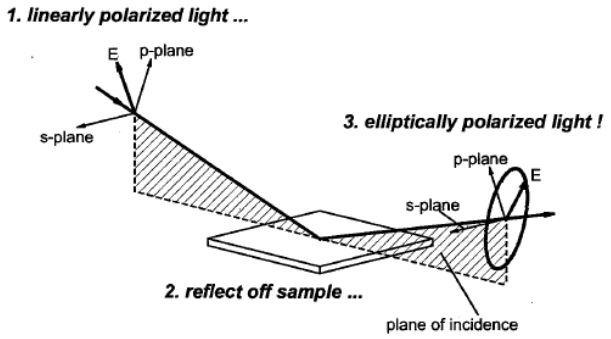

Figure 4.1: Geometry of an ellipsometry experiment, showing the p- and s-directions [13].

Fourier Transform Infrared (FTIR) Spectroscopy

Molecular bonds vibrate at discrete excitation energies, or wavelengths. Each molecular vibration occurs with a frequency characteristic of the molecule, and this

vibration frequency is the same as the electromagnetic wave that is absorbed. Therefore the vibration frequency of a molecule can be directly measured. These energies are derived from the difference between the ground state of the bond energy to an excited state of the bond energy, and are unique for different elements and bonds. The energy associated with this excitation, usually between the first excited state (E_{final}) and the ground state ($E_{initial}$) is given by equation (4.3), which shows that the energy of light absorbed takes on discrete values based on the difference in energy states. The energy corresponding to these molecular vibrations is related to the bond between two atoms, with some mass, and this bond can be treated as a harmonic oscillator with a spring constant given by equations (4.4), (4.5), (4.6), (4.7).

$$E_{final} - E_{initial} = \frac{h\,c}{\lambda} \quad \textbf{(4.3)}$$

$$w = \frac{2\pi}{\lambda} \quad \textbf{(4.4)}$$

$$f = \frac{1}{2\pi}\sqrt{\frac{k}{u}} \quad \textbf{(4.5)}$$

$$f = \frac{1}{2\pi}\sqrt{\frac{k}{u}} \quad \textbf{(4.6)}$$

$$E_n = h\,f\left(n+\frac{1}{2}\right) \quad \textbf{(4.7)}$$

n=0,1,2,3,…

where h= Plank's constant, c= speed of light, λ= wavelength of light,
w= wavenumber, f=frequency of oscillation, k=spring constant,
m_1 & m_2 = mass of the atoms

The energy of this vibration corresponds to the IR spectrum. FTIR is useful in analyzing SiO_2 films because it gives a direct measurement of the density of bonds, showing how stoichiometric a film is and if there are other impurities in the film. Figure 4.2 shows a typical FTIR setup using a Michelson interferometer. The benefit to using FTIR as opposed to DIR spectroscopy is the FTIR method makes use of a Fourier transform of the interferogram as it relates to the spectrum of the probe. This allows for a large range of a spectrum to be analyzed over a short scan period. Even though FTIR was first theorized in the nineteenth century it was not made common until the 1970's and the used of fast Fourier transforms and the computer. Figure 4.3 shows a transmission FTIR absorbance spectrum for a PECVD TEOS sample deposited at RIT. Table 4.1 shows the assignment between wavenumber and bond.

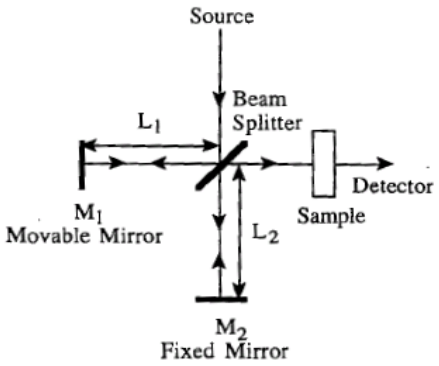

Figure 4.2: Schematic of a typical FTIR system [12].

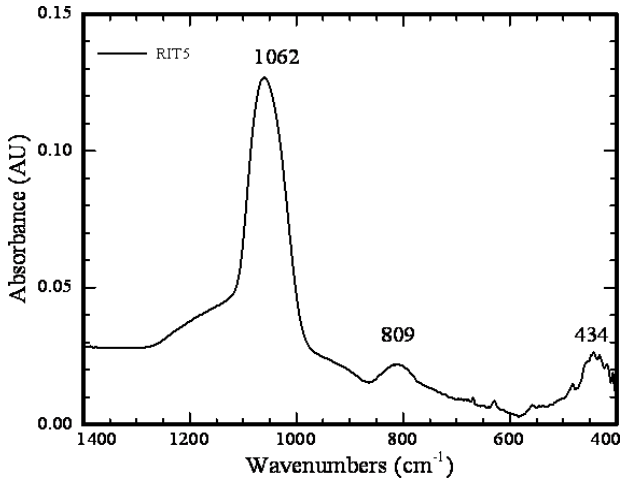

Figure 4.3: FTIR absorbance spectrum for a TEOS sample prepared at RIT.

Table 4.1: Infrared absorptions for plasma-deposited silicon dioxide [14].

Wavenumber, cm^{-1}		
Median	Range	Assignment
3620	3605-3650	Si-OH
3380	3340-3390	H_2O, Si-OH
2270	2260-2280	Si-H
1070	1040-1080	SiO_2
940	930-950	Si-OH
885	880-886	Si-H, Si-OH, Si-O, SiO_2, Si_2O_3
805	800-815	SiO_2
450	445-450	SiO_2

Prism Coupler Thin-Film Measurements

The prism coupler can be used to determine the refractive index and thickness of a thin film. Both parameters are obtained simultaneously and with good accuracy. The method uses a monochromatic laser in conjunction of a coupling prism of known index. Figure 4.4 shows the cross-section of a prism coupler used to measure index of refraction

and thickness of an unknown film. Figure 4.5 shows an example of the intensity vs. angle of incidence for a thin film sample.

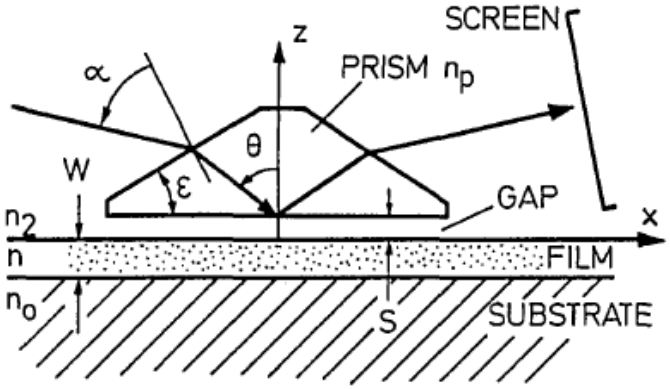

Figure 4.4: Schematic cross section of a prism coupler used in determining film thickness and refractive index [15].

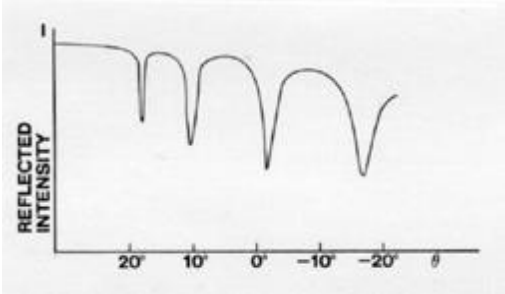

Figure 4.5: Intensity readout of a prism coupler showing the m=0, 1, 2, 3 order minima's [16].

By using this method, the deposited thin film acts as a waveguide. In a waveguide there are a discrete number of modes that can be supported based on the propagation constant. Equation (4.8) shows the relationship between the observed propagation constant, β_m and allowed propagation angles (see Figure 4.4 for context).

Once the allowed propagation angle is known, the index can be solved, equations (4.9), (4.10), (4.11), (4.12), (4.13), (4.14) & (4.15). The distance between drops in reflectivity of the intensity beam can be related to the film thickness and index, as they relate to higher order modes of propagation.

$$\beta_m = n_p k \sin\theta_m \quad \textbf{(4.8)}$$

$$n_2 \sin(\alpha - \varepsilon) = n_p \sin(\theta_m - \varepsilon) \quad \textbf{(4.9)}$$

$$k = \frac{2\pi}{\lambda_o} \quad \textbf{(4.10)}$$

$$\beta_m = k\, n \cos\theta_m \quad \textbf{(4.11)}$$

$$2\, m\, \pi = 2\, k\, n W \sin\theta_m - 2\varphi_{23} - 2\varphi_{21} \quad \textbf{(4.12)}$$

$$\sin\varphi_2 = n\, \beta_m / k \quad \textbf{(4.13)}$$

$$\tan\varphi_{23} = \left(n^2 \sin^2\varphi_2 - n_0^2\right)^{1/2} / \left(n_0^2 n \cos\varphi_2\right) n\, \beta_m / k \quad \textbf{(4.14)}$$

$$\tan\varphi_{21} = \left(n^2 \sin^2\varphi_2 - n_3^2\right)^{1/2} / \left(n_3^2 n \cos\varphi_2\right) n\, \beta_m / k \quad \textbf{(4.15)}$$

where W= film thickness, n_p = prisim index, n = film index, n_0 = substrate index, lambda = wavelength, k = propagation constant

4.2. Physical Materials Characterization

Profilometry Stress Measurements

Film stress is an important parameter that gives insight into the microstructure of a thin film. There are two components to thin film stress; thermal stress and intrinsic stress. When a film is deposited at a temperature that is different from the operating temperature, a thermal stress will be present due to the differences in the thermal

expansion coefficient of the substrate and film. The one dimensional thermal stress is approximated by equation (4.16).

$$\sigma_{th} = E_f(\alpha_f - \alpha_s)(T_s - T_a) \quad \textbf{(4.16)}$$

where E_f is Young's Modulus of the film, α_f and α_s are the average coefficients of thermal expansion for the film and substrate, T_s is the temperature during deposition, and T_a is the temperature during measurement.

A positive value of σ_{th} corresponds to a tensile stress [17]. For silicon and SiO_2 the thermal stress would be as follows, where the coefficients of thermal expansion for silicon and SiO_2 of $3x10^{-6}$ /K and $5.9x10^{-5}$ /K, respectively, and the Young's modulus of 75 GPa for SiO_2:

$$\sigma_{th} = 75GPa(0.59x10^{-6} - 3x10^{-6})(T_s - 300K) = -180.75Pa(T_s - 300K)$$

Assuming the deposition is above room temperature the expected stress state is compressive due to thermal stress alone.

Intrinsic stress can be defined as the component of the total measured stress that cannot be attributed to the thermal stress and is given by equation (4.17),

$$\sigma_{in} = \sigma_m - \sigma_{th} \quad \textbf{(4.17)}$$

where σ_{in} is the intrinsic stress and σ_m is the measured stress.

Intrinsic stress and microstructure in vacuum-deposited films are sensitive to the deposition conditions [17]. Therefore the change in the stress state of a thin film can be attributed to changes in microstructure caused by changes in the deposition conditions.

If the thin film is deposited on a flat substrate with known properties, the non-zero stress in the thin film will cause the substrate to bow and a stress to be introduced in the film as seen in Figure 4.6. This change in bow can be measured by profilometry and the total stress can be determined.

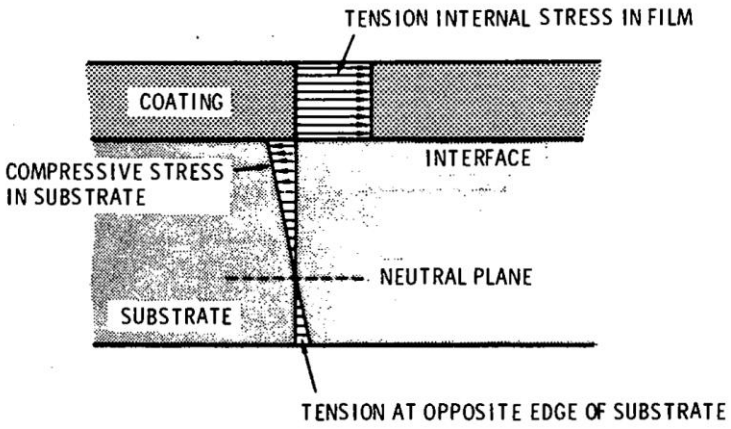

Figure 4.6: Schematic of the stress state of a thin film and substrate [17].

The change in the bow of polished silicon wafers can be measured via profilometry. If a film is deposited and the Young's modulus of the film and substrate are known, the film stress can be extracted.

Time of Flight Secondary Ion Mass Spectrometry, SIMS

SIMS is a very useful technique used to determine the atomic composition of a sample. SIMS has detection limits down to 10^{14} to 10^{15} cm^{-3} due to little background interference signal [12]. SIMS uses a sputter gun to remove layers of the sample; the sputtered material is then analyzed in a mass spectrometer and a spectrum is obtained. The spectrum peaks are monitored over the time and a count for each atomic weight is recorded. This atomic weight/charge count can then be correlated to a specific isotope and concentration profile.

Time-of-flight SIMS (TOF-SIMS) uses a pulsed ion beam from a liquid Ga^{+} gun. The gun is pulsed for nanoseconds and the sputtered ions are measured. A major advantage of TOF-SIMS is that narrow slits on the spectrometer are not needed and ion collection is increased by 10%-50%. This reduces ion current needed and therefore reduces the sputter rate, making it possible to analyze organic surface layers. [12] The ions are analyzed as the rate they arrive at the detector and no mass analysis is needed.

Etch Rates

Chemical etch rate measurements provide relative comparisons of composition and density of the deposited films. The wet etch reaction of SiO_2 and HF and SiO_2 and

buffered hydrofluoric acid (BHF) are shown in equation (4.18) [18]. Table 4.2 shows a list of common etch rates for select oxides and nitrides.

$$SiO_2 + 6HF \rightarrow H_2SiF_{6(aq)} + 2H_2O$$
$$SiO_2 + 4HF + 2NH_4F \rightarrow (NH_4)_2 SiF_{6(aq)} + 2H_2O \quad \textbf{(4.18)}$$

Table 4.2: Table of etch rates for certain oxides and nitrides in different wet chemistries [18].

Etchant Equipment Conditions	**Material**				
	Dry Oxide	**Wet Oxide**	**LTO**	**Stoic Nitride**	**Low-σ Nitride**
10:1 HF Wet Sink Room Temp	230 Å/min	230 Å/min	340 Å/min	11 Å/min	3 Å/min
5:1 BHF Wet Sink Room Temp	1000 Å/min	1000 Å/min	1200 Å/min	9 Å/min	3 Å/min
Phosphoric Acid Heated Bath w/ Reflux 160°C	0.8 Å/min	0.7 Å/min	<1 Å/min	30 Å/min	20 Å/min

The methods presented here are an independent way of assessing dielectric properties. In the following chapter the MOS device will be discussed. The MOS device is an assessment of electric properties of the dielectrics.

Chapter 5

Metal Oxide Semiconductor (MOS) Devices

The Metal Oxide Semiconductor (MOS) system is the basis of modern CMOS technology. The MOS system has been studied extensively due to its direct relationship to planar devices in ICs. In this chapter we will discuss the fundamentals of the MOS device and how operational parameters discussed in previous chapters, can be extracted using these devices.

5.1. Two Terminal Structure (Capacitor)

Capacitance-Voltage (C-V) measurements are useful in determining oxide charge. The following discussion will explain how a C-V measurement is taken and how to interpret the results. Equation (5.1) is the definition of capacitance.

$$C = \frac{dQ}{dV} \tag{5.1}$$

Capacitance is defined as the change in charge due to a change in voltage. During a capacitance measurement an ac voltage (~ ±0.015 V) is superimposed on top of a dc voltage (~-5 to 5 V). The resulting change in charge is the capacitance. For p-type silicon the capacitance equation can be rewritten as seen in Equation (5.2).

$$C = -\frac{dQ_s + dQ_{it}}{dV_{ox} + d\Psi_s} \tag{5.2}$$

where Q_s is the charge in the silicon, Q_{it} is the oxide-silicon interface charge; V_{ox} is the voltage dropped across the oxide; and ψ_s is silicon surface potential.

Qs can be broken down into the contribution of charges from holes (Q_p), electrons (Q_n), and space-charge or bulk charge (Q_b) of the silicon. Equation (5.2) can be rewritten in terms of capacitance as seen in Equation (5.3) where C_{OX} is defined in Equation (5.3).

$$C = \frac{C_{ox}\left(C_p + C_b + C_n + C_{it}\right)}{C_{ox} + C_p + C_b + C_n + C_{it}} \tag{5.3}$$

$$C_{OX} = \frac{\varepsilon A}{t_{OX}} \tag{5.4}$$

There are four stages of a p-type silicon MOS capacitor. A general CV plot can be seen in Figure 5.3. The first stage is accumulation—in this stage the capacitance due to the majority carrier, i.e. holes, dominates (C_p). The accumulation capacitance is very large and the total capacitance becomes C_{ox}. The second stage is depletion. Here the capacitance dominated by the bulk charge ($Q_b = -qN_AW$), and interface charge (Q_{it}). The total capacitance is given by Equation (5.5).

$$C = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_b + C_{it}}} \tag{5.5}$$

The third stage is weak inversion. If the ac frequency is sufficiently low enough for the minority carrier to respond the capacitance is dominated by the electron charge (Q_n), the interface charge (Q_{it}), and the bulk charge (Q_b). The total capacitance can then be written as Equation (5.6).

$$C = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_b + C_{it} + C_n}} \tag{5.6}$$

The fourth stage is inversion. If the ac frequency is sufficiently low enough ~ < 3Hz at room temperature, the inversion charge will respond to the ac voltage and will dominate. The inversion charge will be very large; leaving the total capacitance is Cox. Figure 5.1 shows a MOS cap under general bias conditions and the potential distributions. Figure 5.2 shows the magnitude of the inversion charge for a MOS capacitor. This can be related directly to the ID-VG sweep of a transistor, as the inversion charge is the current carrier in the on state.

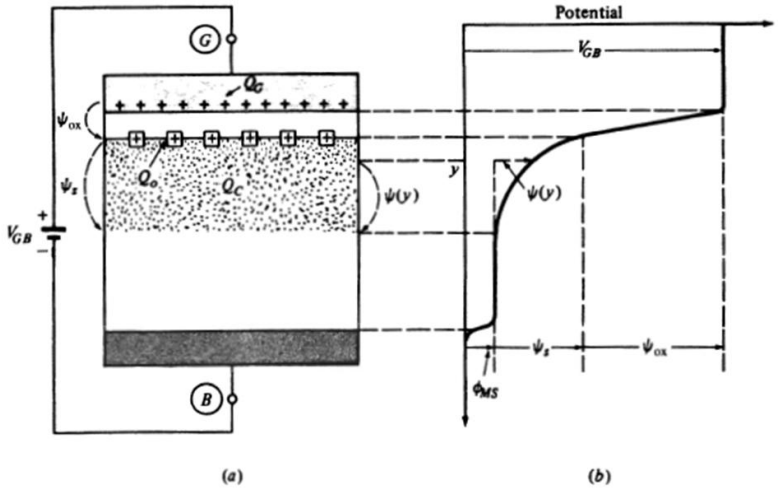

Figure 5.1: (a) A p-type substrate two-terminal MOS structure under general gate bias. (b) Potential distribution assuming the gate, substrate cap, and external wires are all made of the same material (assuming ψs > 0) [19].

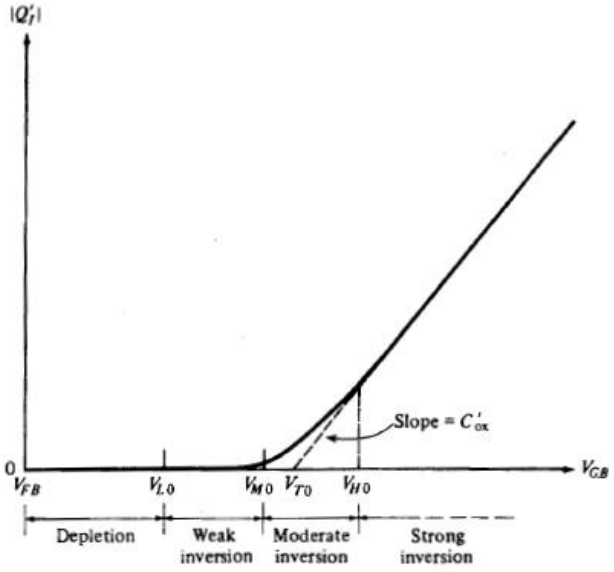

Figure 5.2: Magnitude of inversion charge per unit area vs. gate-substrate bias voltage [19].

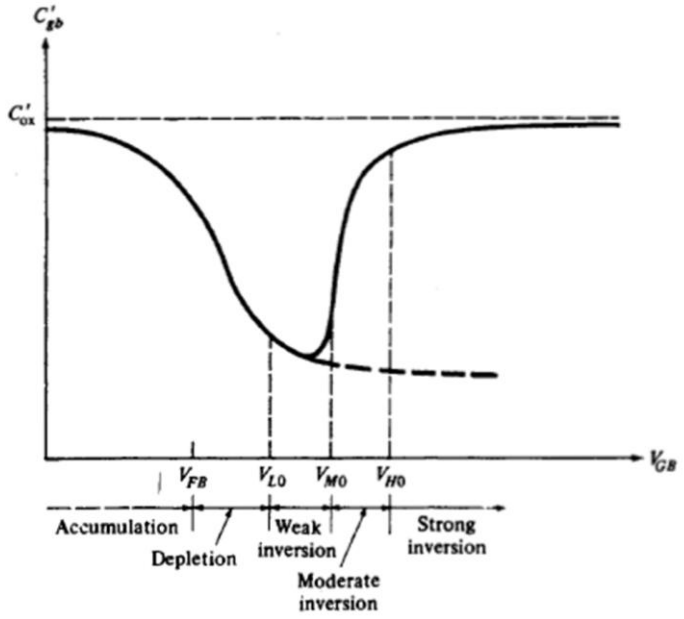

Figure 5.3: Diagram of a C-V curve showing the different regions of operation [19].

An important parameter in a C-V measurement is the flatband-voltage (V_{FB}). The flatband-voltage is the voltage applied to the gate equal to the metal-semiconductor workfunction (φ_{MS}) in an ideal oxide with no charge. In actuality V_{FB} is composed up of φ_{MS} and oxide charges as seen in Equation (5.7).

$$V_{FB} = \varphi_{MS} - \frac{Q_f}{C_{ox}} - \gamma\frac{Q_m}{C_{ox}} - \gamma\frac{Q_{ot}}{C_{ox}} - \frac{Q_{it}(\psi_s)}{C_{ox}} \qquad \textbf{(5.7)}$$

where γ is a position dependent variable that ranges between 0 and 1. Gamma is 0 when at the oxide metal interface and 1 when at the silicon oxide interface.

Shifts in the flatband voltage can be useful in determining an effective fixed and trapped charge in the oxide. A useful technique in determining the mobile ions in an oxide is the Bias-Temperature Stress Test. This technique heats the MOS cap to ~200-

300˚C and applies a bias to the gate. This moves the mobile ions (Na+, K+, Li+) to one of the oxide interfaces. The sample is cooled and a C-V measurement is taken and the flatband extracted. The MOS cap is then stress with the opposite bias at elevated temperatures. The mobile ions are then moved to the opposite oxide interface. The sample is cooled and V_{FB} is again extracted and the difference in V_{FB} is due to the mobile ions in the oxide.

There are several methods to determine the interface trap charge density distribution. They include the low-frequency (quasistatic) method, conductance method, Terman method, Gray-Brown and Jenq method, charge pumping method, and the MOSFET subthreshold current method. These methods are discussed in [12]. Interface trap charge is a function of surface potential and therefore a function of gate voltage in a MOS device. Interface traps cause a stretching of both I-V and C-V curves in the three and two terminal devices because the interface traps are responding to the applied field as well as the channel carriers.

5.2. Gate Oxide Integrity, GOI

Oxide integrity is determined by zero-time and time-dependent measurements. Some of the methods include ramp voltage dielectric breakdown (RVDB) or “zero-time”

breakdown, time-dependent dielectric breakdown (TDDB) and Charge to breakdown. RVDB is performed by sweeping the gate voltage quickly and breakdown is observed as an abrupt increase in current. The extracted parameter is known as the breakdown electric field. TDDB is performed by holding the gate voltage constant and breakdown occurs when a sharp increase in the current is observed. Charge to breakdown is performed by holding the gate current constant and breakdown occurs when a sharp decrease in voltage is observed. An example of a charge to breakdown measurement is shown in Figure 5.4. The extracted parameter is known as charge to breakdown (Q_{DB}) and is given in Equation (5.8).

$$Q_{DB} = \int_0^{t_{BD}} J_G dt \qquad \textbf{(5.8)}$$

where J_G is gate current density.

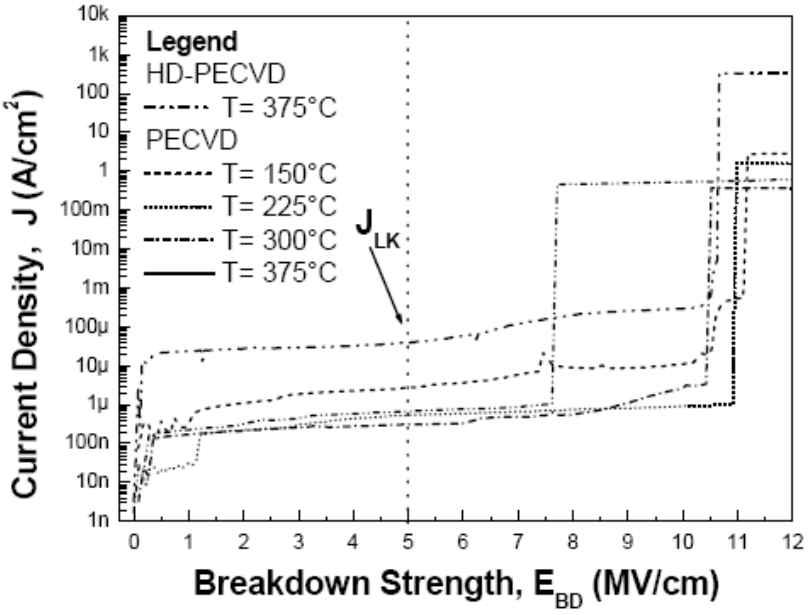

Figure 5.4: Electrical breakdown of different PECVD film [8].

5.3. MOS Field Effect Transistor (MOSFET)

The metal oxide semiconductor field effect transistor is affected by the same gate oxide non-idealities as the MOS cap, namely altering V_{FB}. As can be seen in Figure 5.5, the MOSFET is a MOS cap with a source of channel minority carriers on either side of the channel; this allows for the inversion layer to respond to high frequencies and if the inversion layer is formed current can flow from one terminal to the other. The gate can therefore be used as a switch and logic circuits can be made. The current equation for a MOS cap is shown in Equation (5.9). The threshold voltage equation is shown in Equation (5.10).

$$I_{DS} = \begin{cases} \frac{W}{L}\mu C_{OX}'\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^{\ 2}}{2}\right] & V_{DS} \le V_{DS}' \\ \frac{W}{L}\mu C_{OX}'\frac{(V_{GS}-V_T)^2}{2} & V_{DS} > V_{DS}' \end{cases} \quad \textbf{(5.9)}$$

$$V_T = V_{FB} + 2\phi_f + \frac{1}{C_{ox}'}\sqrt{2q\varepsilon_0\varepsilon_{Si}N_A(2\phi_f)} \quad \textbf{(5.10)}$$

where W is the width of the transistor, L is the length of the transistor, μ is the channel mobility, V_T is the threshold voltage, C_{ox} is the oxide capacitance, V_{FB} is the flatband voltage, V_{DS} is the voltage difference between the drain and source of the transistor, φ_f is the metal workfunction, N_A is the acceptor doping, q is the charge of an electron, ε_0 is the relative permittivity, ε_{si} is the relative permittivity for silicon

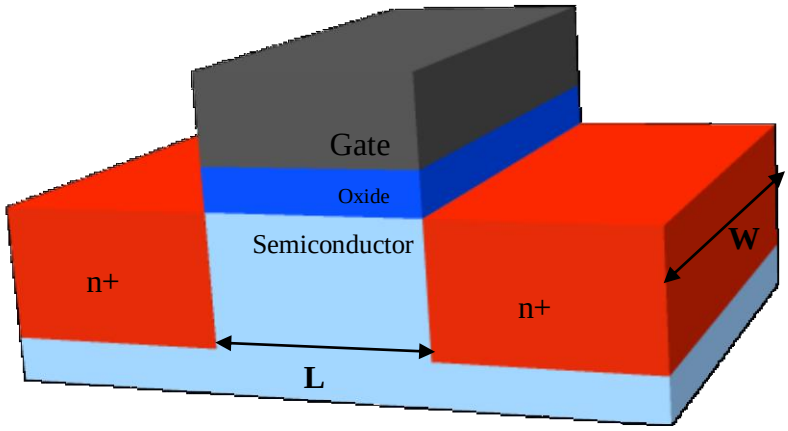

Figure 5.5: Cross-section of an n-MOSFET.

The mobility, μ, is affected by the interface and fixed charge of the gate oxide causing carrier scattering. The threshold voltage, V_T, is dependent on the flatband voltage, which is affected by the charges in the oxide. The oxide capacitance, Cox is affected by oxide thickness variation. While these gate oxide non-idealities are typically nonuniform, circuit designs require that these parameters be well controlled and minimized.

Chapter 6

Two-terminal MOS Devices

6.1. Experiments

The screening process of potential gate dielectrics consisted of fabricating MOS devices. Fabricated two terminal MOS devices that did not seem promising were eliminated. This methodology removed many potential gate dielectrics from the three terminal experiment, but as will be shown later there may be some interest in fabricating certain dielectrics in an integrated three terminal structure in future work as there was an observed interaction between with the gate metal on the three terminal process, improving characteristics.

The development of the dielectrics took place using an Applied Materials P-5000 PECVD system. Figure 6.1 shows the P-5000 and the input and output parameters. The experimental plan was split into three distinct steps or phases. The first phase focused on the deposition process and the physical properties of the film, as well as some initial electrical results. Phase one utilized a physical profilometry measurement to determine the film stress, an interferometer to determine film thickness and uniformity, and a LCR meter with a Hg probe to gather some C-V relationships. The second phase focused on fabricating two-terminal MOS devices (capacitors) and extracting C-V characteristics.

The third phase focused on fabricating three terminal MOS devices (NFETs) and extracting I-V characteristics and C-V characteristics from integrated capacitors.

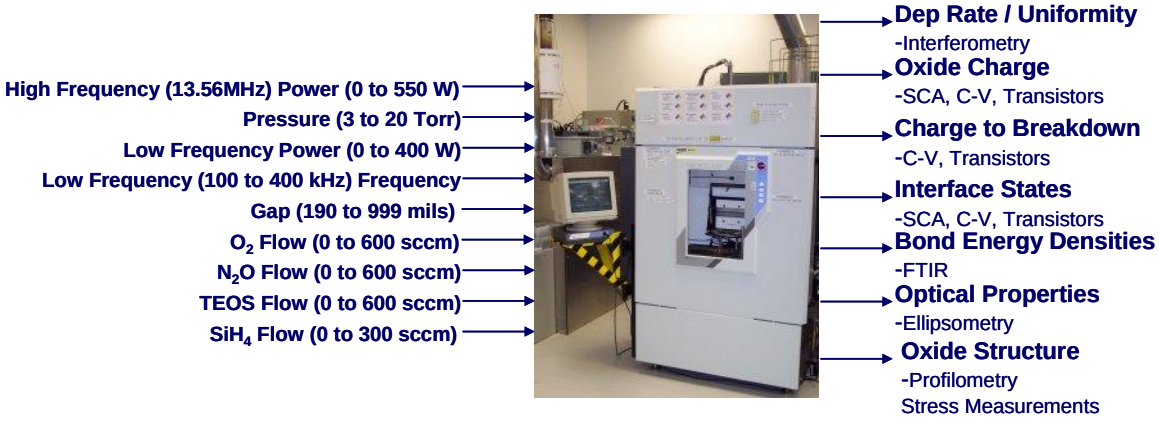

Figure 6.1: Picture of the Applied Materials P-5000 and input and output parameters.

6.2. Two-Terminal MOS Process

There are two different processes used to make MOS devices, each using a different gate metal. All devices were made on 150mm silicon wafers of (100) crystal orientation. A standard RCA clean was done followed by a dilute HF etch to remove any chemical oxide. Figure 6.2 through Figure 6.4 show the fabrication sequence for a MOS device using a mercury gate metal. Figure 6.2 shows the starting silicon wafer.

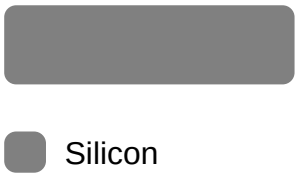

Figure 6.2: Starting substrate is (100) silicon.

The gate oxide was then deposited using a PECVD process. Several different process parameters were investigated. Figure 6.3 shows the cross-section of the MOS structure after the gate oxide has been deposited.

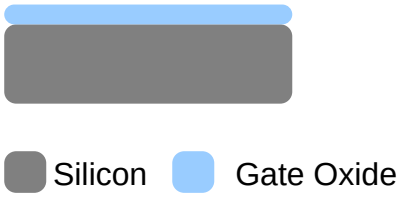

Figure 6.3: Cross-section of a MOS structure after gate oxide deposition.

After gate oxide deposition there were two methods to fabricate a MOS device. The first used mercury as the gate metal; the second used aluminum as the gate metal. This method isolates any effects that the deposition of the gate metal may have had on the device performance. An anneal in forming gas (N_2/H_2 5%) is completed at 400 ˚C for 15 min before testing with mercury. Figure 6.4 shows the cross-section of the MOS device using mercury as the gate metal.

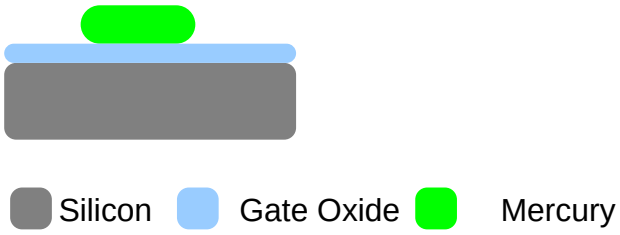

Figure 6.4: Cross section of the MOS device using mercury as the gate metal.

Figure 6.5 through Figure 6.9 show the fabrication sequence for a MOS device using an aluminum metal gate. Figure 6.5 shows the starting substrate (100) silicon wafers.

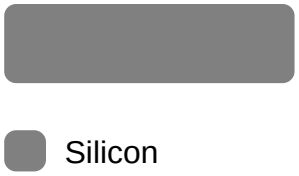

Figure 6.5: Starting (100) silicon substrate.

Gate oxide is then deposited on the silicon substrate. Figure 6.6 shows the MOS device after gate oxide deposition.

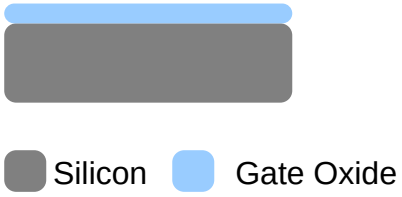

Figure 6.6: Gate oxide deposited on silicon substrate.

Aluminum is then deposited on the wafer using an evaporation process in a tungsten resistive heater basket. Figure 6.7 shows the MOS device after aluminum gate metal deposition.

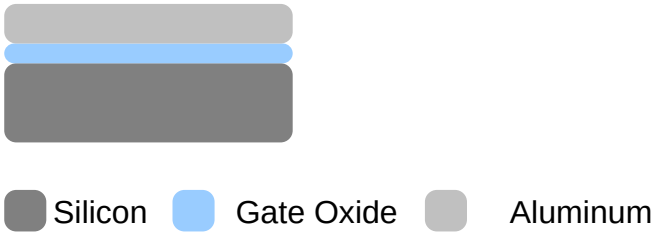

Figure 6.7: Aluminum deposited on gate oxide as gate metal.

The aluminum is then patterned to form the gate of the MOS device, defining the area in equation (5.3).

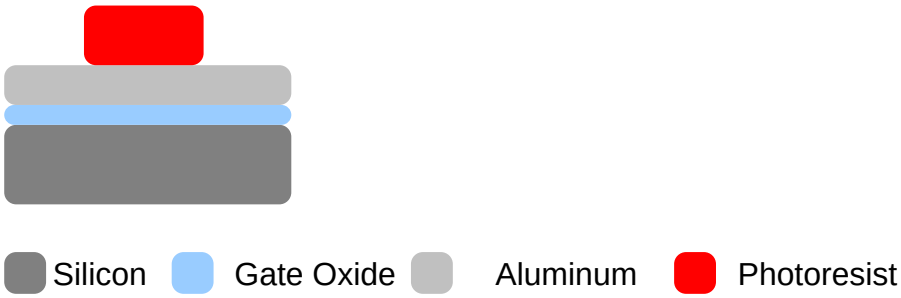

Figure 6.8: Photolithograph of aluminum.

The aluminum is then etched using wet acid chemistry and photoresist is removed using a heated solvent strip. The devices are then annealed in a forming gas ambient at 400C for 15min. Figure 6.9 shows the completed MOS device with an aluminum gate metal.

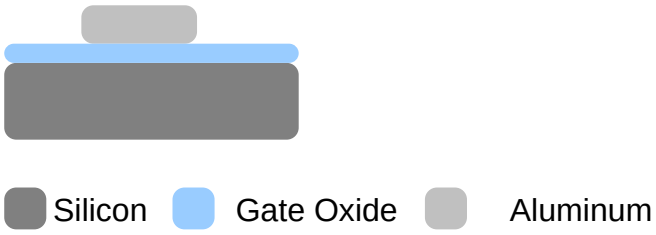

Figure 6.9: Aluminum after being etched.

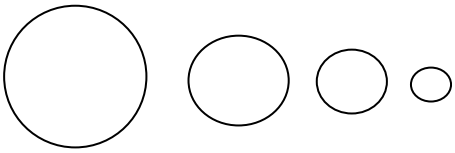

Figure 6.10: Diagram of fabricated circular capacitors ranging in diameter from 0.0357 to 0.1596 cm.

6.3. PECVD TEOS Oxide Standard

Initial characterization of PECVD TEOS films using the standard process used for inter-level dielectric films was completed. The process recipe details were as follows: Power 290 W, pressure 9 Torr, TEOS flow 400 sccm, O_2 flow 285 sccm, electrode gap 290 mils. The stress relaxation study demonstrated a significant change in stress of ~200 MPa from tensile to compressive over a one week period; the results are shown in Figure 6.11. This is characteristic of a porous film, allowing moisture to absorb into the film [20]. Although the initial stress condition of the film is restored after the 8 hr anneal

at 600 ˚C in nitrogen ambient, the stress relaxation is quite different suggesting a structural change during the annealing process.

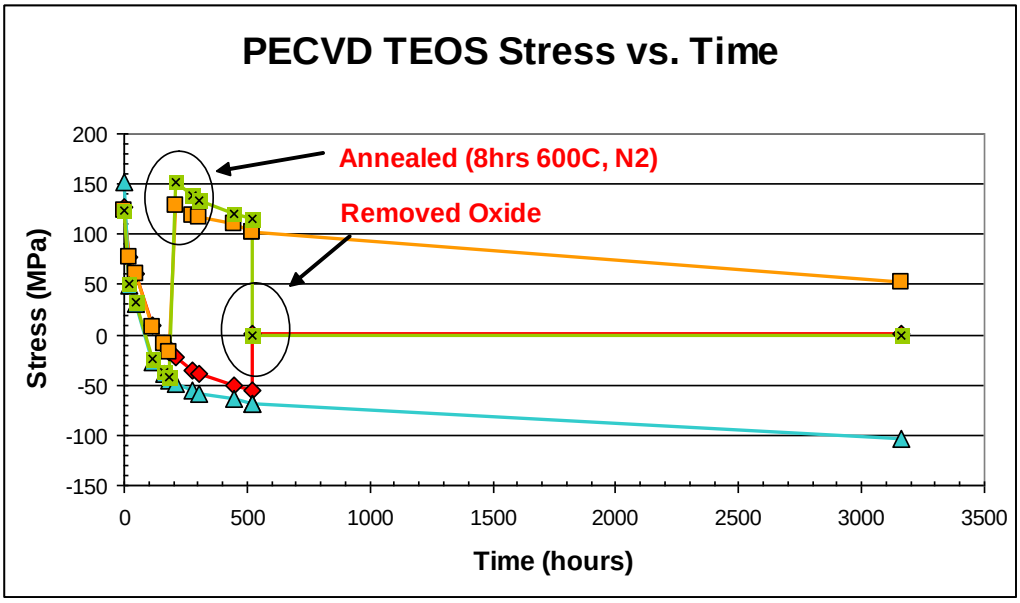

Figure 6.11: Stress relaxation study of the standard PECVD TEOS process.

C-V measurements were also taken of the current PECVD TEOS film, shown in Figure 6.12. Note that this film is used as an inter-level dielectric, rather than a gate dielectric. Table 6.1 shows the index values measured by the prism coupler technique (discussed in section 4.1). The index values are lower than standard oxide, which is consistent with a porous film [20].

Table 6.1: Index values of the standard PECVD TEOS recipe (λ=632 nm).

Location	TEOS Ox	Thermal Ox	Delta
1	1.4429	1.4579	-1.49%
2	1.4432	1.4578	-1.46%
3	1.4435	1.458	-1.43%
4	1.4427	1.458	-1.51%
5	1.442	1.4579	-1.58%
Avg	1.4429	1.4579	-1.50%

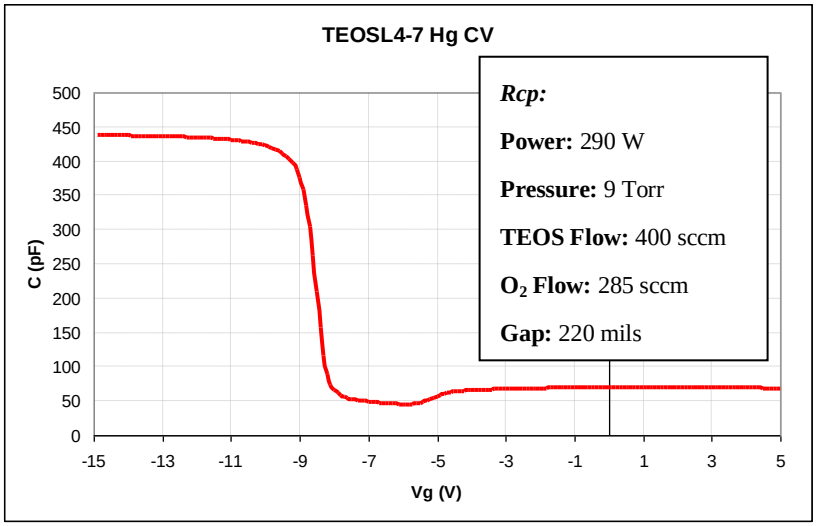

Figure 6.12: C-V measurement of the standard PECVD TEOS recipe used in the SMFL using an aluminum gate and a 0.002 cm2 area capacitor.

The standard TEOS sample showed a high level of oxide charge (~$2x10^{12}cm^{-2}$) and a low index value compared to a thermally oxidized silicon substrate, indicating a porous film [20]. Having a high charge level leads to a large flatband voltage, which is not desirable for fabricating transistors and therefore is not suitable for a TFT gate dielectric process.

FTIR measurements were completed on the standard PECVD TEOS recipe on both 150mm wafers and 100mm wafers using a 150mm silicon wafer carrier during oxide

deposition. The results, seen in Figure 6.13, show an additional adsorption peak on the sample that used a wafer carrier during the PECVD process; perhaps due to poor thermal conductivity, as the sample not using a carrier does not show the additional adsorption peak. Therefore all samples throughout the two-terminal investigation were limited to 150mm wafers.

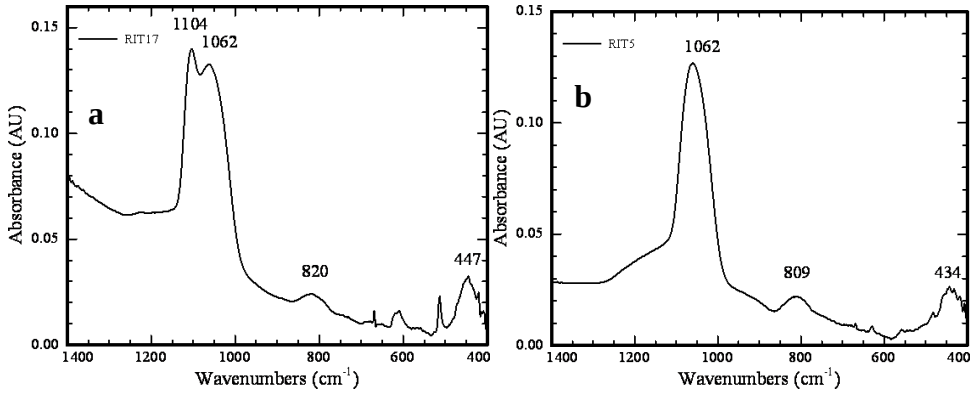

Figure 6.13: FTIR spectrum of PECVD TEOS taken on 100mm samples **(a)** and 150 mm samples **(b)**.

6.4. Investigated Dielectrics and Two-terminal MOS Results

Table 6.2 shows the different gate oxide treatments for the capacitors fabricated on 150 mm substrates, followed by C-V characterization. Samples are labeled by lot number then wafer number (L *lot# - wafer#*). Figure 6.14 shows the C-V curve of sample L7-6, which had a high O_2 to TEOS ratio during gate oxide deposition. These results demonstrated an interface charge level $Q_{it} \sim 10^{11}$ cm^{-2}, which was a significant improvement over the results shown in Figure 6.12.

Table 6.2: Treatment combinations that were used in the MOS fabrication.

ID	Temperature (C)	Pressure (mTorr)	Gas Flows	Power (W/cm^2)	Gap (Mils)	Time (sec)
L7-04	250	300	60sccm SiH_4 120sccm O_2	1.41	700	4
L7-6	300	1000	40sccm TEOS 450sccm O_2	2.26	700	150
L7-11	250	300	60sccm SiH_4 120sccm O_2	1.41	700	4
L7-18	250	300	60sccm SiH_4 10sccm N_2O 110sccm O_2	1.41	700	4
L7-19	250	300	60sccm SiH_4 30sccm N_2O 90sccm O_2	1.41	700	4
L7-20	250	300	60sccm SiH_4 10sccm N_2 110sccm O_2	1.41	700	4
L7-21	250	300	60sccm SiH_4 30sccm N_2 90sccm O_2	1.41	700	4
L7-22	250	300	60sccm SiH_4 15sccm N_2 200sccm O_2	1.41	700	4

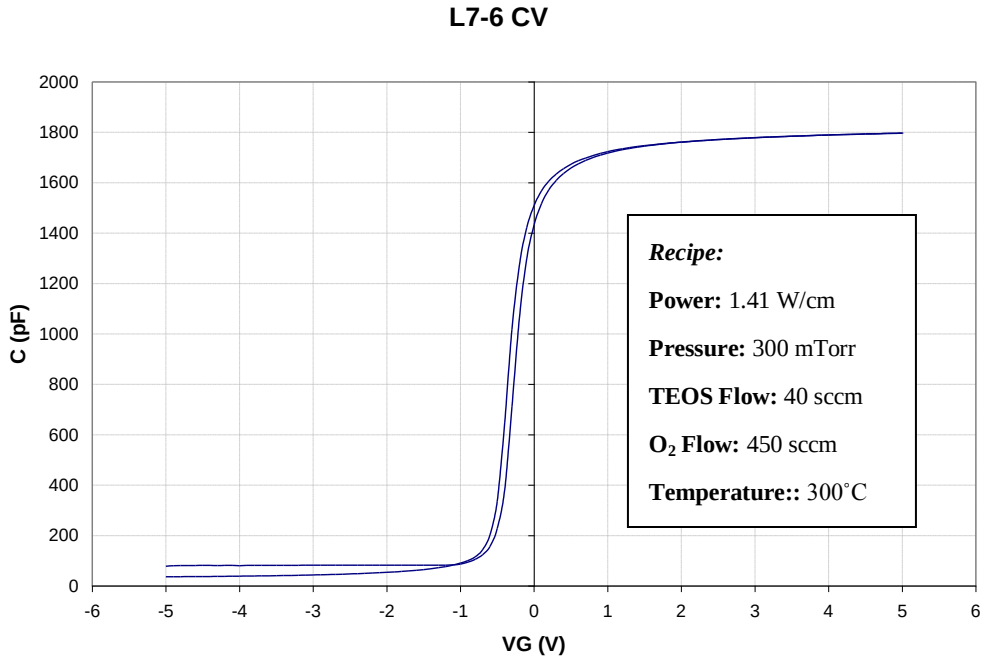

Figure 6.14: C-V plot of a sample that was deposited using a ratio of TEOS to O2 of 1:11.25 and pressure of 1 Torr. The device used aluminum gate metal and a 0.002 cm2 area capacitor.

Figure 6.15 shows the C-V curve overlay of L7-04 and L7-11 which had the same deposition conditions and different post-deposition anneals. L7-04 was sintered in forming gas (5% H_2 in N_2) with no capping layer and then mercury was used as the gate metal to obtain a C-V curve. L7-11 had an Al capping layer during sinter and Al was used as the gate metal. The results show that there is an interaction with the capping layer that is used during the anneal process. It is proposed that aluminum acts as a catalyst releasing monatomic H^+, which passivates dangling bonds at the dielectric / silicon interface and any mobile charges that may cause hysteresis [2,4].

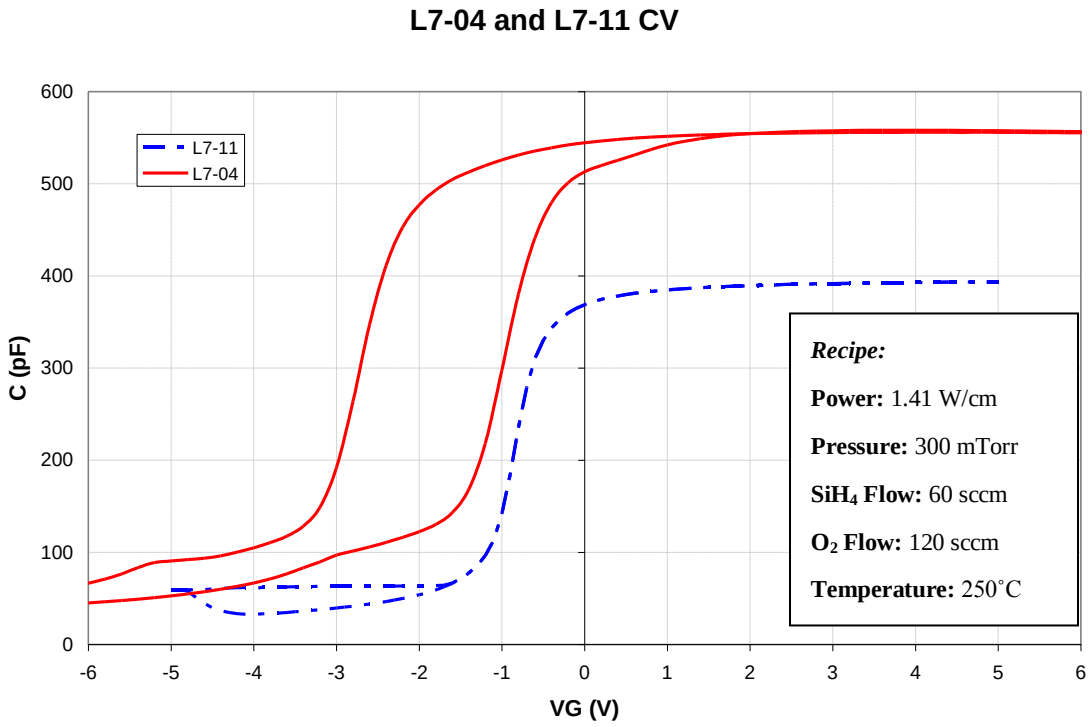

Figure 6.15: Overlay of L7-04 and L7-11 showing elimination of hysteresis with the use of an Al capping layer during sintering. The device used aluminum gate metal and a 0.002 cm2 area capacitor.

Figure 6.16 shows the C-V curves of L7-18, again showing that the oxide charge and hysteresis are dramatically improved with the addition of an anneal with Al as the capping layer. After deposition the sample was separated into 4 pieces and each peace received a different post processing. One was measured as deposited, another was measured after an anneal in forming gas at 400˚C for 15min, another was annealed with forming gas with an Al cap and after the Al was removed the sample was measured with Hg as the gate. The last piece was annealed with forming gas with the Al capping layer, and Al was patterned as the gate and measured, with results shown in Figure 6.21 along with other samples with aluminum gates.

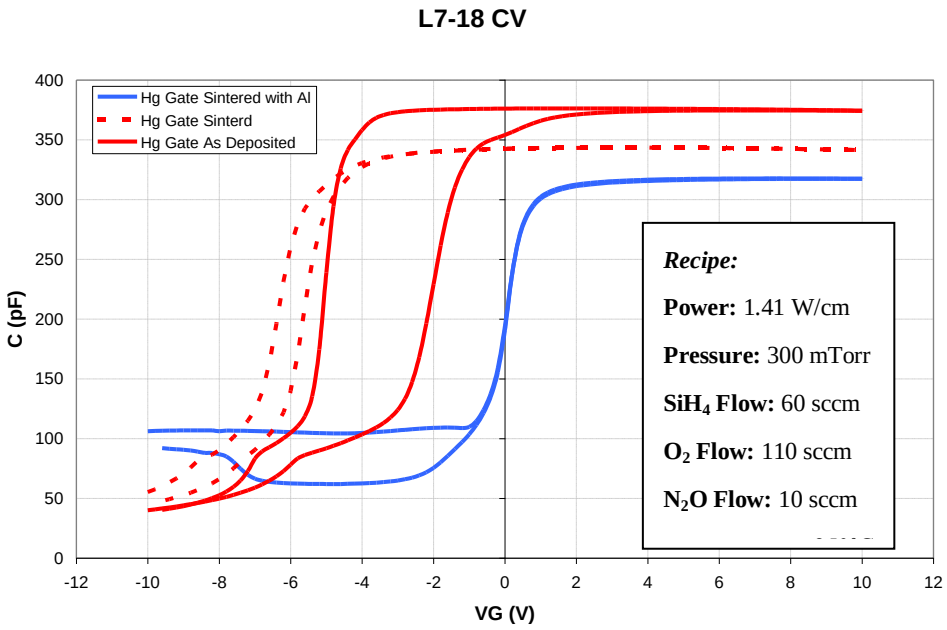

Figure 6.16: Overlay of L7-18 with different post gate oxide deposition annealing processes, showing elimination of hysteresis with the addition of an Al capping layer with use of a Hg gate during testing.

Figure 6.17 shows the C-V overlay for L7-19 with the same post anneal treatments as L7 - 18. The results show a similar trend as the previous figures; by adding an Al layer during a low temperature anneal, charge levels are reduced more than if no layer is present.

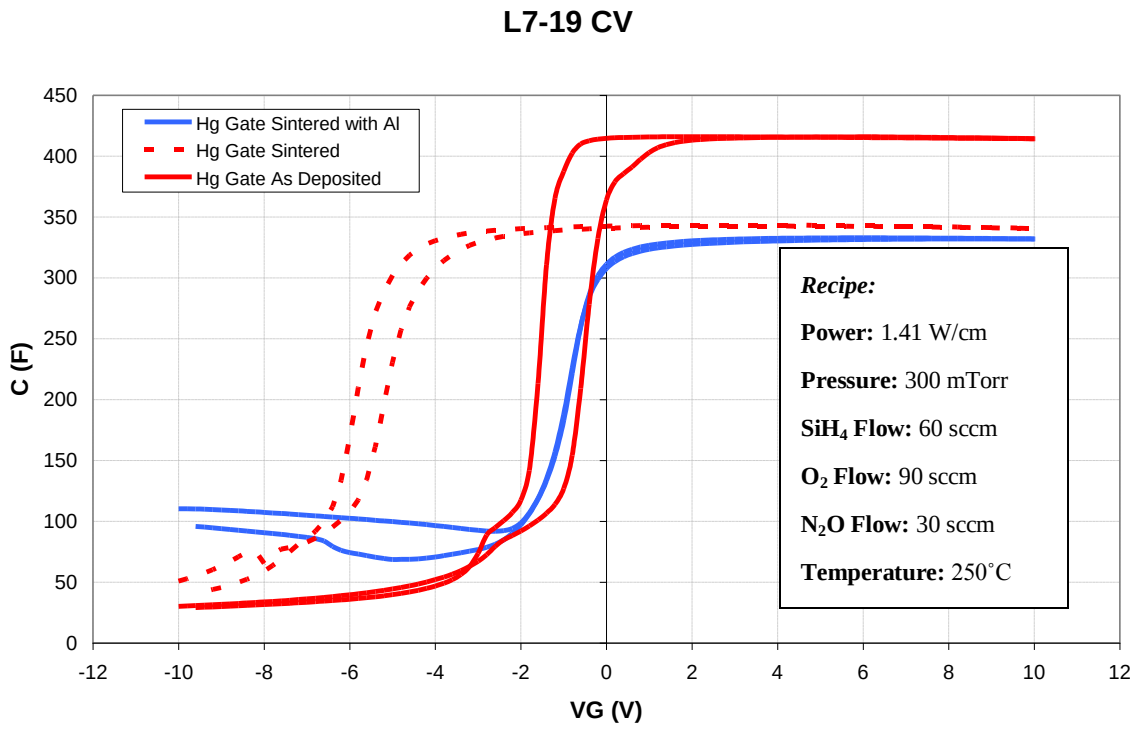

Figure 6.17: Overlay of L7-19 with different post gate oxide deposition annealing processes, showing elimination of hysteresis with the addition of an Al capping layer.

Figure 6.18 shows the C-V overlay for L7-20 with the same post anneal treatments as L7-18. The same results can be seen with this treatment as can be seen with the other deposition recipes, the Al layer is critical in reducing charge levels in the dielectric and at the interface.

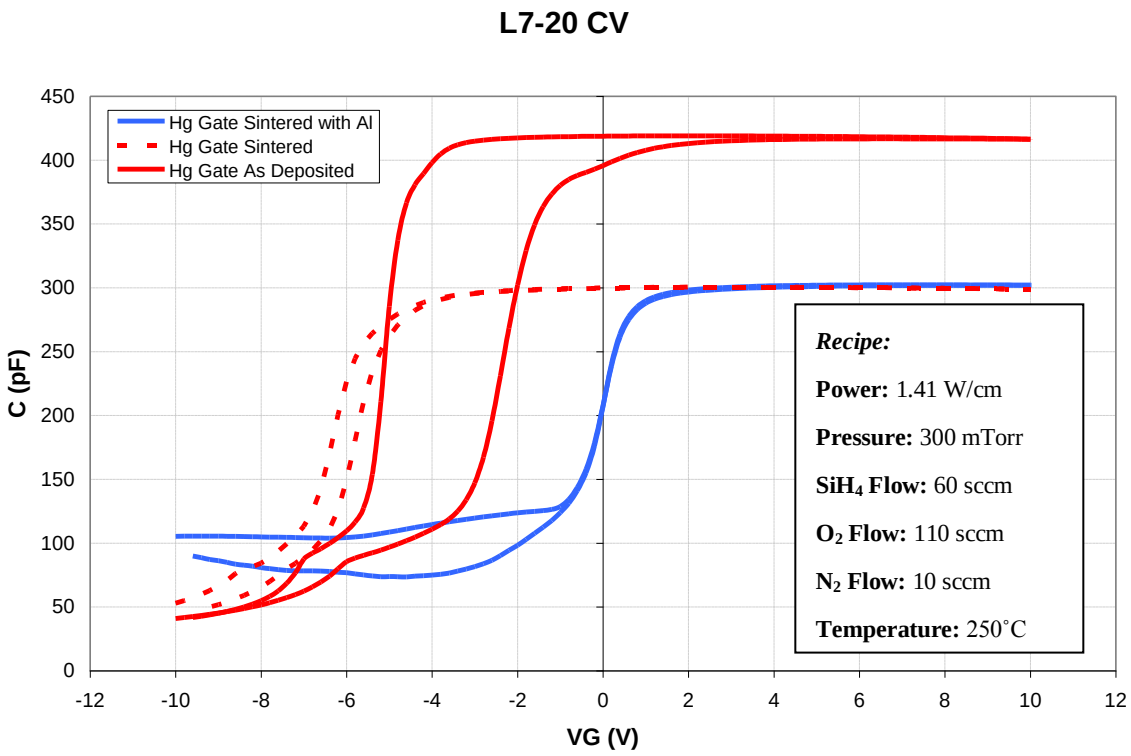

Figure 6.18: Overlay of L7-20 with different post gate oxide deposition annealing processes, showing elimination of hysteresis with the addition of an Al capping layer.

Figure 6.19 shows the C-V overlay for L7-21 with the same post anneal treatments as L7 -18. The results in this case are not as promising as other samples with the Al layer present during the post-deposition anneal. This may be due to the reduced flow of O_2 compared to the other treatments.

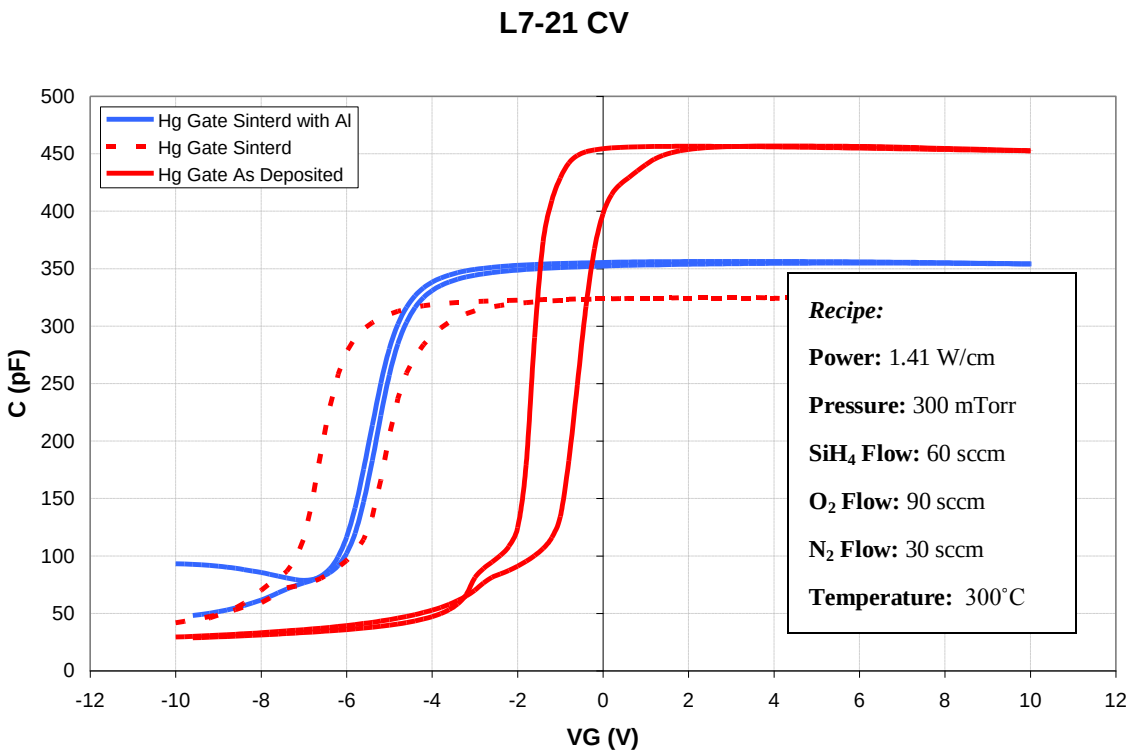

Figure 6.19: Overlay of L7-21 with different post gate oxide deposition annealing processes, showing reduction of hysteresis with the addition of an Al capping layer.

Figure 6.20 shows the C-V overlay for L7-22 with the same post anneal treatments as L7-18. This treatment uses a higher flow of O_2, and shows a similar trend to the other results besides L7-21. Note that the treatment annealed with an Al capping layer demonstrated the lowest charge level.

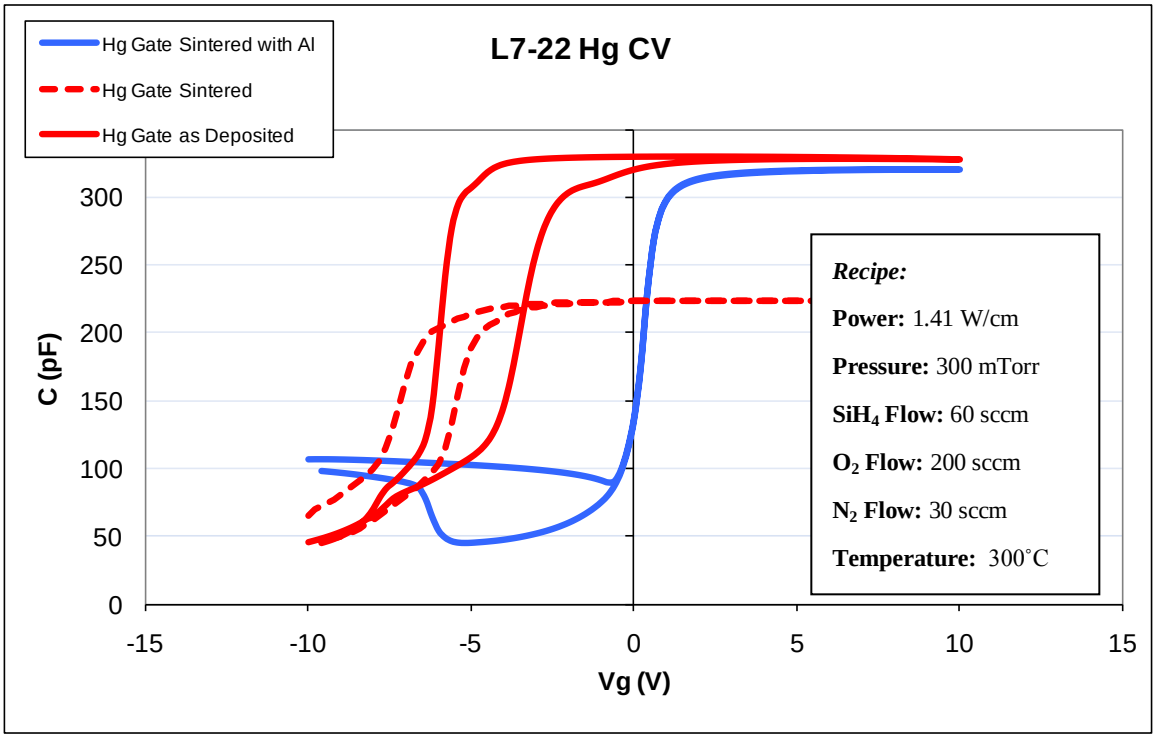

Figure 6.20: Overlay of L7-22 with different post gate oxide deposition annealing processes, showing elimination of hysteresis with the addition of an Al capping layer.

Figure 6.21 shows the overlay of L7-18, L7-19, L7-20, L7-21, & L7-22 for the pieces that received an anneal with an Al capping layer and had an Al gate. The results show that all treatments have low ~10^{11} cm^2 charge levels. The treatment that showed high levels of charge using the Hg probe and an aluminum capping layer demonstrated low charge levels with the Al gate, L7-21; this discrepancy is not understood. Note that the influence of dielectric leakage is observed in the accumulation mode capacitance at relatively low gate bias.

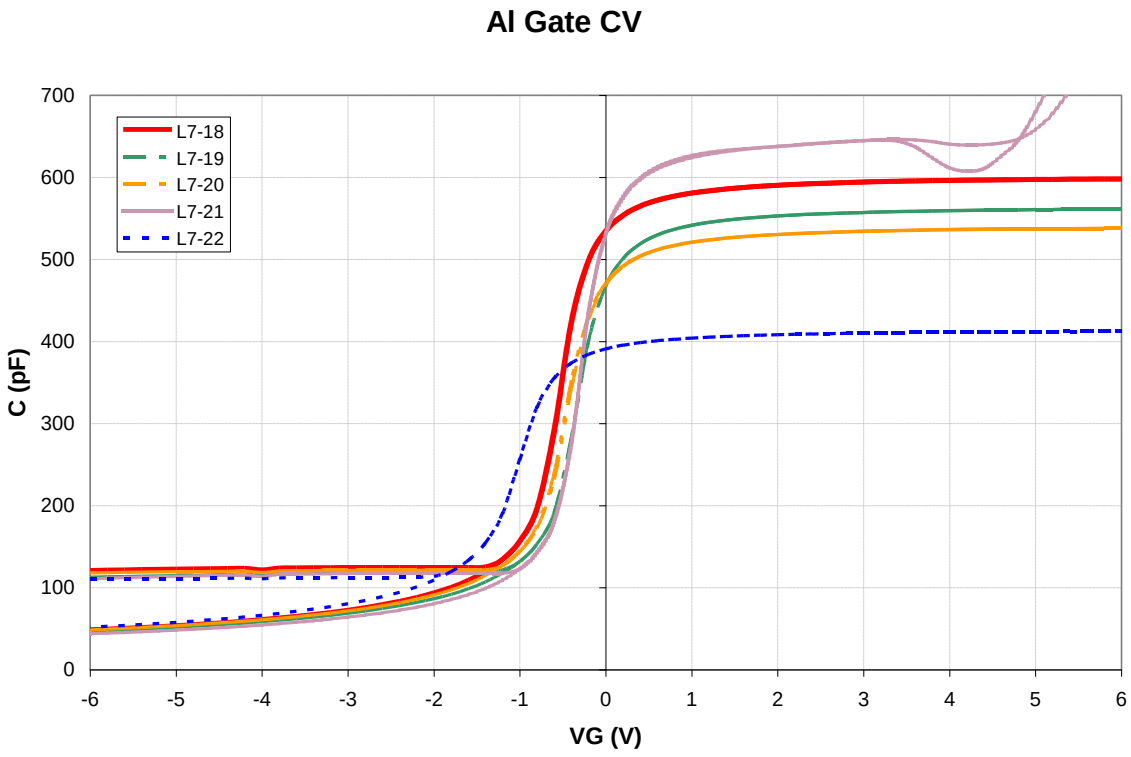

Figure 6.21: Overlay of C-V curves on samples with an Al gate and Al during sinter. The devices used an aluminum gate metal and a 0.002 cm2 area capacitor.

The results in this section show that there is a significant benefit to annealing dielectrics in the presence of an aluminum capping layer. A reduction in hysteresis and fixed charge is observed compared to samples that did not receive this treatment. This is important to note for the three terminal MOS devices, since aluminum is not available as a gate metal option.

Investigation Disruption and Continuation

In order to have a PECVD gate dielectric process that was compatible with transistor fabrication on 100 mm substrates, and provided acceptable process control, certain adjustments to the PECVD system and recipes were made. This included mass flow controller range adjustments for appropriate gas flow settings, introducing the silicon carrier for 100 mm substrates, increasing the time for temperature stabilization prior to film deposition. Test runs were performed to verify the new tool configuration and process settings, with C-V and electrical breakdown results shown. Table 6.3 shows the recipes that were verified and the changes in the previous recipes. Figure 6.22 shows the dielectric breakdown results for the different treatment combinations fabricated using the described treatment combinations.

Table 6.3: Treatment combinations that were used to verify tool modifications impact on MOS results.

ID	Recipe	Temperature (C)	Pressure (mTorr)	Gas Flows	Power (W/cm^2)	Gap (Mils)	Time (sec)	Comment
GC2	TEOS	300	1000	40 sccm TEOS 450 sccm O2	2.26	700	150	
TEOS4	TEOS	300	1000	40 sccm TEOS 450 sccm O2	2.26	700	150	added stab step
TEOSR1	TEOS	300	1000	40 sccm TEOS 450 sccm O2	2.26	700	300	
GD2-1	N2O Ox	250	300	60 sccm SiH4 20 sccm N2O 110 sccm O2	1.41	700	4	
N2O15	N2O Ox	250	300	60 sccm SiH4 20 sccm N2O 110 sccm O2	1.41	700	4	
GD3	SiH4 Ox	250	300	60 sccm SiH4 120 sccm O2	1.41	700	4	
GD4	N2 Ox	250	300	60 sccm SiH4 10 sccm N2 110 sccm O2	1.41	700	4	

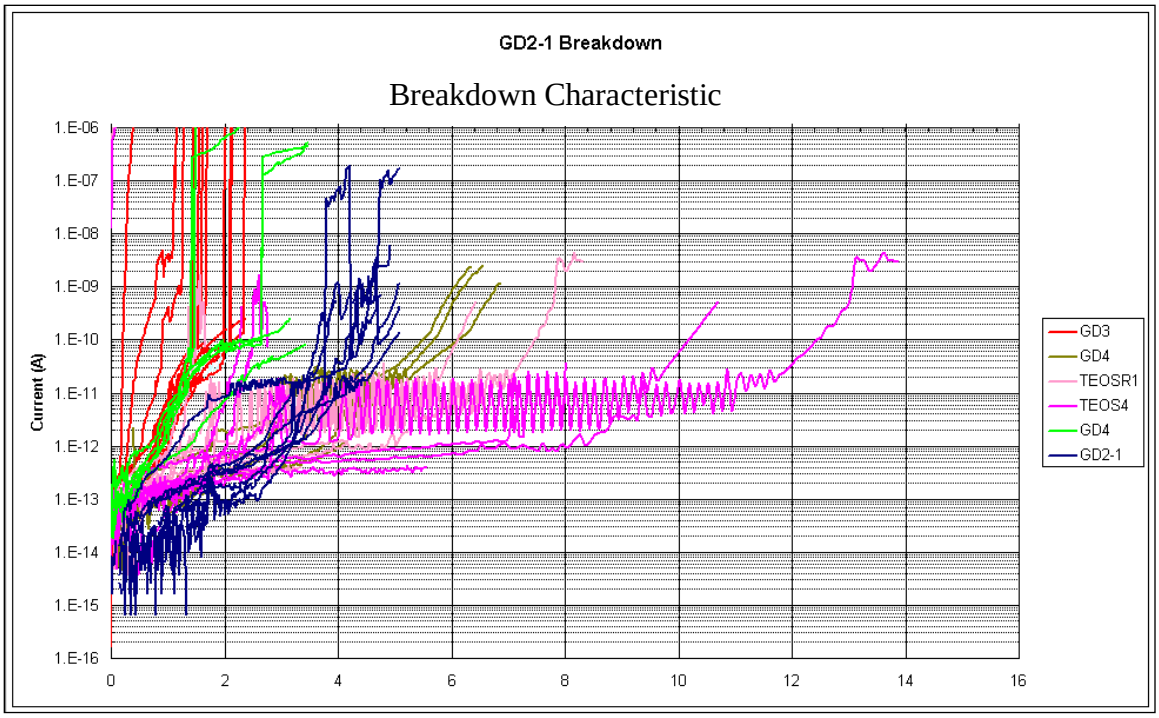

Figure 6.22: Breakdown curves for treatments identified in Table 6.3.

As can be seen from the breakdown results, the TEOS samples have a much higher breakdown (5-10 MV/cm) than the SiH_4 based samples (0.7 - 5 MV/cm). This can be explained by the SiH_4 incorporating more Si in the oxide film than the TEOS

precursor or a homogenous reaction taking place in the gas phase, creating localized defect sites.

In continuing the two-terminal investigation, another experiment was designed using molybdenum as the metal gate. These devices are referred to as "integrated capacitors", because they are compatible with a self-aligned metal gate transistor process (discussed in Chapter 8). Table 6.4 shows the different recipes that were used in the integrated capacitor process. Figure 6.23 shows the C-V curve for the control wafer C2, which had an LPCVD LTO oxide.

Table 6.4: PECVD gate dielectric recipes that were used in an integrated capacitor process. D1, D2, D3 and D4 were processed along with a control wafer (C2) that received silane/oxygen LPCVD oxide.

	D1:	D2:	D3:	D4:	
Recipe	High O_2 /TEOS Ratio	Silane w/ N_2	Silane	Silane w/ N_2O	Units:
TEOS	40	-	-	-	sccm
SiH_4	-	60	60	60	sccm
O_2	450	110	120	100	sccm
N_2	-	10	-	-	sccm
N_2O	-	-	-	20	sccm
Temperature	300	250	250	250	C
Pressure	1000	300	300	300	mTorr
Power	400	250	250	250	W
Gap	394	700	700	700	mils
Time:	300	3.5	3.2	3.5	sec

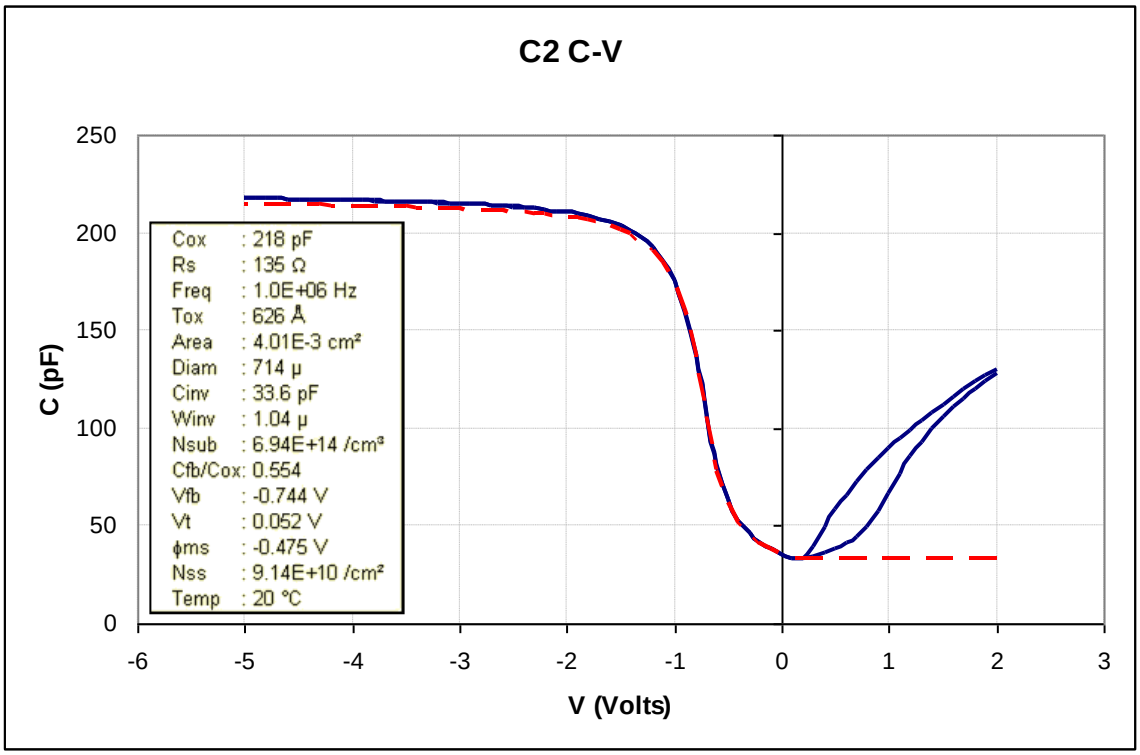

Figure 6.23: C-V curve for the control C2, which had an LTO LPCVD oxide for a gate dielectric and molybdenum for the gate metal in the NMOS process. The red dashed line shows the C-V curve that corresponds to the shown extracted parameters.

The C-V curve for C2 showed an excellent match between the theoretical fit and measured data. These results are typical for the LPCVD gate dielectric process following a sinter process, with $Q_{it} < 10^{11}cm^{-2}$. Results from sample D1 with a TEOS oxide is shown in Figure 6.24, with $Q_{it} \sim 10^{10}cm^{-2}$. This result is markedly improved over the standard ILD TEOS process shown in Figure 6.12. Sample D2 used silane and oxygen, with N_2 added, and results are shown in Figure 6.25.

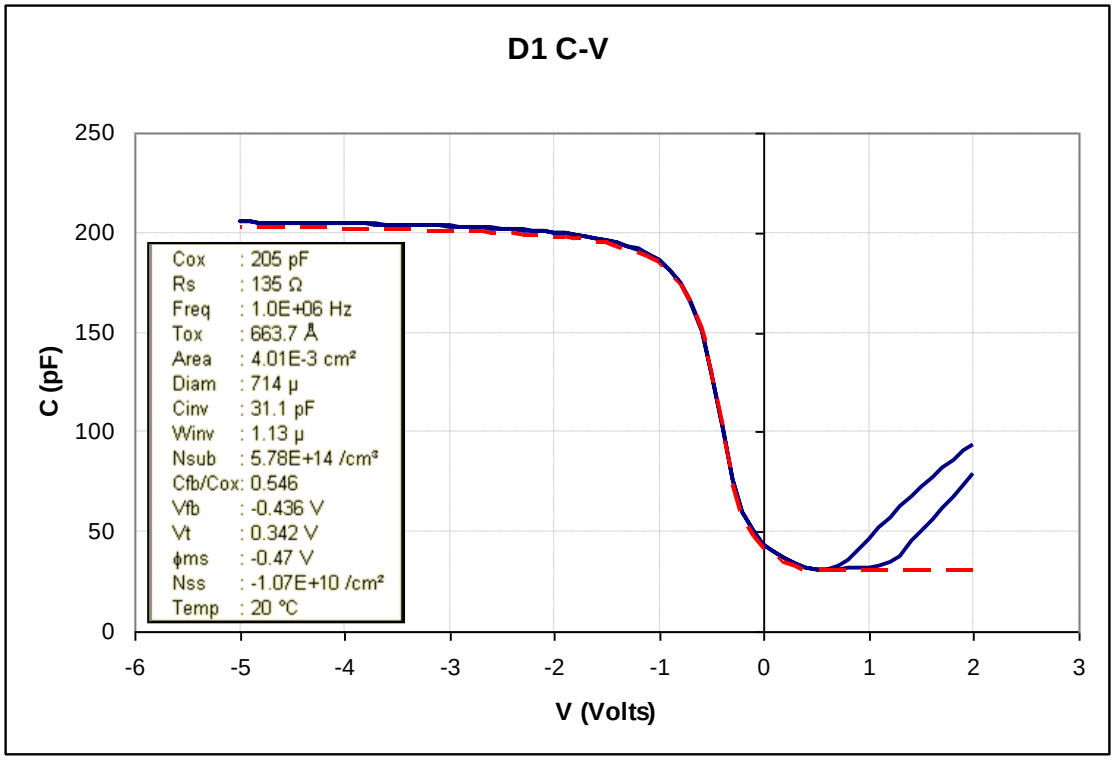

Figure 6.24: C-V curve for the device wafer D1, which had a TEOS based PECVD oxide for a gate dielectric in the NMOS process. The red dashed line shows the C-V curve that corresponds to the shown extracted parameters.

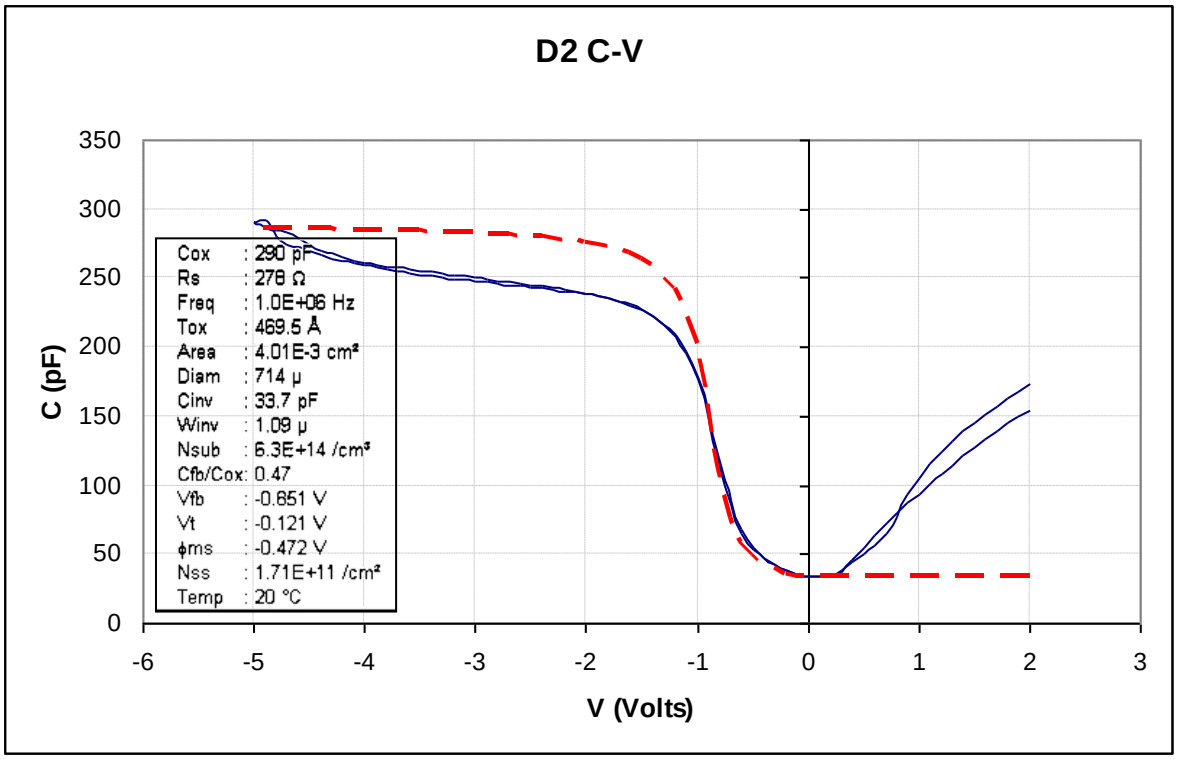

Figure 6.25: C-V curve for the device wafer D2, which had a SiH_4 based PECVD oxide with the addition of N_2 for a gate dielectric in the NMOS process. The red dashed line shows the C-V curve that corresponds to the shown extracted parameters.

While the C-V fit for D2 appears valid only in the depletion/inversion transition, the extracted oxide charge level, $Q_{it} \sim 2x10^{11}cm^{-2}$, appears reasonable. The gradual increase in capacitance in accumulation may be related to the onset of leakage, which was a problem identified using the same PECVD recipe in sample GD4 shown in Figure 6.22. Sample D3 used a PECVD silane and oxygen recipe without any additional gas species, with results shown in Figure 6.26. The theoretical fit to the data provides an excellent match, with an effective surface charge $Q_{it} \sim 10^{11}cm^{-2}$ (negative).

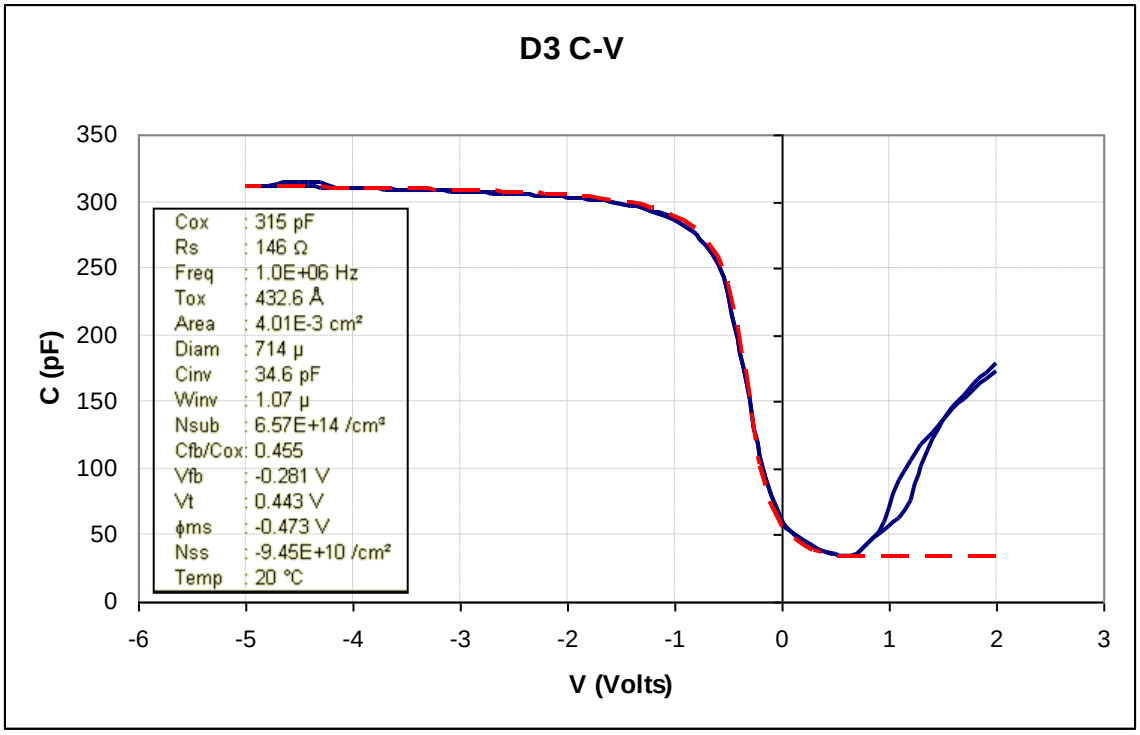

Figure 6.26: C-V curve for the device wafer D3, which had a SiH4 based PECVD oxide for a gate dielectric in the NMOS process. The red dashed line shows the C-V curve that corresponds to the shown extracted parameters.

The E-field breakdown of the oxides was also measured after the NMOS process. Figure 6.27 shows the breakdown results of D1- D3. Sample D1 (TEOS based oxide) shows a higher breakdown than the control (C2), while the SiH_4 based oxides show a lower breakdown than the control.

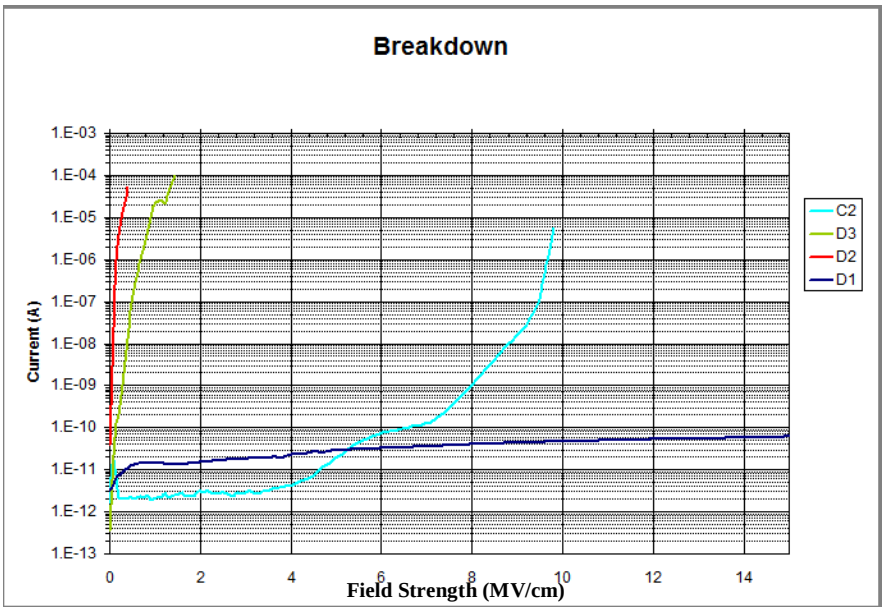

Figure 6.27: Breakdown of D1-D3 and C2, with D1 showing a less leakage and higher breakdown strength than the SiH_4 oxide.

While the C-V results on sample L7-19 shown in Figure 6.17 demonstrated that the silane and oxygen PECVD recipe with N_2O added was a promising candidate. Unfortunately wafer D4 did not yield working transistors or capacitors. There was what seemed to be a roughening of the substrate after the deposition of the gate dielectric, which resulted in adhesion problems of the gate metal, molybdenum. This treatment combination for integrated devices requires further investigation.

Chapter 7

Three-terminal nMOS Transistors

7.1. NFET Process Flow

The NFETs that were fabricated utilized gate isolation, where the gate surrounds the drain. This eliminated the needs for field isolation, but yields only individual devices and is not applicable for circuit design, which was acceptable for the purposes of this project. The gate isolated transistors were designed and along with integrated capacitors and a test reticle was created, which was used for the transistor fabrication along with the integrated capacitor fabrication. The specific NFET process used for this investigation is now presented. The NFET process flow starts with p-type (100) silicon wafers with 13-15 Ω-cm. The wafers were scribed and a piranha clean H_2SO_4:H_2O_2 (50:1) followed by dilute HF (50:1) etch, HPM clean HCl:H_2O_2:H_2O (1:1:5), followed by another dilute HF etch. Figure 7.1 shows the starting substrate.

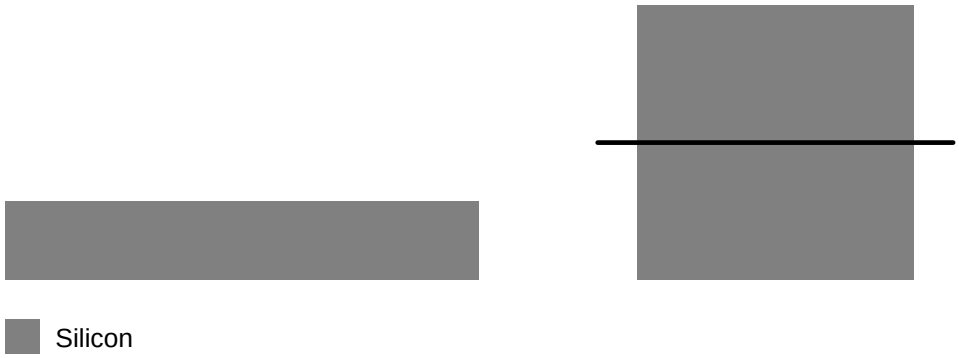

Figure 7.1: Starting (100) p-type silicon substrate.

The next step was the gate dielectric deposition step. This was carried out in an Applied Materials P5000 PECVD chamber using a 13.56MHz RF power supply. The depositions used varying power, pressure, gap between the susceptor and gas shower head, temperature, gas flows and gas composition. The target thickness was 50 nm. Figure 7.2 shows the cross-section of the NFET after gate oxide deposition.

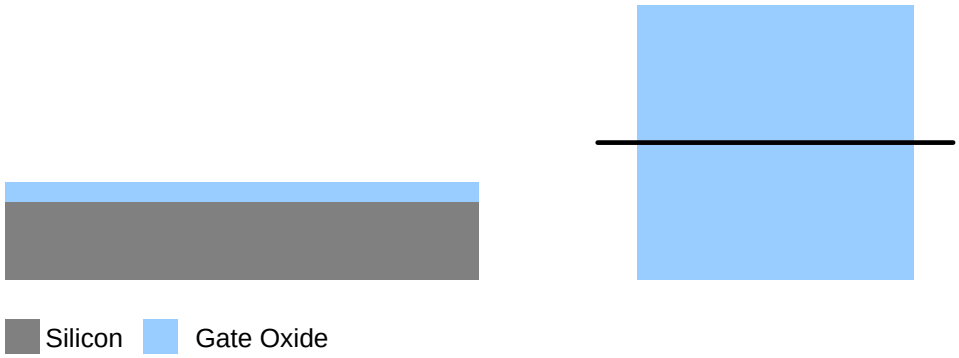

Figure 7.2: Cross-section and top down view after gate oxide deposition.

Next the molybdenum gate metal was deposited via sputtering in a CVC 601 DC sputter system. After a sufficiently low base pressure was reached the chamber was filled

with argon and the pressure was regulated at 2.7 mTorr and a DC power of 9.688 W/cm^2 was used. A 5 min sputter was done with the shutter closed to remove target surface contaminates and oxidation from the molybdenum target. A sputter time of 24.5 min was used to obtain a thickness of 5000 Å. Figure 7.3 shows the cross section and top-down view of the NFET after gate metal deposition.

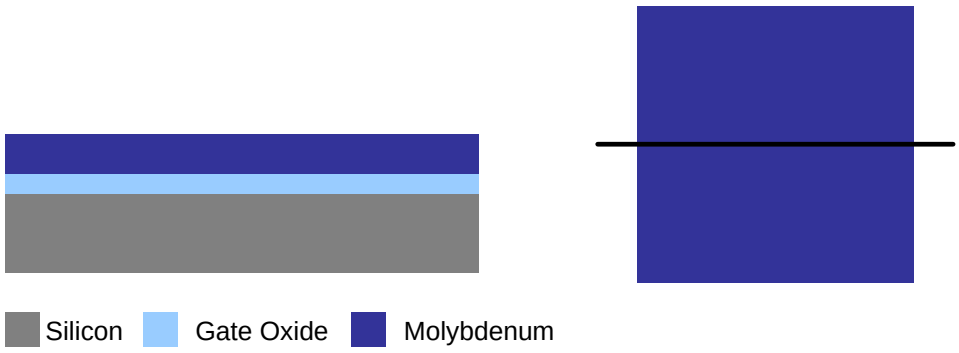

Figure 7.3: Cross section and top down view of the NFET after molybdenum gate metal deposition.

The next process was gate metal lithography. All lithography steps were completed using a GCA G-line stepper. Figure 7.4 shows the resist pattern for the gate structure of the NFET.

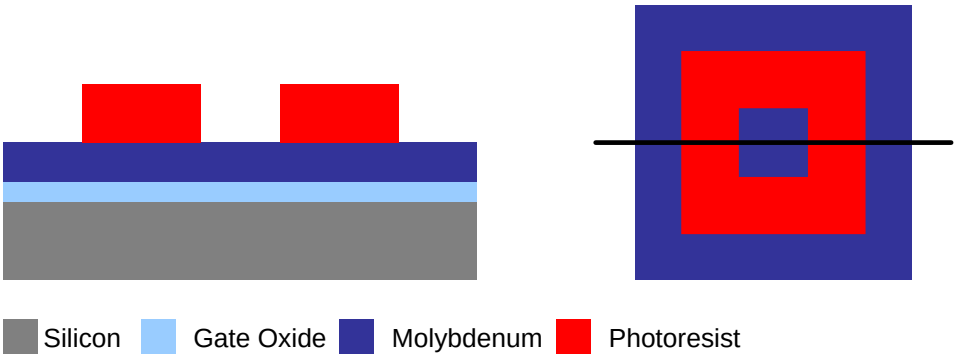

Figure 7.4: Cross-section of the patterned resist for the gate layer and top down view.

The molybdenum was then dry etched using a DRYTEK Quad etching system with 125 mTorr, 125 sccm SF_6, and 180 W process parameters. The resist was removed using a 90 ˚C PRS2000 solvent strip**.** Figure 7.5 shows the cross-section of the NFET after the completion of the metal etch.

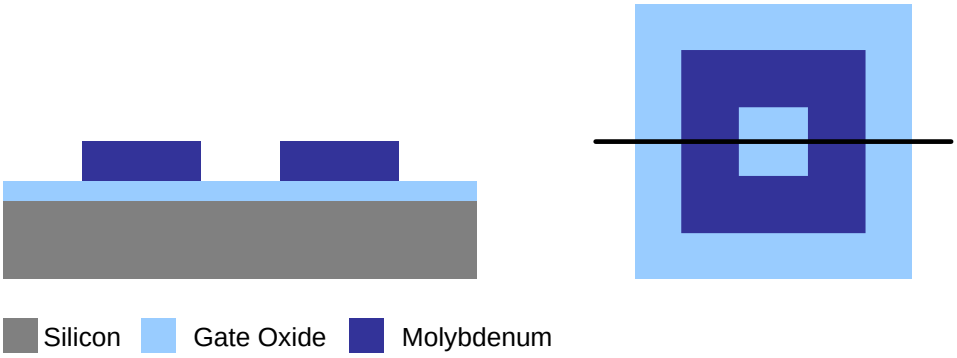

Figure 7.5: Cross-section of the NFET transistor after gate metal etch.

A 600Å LTO screening oxide was then deposited using an LPCVD system. The process parameters are as follows: 425 ˚C, 180sccm O_2, 100 sccm SiH_4, and 300 mTorr

with a 5 min deposition time. The source and drain implants are then completed with mass analyzed P^{31} at 110 keV for a dose of $4x10^{15}$ cm^{-2}. Figure 7.6 shows the cross-section of the NFET after the S/D implants were completed.

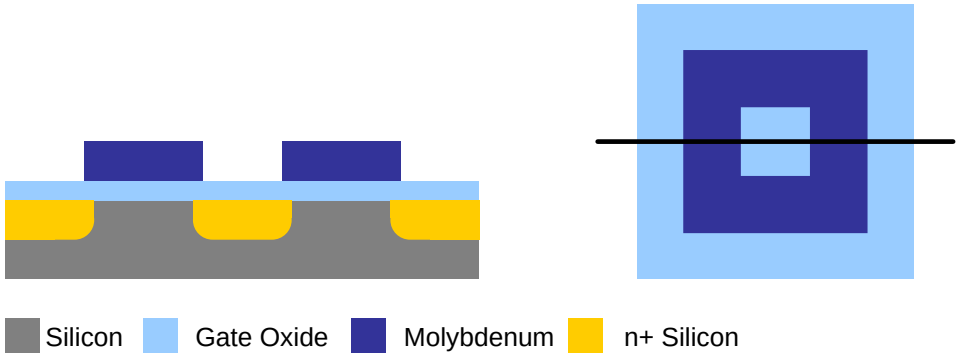

Figure 7.6: Cross-section of the NFET transistor after S/D implants.

A 4000 Å inter-level-dielectric (ILD) was then deposited using the same parameters as the screen oxide with a 33 min deposition time. This is followed by an atmospheric anneal in N_2 at 600 ˚C for 2 hours. Figure 7.7 shows the cross section of the NFET transistor after the ILD has been deposited.

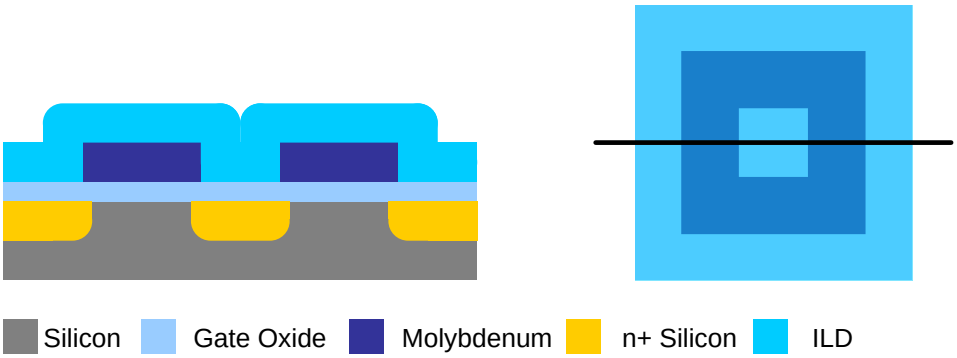

Figure 7.7: Cross-section of the NFET transistor after the ILD has been deposited.

Contact lithography was then completed followed by a wet buffered oxide etch (10:1) for 10 min for the contact openings. Figure 7.8 shows the cross-section of the NFET transistor after contact lithography and Figure 7.9 shows the cross-section after contact cut etch.

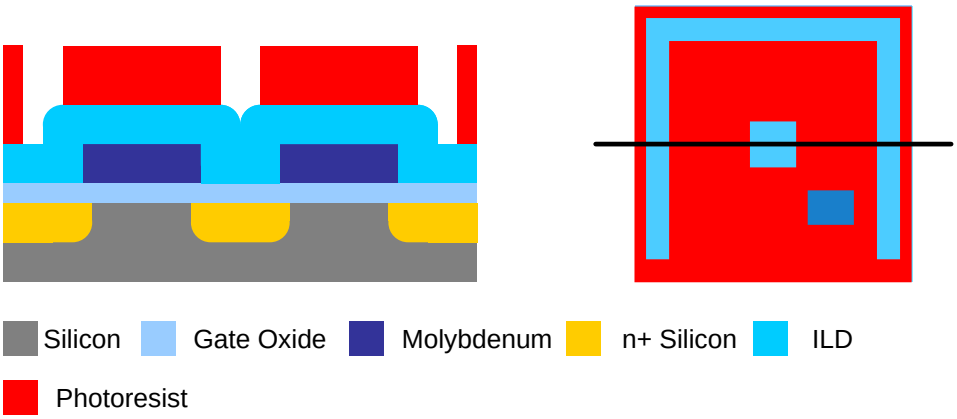

Figure 7.8: Cross-section of the NFET transistor after contact lithography.

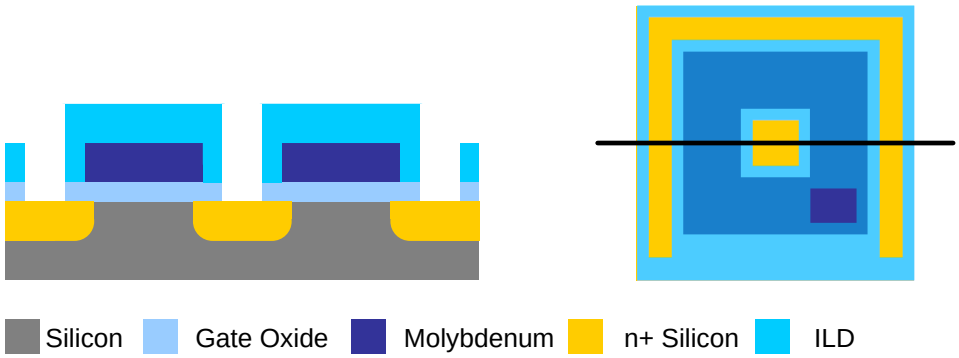

Figure 7.9: Cross-section of the NFET transistor after contact cut etch.

7500 Å aluminum was deposited in a CVC 601 DC sputter system with process parameter as follows: 5 min sputter with shields closed, 23 min sputter, 20 sccm Ar flow, 5 mTorr, 19.376 W/cm^2. Figure 7.9 shows the cross section of the NFET transistor after aluminum deposition.

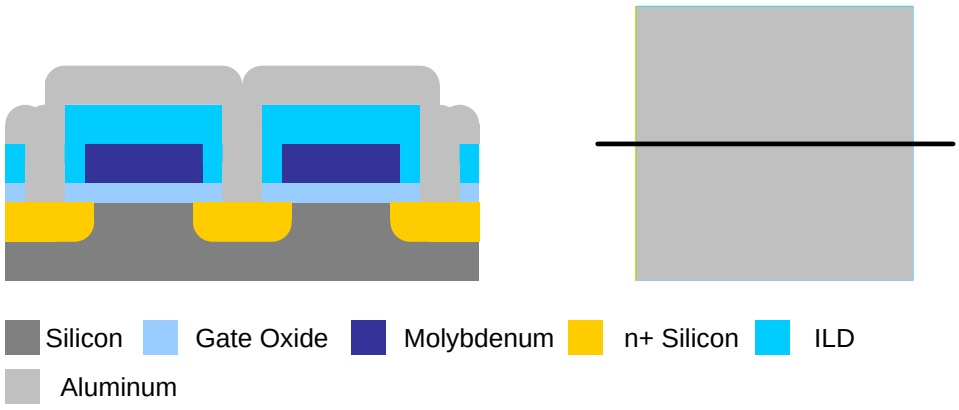

Figure 7.10: Cross-section of the NFET after aluminum deposition

The aluminum was then patterned, and etched in a wet acid bath of commercial aluminum etch by Transcene at 40˚C for 3 min. The resist was then removed with a

solvent strip at 90 ˚C in PRS 2000 for 10 min. Backside metal was deposited in the CVC 601 to ensure an ohmic contact to the substrate. The NEFT is then annealed in forming gas (N_2/H_2 5%) for 30 min at 425 ˚C this is to create ohmic contacts between Al and n^+ Si and passivate any interface traps with H_2. Figure 7.11 shows the NFET transistor after metal lithography and Figure 7.12 shows the cross-section after metal etch and resist strip. After completion of the sinter the transistors were ready for electrical characterization.

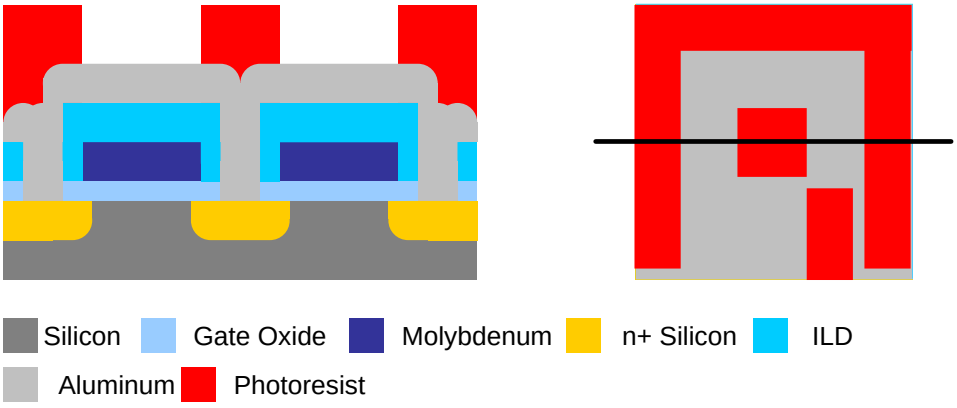

Figure 7.11: Cross-section of the NFET transistor after metal lithography.

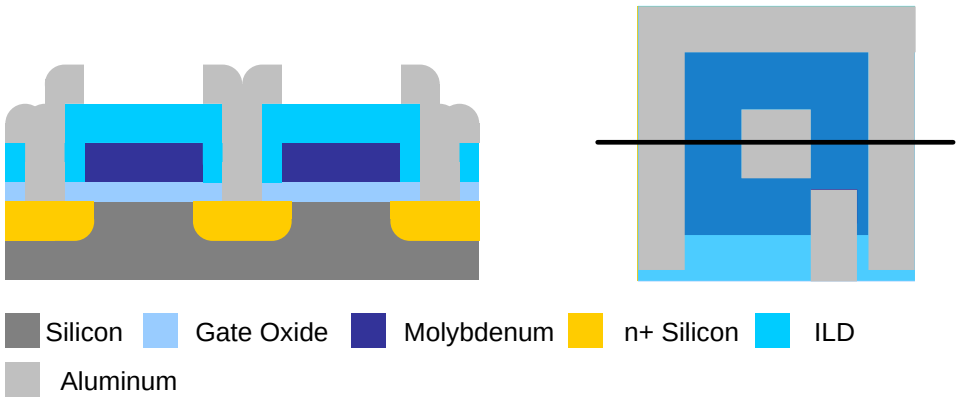

Figure 7.12: Cross-section of the NFET transistor after metal etch.

7.2. NFET Process Results and Electrical Characteristics

NMOS transistors were fabricated on p-type silicon substrates using the four different gate dielectric treatments for integrated device structures described in Table 6.4, along with a control wafer using the standard LPCVD gate dielectric. One of the treatments did not yield working transistors (D4) and therefore no results will be shown. Figure 7.13 shows an optical picture of a complete NMOS transistor.

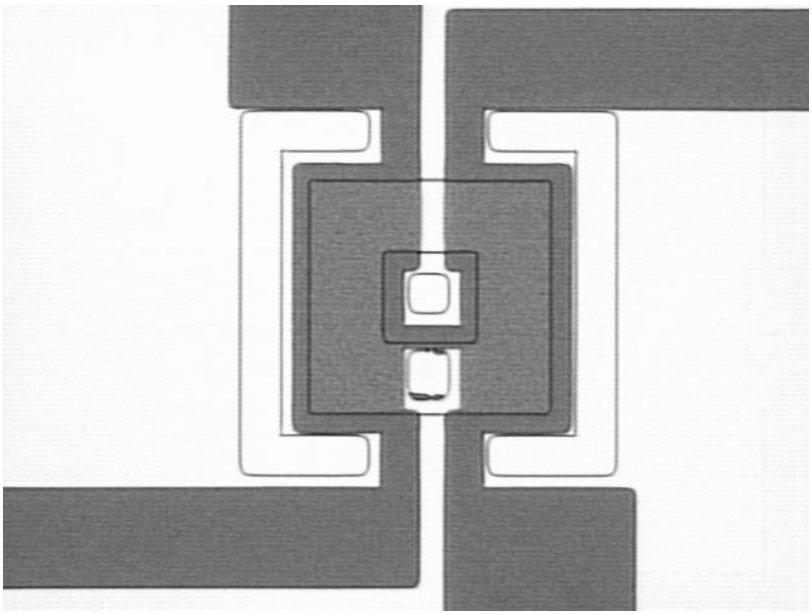

Figure 7.13: Optical picture at 50x showing a completed NMOS transistor with L=16 μm and W~160 μm.

The current voltage relationships were measured in both saturation (V_D=5 V) and linear (V_D=0.1 V) regions. The subthreshold swing *(SS)* and threshold voltage were extracted over the entire 4" wafer. Table 2.1 shows the extracted parameters of subthreshold swing and threshold voltage.

Table 7.1: Average subthreshold swing and threshold voltage values over 111 measured devices for each treatment combination.

Wafer	C2	D1	D2	D3
SS (mV/dec)	163	191	153	127
V_T (Volts)	0.382	0.563	0.513	0.938
V_T stdev (Volts)	0.313	0.121	0.321	0.048

Treatment D3 demonstrated superior results for *SS* and threshold uniformity compared to the control C2 and the other treatments. Figure 7.14 through Figure 7.17 show representative I_D-V_G curves for the different treatment combinations.

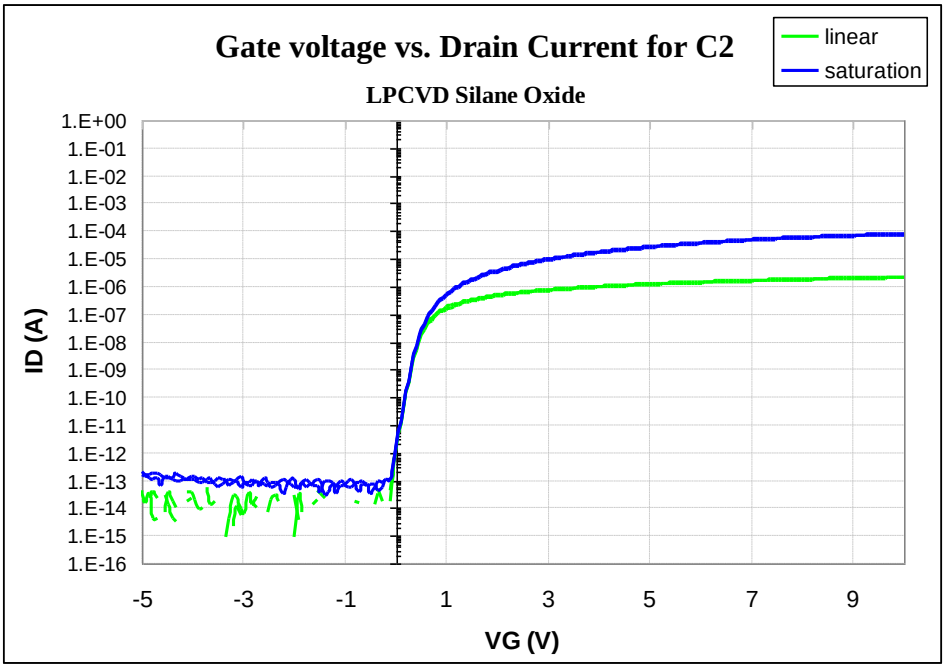

Figure 7.14: The current voltage relationship of representative C2 transistors in both saturation (VD= 5 V) and linear (VD= 0.1 V).

The results show that sample D3 had a very low V_T standard deviation (0.048 V), but does show some negative charge, which is causing a ~1 V threshold voltage, where the ideal V_T (N_{SS} = 0) is ~0.5 V based on the substrate doping. This tells us that the charge levels in the sample D3 are uniform over the wafer and the dielectric physical thickness is also uniform. Sample D1 also showed uniform V_T with a standard deviation

of 0.121 V, which was superior to the control C2, which had an unusually high V_T standard deviation (0.313 V), in part due to thickness variation.

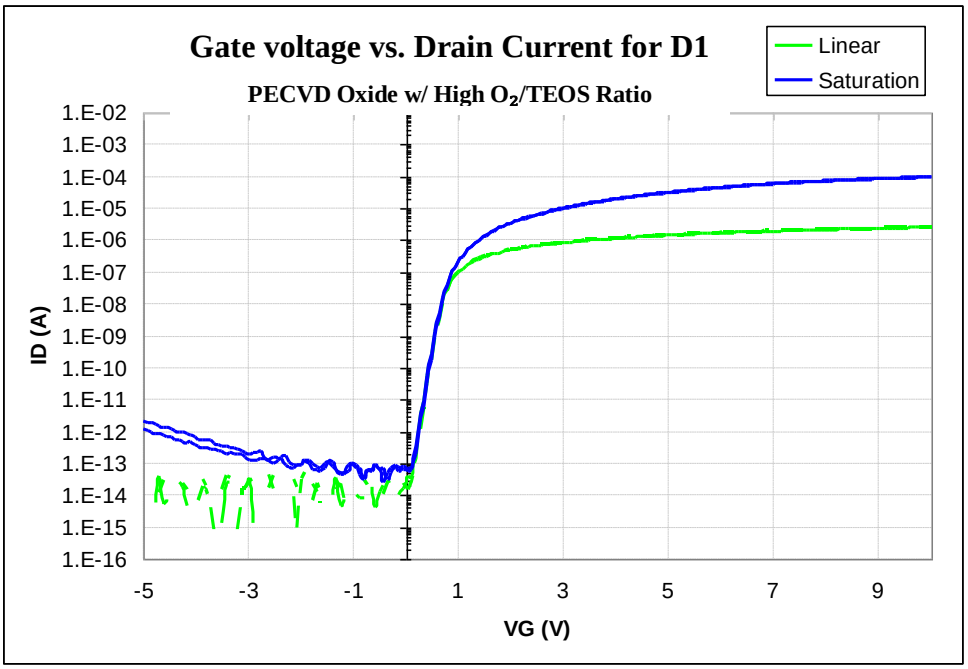

Figure 7.15: The current voltage relationship of representative D1 transistors in both saturation (VD= 5 V) and linear (VD= 0.1 V).

The samples D1 and D2 showed a V_T close to ideal (~0.5 V), which indicates a low charge level that is consistent with capacitor results. The control C2 showed a slightly lower V_T (0.382 V) compared to ideal, indicating a positive charge that is also consistent with capacitor results. All samples did not show any signs of oxide breakdown in the voltage range for the I_D-V_G measurements that were seen in the two terminal measurements in Figure 6.22. This can be due to the area difference between the

capacitors (0.004 cm^{-2}) and transistors ($2.82x10^{-5}$ cm^{-2}), increasing the chance of a defect in the oxide reducing the breakdown strength.

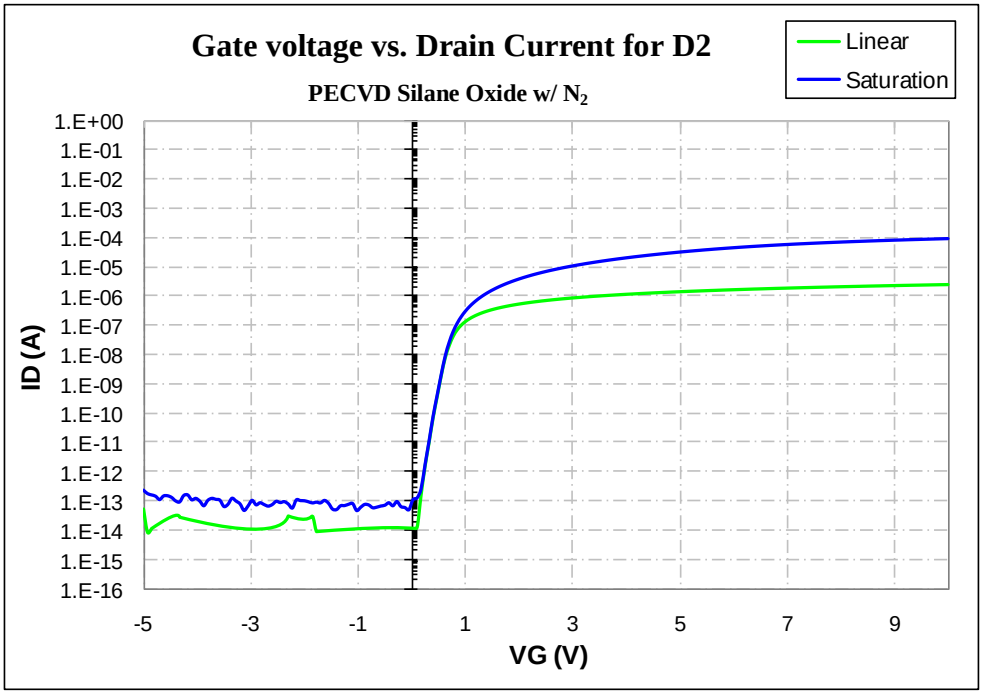

Figure 7.16: The current voltage relationship of a representative D2 transistor in both saturation (VD= 5 V) and linear (VD= 0.1 V).

The subthreshold swing was the best on sample D3 (127 mV/Dec), which was lower than the control C2 that had a *SS* of 162 mV/Dec. The subthreshold swing on the other samples was also quite low, indicating minimal surface damage during the plasma deposition process of the gate dielectric.

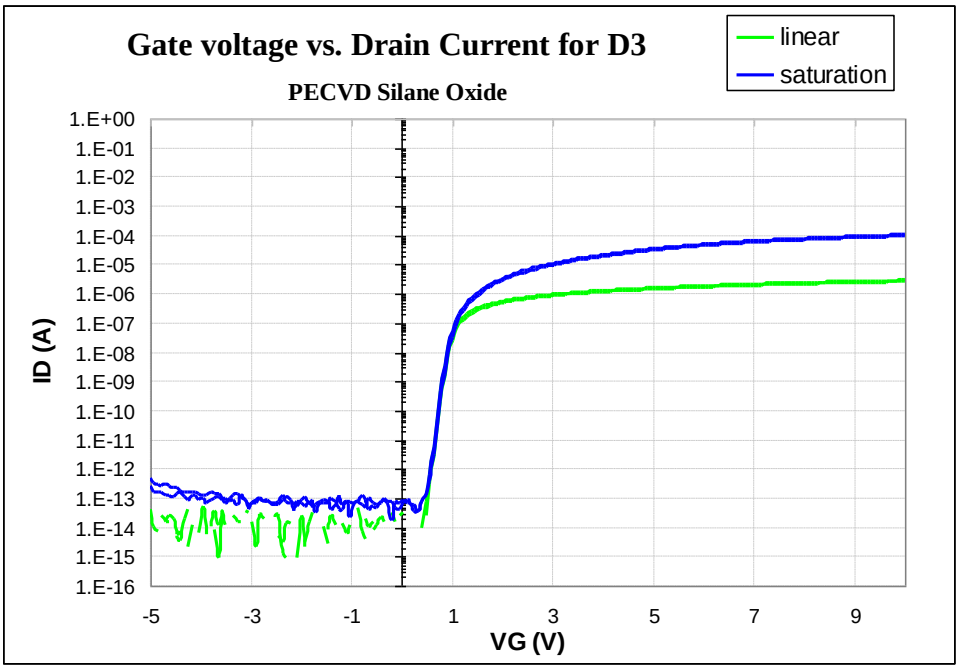

Figure 7.17: The current voltage relationship of D3 in both saturation (VD= 5 V) and linear (VD= 0.1 V).

The TEOS oxide recipe used for D1 is a definite candidate for a PECVD gate dielectric for TFTs, with performance that is comparable to the control process. Both of the silane-based PECVD recipes used on D2 and D3 demonstrated comparable results; however D3 showed excellent V_T uniformity and the steepest subthreshold characteristic. While gate induced drain leakage (GIDL) was not a parameter of primary interest for this study, it can be seen that D1 exhibits a higher level of GIDL in the over-driven off-state than the other treatment combinations. While the PECVD recipe that introduced N_2O in the ambient looked very promising initially (see Figure 6.16), sample D4 did not yield transistors due to molybdenum delamitation for reasons not known.

Chapter 8

Optical and Physical Characterization

8.1. VASE Measurements

The four samples that are seen in Table 6.4 were analyzed using the VASE technique described in Chapter 4. By fitting a Cauchy model as seen in equation (6.1), to the measured polarization parameters, the refractive index was extracted from each of the four samples.

$$n(\lambda) = A + B/\lambda^2 + C/\lambda^4$$
$$k = 0 \qquad \textbf{(6.1)}$$

A representative fit is shown in Figure 8.1**.**

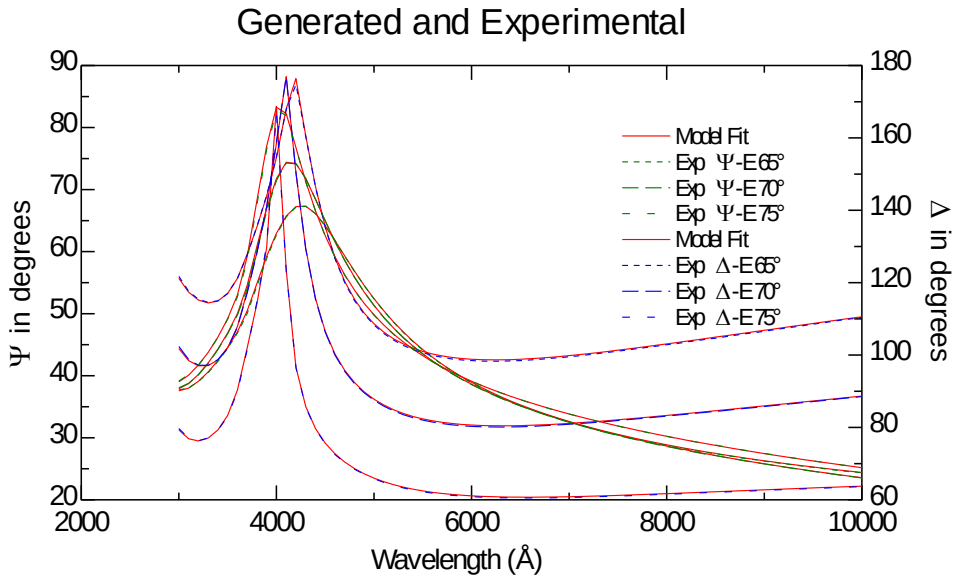

Figure 8.1: Representative fit of Ψ and Δ using a Cauchy model.

Figure 8.2 shows the index of refraction of the modified TEOS recipe along with a thermal oxide index and the standard TEOS recipe. As can be seen the modified TEOS recipe has a higher index of refraction than both the standard TEOS recipe and the thermal oxide. This may be due to formation of a non-stoichiometric oxide (silicon rich), where the oxygen to silicon atomic ratio is less than two.

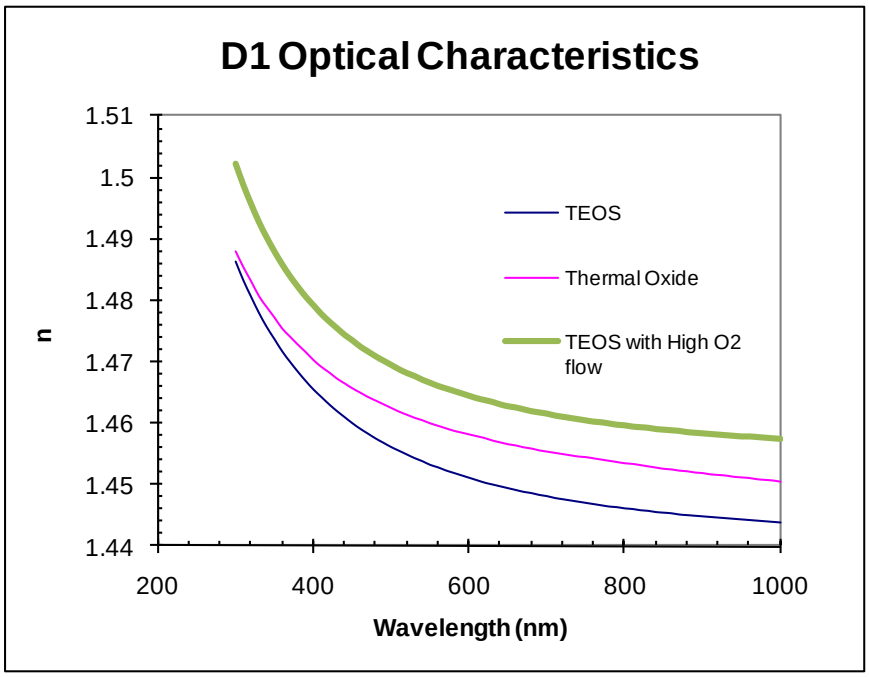

Figure 8.2: Index of refraction of the modified TEOS dielectric, D1, as well as a thermal oxide and the standard TEOS recipe.

Figure 8.3 shows the index of refraction for the sample D2 along with thermal oxide and the standard TEOS oxide for reference. The index is slightly lower than thermal oxide, which can be explained by voiding. The given change in index corresponds to 1.4% voids in the oxide using the Bruggeman effective medium approximation [13].

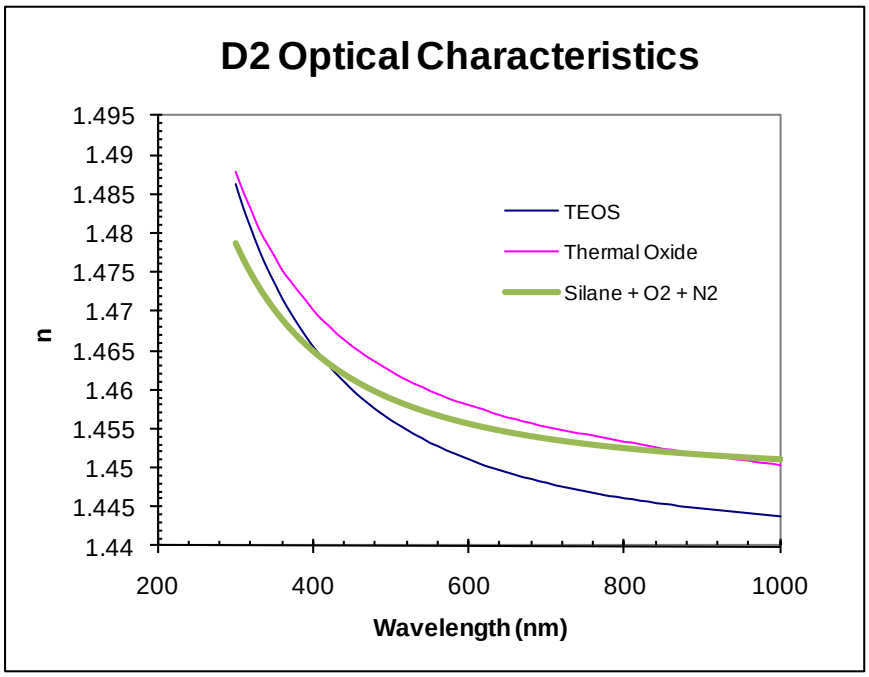

Figure 8.3: Index of refraction of the dielectric formed by the silane, oxygen, and nitrogen reaction.

Figure 8.4 shows the index of refraction of the dielectric formed by the silane and oxygen reaction before and after the tool modification explained in earlier chapters. Both indexes are lower than thermal oxide, which can be explained by voids in the silicon dioxide. The percent of voids before the tool modification was found to be 0.94 % and after tool modification the percent of voids was found to be 6.22 %.

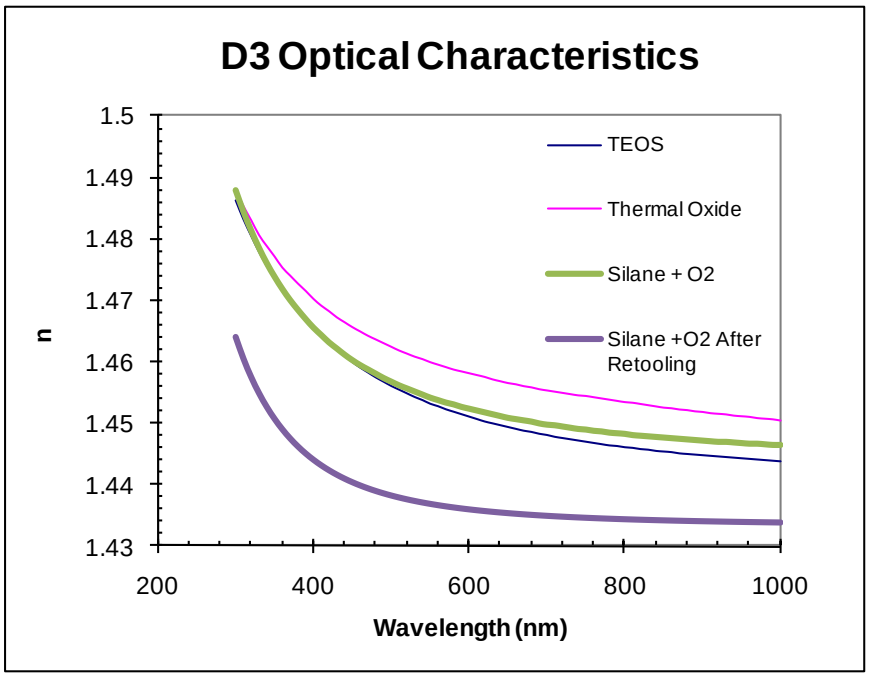

Figure 8.4: Index of refraction for dielectric formed by the silane and oxygen reaction.

Figure 8.5 shows the index of refraction for the dielectric that was formed by the reaction of silane, nitrous oxide, and oxygen. The index is higher than thermal oxide, which might indicate that the oxide is silicon rich, or that there is some nitrogen incorporation in the oxide.

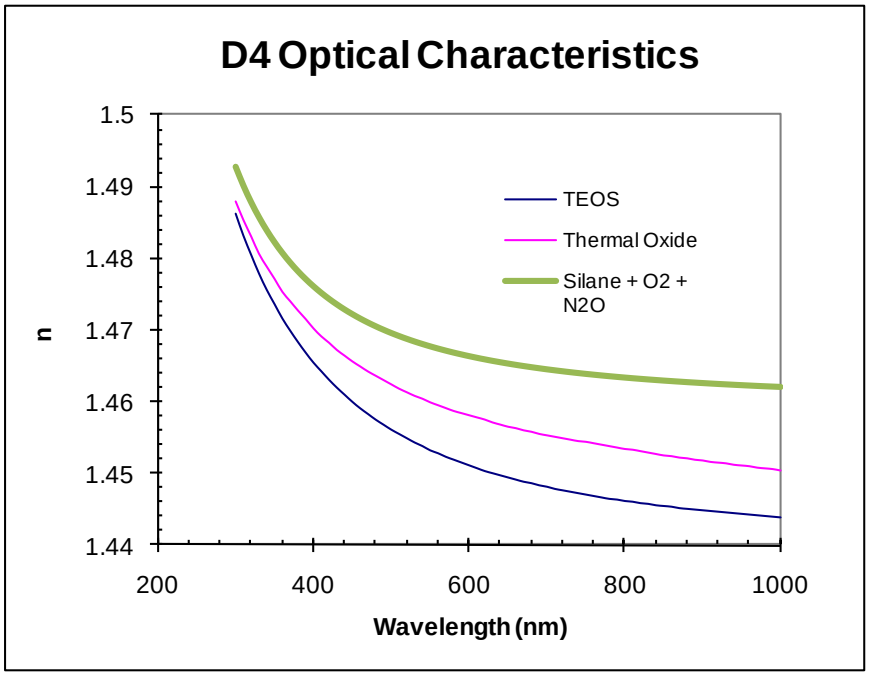

Figure 8.5: Index of refraction for the dielectric formed by the reaction of silane, oxygen and nitrous oxide.

Figure 8.6 shows the index of refraction for various dielectrics deposited with different amounts of nitrous oxide and oxygen flow in a silane PECVD reaction; also plotted are thermal silicon dioxide and silicon nitride. The results show that the index can be modulated from thermal oxide to almost the level of silicon nitride by having only nitrous oxide and no oxygen in the silane reaction. This is more likely due to the oxide being silicon rich, and not due to nitrogen incorporation [20].

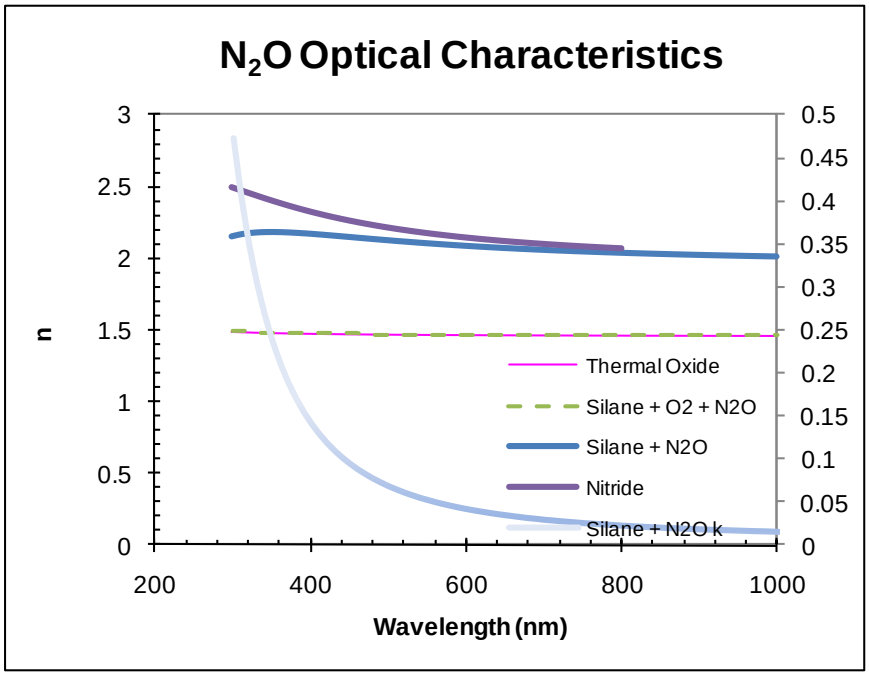

Figure 8.6: The index of refraction of various dielectric deposited with varying amounts of nitrous oxide and oxygen. Also plotted is thermal oxide and silicon nitride.

8.2. Stress Relaxation Measurements

Stress relaxation measurements were also performed on the four dielectrics that were used in transistor fabrication. The results are well correlated, with the lower index values showing a higher change in stress over time in room ambient (25 ˚C and 45% relative humidity), with all films demonstrating a compressive shift in stress. Voids in the oxide, which can change the refractive index, may also promote water absorption. Figure 8.7 shows the stress relaxation data for the modified TEOS sample that was used as the gate dielectric for sample D1; also plotted is the standard TEOS stress relaxation results for reference. The results show a smaller change in stress than the standard TEOS dielectric, which is consistent with an oxide with fewer voids.

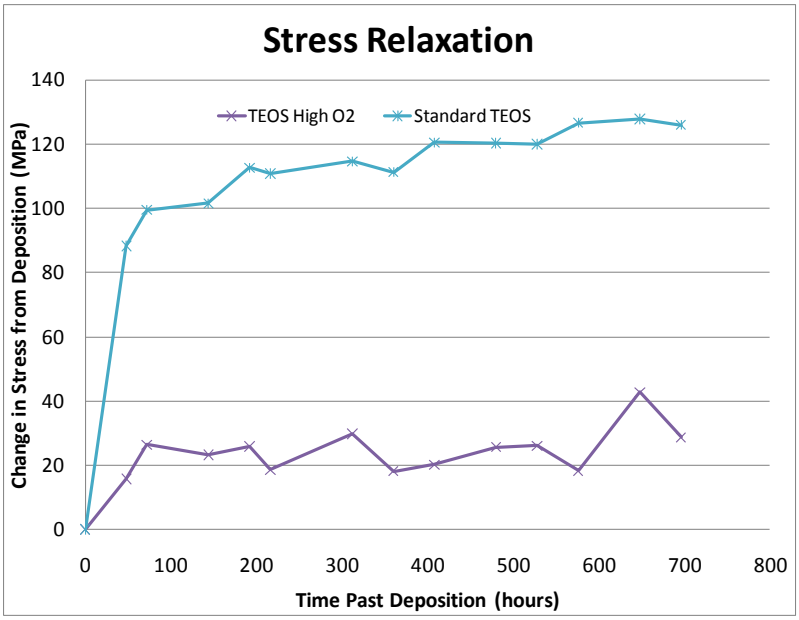

Figure 8.7: Stress relaxation (compressive shift) measurements for the dielectric that was formed by a modified TEOS sample, also used in device D1.

Figure 8.8 shows the stress relaxation data from the dielectric that was formed by a silane, oxygen, and nitrogen reaction. The results show an initial large change in stress, greater than that of the standard TEOS recipe, but then a decrease in stress.

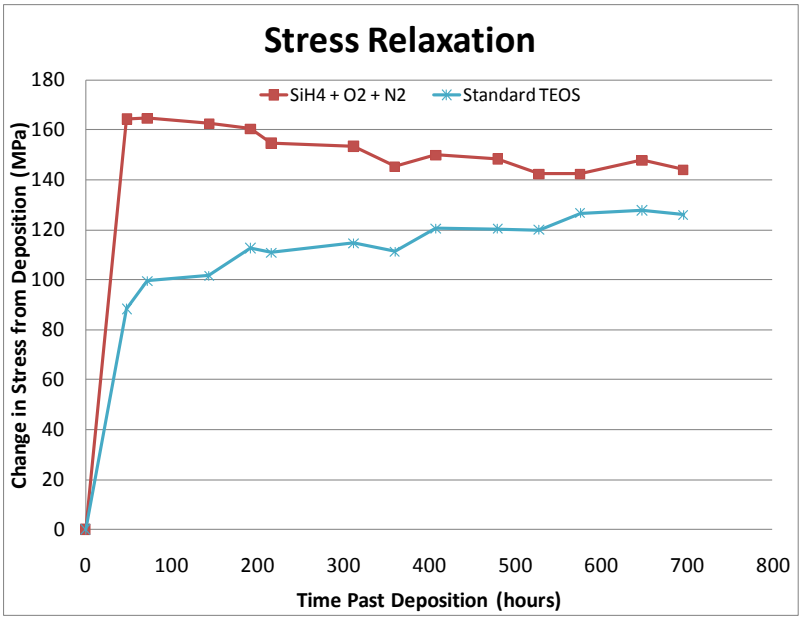

Figure 8.8: Stress relaxation (compressive shift) data for the dielectric that was formed by a silane, oxygen and nitrogen reaction, also used in wafer D2.

Figure 8.9 shows the stress relaxation data for the dielectric that was formed by the reaction of silane and oxygen. The results show a large change in stress initially, then almost no change in stress over time. This sample has the largest initial change in stress and the lowest index of refraction compared to the other samples, both indicating a porous film.

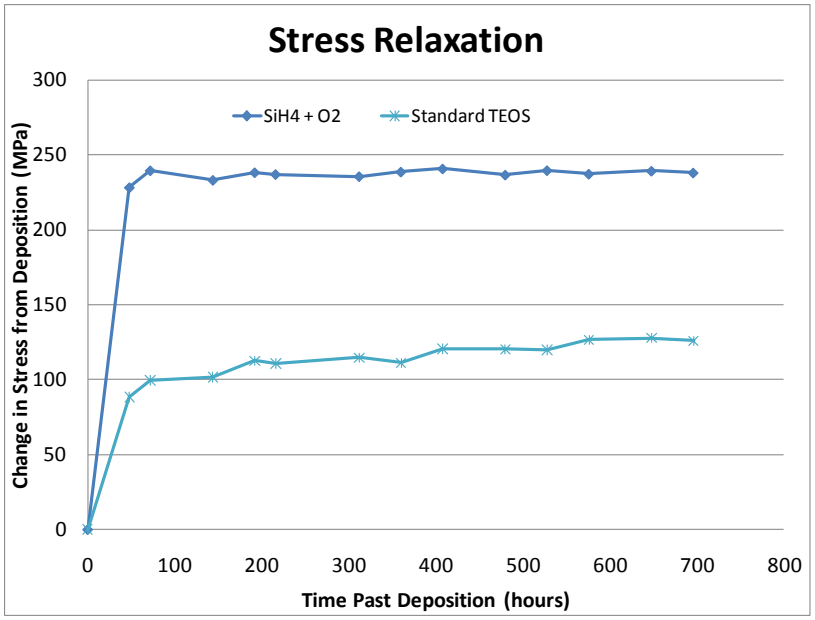

Figure 8.9: Stress relaxation (compressive shift) data from the dielectric that was formed by a reaction of silane and oxygen, used in device wafer D3.

Figure 8.10 shows the stress relaxation data for the dielectric that was formed by a reaction of silane, oxygen, and nitrous oxide. The results indicate a lower change in stress than the other silane-based dielectrics, and it also has the highest index of refraction and breakdown field strength of the three dielectrics that were formed using silane.

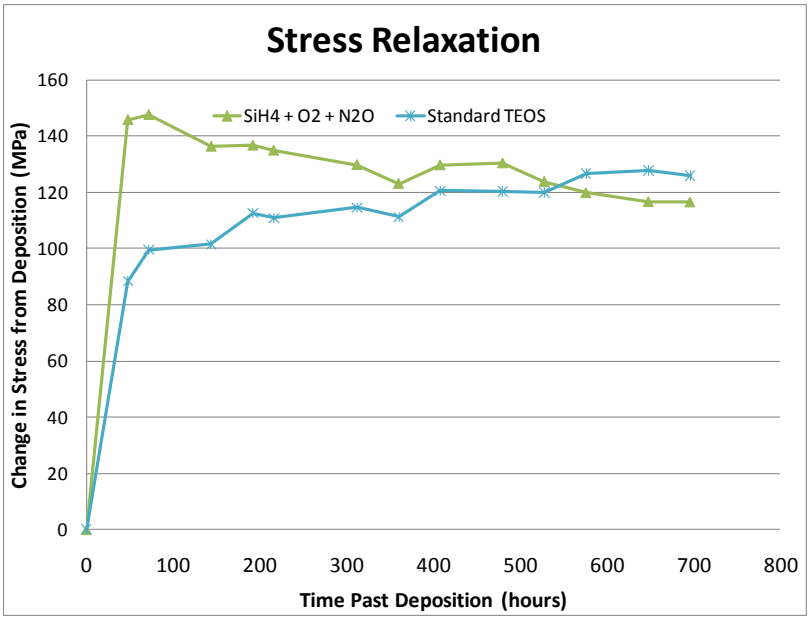

Figure 8.10: Stress relaxation (compressive shift) data from the dielectric that was formed by the reaction of silane, oxygen, and nitrous oxide, used in device wafer D4.

Figure 8.11 shows the index of refraction versus the maximum change in stress over the stress relaxation study for the silane and TEOS based dielectrics. There is a definite correlation between the index of refraction and the maximum change in stress; for lower index values there is an observed increase in the change in stress state compared to other samples. It is important to note that the silane reactions were done at the same power densities and pressures, and the TEOS samples were both done at different power densities and pressures, which will also play a role in film stress.

The TEOS-based sample that corresponds to device wafer D1 demonstrated an index close to that of SiO_2, indicating negligible void content. This sample also

demonstrated a minimal change in the stress over time, which also supports a structure closer to that of thermal SiO_2 compared to the other samples.

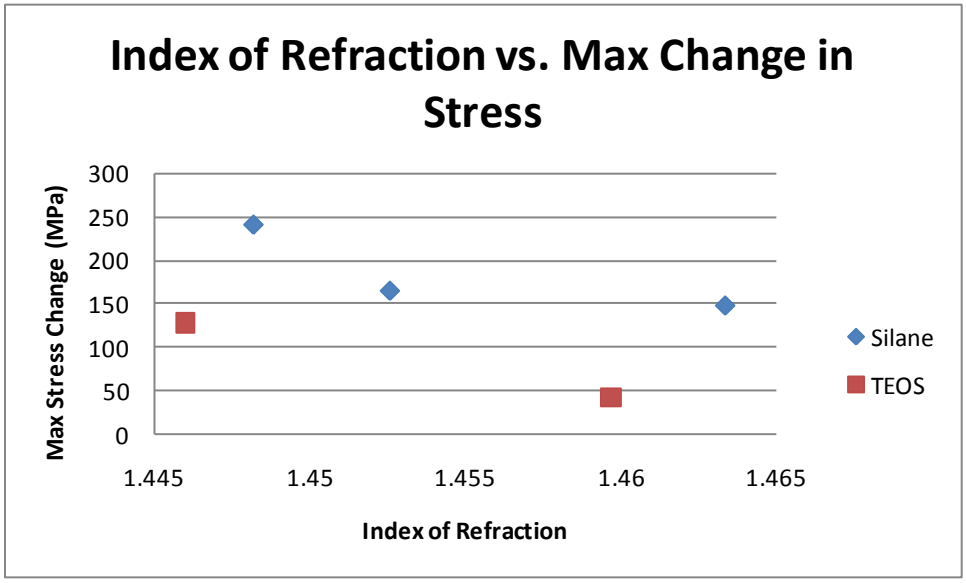

Figure 8.11: Index of refraction (@800 nm) vs. max change in stress for silane based oxides.

It was also observed that the silane samples that had a nitrogen source in the deposition reaction, either N_2 or N_2O, had an initial large shift in stress in the compressive direction, but then a steady smaller shift in the tensile direction as time progressed, seen in Figure 8.8 & Figure 8.10**.** This was not observed in any of the other samples; they would continue to shift in a compressive direction over time after an initial large shift in the compressive direction.

Chapter 9

Conclusion

In conclusion NMOS transistors were fabricated using a low temperature (T<650 ˚C) process with various gate dielectrics. The results show that using a SiH_4 based PECVD oxide can be used to create a transistor with a uniform threshold voltage and subthreshold swing comparable to that of a LPCVD SiH_4 oxide (LTO) that has previously reported [21]. While the silane-based recipes demonstrated excellent film thickness uniformity, one problem that was noticed with the PECVD SiH_4 based oxides is that on large-area devices it appears to suffer from a low breakdown strength (1-6 MV/cm). This may be caused by localized particulate contamination; transistor results did not suffer from this lower breakdown condition. It is hypothesized that using solely nitrous oxide instead with a ratio of 20 parts nitrous oxide to silane in the CVD reaction and/or adding helium to the reaction creating a slower and more complete reaction [7,20,22,23], will mitigate this low breakdown condition by avoiding gas phase homogenous nucleation that creates particulate contamination. While the addition of N_2O to the process recipe showed excellent Hg-probe C-V characteristics, molybdenum delamination issues prevented successful transistor fabrication. This treatment

combination requires further investigation, as it may demonstrate competitive performance in transistor operation.

A PECVD TEOS reaction was also shown to have comparable electric results to the LPCVD LTO process, with a higher breakdown (>10 MV/cm) than the LTO process (~7 MV/cm). The TEOS sample also showed low charge levels, ~10^{10} cm^{-2} as seen in Figure 9.1. The transistor threshold also matched well with the predicted threshold (~0.5 V) as seen in Figure 9.2, and had a small standard deviation, 0.121 V. The developed TEOS-oxide recipe would be an acceptable replacement of the established LTO process. Although the thickness uniformity is equivalent to the LTO process, minor hardware modifications should provide significant improvement.

A possible two-stage recipe combining the PECVD TEOS oxide and the PECVD SiH_4 oxide may take advantage of the best qualities of both dielectrics. Future work should repeat the experiment with the addition of a stacked gate oxide with a silane based oxide and a TEOS based oxide, as well as modifications to the silane based recipes to have increased oxygen concentrations and the addition of helium to the reaction.

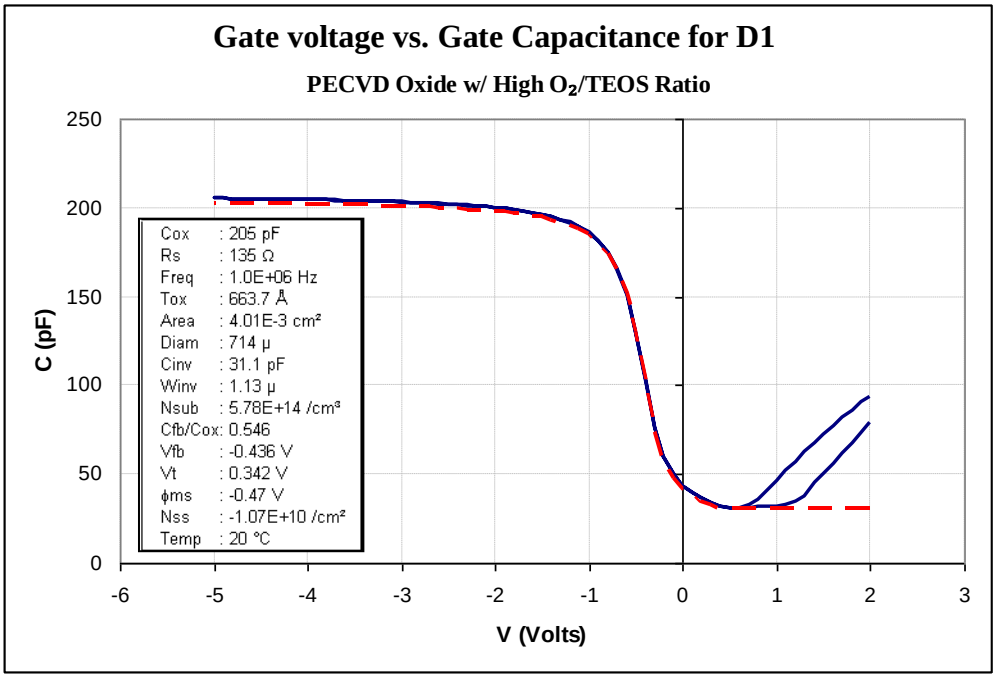

Figure 9.1: Gate voltage vs. gate capacitance for an integrated capacitor with a molybdenum gate and a PECVD TEOS oxide showing low charge levels. Repeat of Figure 6.24.

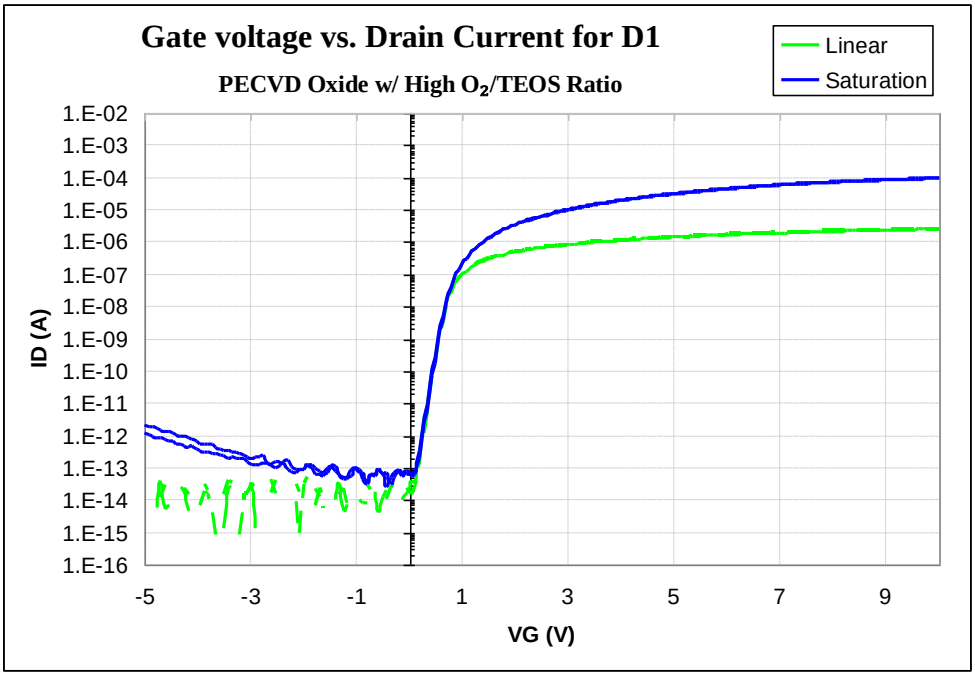

Figure 9.2: Gate voltage vs. drain current for a transistor fabricated with a molybdenum gate and PECVD TEOS gate oxide. Repeat of Figure 7.15.

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