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The Design of Fail-Safe Logic

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THE DESIGN OF FAIL-SAFE LOGIC

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ABSTRACT

This paper examines the behavior of digital logic families, specifically identifying the properties and characteristics of digital fail-safe logic. Fail-safe digital design is examined utilizing classical logic and semiconductor theory. The effects of failures internal to the structure of digital integrated circuits are analyzed and a discussion of pertinent logic design is presented. The techniques to detect all types of multiple failure modes are examined. With these results, a method of design for fail-safe logic is presented and analyzed.

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INTRODUCTION

The intent of writing a paper on fail-safe logic design is to identify and resolve the problems associated with digital circuits as they pertain to fail-safe designs. Existing fail-safe devices and systems have been found to be designed for only a single application and not adaptable for any other use, unable to resolve all potential failure designmmodes, or are hybrid in nature. The need to establish a method or approach for fail-safe logic that resolves all failure modes of logic gates and be useable in various engineering applications is pertinent to many present-day electronic systems.

HISTORICAL OVERVIEW

When, where or who invented the first fail-safe device or system is not known. It is known that where the demand for safety and safer devices or systems has prevailed, fail-safe devices have come into being. With the advent of the Industrial Revolution, systems rapidly became more complex which resulted in increasing numbers of accidents, injuries, and damage. Failure to keep pace with the increasing technological growth became increasingly evident as the occurrence of major disasters increased over the

years. Efforts finally led to adopting legislation for Mine, Industrial, Railroad, Marine, and Traffic safety.

After the turn of the century, Congress passed the Railroad Safety Appliance Act forcing the railroads to install basic safety devices; many involved fail-safe design. The railroads, who initially opposed such legislation became ardent supporters of safety measures. These early fail-safe devices were mechanical in nature but by the mid 1920's electro-mechanical systems designed around unique relays replaced the earlier mechanical devices and quickly proved themselves. This laid the foundation for fail-safe systems that exist today.

With the advent of the semi-conductor, electronic fail-safe systems came into use and have continued to develop and grow. However, the fact that electro-mechanical fail-safe devices are very much in use today, in the age of the integrated circuit, is evidence of the lack of acceptance to convert to, or rely on the electronic device for many fail-safe requirements. Today we have a level of fail-safe design that is basically applications-oriented. In the future, concepts that encompass but extend beyond the particular application, one that involves general fail-safe design techniques may be required in order to make adequate use of the integrated circuit.

SCOPE

The scope of the paper will be fail-safe logic. The

intent is to establish design techniques for the CMOS Logic Family that will enable it to function in a fail-safe mode of operation, by identifying the internal and external (logical) failure modes of digital integrated circuits and using the CMOS gate to resolve these fault conditions by implementing the techniques of complimentation and dynamic self-checking. It is intended that the use of these methods, at the individual gate level of operation, will produce a fail-safe logic gate.

The first three chapters discuss the types of circuit failures common to all families of digital integrated circuits. Chapter I identifies and analyzes the effects of internal component failures on the operation of digital integrated circuits. The effects of threshold variation on the operation of logic is discussed in Chapter II and common logic faults that affect normal logic operation are identified and explained in Chapter III. The paper then focuses on the general requirements of fail-safe logic in Chapter IV, and relates them to the basic properties and limitations of the CMOS logic gate in Chapter V, followed by the techniques that will be implemented by the CMOS logic to produce a fail-safe gate in Chapter VI. Chapter VII will then implement these methods and analyze their results on the CMOS Nand gate. A discussion as to the operation of the fail-safe gate is presented and analyzed in Chapter VIII. The results of the paper are discussed in Chapter IX and conclusions are

then brought forth which indicate the degree of success obtained.

THE CONCEPT OF FAIL-SAFE

The concept of fail-safe has precluded any standardization of a definition. This is due to the fact that the concept is inherently involved with the problems of safety and of risks using such devices or systems. There has not been any major agreement on what a fail-safe design should specifically accomplish. There appears to be some acceptance given to the definition that fail-safe is a characteristic of a device or system which ensures that any malfunction affecting safety is of sufficiently low probability such that the risk is acceptable. This definition relates failures to safety levels in so far as all failure rates should not exceed some specified limit. It implies that failures that do occur must not degrade safety and that no such limit as an absolute fail-safe level exists.

The intent of a fail-safe design is to produce minimal damage and injury in the event of a malfunction to the device or system. Hence, a fail-safe design is one which maximizes the inherent possibility that if the device or system fails, it will fail in the least unsafe condition and preferably in an entirely safe condition. This paper will interpret this definition as implying the following:

1. A circuit designed for fail-safe operation has

the property that once a fault (or faults) has caused the system to malfunction, it must automatically enter a "safe" state from which the system should never leave.

2. The circuit must be capable of acting on single and multiple failures regardless of the sequence of occurrence.

3. The circuit must be capable of detecting internal device failures as well as logical failures.

CHAPTER I

INTERNAL COMPONENT FAILURES OF INTEGRATED CIRCUITS

Internal component failures are crucial in the design of a fail-safe circuit. The fact that an internal failure may cause the output of a device to produce an erroneous signal is compounded by the parameter variations due to temperature, supply voltage, fanout, and noise. If an internal failure produces an undetectable change at the output of the device, then a failure elsewhere could render the circuit unsafe. The purpose of this chapter is to identify potential internal component failure modes and analyze these integrated circuit failures to determine their effect on the gate's operation. By considering different logic structures, the effects of circuit complexity and component selection on circuit performance can be examined.

Table 1 lists the four common integrated circuit components used in digital gates and shows their potential failure modes. The causes of component failures can range from processing and manufacturing techniques to misuse in the application of the device. Regardless of the causes of these failures, it is the effect on the operation of the digital circuit that is of significance. As an example of internal component failures, the NOR transistor circuit in

TABLE 1

TYPES OF COMPONENT FAILURE MODES

COMPONENT	TYPES OF FAILURES
Resistor	Out of tolerance increase Out of tolerance decrease Open-circuit Short-circuit
Capacitor	Open-circuit Short-circuit
Diode	Open-circuit Short-circuit Excessive leakage
Transistor	Short-circuit Open-circuit Excessive leakage Loss of beta

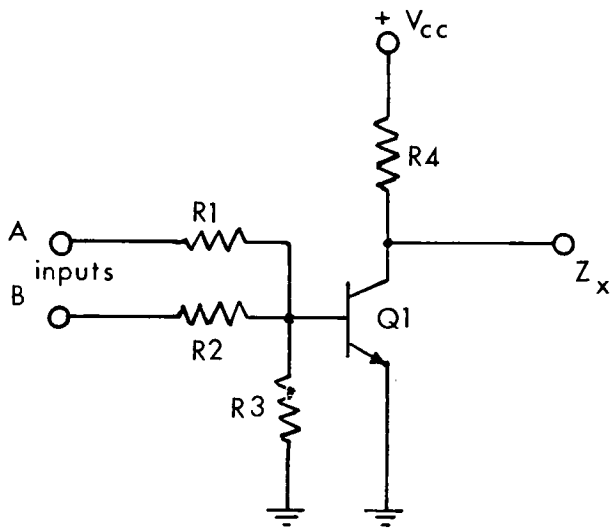
Figure 1 illustrates the defective output functions Z_1 and Z_2 caused by the open-circuit failures of R_1 and R_2 respectively.

The significance of component failures is their impact on the input and output characteristics of the digital circuit. Sample calculations showing the effect of component changes on the output of a basic transistor circuit, as evaluated in terms of the stability and sensitivity of the device, are given in Appendix A.

Analysis of the Resistor Transistor Logic, (RTL), gate in Figure 2 will be used to illustrate the effects of internal component changes on the operation of this circuit. The RTL gate in the left portion of the circuit has its output level high; i.e., the inputs are all assumed low (ground potential). The equivalent circuit loading for the left portion (Q_1 and Q_2) is illustrated in Figure 2b. The analysis for determining the sensitivity to component tolerances is given in Appendix B, with reference to Appendix A for the procedure. The obtained results of output sensitivity to component tolerances for R_B and R_L are as follows:

$$S_{R_B}^{V_o} = 1 - \frac{R_B}{R_B+3R_L} \quad \text{(Fanout = 3)} \qquad (1)$$

$$S_{R_L}^{V_o} = 1 - \frac{3R_L}{R_{B+3R_L}} \quad \text{(Fanout = 3)} \qquad (2)$$

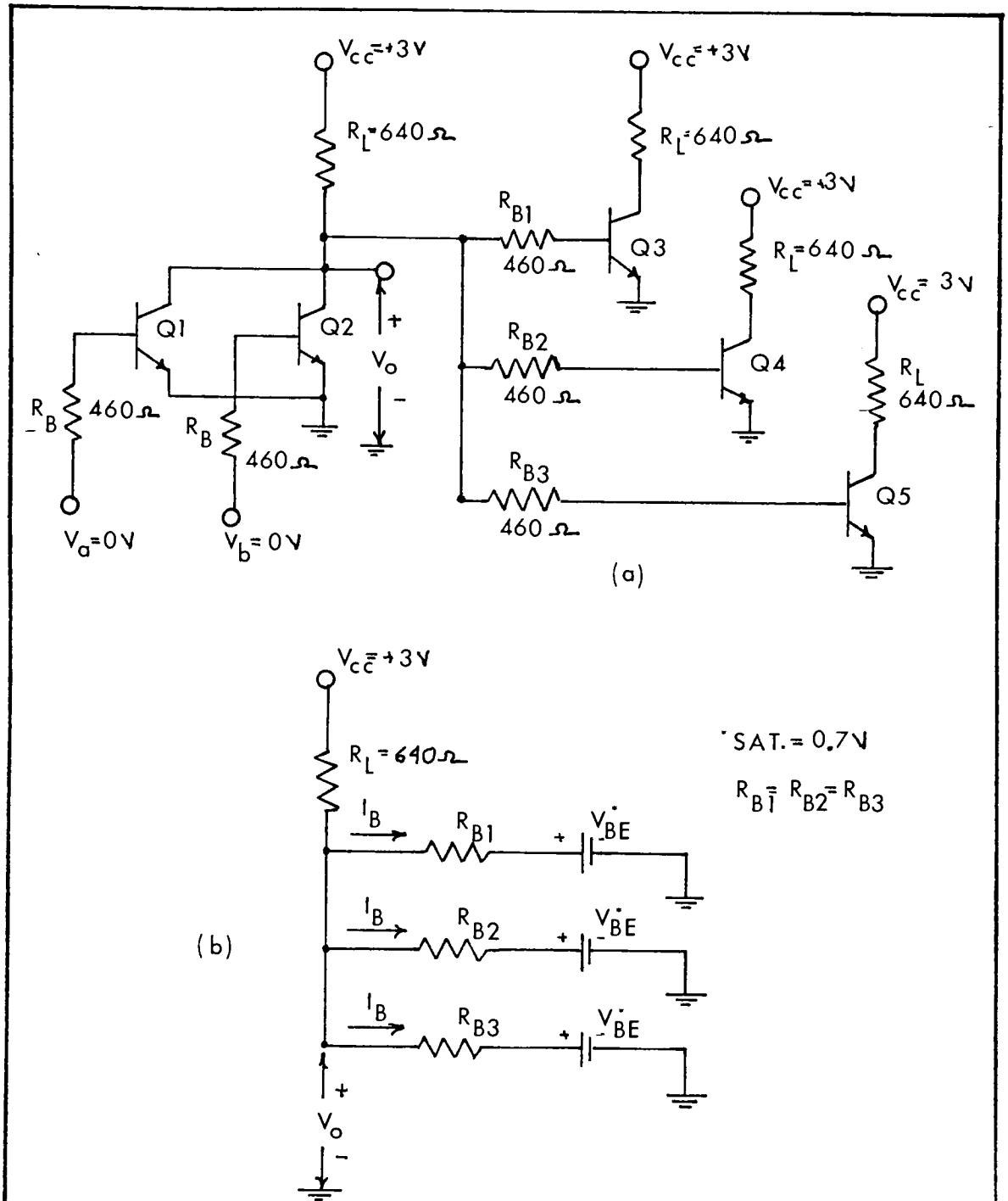


INPUTS		OUTPUTS NORMAL	DEFECTIVE	
A	B	Z_n	Z_1	Z_2
0	0	1*	1*	1*
0	1*	0	0	1*
1*	0	0	1*	0
1*	1*	0	0	0

*DENOTES + SIGNAL

NOR Transistor Circuit & Truth Table with Internal Componet Failures.

FIGURE 1



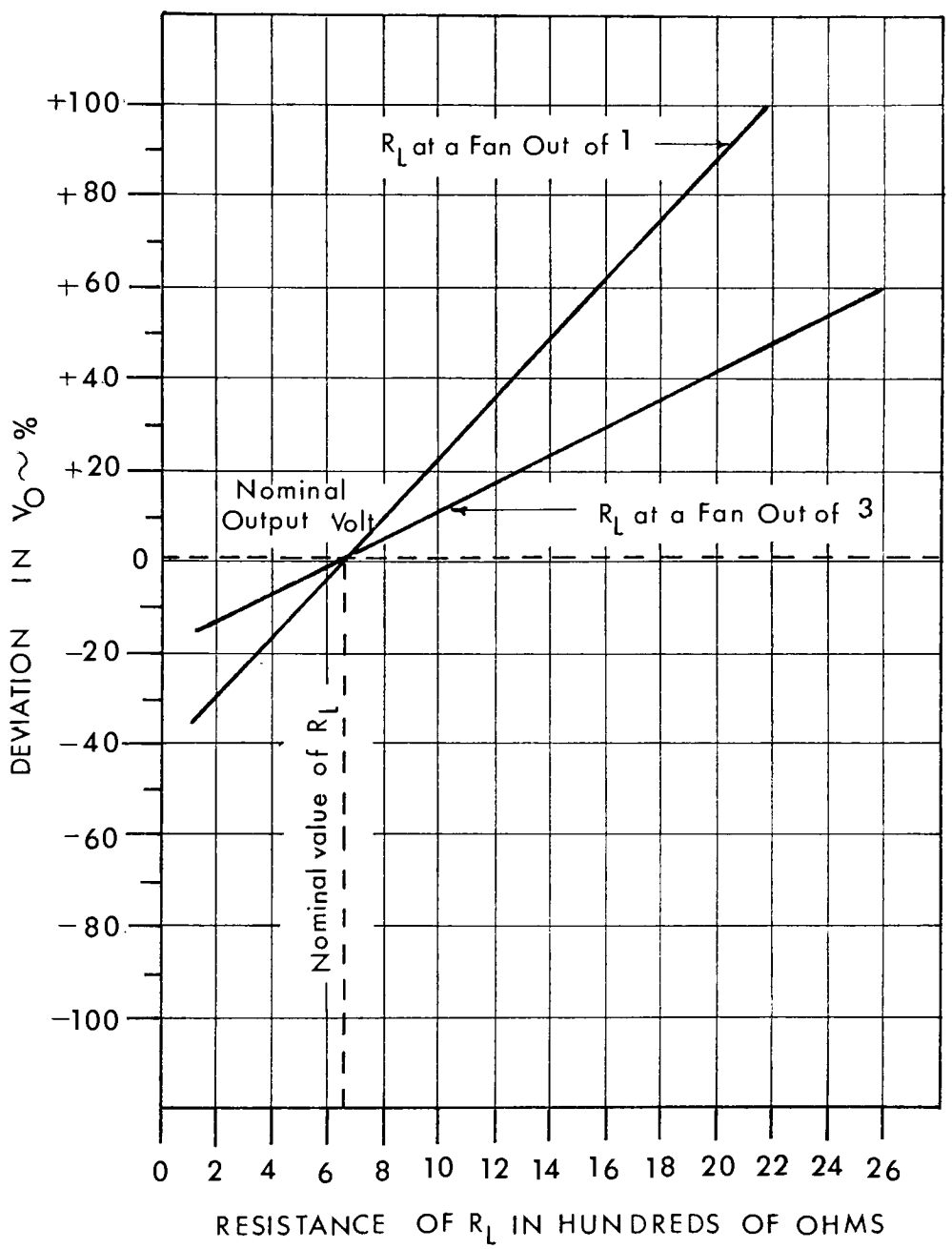
(a) RTL Logic Gate with Loading.
(b) Equivalent Circuit of (a).

FIGURE 2

It can be seen from Eq. 2 that for the nominal values in Figure 2 a change in the value of R_L will result in a corresponding change in V_O as plotted in Curve 1. Also, a plot of the change in V_O as a function of the value of R_B, using the nominal values in Figure 2, is shown in Curve 2. From these plots it can be seen that a change in the value of either R_L or R_B will have a significant effect on the output of the logic gate. Simulating failures by determining the sensitivity to component changes for a fan-out of three, illustrates the ability to detect multiple failures at the output of the gate. However, as shown in Curves 1 and 2, these simple internal failures degrade the information being processed by the gate.

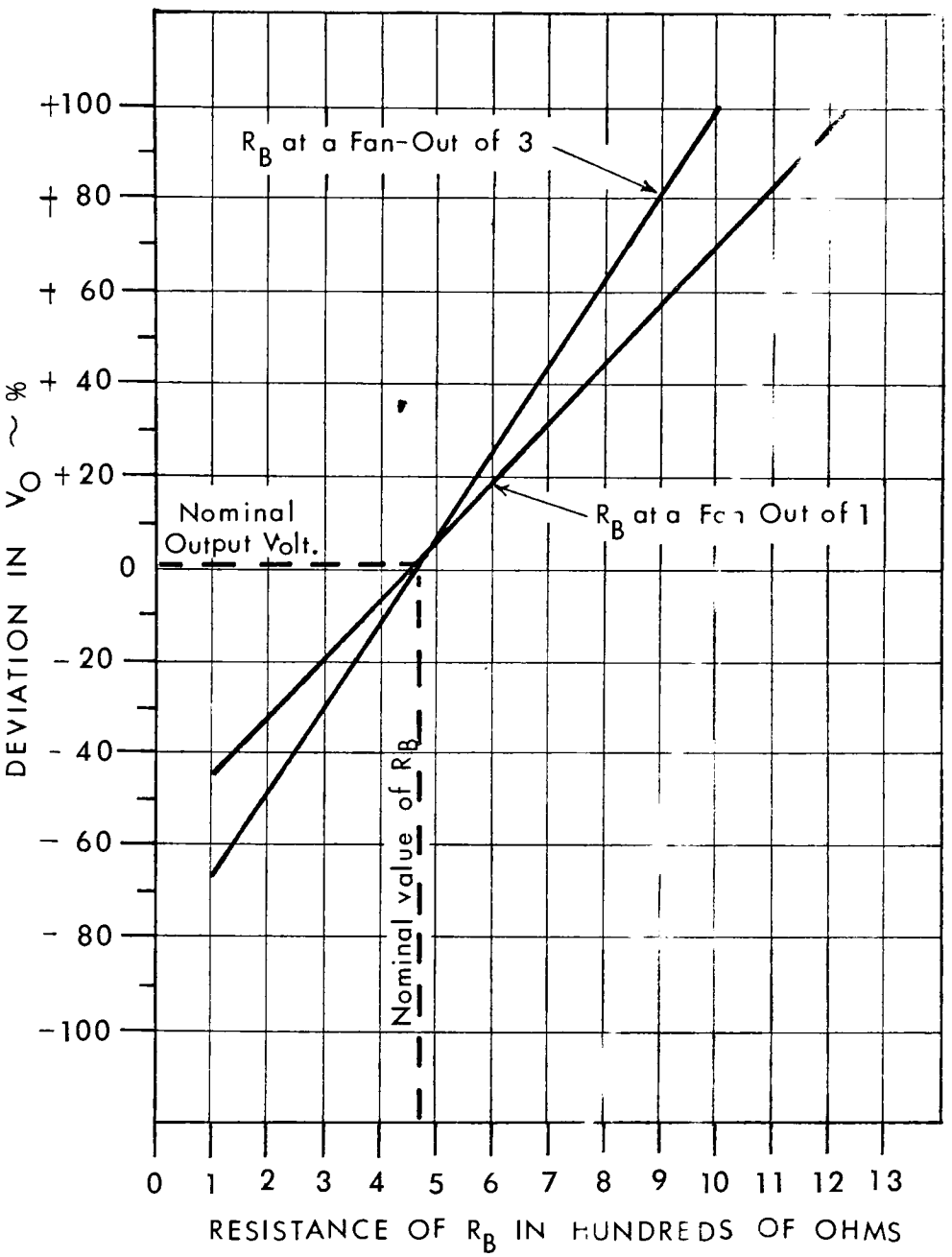
Whereas the discussion on an RTL gate showed the effects of passive component failures on the gate's output, the analysis for the DTL gate in Figure 3 will illustrate the effect of internal component failures on the current gain of the output transistor of the gate. An important property of this type [1] of DTL gate is the current gain (A_i) which is defined as the ratio I_C/I_B. In terms of the circuit components in Figure 3, A_i is given as:

$$A_i = \left[\frac{n \cdot m \cdot I_s \cdot (R_D + R_K)}{V_{DD} - V_{BES}}\right] \cdot \left[\frac{1 + (V_{CC} - V_{CES})/(n \cdot m \cdot I_s \cdot R_L)}{1 - (V_{BB} + V_{BES}) \cdot (R_D + R_K)/(V_{DD} - V_{BES}) \cdot R_B}\right] \qquad (3)$$



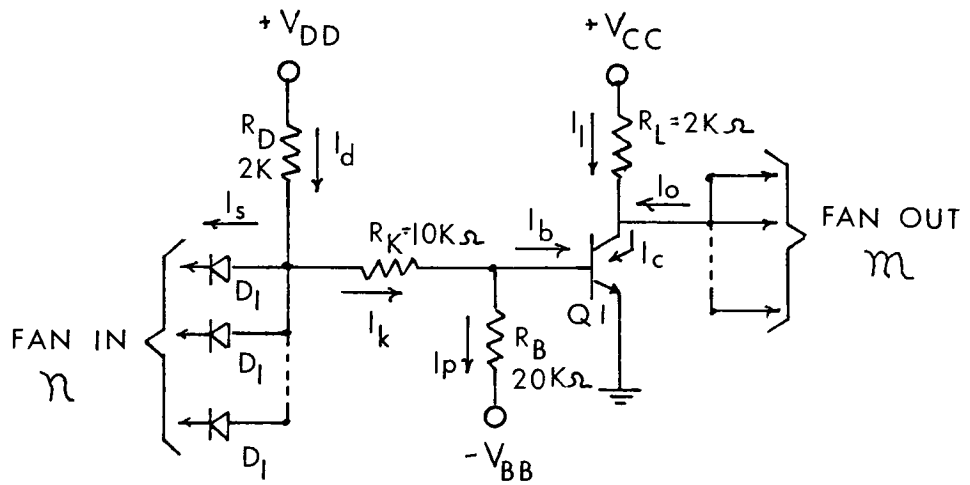
Plot of the Output Voltage as a Function of the Change in R_L for the RTL Gate of Figure 2

CURVE 1



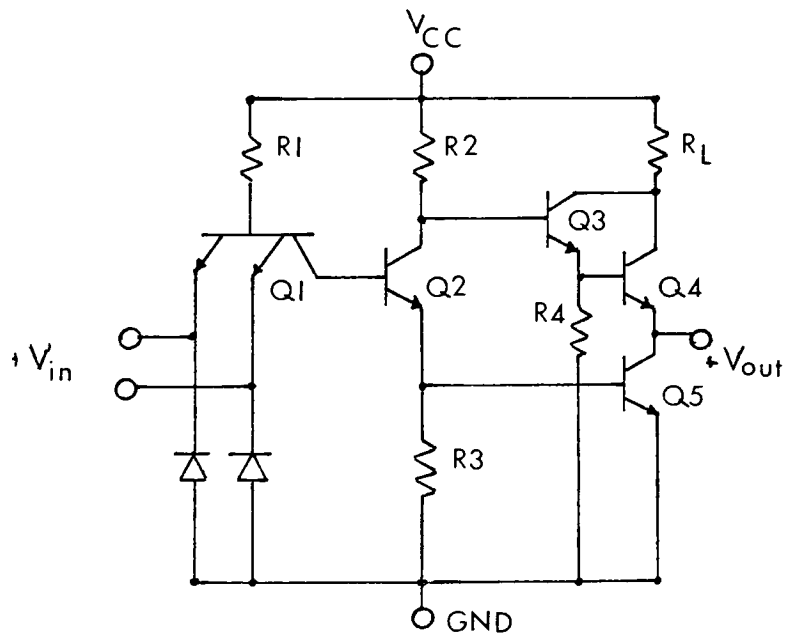
Plot of the Output Voltage as a Function of the Change in R_B for the RTL Gate of Figure 2

CURVE 2



DTL NAND/NOR Gate.

FIGURE 3



TTL NAND Gate.

FIGURE 4

The obtained results of gain sensitivity to component tolerances for R_D, R_K, R_L, and R_B are as follows:

$$S_{R_D}^{A_i} = \frac{2R_D}{R_D+R_K} \tag{4}$$

$$S_{R_K}^{A_i} = \frac{2R_K}{R_D+R_K} \tag{5}$$

$$S_{R_L}^{A_i} = -1 \tag{6}$$

$$S_{R_B}^{A_i} = -1 \tag{7}$$

Various changes in the component tolerances of Figure 3 have been tabulated in Table 2 as a function of the sensitivity of A_i. These results illustrate the effect of failure modes on the output transistor of the gate. The effects produced may cause the output to malfunction in a manner that will prevent the fan-out gates from being properly activated. Thus, a failure within the DTL gate can be detected at the output but the particular component causing the failure may not always be identified. However, multiple internal failures cannot always be distinguished from single failure modes and as shown for the RTL gate, these types of internal failures may degrade the information being processed by the gate.

TABLE 2

SENSITIVITY OF COMPONENT VARIATIONS FOR THE

DTL GATE IN FIGURE 3

CHANGE IN COMPONENT VALUE	CHANGE IN CURRENT GAIN $\sim \Delta_i$			
	$S^{A_i}_{R_D} \cdot \Delta R_D$	$S^{A_i}_{R_B} \cdot \Delta R_B$	$S^{A_i}_{R_K} \cdot \Delta R_K$	$S^{A_i}_{R_L} \cdot \Delta R_L$
$\pm$20%	$\pm$6.7%	$\mp$20%	$\pm$33.3%	$\mp$20%
$\pm$40%	$\pm$13.3%	$\mp$40%	$\pm$66.7%	$\mp$40%
$\pm$60%	$\pm$20.0%	$\mp$60%	$\pm$100%	$\mp$60%
$\pm$80%	$\pm$26.6%	$\mp$80%	$\pm$133.4%	$\mp$80%

Analysis of the Transistor-Transistor Logic, TTL gate in Figure 4 will be used to illustrate the effects of internal component changes on the operation of this type of gate. The analysis for determining the sensitivity to component changes is given in Appendix C with reference to Appendix A for the procedure. The obtained results of sensitivity to component variations are as follows:

$$S_{R_1}^{A_i} = 1 \qquad (8) \qquad S_{R_2}^{A_i} = -1 \qquad (9)$$

$$S_{R_4}^{A_i} = \frac{R_4 \cdot (\beta+1)}{R_2+R_4 \cdot (\beta+1)} - \frac{R_4 \cdot (\beta+1)}{B \cdot R_L+R_4(\beta+1)} \qquad (10)$$

$$S_{R_2}^{A_i} = \frac{R_2}{R_2+R_4 \cdot (\beta+1)} \qquad (11)$$

$$S_{\beta}^{A_i} = 1 \qquad (12) \qquad S_{R_L}^{A_i} = 1 \qquad (13)$$

From the derivedequations of sensitivity for the circuit it can be seen that a change in the value of R_2 will have a significant effect on the gain of Q_2 and little effect on the gain of Q_3 when switched to the opposite state. Also, a parameter change in Q_3, (Eq. 12), will affect the gate's

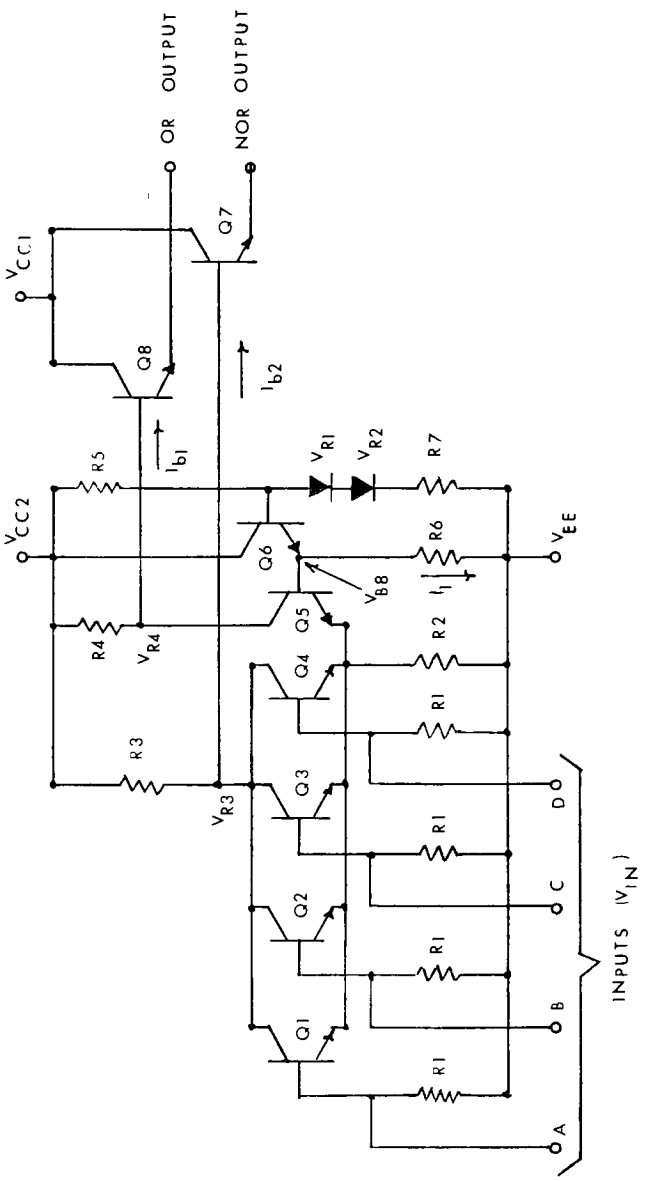
performance in only one binary state. The TTL gate exhibits the same types of faulty output modes as were discussed for the RTL and DTL gates. However, the complexity of the structure masks the identity of most failures from being determined and allows many failures to be detectable in only one of the binary states of the gate.

Analysis of the Emitter Coupled Logic, ECL, gate in Figure 5 will illustrate internal component changes on the operation of this type of gate. The analysis for determining the sensitivity to component changes is given in Appendix D. The obtained results of sensitivity to component variations are as follows:

$$S_{R_4}^{V_{OR}} = 2 \qquad (14) \qquad S_{R_2}^{V_{OR}} = -1 \qquad (15)$$

$$S_{R_3}^{V_{NOR}} = +2 \qquad (16) \qquad S_{R_2}^{V_{NOR}} = -1 \qquad (17)$$

From the derived equations, (Eq. 14 to 16), of sensitivity for the circuit in Figure 5 it can be seen that a change in the value of R_2, R_3, or R_4 will have a significant effect on the norminal output levels of the ECL gate. As with the TTL gate, the complexity of the structure masks the identity of most failures from being determined at the input or out-



Schematic of the ECL Gate.

FIGURE 5

FIGURE 5

put terminals of the gate. Also, an unspecified change in the transistor's beta, R_2, R_3, or R_4 will produce failures that are usually detectable in only one of the binary states of the ECL gate (as observed at the output terminal).

This discussion has dealt with the effects of parameter variations at the output of typical logic gates. Based on the previous analysis we have shown that the normal operation of all digital logic families can be affected by internal component failures. The more complicated structures not only increase the possibility of single and multiple failures occuring but may prevent their detection at the input or output terminals of the gate. Based on the supposition that detection of all internal failures is a necessary (but not sufficient) condition for fail-safe logic operation, we can conclude from this analysis that: (1) all internal component failures must be detectable at the output of the logic gate, (2) all multiple failures within the gate's structure must be detectable, (3) detection of all types of failure modes; open-circuits, short-circuits, leakage, etc., must be provided for, and (4) the detection of internal failures must be accomplished in a manner that does not degrade or change the information being processed by a logic gate.

CHAPTER II

DISCUSSION OF THRESHOLD LEVELS

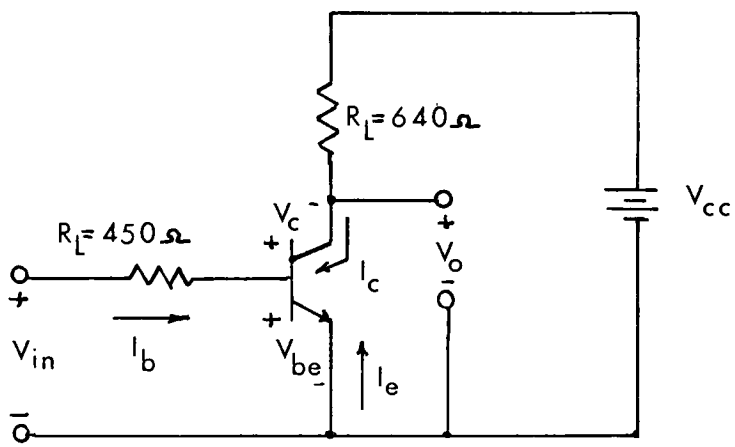
Whereas the previous chapter dealt with the general problem of internal component failure modes of integrated circuits, this chapter will focus on one such type of failure; the instability of internal threshold levels. The purpose of separately identifying and analyzing this failure mode is that fail-safe design techniques will individually address themselves to resolving this failure mode independent of other types of failures. Therefore, it is the intent of this chapter to analyze the threshold level of various types of logic gates to determine their effect on the gate's operation. The threshold level is a function of the internal structure and the gate's ability to maintain its threshold level is essential for proper operation. A change in this level must be considered a failure mode of the gate if it causes the gate to produce a faulty output independent of other internal failures.

An example of the change in base-to-emitter junction voltage, V_{BE}, as a function of temperature is given in Appendix E. The obtained results show that V_{BE} is about 0.6 volts at room temperature and as the temperature increases, V_{BE} decreases at the rate of 2.5 millivolts per

degree centigrade. The significance of this change in V_{BE}, as it affects the threshold voltage level of an RTL gate (Figure 6) is shown plotted in Curves 3, 4, and 5. The analysis of the RTL gate, using the Newton-Raphson Method, is given in Appendix E. Curve 3 illustrates the change in threshold level that can be expected from the RTL gate as the temperature varies from 200°k to 400°k. The effect of this change in threshold level is significant because the input varies by the amount $\triangle V_T$. Curve 4 is a plot of the same input/output transfer characteristics shown in Curve 3 with the additional constraint that R_B has exhibited a change in value consisting of a -100% decrease from its nominal value of 450 ohms. This plot illustrates the effect of an internal component failure on the threshold level of the gate. Curve 5 is a similar plot with the constraints that R_B is reduced in value by -100% and R_L is increased from its nominal value of 640 ohms by +100%. This plot illustrates the effect of multiple component failures on the gate's threshold level.

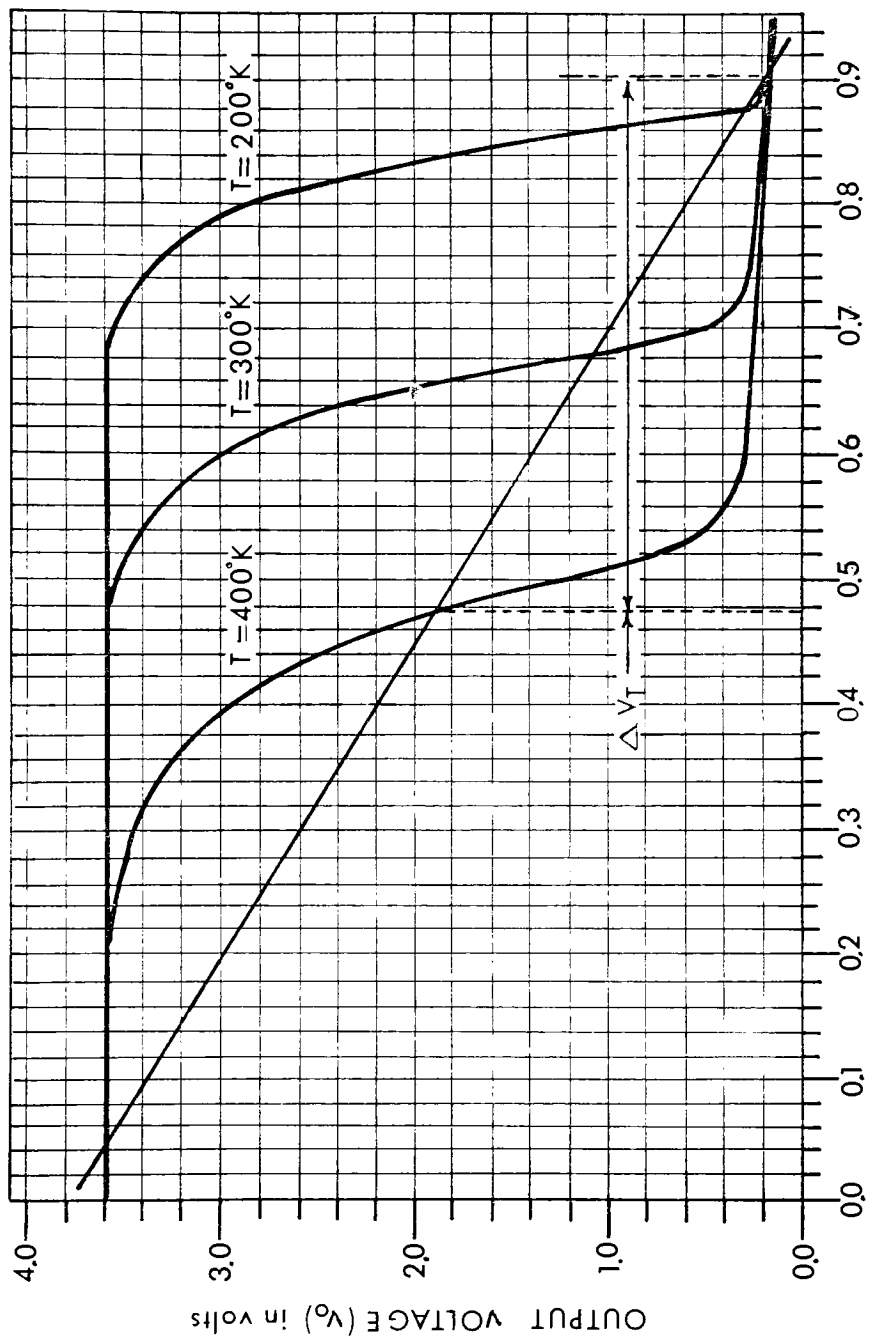
Using the analysis for the ECL gate, given in Appendix D, the sensitivity of threshold voltage (V_{BB}) with respect to internal gate components are as follows:

$$S_{R_5}^{V_{BB}} = \frac{R_5 \cdot (R_6+R_7)}{R_5 \cdot (R_6+R_7)+R_6 \cdot R_7} - \frac{R_5}{R_5+R_7} \qquad (18)$$



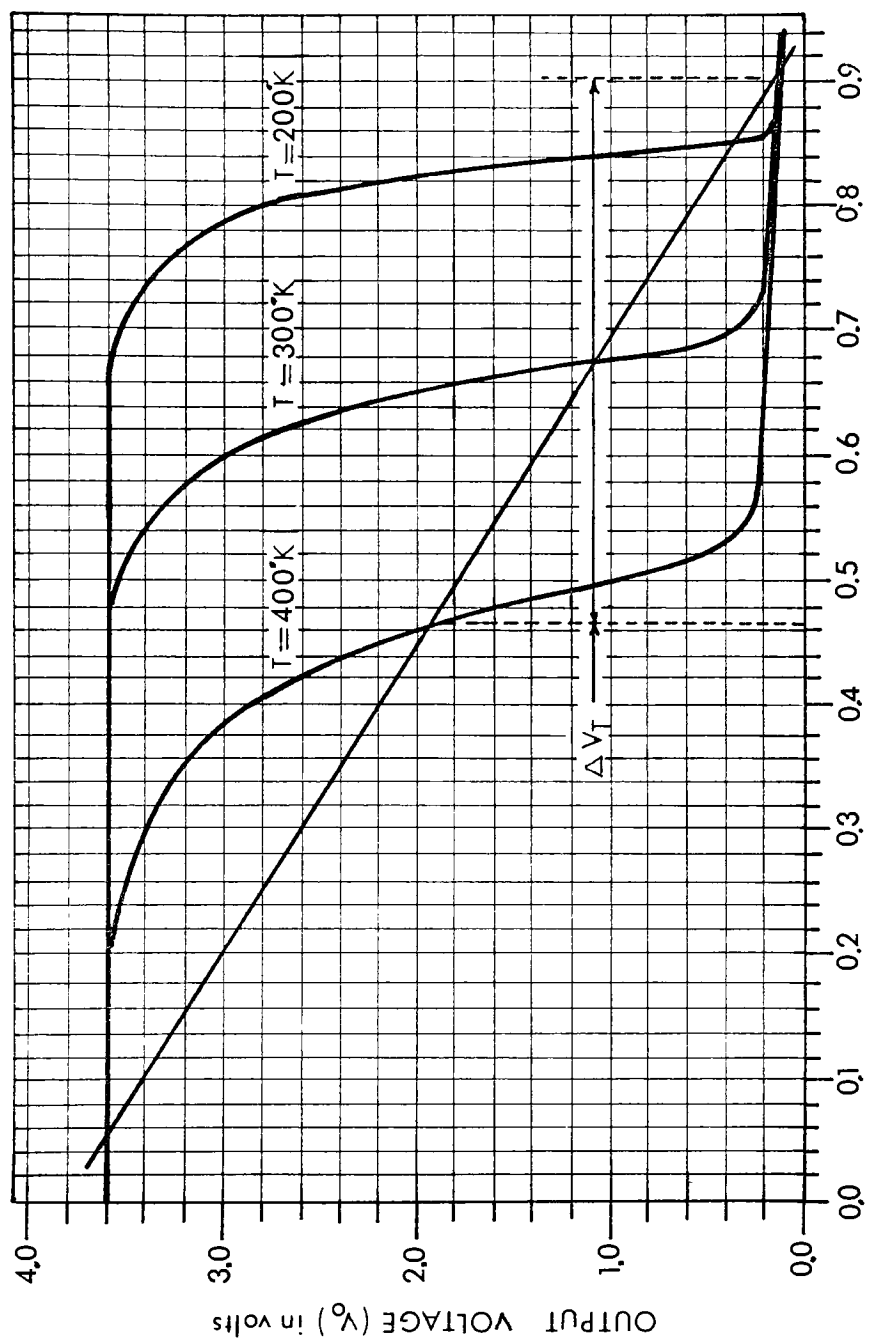
Schematic of a RTL Gate.

FIGURE 6



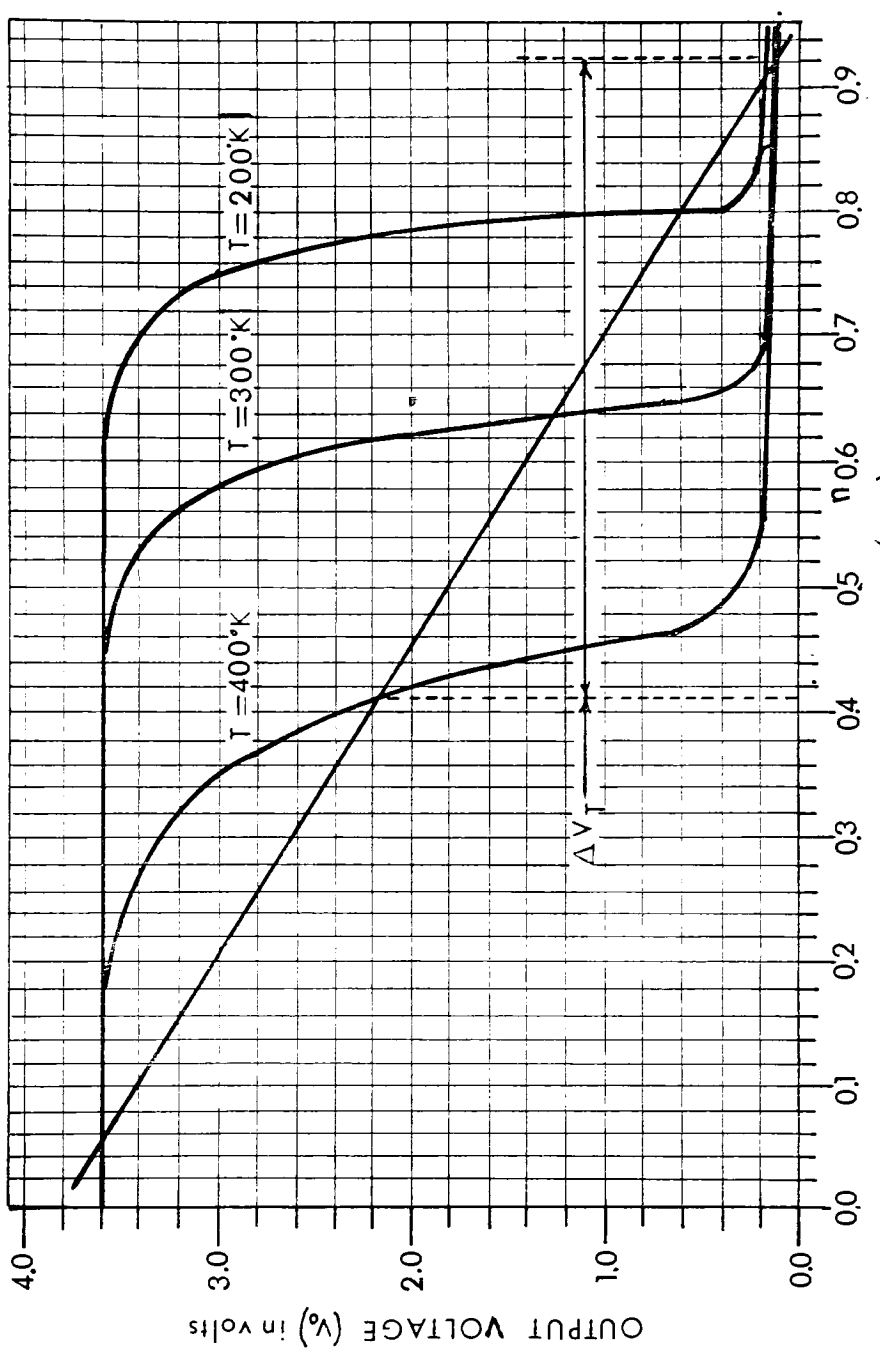
Input/Output Transfer Characteristics of a RTL Gate.

CURVE 3



Input/Output Transfer Characteristics of a RTL Gate with a Failure in the Base Resistor.

CURVE 4



Input Output Transfer Characteristics of a RTL Gate with Failures in both the Base & Load Resistors.

CURVE 5

$$S_{R_6}^{V_{BB}} = \frac{-R_5 \cdot R_7}{R_5 \cdot R_7 + R_6 \cdot R_7 + R_5 \cdot R_6} \qquad (19)$$

$$S_{R_7}^{V_{BB}} = -\left[\frac{1}{R_7/R_6 + R_7/R_5 + 1}\right] + \left[\frac{1}{R_5/R_7 + 1}\right] \qquad (20)$$

$$S_{V_F}^{V_{BB}} = 2 \qquad (21) \qquad S_{B}^{V_{BB}} = -1 \qquad (22)$$

$$S_{V_{BE}}^{V_{BB}} = -2 \qquad (23) \qquad S_{V_{EE}}^{V_{BB}} = +1 \qquad (24)$$

From these results we can see that some component failures will have a significant effect on the threshold level of the ECL gate. In comparison to the RTL gate, the complexity of its structure is an added disadvantage as well as the smaller output voltage swing. Thus, the greater voltage swing required between logical 1 and logical 0 levels will allow for greater variations in component changes before affecting the threshold of the gate.

A similar analysis has been calculated for a TTL type integrated Schmitt trigger circuit in Appendix F. From these results, we can determine the sensitivity of its

threshold voltage to component changes to be:

$$S_{R_E}^{V_{T+}} = + \frac{R_{EQ.}}{R_E+R_{EQ}} = +0.62 \qquad (25)$$

$$S_{R_{EQ.}}^{V_{T+}} = - \frac{R_{EQ.}}{R_E+R_{EQ.}} = -0.62 \qquad (26)$$

$$S_{V_{BE}}^{V_{T+}} = 0 \qquad (27)$$

$$S_{R_2}^{V_{T-}} = - \frac{R_2}{(R_2+R_E)} = -0.81 \qquad (28)$$

$$S_{R_E}^{V_{T-}} = - \left[1+\frac{R_E}{R_E+R_2} \right] = -1.19 \qquad (29)$$

As expected, the resistor R_E is critical for proper threshold detection. A failure in R_E will cause improper detection of the input signal level being applied to the gate.

In addition to the conclusions brought forth in the previous chapter, several additional conclusions can be reached from this analysis. It is apparent that the threshold level is a critical parameter for fail-safe logic and such designs must either provide the means to maintain this level

or the ability to detect an out of tolerance condition at the output of the gate. The analysis has shown the difficulty in maintaining the threshold level because of its dependency on the components and parameter in the structure of the logic gate. Therefore,all fail-safe logic must have the property of providing threshold detection for gates.

CHAPTER III

TYPES OF LOGIC FAULTS

The preceeding chapters have dealt with the failures internal to the structure of integrated circuits. All other types of potential failure modes shall be investigated herein; i.e., all potentail failures that occur external to the structure of the logic gate shall be considered as logic faults. The purpose of this chapter is to identify and analyze various logic faults so as to define the remaining types of faults fail-safe logic must resolve. A discussion of common methods used for logic fault detection is given in Appendix G., along with a discussion of hazard faults in Appendix H.

The logic faults to be considered are assumed to be permanent or solid, i.e., once a permanent fault occurs it will not disappear or change its nature. Also, intermittent faults or transient faults are considered in regards to a predefined time interval. These general categories of faults[2] can be further identified as follows:

A. PERMANENT LOGIC FAILURES

1. An output is stuck at a logic 1 or 0 (possibly due to shorted or open-circuited transistors).
2. A logic gate does not respond to one or more inputs (possibly due to a failed diode).
3. An output is slow to change after the input

changes (possibly due to deteriorating rise or fall time).

4. An output which fans out is logic 1 at some inputs and logic 0 at others.

5. Multiple failures.

6. Failure of a complete chip (possibly due to a power connection break or physical damage to the chip).

7. The shorting of two or more circuits on a single chip (possibly due to failure of a crossover).

B. INTERMITTENT LOGIC FAILURES

1. Electromagnetic coupling of noise into a logic gate.

2. Loose wires or particles in the integrated circuit.

3. Unusual conditions on the primary power input.

4. Temporary overheating of part of the circuit.

5. Random drift in the delay characteristics of a circuit which is used in logic with critical timing.

Fail-safe logic should be capable of detecting bridging faults. A bridging fault occurs when two leads in a logic network are connected accidentally and wired logic is performed at the connection. This type of fault [3] can occur in the following configurations:

1. Inside the integrated circuit package where a crossover connection is a result of defective masking, etching of conductors, breakdown of insulators, etc.

2. Integrated circuit packaging provides bridging faults due to the soldering between the tiny solder pads on the chip and the pins of the package. Two adjacent wires may come into contact when one shakes loose from stress or excessive

solder may establish a so-called "solder bridge" between pads.

3. At the circuit board level shorts may be caused by defective printed circuit traces, feedthroughs, loose or excess bare wires, or solder bridges.

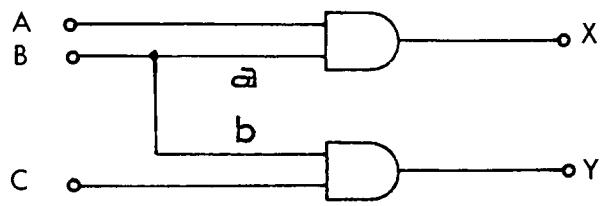
The majority of bridging connections happen at the logic gate level where only the input and output leads of logic gates are involved.

Most failures in digital networks belong to the class of "Stuck-At" faults.[4][5] They are faults which cause a logic gate's input line or output line to become stuck at logic value 1 (S-@-1) or logic value 0 (S-@-0). The faulty lines do not actually assume the corresponding signal values but the circuit behaves as though the particular logic gate's input or output line assumes that "Stuck-At" value. In considering a two-input AND gate, there are four possible binary input patterns; 00, 01, 10, and 11. Some input failures will not cause the output to change, i.e., they are masked. For example, if 00 is applied to the inputs of an AND gate, the output will be affected only when both inputs are S-@-1 and all other possible stuck failures will be masked. If we apply the input pattern 11 to an AND gate, then either or both one's being S-@-1 will cause a change in the output. Therefore, the most sensitive input pattern for a multiple input AND gate is, 111....1. The most sensitive input pattern for OR and NOR gates are all zero inputs. For Exclusive-OR gates all the possible input patterns

have equal sensitivity to stuck-at faults.

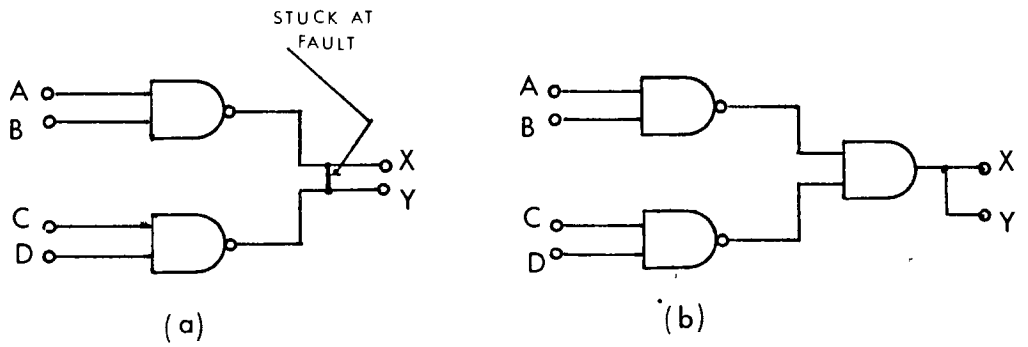
Although an input or output of some gate may assume a fixed logical value independent of the inputs applied to the gate, it should be noted that faulty wires do not actually assume the corresponding signal values but the logic network behaves as if the particular gate input or output assumes that fixed value. For example, in Figure 7, if the wire "a" becomes stuck at the signal value corresponding to logical 1, the wire "b" which is directly connected to it will also become logical 1. However, if the input lead "a" to the AND gate becomes open-circuited the output X becomes independent of the input value B but the output Y of the second AND gate is still BC.

As an example of output logical faults that cannot be represented by S-@-0 or S-@-1, consider the network of Figure 8. Assuming that diode-transistor logic (DTL) is used, if the output of two independent NAND gates are connected together by a bridging fault, both outputs become equal to the AND of the NAND gate outputs as shown in Figure 8B. Consequently, a single fault can cause two independent gates to change their logical function. In some circuits the presence of certain physical faults do not alter any of the functions realized by the logic network. This implies that such faults cannot be detected by applying inputs to the network and observing the outputs. Consider the network of Figure 9 and let the wire "a" be S-@-1. The truth table



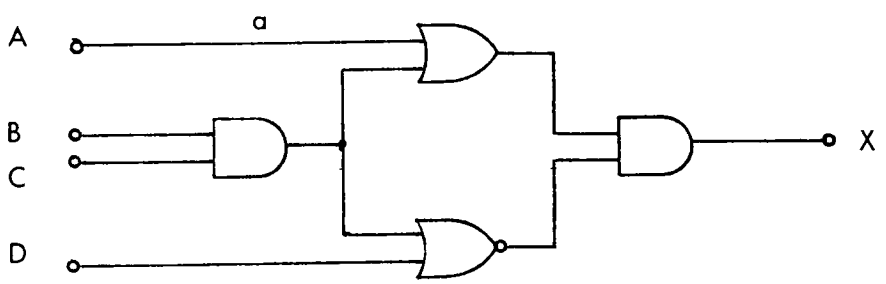
AND Gates ILLustrating Open-Circuit Input Lines.

FIGURE 7



(a) NAND Gates ILLustrating Output Stuck-at-Faults. (b) Equivalent Logic Network.

FIGURE 8



Network ILLustrating Fault Masking.

FIGURE 9

of the output functions of the normal and faulty network are shown in Table 3. We observe in Table 3 that only when the input variables are at the following logic states will an error be produced at the output.

$$ABCD = [0000] , [0010] , [0100] .$$

The problem of multi-valued lines exist when the logic value at all points along a line is not the same although the line may be connected to the inputs of different gates. In Figure 10, it is assumed that the logic value of lines "a", "b", and "c" are identical. If we take the structure of the logic gates into consideration, we observe that the assumption of singled valued lines is not valid. For example, an open-circuit at an input of gate 2 or at gate 3 (assuming a failure such as the input diode of the gates) does not affect the logic value of other terminals because the open-circuit point is floating. However, if the output of gate 1 is S-@-1, it will always force the corresponding inputs of gate 2 and gate 3 to be logical 1. It is possible that a fault at one input terminal will result in all other terminals connected to the faulty terminal being stuck. For example, in Figure 10, a short circuit between the base and emitter of the transistor (DTL logic gates) will cause both lines "a" and "b" to be S-@-0. Therefore, the actual situation may depend on the internal gate's structure.

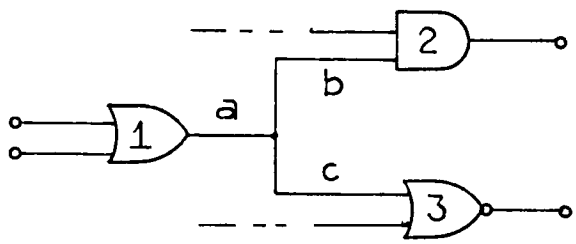
Two failures, i,j, are said to be indistinguishable if for all possible input and control input combinations,

TABLE 3

TRUTH TABLE OF NORMAL (Z) AND FAULTY (Z^a)

OUTPUT FUNCTIONS OF NETWORK IN FIGURE 9

A	B	C	D	Z	Z^a
0	0	0	0	0	1
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	1	1
1	0	0	1	0	0
1	0	1	0	1	1
1	0	1	1	0	0
1	1	0	0	1	1
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0



Example of a Mult-valued Fault Line in a DTL Logic Network.

FIGURE 10

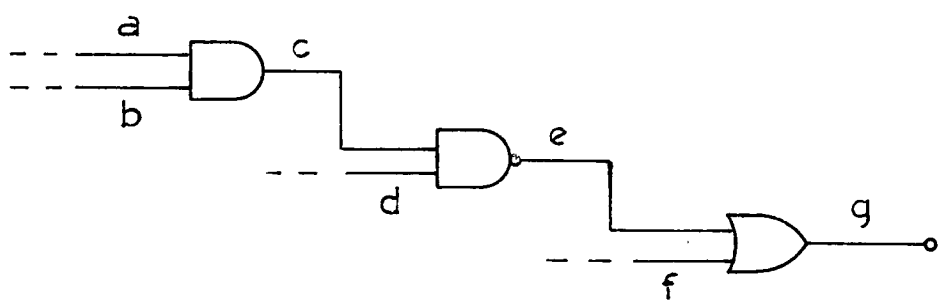


ILLustration of Indistinguishable Faults.

FIGURE 11

the output of the gate with failure i is the same as the output of the gate with failure j. Certain types of indistinguishable failures can easily be identified. For example, given an OR gate with lines "a" and "b" as input terminals and line"c" as the output terminal, the conditions that line "a" is S-@-1 and line "c" is S-@-1 are indistinguishable (if line "a" has a fan-out equal to one) because for either of the failures the output of the OR gate is always equal to 1, and line "b" S-@-1 is also indistinguishable from line "a" or line "c" S-@-1 for the same reason. Similarly, the indistinguishable failures for the other types of gates are as follows:

AND GATE; Any input S-@-0 and output S-@-0.

NOR GATE; Any input S-@-1 and output S-@-0.

NAND GATE; Any input S-@-0 and output S-@-1.

For networks with many cascaded gates the indistinguishable faults may propagate through several levels of gates. For example, in Figure 11, lines "a" or "b" being S-@-0 will cause line "c" to be S-@-0, line "c" S-@-0 will cause line "e" to be S-@-1, and line "e" S-@-1 will cause line "G" to be S-@-1. Therefore, lines "a", "b", "c", and "d" S-@-0 and lines "e", "f","G", S-@-1 are all indistinguishables.

Therefore, we observe that common logic faults are not always easy to detect. The difficulty in detecting stuck-at faults on a network level can be correlated to the

severity of determining internal failures of logic gates, i.e., the more complex the network, the more difficult is the task of determining the presence of the logic fault. The procedure we will utilize in fail-safe logic will be based on the detection of faults at all levels of the logic network, thus eliminating many difficulties presently encountered in identifying and detecting logic faults.

CHAPTER IV.

PROPERTIES OF FAIL-SAFE LOGIC

The previous discussions and analysis have shown the multiple limitations of logic families. It is these modes of internal and logic faults that we will attempt to resolve by establishing: (1) The general properties of fail-safe logic, (2) the advantages and limitations of CMOS logic, (3) pertinent fail-safe design techniques and (4) the analysis for a fail-safe logic gate. It is the intent of this chapter to identify the necessary conditions and characteristics of fail-safe logic circuits. Based upon the previous analysis, the necessary conditions for fail-safe logic are: (1) The ability of all gate threshold levels to either remain stable for all fault conditions or be detectable at the output of the gate or network, (2) the ability of all logic gates to remain insensitive to internal component failure modes or be able to detect and respond to all such faults, and (3) the ability of the logic network to detect all single or multiple fault combinations occurring between the terminals of any and all logic gates in the network.

In providing these conditions it is suggested that fail-safe logic have the following properties: (1) The

ability to inhibit operation of the circuit's function as soon as possible after a fault is detected, (2) the ability to detect all logic faults at the gate level of operation, (3) the ability to detect failures so that all information being processed by the gate or network cannot be changed or degraded, (4) the ability to prevent masking of logic faults, (5) the ability to prevent faults from propagating through the network and (6) the ability to provide detection for "out of tolerance" circuit or internal component changes.

Unrestricted faults may cause any number of possible erroneous failures in a circuit and the ability to check for all possible conditions will require some type of detection circuitry. It is known that if a circuit is duplicated and both circuits are operating independently and in parallel with similar but isolated inputs, then by dynamically comparing the outputs of both circuits any error or fault which does not appear simultaneously in both will be immediately detected. The problem lies in multiple faults common to both circuits that can occur: through common grounds, power lines, simultaneous masking of multiple but different faults, or in the system's ability to evaluate the dynamic outputs. Modification of this basic concept, using CMOS logic, is also considered a characteristic of fail-safe logic.

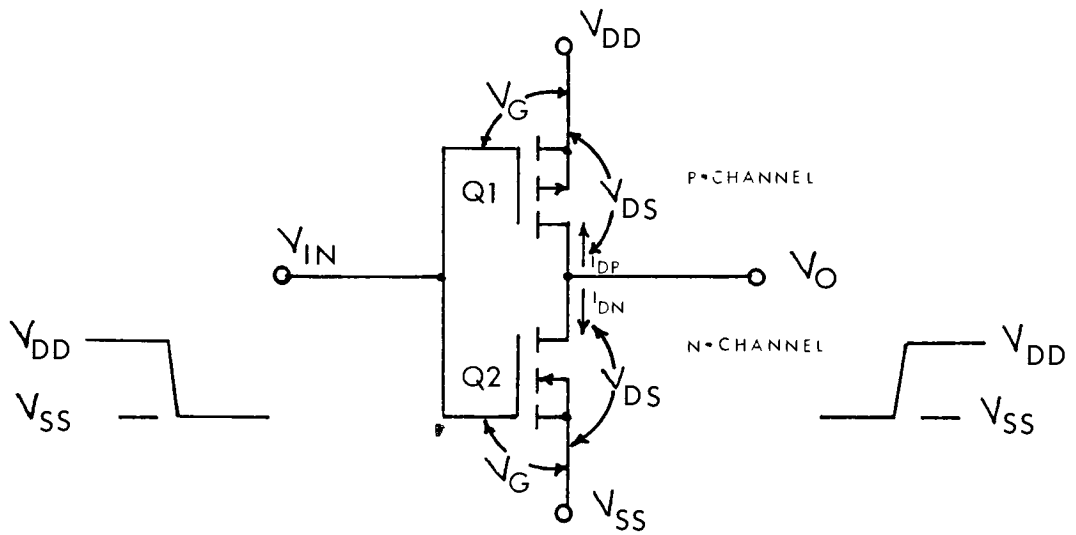
CHAPTER V.

BASIC PROPERTIES AND LIMITATIONS OF THE CMOS LOGIC GATE

The Complementary Metal Oxide Semiconductor, CMOS,[6] is presented herein as a logic family suitable for fail-safe design. The basic CMOS Inverter is analyzed in Appendix I., and the simplicity of its internal structure, as shown in Figure 12, is apparent when compared to the other logic families previously discussed. The intent of this chapter is to identify those characteristics of the CMOS gate which make it useable in fail-safe logic and to point out several of its limitations that will effect its usefulness.

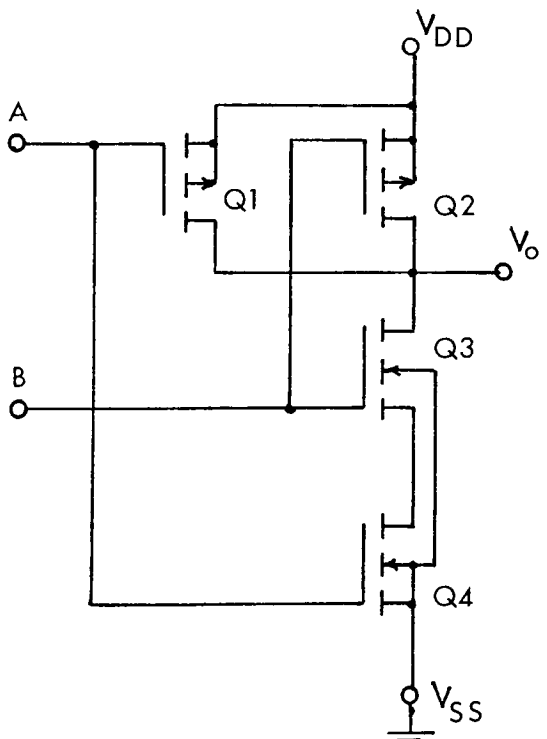
The selection of the CMOS gate is based upon the following characteristics: (1) The complementary nature of its circuit, (2) the symmetry associated with its voltage transfer characteristics, (3) its ability to function as a three-terminal device (discussed in a later chapter), and (4) the simplicity of its internal structure.

The CMOS NAND gate, as shown in Figure 13, will be utilized as the basic building block of fail-safe logic. The input gates of transistors Q1 and Q4 are tied together to form input 1 of the basic inverter. The input gates of transistors Q2 and Q3 form input 2. Transistor Q3 acts as



Internal Structure of the CMOS Inverter.

FIGURE 12



TRUTH TABLE

A	B	V_o
0	0	1
0	1	1
1	0	1
1	1	0

0 = GND. 1 = +10v.

Structure & Truth Table of a Two Input CMOS NAND Gate.

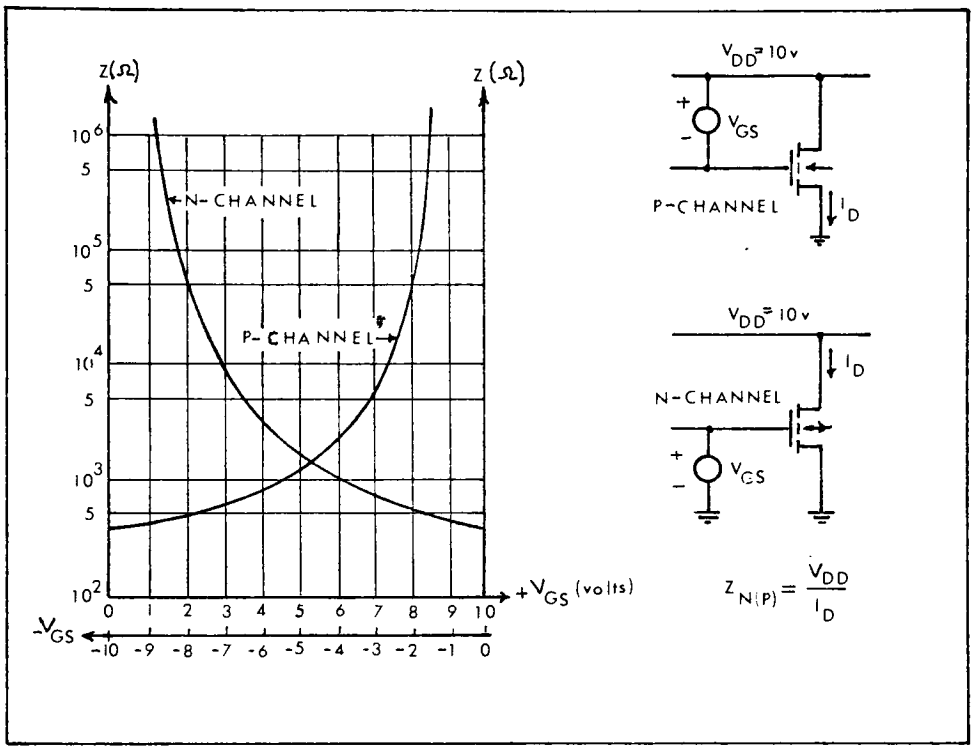
FIGURE 13

a series resistance which is extremely high or low depending upon its input signal in the inverter formed by Q1 and Q4. Likewise transistors Q4 acts as a series resistance in the other inverter configuration. The output of the circuit is at ground (V_{SS}) potential only when both transistors, Q3 and Q4, are in saturation. This occurs when both inputs 1 and 2 are at V_{DD}. Since the output is equally isolated from both V_{DD} and V_{SS} the gate can operate with negative as well as positive supplies. The only requirement is that V_{DD} be more positive than V_{SS}.

Since the gate's MOS transistors are mainly voltage controlled resistors, the transfer region is determined by the parallel/series combination of the transistor impedances in conjunction with the input voltages, the number of inputs, and the gate circuit configuration. The transfer region of the gate (Appendix I) can be defined as:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = \Delta V_{MAXIMUM} \qquad (30)$$

As shown in Figure 14, the values of the standard transistor ON resistance may vary from 10 megohms to 30 ohms depending on the physical dimensions of the MOS transistor and the value of the applied voltages. For the NAND gate the transfer region is given by the ratio of the impedance of the N-channel



Typical N— and P—Channel Impedance. [6]

FIGURE 14

transistors connected in series and the P-channel transistors connected in parallel. Using these conditions for the CMOS NAND gate, the bounds of the transfer voltage can be defined (approximately) by the empirical equations[6] listed below:

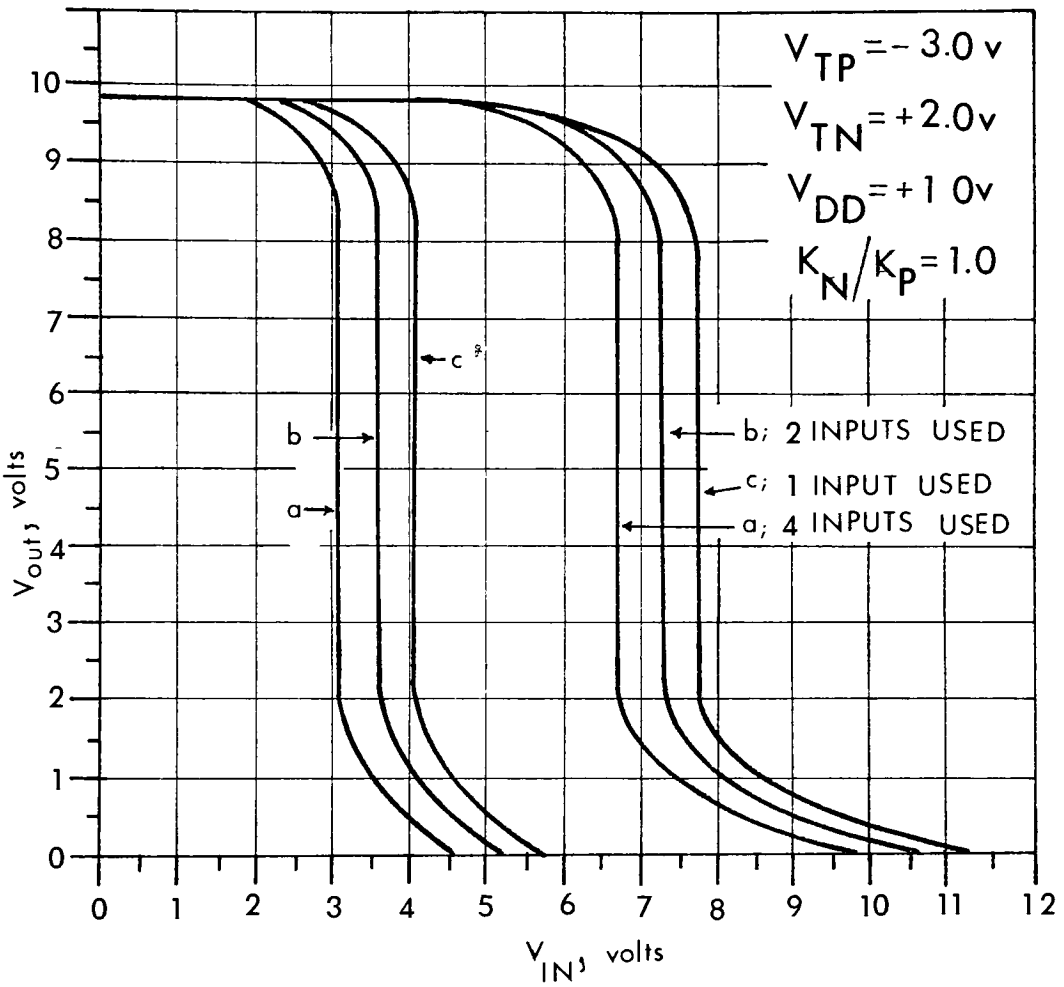
$$V_{LOWER\ BOUND} \cong V_{DD} \cdot \left[\frac{1}{1.5+N_X/N_T} - 0.1\right] \qquad (31)$$

$$V_{UPPER\ BOUND} \cong V_{DD} \cdot \left[0.9 - \frac{1}{1.5+N_X/N_T}\right] \qquad (32)$$

Where; N_X = Total number of inputs per gate.

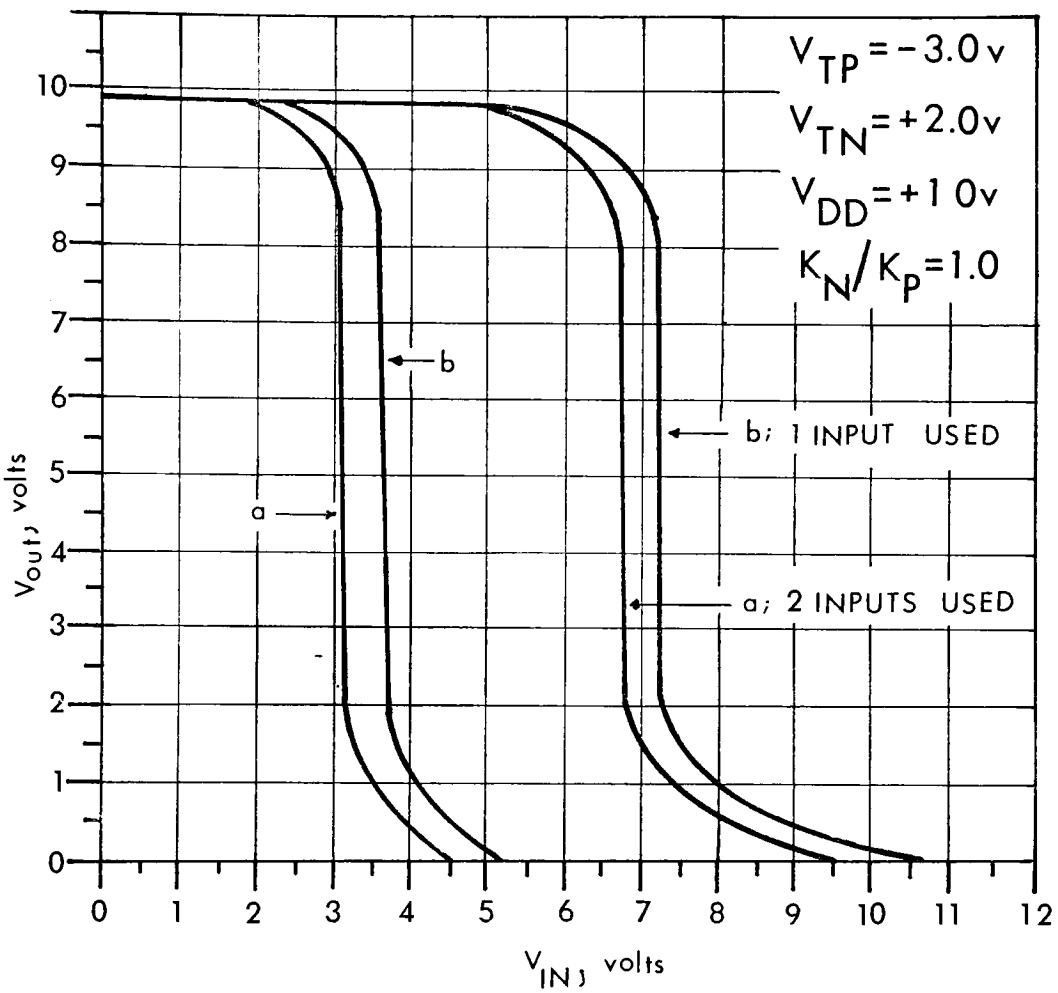
N_T = Number of used inputs per gate.

A plot of eq. 31 and 32, for all input combinations of a four input NAND gate, is shown in Figure 15. The significance of this plot is to place a restriction on the NAND gate as to the number of gate interconnections allowed because of the large variation in transfer voltage that can occur. When considering the two input NAND gate, we will utilize both gate inputs. This restriction will impact the size of any given fail-safe logic network but will provide better transfer voltage control of the gate as illustrated in Figure 16. From these plots we observe that the transfer voltage can vary significantly as a function



Maximum & Minimum Voltage Transfer Characteristics for the Four Input NAND Gate.

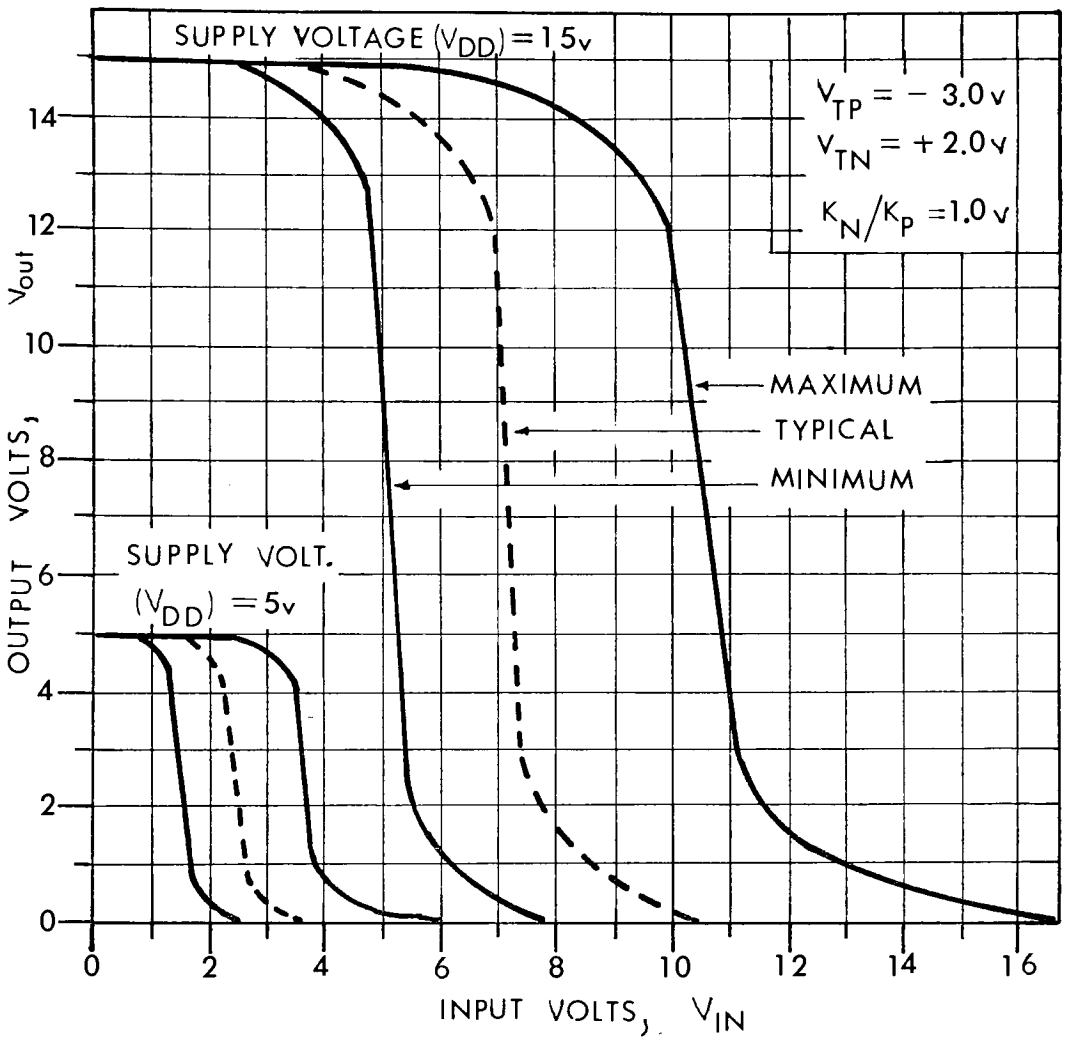
FIGURE 15



Maximum & Minimum Voltage Transfer Characteristics for the Two Input NAND Gate.

FIGURE 16

of various gate parameters. This wide voltage transfer spread must be considered in checking or detecting variations in the gates' threshold levels. A plot of the minimum and maximum voltage transfer characteristics for the two-input NAND gate, as a function of the V_{DD} supply voltage, is shown in Figure 17. This plot will be utilized later on in conjunction with the operation of a fail-safe gate.



Maximum & Minimum Voltage Transfer Characteristics of a Typical Two Input NAND Gate for Supply Voltages (V_{DD}) of 5vdc & 15vdc.

CURVE 17

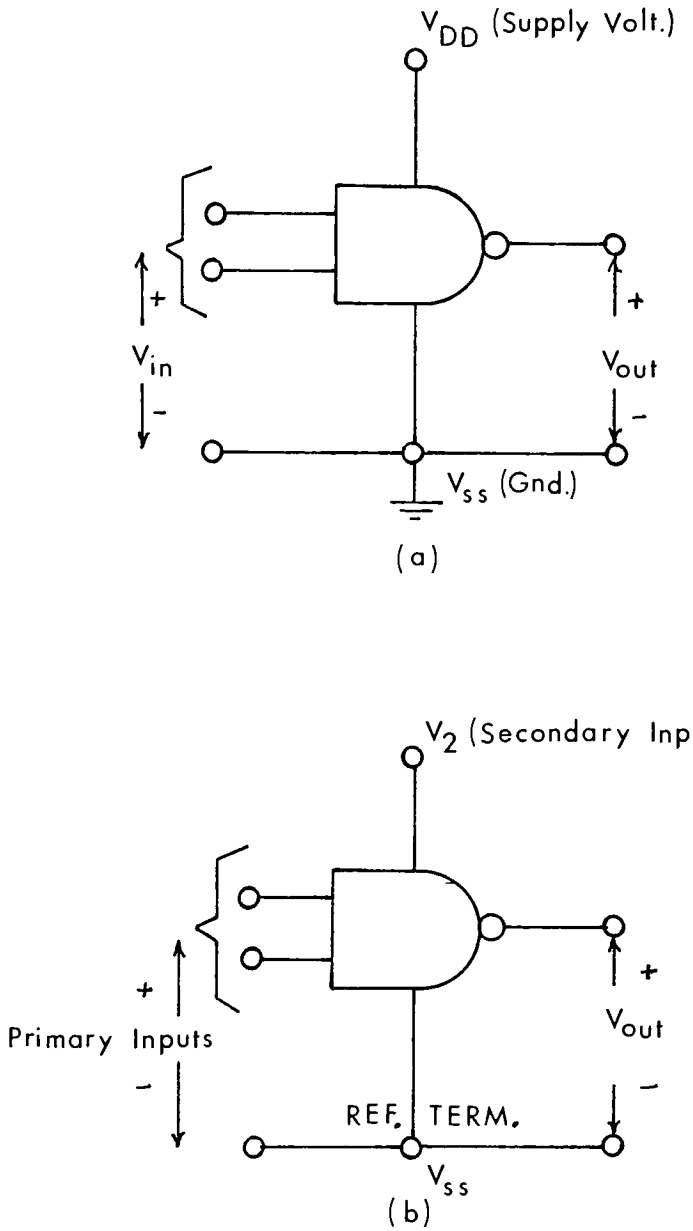
CHAPTER VI

DISCUSSION OF FAIL-SAFE DESIGN TECHNIQUES

The purpose of this chapter is to identify and discuss how various techniques can be implemented to overcome the short comings of integrated circuit failure modes and logic faults. Although the methods are presented individually, it is intended that they be combined (discussed in a later chapter) to be effective in the use of fail-safe logic.

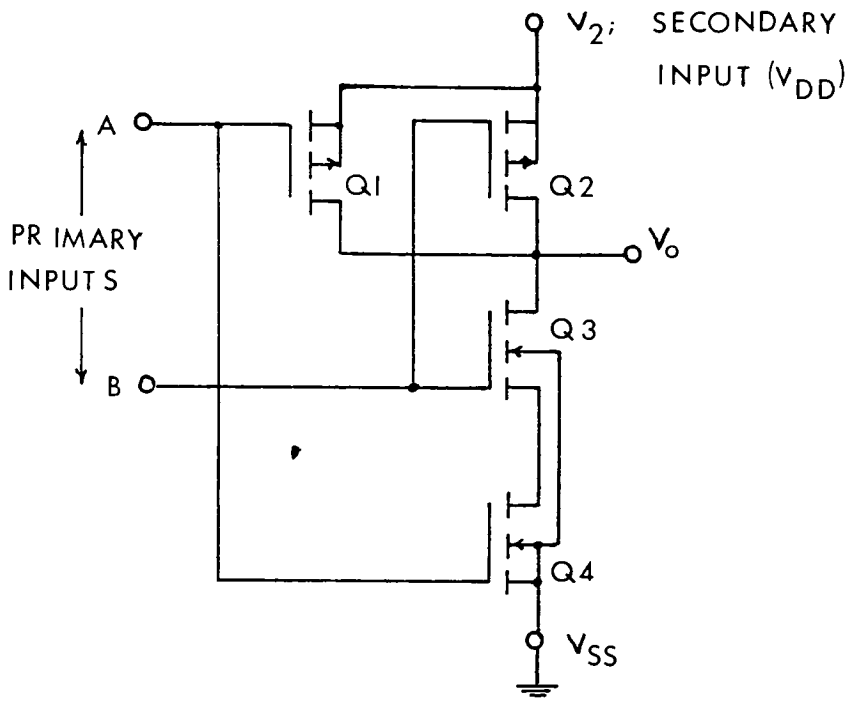
THREE TERMINAL LOGIC GATE

We shall redefine the CMOS logic gate as a device which can function as a three terminal logic gate. Figure 18b shows the CMOS gate of Figure 18a with its terminals redefined. The difference being that the reference terminal must always be at a potential less than the secondary input terminal (not necessarily ground) and that the secondary terminal will not be held constant but will change periodically within given operating tolerances. Figure 19 shows the structure of the three terminal gate and its truth table modified to define the normal operating states of all internal semiconductors. By allowing the secondary input, V_2, to take on particular values, we have a means



Comparison of (a) Two Input CMOS NAND Gate, (b) a Three Terminal logic Gate.

FIGURE 18



PRIMARY INPUTS A	B	OUTPUT V_O	INTERNAL STATES Q1	Q2	Q3	Q4
1	1	0	OFF	OFF	ON	ON
0	1	1	ON	OFF	ON	OFF
0	0	1	ON	ON	OFF	OFF
1	0	1	OFF	ON	OFF	ON

The Structure & Truth Table of a Three Terminal Gate.

FIGURE 19

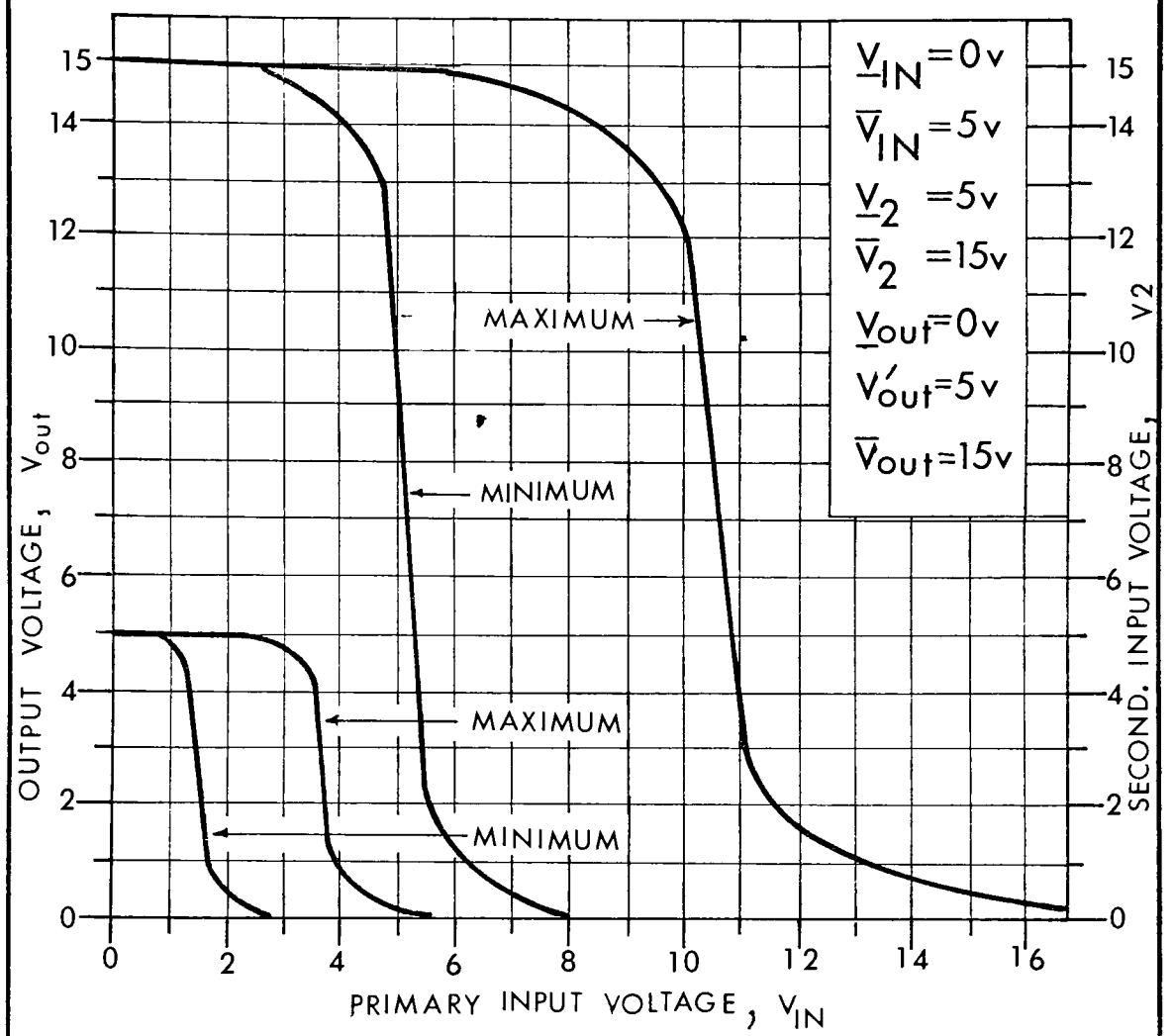
of transforming the basic CMOS gate into a three terminal device. Its voltage transfer characteristics, redefined from the NAND gate in Figure 17., is presented in Figure 20 along with a list of symbol definitions.

The purpose of using the three terminal gate is to; (1) Sensitize the set of primary input variables such that all primary input combinations can be utilized in the detection of internal gate faults, (2) to detect out-of-tolerance changes in the threshold level of the gate, (3) to propagate to the output any faults and normal gate functions in a dynamic operating mode, and (4) to self-diagnose faults occurring at the gate's terminals.

TERNARY LOGIC

The nature of a fault state can be viewed as a third value (N) different from 0 and 1, representing the condition that a faulty input, output, or internal value has occurred. The fail-safe gate with this property of ternary (i.e. 0, 1, N) inputs should be able to produce ternary outputs such that all failure modes produce a 0→N or 1→N output. Conversely, the gate should not produce a failure such that a 0→1 or 1→0 change at the output.

Takaoka and Mine [7] first proposed a fail-safe system based on ternary inputs and outputs which they called the N-Fail-Safe (NFS) system. They showed that any switching function could be realized by a NFS system, such that



Maximum & Minimum Voltage Transfer Characteristics of a Typical Three Terminal Gate with Plots for a Secondary Input, V_2, of 5vdc & 15vdc.

FIGURE 20

output failures are $0 \rightarrow N$ or $1 \rightarrow N$ (neither $1 \rightarrow 0$ nor $0 \rightarrow 1$) for any input failures $0 \rightarrow N$ or $1 \rightarrow N$. Takaoka and Ibaraki [8] extended the concept to sequential machines. Where the realization of such a machine is based on double-line logic that makes use of dual coding: $0 \leftrightarrow (1,0)$, $1 \leftrightarrow (0,1)$, and $N \leftrightarrow (1,1)$ for inputs and outputs. However logic faults caused by asymmetric failures, $1 \rightarrow 0$, cannot be realized. Also, no consideration for internal failure modes of the binary logic gates were considered and the hardware implementation utilized binary delay elements which can have additional undetectable failure modes as discussed in Appendix H. However, by extending their concept, not only with two-rail logic (discussed in Appendix G), but with the three terminal logic gate it is intended to overcome these basic short comings.

SELF-CHECKING

In order for a fault to be detectable, it is not necessary to be able to propagate the fault's occurrance to some observable output. It is only necessary for the fault to interrupt the normal behavior at the output of the failed gate. It is this interruption in normal operation that will be propagated to some observable output, independent of the location, type of fault, or quantity of faults within the network. The self-check is composed of a periodic signal applied to the secondary, V_2, input of the

three terminal gate. By keeping the primary input from having to perform testing on the gate we will be able to accomplish the following: (1) Isolate all faults to the gate level, (2) provide separate outputs for normal and failure modes of operation, (3) prevent the dependence on external hardware to propagate a fault to the circuit's output for detection, (4) provide the capability to thoroughly test for all internal faults, and (5) provide the capability for continuous checking of all gates.

In a normally functioning circuit, signals whose logical value varies in time with some predictable behavior can be generated and applied to the secondary input of the three terminal gate. During normal operation the signal has a waveform as shown in Figure 21. In addition to previously discussed failure modes, variations in T_{ON} and T_{OFF}, due to some additional failure, will alter the duty cycle (T_{ON}/T_{PERIOD}). Circuits designed to detect errors in periodic signals have used the method of forcing an erroneous signal into the circuit and observing the output. This requires the capability of interrupting normal operation to perform the test. The concept of "Self-Checking" introduced by Carter and Schneider [9] will be applied to the three-terminal gate. We can define the three-terminal gate as a self-checking logic gate for a primary input set of variables, A, a secondary (periodic) input set of variables, N, and a fault set of variables, F, if each fault in F causes a non-cyclic output

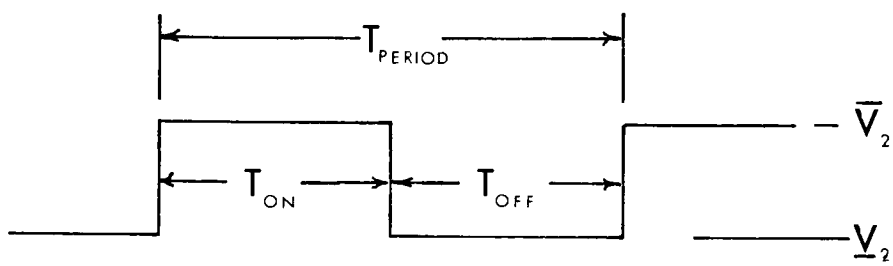


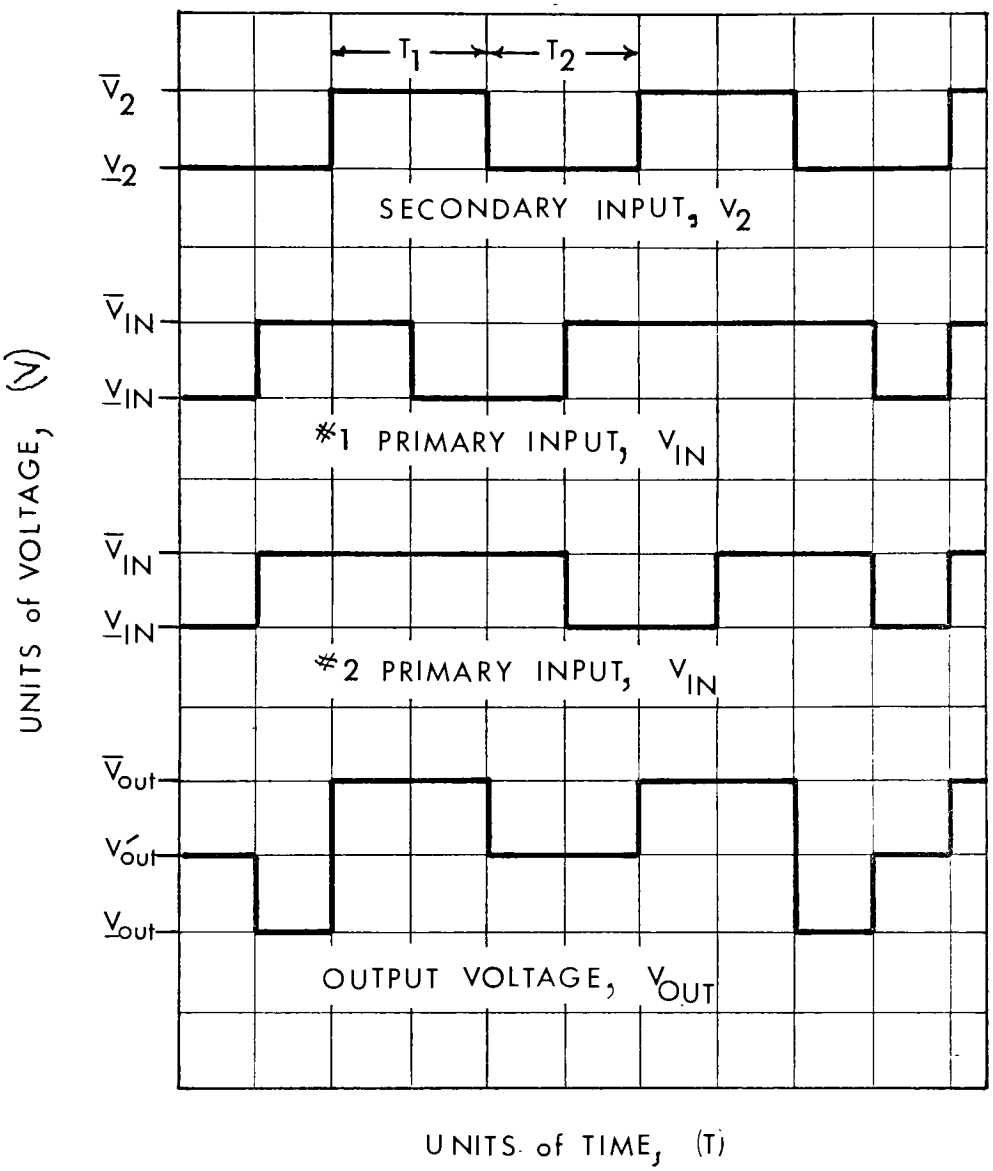
FIGURE 21 Secondary Input Signal of the Three Terminal Gate.

for some input in A and N. Self-checking is necessary to insure that all conditions for single and multiple faults that may occur will be detectable. Hence, if we take A to be a set of primary inputs applied for at least one period that N is applied, then no fault in F should cause an undetectable error during normal operation and the device is a totally self-checking logic gate.

The input and output waveforms of the three-terminal gate during normal operation is illustrated in Figure 22, and Table 4 is a modified truth table showing both the logic states for all inputs and outputs as well as the normal states of all internal semiconductors. The symbols used denote the applied conditions as illustrated in Figure 19. These waveforms illustrate the ternary output states; $\underline{V}_{OUT}$, $\bar{V}_{OUT}$, $\not{V}_{OUT}$, and the ternary input states; $\bar{V}_{IN}$, $\underline{V}_{IN}$, and V_2. The truth table shows the internal state variations with the application of V_2. For example, when A and B are set to $\bar{V}_{IN}$ and V_2 changes state, all four semiconductors change states in a complementary manner. Therefore, the ternary inputs and outputs and complementary cycling provide self-checking at the gate level.

DYNAMIC OUTPUT

The ability of a gate to remain in a dynamic state is an indication that it is functioning properly. Upon failure the gate should not enter into a state or sequence



Input & Output Waveforms of the Three Terminal Gate.

FIGURE 22

TABLE 4

TRUTH TABLE OF THE THREE-TERMINAL GATE

SHOWN IN FIGURE 19

PRIMARY INPUTS		SECONDARY INPUT	OUTPUT	INTERNAL STATES			
A	B	V_2	V_{OUT}	Q1	Q2	Q3	Q4
$\bar{V}_{IN}$	$\bar{V}_{IN}$	$\underline{V}_2$	$\underline{V}_{OUT}$	OFF	OFF	ON	ON
		$\bar{V}_2$	$\bar{V}_{OUT}$	ON	ON	OFF	OFF
$\underline{V}_{IN}$	$\bar{V}_{IN}$	$\underline{V}_2$	V'_{OUT}	ON	OFF	ON	OFF
		$\bar{V}_2$	$\bar{V}_{OUT}$	ON	ON	OFF	OFF
$\underline{V}_{IN}$	$\underline{V}_{IN}$	$\underline{V}_2$	V'_{OUT}	ON	ON	OFF	OFF
		$\bar{V}_2$	$\bar{V}_{OUT}$	ON	ON	OFF	OFF
$\bar{V}_{IN}$	$\underline{V}_{IN}$	$\underline{V}_2$	V'_{OUT}	OFF	ON	OFF	ON
		$\bar{V}_2$	$\bar{V}_{OUT}$	ON	ON	OFF	OFF

of states that are not detectable. Thus, fail-safe logic should assure a safe-side output upon failure. For example, consider a traffic controller with red and green lights. The green light denotes a safe state or go and the red light denotes a dangerous state or stop. When the system fails the controller should show the red light regardless of the actual situation on the road. If the failed traffic controller shows a green light or no light while the actual situation on the road is dangerous, then an accident may occur. Many fail-safe systems [10] [11] , have the undesirable characteristic that component failures must be assumed to be one way, i.e., they all fail to either a S-@-0 or S-@-1 fault but not both. In utilizing the three-terminal gate, we will attempt to be fail-safe for both S-@-1 and S-@-0 failure modes.

We have discussed that by applying the most sensitive input pattern to a NAND gate (1, 1), any stuck-at fault will alter the gate's output for some categories of permanent faults. If we then apply a non-sensitive input pattern to the NAND gate (0, 0) the combination of both input patterns will cause the output to vary so as to detect the stuck-at faults of the gate. Therefore, by complementing the input pattern to the gate, the change or lack of change at the output is a method of detecting internal failures and logic faults at the gate. The ability of fail-safe logic to produce a dynamic output is a measure of its

failure mode and an important characteristic of such logic. When the output ceases to be dynamic, it will remain in either the 1 or 0 state and this change to a static state is an indication of a safe failure. By applying this method to all gates, single and multiple faults can be detected and will not be masked by the propagation of one failed gate through another to the output of the circuit. We have discussed the ability of a three-terminal gate to produce a ternary output. By connecting multiple three-terminal gates in a complementary arrangement (fail-safe gate), it is possible to produce a dynamic output for fault detection.

COMPLEMENTATION

The nature of complementation is discussed in detail in the analysis of the fail-safe gate (later chapter). The purpose now is to illustrate that the limitations of the three-terminal gate will require such a method to resolve its inherent difficulties.

An analysis of particular internal failures is illustrated in Table 5. Item 1 of the table shows for Q1 being S-@-1 for the input conditions: $\bar{V}_{IN}$ (A and B), and $\underline{V}_2$, the output state will be $\underline{V}_{OUT}$. Comparison to the normal output state (Table 4), for the same input states, shows the output is identical. This indicates that the fault is undetectable. Also, examining Figure 19 for all

TABLE 5

ILLUSTRATION OF INTERNAL FAULTS OF THE THREE-TERMINAL GATE OF FIGURE 19

ITEM	PRIMARY INPUTS		SECONDARY INPUTS	INTERNAL STATES				OUTPUT	CONDITION
	A	B	V_2	Q1	Q2	Q3	Q4		
1	$\bar{V}_{IN}$	$\bar{V}_{IN}$	$\underline{V}_2$	**ON**	OFF	ON	ON	$\underline{V}_{OUT}$	Q1: S-@-1
2	$\bar{V}_{IN}$	$\bar{V}_{IN}$	$\bar{V}_2$	ON	ON	**OFF**	OFF	$\bar{V}_{OUT}$	Q3: S-@-0
	$\bar{V}_{IN}$	$\bar{V}_{IN}$	$\underline{V}_2$	OFF	OFF	**OFF**	ON	$\underline{V}_{OUT}$	
3	$\underline{V}_{IN}$	$\underline{V}_{IN}$	$\bar{V}_2$	ON	ON	**OFF**	OFF	$\bar{V}_{OUT}$	Q3: S-@-0
	$\underline{V}_{IN}$	$\underline{V}_{IN}$	$\underline{V}_2$	OFF	OFF	**OFF**	ON	$\underline{V}_{OUT}$	

internal states, as defined for item 1 above, shows that Q1 being S-@-1 causes a short from the V_2, (V_{DD}), terminal to ground, (V_{SS} terminal). Consequently, the three-terminal gate is unable to detect this type of failure. Another type of undetectable failure is shown in items 2 and 3 of Table 5. For these conditions, Q3 is assumed to be S-@-0. Analysis of Figure 19 and Table 4 shows the output to be in the normal (non-failure) state, but during the interval that the secondary input, is low, $\underline{V}_2$, an open-circuit exists within the gate's structure. These two limitations restrict the three-terminal gate's usefulness which can be overcome by using a fail-safe gate configuration (to be presented in a later chapter).

CHAPTER VII

ANALYSIS OF THE THREE TERMINAL GATE

The purpose of this chapter is to analyze the three-terminal gate, as shown in Figure 19 and defined in Table 4, for internal failure modes, logic faults, and failures resulting from changes in its threshold level. The methods discussed in the previous chapter are implemented into the gate's operation and it is intended to show the degree of fault detection obtained by combining them in the manner described herein.

INTERNAL FAILURES

For this analysis the inputs of the three-terminal gate, (A, B), are sequenced through all sets of input variables: 00 01 10 11. The selected sequence is random but the failure modes are assumed to occur before the sequence begins. The types of failures are defined as S-@-0, (ON), or S-@-1, (OFF). This definition assumes all permanent internal failure modes can be represented by a short-circuit or open-circuit of the transistors Q1 through Q4 or a variable resistance, Figure 14, of these transistors.

All possible combinations of open-circuits and/or short-circuit failures (Figure 19) are tabulated in Table 6.

TABLE 6

INTERNAL FAILURE MODES OF THE THREE-TERMINAL GATE

SECONDARY INPUT V_2	FAULT CONDITIONS Q1	Q2	Q3	Q4	OUTPUT SEQ. FOR INPUT SEQ. OF 00	01	10	11
$\underline{V}_2$	OFF	OFF	OFF	OFF	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$	$\underline{V}_0$
$\overline{V}_2$	OFF	OFF	OFF	OFF	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$
$\underline{V}_2$	ON	OFF	OFF	OFF	$\underline{V}_0'$	$\underline{V}_0'$	$\underline{V}_0'$	$*\underline{V}_0'$
$\overline{V}_2$	ON	OFF	OFF	OFF	$\overline{V}_0$	$\overline{V}_0$	$\overline{V}_0$	$\overline{V}_0$
$\underline{V}_2$	ON	ON	OFF	OFF	$\underline{V}_0'$	$\underline{V}_0'$	$\underline{V}_0'$	$*\underline{V}_0'$
$\overline{V}_2$	ON	ON	OFF	OFF	$\overline{V}_0$	$\overline{V}_0$	$\overline{V}_0$	$\overline{V}_0$
$\underline{V}_2$	ON	ON	ON	OFF	$\underline{V}_0'$	$\underline{V}_0'$	$\underline{V}_0'$	$*\underline{V}_0'$
$\overline{V}_2$	ON	ON	ON	OFF	$\overline{V}_0$	$\overline{V}_0$	$\overline{V}_0$	$\overline{V}_0$
$\underline{V}_2$	ON	ON	ON	ON	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$	$\underline{V}_0$
$\overline{V}_2$	ON	ON	ON	ON	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$
$\underline{V}_2$	OFF	ON	ON	ON	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$	$\underline{V}_0$
$\overline{V}_2$	OFF	ON	ON	ON	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$
$\underline{V}_2$	OFF	OFF	ON	ON	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$	$\underline{V}_0$
$\overline{V}_2$	OFF	OFF	ON	ON	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$
$\underline{V}_2$	OFF	OFF	OFF	ON	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$	$\underline{V}_0$
$\overline{V}_2$	OFF	OFF	OFF	ON	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$
$\underline{V}_2$	OFF	ON	OFF	OFF	$\underline{V}_0'$	$\underline{V}_0'$	$\underline{V}_0'$	$*\underline{V}_0'$
$\overline{V}_2$	OFF	ON	OFF	OFF	$\overline{V}_0$	$\overline{V}_0$	$\overline{V}_0$	$\overline{V}_0$
$\underline{V}_2$	OFF	OFF	ON	OFF	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$	$\underline{V}_0$
$\overline{V}_2$	OFF	OFF	ON	OFF	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$

V_2	Q1	Q2	Q3	Q4	00	01	10	11
$\underline{V}_2$	OFF	OFF	OFF	ON	$*\underline{V}_O$	$*\underline{V}_O$	$*\underline{V}_O$	$\underline{V}_O$
$\overline{V}_2$	OFF	OFF	OFF	ON	$*\underline{V}_O$	$*\underline{V}_O$	$*\underline{V}_O$	$*\underline{V}_O$
$\underline{V}_2$	ON	OFF	ON	ON	$*\underline{V}_O$	$*\underline{V}_O$	$*\underline{V}_O$	$\underline{V}_O$
$\overline{V}_2$	ON	OFF	ON	ON	$*\underline{V}_O$	$*\underline{V}_O$	$*\underline{V}_O$	$*\underline{V}_O$
$\underline{V}_2$	ON	ON	OFF	ON	$\underline{V}_O'$	$\underline{V}_O'$	$\underline{V}_O'$	$*\underline{V}_O'$
$\overline{V}_2$	ON	ON	OFF	ON	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$
$\underline{V}_2$	ON	ON	ON	OFF	$\underline{V}_O'$	$\underline{V}_O'$	$\underline{V}_O'$	$*\underline{V}_O'$
$\overline{V}_2$	ON	ON	ON	OFF	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$
$\underline{V}_2$	ON	OFF	OFF	ON	$\underline{V}_O'$	$\underline{V}_O'$	$\underline{V}_O'$	$*\underline{V}_O'$
$\overline{V}_2$	ON	OFF	OFF	ON	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$
$\underline{V}_2$	OFF	ON	ON	OFF	$\underline{V}_O'$	$\underline{V}_O'$	$\underline{V}_O'$	$*\underline{V}_O'$
$\overline{V}_2$	OFF	ON	ON	OFF	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$
$\underline{V}_2$	OFF	OFF	OFF	—	$*\underline{V}_O$	$*\underline{V}_O$	$*\underline{V}_O$	$\underline{V}_O$
$\overline{V}_2$	OFF	OFF	OFF	—	$*\underline{V}_O$	$*\underline{V}_O$	$*\underline{V}_O$	$*\underline{V}_O$
$\underline{V}_2$	ON	OFF	OFF	—	$\underline{V}_O'$	$\underline{V}_O'$	$\underline{V}_O'$	$*\underline{V}_O'$
$\overline{V}_2$	ON	OFF	OFF	—	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$
$\underline{V}_2$	OFF	ON	OFF	—	$\underline{V}_O'$	$\underline{V}_O'$	$\underline{V}_O'$	$*\underline{V}_O'$
$\overline{V}_2$	OFF	ON	OFF	—	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$
$\underline{V}_2$	OFF	OFF	ON	—	$*\underline{V}_O$	$*\underline{V}_O$	$\underline{V}_O'$	$\underline{V}_O$
$\overline{V}_2$	OFF	OFF	ON	—	$*\underline{V}_O$	$*\underline{V}_O$	$*\underline{V}_O$	$*\underline{V}_O$
$\underline{V}_2$	ON	ON	OFF	—	$\underline{V}_O'$	$\underline{V}_O'$	$\underline{V}_O'$	$*\underline{V}_O'$
$\overline{V}_2$	ON	ON	OFF	—	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$
$\underline{V}_2$	OFF	ON	ON	—	$\underline{V}_O'$	$\underline{V}_O'$	$*\underline{V}_O$	$*\underline{V}_O$
$\overline{V}_2$	OFF	ON	ON	—	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$	$\overline{V}_O$

V_2	Q1	Q2	Q3	Q4	00	01	10	11
$\underline{V}_2$	ON	OFF	ON	—	V_o'	V_o'	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	ON	OFF	ON	—	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	ON	ON	ON	—	V_o'	V_o'	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	ON	ON	ON	—	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	OFF	—	OFF	OFF	V_o'	$*\underline{V}_o$	V_o'	$\underline{V}_o$
$\overline{V}_2$	OFF	—	OFF	OFF	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	ON	—	OFF	OFF	V_o'	V_o'	V_o'	$*V_o'$
$\overline{V}_2$	ON	—	OFF	OFF	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	OFF	—	ON	OFF	V_o'	$*\underline{V}_o$	V_o'	$\underline{V}_o$
$\overline{V}_2$	OFF	—	ON	ON	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	OFF	—	OFF	ON	V_o'	$*\underline{V}_o$	V_o'	$\underline{V}_o$
$\overline{V}_2$	OFF	—	OFF	ON	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	ON	—	ON	OFF	V_o'	V_o'	V_o'	$*V_o'$
$\overline{V}_2$	ON	—	ON	OFF	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	OFF	—	ON	ON	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	OFF	—	ON	ON	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$
$\underline{V}_2$	ON	—	OFF	ON	V_o'	V_o'	V_o'	$*V_o'$
$\overline{V}_2$	ON	—	OFF	ON	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	ON	—	ON	ON	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	ON	—	ON	ON	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$	$\underline{V}_o$
$\underline{V}_2$	—	OFF	OFF	OFF	V_o'	V_o'	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	—	OFF	OFF	OFF	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	—	ON	OFF	OFF	V_o'	V_o'	V_o'	$*V_o'$
$\overline{V}_2$	—	ON	OFF	OFF	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$

V_2	Q1	Q2	Q3	Q4	00	01	10	11
$\underline{V}_2$	—	OFF	ON	OFF	V_o'	V_o'	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	—	OFF	ON	OFF	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	—	OFF	OFF	ON	V_o'	V_o'	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	—	OFF	OFF	ON	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	—	ON	ON	OFF	V_o'	V_o'	V_o'	$*V_o'$
$\overline{V}_2$	—	ON	ON	OFF	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	—	OFF	ON	ON	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	—	OFF	ON	ON	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$
$\underline{V}_2$	—	ON	OFF	ON	V_o'	V_o'	V_o'	$*V_o'$
$\overline{V}_2$	—	ON	OFF	ON	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	—	ON	ON	ON	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	—	ON	ON	ON	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$
$\underline{V}_2$	OFF	OFF	—	OFF	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	OFF	OFF	—	OFF	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$
$\underline{V}_2$	ON	OFF	—	OFF	V_o'	V_o'	V_o'	$*V_o'$
$\overline{V}_2$	ON	OFF	—	OFF	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	OFF	ON	—	OFF	V_o'	V_o'	V_o'	$*V_o'$
$\overline{V}_2$	OFF	ON	—	OFF	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	OFF	OFF	—	ON	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	OFF	OFF	—	ON	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$
$\underline{V}_2$	ON	ON	—	OFF	V_o'	V_o'	V_o'	$*V_o'$
$\overline{V}_2$	ON	ON	—	OFF	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	OFF	ON	—	ON	V_o'	$*\underline{V}_o$	V_o'	$\underline{V}_o$
$\overline{V}_2$	OFF	ON	—	ON	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$

V_2	Q1	Q2	Q3	Q4	00	01	10	11
$\underline{V}_2$	ON	OFF	—	ON	V_o'	$^*\underline{V}_o$	V_o'	$\underline{V}_o$
$\overline{V}_2$	ON	OFF	—	ON	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	ON	ON	—	ON	V_o'	$^*\underline{V}_o$	V_o'	$\underline{V}_o$
$\overline{V}_2$	ON	ON	—	ON	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	OFF	OFF	—	—	$^*\underline{V}_o$	$^*\underline{V}_o$	$^*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	OFF	OFF	—	—	$^*\underline{V}_o$	$^*\underline{V}_o$	$^*\underline{V}_o$	$^*\underline{V}_o$
$\underline{V}_2$	ON	ON	—	—	V_o'	V_o'	V_o'	$^{**}\underline{V}_o$
$\overline{V}_2$	ON	ON	—	—	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	ON	OFF	—	—	V_o'	V_o'	V_o'	$^{**}\underline{V}_o$
$\overline{V}_2$	ON	OFF	—	—	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	OFF	ON	—	—	V_o'	V_o'	V_o'	$^{**}\underline{V}_o$
$\overline{V}_2$	OFF	ON	—	—	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	OFF	—	OFF	—	V_o'	$^*\underline{V}_o$	V_o'	$\underline{V}_o$
$\overline{V}_2$	OFF	—	OFF	—	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	ON	—	ON	—	V_o'	V_o'	$^*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	ON	—	ON	—	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	ON	—	OFF	—	V_o'	V_o'	V_o'	$^*V_o'$
$\overline{V}_2$	ON	—	OFF	—	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	OFF	—	ON	—	V_o'	$^*\underline{V}_o$	$\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	OFF	—	ON	—	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	OFF	—	—	OFF	V_o'	$^*\underline{V}_o$	V_o'	$\underline{V}_o$
$\overline{V}_2$	OFF	—	—	OFF	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	ON	—	—	ON	V_o'	$^*\underline{V}_o$	V_o'	$\underline{V}_o$
$\overline{V}_2$	ON	—	—	ON	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$

V_2	Q1	Q2	Q3	Q4	00	01	10	11
$\underline{V}_2$	ON	—	—	OFF	V'_o	V'_o	V'_o	$*V'_o$
$\overline{V}_2$	ON	—	—	OFF	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	OFF	—	—	ON	V'_o	$*\underline{V}_o$	V'_o	$\underline{V}_o$
$\overline{V}_2$	OFF	—	—	ON	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	—	OFF	OFF	—	V'_o	V'_o	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	—	OFF	OFF	—	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	—	ON	ON	—	V'_o	V'_o	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	—	ON	ON	—	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	—	ON	OFF	—	V'_o	V'_o	V'_o	$*V'_o$
$\overline{V}_2$	—	ON	OFF	—	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	—	OFF	ON	—	V'_o	V'_o	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	—	OFF	ON	—	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	—	OFF	—	OFF	V'_o	V'_o	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	—	OFF	—	OFF	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	—	ON	—	ON	V'_o	$*\underline{V}_o$	V'_o	$\underline{V}_o$
$\overline{V}_2$	—	ON	—	ON	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	—	ON	—	OFF	V'_o	V'_o	V'_o	$*V'_o$
$\overline{V}_2$	—	ON	—	OFF	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	—	OFF	—	ON	V'_o	$*\underline{V}_o$	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	—	OFF	—	ON	V_o	V_o	V_o	V_o
$\underline{V}_2$	—	—	OFF	OFF	V'_o	V'_o	V'_o	$**\underline{V}_o$
$\overline{V}_2$	—	—	OFF	OFF	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$	$\overline{V}_o$
$\underline{V}_2$	—	—	ON	ON	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$	$\underline{V}_o$
$\overline{V}_2$	—	—	ON	ON	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$	$*\underline{V}_o$

V_2	Q1	Q2	Q3	Q4	00	01	10	11
$\frac{V_2}{\overline{V}_2}$	—	—	ON	OFF	$\frac{V'_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{**V_o}{\overline{V}_o}$
$\frac{V_2}{\overline{V}_2}$	—	—	OFF	ON	$\frac{V'_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{**V_o}{\overline{V}_o}$
$\frac{V_2}{\overline{V}_2}$	ON	—	—	—	$\frac{V'_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{**V_o}{\overline{V}_o}$
$\frac{V_2}{\overline{V}_2}$	OFF	—	—	—	$\frac{V'_o}{\overline{V}_o}$	$\frac{*V_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{V_o}{\overline{V}_o}$
$\frac{V_2}{\overline{V}_2}$	—	ON	—	—	$\frac{V'_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{**V_o}{\overline{V}_o}$
$\frac{V_2}{\overline{V}_2}$	—	OFF	—	—	$\frac{V'_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{*V_o}{\overline{V}_o}$	$\frac{V_o}{\overline{V}_o}$
$\frac{V_2}{\overline{V}_2}$	—	—	ON	—	$\frac{V'_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{*V_o}{\overline{V}_o}$	$\frac{V_o}{\overline{V}_o}$
$\frac{V_2}{\overline{V}_2}$	—	—	OFF	—	$\frac{V'_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{**V_o}{\overline{V}_o}$
$\frac{V_2}{\overline{V}_2}$	—	—	—	ON	$\frac{V'_o}{\overline{V}_o}$	$\frac{*V_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{V_o}{\overline{V}_o}$
$\frac{V_2}{\overline{V}_2}$	—	—	—	OFF	$\frac{V'_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{V'_o}{\overline{V}_o}$	$\frac{**V_o}{\overline{V}_o}$

The table identifies when the output changes from its nomal value (of Table 4) by the asterisk before the symbol in the output sequence column. By examining Table 6, we can conclude that: (1) all possible combinations of internal stuck-at-faults, except those identified by a double asterisk, can be detected at the output terminal of the three-terminal gate for the specified sequence, (2) the periodic secondary input, V_2, does not contribute significantly to these types of failures, and (3) a particular stuck-at-fault combination may not always be detected for a given set of input variables. We observe that the double asterisk items of Table 6 are open-circuit or short-circuit modes of operation, as seen at the output. However, these failure modes can be detected by the fail-safe gate by the choice of implementation of the three-terminal gate into its structure.

LOGIC FAULTS

Table 7 is a tabulation of all combinations of logic faults that will appear at the terminals of the three-terminal gate. This table indicates that these failure modes may be detected at the gate's output but the secondary input, V_2, does not contribute significantly to their detection.

TABLE 7

TERMINAL FAILURE MODES OF THE

THREE-TERMINAL GATE

SECONDARY INPUT V_2	FAULT CONDITIONS ON INPUT LINES A	B	OUTPUT SEQUENCE FOR INPUT SEQUENCE OF 00	01	10	11
$\underline{V}_2$	S-@-0	NORMAL	V_0'	V_0'	V_0'	$*V_0'$
$\bar{V}_2$	S-@-0	NORMAL	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$
$\underline{V}_2$	S-@-1	NORMAL	V_0'	$*V_0$	V_0'	$\underline{V}_0$
$\bar{V}_2$	S-@-1	NORMAL	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$
$\underline{V}_2$	NORMAL	S-@-0	V_0'	V_0'	V_0'	$*V_0'$
$\bar{V}_2$	NORMAL	S-@-0	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$
$\underline{V}_2$	NORMAL	S-@-1	V_0'	V_0'	$*\underline{V}_0$	$\underline{V}_0$
$\bar{V}_2$	NORMAL	$\bar{S}$-@-1	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$
$\underline{V}_2$	S-@-0	S-@-0	V_0'	V_0'	V_0'	$*V_0'$
$\bar{V}_2$	S-@-0	S-@-0	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$
$\underline{V}_2$	S-@-0	S-@-1	V_0'	V_0'	V_0'	$*V_0'$
$\bar{V}_2$	S-@-0	S-@-1	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$

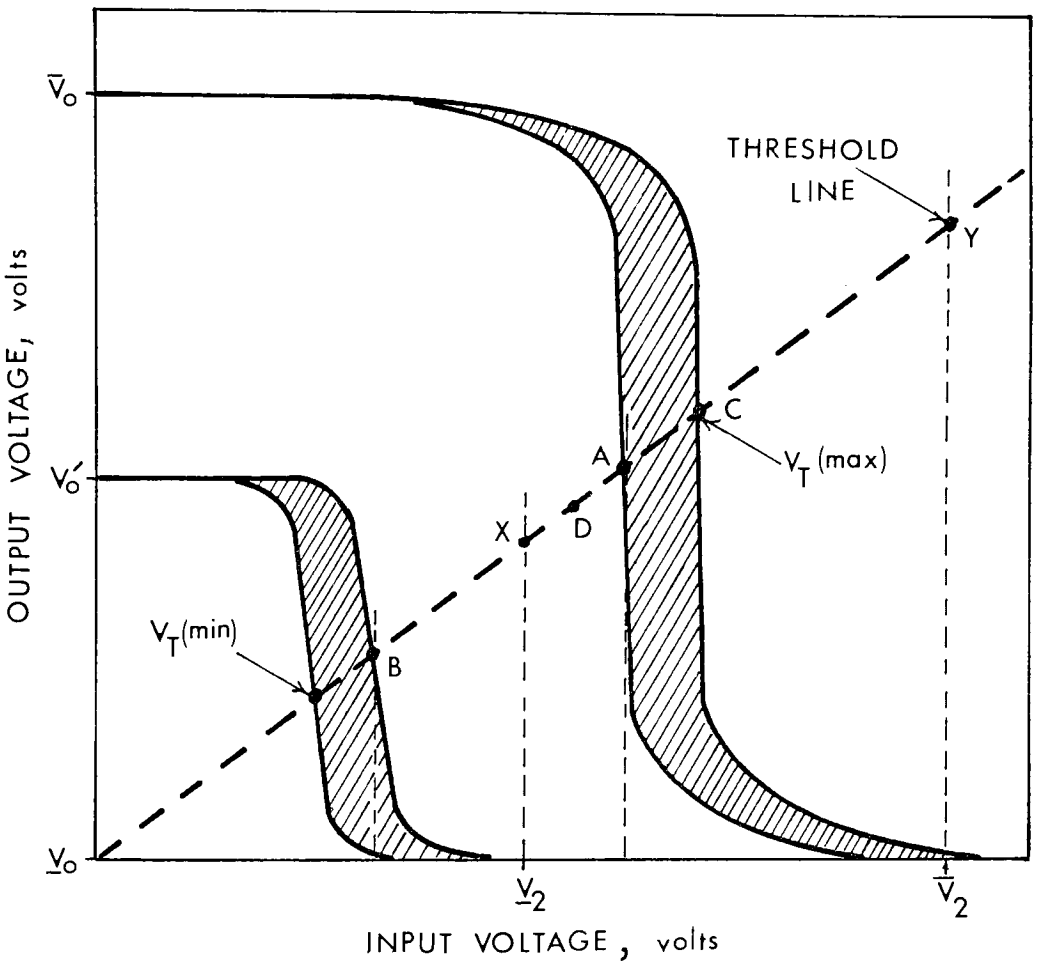
TABLE 7 (cont'd)

SECONDARY INPUT V_2	FAULT CONDITIONS ON INPUT LINES A	B	OUTPUT SEQUENCE FOR INPUT SEQUENCE OF 00	01	10	11
$\underline{V}_2$	S-@-1	S-@-0	V_0'	V_0'	V_0'	$*V_0'$
$\bar{V}_2$	S-@-1	S-@-0	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$
$\underline{V}_2$	S-@-1	S-@-1	$*\underline{V}_0$	$*\underline{V}_0$	$*V_0$	$\underline{V}_0$
$\bar{V}_2$	S-@-1	S-@-1	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$

SECONDARY INPUT V_2	FAULT CONDITIONS ON OUTPUT LINE V_0	OUTPUT SEQUENCE FORE INPUT SEQUENCE OF 00	01	10	11
$\underline{V}_2$	S-@-0	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$	$**\underline{V}_0$
$\bar{V}_2$	S-@-0	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$	$*\underline{V}_0$
$\underline{V}_2$	S-@-1	V_0'	V_0'	V_0'	$*V_0'$
$\bar{V}_2$	S-@-1	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$	$\bar{V}_0$

THRESHOLD FAILURE MODES

The purpose of V_2 is to provide internal transistor complementation for threshold failure modes. Figure 23 is a graphical representation of Figure 20 in which the maximum and minimum threshold levels of the three-terminal gate are illustrated. If internal failures cause the gate's transistors to fail in a mode other than an open-circuit or short-circuit, then these marginal failures may effect the threshold level of the gate by producing a faulty output signal. Referring to Figure 23, it is observed that when the secondary input is low, $\underline{V}_2$, any marginal failures may cause the normal threshold level, (point B), to increase along the threshold line beyond point X. When this occurs the output of the three-terminal gate will change from $\underline{V}_0$ to $\bar{V}_0$ and detect this marginal fault. Likewise, with the secondary input at $\bar{V}_2$ any marginal failures may cause the normal threshold level, (point C), to increase beyond point Y and cause the output to shift from V_0 to $\bar{V}_0$. Also, marginal failures that shift the transfer curve in the opposite direction, (point A decreasing to point X), will result in an output change from $\bar{V}_0$ to $\underline{V}_0$. Faults in the periodic check signal, V_2, could either shift its maximum value, $(\bar{V}_2)$ or minimum value, $(\underline{V}_2)$, which would appear as a marginal fault and result in similar types of detectable outputs. Therefore, the values selected for $\bar{V}_2$, $\underline{V}_2$, and the gate's transfer curve will determine the threshold



Graph of Maximum & Minimum Threshold Levels of the Three Terminal Gate.

FIGURE 23

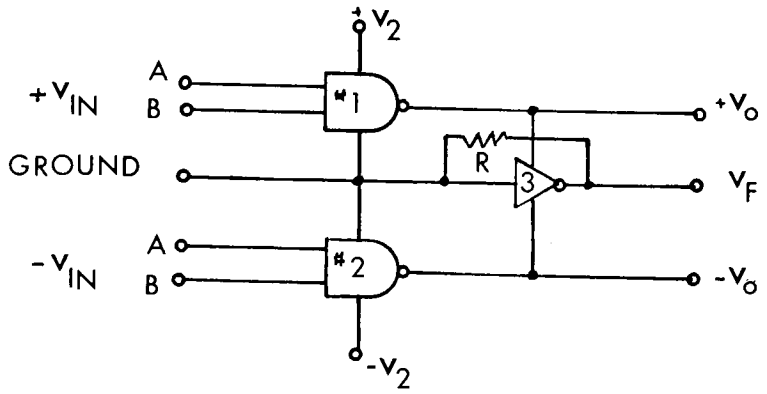
tolerance, i.e., the degree in which a marginal (threshold) fault is detectable. If a marginal fault causes a shift from point A to B, the output may shift enough to be detectable as a logic fault by the following gate. Therefore, self-checking of the periodic secondary input is accomplished by the three-terminal gate as well as threshold detection that exceeds specified tolerances.

CHAPTER VIII

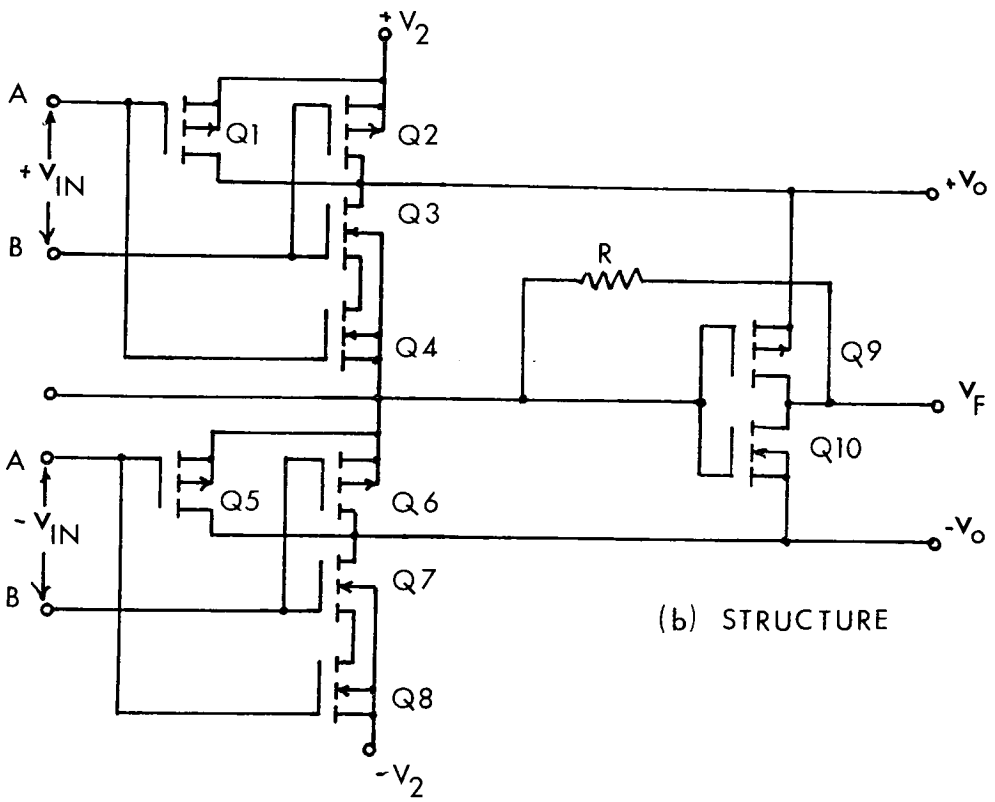
THE FAIL-SAFE LOGIC GATE

The purpose of this chapter is to define and analyze the fail-safe logic gate, F.S.G. The operation of the F.S.G. will illustrate the utilization of the techniques in Chapter VI and resolve the limited detectability of faults in the three-terminal gate. The fail-safe gate can be defined as any multiple-input, dual-output circuit constructed with CMOS logic gates, as shown in Figure 24. The multiple inputs consist of primary lines for processing circuit information as to the gate's failure modes such that a failure will be any detectable transformation of the correct gate function. The fail-safe gate is said to be sensitized for a particular set of primary input variables if a change in output V_F is the result of a fault. Therefore, if any combination of primary input variables is applied to the gate, and the observed output is correct, then no faults exist within the gate. If the output states are incorrect, it will be observed as the complement of its correct value (state) and indicate the presence of a fault or faults.

The fail-safe gate is composed of three-terminal gates; two consisting of two input CMOS NAND gates and one CMOS INVERTER gate, interconnected as shown in Figure 24.



(a) FUNTIONAL DIAGRAM



(b) STRUCTURE

FIGURE 24 THE FAIL SAFE GATE

The relationship of the symbols for the F.S.G. in Figure 24, and the CMOS gate are given in Table 8. The F.S.G. requires the use of positive and negative logic signals as identified in Table 9. The maximum and minimum voltage transfer characteristics of a typical gate with plots for a secondary input, $\pm V_2$, of ± 5 volts and ± 15 volts is shown in Figure 25. Element #1 operates with positive logic: i.e., a low binary state defined as ground reference level. Element #2 operates with negative logic; i.e., a high state defined as being at ground reference level. Element #3 requires both positive and negative logic to provide a continuous dynamic output signal. With the use of positive and negative logic the voltage levels, $\pm V_0$, will never be identical except when failure modes occur at the gate.

The fail-safe gate has a fault output terminal, V_F, which enables detection of failure modes at the gate level. In this manner fault detection is always independent of the normal circuit operation. The element #3 is incorporated into the gate's structure so that it can operate as a dynamic detector. By connecting its input to ground and providing a resistor R between the input and output terminals, the voltage at the fault terminal, V_F, must be greater than or less than a ground level for proper gate operation. This is illustrated in the waveforms in Figure 26. By switching between known states V_F will always be at: $+V_0'$, $-V_0'$, $-V_0$, or $+V_0$ for fault free operation. When V_F produces a

TABLE 8

IDENTIFICATION OF THE INPUT AND OUTPUT TERMINALS FOR THE FAIL-SAFE LOGIC GATE SHOWN IN FIGURE 24

CMOS GATE TERMINALS	FAIL-SAFE GATE TERMINALS		
	ELEMENT #1	ELEMENT #2	ELEMENT #3
V_{DD}	$+V_2$	GROUND	$+V_O$
V_{SS}	GROUND	$-V_2$	$-V_O$
V_{IN}	$+V_{IN}$	$-V_{IN}$	GROUND
V_{OUT}	$+V_O$	$-V_{OUT}$	V_F

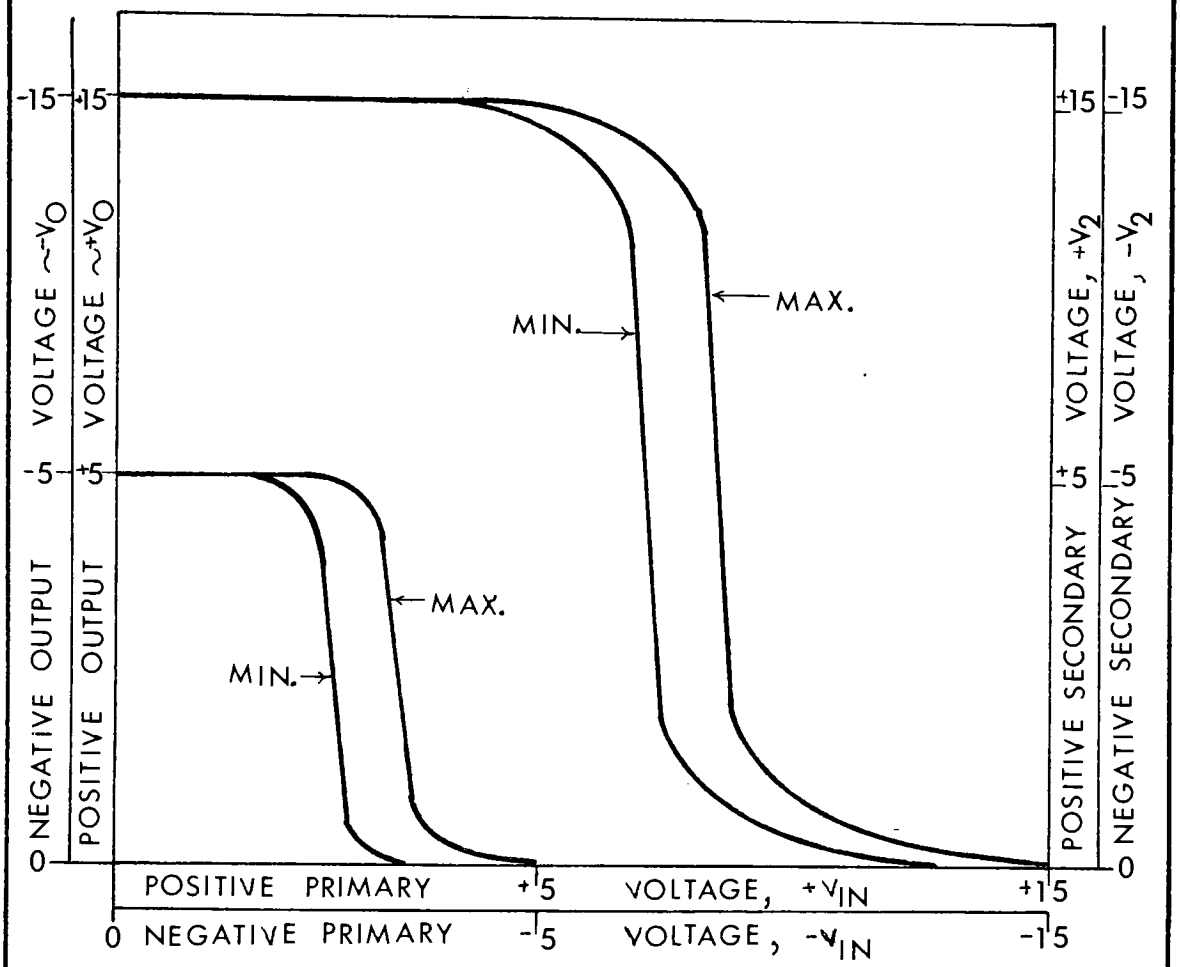
TABLE 9

TRUTH TABLE OF THE FAIL-SAFE GATE

SECONDARY INPUT V_2	PRIMARY INPUTS A	PRIMARY INPUTS B	FAIL-SAFE OUTPUTS V_O	DETECTOR OUTPUT V_F
$+V_2$	$+\bar{V}_{IN}$	$+\bar{V}_{IN}$	$+\underline{V}_O$	
$+\bar{V}_2$	$+\bar{V}_{IN}$	$+\bar{V}_{IN}$	$+\bar{V}_O$	$0 \longrightarrow -V'_O$
$-\underline{V}_2$	$-\bar{V}_{IN}$	$-\bar{V}_{IN}$	$-\underline{V}_O$	
$-\bar{V}_2$	$-\bar{V}_{IN}$	$-\bar{V}_{IN}$	$-V'_O$	
$+\underline{V}_2$	$+\underline{V}_{IN}$	$+\bar{V}_{IN}$	$+V'_O$	
$+\bar{V}_2$	$+\underline{V}_{IN}$	$+\bar{V}_{IN}$	$+\bar{V}_O$	$0 \longrightarrow +V'_O$
$-\underline{V}_2$	$-\underline{V}_{IN}$	$-\bar{V}_{IN}$	$-\underline{V}_O$	
$-\bar{V}_2$	$-\underline{V}_{IN}$	$-\bar{V}_{IN}$	$-\bar{V}_O$	
$+\underline{V}_2$	$+\bar{V}_{IN}$	$+\underline{V}_{IN}$	$+V'_O$	
$+V_2$	$+\bar{V}_{IN}$	$+\underline{V}_{IN}$	$+\bar{V}_O$	$0 \longrightarrow +V'_O$
$-\underline{V}_2$	$-\bar{V}_{IN}$	$-\underline{V}_{IN}$	$-\underline{V}_O$	
$-\bar{V}_2$	$-\bar{V}_{IN}$	$-\underline{V}_{IN}$	$-V_O$	

TABLE 9 (cont'd)

SECONDARY INPUT V_2	PRIMARY INPUTS A	PRIMARY INPUTS B	FAIL-SAFE OUTPUTS V_0	DETECTOR OUTPUT V_F
$+\underline{V}_2$	$+\underline{V}_{IN}$	$+\underline{V}_{IN}$	$+V_0'$	
$+\bar{V}_2$	$+\underline{V}_{IN}$	$+\underline{V}_{IN}$	$+\bar{V}_0$	
				$0 \longrightarrow +V_0'$
$-\underline{V}_2$	$-\underline{V}_{IN}$	$-\underline{V}_{IN}$	$-\underline{V}_0$	
$-\bar{V}_2$	$-\underline{V}_{IN}$	$-\underline{V}_{IN}$	$-\bar{V}_0$	

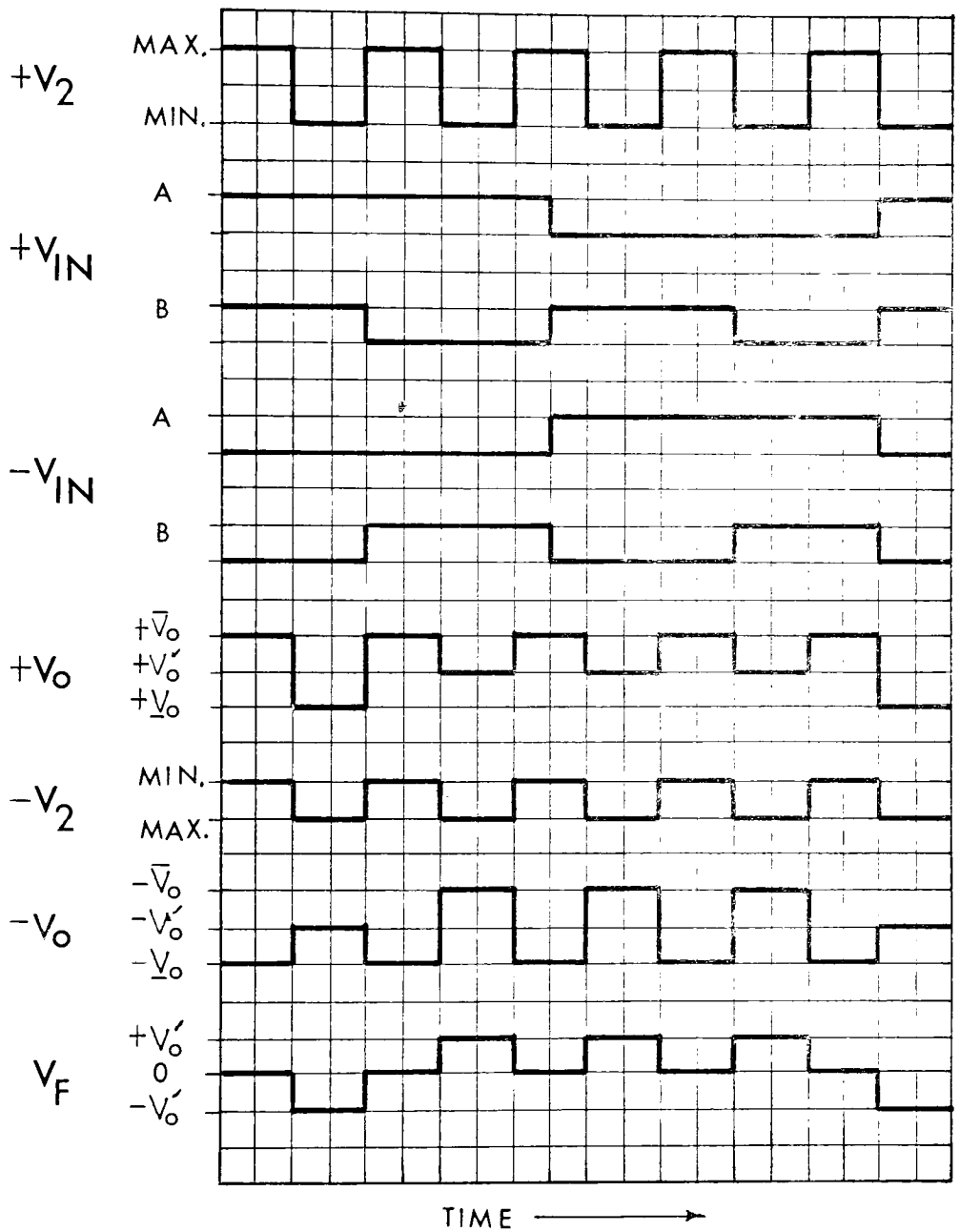


SYMBOL TABLE

$+\underline{V}_{IN} = 0v$	$+\underline{V}_2 = +5v$	$+\underline{V}_o = 0v$	$-\underline{V}_o = -15v$
$+\overline{V}_{IN} = 5v$	$+\overline{V}_2 = +15v$	$+V_o' = +5v$	$-V_o' = -5v$
$-\underline{V}_{IN} = 5v$	$-\underline{V}_2 = -15v$	$+\overline{V}_o = +15v$	$-\overline{V}_o = 0v$
$-\overline{V}_{IN} = 0v$	$-\overline{V}_2 = -5v$		

Voltage Transfer Characteristics of a Typical Fail Safe Gate.

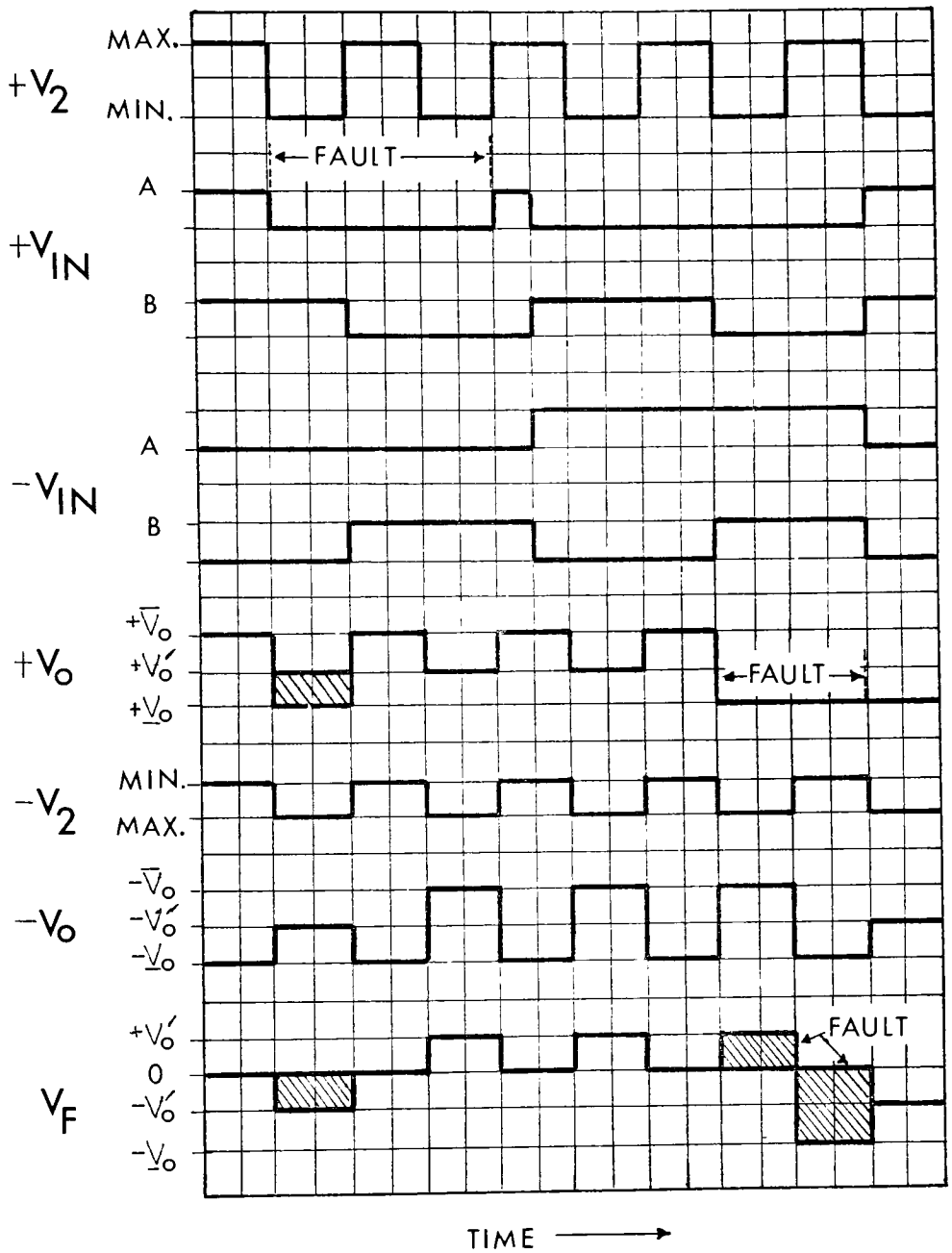
FIGURE 25



(a) Normal Gate-Operation.

Input & Output Waveforms of the Fail-Safe Gate.

FIGURE 26



(b) Gate Operation with Indicated Failures.

FIGURE 26 (continued)

value of $\pm V_0$ or $-\bar{V}_0$ then a fault has occurred within the gate or at its input/output terminals. Failures that occur internal to the gate, but are external to the three elements, (gate interconnections), are also detectable at the fault terminal V_F.

Figure 26b illustrates intermittent (non-permanent) failure modes that have occurred at the A input terminal of element #1 and the $+V_0$ terminal due to an internal failure. The ability to detect these faults are indicated by the variation in voltage level at the fault terminal. This output normally varies between zero and $\pm V'$ and is a function of the gate's transfer characteristics, feedback resistor, and input voltage of the #3 element. To operate, this portion of the fail-safe gate will require component selection to meet specific detection levels at the V_F terminal. If these failure modes were permanent, then the V_F waveform, shown in Figure 26b would be different for each simulated fault.

In reference to the waveforms of Figure 26, the $\pm V_0$ waveforms show ternary levels of $\pm V_0'$, $\pm \bar{V}_0$, and $\pm \underline{V}_0$ for the binary inputs; $\pm \bar{V}_{IN}$ and $\pm \underline{V}_{IN}$, because the example has been idealized for the purpose of illustration. In normal operation only the input gate for a logic network would function with ternary inputs, ($\pm \underline{V}_{IN}$, $\pm V_{IN}'$, and $\pm \bar{V}_{IN}$). Also, the waveforms show that the input state; $+V_{IN}$ or $-V_{IN}$ can occur only when the secondary input, V_2, is at $+V_2$ or $-\underline{V}_2$,

respectively. Therefore, any failure modes that restrict this sequence of operation will be detectable because they will create failures within the gate.

The fail-safe elements, as shown in Figure 24, are three-terminal gates as discussed in previous chapters. The element #1 has been analyzed in Table 6 and 7 of Chapter VII. A similar analysis for element #2 is shown in Table 10 and 11. The structure and truth table for element #3 is shown in Figure 27. Its function is to independently detect all failure modes of the fail-safe gate including faults internal to its own structure. The element should also prevent the masking of multiple gate faults. The device is a three-terminal gate with its primary input, V_{IN}, referenced to ground. Its two secondary inputs, $\pm V_0$, function as identified in Table 8 and Figure 26. By continuously comparing the signals at the secondary input terminals, the #3 element of the fail-safe gate produces a unique dynamic output, V_F, for the normal sets of primary input variables to the fail-safe gate (as shown in Table 9). The output will always maintain this set of voltage levels unless a failure occurs to the fail-safe gate. Table 12 identifies the type of output change produced for specific failure modes. Analysis of the failure modes of element #3 is shown in Table 13, indicating all fault conditions are detectable at the output of this element. Note that an open-circuit or short-circuit failure at either second-

TABLE 10

INTERNAL FAILURE MODES OF THE FAIL-SAFE GATE

SECONDARY INPUT $-V_2$	FAULT CONDITIONS Q5	Q6	Q7	Q8	OUTPUT SEQ. FOR INPUT SEQ. OF 00	01	10	11
$-\underline{V}_2$	OFF	OFF	OFF	OFF	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\bar{V}_2$	OFF	OFF	OFF	OFF	$-\bar{V}_O$	$-\bar{V}_O$	$-\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\underline{V}_2$	ON	OFF	OFF	OFF	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\bar{V}_2$	ON	OFF	OFF	OFF	$-\bar{V}_O$	$-\bar{V}_O$	$-\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\underline{V}_2$	ON	ON	OFF	OFF	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\bar{V}_2$	ON	ON	OFF	OFF	$-\bar{V}_O$	$-\bar{V}_O$	$-\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\underline{V}_2$	ON	ON	ON	OFF	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\bar{V}_2$	ON	ON	ON	OFF	$-\bar{V}_O$	$-\bar{V}_O$	$-\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\underline{V}_2$	ON	ON	ON	ON	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\bar{V}_2$	ON	ON	ON	ON	$-\bar{V}_O$	$-\bar{V}_O$	$-\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\underline{V}_2$	OFF	ON	ON	ON	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\bar{V}_2$	OFF	ON	ON	ON	$-\bar{V}_O$	$-\bar{V}_O$	$-\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\underline{V}_2$	OFF	OFF	ON	ON	$-\underline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$
$-\bar{V}_2$	OFF	OFF	ON	ON	$\overset{*}{-}V'_O$	$\overset{*}{-}V'_O$	$\overset{*}{-}V'_O$	$-V'_O$
$-\underline{V}_2$	OFF	OFF	OFF	ON	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\bar{V}_2$	OFF	OFF	OFF	ON	$-\bar{V}_O$	$-\bar{V}_O$	$-\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\underline{V}_2$	OFF	ON	OFF	OFF	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\bar{V}_2$	OFF	ON	OFF	OFF	$-\bar{V}_O$	$-\bar{V}_O$	$-\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\underline{V}_2$	OFF	OFF	ON	OFF	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$	$\overset{*}{-}\bar{V}_O$
$-\bar{V}_2$	OFF	OFF	ON	OFF	$-\bar{V}_O$	$-\bar{V}_O$	$-\bar{V}_O$	$\overset{*}{-}\bar{V}_O$

$-V_2$	Q5	Q6	Q7	Q8	00	01	10	11
$-\underline{V}_2$	OFF	OFF	OFF	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	OFF	OFF	OFF	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	ON	OFF	ON	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	OFF	ON	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	ON	ON	OFF	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	ON	OFF	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	ON	ON	ON	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	ON	ON	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	ON	OFF	OFF	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	OFF	OFF	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	OFF	ON	ON	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	OFF	ON	ON	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	OFF	OFF	OFF	—	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	OFF	OFF	OFF	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	ON	OFF	OFF	—	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	OFF	OFF	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	OFF	ON	OFF	—	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	OFF	ON	OFF	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	OFF	OFF	ON	—	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$
$-\overline{V}_2$	OFF	OFF	ON	—	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$-\overline{V}_O$
$-\underline{V}_2$	ON	ON	OFF	—	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	ON	OFF	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	OFF	ON	ON	—	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	OFF	ON	ON	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$

$-V_2$	Q5	Q6	Q7	Q8	00	01	10	11
$-\underline{V}_2$	ON	OFF	ON	—	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	OFF	ON	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	ON	ON	ON	—	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	ON	ON	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	OFF	—	OFF	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$-\underline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	OFF	—	OFF	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	ON	—	OFF	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	—	OFF	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	OFF	—	ON	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	OFF	—	ON	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	OFF	—	OFF	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	OFF	—	OFF	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	ON	—	ON	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	—	ON	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	OFF	—	ON	ON	$\overset{*}{-}\overline{V}_O$	$-\underline{V}_O$	$\overset{*}{-}\overline{V}_O$	$-\underline{V}_O$
$-\overline{V}_2$	OFF	—	ON	ON	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$
$-\underline{V}_2$	ON	—	OFF	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	—	OFF	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	ON	—	ON	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	—	ON	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	—	OFF	OFF	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	OFF	OFF	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	—	ON	OFF	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	ON	OFF	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$

$-V_2$	Q5	Q6	Q7	Q8	00	01	10	11
$-\underline{V}_2$	—	OFF	ON	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	OFF	ON	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	—	OFF	OFF	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	OFF	OFF	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	—	ON	ON	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	ON	ON	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	—	OFF	ON	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$
$-\overline{V}_2$	—	OFF	ON	ON	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$-\overline{V}_O$
$-\underline{V}_2$	—	ON	OFF	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	ON	OFF	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	—	ON	ON	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	ON	ON	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	OFF	OFF	—	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	OFF	OFF	—	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	ON	OFF	—	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	OFF	—	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	OFF	ON	—	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	OFF	ON	—	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	OFF	OFF	—	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$
$-\overline{V}_2$	OFF	OFF	—	ON	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$-\overline{V}_O$
$-\underline{V}_2$	ON	ON	—	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	ON	—	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	OFF	ON	—	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	OFF	ON	—	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$

$-V_2$	Q5	Q6	Q7	Q8	00	01	10	11
$-\underline{V}_2$	ON	OFF	—	ON	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\overline{V}_2$	ON	OFF	—	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\underline{V}_2$	ON	ON	—	ON	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\overline{V}_2$	ON	ON	—	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\underline{V}_2$	OFF	OFF	—	—	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$-\underline{V}_O$
$-\overline{V}_2$	OFF	OFF	—	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$-V_O'$
$-\underline{V}_2$	ON	ON	—	—	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\overline{V}_2$	ON	ON	—	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\underline{V}_2$	ON	OFF	—	—	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\overline{V}_2$	ON	OFF	—	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\underline{V}_2$	OFF	ON	—	—	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\overline{V}_2$	OFF	ON	—	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\underline{V}_2$	OFF	—	OFF	—	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\overline{V}_2$	OFF	—	OFF	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\underline{V}_2$	ON	—	ON	—	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\overline{V}_2$	ON	—	ON	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\underline{V}_2$	ON	—	OFF	—	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\overline{V}_2$	ON	—	OFF	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\underline{V}_2$	OFF	—	ON	—	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$-\underline{V}_O$
$-\overline{V}_2$	OFF	—	ON	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$-V_O'$
$-\underline{V}_2$	OFF	—	—	OFF	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\overline{V}_2$	OFF	—	—	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\underline{V}_2$	ON	—	—	ON	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$	$\pm^{*}\overline{V}_O$
$-\overline{V}_2$	ON	—	—	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\pm^{*}\overline{V}_O$

$-V_2$	Q5	Q6	Q7	Q8	00	01	10	11
$-\underline{V}_2$	ON	—	—	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	—	—	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	OFF	—	—	ON	$\overset{*}{-}\overline{V}_O$	$-\underline{V}_O$	$\overset{*}{-}\overline{V}_O$	$-\underline{V}_O$
$-\overline{V}_2$	OFF	—	—	ON	$-\overline{V}_O$	$\overset{*}{-}V'_O$	$-\overline{V}_O$	$-V'_O$
$-\underline{V}_2$	—	OFF	OFF	—	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	OFF	OFF	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	—	ON	ON	—	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	ON	ON	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	—	ON	OFF	—	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	ON	OFF	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	—	OFF	ON	—	$-\underline{V}_O$	$\overset{*}{-}\overline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$
$-\overline{V}_2$	—	OFF	ON	—	$\overset{*}{-}V'_O$	$-\overline{V}_O$	$\overset{*}{-}V'_O$	$-V'_O$
$-\underline{V}_2$	—	OFF	—	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	OFF	—	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	—	ON	—	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	ON	—	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	—	ON	—	OFF	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	ON	—	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	—	OFF	—	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$
$-\overline{V}_2$	—	OFF	—	ON	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}V'_O$	$-V'_O$
$-\underline{V}_2$	—	—	OFF	OFF	$-\underline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	—	OFF	OFF	$\overset{*}{-}V'_O$	$\overset{*}{-}V'_O$	$\overset{*}{-}V'_O$	$-V'_O$
$-\underline{V}_2$	—	—	ON	ON	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$-\underline{V}_O$
$-\overline{V}_2$	—	—	ON	ON	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$-V'_O$

$-V_2$	Q5	Q6	Q7	Q8	00	01	10	11
$-\underline{V}_2$	—	—	ON	OFF	$-\underline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	—	ON	OFF	$\overset{*}{-}V'_O$	$\overset{*}{-}V'_O$	$\overset{*}{-}V'_O$	$-\overline{V}_O$
$-\underline{V}_2$	—	—	OFF	ON	$-\underline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	—	OFF	ON	$\overset{*}{-}V'_O$	$\overset{*}{-}V'_O$	$\overset{*}{-}V'_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	ON	—	—	—	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	ON	—	—	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	OFF	—	—	—	$-\underline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$-\underline{V}_O$
$-\overline{V}_2$	OFF	—	—	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$-V'_O$
$-\underline{V}_2$	—	ON	—	—	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	ON	—	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	—	OFF	—	—	$-\underline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$
$-\overline{V}_2$	—	OFF	—	—	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{**}{-}\overline{V}_O$	$-V'_O$
$-\underline{V}_2$	—	—	ON	—	$-\underline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$
$-\overline{V}_2$	—	—	ON	—	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}V'_O$	$-V'_O$
$-\underline{V}_2$	—	—	OFF	—	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	—	OFF	—	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\underline{V}_2$	—	—	—	ON	$-\underline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$	$-\underline{V}_O$
$-\overline{V}_2$	—	—	—	ON	$-\overline{V}_O$	$\overset{**}{-}\overline{V}_O$	$-\overline{V}_O$	$-V'_O$
$-\underline{V}_2$	—	—	—	OFF	$-\underline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$	$\overset{*}{-}\overline{V}_O$
$-\overline{V}_2$	—	—	—	OFF	$-\overline{V}_O$	$-\overline{V}_O$	$-\overline{V}_O$	$\overset{*}{-}\overline{V}_O$

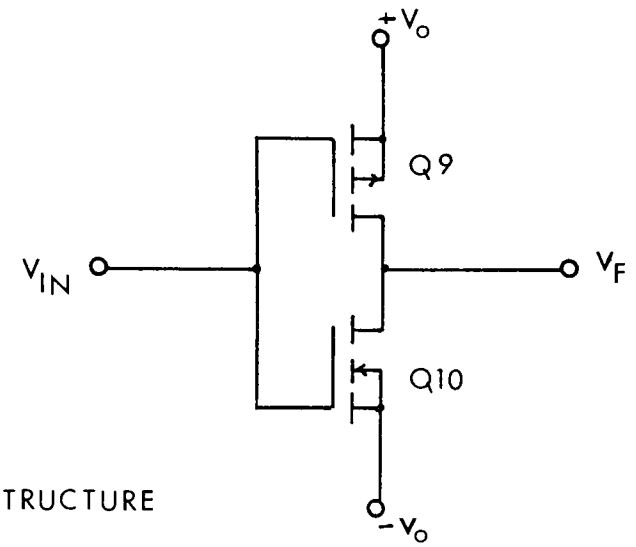
TABLE 11

TERMINAL FAILURE MODES OF THE FAIL-SAFE GATE

SECONDARY INPUT $-V_2$	FAULT CONDITIONS ON INPUT LINES A	B	OUTPUT SEQUENCE FOR INPUT SEQUENCE OF 00	01	10	11
$-\underline{V}_2$	S-@-0	NORMAL	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$
$-\bar{V}_2$	S-@-0	NORMAL	$-\bar{V}_0$	$-\bar{V}_0$	$-\bar{V}_0$	$^{*}-\bar{V}_0$
$-\underline{V}_2$	S-@-1	NORMAL	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$
$-\bar{V}_2$	S-@-1	NORMAL	$-\bar{V}_0$	$^{*}-V_0'$	$-\bar{V}_0$	$-V_0'$
$-\underline{V}_2$	NORMAL	S-@-0	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$
$-\bar{V}_2$	NORMAL	S-@-0	$-\bar{V}_0$	$-\bar{V}_0$	$-\bar{V}_0$	$^{*}-\bar{V}_0$
$-\underline{V}_2$	NORMAL	S-@-1	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$
$-\bar{V}_2$	NORMAL	S-@-1	$-\bar{V}_0$	$-\bar{V}_0$	$^{*}-V_0'$	$-V_0'$
$-\underline{V}_2$	S-@-0	S-@-0	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$
$-\bar{V}_2$	S-@-0	S-@-0	$-\bar{V}_0$	$-\bar{V}_0$	$-\bar{V}_0$	$^{*}-\bar{V}_0$
$-\underline{V}_2$	S-@-0	S-@-1	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$
$-\bar{V}_2$	S-@-0	S-@-1	$-\bar{V}_0$	$-\bar{V}_0$	$-\bar{V}_0$	$^{*}-\bar{V}_0$

TABLE 11 (cont'd)

$-V_2$	A	B	00	01	10	11
$-\underline{V}_2$	S-@-1	S-@-0	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$
$-\bar{V}_2$	S-@-1	S-@-0	$-\bar{V}_0$	$-\bar{V}_0$	$-\bar{V}_0$	$^{*}-\bar{V}_0$
$-\underline{V}_2$	S-@-1	S-@-1	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$
$-\bar{V}_2$	S-@-1	S-@-1	$^{*}-V_0'$	$^{*}-V_0'$	$^{*}-V_0'$	$-V_0'$
	FAULT CONDITIONS ON OUTPUT LINE $-V_0$					
$-\underline{V}_2$	S-@-0		$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$	$-\underline{V}_0$
$-\bar{V}_2$	S-@-0		$^{*}-V_0'$	$^{*}-V_0'$	$^{*}-V_0'$	$^{*}-V_0'$
$-\underline{V}_2$	S-@-1		$^{*}-\bar{V}_0$	$^{*}-\bar{V}_0$	$^{*}-\bar{V}_0$	$^{*}-\bar{V}_0$
$-\bar{V}_2$	S-@-1		$-\bar{V}_0$	$-\bar{V}_0$	$-\bar{V}_0$	$^{*}-\bar{V}_0$



(a) STRUCTURE

V_{IN}	$+V_o$	$-V_o$	$^*V_F$
GND.	$+\bar{V}_o$	$-\underline{V}_o$	V_F
GND.	$+V_o'$	$-\bar{V}_o$	$\bar{V}_F$
GND.	$+\underline{V}_o$	$-V_o'$	$\underline{V}_F$

$^*\underline{V}_F = -V_o'$
$^*V_F = +\underline{V}_o$
$^*\bar{V}_F = +V_o'$

(b) TRUTH TABLE

The Structure & Truth Table of the Element #3.

FIGURE 27

TABLE 12

EXAMPLES OF DETECTABLE FAILURE MODES

OF THE FAIL-SAFE GATE

GATE FAILURE MODE	OUTPUT SIGNAL @ V_F WITH THE PRIMARY INPUT VARIABLES			
	$\bar{\bar{V}}_{IN}\ \bar{\bar{V}}_{IN}$	$\underline{V}_{IN}\ \bar{\bar{V}}_{IN}$	$\bar{\bar{V}}_{IN}\ \underline{V}_{IN}$	$\underline{V}_{IN}\ \underline{V}_{IN}$
NONE	$V_F \rightarrow \underline{V}_F$	$V_F \rightarrow \bar{\bar{V}}_F$	$V_F \rightarrow \bar{\bar{V}}_F$	$V_F \rightarrow \bar{\bar{V}}_F$
$+V_0$: S-@-0	$V_F \rightarrow -\underline{V}_0$	$V_F \rightarrow -\underline{V}_0$	$V_F \rightarrow -\underline{V}_0$	$V_F \rightarrow -\underline{V}_0$
A: S-@-0	$V_F \rightarrow -\bar{\bar{V}}_0$	$V_F \rightarrow \bar{\bar{V}}_F$	$V_F \rightarrow \bar{\bar{V}}_F$	$V_F \rightarrow \bar{\bar{V}}_F$
B: S-@-1	$V_F \rightarrow \underline{V}_F$	$V_F \rightarrow \bar{\bar{V}}_F$	$V_F \rightarrow -\underline{V}_0$	$V_F \rightarrow \bar{\bar{V}}_F$
Q1: S-@-1	$V_F \rightarrow -\underline{V}_0$	$V_F \rightarrow \bar{\bar{V}}_F$	$V_F \rightarrow \bar{\bar{V}}_F$	$V_F \rightarrow \bar{\bar{V}}_F$
Q5: S-@-1	$V_F \rightarrow -\underline{V}_0$	$V_F \rightarrow -\underline{V}_0$	$V_F \rightarrow -\underline{V}_0$	$V_F \rightarrow -\underline{V}_0$
$-V_2$: S-@-0	$V_F \rightarrow -\bar{\bar{V}}_0$	$V_F \rightarrow -\bar{\bar{V}}_0$	$V_F \rightarrow -\bar{\bar{V}}_0$	$V_F \rightarrow -\bar{\bar{V}}_0$

TABLE 13

INTERNAL FAILURE MODES OF THE ELEMENT #3

FAULT CONDITIONS		V_F OUTPUT SEQUENCE FOR F.S.G. INPUT:	
Q9	Q10	$+\bar{\bar{V}}_0 \rightarrow +\underline{V}_0$ $-\underline{V}_0 \rightarrow -V_0'$ AB = 11	$+\bar{\bar{V}}_0 \rightarrow +\underline{V}_0$ $-\underline{V}_0 \rightarrow -\bar{\bar{V}}_0$ AB = 00, 01, 10
ON	ON	$*V_F \rightarrow *V_F$	$*V_F \rightarrow *V_F$
OFF	OFF	$V_F \rightarrow *V_F$	$V_F \rightarrow *V_F$
ON	OFF	$\overset{*}{+}\bar{\bar{V}}_0 \rightarrow *V_F$	$\overset{*}{+}\bar{\bar{V}}_0 \rightarrow \bar{\bar{V}}_F$
OFF	ON	$\overset{*}{-}\underline{V}_0 \rightarrow V_F$	$\overset{*}{-}\underline{V}_0 \rightarrow *V_F$
ON	-	$\overset{*}{+}\bar{\bar{V}}_0 \rightarrow \overset{*}{+}\underline{V}_0$	$\overset{*}{+}\bar{\bar{V}}_0 \rightarrow \bar{\bar{V}}_F$
OFF	-	$\overset{*}{-}\underline{V}_0 \rightarrow \underline{V}_F$	$\overset{*}{-}\underline{V}_0 \rightarrow *V_F$
-	ON	$\overset{*}{-}\underline{V}_0 \rightarrow \underline{V}_F$	$\overset{*}{-}\underline{V}_0 \rightarrow *V_F$
-	OFF	$\overset{*}{+}\bar{\bar{V}}_0 \rightarrow \overset{*}{+}\bar{\bar{V}}_0$	$\overset{*}{+}\bar{\bar{V}}_0 \rightarrow \bar{\bar{V}}_F$

ary terminal is identical to the internal faults of element #1 or #2 that were identified by a double asterisk in Table 6 and 10. Consequently the fail-safe gate detects these types of otherwise undetectable failure modes.

We can conclude that the combination of ternary states, logic complementation, dynamic signals, and two-rail logic provide the means to structure the CMOS logic gate for fault detection. Specifically, the fail-safe gate is capable of detecting single and multiple failure modes that may occur either internally or at the terminals of the gate. All permanent failure modes and intermittent failures that exceed one cycle of the periodic check frequency at V_2 will be detected. By incorporating the element #3 into the fail-safe gate, the method for self-checking at each gate level is accomplished.

CHAPTER IX

RESULTS

The paper has identified and analyzed types of internal failures and logic faults that can effect the normal behavior of digital circuits. By presenting these failures as a composite group of problems that can affect any logic gate, we have accurately identified the objectives of fail-safe logic. This is significant because a thorough review of the literature has shown either a failure to identify all relevant types of failure modes or restriction toward a specific set of logic applications. It is believed that this failure to specifically identify the internal failures of logic gates have made most techniques unacceptable for fail-safe logic.

From the analysis of the various logic families, we have shown that none are acceptable for fail-safe logic. However, by identifying the properties and characteristics of fail-safe logic and the CMOS logic gate, we have been able to identify that it is best suited for fail-safe logic because of the simplicity of its internal structure.

The techniques brought forth in Chapter VI are a significant aspect of this paper. We have shown that by implementing these design techniques, a successful method of pro-

viding fail-safe logic can be achieved. Although the purpose of each technique has been presented, their implementation into the fail-safe gate has identified some short comings. The analysis of the three-terminal gate has shown: (1) Only certain sets of primary input combinations will sensitize the gate for all fault detection, (2) the degree of threshold detection is a function of the gate's transfer characteristics and present technology restricts its use to marginal threshold detection, (3) the implementation of self-checking through the use of second input terminal of the three-terminal gate is a major achievement toward internal fault detection, (4) it is instrumental in isolating faults at the gate level, and (5) it provides the means for dynamic operation. The use of ternary logic would be complicated to implement into a large logic network, i.e., to keep track of all the positive and negative logic levels would compound existing design problems. However, its use provides a positive means to identify a logic fault and allows all normal signals within the network to operate independently of a ground or zero state. The technique of detecting failure modes at the gate level, V_F, resolves the existing problems of gate masking and multiple logic faults but complicates the detection process by the necessity for multiple fault terminals that have to be implemented into an observable output.

The fail-safe gate is shown to be an effective gate

for fail-safe logic. Although implemented to produce complete fault detection, it is somewhat limited by its complex structure. It is possible to reduce its structure if the probability of occurrance of certain types of failures is considered insignificant. However, if the fail-safe gate is considered as a means of implementing the presented techniques, then different fail-safe gate configurations are possible and may prove more effective in complex logic networks.

CHAPTER X

CONCLUSIONS

Although the reliability and fault-tolerance capability of a logic gate can be improved by using reliable components and/or providing redundancy in the circuit, no matter how reliable the components are or how much redundancy has been provided, no component can last forever due to gradual deterioration or physical damage. Thus, it is important to detect faulty components or gates as soon as they occur, so that proper action of rendering the gate or network into a safe mode can be initiated. By designing a circuit as a building block of similar fail-safe gates the detection process is easily implemented and the fault location is determined by a gate self-check. Thus, a combination of internal component detection, complementation, ternary logic states, two-rail logic and continuous self-checking are combined into a method of designing fail-safe logic which utilizes the CMOS gate as its basic element.

The CMOS gate achieves some degree of success when the techniques described herein are applied. The wide tolerance variations exhibited by its transfer characteristics, the limitations of the gate's maximum operating levels, and the inability to predict a known logic state for some

common failure modes limit its fail-safe capabilities. Any digital design would be restricted without a storage element and using the fail-safe gate in combinational logic networks as the only type of logic gate would restrict its usefulness. The concepts of: Dynamic self-checking, three-terminal logic gates, and independent fault detection, prove to be useful techniques for fail-safe logic. The realization of these techniques and the importance of detecting all internal failure modes are the major goals that have been achieved.

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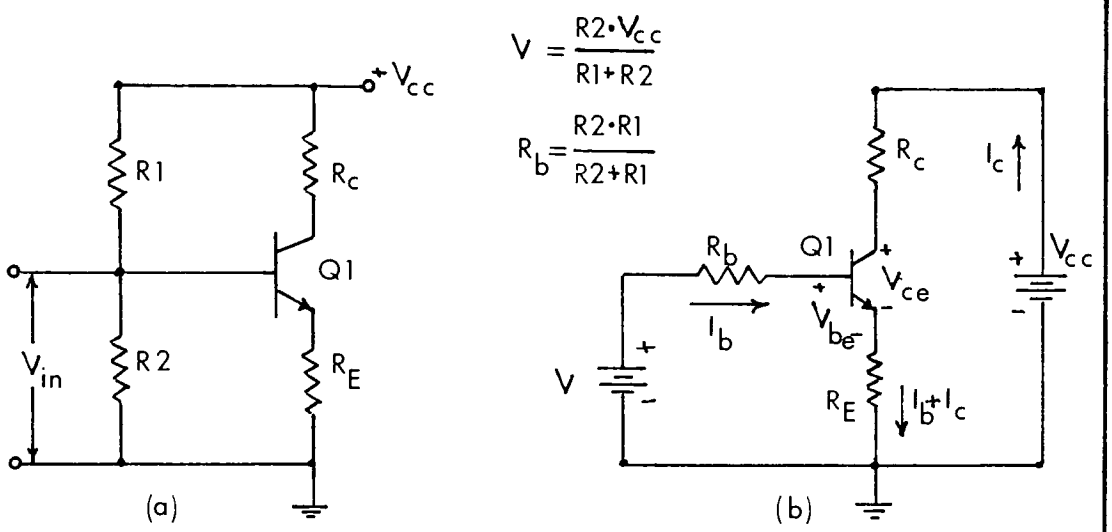
APPENDIX A

EVALUATING THE EFFECTS OF FAILURE MODES BY CALCULATING THE STABILITY AND SENSITIVITY OF A CIRCUIT

STABILITY

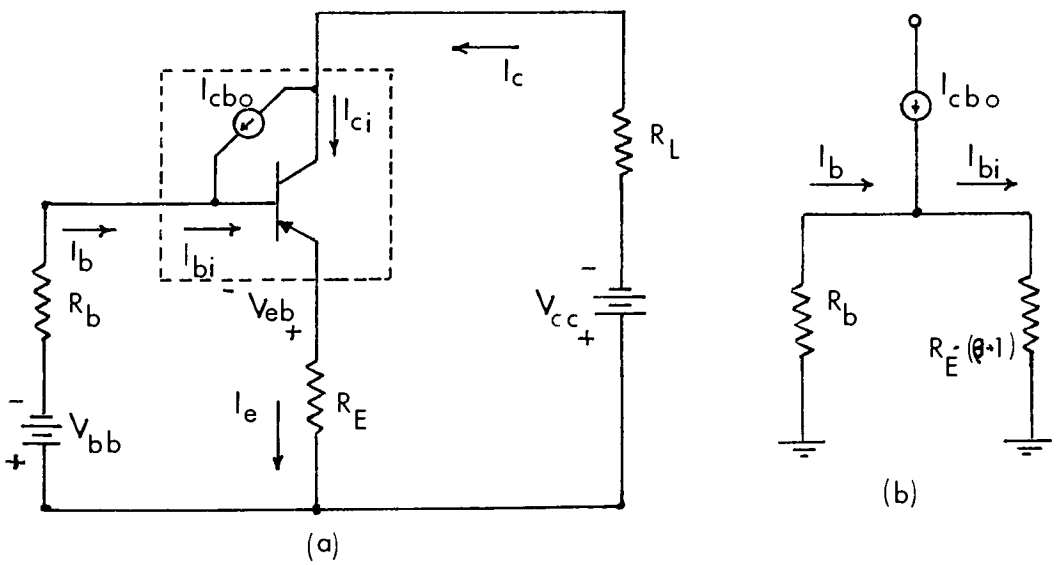
An important cause of transistor failure is thermal instability. The transistor's reverse saturation current, I_{CBO}, changes significantly with temperature. For example, the collector current, I_C, causes the collector junction temperature to rise with increasing I_{CBO}. As a result of this increase in I_{CBO}, I_C, will increase and may further increase the junction temperature and consequently, I_{CBO}. It is possible for this succession of events to become cumulative so that the ratings of the transistor are exceeded and the device burns out. It is possible for a transistor which is biased in the cut-off region to find itself in the active or saturation region as a result of this operating point instability.

Analysis of a simple transistor circuit by examining the rate of change in collector current with respect to I_{CBO} will define the stability of the circuit. The stability will illustrate how failure modes can affect the operation of a circuit. In the active region, Figure A-1, the relation-



(a) Transistor Circuit. (b) Simplification of Base Circuit in (a) by the use of Thevenin's Theorem.

FIGURE A1



(a) PNP Transistor Circuit. (b) Equivalent Circuit of the Leakage Current.

FIGURE A2

ship between I_C and I_B is given by:

$$I_C = (1+\beta) \cdot I_{CBO} + \beta I_B \qquad (A\text{-}1)$$

Definition of stability (S):

$$S = \frac{\partial I_C}{\partial I_{CBO}} \simeq \frac{\Delta I_C}{\Delta I_{CBO}} \qquad (A\text{-}2)$$

Differentiating Eq. A-1 with respect to I_C, consider constant:

$$1 = \frac{1+\beta}{S} + \beta \cdot \frac{dI_B}{dI_C}$$

$$S = \frac{1+\beta}{1 - \beta \cdot (dI_B/dI_C)} \qquad (A\text{-}3)$$

Kirchhoff's Voltage Law around the base circuit:

$$V = I_B \cdot R_B + V_{BE} + R_E \cdot (I_B + I_C) \qquad (A\text{-}4)$$

Differentiating Eq. A-4 and letting V_{BE} be independent of I_C:

$$\frac{dI_B}{dI_C} = -\frac{R_E}{R_E + R_B} \qquad (A\text{-}5)$$

Substitute Eq. A-5 into Eq. A-1, it can be shown that:

$$S = \frac{1 + \beta}{1 + \dfrac{\beta}{\beta \cdot R_E / R_E + R_B}} \qquad \text{(A-6)}$$

From Eq. A-6, it can be seen that if the transistor's beta increased, the stability of the circuit decreases. Also, the smaller the value of R_B, the better will be the stabilization. Therefore, a failure mode in which the value of R_B increases beyond its design tolerance or R_E changes by decreasing in value (or becomes a short-circuit) will cause the circuit to exhibit an increased instability.

SENSITIVITY

Internal component failures are not confined to open or short-circuit conditions only. The variation in component parameters as a function of circuit performance accounts for a significant number of static and transient failures. The output variations of a digital circuit, analyzed as to its sensitivity to component changes will serve to illustrate their effect on creating failure modes.

Analysis of the effect of component failures on the performance of a PNP transistor circuit, Figure A-2, will illustrate the sensitivity of the collector current, I_C, to various component failure modes.

From circuit in Figure A-2:

$$I_C = I_{Ci} + I_{CBO} = I_{Bi} \cdot \beta + I_{CBO} \qquad \text{(A-7)}$$

$$I_{Bi} = I_B + I_{CBO} \qquad \text{(A-8)}$$

$$I_C = \beta \cdot I_B + I_{CBO} \cdot (\beta + 1) \qquad \text{(A-9)}$$

Assuming that V_{EB} is negligible and assumming the voltages about the emitter-base loop:

$$V_{BB} = I_B \cdot R_B + I_E \cdot R_E \qquad \text{(A-10)}$$

AND

$$I_E = I_{Bi} + I_{Ci} = I_{Bi} \cdot (\beta + 1) \qquad \text{(A-11)}$$

$$I_{Bi} = I_B + I_{CBO} \qquad \text{(A-12)}$$

Substitute Eq. A-12 into Eq. A-11:

$$I_E = (\beta + 1) \cdot (I_B + I_{CBO}) \qquad \text{(A-13)}$$

Substitute Eq. A-13 into Eq. A-10:

$$V_{BB} = I_B \cdot R_B + (\beta + 1) \cdot (I_B + I_{CBO}) \cdot R_E \qquad \text{(A-14)}$$

Solve Eq. A-14 for I_B:

$$I_B = \frac{V_{BB} - I_{CBO} \cdot R_E (\beta + 1) - V_{BE}}{R_B + R_E \cdot (\beta + 1)} \qquad \text{(A-15)}$$

Substitute Eq. A-15 into Eq. A-9:

$$I_C = \beta \cdot \frac{V_{BB} - I_{CBO} \cdot R_E \cdot (\beta + 1)}{R_B + R_E \cdot (\beta + 1)} + I_{CBO} \cdot (\beta + 1) \qquad \text{(A-16)}$$

Result:

$$I_C = \frac{\beta \cdot V_{BB}}{R_B + R_E \cdot (\beta + 1)} + \frac{I_{CBO} \cdot (\beta + 1) \cdot (R_E + R_B)}{R_B + R_E \cdot (\beta + 1)} \qquad \text{(A-17)}$$

Definition of sensitivity (S_y^x):

The sensitivity of a quantity (X) with respect to a parameter (Y) is given by:

$$S_y^x = \frac{\partial x/x}{\partial y/y} = \frac{dx}{dy} \cdot \frac{y}{x} \qquad \text{(A-18)}$$

Using the definition for sensitivity, Eq. A-18, and the quantity I_C in Eq. A-17, the sensitivity of I_C with respect to R_B, R_E, and β are as follows:

$$S_{R_B}^{I_C} = \frac{R_B}{R_E + R_B} \cdot \left[1 - \frac{2}{(\beta + 1)} \right] \qquad \text{(A-19)}$$

$$S_{R_E}^{I_C} = \frac{R_E}{R_E + R_B} - \frac{2 \cdot R_E \cdot (\beta + 1)}{R_B + R_E \cdot (\beta + 1)} \qquad \text{(A-20)}$$

$$S_{\beta}^{I_C} = \frac{\beta \cdot R_E}{R_B + R_E \cdot (\beta + 1)} \qquad \text{(A-21)}$$

It can be seen from Eq. A-19 that for the nominal values of: $R_B = 20k\Omega$, $\beta = 20$, $R_E = 1k\Omega$, and $R_C = 2k\Omega$, then (as shown below) a $\pm 20\%$ change in the value of R_B will result in a $\pm 17\%$ change in the current I_C.

From Eq. A-19:

$$S_{R_B}^{I_C} = \frac{20kr}{21kr} \cdot \left[1 - \frac{2}{20 + 1} \right] = 0.862$$

From Eq. A-18:

$$\frac{dI_C}{I_C} = S_{R_B}^{I_C} \cdot \frac{dR_B}{R_B}$$

$$\therefore \frac{dI_C}{I_C} = \Delta I_C = (0.862)\ (+0.20) = 17.2\%$$

Various changes in the tolerances of the circuit's components have been tabulated in Table A-1 as a function of the sensitivity of I_C. These results illustrate the effect of failure modes on the performance of the circuit.

TABLE A-1

SENSITIVITY VS COMPONENT VARIATIONS

FOR THE CIRCUIT IN FIGURE A-2

CHANGE IN COMPONENT VALUE	$S_{R_B}^{I_C} \cdot \Delta R_B$	$S_{R_E}^{I_C} \cdot \Delta R_E$	$S_{\beta}^{I_C} \cdot \Delta \beta$
±20%	±17.2%	±19.5%	±9.8%
±40%	±34.5%	±39.1%	±19.5%
±60%	±51.7%	±58.6%	±29.3%

APPENDIX B

ANALYSIS OF A RTL CIRCUIT

In reference to the circuit in Figure 2:

$$V_O = V_{CC} - 3 \cdot I_B \cdot R_L \qquad \text{(B-1)}$$

WHERE:

$$I_B = \frac{V_O - V_{BE}\ (SAT)}{R_B} \qquad \text{(B-2)}$$

THEREFORE:

$$V_O = V_{CC} - \frac{3 \cdot R_L}{R_B} \cdot (V_O - V_{BE(SAT)}) \qquad \text{(B-3)}$$

RESULTS:

$$V_O = \frac{R_B \cdot V_{CC} + 3 \cdot R_L \cdot V_{BE(SAT)}}{R_B + 3 \cdot R_L} \qquad \text{(B-4)}$$

In reference to Appendix A and Eq. B-4, the sensitivity of V_O to R_B and R_L is:

$$S_{R_B}^{V_O} = 1 - \frac{R_B}{R_B + 3R_L} \quad (\text{FANOUT} = 3) \qquad \text{(B-5)}$$

$$S_{R_L}^{V_O} = 1 - \frac{3 \cdot R_L}{R_B + 3R_L} \quad (\text{FANOUT} = 3) \qquad \text{(B-6)}$$

APPENDIX C

ANALYSIS OF A TTL NAND GATE

Analysis of the gate's internal failure modes is based on the TTL gate in Figure 4. The piecewise analysis of the changes in internal current verses parameter changes will illustrate the potential failure modes of multiple transistor stages in the gate's structure. Using Figure C-1 for the low-level output state and Figure C-2 for the high-level output state, we can determine the sensitivity to component changes as follows:

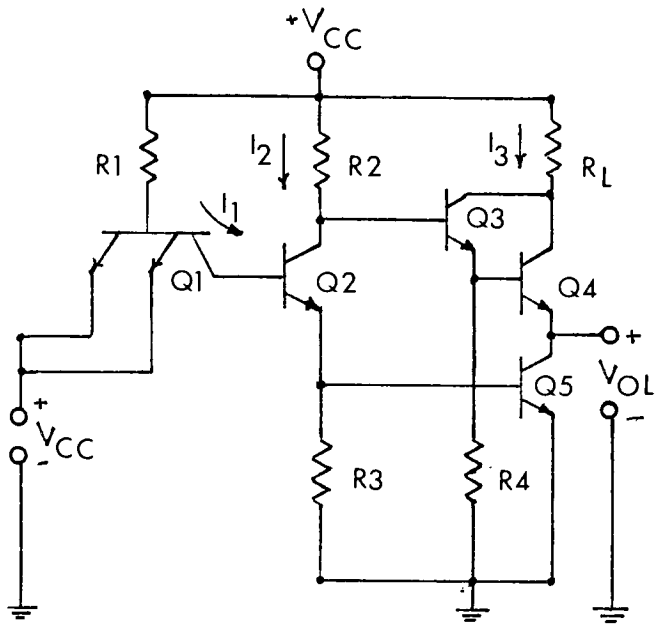
From figure C-1:

$$I_1 = \frac{V_{CC} - V_{BE}(Q1) - V_{BE}(Q2) - V_{BE}(Q5)}{R_1} \qquad (C\text{-}1)$$

$$I_2 = \frac{V_{CC} - V_{CE}(Q2) - V_{BE}(Q5)}{R_2} \qquad (C\text{-}2)$$

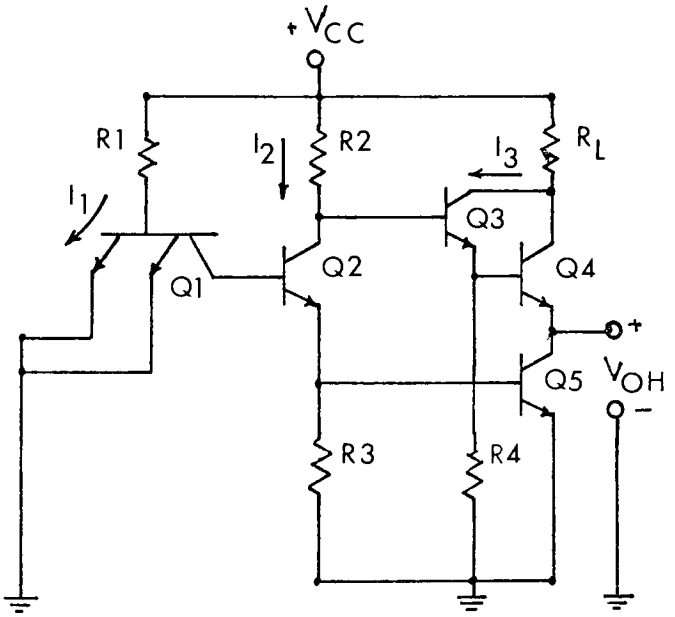
Let $V_{BE}(Q5) = V_{BE}(Q2) = V_{BE}(Q1)$;
The current gain of Q2 is:

$$A_i = \frac{I_2}{I_1} = \frac{V_{CC} - V_{CE}(Q2) - V_{BE}(Q5)}{R_2} \cdot \frac{R_1}{V_{CC}-V_{BE}(Q1)-V_{BE}(Q} \qquad (C\text{-}3)$$



TTL NAND Gate with the Output in a Low State.

FIGURE C1



TTL NAND Gate with the Output in a High State.

FIGURE C2

Simplifying:

$$A_i = \frac{R_1 \cdot (V_{CC} - V_{CE}\ (Q2) - V_{BE})}{R_2 \cdot (V_{CC} - 2V_{BE})} \qquad (C\text{-}3)$$

From Eq. C-3 and Appendix A:

$$S_{R_1}^{A_1} = 1 \ ; \ S_{R_2}^{A_1} = -1$$

From Figure C-2:

$$I_1 = \frac{V_{CC} - V_{BE}\ (Q1)}{R_1} \qquad (C\text{-}4)$$

$$I_2 = \frac{V_{CC} - V_{BE}\ (Q3)}{R_2 + R_4 \cdot (\beta + 1)} \qquad (C\text{-}5)$$

$$I_3 = \frac{V_{CC} - V_{CE}\ (Q3)}{R_L + R_4 / (\beta + R_4)} \qquad (C\text{-}6)$$

The current gain of Q3 is:

$$A_i = \frac{\beta \cdot \left[V_{CC} - V_{CE}\ (Q3)\right] \cdot \left[R_2 + R_4 \cdot (\beta + 1)\right]}{\left[V_{CC} - V_{BE}\ (Q3)\right] \cdot \left[(\beta + 1) \cdot R_4 + R_L\right]} \qquad (C\text{-}7)$$

From Eq. C-7 and Appendix A:

$$S_{R_4}^{A_i} = \frac{R_4 \cdot (\beta + 1)}{R_2 + R_4 \cdot (\beta + 1)} - \frac{R_4 \cdot (\beta + 1)}{\beta \cdot R_L + R_4 \cdot (\beta + 1)}$$

$$S_{R_2}^{A_i} = \frac{R_2}{R_2 + R_4 \cdot (\beta + 1)}$$

$$S^{A_i} = 1$$

$$S_{R_L}^{A_i} = 1$$

APPENDIX D

ANALYSIS OF A ECL GATE

Analysis of the gate's internal failure modes is based on the ECL gate in Figure 5.[12] We can determine the sensitivity to component changes as follows:

Current I_1 is:

$$I_1 = \frac{V_{EE} - \left[V_{BB} + V_{BE}\ (Q5)\right]}{R_2} \qquad \text{(D-1)}$$

When all gate inputs equal logic zero, thus transistors Q_1 through Q_4 will be in cutoff.

The voltage drop at the collector of Q5 is:

$$V_{R_4} = I_1 \cdot R_4 + I_{B_1} \cdot R_4 \qquad \text{(D-2)}$$

The OR output is:

$$V_{OR} = V_{R_4} + V_{BE}\ (Q8) \qquad \text{(D-3)}$$

Therefore:

$$V_{OR} = R_4 \cdot \frac{V_{EE} - \left[V_{BB} + V_{BE}\ (Q5)\right]}{R_2} + I_{B_1} \cdot R_4 + V_{BE}(Q8) \qquad \text{(D-4)}$$

From Eq. D-4 and Appendix A:

$$S_{R_4}^{V_{OR}} = 2 \; ; \qquad S_{R_2}^{V_{OR}} = -1$$

Current I_1 is:

$$I_1 = \frac{V_{EE} - \left[V_{IN} - V_{BE}\ (Q5)\right]}{R_2} \qquad \text{(D-5)}$$

When one or more of the gate inputs are at a logic one level.

The voltage drop at the collector of Q5 is:

$$V_{R_3} \simeq I_1 \cdot R_3 + I_{B_2} \cdot R_3 \qquad \text{(D-6)}$$

And the NOR output is:

$$V_{NOR} = V_{R_3} + V_{BE}\ (Q7) \qquad \text{(D-7)}$$

Therefore:

$$V_{NOR} = R_3 \cdot \frac{V_{EE} - \left[V_{IN} - V_{BE(Q5)}\right]}{R_2} + I_{B_3} \cdot R_3 + V_{BE(Q7)} \qquad \text{(D-8)}$$

From Eq. D-8 and Appendix A:

$$S_{R_3}^{V_{NOR}} = +2 \; ; \quad S_{R_2}^{V_{NOR}} = -1$$

Let V_{BE} of Q1 through Q8 be equal, $V_{R1} = V_{R2} = V_F$

Taking loop equations of the bias supply circuit, the threshold voltage, V_{BB}, is:

$$V_{BB} = \frac{R_5 \cdot R_6 \cdot \beta \cdot \left[V_{EE} - V_{BE(Q6)} - 2V_F\right] + R_5 \cdot R_6 \cdot \left[V_{EE} - V_{BE} - 2V_F\right]}{\beta \cdot \left[R_5 \cdot R_6 + R_7 \cdot R_6\right]} -$$

$$\frac{R_7 \cdot R_6 \cdot \quad \cdot V_{BE} - R_7 \cdot R_6 \cdot V_{BE} + R_5 \cdot R_7 \cdot V_{EE}}{R_5 \cdot R_7 + R_7 \cdot R_6 + R_5 \cdot R_6} \qquad \text{(D-9)}$$

APPENDIX E

ANALYSIS OF A RTL GATE USING THE NEWTON-RAPHSON METHOD

Diode equation:

$$I = I_o \cdot \left[\varepsilon^{QV_{BE}/nKT} - 1 \right] \qquad \text{(E-1)}$$

Where I_o is proportional to $T^{3/2} \cdot \varepsilon^{-QVg/nKT}$

Using the following values to plot curve E-1.

$T_1 = 200°K$

$T_2 = 300°K$

$T_3 = 400°K$

I_o @ 300°K = 10nANOAMPERES

n = 2 for silicon

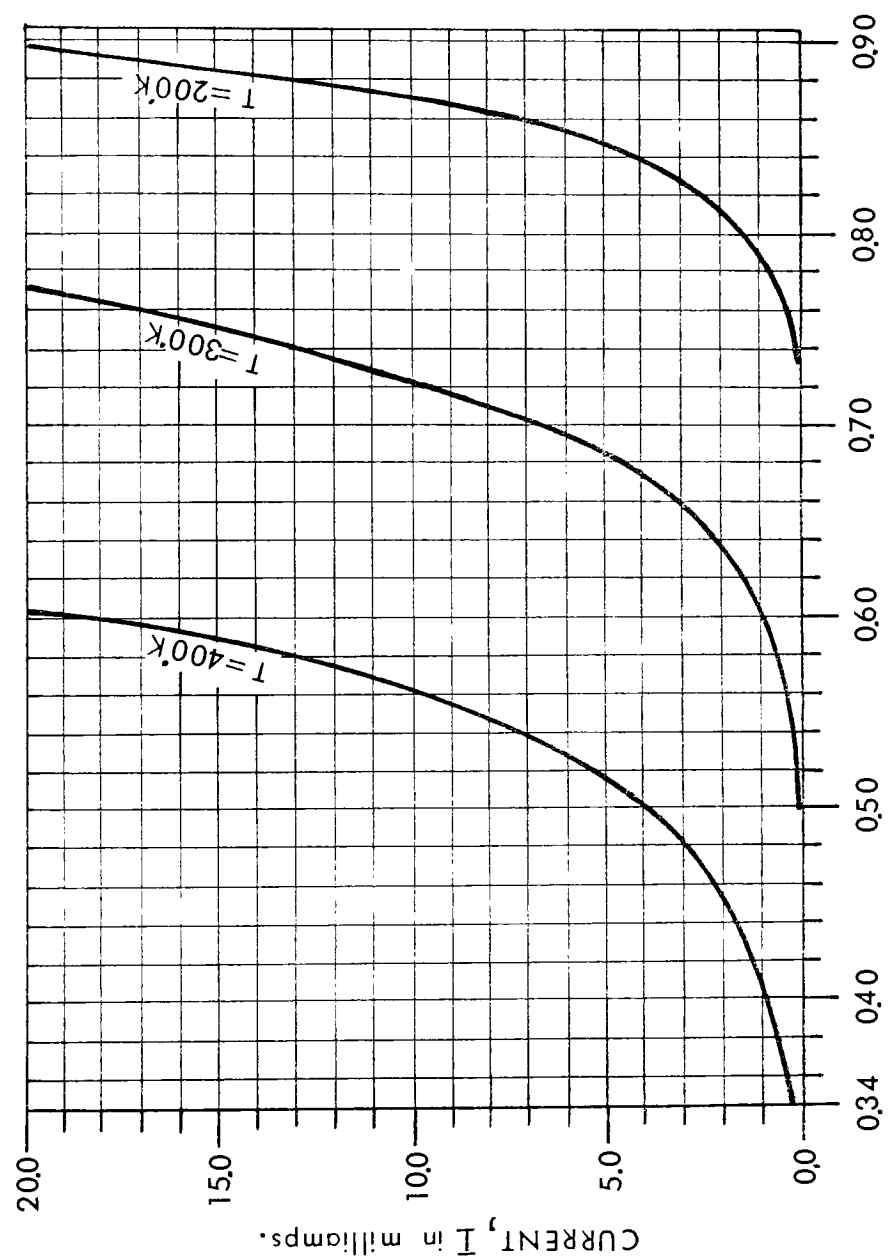
V_G = 1.1 volt at room temperature (300°K)

$Q = 1.602 \times 10^{-19}$

$k = 1.38 \times 10^{-23}$

Taking loop equations of the circuit in Figure 6:

$$V_{IN} = R_B \cdot I_B + V_{BE} \qquad \text{(E-2)}$$



CURVE E1

Silicon P-N Junction Diode I-V Characteristics.

Using the Ebers-Moll transistor model:

$$I_C = \frac{\alpha_n \cdot I_{EO}\left[\varepsilon^{V_{BE}/nV_Q} - 1\right]}{1 - \alpha_n \alpha_I} - \frac{I_{CO}\cdot\left[\varepsilon^{V_C/nV_Q} - 1\right]}{1 - \alpha_n \alpha_I} \qquad \text{(E-3)}$$

$$I_E = \frac{\alpha_I \cdot I_{CO}\left[\varepsilon^{V_C/nV_Q} - 1\right]}{1 - \alpha_n \alpha_I} - \frac{I_{EO}\cdot\left[\varepsilon^{V_{BE}/nV_Q} - 1\right]}{1 - \alpha_n \alpha_I} \qquad \text{(E-4)}$$

$$I_B = -\left[I_C + I_E\right] \qquad \text{(E-5)}$$

Therefore:

$$I_B = I_{CO}\left[\varepsilon^{V_C/nV_Q} - 1\right] - \alpha_n I_{EO}\left[\varepsilon^{V_{BE}/nV_Q} - 1\right] + I_{EO}\cdot \left[\varepsilon^{V_{BE}/nV_Q} - 1\right] - \alpha_n I_{CO}\left[\varepsilon^{V_C/nV_Q} - 1\right] \Big/ 1 - \alpha_n \alpha_I \qquad \text{(E-6)}$$

And the input voltage is:

$$V_{IN} = V_{BE} + R_B\left[I_{CO}\left(\varepsilon^{V_C/nV_Q} - 1\right) - \alpha_n I_{EO}\left(\varepsilon^{V_{BE}/nV_Q} - 1\right) + I_{EO}\left(\varepsilon^{V_{BE}/nV_Q} - 1\right) - \alpha_I I_{CO}\left(\varepsilon^{V_C/nV_Q} - 1\right) \Big/ 1 - \alpha_n \alpha_I\right] \qquad \text{(E-7)}$$

The output voltage is:

$$V_O = V_{CC} - R_L I_C = V_{BE} - V_C = V_{CE}$$

$$V_O = V_{CC} - R_L\left[\frac{\alpha_n I_{EO}\left(\varepsilon^{V_{BE}/nV_Q} - 1\right) - I_{CO}\left(\varepsilon^{V_C/nV_Q} - 1\right)}{1 - \alpha_n \alpha_I}\right] \qquad \text{(E-8)}$$

The following values are specified as for curve 3, 4, and 5:

I_{CO} = 0.1298 X 10^{-9} (200°K); 10 X 10^{-9} (300°K);
3,14 X 10^{-6} (400°K);

I_{EO} = 0.0655 X 10^{-12} (200°K); 5 X 10^{-9} (300°K);
1.5858 X 10^{-6} (400°K)

α_n = 0.99 α_I = 0.50 (300°K)

V_Q = .026 volts (300°K)

η = 2 (silicon)

V_{CC} = 3.6 volts

R_B = 450 ohms R_L = 640 ohms

APPENDIX F

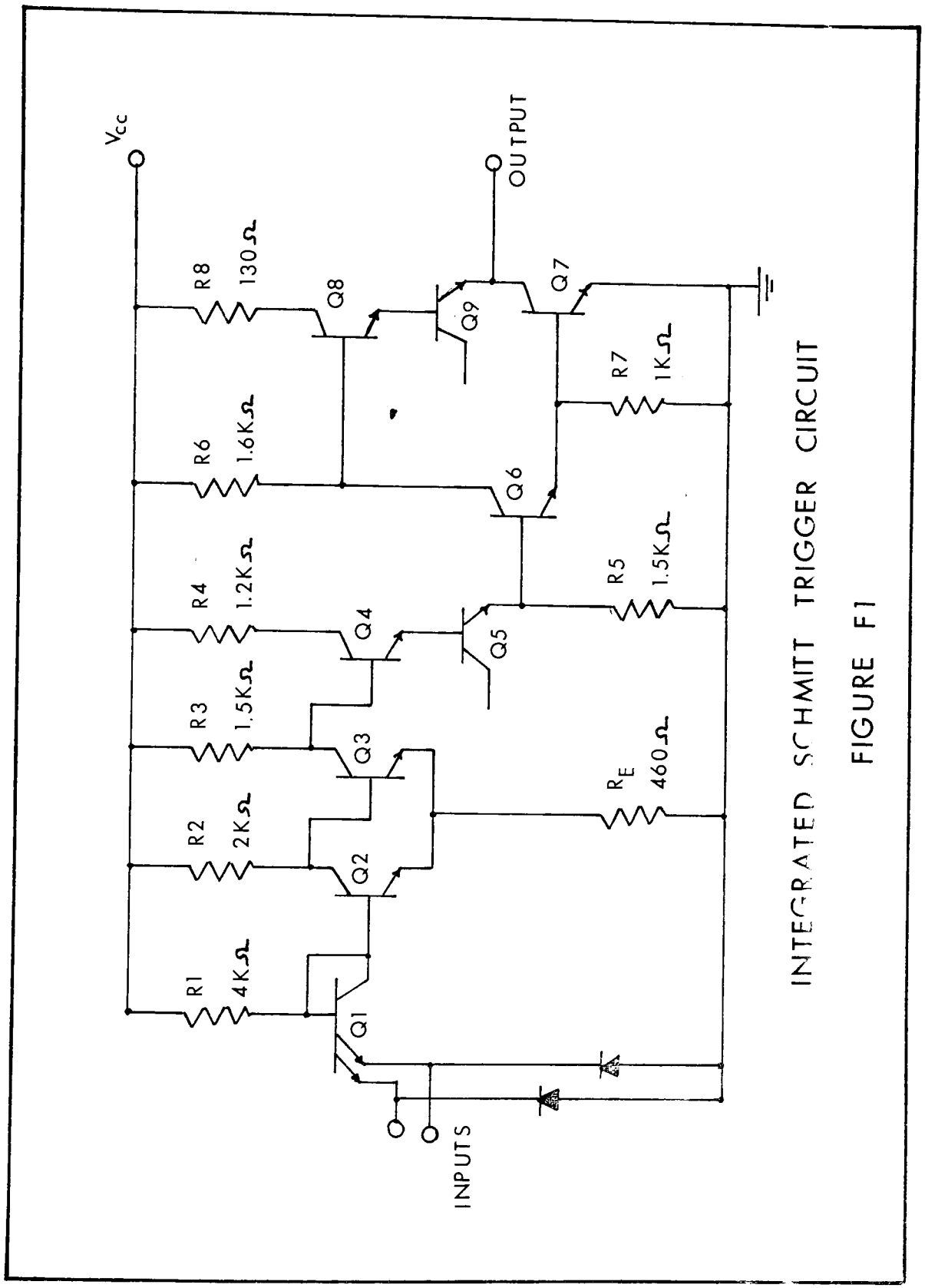
ANALYSIS OF A TTL SCHMITT TRIGGER GATE

The following analysis of a TTL type integrated Schmitt trigger circuit [13] will illustrate the dependence of its threshold levels on circuit parameters. The integrated Schmitt circuit is illustrated in Figure F-1. The operation of the circuit is as follows: The multiple-emitter transistor Q1 operates as a diode. Transistors Q2 and Q3 are the actual Schmitt trigger and transistors Q4 through Q9 make up a NAND gate of the TTL type. The transistors Q5 and Q9 function as emitter-base diodes. When all inputs are tied together at a low level, Q2 is off and Q3 is saturated. The circuit in Figure F-2 and Figure F-2a is used to obtain the positive-going voltage (V_{T+}) needed to switch from a high to a low state. Summing voltage drops around the input loop;

$$V_{T+} = -V_{BE}(Q1) + V_{BE}(Q2) + V_E \qquad (F-1)$$

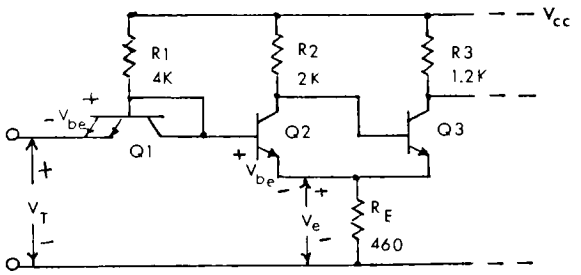
$$V_E = R_E \cdot V_{CC}/(R_{EQ.} + R_E) \qquad (F-2)$$

The negative-going threshold V_{T-} can be determined by

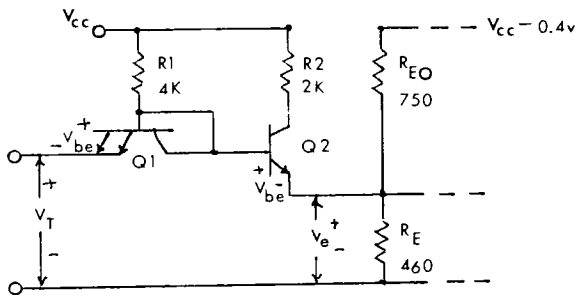


INTEGRATED SCHMITT TRIGGER CIRCUIT

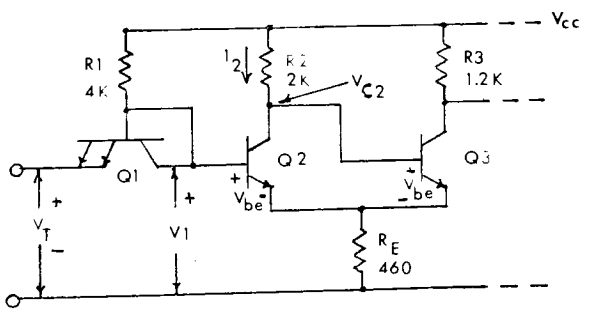
FIGURE F1



Integrated Schmitt Trigger Circuit with Positive & Negative Thresholds.



(a). V_{T+} with Q2 in Cutoff & Q3 in Saturation.



(b). V_{T-} with Q2 in Saturation & Q3 in Cutoff.

FIGURE F2

assuming transistor Q2 is ON and saturated. As the input to the Schmitt trigger drops transistor Q3 begins to turn on and the circuit conditions of Figure F-2b apply. When Q3 turns on transistor Q2 is in the active state and its collector voltage is:

$$V_{C2} = V_{CC} - I_2 \cdot R2 \qquad \text{(F-3)}$$

The collector current of Q2 is:

$$I_2 = \frac{\alpha_2 \, (V_1 - V_{BE}(Q2))}{R_E} \qquad \text{(F-4)}$$

α_2 is the common-base current gain of transistor Q2 and assumed = 1.

Substituting Eq. F-4 into Eq. F-3:

$$V_1 = \frac{V_{BE}(Q2) + \left[V_{CC} - V_{BE}(Q3)\right]}{1 + R2/R_E} \qquad \text{(F-5)}$$

The equation for V_{T-} becomes:

$$V_{T-} = -V_{BE}(Q1) + V_{BE}(Q2) - V_{BE}(Q3) + V_{C2} \qquad \text{(F-6)}$$

$$V_{T-} = -V_{BE}(Q1) + V_1$$

Replacing V_1 with F-5:

$$V_{T-} = \frac{-V_{BE}(Q1) + V_{BE}(Q2) + \left[V_{CC} - V_{BE}(Q3)\right]}{1 + \frac{R2}{R_E}} \qquad (F-7)$$

Letting $V_{BE}(Q1) = V_{BE}(Q2)$:

$$V_{T-} = \frac{V_{CC} - V_{BE}(Q3)}{1 + \frac{R2}{R_E}} \qquad (F-8)$$

APPENDIX G

LOGIC FAULT DETECTION

For circuits built in integrated form the only accessible points are the input and output terminals of the logic network and the only means of analyzing it is by performing a test, i.e., applying a set of input variables and observing the output response. Therefore, given a logic network to find an input/output pair A,X such that the response of the logic network to A will be X if and only if the circuit is operating correctly is the basis of fault detection. The application of a set of input variables A and the observation of the response to observe if it is X is called a check or test of the logic network. The major difficulty in fault detection is that for a given failure (S-@-1), it may be sensitized by A but for another failure on the same network (S-@-0), it is not. Also, the number of tests which must be applied to the circuit is proportional to the number of logic gates and is independent of the number of input terminals available.

Fault detection attempts to achieve the following objectives: (1) To detect at least a specified percentage of faults which might occur in a logic network, (2) to locate which element or gate has the fault causing the

error, (3) to detect errors fast enough to allow the circuit to retry the operation interrupted by the fault, and (4) to classify the faults as to possible cause.

There are a number of types of checking circuits used for fault detection. Their purpose usually falls within one of the following categories: (1) To check every output at all times (except possibly during transitions). Any deviation from the correct output should be detected, (2) to check any deviation from the correct output due to a single fault in the logic. Errors due to multiple faults may or may not be detected, and (3) to partially check for some incorrect outputs while other faults are not checked for.

Fault detection circuits should be designed so that faults do not propagate very far through the circuit before they are detected. The detection should stop the operation of the circuit as soon as possible after the fault is observed. Fault detection circuitry can fail just as easily as the logic being checked. It can fail in two different ways:[14] By giving an indication of a fault when it should not, or by failing to indicate faults when they occur. There are several approaches to fault detection circuitry. One method is by periodically running test sequences through the detection circuit to ensure that it operates as intended. Another method is to use two checkers on the logic instead of one. If one fails the other will

still give an output when the logic being checked fails. This method assumes that both checkers do not fail before the logic does. A practical design guideline is to design the fault detection circuitry to detect all single faults. A circuit that detects single faults soon after they occur will therefore catch many multiple faults.

LOGIC FAILURE PROBABILITY [14]

Portions of any check circuit which are tested by some checkout sequence should be considered for possible sources of undetected faults. Sometimes the check circuitry will have a built-in test sequence. One function of such a test sequence is to determine that the check circuitry is operating properly. If the check circuit is tested periodically, then calculation of the probability of a failure being undetected in the checker can be determined as follows:

The probability of no undetected failures occurringiin a period of time from 0 to T is:

$$\sum_{x=0}^{\infty} P_{CHK}^{X} \cdot P_X(t)$$

- Where P_{CHK} is the probability that a check circuit gives an indication that it contains a fault.
- Where $P_X(t)$ is the probability of "X" failures in the checker's logic occurring in the period between 0 and T.

A common form of $P_X(t)$ is:

$$P_X(t) = \frac{(\lambda \cdot T)^X \cdot \mathcal{E}^{-\lambda T}}{X!} \qquad (G\text{-}2)$$

$1/\lambda$ = means time to fail for a logic gate.

Therefore, the probability of no undetected failures is:

$$\sum_{X=0}^{\infty} \frac{(P_{CHK} \cdot \lambda \cdot T)^X}{X!} \cdot \mathcal{E}^{-\lambda T} = \mathcal{E}^{-\lambda T (1 - P_{CHK})} \qquad (G\text{-}3)$$

The mean time to an undetected failure is:

$$M.T.U.F. = \frac{1}{\lambda (1 - P_{CHK})} \qquad (G\text{-}4)$$

Eq. G-4 is independent of how often the check circuit is tested. If a failure occurs the check circuit will operate until the next test period. If T is the period between tests, then an undetected failure will be found when the next test period of the gate is run. The smaller T is, the smaller the average amount of time the check circuit will be operating with an undetected failure.

TWO-RAIL LOGIC[14]

A technique for checking is to use a variation on

duplication; that is, to use the so-called "Two-Rail" logic technique. For this type of fault detection logic two lines are used to represent every variable; i.e., the 1 state of the variable is represented by one of the lines being at logic 1 and the other line being at logic 0. Likewise, the 0 state of the variable is represented by the first line being at logic 0 and the second line being at logic 1. Using two lines to carry one "bit" of information will yield four different signals; 00, 01, 10, and 11. It is possible to select the binary states 01 and 10 to represent the 0 and 1 states respectively, while the 00 and 11 states are utilized as the third or fault state. With the coexistance of the true and complement of any logic function, an error in the input variable A and A will always be detected by comparing the output of the gate X and X. All faults caused by a single failure are detected since A and A will not be in error simultaneously.

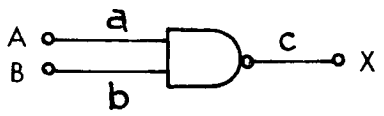
MULTIPLE LOGIC FAULTS [15] [16]

The subject of multiple faults is approached from the viewpoint that failures in a network can be represented as S-@-0 and S-@-1 conditions. This assumption covers most circuit failures due to a diode being open or short, a cut wire, a resistor being open or short, or a semiconductor being open or short. It also assumes that at more than one such fault is present in the circuit at the time a test is performed for detection. One problem associated with multiple faults in a given network is the potentially large

number of faults in it. In a network with "M" lines, there are 2^M-1 possible multiple faults. This potential number of multiple faults does not include internal failures that are isolated from the input or output pins of the logic gates.

One technique has been to generate a method to detect single faults and then extend it so that it can handle some specified types of multiple faults. In doing so a problem which arises is the masking phenomenon among faults. As an illustration, consider the circuit of Figure G-1. When the input variables are at the logic states, AB = 01, detection of the single fault of line a being S-@-1 can be accomplished. If line a and c are both S-@-1, then the application of AB will not detect the presence of line a being S-@-1. This corresponds to a masking effect of line c on line a under the presence of test AB. However, this masking is not a problem if we apply a different set of input variables in addition to AB. The application of AB = 11 detects the fault of line c being S-@-1 and no fault masks line c being S-@-1 under the presence of the test AB = 11.

As another example of fault masking, consider the logic network shown in Figure G-2. In this network a fault consisting of line a being S-@-1 is not detectable at the output X. The set of input variables, S = ABCD, ABC, ABCDE, ABCDE, and BCD , will detect all single faults in this network. Thus, line b being S-@-0 is detected at X

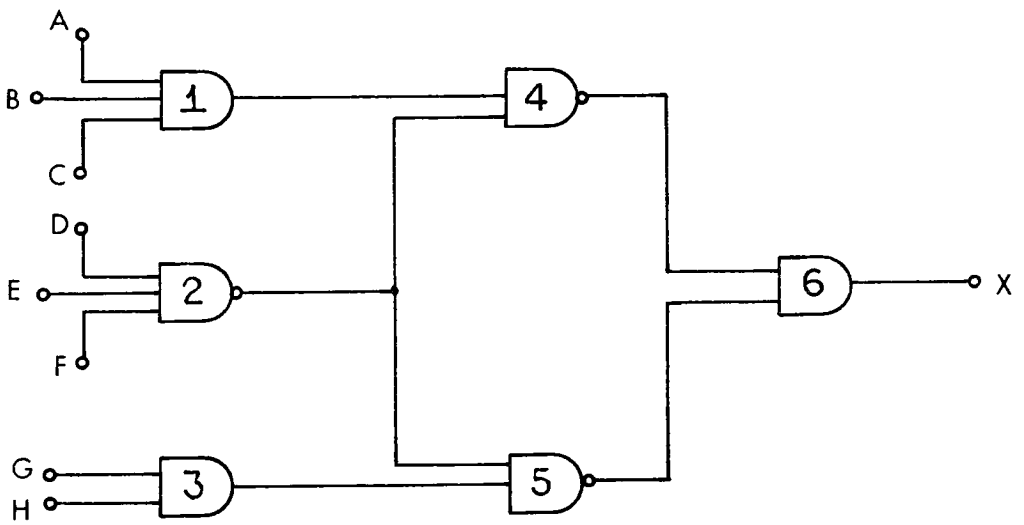


TRUTH TABLE

A	B	X
0	0	1
0	1	1
1	1	0
1	0	1

Logic Gates with Multiple Faults.

FIGURE G1

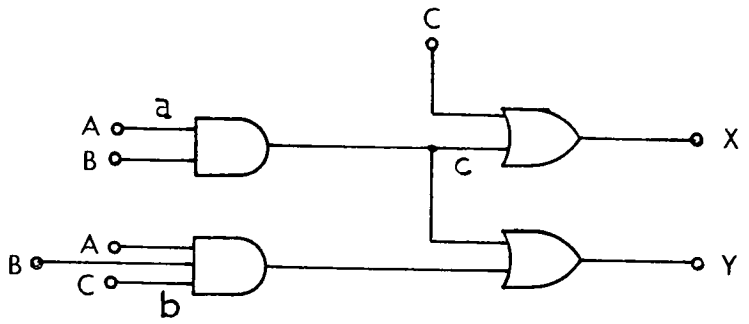


Logic Network with Multiple Faults.

FIGURE G2

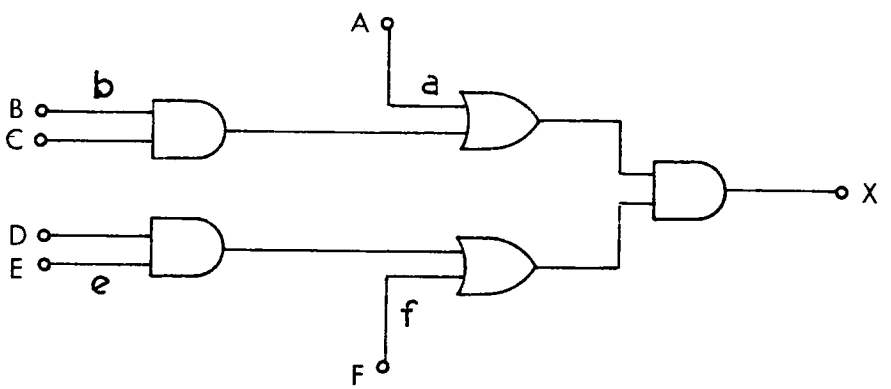
by the input variables ABCDE. However, this input will not detect the fault in the presence of the fault of line a being S-@-1 because the effect of the fault can not be made to propagate through gate 6 when A = C = 1. Under these conditions line b being S-@-0 is detectable when the input variables are ABC, which is not included in the set of input tests.

The occurrence of an undetectable fault can make two distinguishable faults indistinguishable as shown in Figure G-3, for the following example. The fault consisting of line b being S-@-1 is not detectable at output Y. The fault consisting of line a being S-@-0 is detectable at output Y by setting the input variables at ABC and at output X by setting the input at ABC. The fault consisting of line c being S-@-0 is detectable only at output X by the input variables of ABC. Hence, line a and c, S-@-0, are distinguishable. However, if the fault consisting of line b being S-@-1 occurs, these two faults (line a and c) become indistinguishable since they are both detectable only on output X by the input variables of ABC. Therefore, any set of input variables that detects all single faults may not necessarily detect all multiple faults for multilevel networks with multiple outputs. This is also true of single output multilevel networks, as illustrated in Figure G-4 and Table A. The six sets of input variables listed in Table A will detect any single fault



Logic Network ILLustrating Fault Masking for Multiple Outputs.

FIGURE G3



A	B	C	D	E	F
1	1	1	0	1	0
0	0	1	0	0	1
0	1	1	1	1	0
1	0	0	1	0	0
1	0	1	1	0	1
0	1	0	1	1	1

FIGURE G4 Logic Network showing Fault Masking for Single Outputs.

but they do not detect the multiple faults that consist of the following four faults:

> When line a and f are S-@-0 and line b and e are S-@-1.

Consequently, the technique of monitoring the output of a logic network to detect all logic faults is not adequate because of the inability to propagate many faults through to the output of the network.

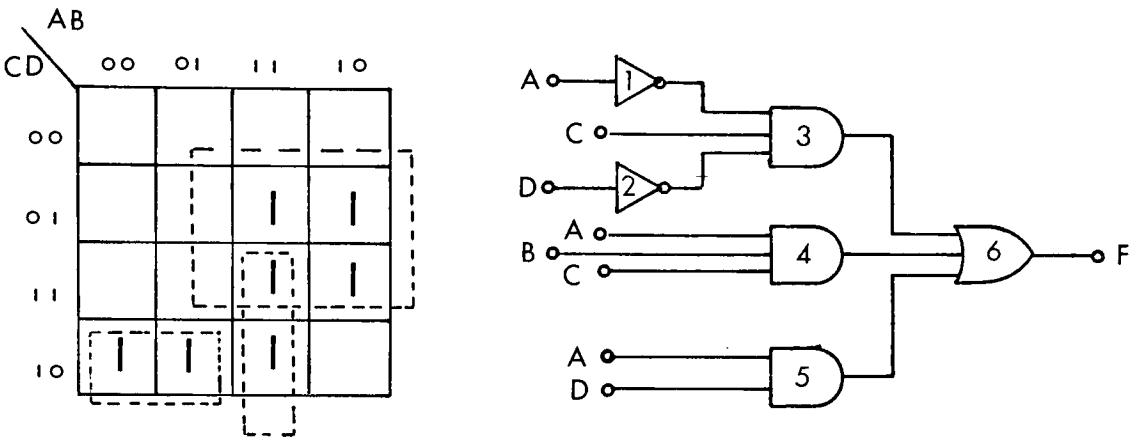
APPENDIX H

LOGIC HAZARDS

STATIC HAZARDS [17]

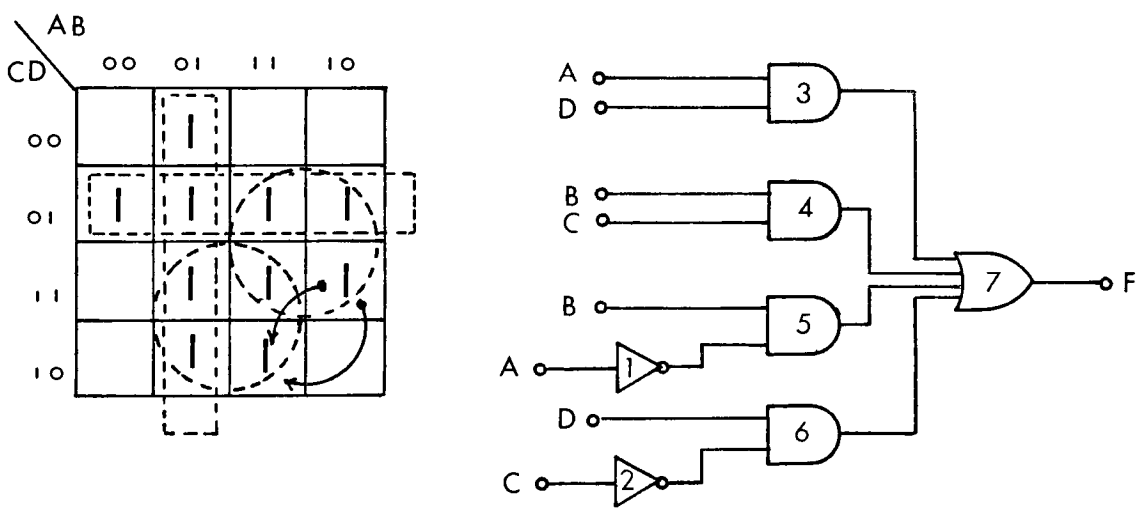
Practical electronic switching circuits differ from theoretical circuits largely in the presence of delay. Signals representing the same variable may temporarily take opposite values; signals representing complements may temporarily take identical values. As a result of this departure from the ideal a switching circuit may operate incorrectly. A logical circuit in which delays may assume values which will cause this incorrect operation contain a fault commonly refered to as a hazard. Such faults cannot be designed away and have to be corrected by delay, whether or not the circuit contains fail-safe gates.

Figure H-1 contains the Karnaugh map of a switching function and a minimum AND/OR gate realization of that function. If we assume that ABCD = 0110; we expect F = 1. If we change A so that ABCD = 1110; we expect F = 1. But the new value of A propagates toward the output along two paths. One path includes gates 1, 3 and 6; the second path includes gates 4 and 6. If the total delay introduced by gates 1 and 3 is less than the delay of gate 4 ($\tau_1 + \tau_3 < \tau_4$)



A Switching Function and a Hazardous Realization.

FIGURE H1



A Network which is not Static Hazard Free if Two Input Variables Change.

FIGURE H2

then for a period of time $[\tau_4-(\tau_1+\tau_3)]$ zeros will be present at all input terminals of the OR gate. A zero will appear on the output line if these input signals remain long enough so that gate 6 can respond, i.e., .
This is in contradiction to the ideal Boolean algebra expression. Whether a $\emptyset$ will appear in a given network will depend on the specific delay magnitudes of that network.

Once these static hazards are identified, they may be eliminated by proper design. One prime implicant selected when designing the network of Figure H-1 covers minterm 0110 and another covers minterm 1110. The AND gates 3 and 4 correspond directly to these prime implicants. When we vary the input signal, we cause the output signal of one of these gates to change from $\emptyset$ to 1 and the output signal of the other AND gate to change from 1 to $\emptyset$. If these variations do not take place at the same time, a false value of F will appear. The solution to this problem is the addition of a redundant AND gate that maintains an output value of 1 when A is varied. It is always possible to find a suitable AND gate (prime implicant) when we consider changes of a single input variable only (adjacent minterms). If we add to the network of Figure H-1b and AND gate that realizes prime implicant BCD (the prime implicant that covers minterms 0110 and 1110), this hazard will be removed. This additional AND gate continously presents a 1 to the OR gate when A is changed. Consequently, F may

not vary as a result of these changes of A. In summary, static hazards are eliminated from logic gates by basing such networks on a prime implicant cover of a switching function such that every pair of adjacent minterms is covered by at least one selected prime implicant.

MULTIPLE INPUT-CHANGE HAZARDS

If two or more input variables are allowed to change simultaneously, then false values of the output may arise in either of two ways. One is a generalization of the static hazard and can be prevented by a generalization of the technique for preventing static hazards. Figure H-2 provides a map and realization of a switching function that illustrates the generalized static hazards. The network is free of static hazards if only a single input-variable change is allowed. But if the input is varied from ABCD = 1111 to 0101, i.e., A and C are changed at the same time, then the output signals of all four AND gates must change. If AND gates 3 and 4 provide Ø's to the OR gate before AND gates 5 and 6 provide 1's (due to the delay introduced by the inverters), than a false value of F may appear.

Generalizing to include this type of activity, a static hazard exists if $f(X^i) = f(X^j) = 1$ (or Ø) and $f = Ø$ (1) can appear temporarily when the input is changed from X^i to X^j. This static hazard may be eliminated by including

in the sum-of-products expression of f a prime implicant that covers X^i and X^j if such a prime implicant exists. Prime implicant BD must be included to prevent the static hazard mentioned. Eliminating static hazards (in general) requires that all prime implicants be included in the sum-of-products expression of a function. Networks based upon the sum of all prime implicants will not be free of all hazards if arbitrary input changes are allowed. No prime implicant covers minterms 1011 and 1110 in Figure H-2. Thus, input changes from 1011 to 1110 or vice versa are not necessarily free of hazards.

If an input is allowed to change from X^i to X^j and the smallest cube which covers minterm X^i and X^j is not an implicant of the function, than a function hazard exists. In Figure H-2, if the input varies from 1011 to 1110, i.e., both B and D change, then the output signal of AND gate 3 is to change from 1 to Ø, and the output signal of AND gate 4 is to change from Ø to 1. The AND gates 5 and 6 present Ø's to the OR gate. The delays of gates 3 and 4 may be such that all Ø's are temporarily presented to the OR gate and F may assume the false value of Ø. Differences in gate delays have the effect of changing B and D in sequence. Because the exact magnitudes of these delays are unknown, we cannot conclude which sequence; B then D, or D then B, the OR gate will see. The network can take either of the two paths marked on the Karnaugh

map of Figure H-2.

Function hazards cannot be eliminated by adding redundant gates to a network. Function hazards are common if multiple input changes are allowed so that input changes must be restricted when it is necessary for fault-free operation. Thus, a second restriction is placed upon the manner in which networks are operated: Input changes are restricted to single input-variable variations.

APPENDIX I

ANALYSIS OF THE CMOS GATE

The following analysis of the CMOS inverter[6], Figure I-1, will illustrate many of its characteristics. It consists of P-and N-channel transistors, (MOS) connected as shown in Figure I-2. The following equations describe the channel characteristics of the transistors when they are connected together:

The N-channel device operating in the non-saturated region:

$$I_{DN} = K_N \cdot \left[V_{OUT} \cdot (V_{IN} - V_{TN}) - V_{OUT}^2/2 \right] \qquad (I\text{-}1)$$

Where: $V_{OUT} \leq V_{IN} - V_{TN}$

$V_{IN} > V_{TN}$

$K_N = \mu \cdot N \cdot Z \cdot C_{OX}/L$

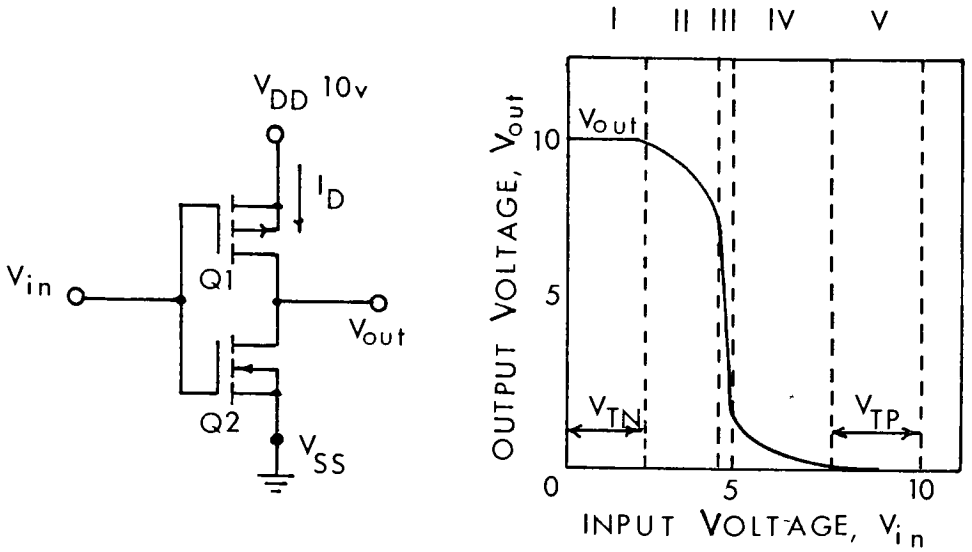
N = Surface mobility of channel carriers

Z = Channel width

L = Channel length

C_{OX} = Capacitor formed by the silicon substrate and metal gate

V_{TN} = Threshold voltage of Q2



Voltage Transfer Characteristics of a CMOS Inverter.

FIGURE I-1

V_{IN}		Q1	Q2
$0 \leq V_{IN} \leq V_{TN}$	I	NON-SAT.	CUT-OFF
$V_{out} - \lvert V_{TP} \rvert \geq V_{IN} \geq V_{TN}$	II	NON-SAT.	SAT.
$V_{out} - \lvert V_{TP} \rvert \leq V_{IN} \leq V_{out} + V_{TN}$	III	SAT.	SAT.
$V_{out} + V_{TN} \leq V_{IN} \leq V_{DD} - \lvert V_{TP} \rvert$	IV	SAT.	NON-SAT.
$V_{DD} - \lvert V_{TP} \rvert \leq V_{IN} \leq V_{DD}$	V	CUT-OFF	NON-SAT.

Piece wise Linear Equations showing Operation of Transistors Q1 & Q2 in Figure I-1

FIGURE I-2

The N-channel device operating in the saturated region:

$$I'_{DN} = \frac{K_N}{2} \cdot \left[V_{IN} - V_{TN} \right]^2 \qquad \text{(I-2)}$$

Where: $V_{OUT} \geq V_{IN} - V_{TN}$

$V_{IN} > V_{TN}$

The P-channel device operating in the non-saturated region:

$$I_{DP} = -K_P \cdot \left[(V_{OUT}-V_{DD}) \cdot (V_{IN}-V_{DD}-V_{TP}) - \frac{(V_{OUT}-V_{DD})^2}{2} \right] \qquad \text{(I-3)}$$

Where: $V_{OUT} \geq V_{IN} + |V_{TP}|$

$V_{IN} \leq V_{DD} - |V_{TP}|$

V_{TP} = Threshold voltage of Q1

$$K_P = \frac{\mu P \cdot Z \cdot C_{OX}}{L}$$

μP = Surface mobility of channel carriers

The P-channel device operating in the saturation region:

$$I'_{DP} = -\frac{K_P}{2} \cdot \left[V_{IN} - V_{DD} - V_{TP} \right]^2$$

Where: $V_{OUT} \leq V_{IN} + |V_{TP}|$

$V_{IN} \leq V_{DD} + |V_{TP}|$

The operation of the complementary pair MOS inverter, as defined in Eq. I-1, I-2, I-3, and I-4, is illustrated in Figure I-2b and shows the voltage transfer characteristics, (V_{IN} versus V_{OUT}), at a supply voltage of +10VDC. These characteristics have been divided into five regions and the function of transistors Q1 and Q2 are summarized in Table I-1. Using the DC equations for the N-channel transistor in Eq. I-1 and I-2 and the P-channel transistor in Eq. I-3 and I-4, the DC transfer characteristics of the CMOS inverter are calculated as follows:

In the transfer region III of Figure I-2b:

$$I'_{DN} + I'_{DP} = 0 \qquad \text{(I-5)}$$

Substituting Eq. I-2 and I-4 into Eq. I-5, the transfer voltage is:

$$V = \frac{V_{DD} + V_{TP} + V_{TN} \cdot \sqrt{K_N/K_P}}{1 + \sqrt{K_N/K_P}} \qquad \text{(I-6)}$$

The equation for V_{OUT} in region II is:

$$V_{OUT}=V_{IN}-V_{TP}+\left[(V_{DD}-V_{TP}-V_{IN})^2-\frac{K_N}{K_P}.(V_{IN}-V_{TN})^2\right]^{\frac{1}{2}} \qquad \text{(I-7)}$$

And V_{OUT} in region IV is:

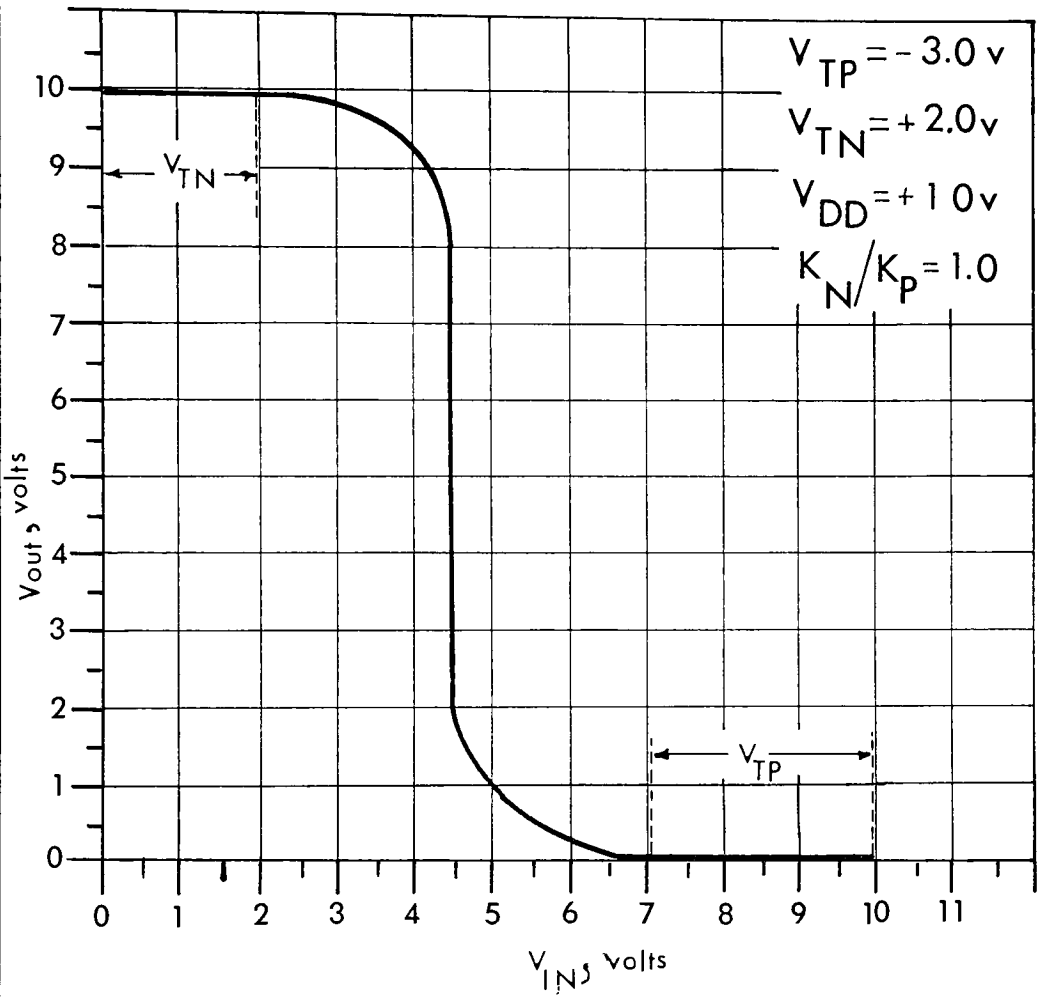
$$V_{OUT} = V_{IN}-V_{TN}-\left[(V_{IN}-V_{TN})^2-\frac{K_P}{K_N}\cdot(V_{IN}-V_{DD}-V_{TP})^2\right]^{\frac{1}{2}} \qquad \text{(I-8)}$$

Figure I-3 illustrates the calculated (Eq. I-5, I-6, I-7, and I-8) voltage transfer characteristics for the CMOS inverter with the following conditions assumed:

$K_N/K_P = 1.0$ $\qquad$ $V_{TP} = 3.0$

$V_{TN} = +2.0$ $\qquad$ $V_{DD} = +10.0\text{VDC}$

From the transfer curve it can be seen that the transfer voltage, V, is approximately equal to 4.5 volts. If the transistor parameters were obtained for $|V_{TP}| = |V_{TN}|$ when $K_N = K_P$, the transfer voltage would be equal to $V_{DD}/2$; the symmetry of which is apparent. However, the values for K_N and K_P are usually different for the gate, reflecting a compromise between noise immunity and switching speed.



Complementary Inverter Transfer Characteristics.

FIGURE 1-3

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