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A physics-based model of SiC-based MESFETs

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A Physics-Based Model of SiC-Based MESFETs

by

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I still remember the time when I would peruse through a thick book written by Millman and Halkias entitled *Integrated Electronics: Analog and Digital Circuits and Systems*, and wondered with awe what it takes to be at the forefront of device research. Now I know. It takes a lot of effort, yes, but also the consorted encouragement and blessings of people around me. Of course, it is impossible to thank everyone. There have been too many people who have assisted me along my way here. But I would especially like to take this opportunity to thank the following people.

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ABSTRACT

Silicon Carbide (SiC) has been investigated as an alternative material to Silicon (Si) for enhancing the power-handling capability of semiconductor devices for simultaneous high-temperature and high frequency applications. Its high thermal conductivity, high bandgap, low permittivity, high saturation velocity, moderate mobility, material hardness and chemical inertness make it a prime candidate for power electronics, heat and light sensors, and MEMS applications. The MESFET is the most viable power transistor based on SiC. The performance of SiC MESFETs is limited by trapping and thermal effects.

A physics-based analytical model of the SiC MESFET incorporating trapping and thermal effects is reported. The model takes into account the field and temperature dependencies of carrier transport parameters and carrier trapping effects. Both surface and substrate traps have been incorporated in the model to calculate the observed current slump in the *I-V* characteristics. The trapping and detrapping from surface traps control the channel opening at the drain end of the channel that requires the drain resistance to be gate and drain voltage dependent. The substrate traps capture channel electrons at high drain bias when the buffer layer is fully depleted resulting in current collapse at low drain bias in the following *I-V* trace. The detrapping of the captured electrons is initiated with the increasing drain bias and the channel electron concentration increases which is accelerated by increased thermal effects. As a result, restoration of collapsed drain current is obtained before the trapping effect is reinitiated at high drain bias. The calculated results using the current model are in good agreement with experimental data.

A small-signal model for the MESFET has also been proposed. Calculations for the output conductance, the transconductance, the gate-source and gate-drain capacitance has also been presented.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Al	**Al**uminum
Au	Gold
BN	**B**oron **N**itride
BWO	**B**ackward **W**ave **O**scillator
CFA	**C**rossed **F**ield **A**ntenna
DC	**D**irect **C**onvention
DLTS	**D**eep **L**evel **T**ransient **S**pectroscopy
FET	**F**ield **E**ffect **T**ransistor
GUI	**G**raphical **U**ser **I**nterface
HEMT	**H**igh **E**lectron **M**obility **T**ransistor
HTCVD	**H**igh-**T**emperature **C**hemical **V**apor **D**eposition
InN	**In**dium **N**itride
LNA	**L**ow **N**oise **A**mplifier
MESFET	**M**etal-**S**emiconductor **F**ield **E**ffect **T**ransistor
MOS	**M**etal **O**xide **S**emiconductor
Ni	**Ni**ckel
PVT	**P**hysical **V**apour **T**ransport
SHR	**S**hockley-**R**ead-**H**all
Si	**Si**licon
SI	Semi-**I**nsulating
Ti	**Ti**tanium
TWT	**T**raveling **W**ave **T**ube
UMOSFET	**U**-trench **MOSFET**

ε	Permittivity of SiC
μ	The channel mobility of electrons. This is position dependent but positional dependence is not explicitly mentioned.
μ_{min}	The minimum value of the mobility of electrons in SiC. This is used as a parameter in the Caughey-Thomas model for specifying the dependence of low-field mobility on the doping.
μ_{max}	The maximum value of the mobility of electrons in SiC. This is used as a parameter in the Caughey-Thomas model for specifying the dependence of low-field mobility on the doping.
α	Fitting parameter used for the prediction of the doping dependence of the low-field mobility
μ_0	The low-field mobility
β	A fitting parameter used in the calculation of the field-dependence of mobility of electrons in SiC
ξ	Parameter used for the definition of the critical electric field
ΔT	Temperature difference between the outside contact and the channel
a	Thickness of the channel
C_{gd}	Gate-drain capacitance
C_{gs}	Gate-Source capacitance
D	Coupling Constant
E	This is the magnitude of the lateral electric field at position x of the channel. The x dependence is not explicitly mentioned.
E_S	Saturation electric field
g_m	Transconductance
g_{ml}	Transconductance in the linear region
g_{ms}	Transconductance in the saturation region
$h(x)$	Height of the depletion region at the gate metal-semiconductor interface
$h_1(x)$	Height of the depletion region formed in the channel due to the p-n junction at the channel-buffer interface

h_{1L} Thickness of the depletion region in the channel due to the p-n junction formed between the channel and the buffer at the drain end of the channel. This is numerically equivalent to $h_1(L)$.

h_{1L1} Thickness of the depletion region in the channel due to the p-n junction formed between the channel and the buffer at the point where pinchoff occurs. This is numerically equivalent to $h_1(L_1)$.

h_{1S} Thickness of the depletion region in the channel due to the p-n junction formed between the channel and the buffer at the source end of the channel. This is numerically equivalent to $h_1(0)$.

h_D Thickness of the depletion region due to the gate metal-semiconductor contact at the drain end of the channel before pinchoff. This is numerically equivalent to $h(L)$.

h_{L1} Thickness of the depletion region due to the gate metal-semiconductor contact at the point where pinchoff occurs. This is numerically equivalent to $h(L_1)$.

h_S Thickness of the depletion region due to the gate metal-semiconductor contact at the source end of the channel. This is numerically equivalent to $h(0)$.

I_D The magnitude of the drain current

K Heat capacity of SiC

L Length of the channel

L_1 The length of the channel where pinchoff occurs. This is a condition that occurs only after saturation and so this variable has meaning only after the current has saturated. This parameter is representative of channel length modulation.

m_0 Rest mass of an electron

m_t Transverse effective mass of an electron

N The doping concentration for use in the Caughy-Thomas model for calculating the doping dependence of the low-field mobility

N_A Doping concentration of the buffer layer

N_D Effective doping concentration of the channel

$N_{Dactual}$ Actual doping concentration of the channel

N_{Ref} The reference doping concentration for the Caughy-Thomas model

P_{diss} The power dissipation in the channel

q	Magnitude of the charge in an electron
Q_1	The magnitude of charge in the depletion region under the gate
R_D	Drain resistance
R_S	Source Resistance
T	Absolute temperature
U_{bi}	Built-in potential at the p-n junction between the channel and the buffer
ul	Velocity of sound in SiC
v	Drift velocity of the electrons
$V(x)$	Potential at point x in the channel
V_1	Channel potential at $x = L_1$
V_A	The value of the drain bias at which the electron release from substrate traps commences
V_B	The value of the drain bias at which the effective channel doping equals the actual channel doping
V_{bi}	Built-in potential at the gate metal-semiconductor interface
V_D	Applied drain voltage
V_G	Magnitude of the applied gate voltage
v_{sat}	The saturation velocity of electrons in SiC
W	Width of the channel
$W(x',y)$	Potential function used for effecting the two-dimensional analysis of the depletion region under the gate
x	Position along the channel. The point just under the source end of the gate is considered 0 (See Fig. 2-2)
x'	A transformed reference frame used for a two-dimensional analysis of the depletion region under the gate
y	Position normal to the channel. The point just under the gate is considered 0
Ξ	Acoustic deformation potential
Ω_0	Optical phonon energy

Journal

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Chapter 1

Introduction

1.1 Introduction

Since the conception and introduction of semiconductor devices, vacuum tube technology has been replaced by semiconductor devices in virtually all areas of microwave electronics. Power electronics present the last frontier for semiconductor devices. The primary disadvantage of semiconductor devices has always been their thermal instability. Commercial microwave and broadband communications require devices to handle powers of the order of a few watts to a few megawatts. Further, semiconductor realestate being inherently expensive, there is a constant drive towards miniaturization in the semiconductor industry. Commercial semiconductor power transistors are of the order of 5 μm × 500 μm, and dissipating megawatts of power over such small areas is inherently difficult. Further voltage drops of the order of 35-40 V across the 5 μm length of a transistor create excessive electrical stress in the device, especially since most of the voltage drop generally occurs across a very small fraction of the gate length of the device. Thus high-power electronics is still dominated by vacuum tube devices. To successfully combat thermal and electrical stress, it is necessary to inhibit thermally excited electrons from crossing the energy gap. This may be achieved by increasing the bandgap between the conduction band and the valence band, while taking care that semiconductor properties still characterize the device. Since the difficulty encountered by electrons in crossing the bandgap is exponentially dependent upon the magnitude of the bandgap (according to Fermi-Dirac statistics), even a small increase in the bandgap yields great power advantages. In short, the quest for

materials better suited for the manufacture of high power devices transits naturally into the quest for the material having the greatest energy band separation. This simple truth was realized very early on, but like so many other great ideas, had to wait until mature manufacturing processes were developed for the production of what is now known as the set of *wide-bandgap* materials, primary among them being the materials GaN, AlN, InN, BN and several ploytypes of SiC. As can be seen from Fig. 1-1 [1], the state-of-the-art of semiconductor power devices are able to produce powers of several hundred watts at about 2 GHz to around a watt of output power at 100 GHz. They are not yet powerful enough to replace the klystrons, gyrotrons, Crossed Field Antennas (CFAs), gridded tubes, Backward Wave Oscillator (BWOs) and Traveling Wave Tubes (TWTs). Still, the first steps have been taken.

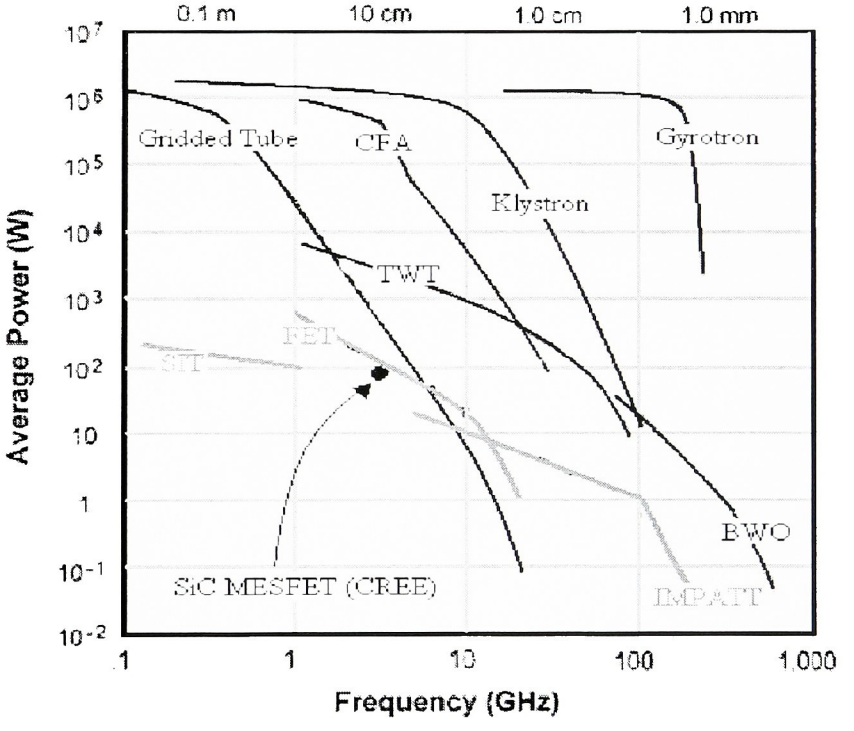


Fig. 1-1. A graphic description of the power-frequency characteristics of the current state-of-the-art of SiC MESFETs superimposed over power-frequency characteristics of several vacuum tube and GaAs-based devices [1]. Dark lines represent vacuum-tube devices while the light lines represent semiconductor-based devices.

Semiconductor FETs and MESFETs are able to compete (at least in part) with the gridded tubes. Further improvements in device fabrication, coupled with sound theoretical insight into the workings of these devices should definitely improve yield and the necessity for a vast majority of the vacuum tube technology removed.

1.2 Material Advantages of SiC

SiC being a high-bandgap semiconductor is a natural choice for high-power devices. Apart from having a wide bandgap, SiC also has a number of other electrical and mechanical parameters that make it suitable for high-power and high-frequency applications. Table 1-I depicts the most important material parameters that yields SiC suitable for the manufacture of high-power devices. The material parameters are explain in detail below.

Table 1-I. Comparison of the material properties of SiC [2], GaN [2], GaAs [3] and Si [3].

Property	4H-SiC	6H-SiC	3C-SiC	GaN	Si	GaAs
Energy Gap (eV)	3.23	3.0	2.36	3.39	1.1	1.43
Critical Electric Field (MV/cm)	3-5	3-5	1	5	0.2	0.4
Saturation Velocity × 10^7 (cm/s)	2	1.5	2	2.5	1	0.7
Mobility (cm^2/Vs)	900	400	800	1000	1350	8500
Relative Dielectric Constant	9.66	9.66	9.72	9	11.8	12.5

1.2.1 Bandgap

The bandgap of SiC (3.23 eV) is three times that of Si (1.12 eV). This allows it to have significant advantages over Si and other smaller bandgap materials and this is the reason why the so-called high-bandgap materials are being investigated vigorously as material alternatives for power devices. Due to the high bandgap of SiC, it requires a large electric field for electrons to transit from the valence band to the conduction band. As a direct consequence, the intrinsic concentration of SiC is of the order of 10^{-8} cm^{-3} [2] while that of Si is of the order of 10^{10} cm^{-3} [3]. This allows the manufacture of SiC substrates that are

nearly semi-insulating. Semi-insulating substrates may be created by the introduction of defects within the bandgap (by the introduction of vanadium [4] for example). Defects within the bandgap succor recombination resulting in a reduction of the intrinsic carrier concentration, and a consequent decrease in the conductivity. Further, due to the high bandgap, the leakage current of a SiC diode is lower than that of a Si diode by a factor of 10^4-10^5 [5], [6]. Thus, sensors created of SiC are generally up to 10,000 times more accurate than comparable Si-based diodes.

Depending upon the polytype used, inter-band transitions of electrons from the conduction band to valence band allow for colored electromagnetic emissions, notably green (6H-SiC), green-yellow (4H-SiC), yellow (15R) and pale-yellow for the doped material and greenish-yellow for the undoped material [7]. Further, SiC may be used for the detection and emission of blue and ultraviolet radiation.

1.2.2 Critical Electric Field

Due to the higher bandgap of SiC, the critical electric field necessary for electrical breakdown of SiC (3 MV/cm) is 10 times higher than that of Si (0.3 MV/cm) [8]. It is thus possible to apply much higher voltages to a device manufactured using SiC when compared to an equal-sized Si-based device. The primary aim of a power device is to be able to control and amplify high voltages, and thus the critical electric field is of paramount importance in determining the operational limit of a power device. Further, the higher power supply voltages allow devices to deliver higher output power.

1.2.3 Mobility

The low-field, intrinsic mobility of the device is one of the most important factors influencing the frequency characteristics of the device since it determines the ability of the free electrons in the material to respond to changes in the electric field applied across it. The low field bulk mobility of SiC is 1000 $cm^2/V.s$, which compares favorably with that of 1350 $cm^2/V.s$ of undoped Si.

1.2.4 Saturation Velocity

With an increase in the electric field, the mobility steadily decreases until a point is reached wherein any increase in electric field does not result in any further increase in the velocity of electrons. The

corresponding velocity is known as saturation velocity. This is discussed in detail in Chapter 2. It is a quantity that primarily determines the magnitude of the saturation drain current and hence directly affects the transconductance of the device in the saturation region of operation. Thus a higher saturation velocity is tantamount to greater transconductance. The saturation velocity of SiC is 2×10^7 cm/s, which is twice that of Si.

1.2.5 Relative Dielectric Constant

Since the relative dielectric constant of SiC (9.7) is smaller compared to that of Si (11.8), SiC based devices have much lower capacitances compared with Si-based devices and thus allow the devices to operate at much greater frequencies. The high saturation velocity, moderate mobility and low relative dielectric constant permit SiC-based devices to operate at high frequencies.

1.2.6 Thermal Conductivity

The thermal conductivity of SiC is 4.9 W/cm.K, which is greater than 1.5 W/cm K of Si. Even if a lot of heat is generated in the device, it is easily drained out of the device due to the high thermal conductivity.

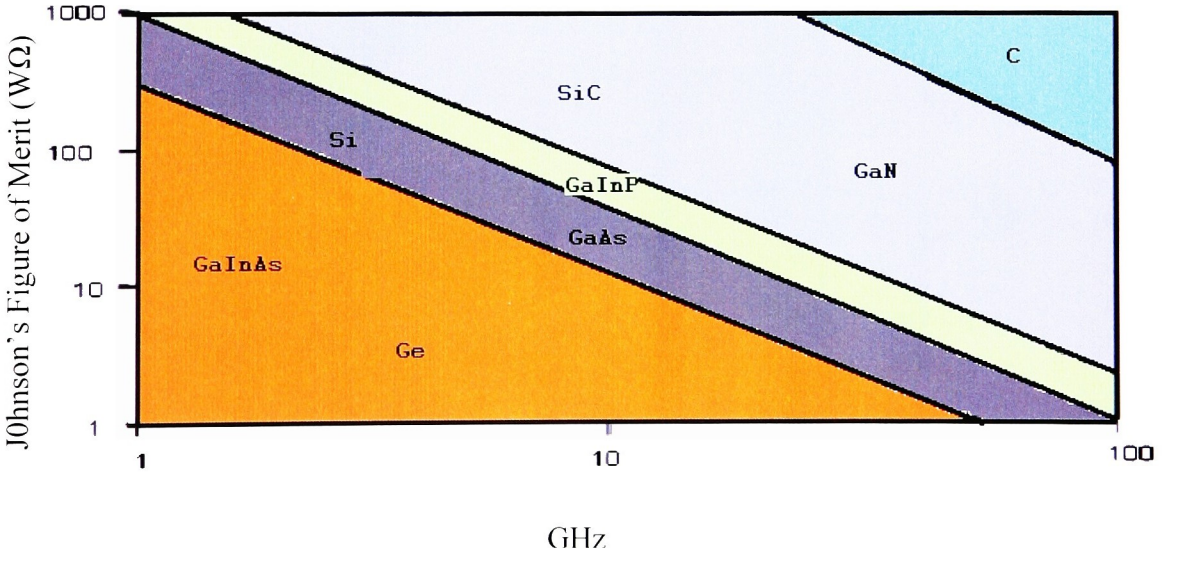


Fig. 1-2. Johnson's figure of merit for various semiconductors. SiC and GaN are among the best materials for power-devices [9].

Thus the need for elaborate cooling mechanisms is obviated in most cases. It is interesting to note here that when other semiconductor materials (such as GaN) are used for making a power device, they are generally grown on a SiC substrate for this reason.

One of the most important metrics to measure the power-handling capacity of a device at high frequency is Johnson's figure of merit [9]. Johnson's figure of merit for several materials is depicted in Fig. 1-2. It is seen that SiC together with GaN has one of the best Johnson's figure of merit and is second only to diamond.

1.2.7 Physical Parameters

SiC is a very hard material (having a Young's Modulus of 700 GPa [2] while that of Si is only 165 GPa, [3]) and is chemically inert. Thus, SiC is also suited for operations in high-radiation areas like nuclear reactors and outer-space, as well as for MEMS applications.

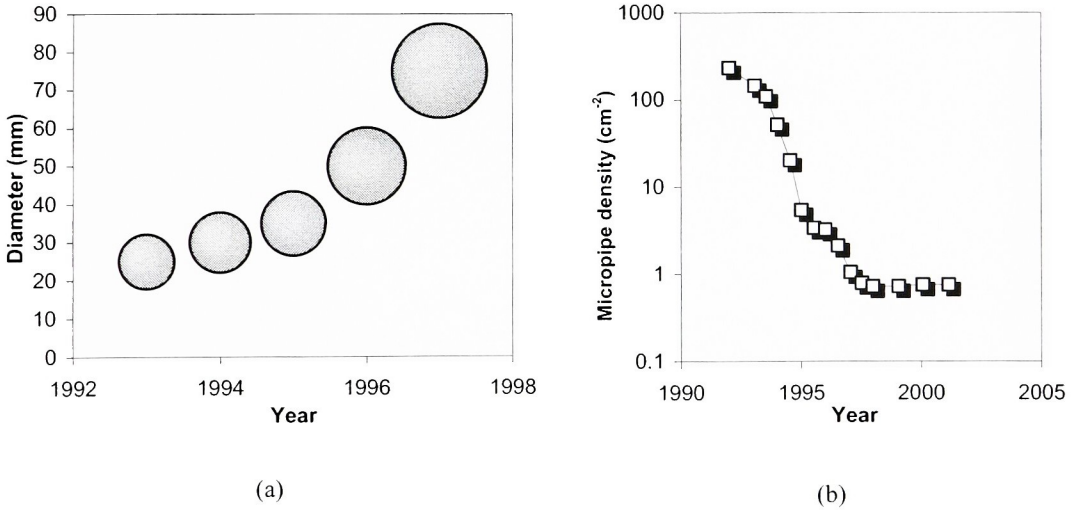


Fig 1-3. The improvement in device fabrication technology as shown by the (a) increase in size of wafer (CREE® corporation), and (b) decrease in the micropipe density per year [10].

Power devices are generally large since they need to dissipate high power and carry high current. Thus it is important to be able to manufacture wafers that are devoid of defects. Device fabrication using 3C-SiC was initially pursued but since it was easier to manufacture the 4H- and 6H-SiC polytypes of SiC, they have been studied and characterized extensively. Currently 2-inch and 3-inch 4H- and 6H- SiC wafers are available, with the 2-inch wafers being virtually micropipe free [10].

Today, the number of manufacturers providing the SiC substrate has increased from a single manufacturer to more than five manufacturers. A diagram depicting the increase in the wafer size and the simultaneous decrease in the micropipe density by the year is depicted in Fig. 1-3. It is clear that the process technology has improved rapidly and is expected to keep improving in the future. As the micropipe density decreases, bigger devices having better power-handling capability may be built, and further, the yield of each wafer may be significant.

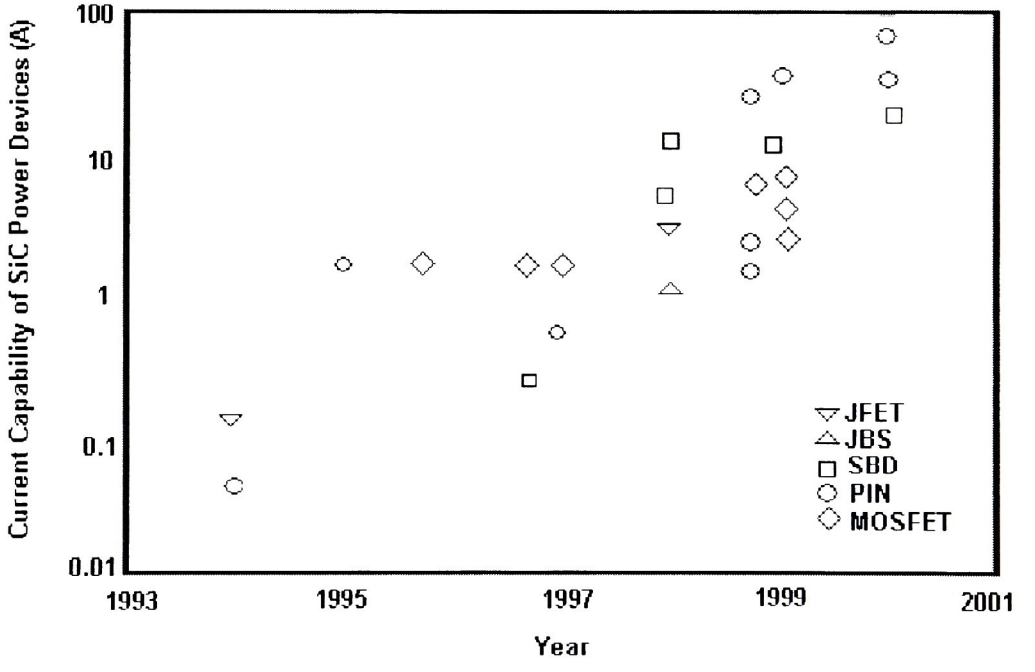


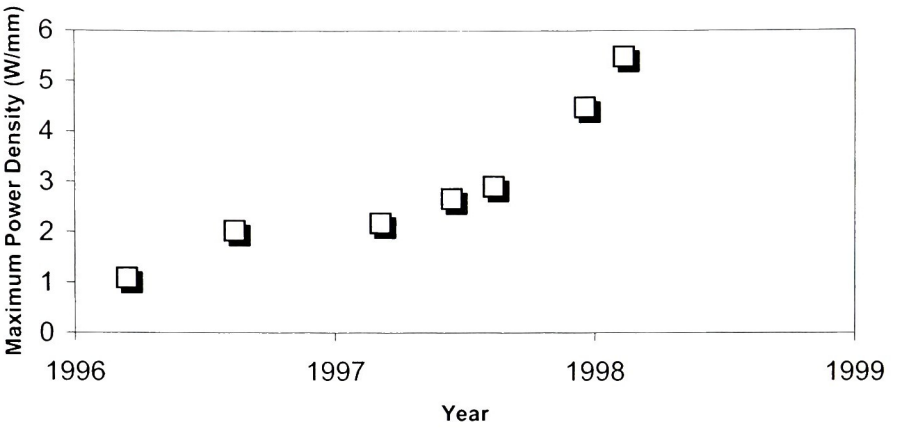
Fig. 1-4. A schematic diagram of the progress in the current-carrying capabilities of SiC power devices over the years.

As a result of the beneficial characteristics of SiC, various devices have been fabricated using SiC such as Schottky [11], [12] and p-n junction diodes [13], thyristors [14] and U-trench MOSFETs (UMOSFETs) [15]. The power handling capability of the devices has steadily increased through the years as evident from

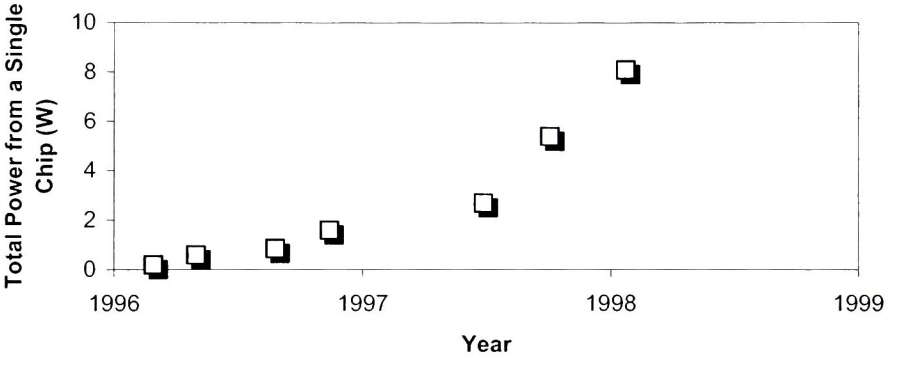
the statistics shown in Fig. 1-4, which depicts the increase in the current carrying capabilities of various SiC based devices over the years. Current carrying capabilities of SiC power devices have increased a hundred fold over a span of less than ten years, from less than one ampere in 1993 to close to a hundred amperes in 1999.

1.3 Reasons for the Popularity of the SiC MESFET

Heterostructure configurations for SiC, although under current research [16]-[18], are not yet popular. Further, even though there have been great improvements in oxide growth over SiC, the surface mobility of electrons in SiC [19], [20] based MOS devices are still not production grade. The power device of choice that has been extensively studied and characterized and still under inspection is the metal semiconductor field effect transistor (MESFET). This structure allows the electrons to flow through the doped channel which causes the electrons to travel with bulk mobility as opposed to surface mobility of the MOS structure, thus allowing for better mobility and subsequently better frequency operation. Fig. 1-5 shows the development of the state of the art of SiC MESFET technology. It can be seen that the maximum power density of the SiC MESFET has had a steady increase and has increased nearly six-fold between 1996 and 1999, while the total power from a single chip has increased more than eight fold during the same time. Such improvements in power performance have spurred further research in SiC MESFETs. Currently, commercial grade SiC power MESFETs are obtainable from CREE corporation® like the CRF-24010®. Further, since the frequency-power-bandwidth tradeoffs between the GaN HEMT and the SiC MESFET are not fully understood, the SiC MESFET having the lower input capacitance might offer much better total power output.



(a)



(b)

Fig 1-5. Improvements in the capabilities of the MESFETs in terms of the (a) the maximum power density and (b) the total power from a single chip.

1.5 Thesis Contribution

SiC MESFETs were initially prepared on n^+ substrates [21]. These MESFETs had problems pertaining to capacitive losses and the formation of secondary channels in the substrate, resulting in the degradation (in part) of transistor operation. The introduction of preparatory techniques for SI substrates has led to the realization of large-periphery SiC MESFET structures, which can support much higher currents without detrimental capacitive effects.

The SI substrates are semi-insulating by the introduction of vanadium. Vanadium introduces levels at 1.17eV, 1.7eV and 0.97eV below the conduction-band [2]. DLTS measurements [22] have also revealed trap levels at 0.51eV, 0.60eV, 0.68eV, 0.768eV and 0.89eV above the valence band. The trap located at 0.51eV above the valence band is probably due to the defects created by the introduction of nitrogen (used for doping the channel) [23]. The trap located at 0.6eV above the valence band is due to vanadium [24]. The other trap levels are of unknown origin. Apart from the traps present at the substrate, surface traps have also been observed [25], [26]. These traps are responsible for significant current collapse of the *I-V* characteristics resulting in temporal current degradation [27]. Transconductance and output conductance become frequency-dependent as a result of the trapping phenomenon [28].

Various attempts have been made in the way of characterization of these traps [29] and their effects [30]. Although extensive research has been carried out in this field, the understanding of the SiC traps is still in its infancy. Some understanding of the trapping phenomenon has been obtained as a result of this investigation and various methods have been proposed for circumventing the effects of the traps. Some of these techniques involve the investigation of alternative methods of substrate growth [31], some involve the investigation of alternative device geometries while others involve the variation of the characteristics of the buffer layer [32], [33] (a thin epitaxially grown layer separating the channel and the substrate, which will be investigated in detail later in the thesis).

Even though various qualitative theories describing the trapping phenomenon in the SiC MESFET have been suggested [33], prevalent research has not been geared toward the proposal of a quantitative model intended to quantify the slump in *I-V* measurements. In this work, a new model for the calculation of the *I-V* characteristics in the presence of surface and substrate traps has been proposed. Further, the current model of the *I-V* characteristics takes into account the source and the drain resistances and the effect of the buffer layer when present.

A small-signal model for the MESFET has also been proposed which incorporates the source and drain resistances, and the depletion layer formed at the channel/buffer interface.

1.4 Thesis Outline

Chapter 2 discusses the DC model of the SiC MESFET. First, the mobility model for the electrons is described. This mobility model incorporates the (lateral) field dependence, the temperature dependence and the concentration dependence mobility. The general structure and the working principles of the MESFET are introduced next. Characteristics of the depletion region that appear between the channel and the buffer are discussed next. This is key in understanding the trapping mechanism that has been proposed. Then the current equations for the linear regions are derived, followed by the description of the pinchoff criterion and finally the current equations for the drain current equations at saturation are described.

Chapter 3 discusses the non-idealities present in the *I-V* relationship in the SiC MESFET as a result of trapping and thermal effects. The first part of Chapter 3 is dedicated to the description of the various trapping phenomena, the consequent current slump and the proposed model for the *I-V* characteristics. The chapter discusses the substrate traps, the effects of the surface and the substrate traps and the way in which they are modeled. The second part of Chapter 3 describes the thermal dependencies of the model. Since MESFETs are generally intended to be used as power devices, significant joule heating is expected within the device. Although the power dissipating capability of the material is significantly greater than most of the other semiconductor materials, self-heating effects are not entirely absent. The chapter describes the thermal dependencies of the various material parameters used during the simulations and the method by which these temperature dependencies have been incorporated.

Chapter 4 describes a small-signal model of the device. This model describes the low-frequency model of the transconductance, the output conductance, the capacitances between the gate and the drain and that between the gate and the source. This derivation of the capacitances does not take into account either the temperature dependence of the small-signal parameters or the frequency dependence of the small-signal parameters.

Chapter 5 presents the conclusion and looks at the future work that may be done.

Chapter 2

Modeling DC Characteristics

2.1 Introduction

In this chapter, the *I-V* characteristics for a SiC-based MESFET are derived. Section 2.2 describes the structure and the basic principles of the MESFET. Section 2.3 describes various depletion regions present in SiC-based MESFET structures. A very general mobility model has been used in the simulation, which has been described in Section 2.4. In Section 2.5, the current equation in the linear region is derived. Section 2.6 determines the important criterion of pinchoff. Finally, in Section 2.7 the current equations for the saturation region have been derived.

2.2 A Brief Overview of the General Structure and Principles of the MESFET

The simplest MESFET structure is shown in Fig. 2-1. A doped channel is grown over a semi-insulating (SI) substrate. Ohmic contacts for a source and a drain are formed and a lateral electric field controls the electron/hole flow in the channel when a potential is applied between the source and the drain. For controlling the amount of charge moving through the channel (and thus controlling the current through the channel) a Schottky gate is placed between the source and the drain. Application of a bias voltage at the gate allows one to control the thickness of the depletion region under the gate and thus control the drain current. When a sufficiently large voltage bias is applied at the gate, the depletion region pinches off the channel and the drain current becomes independent (actually, nearly independent) of the drain voltage, and dependent only upon the gate voltage. In SiC, the semi-insulating substrate is created by the introduction of vanadium. Vanadium introduces deep levels near the center of the energy-gap of SiC. Since the energy-gap

of SiC is very high, the introduction of deep-levels succors the resistivity by *freezing-out* the already meager amount of intrinsic carriers present. Unfortunately deep levels not only capture intrinsic carriers present in the substrate, but also channel carriers that escape from the channel and end up in the substrate.

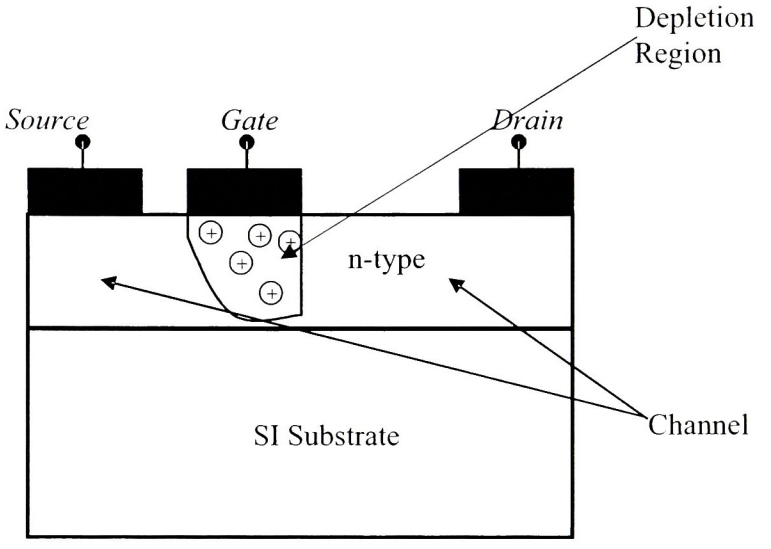


Fig. 2-1 A schematic representation of the basic MESFET structure.

The formation, the capture process and the release of electrons from these deep levels will be examined in the Chapter 3 in greater detail. The channel is generally n-type doped. This is because the bulk-mobility of holes in SiC is impracticably low and thus p-channel MESFETs are generally low-frequency devices. The epitaxial growth of the channel introduces lattice-mismatch between the n-channel and the substrate. This leads to the formation of traps at the interface between the n-channel and the substrate. To mitigate the effects of the interface traps, another layer is inserted between the channel and the substrate. This layer is known as the buffer layer and is generally p-type doped. Interface traps formed between the buffer-layer and the substrate do not affect the interface between the buffer layer and the channel.

In general, the current flowing through the channel is primarily determined by the dimensions, the doping conditions of the channel (which determine the channel resistivity), the mobility and the velocity of electrons in the channel. In the MESFET structure analyzed in this work, the electrical dimensions of the channel are determined by the depletion regions formed within the channel at the metal-semiconductor junction of the gate and the channel-buffer p-n junction. The velocity of the electrons in a semiconductor is

determined by the electric field and the mobility of the mobile carriers in it. Since the depletion regions in the channel and the carrier mobility are of paramount importance in determining the *I-V* relationship of the device, both the depletion regions and the electric field are revisited in Sections 2.3 and 2.4, respectively.

2.3 The Depletion Regions

Fig. 2-2 depicts a snapshot of a simulation of the MESFET in operation at a gate voltage of -1V and a drain voltage of 1V. In the snapshot, the depletion region boundaries are represented as red lines and the current density is represented in gray-scale. It may be observed that the current density is limited to the undepleted region of the channel. The simulation is obtained using the 2D Atlas® simulator. The simulator details are described in Annexure I.

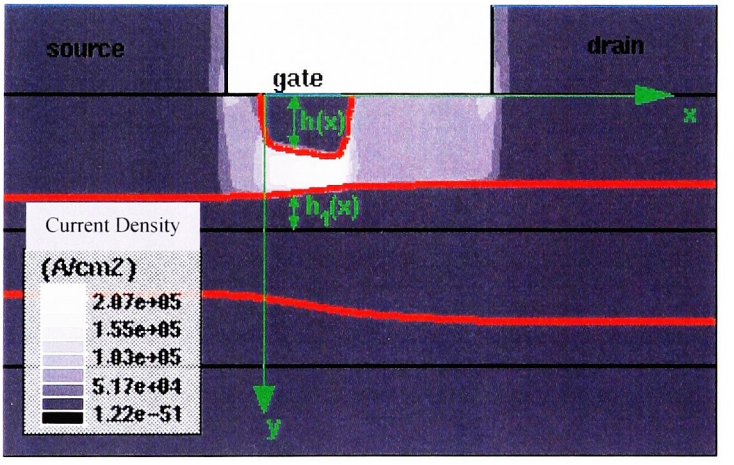


Fig. 2-2 A snapshot of the cross-section of the MESFET simulation depicting the buffer layer and the resulting depletion region formed. It also shows the depletion region formed at the Schottky gate. The depletion region boundaries are shown in red while the conduction region current density is shown in gray-scale.

Prevalent analytical solutions take into account the depletion region due to the gate only, but as clearly seen from Fig. 2-3, both depletion regions are necessary in determining *I-V* characteristics of the device. The

axes and the depletion region depths within the channel are shown in green (and have been appended to the figure on the simulator output).

The depletion region under the gate is due to the metal-semiconductor Schottky contact with the application of the gate bias. In general, the height of this depletion region at the point x in the channel is given by the equation:

$$h(x) = \sqrt{\frac{2\varepsilon}{qN_D}\left[-V_G + V_{bi} + V(x)\right]}, \tag{2-1}$$

where ε is the permittivity of SiC, N_D is the doping concentration of the channel, q is the magnitude of the electron charge, V_G is the applied gate bias, and $V(x)$ is the potential of the channel at point x. V_{bi} is the built-in potential of the metal-semiconductor Schottky contact and this is given by:

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right), \tag{2-2}$$

where n_i is the intrinsic carrier concentration of SiC. Equation (2-1) predicts that the higher the magnitude of the gate bias, the thicker the depletion region under the gate. This can be seen in Fig. 2-3. Fig. 2-3 shows the height of the depletion regions under different gate biases. The drain bias is held constant at 0.01 V. In Fig. 2-3 (a) the gate bias is 0V while in Fig. 2-3 (b), the gate bias is –3V. It may be plainly observed that the depletion region depths increase with an increase in the magnitude of the gate bias. The equation predicts that the height of the depletion region under the gate is also dependent upon the channel potential and should thus be position dependent. Since the drain bias in Fig. 2-3 is very low (V_D = 0.01V), the height of the depletion region under the gate is nearly constant over the length of the gate. However, as the drain bias is increased, the height of the depletion region under the gate due to the Schottky contact increases along the length of the device toward drain, as seen in Fig. 2-2.

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the channel-buffer interface increases as channel potential increases from 0V at the source end of the channel to 1V at the drain end of the channel.

2.4 Mobility

An electric field applied across the crystal lattice of a material introduces force on the charged particles constituting the device. Mobile charges are accelerated either in the direction of the electric field or in a direction opposite to the electric field depending upon the nature of charge of the mobile carriers. The charges cannot accelerate indefinitely however, but acquire a constant velocity v called the drift velocity under the influence of the electric field E. The relationship between the drift velocity v and the electric field E is linear for low values of electric field and is given by the relation:

$$v = \mu E , \tag{2-5}$$

where μ is the mobility of the mobile carriers. As MESFETs made of SiC are generally n-type, the mobile carriers are generally electrons. All further references to either mobile carriers or majority carriers will refer to electrons unless specifically mentioned otherwise. The drift velocity of the electrons is seen to be linearly proportional to the electric field in equation (2-5). This is true only when the electric field is sufficiently low. As the electric field increases, the velocity asymptotically approaches a constant maximum velocity. This is called the saturation velocity of the electrons and is denoted by v_{sat}. The cause of a constant drift velocity is the energy loss that occurs during electron-phonon interactions. Thermal effects are less at low drain voltages. It is thus only natural that the low-field mobility should be a stronger function of the doping concentration. The most widely used model for the determination the mobility of a doped material was proposed by Caughey and Thomas and is widely known as the Caughey-Thomas model. The low-field mobility, according to the Caughey-Thomas model is [34-35]:

$$\mu_0 = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left(N / N_{\mathrm{Re}f}\right)^{\alpha}} , \tag{2-6}$$

where α, μ_{max}, μ_{min} and N_{Ref} are characteristic of the material. For SiC these values are 0.5, 950 $cm^2/V.s$, 40 $cm^2/V.s$ and 2×10^{17} cm^{-3}, respectively. Although the electron velocity appears to be a linear function of the electric field, it is in fact only nearly linear for low lateral fields. As the electric field increases the electron velocity gradually deviates from the linear dependence on electric field and at sufficiently high fields, becomes almost constant, independent of the electric field.

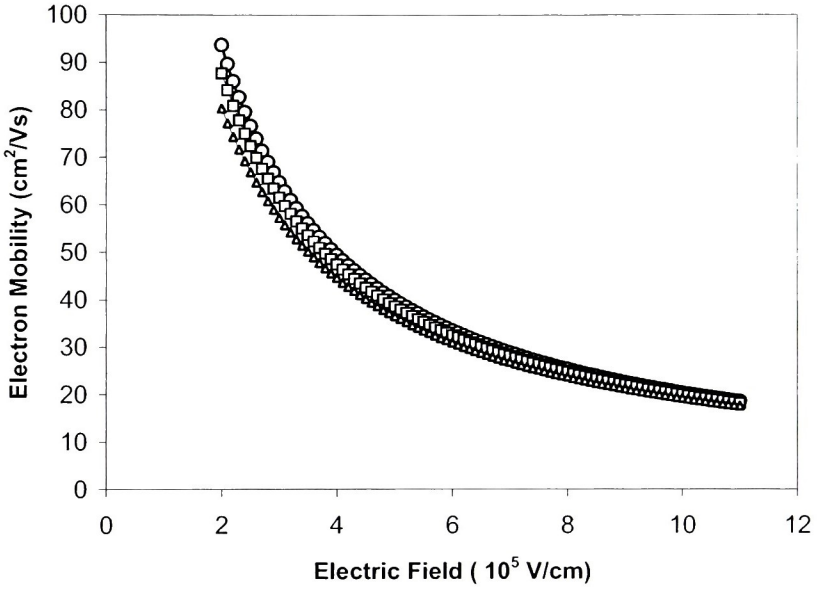


Fig. 2-4. A plot of mobility vs. electric field with β = 0.86(Δ), β = 1.0(□) and β = 1.2(O).

This phenomenon is called velocity saturation and is denoted by v_{sat}. Velocity saturation is incorporated into equation (2-5) by modifying the mobility such that it becomes a function of the electric field. Various empirical models have been proposed which are able to predict the electric field dependence of the mobility. The one that has been used in this work is [36]:

$$\mu = \frac{\mu_0}{\left\{1 + \left(\frac{\mu_0 |E|}{v_{sat}}\right)^{\beta}\right\}^{1/\beta}}, \qquad (2\text{-}7)$$

where E is the lateral electric field and v_{sat} is the saturation velocity of the electrons. β is a constant which is very close to unity for 4H-SiC. Monte-Carlo simulation results yield values of 0.84 [32] for the value of β while experimental observations yield a value of 1.2 [37]. For the purpose of this present work, a value of 1 has been used for β. It is evident from Fig. 2-4 that this value of β is sufficiently accurate. For 4H-SiC the value of the saturation velocity is 2.07×10^7 cm/s. The velocity of the electrons is plotted against the electric field in Fig. 2-5. It can be seen that the velocity of the electrons increases linearly at low fields and then saturates at a velocity of 2.07×10^7 cm/s at excessively high electric fields.

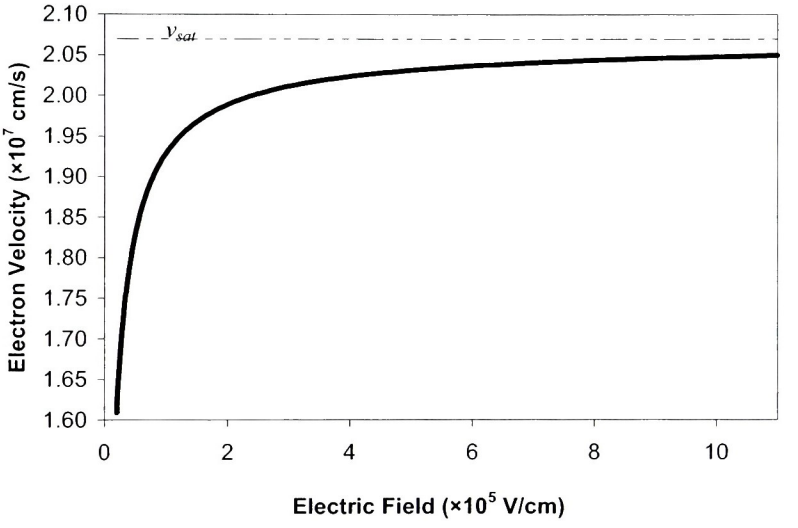
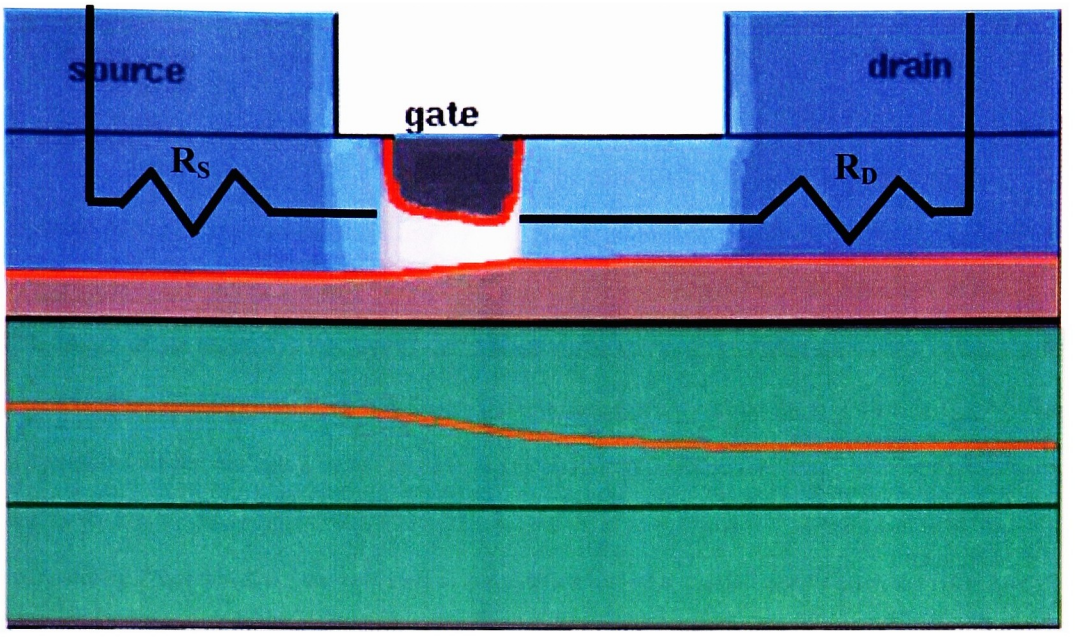


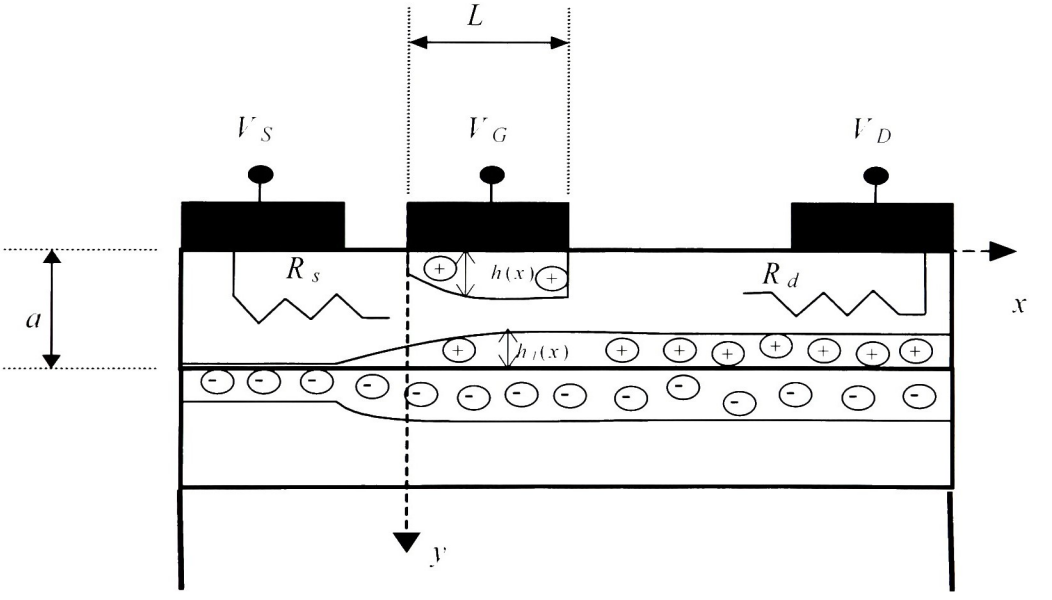
Fig 2-5. The electron velocity as a function of the electric field (thick line), and the saturation velocity is shown by a dashed line.

2.5 Current Equations Before Pinch-off

In the MESFET model considered in this work, various additions have been made to the simple MESFET structure that is shown in Fig. 2-1. Fig. 2-6 (a) has been split up into four sections.



(a)



(b)

Fig. 2-6. A schematic representation of the MESFET cross-section that is used for *I-V* modeling. Fig. 2-2 has been split up to show the physical locations of the drain/source resistances, and the depletion regions that have been modeled in the *I-V* relationships (a), and a schematic diagram representing the cross section that is to be used for modeling the *I-V* relations.

The bottom section comprising the buffer region and the SI substrate has not been modeled. The effect of the buffer region however has been modeled by the depletion region in the channel, shown in the channel in a shade of orange. The part of the channel beyond the gate (shown in the channel in a shade of blue) is modeled by the source and the drain resistances. The corresponding schematic of the cross-section of the MESFET is shown in Fig. 2-6 (b).

The length of the channel is the part of the channel under the gate. The thickness of the channel is a, the width is W and the length is L. R_S and R_D are the source and drain resistances as shown in Fig. 2-6. Due to the presence of the current I_D in the channel, the potential drop across the source and the drain resistances are $I_D R_S$ and $I_D R_D$, respectively. Thus, the potentials at $x = 0$ and $x = L$ are $I_D R_S$ and $V_D - I_D R_D$, respectively. Equation (2-1) may be used in conjunction with the channel potentials at the source and drain end of the channel (just mentioned) to obtain an expression for the height of the depletion region under the gate due to the Schottky gate as:

$$\begin{aligned} h_S &= \sqrt{\frac{2\varepsilon}{qN_D}\left[-V_G + V_{bi} + I_D R_S\right]} \\ h_D &= \sqrt{\frac{2\varepsilon}{qN_D}\left[-V_G + V_{bi} + V_D - I_D R_D\right]} \end{aligned}, \tag{2-8}$$

and the height of the depletion region formed at the buffer-channel junction, at the source and the drain ends of the channel may be obtained by solving equation (2-3) in conjunction with the channel potentials at the end of the channel to obtain:

$$\begin{aligned} h_{1S} &= \left[\frac{N_A}{N_A + N_D}\right]\sqrt{\frac{2\varepsilon}{q}\frac{N_A + N_D}{N_D N_A}\left[U_{bi} + I_D R_S\right]} \\ h_{1L} &= \left[\frac{N_A}{N_A + N_D}\right]\sqrt{\frac{2\varepsilon}{q}\frac{N_A + N_D}{N_D N_A}\left[U_{bi} + V_D - I_D R_D\right]} \end{aligned}. \tag{2-9}$$

At point x in the channel, the equation for the drain current is given by:

$$I_D = qWn(x)\mu(E)E(x)[a - h(x) - h_1(x)], \tag{2-10}$$

where $\mu(E)$ is the mobility of the electrons for the electric field E, $n(x)$ is the charge concentration of the channel and is given by N_D, the doping concentration of the channel, and a is the thickness of the channel. Using the expression for mobility (equation (2-7)) in equation (2-10) leads to the expression:

$$I_D = qWN_D \frac{\mu_0}{1 + \frac{\mu_0 E}{v_{sat}}} E(x)[a - h(x) - h_1(x)]. \tag{2-11}$$

The electric field at point x in the channel is given by the negative spatial derivative of the potential at that point. Since the magnitude of the current is being sought at this point, the negative sign is neglected. $h(x)$ and $h_1(x)$ may be substituted into equation (2-11) using equations (2-1) and (2-3) and the resultant differential equation solved to obtain the value of the channel current. Boundary conditions are those of the channel potential at the two ends of the channel and the depletion region depths at the two ends of the channel as given by equations (2-8) and (2-9). The equation for the drain current for the linear region is given by the equation:

$$I_D = \frac{qWN_D\mu_0 v_{sat}}{v_{sat}L + \mu_0[V_D - I_D(R_S + R_D)]}\left\{a[V_D - I_D(R_S + R_D)] - \right.$$
$$\left. -\frac{2}{3}\frac{qN_D}{2\varepsilon}\left[h_D^3 - h_S^3\right] - \frac{2}{3}\frac{qN_D}{2\varepsilon}\frac{N_A + N_D}{N_A}\left[h_{1L}^3 - h_{1S}^3\right]\right\} \tag{2-12}$$

2.6 Pinchoff

As the gate bias or the drain bias is decreased, the height of the depletion region (especially at the drain end of the channel) slowly increases until the channel under the gate is pinched off. Also, it is assumed that pinchoff occurs after velocity saturation. This is a reasonable assumption for a channel thickness of about

2 μm and a doping concentration of about $10^7 cm^{-3}$[36]. Under these circumstances, the velocity of the electrons are v_{sat}, and the corresponding electron current is given by:

$$I_{Dsat} = qWN_D v_{sat}\left[a - \sqrt{\frac{2\varepsilon}{qN_D}\left[-V_G + V_{bi} + V_{Dsat} - I_{Dsat}R_D\right]} - \sqrt{\frac{2\varepsilon}{qN_D}\frac{N_A}{N_A + N_D}\left[U_{bi} + V_{Dsat} - I_D R_D\right]}\right], \quad (2\text{-}13)$$

where I_{Dsat} and V_{Dsat} are the saturation current and saturation voltage respectively. Pinchoff occurs when the saturation current given by the equation (2-13) equals the linear current given by the equation (2-12). For obtaining the values of V_{Dsat} and I_{Dsat}, equations (2-12) and (2-13) need to be solved simultaneously, at each value of V_D. For the linear region, the current calculated by the equation (2-12) is always less than the current calculated by the equation (2-13). At the point of pinchoff (V_{Dsat}) however, the current (I_{Dsat}) calculated using the equation (2-12) equals that calculated using the equation (2-13).

2.7 Beyond Pinchoff

Fig. 2-7 may be used for visualizing the model used for arriving at the saturation current equations beyond pinchoff. Beyond pinchoff, the depletion region under the gate encroaches more and more into the channel and the point at which pinchoff occurs shifts toward the source. The effective length of the linear part of the channel decreases. This is termed channel-length modulation and is responsible for the finite slope of the *I-V* plot of saturation. In Fig. 2-7 for example, the point at which pinchoff occurs has shifted to a point $x = L_1$. It is assumed that for the rest of the region beyond point L_1, the channel opening remains of the same thickness.

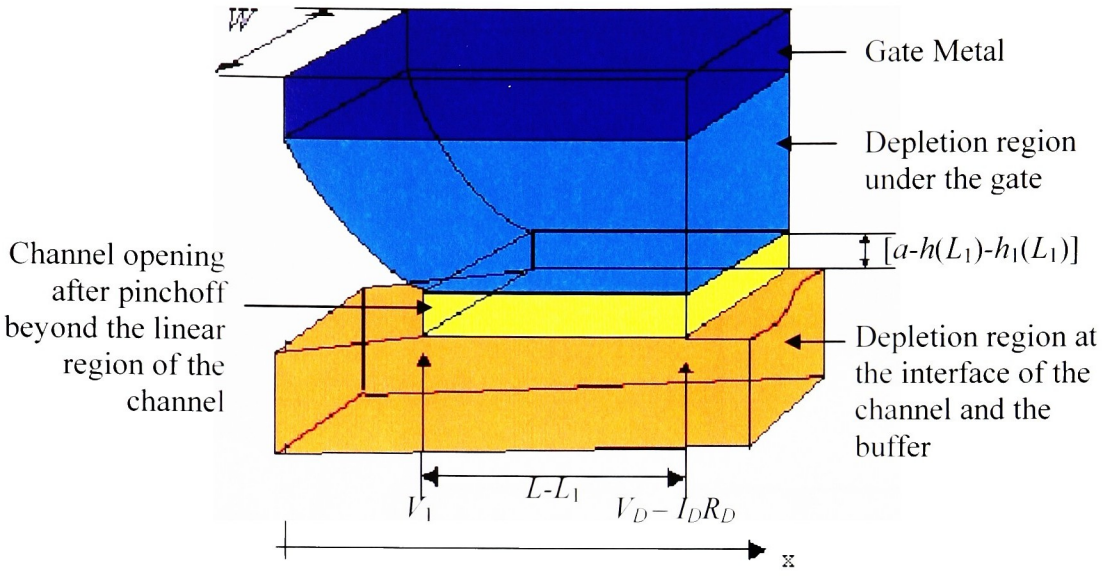


Fig. 2-7. A schematic diagram of the channel after pinchoff. Note that saturation has been greatly exaggerated, and the structure greatly simplified for the purpose of visualization.

Let the length of the channel at which pinchoff occurs be L_1. Let the potential at this point be V_1. The current in the linear part of the channel may be obtained by solving the differential equation (2-11) over the length $x = 0$ to $x = L_1$. Solving the differential equation leads to:

$$I_D = \frac{qWN_D\mu_0 v_{sat}}{v_{sat}L_1 + \mu_0[V_1 - I_D R_S]}\left\{a[V_1 - I_D R_S] - \frac{2}{3}\frac{qN_D}{2\varepsilon}\left[h_{L1}^3 - h_S^3\right] - \frac{2}{3}\frac{qN_D}{2\varepsilon}\frac{N_A + N_D}{N_A}\left[h_{1L1}^3 - h_{1S}^3\right]\right\}, \quad (2\text{-}14)$$

where the equations for h_{L1} and h_{1L1} are given by:

$$h_{L1} = \sqrt{\frac{2\varepsilon}{qN_D}\left[-V_G + V_{bi} + V_1\right]}$$
$$h_{1L1} = \left[\frac{N_A}{N_A + N_D}\right]\sqrt{\frac{2\varepsilon}{q}\frac{N_A + N_D}{N_D N_A}\left[U_{bi} + V_1\right]}. \quad (2\text{-}15)$$

Assuming that the height of the depletion layer under the gate beyond the length $x = L_1$ is constant, the current through this region is given by:

$$I_D = qWN_D v_{sat}\left[a - \sqrt{\frac{2\varepsilon}{qN_D}\left[-V_G + V_{bi} + V_1\right]} - \sqrt{\frac{2\varepsilon}{qN_D}\frac{N_A}{N_A + N_D}\left[U_{bi} + V_1\right]}\right]. \quad (2\text{-}16)$$

At this moment, three variables are unknown. These are I_D, V_1 and L_1. Thus, it is necessary to have another equation for solving the current. This equation may be obtained by a two-dimensional analysis of the potential in the depletion region under the gate. The potential under the gate is given by the equation

$$\frac{\partial^2 V(x,y)}{\partial x^2} + \frac{\partial^2 V(x,y)}{\partial y^2} = -\frac{qN_D}{\varepsilon}, \quad (2\text{-}17)$$

and using the gradual channel approximation,

$$\frac{\partial^2 V(x,y)}{\partial y^2} = -\frac{qN_D}{\varepsilon}. \quad (2\text{-}18)$$

For the solution, a new reference frame is selected at $x' = x - L_1$, and a new potential function W is created such that

$$W(x',y) = V(x,y) + \frac{qN_D}{2\varepsilon}y^2. \quad (2\text{-}19)$$

The general form of the solution of the differential-equation (2-18) is given by [36]

$$W(x',y)=\left(Ae^{kx'}+Be^{-kx'}\right)\left(C\cos(ky)+D\sin(ky)\right)+Ex'y+Fx'+Gy+H\,. \quad (2\text{-}20)$$

The boundary conditions for the solution of (2-20) are

I. $W(x',y)\big|_{y=0}=-\left(-V_G+V_{bi}\right)$,

II. $\left.\dfrac{\partial V(x',y)}{\partial y}\right|_{\substack{x=L_1\\y=h_{1L1}}}=0$, (2-21)

III. $\left.\dfrac{\partial W(x',y)}{\partial x'}\right|_{\substack{x'=0\\y=h_{1L1}}}=\left.\dfrac{\partial V(x',y)}{\partial x}\right|_{\substack{x=L_1\\y=h_{1L1}}}=E_S$, and

IV. $V(x,y)\big|_{\substack{x=L\\y=h_{1L1}}}=V_D-I_DR_D$.

The first boundary condition represents the fact that the potential at any point in the depletion region closest to the gate is equal to the gate voltage and the built-in potential, and is independent of the lateral position of the point under consideration. The second boundary condition states that the vertical component of the electric field at the edge of the depletion region is zero. All the vertical electric field that ends at the gate originates at an ionized dopant ion in the depletion region. Thus, below the depletion region, no vertical electric field may exist. The third boundary condition is the mathematical representation of the assumption that velocity saturation occurs before pinchoff. Here, E_S represents the saturated electric field.

The calculation of E_S proceeds as follows. Theoretically, the value of the electric field at which velocity saturates is infinite. For the purpose of practicality, it is assumed that for a sufficiently large amount of electric field (E_S), the velocity of the electrons is sufficiently close to the actual saturation velocity. For example, if the actual velocity of the electrons is ξv_{sat} (where ξ is very close to 1), then by equation (2-5),

$$\xi v_{sat} = \mu(E_S)E_S\,, \tag{2-22}$$

and substituting the value of the low-field mobility in equation (2-7),

$$\xi v_{sat} = \frac{\mu_0}{1+\dfrac{\mu_0 E_S}{v_{sat}}} E_S\,. \tag{2-23}$$

Solving for E_S,

$$E_S = \frac{v_{sat}}{\mu_0}\left(\frac{\xi}{1-\xi}\right). \tag{2-24}$$

The final boundary condition represents the fact that at the drain end of the channel, the potential is equal to the difference between the drain bias and the drop that appears across the channel. Using boundary conditions given by equations (2-21), the differential equation (2-18) may be solved as:

$$V_D - I_D R_D = \frac{2E_S h_{L1}}{\pi}\sinh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right) + V_1\,. \tag{2-25}$$

Now, equation (2-14), (2-16) and (2-25) may be solved simultaneously to obtain the value of the current after pinchoff has taken place.

Chapter 3

Trapping and Thermal Effects in the SiC MESFETs

3.1 Introduction

The *I-V* characteristics described in Chapter 2 are ideal. SiC based devices are plagued by traps and the ideal *I-V* characteristics are inadequate to explain experimental results. In the following sections, the theoretical origin and nature of these non-idealities and their effects on the *I-V* characteristics and modeling issues will be described. Two types of traps have been identified: surface traps and substrate traps. Surface traps cause the drain resistance to become drain bias dependent and result in the decrease of transconductance. The substrate traps decrease the channel electron concentration by capturing electrons and result in current slump in the *I-V* characteristics. Although SiC is a popular material for its high thermal conductivity, devices based on SiC suffer significantly from self-heating effects at high power density applications [38]. For accurate device modeling, both trapping and self-heating effects need to be modeled. Thermal effects result in a change in the transport parameters leading to a drop in the channel current concentration at high power levels.

Section 3.2 describes trapping effects and the methods to model their effects. Thermal effects are described in Section 3.3. The parameters in the *I-V* relationship that are dependent upon temperature are described in Section 3.4, along with their temperature dependencies. The temperature dependency of the thermal conductivity of SiC is explained in Section 3.6. Finally the method of solution for calculating the drain current is explained in Section 3.7.

3.2 Trapping Effects

Ideal semiconductors are devoid of energy levels in the energy gap between the conduction and the valence band. In practice, however, one or more energy-states are present in the energy gap between the conduction and the valence bands. Sometimes these levels are intentionally introduced. Gold is introduced in silicon for example to succor recombination [39]. Vanadium is introduced in SiC to create SI properties [24]. At other times, their presence is not desired, since they form trapping centers responsible for unintentional electron capture. Trap levels are present in SiC for various reasons. Some of them are discussed below.

3.2.1 Intrinsic Defects in 4H-SiC

Intrinsic defects are primarily of three kinds. First, there are intrinsic defects with associated bound-excitons near the bandgap region. The second type of defects is seen in high-temperature chemical vapor deposition (HTCVD) substrates. It is believed that these deep defects are responsible for the SI characteristics of HTCVD SiC, since these are devoid of vanadium. The third type of defect is the intrinsic structural defect caused due to stacking faults and dislocations [40].

3.2.2 Defects Introduced by Vanadium

Vanadium is introduced in SiC in physical vapor transport (PVT) substrates to produce SI characteristics. This introduces energy states at 1.6eV [40], 0.7eV [40], 0.97eV [2] and 1.17eV [2] below the conduction band. The level at 1.6eV below the conduction band is nearly at the center of the energy gap and is responsible for imparting the SI characteristics by forming recombination centers. Another deep level is observed at 1.1eV below the conduction band in SiC grown by HTCVD and not doped using vanadium.

Although various theories have been proposed, the origin of the deep-level at 1.1eV below the conduction band is still unknown [40].

3.2.3 Defects Introduced by Dopants like Nitrogen and Aluminum

Nitrogen is used for both n- and p-type doping in SiC. Nitrogen introduces a trap level at 0.51eV [40] above the valence band and is attributed to dopant-defect complex. Ion-implantation results in intrinsic defects at 1.9eV, 1.3eV, 0.9eV, 0.7eV and 0.5eV below the conduction band [41]. The implantation of Al introduces a level at 1.43eV below the conduction band [42].

Intrinsic defects and defects introduced by nitrogen and vanadium result in deep-level traps.

3.2.4 Surface Traps

Apart from these deep-level traps, surface traps present at the surface further deteriorate the MESFET performance. The presence of an oxide layer further exacerbates the defects at the surface [43]. Three dominant surface trapping levels have been observed at 0.68eV, 0.77eV and 0.89eV [22] above the valence band. A summary of the type of traps observed in the SiC MESFET is shown in Table 3-I.

Table 3-I: A summary of the locations and densities of various types of traps observed in the 4H-SiC MESFET [22].

Trap Number	Trap Location (eV)	Trap Density (cm^{-3})	Capture Cross Section (cm^2)
1	$E_V + 0.51$	1×10^{16}	6.4×10^{-15}
2	$E_V + 0.60$	1×10^{14}	3.2×10^{-16}
3	$E_V + 0.68$	1×10^{15}	8.3×10^{-16}
4	$E_V + 0.77$	1×10^{15}	1.2×10^{-15}
5	$E_V + 0.89$	1×10^{15}	9.0×10^{-15}

Traps for electrons exist both at the surface and the substrate. The trapping and detrapping of electrons is shown in the Fig. 3-1. A number of traps exist at the surface. These have a propensity for capturing and retaining electrons. The presence of a nitride layer mitigates the propagation of electrons from the gate metal to the traps, but do not prevent the traps from capturing electrons, however, when sufficient positive bias is applied between the drain and the gate. Thus the depletion region below the gate extends beyond the

gate due to the presence of these captured electrons. This work models this physical phenomenon by incorporating the effects of the depletion length in the drain resistance.

3.2.5 Modeling Electron Capture and Release in Bulk Traps

The schematic diagram of the crosssection of the MESFET is shown in Fig.3-1. Initially, when no drain bias is applied (as shown in Fig. 3-1. (a),) the depletion region throughout the channel is of constant thickness.

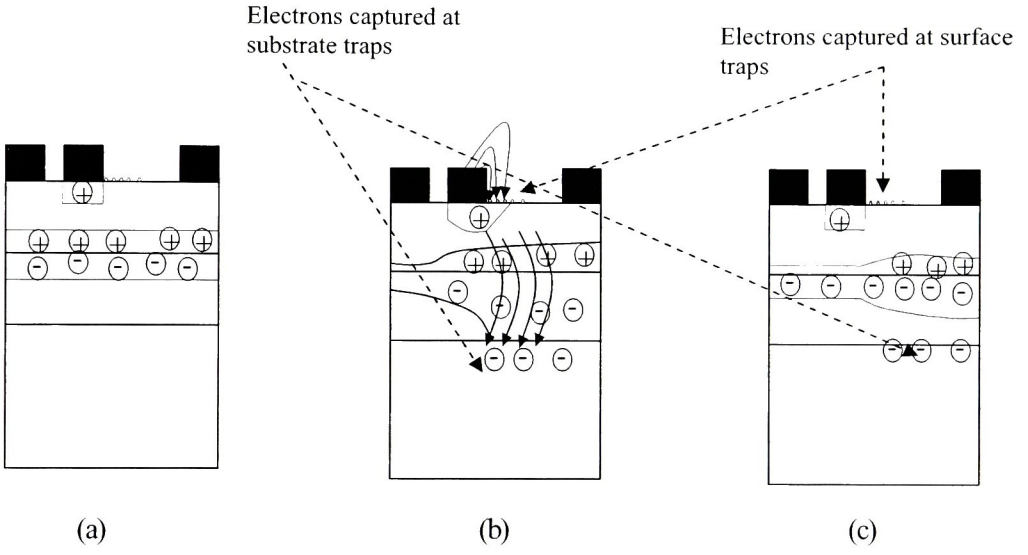


Fig. 3-1 A schematic diagram showing the cross section of a MESFET depicting electron capture and release from bulk and surface traps. Fig. 3.1 (a) depicts depletion regions between at the channel-buffer and the gate-channel interface in the absence of drain voltage and at a time when electrons are absent from the traps, (b) depicts the condition when a large drain bias is applied resulting in the capturing of electrons by traps, and (c) depicts the state of the depletion regions just after the removal of drain voltage after traps have been captured.

As the drain bias is increased, the depletion region towards the drain is increased until the drain end of the buffer layer is fully depleted. Further increase in drain bias allows electrons from the channel to travel right through the buffer layer and reach the SI substrate. These electrons get captured in the traps present in the

substrate (as shown in Fig. 3-1. (b)). In the next sweep, the drain voltage is dropped to zero and the gate voltage is changed. At this point, although the drain end is not biased, electrons that were previously captured by the substrate traps have not been released yet. Thus the depletion region between the channel and the buffer is thicker in the drain side as shown in Fig. 3-1. (c). At this point the de-trapping process starts. The de-trapping of electrons depends primarily on the effective lifetime of the trapped electrons. As the voltage increases in the following sweep, the traps are progressively de-trapped, and the current collapse disappears after some voltage. The rate at which the bulk traps are de-trapped depends upon the trap activation energy, capture cross section, effective mass of the electrons, among others. Thus, in the *I-V* characteristics, the voltage at which the de-trapping is complete is entirely dependent on the rate at which the drain voltage is changed. Let the concentration of the traps be N_T. Assuming that when the trapping process occurs, all of the traps the filled and the concentration in the channel reduces to $N_{DActual} - N_T$. At a particular voltage (V_A) de-trapping starts and by the time the drain voltage rises to V_B, all electrons have been de-trapped. Between the voltages V_A and V_B the channel concentration monotonically increases from $N_{DActual} - N_T$ to $N_{DActual}$. A linear increase in the channel concentration from concentration N_A to concentration N_B is given by

$$N_D = \begin{cases} N_{DActual} - N_T & V_D < V_A \\ N_{DActual} - N_T + \dfrac{N_T(V_D - V_A)}{(V_B - V_A)} & V_A < V_D < V_B \\ N_{DActual} & V_B < V_D \end{cases}, \tag{3.1}$$

but this is a completely arbitrary choice. This function might be a exponentially interpolated value or even a polynomial function of some kind. The linear increase however was sufficient in explaining the trapping characteristics.

3.2.6 Source and Drain Resistance Modeling

Source and drain resistances may be obtained by measurement, but they are not of much use to the circuit designer. Analytical models that are able to predict the nature of the source and drain resistance are very important. Although the bias dependent source and drain resistances are derived empirically in this work

since surface and substrate trap concentrations and their behavior has not been fully modeled at this time, a novel approach for the calculation of the drain resistance is described. Both the source and the drain resistances are composed partly of the metal contact resistance, and partly of the resistance of the semiconductor bulk present before and after the length of the gate. Since the number of electrons trapped at the surface is a function of the gate and the drain biases, the height of the depletion region beyond the gate is also some function of the gate and the drain bias. The source end of the device is generally unaffected by the gate bias as much as the drain end of the device is affected since the potential between the gate and the source is generally not as much as that between the gate and the drain. The metal contact resistance is taken to be a constant, both for the source and the drain. This varies from device to device, however, depending upon the dimensions of the drain and the source contacts and the resistivity of the constituting materials. There is further resistance due to the highly doped semiconductor material that exists between the drain end of the channel and the drain and the source end of the channel and the source. For the source, the resistance of the channel between the source and the gate is assumed constant. For the drain, the resistance would generally be a highly nonlinear function of the gate and the drain voltages. The drain resistance is modeled as shown in Fig. 3-2. The density of trapped electrons at the surface states decreases towards the drain

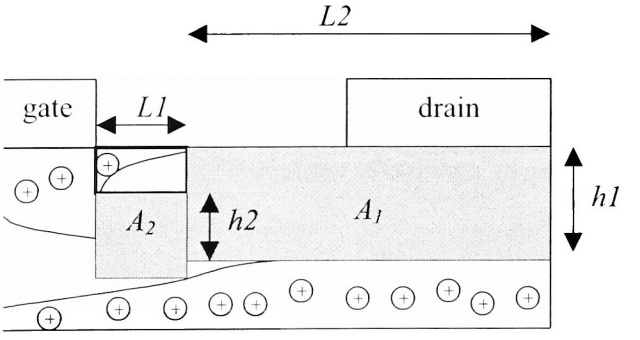


Fig. 3-2. A schematic representation of the block approximation of the resistive components of the channel that result in drain resistance augmentation with increasing drain voltage.

. The channel region between the drain and the gate is divided up into two regions A_1 and A_2 as shown. A_1 constitutes the part of the channel over which trapped electron concentration in the surface traps is almost negligible. Over A_2 the depletion region due to the surface traps has been considered. The region above A_2 is a step approximation of the depletion region formed due to the presence of the electrons captured by surface traps. That below the regions labeled A_1 and A_2 is a step approximation for the depletion region formed at the junction between the channel and the buffer region. The height of the region A_2 (i.e. *h2*) is a function of the gate and drain voltages, while the height of the region A_1 (i.e. *h1*) is a function of the drain voltage alone. Thus,

$$R_{A1} = f_1(V_G, V_D), \tag{3.2}$$

$$R_{A2} = f_2(V_D), \text{ and} \tag{3.3}$$

$$R_D = R_{A1} + R_{A2} + R_0 = R_0 + f_1(V_G, V_D) + f_2(V_D), \tag{3.4}$$

where R_0 is the resistance representing the contact resistance used for the formation of ohmic contact. R_{A1} and R_{A2} are given by the expressions

$$R_{A1} = \frac{1}{q\mu_n n}\left(\frac{L1}{Wh1}\right), \text{ and} \tag{3.5}$$

$$R_{A1} = \frac{1}{q\mu_n n}\left(\frac{L2}{Wh2}\right) \tag{3.6}$$

respectively.

3.3 Thermal Effects

A major area in which the SiC MESFET is predicted to be useful is in power applications. The inherent nature of power devices requires these devices to be able to dissipate large amounts of power. Self-heating (also known as Joule heating) is a natural consequence. Although the thermal conductivity of SiC is large

(close to that of copper [2]) the temperature of the channel is significantly higher than the temperature of the backside contact in most practicable MESFET structures, as shall be shown later in this chapter. The change in temperature entails a change in the various transport parameters which finally translates to a change in the *I-V* characteristics. Thus, it becomes important to model the self-heating effects of these devices for effectively modeling the *I-V* characteristics.

3.4 Temperature-Dependent Variables in the *I-V* Equations

In this section the variables in the current equation that are temperature-dependent are described. Incorporation of the temperature dependence of the variables in the current equations (thus rendering the *I-V* equations temperature dependent) is the first step toward the modeling of self-heating effects. Generally, three terms in the *I-V* equations need modification: the low-field mobility, saturation velocity and the free carrier concentration. As the temperature increases, the mobility and the saturation velocity decreases. This is due to the fact that electron-phonon interactions increase with increasing temperature. This causes a general reduction in the current density. Further, in the case of incomplete ionization of carriers, any increase in temperature result in further ionization and thus greater channel concentration, resulting in greater current. This is true only in the case of degenerate semiconductors and in not of much use in the present discussion. A quantitative description of the temperature dependencies of each of the parameters are provided in the following sections.

3.4.1 Effect of Temperature on Low-Field Mobility

The equation for the low-field mobility for SiC is:

$$\mu_0 = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left(\frac{N}{N_{Ref}} \right)^{\alpha}}, \tag{3-7}$$

where $\mu_{\min}$ is the minimum value of the low-field mobility, $\mu_{\max}$ is the maximum value of the low-field mobility, N_{Ref} is the reference concentration, N is the doping concentration and α is an exponential

parameter for incorporating the doping dependence of the low-field mobility. All of the variables other than α are temperature dependent, and their temperature dependence is given by the equations shown below [35]:

$$\mu_{\max} = 950\left(\frac{T}{300}\right)^{-2.4} \text{ cm}^2/\text{Vs},$$

$$\mu_{\min} = 40\left(\frac{T}{300}\right)^{-0.5} \text{ cm}^2/\text{Vs, and} \tag{3-8}$$

$$N_{ref} = 2\times10^{17} \times \left(\frac{T}{300}\right) \text{cm}^{-3}.$$

The temperature dependencies of these parameters are shown in Fig. 3-3 and the resulting variation in the low-field mobility is shown in Fig. 3-4.

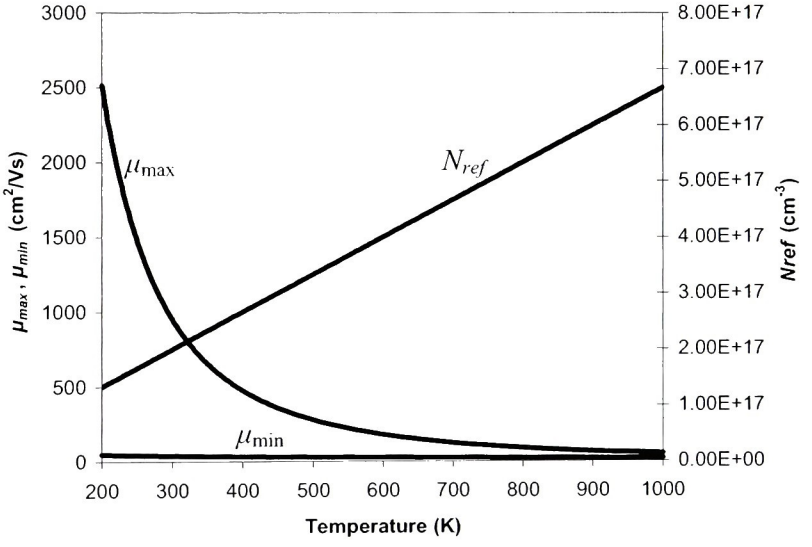


Fig. 3-3. The variation of the maximum (μ_{max}), minimum (μ_{min}) low-field mobilities and the reference concentration (N_{ref}).

As can be seen from Fig. 3-3, both μ_{max}, and μ_{min} decrease with temperature. μ_{max} decreases from a value of about 2500 cm^2/Vs at a temperature of 200 K to a value of about 50 cm^2/Vs at 1000 K. N_{Ref} on the other

hand, increases with temperature. It increases linearly from a concentration of 1.33×10^{17} cm^{-3} at 200 K to a concentration of 6.67×10^{17} cm^{-3} at 1000 K. All these factors result in a decrease in the mobility of the carriers as seen in Fig. 3-4.

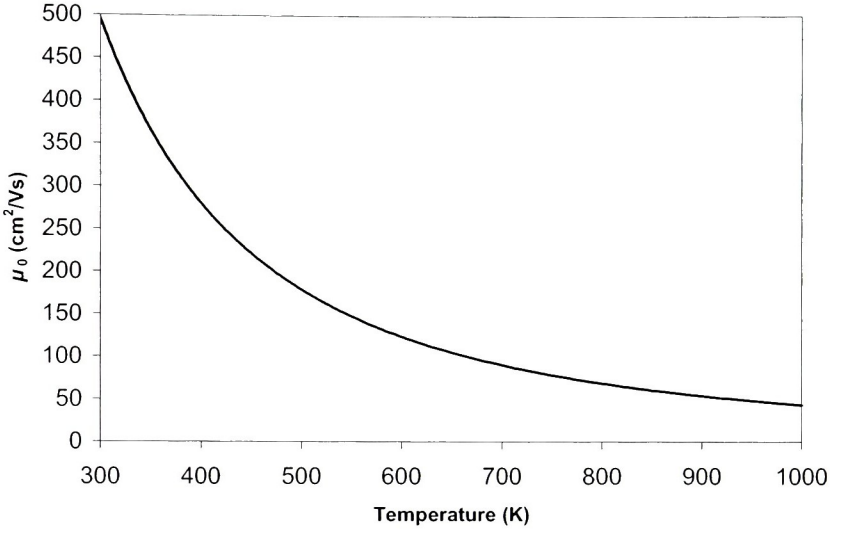


Fig. 3-4. The variation of low-field mobility (μ_0) as a function of the temperature (N = 2×10^{17} cm^{-3}, $\alpha = 0.5$).

Fig. 3-4 depicts the change in the value of the low-field mobility with respect to the change in temperature. As can be seen from the figure, the value of the mobility decreases with temperature. This mobility model incorporates the decrease in mobility resulting from the introduction of the dopants. At 300 K the mobility of the electrons are about 500 cm^2/Vs (and not 1000 cm^2/Vs, which is the bulk mobility), corresponding to a doping concentration of 2×10^{17} cm^{-3}. At 1000 K, this value of mobility decreases to 50 cm^2/Vs. The field-dependent mobility is given by the equation:

$$\mu = \frac{\mu_0}{\left(1+\left(\frac{\mu_0 \times E}{v_{sat}}\right)^{\beta}\right)^{\frac{1}{\beta}}}. \qquad (3\text{-}9)$$

Assuming that $\beta = 1$ and a constant saturation velocity ($v_{sat} = 2 \times 10^7$ cm/s), the plot of the field-dependent mobility with respect to the electric field and temperature is shown in Fig. 3-5. It can be seen that the value of the field-dependent mobility varies little at high electric fields, even for high temperatures, while it varies significantly when the electric field is low. For example, for a lateral field of 2×10^5 V/cm, there is a 70% change in the value of the field dependent mobility as the temperature changes from 200K to 1000K. For a lateral field of 12×10^5 V/cm however, the corresponding change in the value of the field-dependent mobility is only 35%, for the same temperature variation.

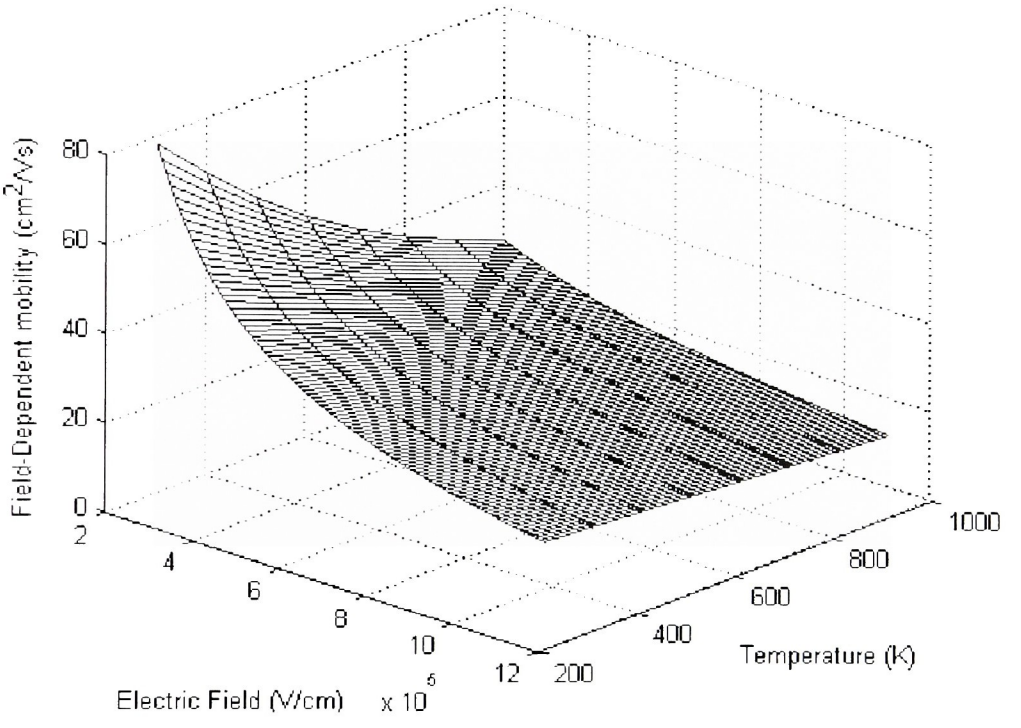


Fig. 3-5. The variation of the field-dependent mobility with temperature and electric field ($N = 2\times 10^{17}$ cm^{-3}, $\alpha = 0.5$).

Thus, the temperature dependence of current due to the temperature dependence of mobility is important only in the linear region of operation. In the saturation region, when the electric field is high, the

temperature dependence of current is strongly dependent upon the temperature dependence of saturation velocity, which is taken up in the next section.

3.4.2 Effect of Temperature on Saturation Velocity

Current theory in not sufficiently mature to predict accurately the temperature dependence of saturation velocity [38], since the uncertainty that affects the coupling constant values remain very large. The variation of saturation velocity with temperature is the one used by Royet *et al.* [38]:

$$v_{sat} = \frac{2\hbar u_l}{\sqrt{3\pi}} \frac{D}{\Xi} \left(m_t k_B T + \frac{\hbar m_t u_l}{2\omega_0} \frac{\exp\left(\frac{\hbar\varpi_0}{k_B T}\right)+1}{\exp\left(\frac{\hbar\varpi_0}{k_B T}\right)-1} \left(\frac{D}{\Xi}\right)^2 \right)^{-1/2} . \qquad (3\text{-}10)$$

where u_l is the velocity of sound in SiC taken to be 13300 m/s, D is the coupling constant, Ξ is the acoustic deformation potential, ω_0 is the optical phonon energy and m_t is the transverse effective mass of the electron. The values of these quantities are shown in Table 3-2.

Table 3-2: Numerical values for calculating the saturation velocity [38].

Parameter	Value
Velocity of sound in SiC (u_l)	13,300.00 m/s
Coupling Constant (D)	6.5 x 10^9 eV/cm
Acoustic deformation potential (Ξ)	15 eV
Optical phonon energy (ω_0)	$\hbar\varpi_0$ = 120 meV
Transverse effective mass (m_t)	0.42 m_0

A plot of the variation of the normalized value of the saturation velocity with temperature is plotted with temperature in Fig. 3-6. The normalization has been carried out such that the value of the normalized saturation velocity is 1 at 300 K. As seen in Fig. 3-6 the saturation velocity decreases by about 30% when the temperature changes from 300K to 600K. Since the current in the saturation region is directly proportional to the saturation velocity, it may be seen that this change in the magnitude of saturation velocity is significant even for a small change in the channel temperature, and needs to be incorporated for properly modeling thermal effects.

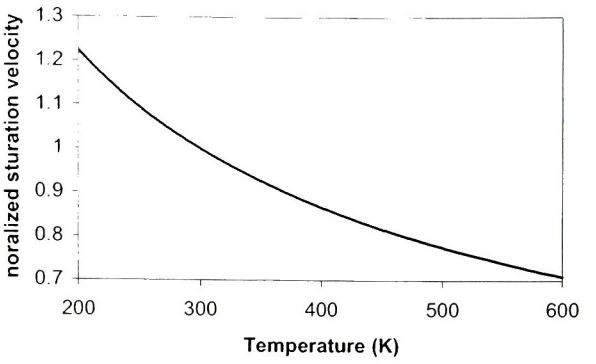


Fig. 3-6. The variation of a normalized saturation velocity with respect to temperature.

3.4.3 Effect of Temperature on Free-carrier Concentration

It has been proposed that the variation of the charge density with temperature in a SiC bulk necessitates the numerical solution of the neutrality equation:

$$n = N_A + \frac{N_{D1}}{1 + \frac{2n}{N_C(T)} \exp\left(\frac{E_{D1}}{k_B T}\right)} + \frac{N_{D2}}{1 + \frac{2n}{N_C(T)} \exp\left(\frac{E_{D2}}{k_B T}\right)} \tag{3-11}$$

However, since manufacturing processes are yet immature, a significant number of majority carriers interact with surface and substrate states in a complex manner. It is further assumed that the theoretical variation of the majority carrier concentration with temperature is insignificant compared to the temporal of channel electron concentration resulting from surface and substrate traps. Thus the variation of channel electron concentration with respect to temperature has been neglected in this work.

3.5 Temperature Dependence of the Thermal Conductivity of SiC

Although the thermal conductivity of SiC is very high compared to the thermal conductivity of other semiconductor materials, it is not constant with temperature. The thermal conductivity of SiC is as good as copper only at low temperatures. As the temperature increases, the thermal conductivity of SiC starts decreasing. Thus, at higher temperatures, the ability of SiC to dissipate heat decreases significantly. If this

in not modeled into the heat-flow equation, the correct thermal profile can not be obtained. This section describes the variation of the thermal conductivity of SiC with respect to temperature. The variation of thermal conductivity on temperature is given by the relation [38]:

$$\kappa(T) = \kappa_{00}\left(\frac{T}{300}\right)^{-1.5} \tag{3-12}$$

where κ_{00} is the thermal conductivity of SiC at 300K having a value of 3.2 W/cm/K, and T is the temperature in K of the bulk. The variation of the normalized thermal conductivity with temperature is shown in Fig. 3-7:

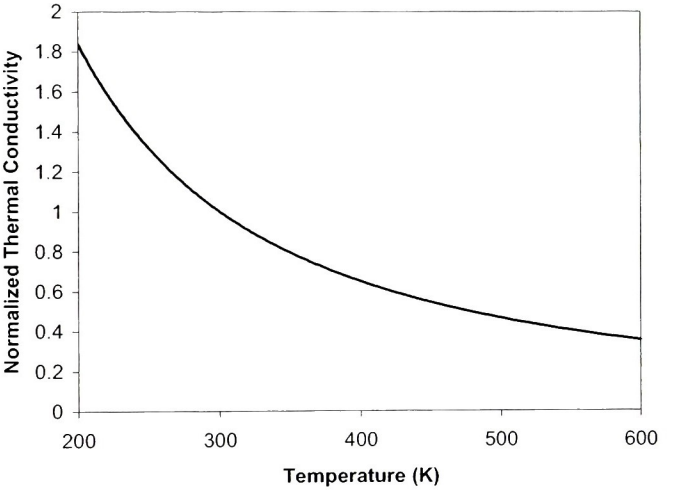


Fig. 3-7. The variation of the normalized thermal conductivity with respect to temperature.

Again, the normalization has been carried out so that the normalized thermal conductivity is 1 at 300 K. As can be seen, the thermal conductivity at 600K reduces to about 40% of its value at 300K. Thus, it is imperative that any temperature-dependence of the I-V equations takes care of the variation of the thermal conductivity of the SiC bulk with temperature.

3.6 Power Dissipation Equations Representing Thermal Equilibrium

Equation (3-12) may be linearized using Krickoff's transformation to:

$$\Delta T = \frac{1}{\kappa(T_0)} \int_{T_0}^{T} \kappa(T') dT' \tag{3-13}$$

Approximating the channel to a half-cylinder, the temperature difference between the backside contact and the channel is going to be given by [38]:

$$\Delta T = \frac{P_{diss}}{\pi \kappa(T_0) W} \ln\left(\frac{8t_{sub}}{\pi L}\right) = \frac{P_{diss}}{P_0} T_0 \tag{3-14}$$

where P_{diss} is the power dissipated in the channel, T_0 is the temperature of the backside contact and t_{sub} is the thickness of the substrate and $P_0 = (\pi \kappa(T_0) W T_0 / P_{diss}) / \ln(8t_{sub}/\pi L)$. Equation (3-13) may be integrated and the result simplified by using equation (3-14) yielding the equation:

$$\Delta T = T_0 \frac{1 - \left(1 - \frac{P_{diss}}{2P_0}\right)^2}{\left(1 - \frac{P_{diss}}{2P_0}\right)^2} \tag{3-15}$$

3.7 The Iterative Solution for the Temperature-Dependent Current

The method for the solution of the temperature-dependent drain current is described as follows. First the current is calculated using the current equations for a particular drain voltage assuming a channel temperature of 300K. The dissipated power P_{diss} is the product of the drain current and the drain voltage. This dissipated power is used to find the difference in temperature between the backside contact and the channel using equation (3-15). ΔT is then used to find the temperature of the channel ($\Delta T + T_0$), which is subsequently used for finding the value of the current at the designated temperature. This procedure is carried on iteratively until sufficient convergence is observed.

3.8 Results

Data were obtained from [31] for a MESFET fabricated by Sghaier *et al.* at Thales Research and Technology at Orsay, France. The transistor has a gate length of 1 μm, a width of 2×250 μm, a buffer layer thickness of 0.3 μm, a channel thickness of 0.3 μm, a channel doping level of 2×10^{17} cm^{-3} and a buffer doping of 1×10^{16} cm^{-3}. The distance between the source and the gate contact is 1 μm and that between the gate and the drain is 2 μm. A SiO_2 layer is present on top of the structure. The *I-V* characteristics of the MESFET is shown in Fig. 3-8.

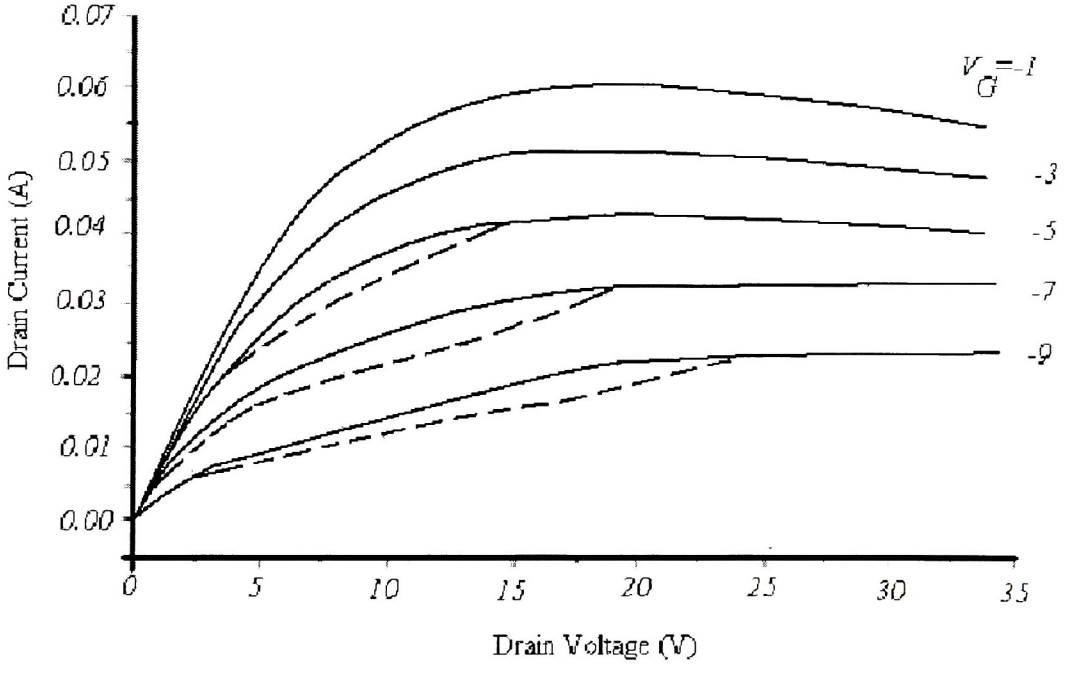


Fig. 3-8. The measured *I-V* characteristics of the MESFET fabricated by Sghaier *et al.* [31] depicting the various non-idealities present in the MESFET.

Fig. 3-8 contains two sets of *I-V* curves. Current components depicted by solid lines represent simulations in which the gate voltage was progressively decreased from –1V to –9 V, while those represented by the

dashed lines are representative of the *I-V* characterictics measured while the gate bias was progressively increased from –9 V to –1V. For the gate voltages of –1V and –3 V, the two sets of curves overlap. For the gate voltages of –5 V, -7 V and –9 V however, the currents in the two sets are different and differ in the amount of current collapse resulting from substrate trapping effects. Thermal deterioration of drain current is also evident, especially for low gate and high drain biases, wherein the drain current is seen to decrease rather than increase with increasing drain bias.

Fig. 3-9 depicts the simulation results resulting from neglecting both buffer and substrate traps. It incorporates thermal effects so that the true nature of the drain-current reductions due to the surface and the substrate traps become evident. It can be seen from the figure that the drain currents predicted by the absence of the trapping effects are significantly greater than the measured value.

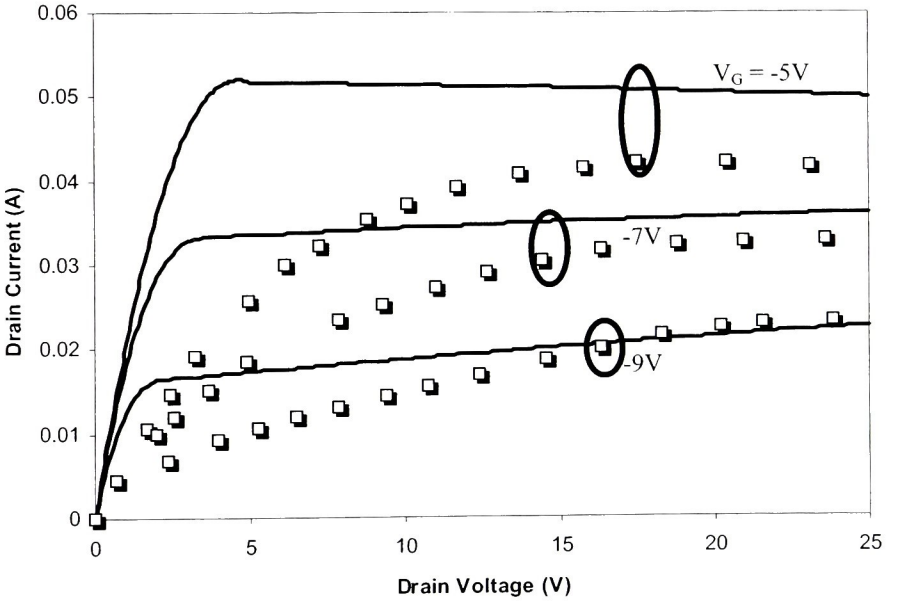


Fig. 3-9. Measured (□) and calculated *I-V* characteristics showing the difference in the measured and calculated values when trapping characteristics are not incorporated.

Fig. 3-11 represents the *I-V* characteristics in which the surface traps have been incorporated but the substrate traps have not been incorporated, while Fig. 3-13 represents the *I-V* characteristics wherein both the surface and the substrate traps have been accounted for.

As can be seen from the Fig. 3-9, Fig. 3-11 and Fig 3-13, there is significant current collapse not only due to the substrate traps but there is significant loss of current due to the presence of the surface traps as well. When trapping effects are neglected, the predicted value of the saturation current for a gate bias of –5 V is of the order of 0.05 A while the corresponding measured value is of the order of 0.04 A, as seen in Fig. 3-9. As mentioned before, the surface traps are primarily responsible for increasing the drain resistance of the channel. For the results shown below, the variation of the drain resistance with the drain bias is shown in Fig. 3-10.

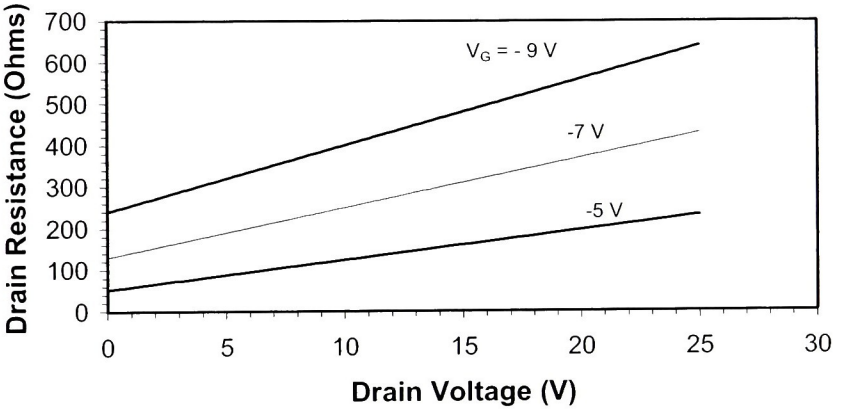


Fig. 3-10. Variation of drain resistance with the gate and the drain voltage.

This results in greater potential drop across the drain and the source resistances and thus lesser current. It may be predicted from this that the greater the current, the greater the magnitude of the current deviates from the measured value.

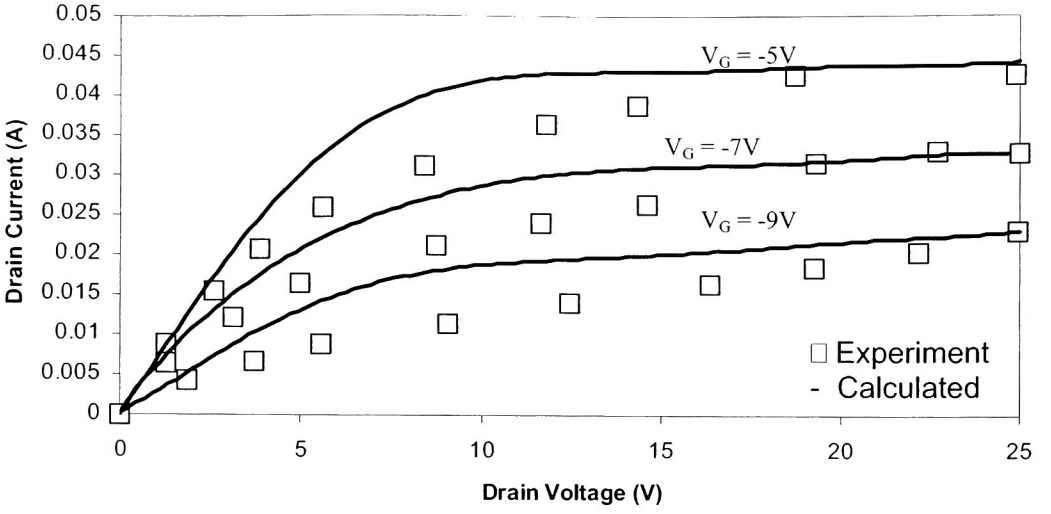


Fig. 3-11. Measured and calculated *I-V* characteristics depicting the difference between the measured and calculated values when substrate trapping effects are neglected.

This is evident in Fig. 3-9 where the greatest deviation from measured current is for the gate voltage of -5 V. As seen in Fig. 3-13, the inclusion of the substrate trapping effects in the *I-V* relationship results in much better prediction of current, especially in the saturation region. However, it is still insufficient in predicting the current collapse that is observed as a result of the buffer traps. Buffer traps capture electrons in the previous sweep and steadily release electrons in the subsequent sweep. The variation of the effective channel concentration (n) with respect to the drain voltage is shown in Fig. 3-12. The release of electrons from buffer traps for different biases is dependent mainly upon the difference in channel/buffer temperature for the biases. The channel (and thus the buffer) temperature at a gate voltage of –9 V is lower than the channel temperature at the gate voltage of –5 V.

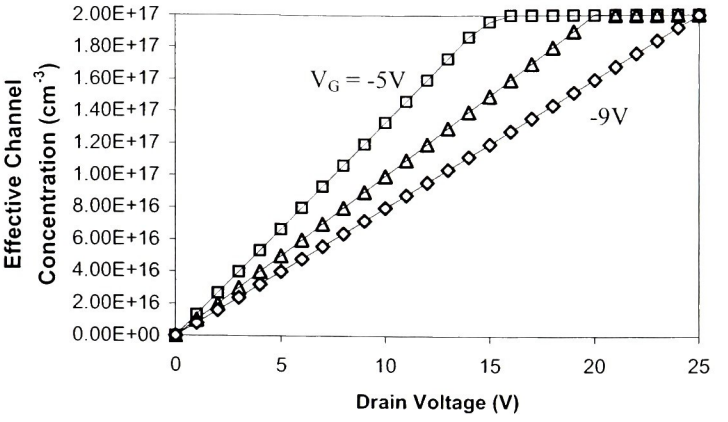


Fig. 3-12. The variation of the effective channel concentration with respect to the drain voltage.

It is evident that it will necessarily take greater time for the electrons in the buffer traps to get detrapped for the gate voltage of –9 V than it would take for the buffer traps to get detrapped for the gate voltage of –5 V. This is seen to be the case in Fig. 3-9. Incorporation of the buffer trapping effect into the *I-V* relationship results in the correct prediction of the current relationships, as shown in Fig. 3-13.

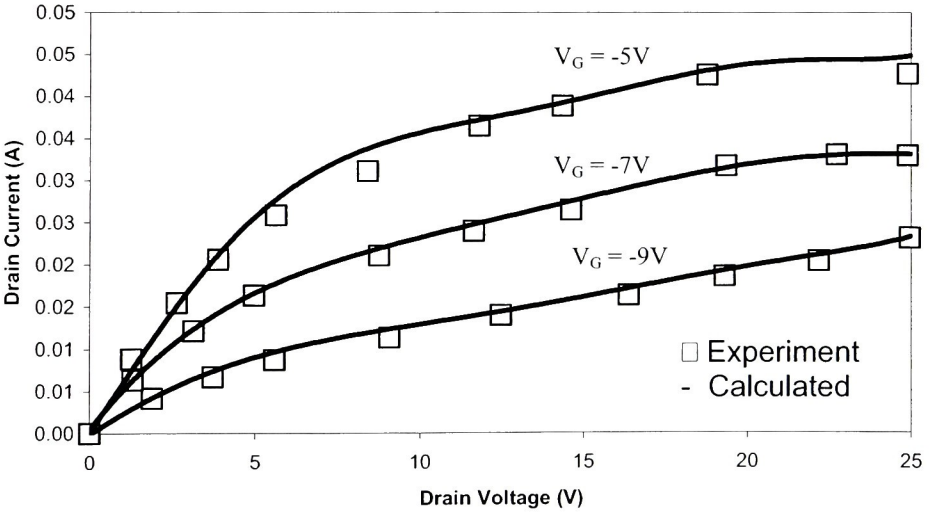
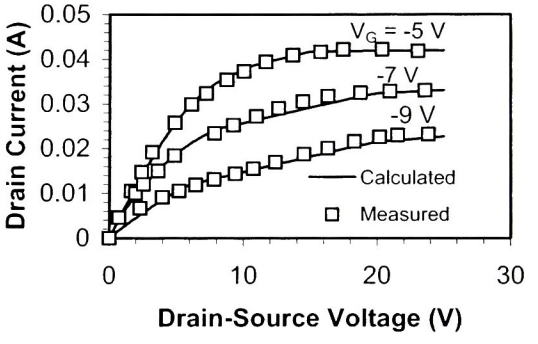
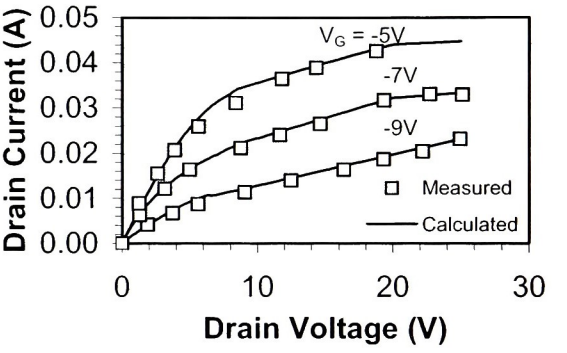


Fig. 3-13. Measured and calculated *I-V* characteristics showing the agreement between the two when all non-idealities are incorporated into the *I-V* relationships.

Fig. 3-14 (a) depicts the measured and calculated *I-V* relationship when the gate voltage was progressively decreased from –1 V to –9 V, while Fig. 3-14 (b) depicts the measured and the calculated *I-V* relationship when the gate voltage was increased from –9 V to –1V. In the former case, before the sweep begins, the temperature of the device in general is higher since the previous sweep happened to dissipate more heat. This is shown in Fig. 3-14 (b) where the buffer-trapping effect is more pronounced when the gate voltage increases from –9 V to –1 V than in the case when the gate voltage decreases from –1 V to –9 V.



(a)



(b)

Fig. 3-14. Measured and calculated *I-V* characteristics for instances where (a) the gate voltage was decreased from –1 V to –9 V and (b) the gate voltage was increased from –9 V to –1 V.

Another device simulation has also been carried out for further corroborating the theory. This device has been reported by Huang *et al.* [44]. The MESFET structure is similar to that that made by Sghaier *et al.* with the following characteristics: the n-type channel has a doping of 1.7×10^{17} cm^{-3}, and a depth of 0.26 μm. The main difference between the previous and the current device is that this device has a very thick buffer layer of 6 μm and has a concentration of 1.4×10^{15} cm^{-3}. The source and the gate lengths are 1 μm and the gate length is 0.7 μm. The measured and the simulated *I-V* characteristics are shown in Fig. 3-15.

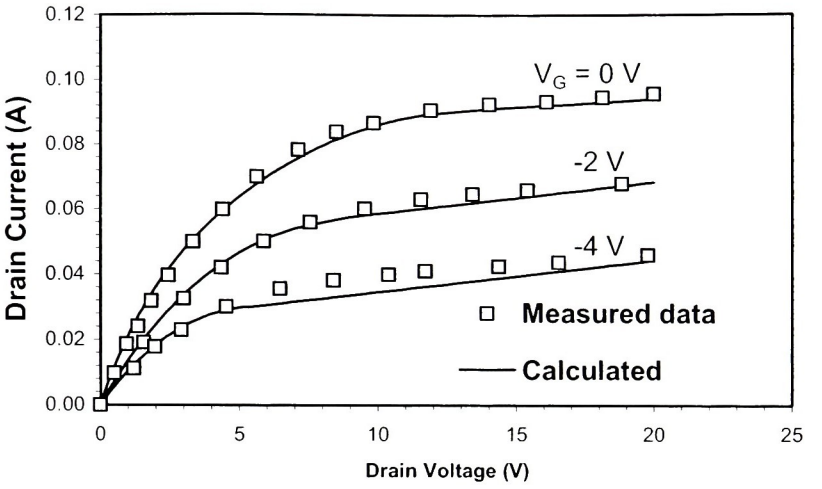


Fig. 3-15. Measured and calculated *I-V* characteristics showing the importance of having a thick buffer layer.

The *I-V* characteristics have been simulated without the inclusion of substrate traps but with the inclusion of surface trapping effects. The figure shows that the presence of a very thick buffer layer effectively eliminates the buffer trapping effects.

Chapter 4

The Effects of the Buffer Layer on the Electrical Characteristics of the MESFET

4.1 Introduction

In this chapter, two-dimensional simulations to investigate the effects of the buffer layer thickness and doping concentration on the electrical characteristics of the SiC MESFET have been carried out using the Atlas® device simulator*. The buffer layer is primarily used for preventing electrons from crossing the buffer layer and getting trapped into the buffer traps as shown in the previous chapter. It is further seen in Chapter 2 that the current equations are significantly altered as a result of the presence of the depletion region at the channel/buffer interface. It may be inferred that the electrical characteristics of the MESFET will be significantly altered by the presence of the depletion region. In theoretical calculations, it is assumed that the depletion region at the buffer/channel interface is devoid of channel electrons. This is not strictly accurate. As shall be seen in this chapter, two-dimensional numerical simulations show that for weakly doped buffer regions, channel electrons leak into the depletion region creating a duplicate channel, and the electrical characteristics of the device are greatly affected by it. This chapter investigates the variations of transconductance, output resistance, gate-source capacitance, gate-drain capacitance and (cutoff frequency) f_T with respect to the change in buffer layer thickness and doping concentration.

For a SiC MESFET with buffer layer thickness of 0.3 μm and gate length of 1 μm, drain current increases from 0.1 A/ μm to above 0.45 A/ μm as the buffer layer doping density is decreased from 1.9×10^{17} cm^{-3} to 1×10^{16} cm^{-3}. The simulations were carried out at a gate-source voltage of –1 V and a drain-source voltage of 15 V. Under similar conditions, the output resistance decreases from 1.2×10^{6} Ω/μm to

* The details of device simulation and parameters used for device simulation may be found in Appendix I-2D Device Simulation

Ω/μm, and the transconductance decreases from 5.9 mS/ μm to 5.3 mS/ μm, and f_T decreases from 0.11 GHz to 0.08 GHz.

4.2 Results and Discussion

In this analysis, three n-channel SiC-based MESFETs with different buffer layers have been considered as described in Fig. 4-1 and Table 4-I. For comparison of the performance variations due to different buffer layers, the same channel doping density and thickness of all three structures have been considered. These are 2×10^{17} cm^{-3} and 0.3 μm, respectively. Structure-I has a thin (0.3 μm) and lightly-doped (1×10^{16} cm^{-3}) buffer region, Structure-II has a thin (0.3 μm) but heavily-doped buffer region, and Structure-III has a thick (0.6 μm) and moderately-doped (5×10^{16} cm^{-3}) buffer layer.

Table 4-I – Device structures used in the analysis.

Structure	I	II	III
Buffer thickness (μm)	0.3	0.3	0.6
Buffer doping (cm^{-3})	1×10^{16}	1×10^{17}	5×10^{16}
Channel doping (cm^{-3})	2×10^{17}	2×10^{17}	2×10^{17}
Channel thickness (μm)	0.3	0.3	0.3

Fig. 4-1 depicts the channel current density and the vertical component of the electric field along the cross section of the devices. It can be seen from Fig. 4-1(a) that the electric field in Structure-I is very weak at the channel/buffer interface compared to that present in Structure-II and Structure-III. This is because the lower doping in the buffer layer of Structure-I would entail a much smaller built-in voltage at the channel/buffer interface and a correspondingly low electric field would result. However, a net electric field across the buffer exists as the buffer layer is fully depleted. As a result, the channel electrons in Structure-I are not completely confined within the channel and leak into substrate region through the buffer layer and are subsequently captured by the traps. The dispersion of electrons causes the drain current in the saturation region to become linearly dependent upon the drain voltage. Thus, the output resistance of the channel is significantly reduced as shown in the *I-V* characteristics of Structure-I (see Fig. 4-2, curves shown by □).

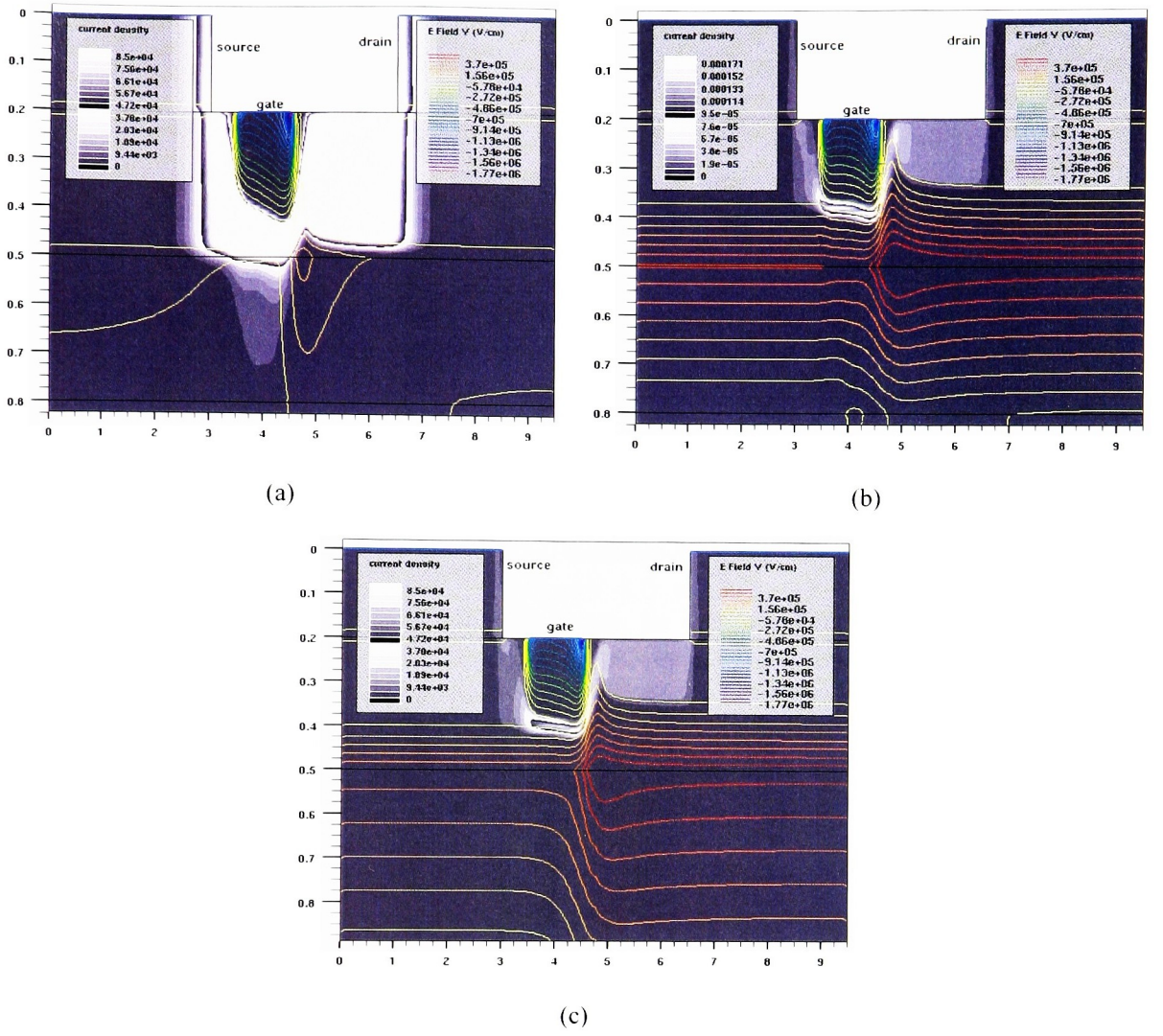


Fig. 4-1. The current density and the vertical component of electric field lines are plotted across the device cross-sections under similar biasing conditions (V_{GS} = -5V and V_{DS} = 15V). It may be observed that the spatial dispersion of free carriers is the highest in Structure-I (Fig. 1a) - where the buffer layer is totally depleted, and is lowest in the Structure-II (Fig. 1b) - where the buffer is least depleted. Structure-III (Fig. 1c) exhibits a greater degree of spatial dispersion of carrier density compared to Structure-II as the depletion region width in the buffer layer is increased.

In Structure-II and Structure-III, the buffer layer is not fully depleted due to an increase in doping density and/or buffer layer thickness. As a result, the carriers are confined inside the channel due to the absence of a net electric field across the buffer.

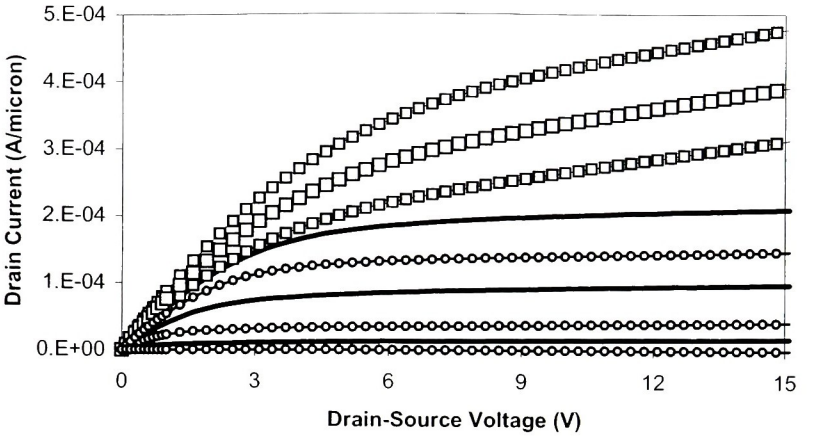
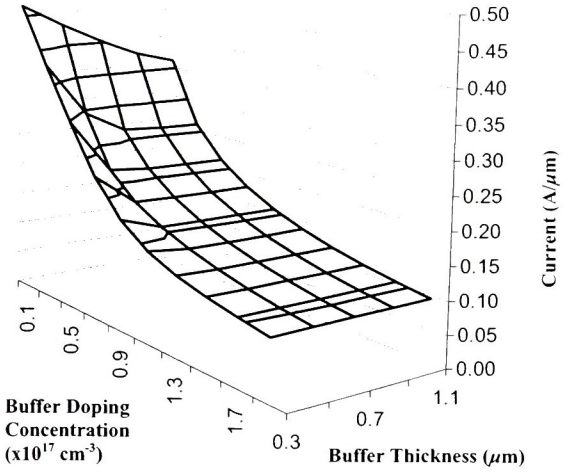
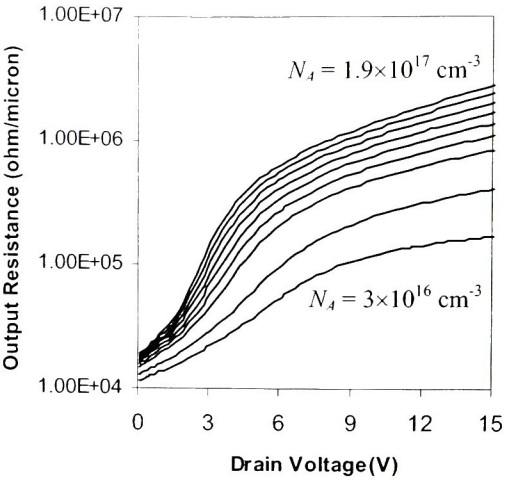


Fig. 4-2. *I-V* characteristics of Structure-I, -II and -III. The I-V characteristics of Structure-I (□) exhibits the highest saturation drain current, however, its output resistance is the lowest. Structure-II (o) has the lowest saturation drain current and the highest output resistance. In Structure-III (—), an increase in saturation drain current is obtained at the expense of reduced output resistance. Gate voltages are -1V (top), -3V (middle) and -5V (bottom).

As a result, higher output resistance is observed in the *I-V* characteristics of Structures-II and -III as shown in Fig. 4-2. However, since the concentration of the buffer layer of Structure-II is double the concentration of the buffer layer of Structure-III, carrier confinement is significantly higher and so is the output resistance. One consequence of improper confinement of the channel current density resulting from a low-doped buffer region is that the drain current is higher due to the effective increase in channel thickness. Fig. 4-3(a) shows the variation of the drain current with the variations in the buffer layer thickness and buffer doping concentration at V_{GS} = -1 V and V_{DS} = 15 V. The drain current varies significantly with the buffer doping concentration and only slightly with the buffer thickness, especially in buffers that are highly doped. The thick and heavily doped buffers have the least current while thin and lightly doped buffers have the maximum current. From the previous discussion, it may be inferred that the buffers that are heavily doped should exhibit the greatest output resistances. This can be seen from Fig. 4-3(b), which shows the variation of the output resistance as a function of drain voltage with the buffer doping concentration as a parameter, at a gate bias of –1 V.



(a)



(b)

Fig. 4-3. Effects of buffer layer - (a) variation of the drain current with the variations in buffer concentration and thickness at V_{GS}= -1 V and V_{DS}= 15 V, and (b) variation of the drain resistance with the variations in drain voltage and buffer layer concentration at V_{GS}= -1 V.

As expected, the output resistance steadily increases with increasing drain voltage and buffer layer concentration. The variation of the gate-source capacitance (C_{GS}) with respect to the buffer thickness and buffer doping concentration is shown in Fig. 4-4(a). The gate-source capacitance is of the order of 5 fF/μm and is nearly independent of the thickness of the channel. However, it increases linearly with decreasing doping concentration. The variation of the gate-drain capacitance (C_{GD}) with respect to the buffer thickness and doping concentration is shown in Fig. 4-4(b). The gate-drain capacitance is nearly independent of the buffer thickness and increases almost linearly with decreasing buffer doping concentration. The transconductance (G_m) as a function of buffer concentration and buffer thickness is shown in Fig. 4-4(c). The transconductance is nearly independent of both the doping and the buffer thickness. However, for low values of buffer concentration, the transconductance decreases at low channel thickness.

Finally, f_T for the transistor is calculated using:

$$f_T = \frac{G_m}{2\pi(C_{GS} + C_{GD})} \tag{4-1}$$

A plot of f_T is shown in Fig. 4-4(d). As can be seen from the figure, f_T is also nearly independent of both the buffer thickness and buffer concentration.

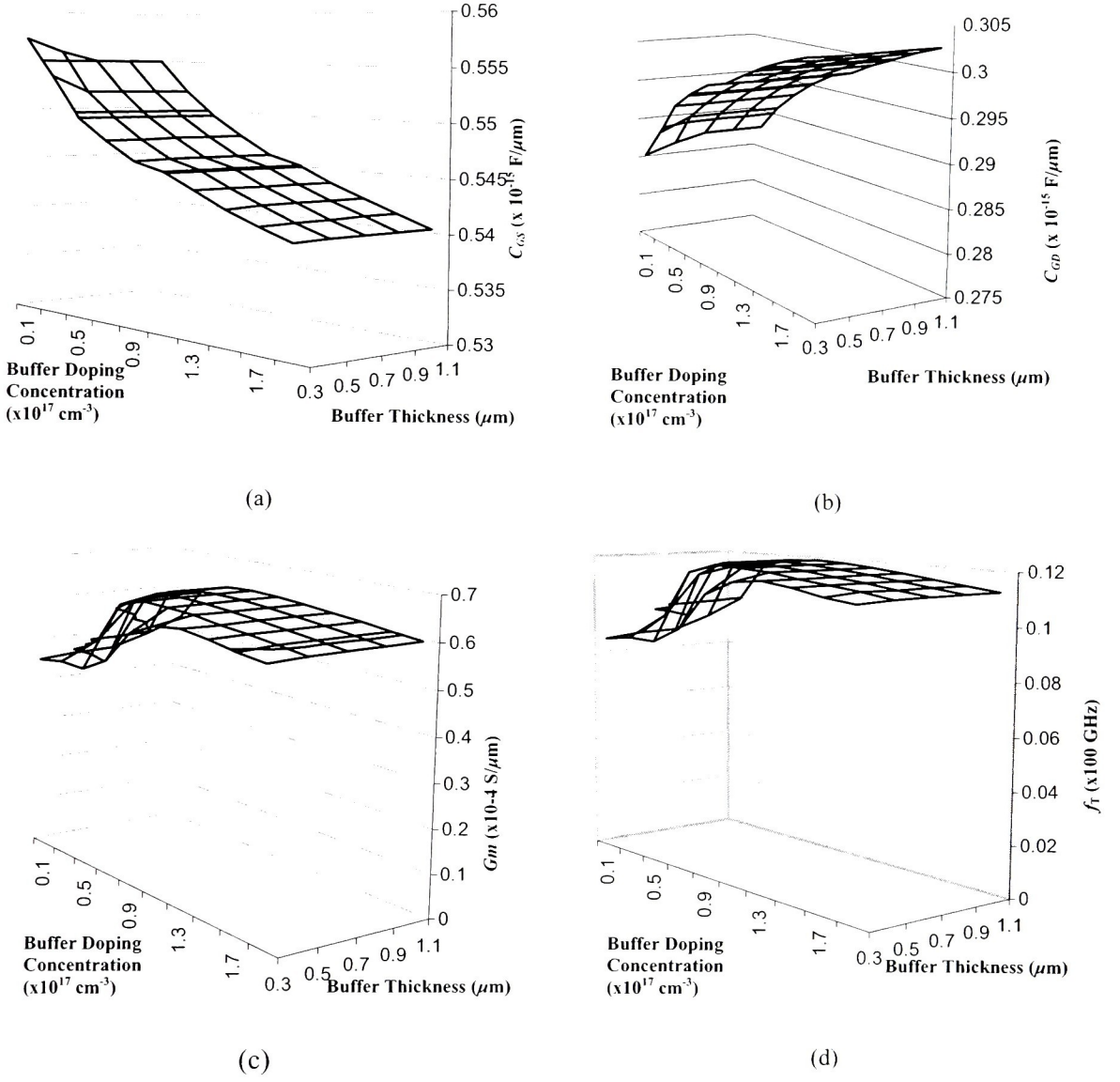


Fig. 4-4. Small-signal parameters- (a) the gate-source capacitance, (b) the gate-drain capacitance, (c) the transconductance and (d) f_T, as a function of the buffer concentration and buffer thickness.

For low values of buffer concentration, a sharp drop in f_T can be observed. This decrease in the value of f_T is seen to mimic the decrease in transconductance shown in Fig. 4-4(c). C_{GS} and C_{GD} exhibit

complementary behavior toward doping concentration and the summation of C_{GD} and C_{GS} is almost independent of both buffer doping concentration and thickness.

4.3 Conclusions

This chapter investigated the effects of the doping concentration and thickness of the buffer layer on the SiC-based MESFET characteristics. It was found that high values of doping concentration of the buffer layer results in higher output resistance and higher f_T, which are important for the devices to be used in RF power amplifiers. As the maximum drain current in the devices with higher doping concentration is significantly reduced, devices with larger channel widths are required to compensate for the decreasing current. A highly doped buffer prohibits channel electrons from reaching the electron traps located at the buffer-substrate interface and thus would result in the mitigation of substrate trapping effects.

Chapter 5

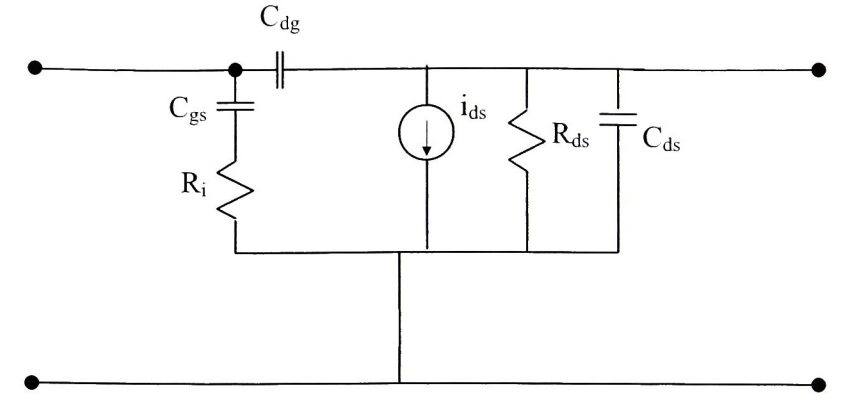
Small-Signal Parameters

5.1 Introduction

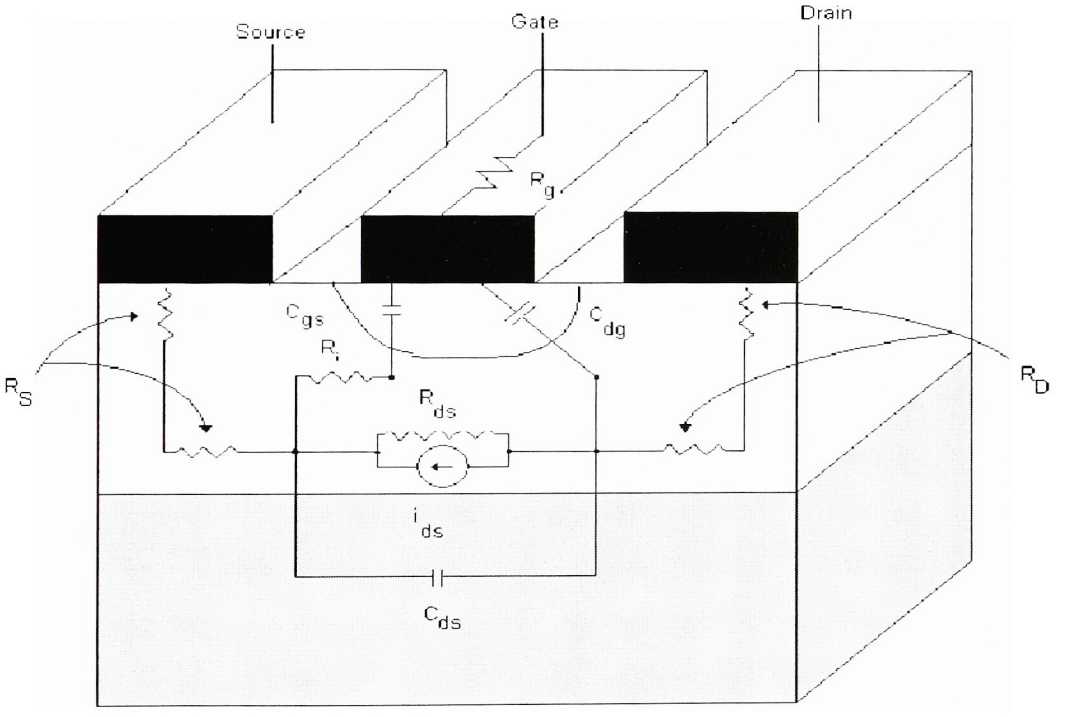
In this chapter, the small-signal model of the MESFET is studied. The model does not take into account the thermal effects arising from electron-phonon interactions and trapping effects. The small-signal model necessary for using the transistor for RF/analog applications, is made up of a set of resistors, capacitors and typically a voltage controlled current source (defined at a given set of bias voltages). This model can then be used as a sub-circuit in larger circuit applications (eg. power amplifiers, LNAs), and analyzed using standard circuit analysis. Once the small-signal model is determined, it is also possible to determine the frequency characteristics of the device, the optimum frequency of operation of the transistor and the maximum operating frequency of the device. Subsequently, digital applications can use this information to find the turn-on and turn-off times of logic-gates, clock generators, etc., fabricated using the device.

5.2 The Small-Signal Model of the MESFET

A number of small-signal models are available for the MESFET [45]-[49]. Most of the models are very similar to various well-known FET models [50], [51]. A typical small-signal model of the MESFET is shown in Fig. 5-1(a). In Fig. 5-1(b) the physical origins of various elements present in the small-signal model of Fig. 5-1(a) are shown. The model and the diagram have been adapted from the book Ref. [52].



(a)



(b)

Fig. 5-1. (a) small-signal circuit model, and (b) a schematic representation of the origins of each of the elements present in the small-signal representation [52].

From the figure, it can be seen that source, gate and drain resistances are modeled by the resistances R_S, R_G and R_D, respectively. Further, it may be observed that the source and the drain resistances are broken up into two parts: the resistance of the source/drain ohmic contacts and the resistance of the semiconductor present between the source/drain contact regions and the gate region. The gate resistance is primarily composed of the gate contact resistance. As shall be discussed later, none of the resistances are modeled into the small-signal parameters. The height of the depletion region under the gate toward the source side is controlled by the potential between the gate and the source. A differential change in the source-to-gate voltage induces a corresponding differential change in the amount of charge in the depletion region under the gate in the channel. The ratio of this variation of the depletion charge under the gate with the corresponding variation in the change in the source-to-gate voltage with the drain voltage held constant corresponds to the gate-source capacitance C_{gs}, as shown in the Fig. 5-1 (b). A similar situation occurs when the drain voltage is varied while the gate and source voltages are held constant. In this situation, the potential across the channel changes slightly. This induces a change in the height of the depletion region and thus a change in the magnitude of the charge in the depletion region under the channel. This differential change in the depletion-region charge under the gate divided by the differential change in the drain voltage (while all other voltages remaining constant,) is represented by the gate-drain capacitance C_{gd}. i_{ds} is the gate voltage-controlled current source. The current in the channel is ideally dependent only upon the gate voltage and not on the drain voltage when the device is operating in the saturation region. Effects of the drain voltage on the *I-V* curves cannot be neglected in the saturation region of operation. The drain voltage dependence of the current is modeled by using a bias dependent channel resistance R_{ds}. The drain-source capacitance C_{ds} is used to model the significant displacement current that may flow through the channel at high frequencies. In this thesis, methods for determining the gate-source capacitance, the gate-drain capacitance, the transconductance and the output conductance is determined. The transconductance and the output conductance are obtained by differentiating the drain current with respect to the gate voltage and drain voltage, respectively, while the gate-source and gate-drain capacitances are obtained by differentiating the charge under the gate with respect to the gate and the drain voltages, respectively.

5.3 **Current Equations Revisited**

It needs to be noted that the current equations that have been derived in the first chapter correspond to an extrinsic transistor wherein the source and the drain resistance are modeled into the current. However, the small-signal model derived in this chapter is an intrinsic model as seen from Fig. 5-1. In this model, the small signal parameters are independent of the source and the drain voltages. The potentials at the source and the drain are assumed to be equal to those applied at the terminals. Under these circumstances, the current equations need to be re-derived by neglecting the source and the drain resistances. The procedure for the derivations is the same as that in Chapter 2 and so only the results are shown here. The equation for the source-drain current in the linear region is given by:

$$I_D = \frac{qWN_D\mu_0 v_{sat}}{v_{sat}L + \mu_0 V_D}\left\{aV_D - \frac{2}{3}\frac{qN_D}{2\varepsilon}\left[h_D^3 - h_S^3\right] - \frac{2}{3}\frac{qN_D}{2\varepsilon}\frac{N_A + N_D}{N_A}\left[h_{1L}^3 - h_{1S}^3\right]\right\}, \tag{5-1}$$

where, all parameters are the same as defined in Chapter 2 other than the heights of the depletion regions which are defined as:

$$\begin{aligned} h_S &= \sqrt{\frac{2\varepsilon}{qN_D}\left[-V_G + V_{bi}\right]} \\ h_D &= \sqrt{\frac{2\varepsilon}{qN_D}\left[-V_G + V_{bi} + V_D\right]} \\ h_{1S} &= \left[\frac{N_A}{N_A + N_D}\right]\sqrt{\frac{2\varepsilon}{q}\frac{N_A + N_D}{N_D N_A}\left[U_{bi}\right]} \\ h_{1L} &= \left[\frac{N_A}{N_A + N_D}\right]\sqrt{\frac{2\varepsilon}{q}\frac{N_A + N_D}{N_D N_A}\left[U_{bi} + V_D\right]} \end{aligned} \tag{5-2}$$

For solving for the current equations in the saturation region the following three equations need to be solved simultaneously:

$$I_D = \frac{qWN_D\mu_0 v_{sat}}{v_{sat}L_1 + \mu_0 V_1}\left\{aV_1 - \frac{2}{3}\frac{qN_D}{2\varepsilon}\left[h_{L1}^3 - h_S^3\right] - \frac{2}{3}\frac{qN_D}{2\varepsilon}\frac{N_A + N_D}{N_A}\left[h_{1L1}^3 - h_{1S}^3\right]\right\}, \tag{5-3}$$

$$I_D = qWN_D v_{sat}\left[a - \sqrt{\frac{2\varepsilon}{qN_D}\left[-V_G + V_{bi} + V_1\right]} - \sqrt{\frac{2\varepsilon}{qN_D}\frac{N_A}{N_A + N_D}\left[U_{bi} + V_1\right]}\right], \tag{5-4}$$

$$\text{and } V_D = \frac{2E_S h_{L1}}{\pi}\sinh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right)+V_1 . \tag{5-5}$$

Again, all parameters have already been defined in Chapter 2.

5.4 The Output Conductance

The output conductance is the reciprocal of the output resistance R_{ds}. This is a small signal parameter defined as the ratio of the differential change in the drain current to a differential change in the drain voltage. In the linear region of operation, the output conductance may be calculated by differentiating the linear region drain current equation with respect to drain voltage as shown below:

$$g_{ol} = \frac{dI_D}{dV_D} = \frac{qWN_D\mu_0 v_{sat}}{v_{sat}L+\mu_0 V_D}\{a-h_D-h_{1L}\}-\frac{I_D\mu_0}{[v_{sat}+\mu_0 V_D]} \tag{5-6}$$

For obtaining the output conductance in the saturation region, the three equations (5-3), (5-4) and (5-5) need to be differentiated with respect to the drain voltage, and the differentials dL_1/dV_D and dV_1/dV_D need to be eliminated from the resulting equations. Differentiating equation (5-3) with respect to V_D we obtain:

$$\begin{aligned} g_{os} = \left.\frac{dI_{Dsat}}{dV_D}\right|_{V_G=const.} &= \frac{qWN_D\mu_0 v_{sat}}{[v_{sat}L_1+\mu_0 V_1]}\times\left\{a\left[\frac{dV_1}{dV_D}\right]\right. \\ &\left.-\left[h_{L1}\frac{dV_1}{dV_D}\right]-\left[h_{1L1}\frac{dV_1}{dV_D}\right]\right\}-\frac{I_D}{[v_{sat}L_1+\mu_0 V_1]}\left\{v_{sat}\frac{dL_1}{dV_D}+\mu_0\left(\frac{dV_1}{dV_D}\right)\right\} \end{aligned}, \tag{5-7}$$

which may be rearranged to an equation of the form:

$$\begin{aligned} g_{os} = &\left[\frac{qWN_D\mu_0 v_{sat}}{[v_{sat}L_1+\mu_0 V_1]}\{a-h_{L1}-h_{1L1}\}-\frac{I_D\mu_0}{[v_{sat}L_1+\mu_0 V_1]}\right]\left[\frac{dV_1}{dV_D}\right] \\ &-\frac{I_D v_{sat}}{[v_{sat}L_1+\mu_0 V_1]}\left\{\frac{dL_1}{dV_D}\right\} \end{aligned}. \tag{5-8}$$

which may be rewritten as:

$$g_{os} = M_{11}\left[\frac{dV_1}{dV_D}\right]-M_{12}\left\{\frac{dL_1}{dV_D}\right\}, \tag{5-9}$$

where,

$$M_{11} = \left[\frac{qWN_D \mu_0 v_{sat}}{\left[v_{sat} L_1 + \mu_0 V_1 \right]} \{ a - h_{L1} - h_{1L1} \} - \frac{I_D \mu_0}{\left[v_{sat} L_1 + \mu_0 V_1 \right]} \right], \text{ and} \tag{5-10 a}$$

$$M_{12} = \frac{I_D v_{sat}}{\left[v_{sat} L_1 + \mu_0 V_1 \right]}. \tag{5-10 b}$$

Now, differentiating equation (5-4) with respect to V_D, we obtain:

$$g_{os} = -\varepsilon W v_{sat} \left[\frac{1}{h_{L1}} + \left(\frac{N_A}{N_A + N_D} \right) \frac{1}{h_{1L1}} \right] \left(\frac{dV_1}{dV_D} \right), \tag{5-11}$$

which may be rewritten as:

$$g_{os} = -M_{13} \left(\frac{dV_1}{dV_D} \right) \tag{5-12}$$

where:

$$M_{13} = \varepsilon W v_{sat} \left[\frac{1}{h_{L1}} + \left(\frac{N_A}{N_A + N_D} \right) \frac{1}{h_{1L1}} \right]. \tag{5-13}$$

And finally, differentiating equation (5-5) with respect to V_D, we obtain:

$$\begin{aligned} 1 = {} & \frac{dV_1}{dV_D} + \frac{2E_S}{\pi} \sinh\left(\frac{\pi(L - L_1)}{2h_{L1}} \right) \left(\frac{2\varepsilon}{qN_D} \right) \left(\frac{1}{h_{L1}} \right) \left(\frac{dV_1}{dV_D} \right) + \\ & \frac{2E_S}{\pi} h_{L1} \cosh\left(\frac{\pi(L - L_1)}{2h_{L1}} \right) \left(\frac{1}{4h_{L1}^2} \right) \left[2h_{L1} \pi \left(-\frac{dL_1}{dV_D} \right) - \right. \\ & \left. \pi(L - L_1) \left(\frac{1}{2h_{L1}} \right) \left(\frac{2\varepsilon}{qN_D} \right) \left(\frac{dV_1}{dV_D} \right) \right] \end{aligned}, \tag{5-14}$$

which may be rearranged to:

$$\begin{aligned} 1 = {} & \left[\frac{dV_1}{dV_D} \right] \left[1 + \frac{2E_S}{\pi} \frac{2\varepsilon}{qN_D} \frac{1}{2h_{L1}} \sinh\left(\frac{\pi(L - L_1)}{2h_{L1}} \right) - \right. \\ & \left. \frac{E_S (L - L_1)}{4h_{L1}^2} \left(\frac{2\varepsilon}{qN_D} \right) \cosh\left(\frac{\pi(L - L_1)}{2h_{L1}} \right) \right] - \left(\frac{dL_1}{dV_D} \right) \left[2E_S \cosh\left(\frac{\pi(L - L_1)}{2h_{L1}} \right) \right] \end{aligned}. \tag{5-15}$$

Again, this is represented as:

$$1 = \left[\frac{dV_1}{dV_D}\right] M_{14} - \left[\frac{dL_1}{dV_D}\right] M_{15} \tag{5-16}$$

where,

$$M_{14} = \left[1 + \frac{2E_S}{\pi}\frac{2\varepsilon}{qN_D}\frac{1}{2h_{L1}}\sinh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right) - \frac{E_S(L-L_1)}{4h_{L1}^2}\left(\frac{2\varepsilon}{qN_D}\right)\cosh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right)\right] \tag{5-17 a}$$

$$M_{15} = 2E_S \cosh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right). \tag{5-17 b}$$

Using equations (5-9), (5-12) and (5-16), the equation for the output conductance may be obtained as:

$$g_0 = \frac{[M_{12}/M_{15}]}{1 + M_{11}/M_{13} - (M_{12}M_{14})/(M_{13}M_{15})}. \tag{5-18}$$

5.5 **The Transconductance**

The transconductance is defined as the differential change in the drain current with respect to a differential change in the gate voltage. In the linear region, the transconductance may be determined by differentiating the current equation in the linear region (5-1) with respect to the gate voltage:

$$g_{ml} = \frac{qWN_D\mu_0 v_{sat}}{v_{sat}L + \mu_0 V_D}[-(h_D - h_S)]. \tag{5-19}$$

In the saturation region, all the three current equations for the saturation region (5-3), (5-4) and (5-5) need to be differentiated with respect to the gate voltage. Differentiating (5-3) with respect to the gate voltage, we obtain:

$$g_{ms} = \frac{qWN_D v_{sat}\mu_0}{v_{sat}L_1 + \mu_0 V_1}\left[a\frac{dV_1}{dV_G} - \left\{h_{L1}\left(1 + \frac{dV_1}{dV_G}\right) - h_S\right\} - \left\{h_{1L1}\frac{dV_1}{dV_G}\right\}\right], \tag{5-20}$$
$$- \frac{I_D}{v_{sat}L_1 + \mu_0 V_1}\left\{v_{sat}\left(\frac{dL_1}{dV_G}\right) + \mu_0\left(\frac{dV_1}{dV_G}\right)\right\}$$

which can be rewritten as

$$g_m = \left[\frac{qWN_D v_{sat}\mu_0}{v_{sat}L_1 + \mu_0 V_1}\{a - h_{L1} - h_{1L1}\} - \frac{I_D \mu_0}{v_{sat}L_1 + \mu_0 V_1} \right] \frac{dV_1}{dV_G} - \frac{qWN_D v_{sat}\mu_0}{v_{sat}L_1 + \mu_0 V_1}\{h_{L1} - h_S\} - \frac{I_D \mu_0}{v_{sat}L_1 + \mu_0 V_1}\frac{dL_1}{dV_G} \tag{5-21}$$

which may be rewritten as:

$$g_m = M_{21}\left(\frac{dV_1}{dV_G}\right) + M_{22} - M_{23}\left(\frac{dL_1}{dV_G}\right) \tag{5-22}$$

where M_{21}, M_{22} and M_{23} are defined as,

$$M_{21} = \left[\frac{qWN_D v_{sat}\mu_0}{v_{sat}L_1 + \mu_0 V_1}\{a - h_{L1} - h_{1L1}\} - \frac{I_D \mu_0}{v_{sat}L_1 + \mu_0 V_1} \right], \tag{5-23 a}$$

$$M_{22} = -\frac{qWN_D v_{sat}\mu_0}{v_{sat}L_1 + \mu_0 V_1}\{h_{L1} - h_S\}, \text{ and} \tag{5-23 b}$$

$$M_{23} = \frac{I_D \mu_0}{v_{sat}L_1 + \mu_0 V_1}. \tag{5-23 c}$$

Now, differentiating equation (5-4) with respect to the gate voltage we obtain,

$$g_m = \varepsilon W v_{sat}\left[-\frac{1}{h_{L1}} - \frac{1}{h_{1L1}}\left(\frac{N_A}{N_A + N_D}\right)\right]\frac{dV_1}{dV_G} - \frac{\varepsilon W v_{sat}}{h_{L1}}, \tag{5-24}$$

which may be represented as,

$$g_m = M_{24}\frac{dV_1}{dV_D} - M_{25} \tag{5-25}$$

where,

$$M_{24} = \varepsilon W v_{sat}\left[-\frac{1}{h_{L1}} - \frac{1}{h_{1L1}}\left(\frac{N_A}{N_A + N_D}\right)\right], \text{ and} \tag{5-26 a}$$

$$M_{25} = \frac{\varepsilon W v_{sat}}{h_{L1}}. \tag{5-26 b}$$

And finally, differentiating equation (5-5) with respect to the gate voltage, we obtain:

$$0=\frac{2E_S h_{L1}}{\pi}\cosh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right)\left[\frac{\pi}{2h_{L1}}\left(-\frac{dL_1}{dV_G}\right)-\frac{\pi(L-L_1)}{4h_{L1}}\times\right.$$
$$\left.\frac{1}{(V_G+V_1+V_{bi})}\left(1+\frac{dV_1}{dV_G}\right)\right]+\frac{2E_S}{\pi}\sinh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right)\times \tag{5-27}$$
$$\frac{h_{L1}}{2(V_G+V_1+V_{bi})}\left(1+\frac{dV_1}{dV_G}\right)+\frac{dV_1}{dV_G}$$

which may be rearranged to the form:

$$0=\left[\frac{dV_1}{dV_G}\right]\left[1+E_S\cosh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right)\left\{-\frac{(L-L_1)}{2h_{L1}^2}\frac{2\varepsilon}{qN_D}\right\}+\frac{E_S}{h_{L1}\pi}\frac{2\varepsilon}{qN_D}\sinh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right)\right]$$
$$-\left[\frac{dL_1}{dV_G}\right]\left[E_S\cosh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right)\right] \tag{5-28}$$
$$+\frac{E_S}{h_{L1}\pi}\frac{2\varepsilon}{qN_D}\sinh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right)-\frac{E_S(L-L_1)}{2h_{L1}^2}\frac{2\varepsilon}{qN_D}\cosh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right)$$

which may be rewritten in the form:

$$\left[\frac{dV_1}{dV_G}\right]M_{26}-\left[\frac{dL_1}{dV_G}\right]M_{27}+M_{28}=0\,, \tag{5-29}$$

where,

$$M_{26}=1+E_S\cosh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right)\left\{-\frac{(L-L_1)}{2h_{L1}^2}\frac{2\varepsilon}{qN_D}\right\}+\frac{E_S}{h_{L1}\pi}\frac{2\varepsilon}{qN_D}\sinh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right), \tag{5-30 a}$$

$$M_{27}=E_S\cosh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right), \text{ and} \tag{5-30 b}$$

$$M_{28}=\frac{E_S}{h_{L1}\pi}\frac{2\varepsilon}{qN_D}\sinh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right)-\frac{E_S(L-L_1)}{2h_{L1}^2}\frac{2\varepsilon}{qN_D}\cosh\left(\frac{\pi(L-L_1)}{2h_{L1}}\right). \tag{5-30 c}$$

Finally, using equations (5-22), (5-25) and (5-29), the equation for the transconductance may be obtained as:

$$g_m = \frac{\left[M_{21} - \frac{M_{23}M_{26}}{M_{27}}\right]\frac{M_{25}}{M_{24}} + M_{22} - \frac{M_{28}}{M_{27}}}{1 - \left\{\frac{M_{21}}{M_{24}} - \frac{M_{23}}{M_{24}}\frac{M_{26}}{M_{27}}\right\}}. \tag{5-31}$$

5.6 **The Gate-Source Capacitance**

The magnitude of depletion charge under the gate is dependent upon the gate and the drain biases. Differential changes of these biases result in differential changes of the magnitude of the charge under the gate. This leads to the formation of capacitances between the gate and the drain terminals and capacitances between the gate and the source terminals. These are termed the as gate-drain capacitance (C_{gd}) and the gate-source capacitance (C_{gs}), respectively. There are a number of definitions for the each of these capacitances [53-55], but the most common definition for the gate-source and gate-drain capacitances are $\left.\frac{dQ_1}{dV_G}\right|_{V_D=const.}$ and $\left.\frac{dQ_1}{dV_D}\right|_{V_G=const.}$, respectively [56].

The charge under the gate is given by the equation:

$$Q_1 = qWN_D \int_0^L h(x)dx \tag{5-32}$$

in the linear region and by

$$Q_1 = qWN_D \int_0^{L_1} h(x)dx + qWN_D h\big|_{x=L_1}(L - L_1) \tag{5-33}$$

in the saturation region. These equations may be differentiated with respect to the gate voltage while the drain voltage is held constant to obtain the gate-source capacitance. In the linear region the gate-source capacitance is given by:

$$C_{gs} = \frac{dQ_1}{dV_G} = qWN_D \int_0^L \frac{d}{dV_G}\sqrt{\frac{2\varepsilon}{qN_D}\left[-V_G + V_{bi} + V\right]}dx \tag{5-34}$$

After the differentiation is carried out, the value of the capacitance is given by the equation:

$$C_{gs} = -\varepsilon W \int_0^L \frac{dx}{h(x)} \tag{5-35}$$

Equation (2-11) may be used to find an expression relating x, the position along the channel and the corresponding channel potential V. This may be used for variable substitution. After variable substitution from x to V is carried out, the equation (5-35) may be represented by the equation:

$$C_{gs} = \varepsilon W \int_0^{V_D} \frac{1}{h}\left[\frac{qWN_D\mu_0}{I_D}\{a - h - h_1\} - \frac{\mu_0}{v_{sat}}\right] dV \tag{5-36}$$

where h and h_1 are functions of V. Equation (5-36) may be simplified by using the equation (5-2) as:

$$\begin{aligned} C_{gs} &= \varepsilon W\left[\frac{qWN_D\mu_0}{I_D}a - \frac{\mu_0}{v_{sat}}\right]\int_{h_S}^{h_D}\frac{qN_D}{\varepsilon}\,dh \\ &- \varepsilon W\frac{qWN_D\mu_0}{I_D}[V_D] \\ &- \varepsilon W\frac{qWN_D\mu_0}{I_D}\int_0^{V_D}\sqrt{\frac{N_A}{N_A+N_D}\left(\frac{U_{bi}+V}{V_{bi}+V-V_G}\right)}\,dV \end{aligned} \tag{5-37}$$

Finally, solving the equation (5-37) leads to the expression for the gate-source capacitance in the linear region as:

$$C_{gs} = \varepsilon W\left[\frac{qWN_D\mu_0}{I_D}a - \frac{\mu_0}{v_{sat}}\right]\left[h_D - h_S\right]$$
$$- \varepsilon W\frac{qWN_D\mu_0}{I_D}\left[V_D\right] - \varepsilon W\frac{qWN_D\mu_0}{I_D}\sqrt{\frac{N_A}{N_A+N_D}}\times$$
$$\left[\sqrt{\left(V_D+U_{bi}\right)\left(V_D-V_G+V_{bi}\right)} - \sqrt{\left(U_{bi}\right)\left(-V_G+V_{bi}\right)}\right. \qquad (5\text{-}38)$$
$$-\frac{\left(U_{bi}-V_G-V_{bi}\right)}{2}\ln\left\{\frac{\sqrt{V_D+U_{bi}}-\sqrt{V_D-V_G+V_{bi}}}{\sqrt{U_{bi}}-\sqrt{-V_G+V_{bi}}}\right\}+$$
$$\left.\frac{\left(U_{bi}-V_G-V_{bi}\right)}{2}\ln\left\{\frac{\sqrt{V_D+U_{bi}}+\sqrt{V_D-V_G+V_{bi}}}{\sqrt{U_{bi}}+\sqrt{-V_G+V_{bi}}}\right\}\right]$$

In the saturation region the equation (5-33) rather than the equation (5-32) must be differentiated with respect to the gate voltage. The capacitance is this given by:

$$C_{gs} = \frac{dQ_1}{dV_G} = \left\{qWN_D\int_0^{L_1}\frac{d}{dV_G}\sqrt{\frac{2\varepsilon}{qN_D}\left[-V_G+V_{bi}+V\right]}dx\right.$$
$$\left. + qWN_Dh_{L1}\frac{d}{dV_G}\left(L_1\right) - qWN_Dh_{L1}\frac{d}{dV_G}\left(0\right)\right\} - qWN_Dh_{L1}\frac{d}{dV_G}\left(L_1\right) \qquad (5\text{-}39)$$
$$+ qWN_D\left(L-L_1\right)\frac{dh_{L1}}{dV_G}$$

which may be rewritten in the form:

$$C_{gs} = qWN_D\int_0^{L_1}\frac{d}{dV_G}\sqrt{\frac{2\varepsilon}{qN_D}\left[-V_G+V_{bi}+V\right]}dx + qWN_D\left(L-L_1\right)\frac{dh_{L1}}{dV_G} \qquad (5\text{-}40)$$

dh_{L1}/dV_G may be obtained by differentiating equation (2-15) and using equation (5-25) to obtain the value of dV_1/dV_G as:

$$\frac{dh_{L1}}{dV_G} = \frac{1}{2h_{L1}}\frac{2\varepsilon}{qN_D}\left(\frac{g_m - M_{25}}{M_{24}}\right) \qquad (5\text{-}41)$$

And finally the equation for the gate-source capacitance in the saturation region is given by:

$$
\begin{aligned}
C_{gs} &= -\varepsilon W\left[\frac{qWN_D\mu_0}{I_D}a-\frac{\mu_0}{v_{sat}}\right]\left[h_{L1}-h_S\right]+\varepsilon W\frac{qWN_D\mu_0}{I_D}\left[V_1\right] \\
&+\varepsilon W\frac{qWN_D\mu_0}{I_D}\sqrt{\frac{N_A}{N_A+N_D}}\times \\
&\left[\sqrt{\left(V_1+U_{bi}\right)\left(V_1-V_G+V_{bi}\right)}-\sqrt{U_{bi}\left(-V_G+V_{bi}\right)}\right. \\
&-\frac{\left(U_{bi}+V_G-V_{bi}\right)}{2}\ln\frac{\sqrt{V_1+U_{bi}}-\sqrt{V_1-V_G+V_{bi}}}{\sqrt{U_{bi}}-\sqrt{-V_G+V_{bi}}}+ \\
&\left.\frac{\left(U_{bi}+V_G-V_{bi}\right)}{2}\ln\frac{\sqrt{V_1+U_{bi}}+\sqrt{V_1-V_G+V_{bi}}}{\sqrt{U_{bi}}+\sqrt{-V_G+V_{bi}}}\right] \\
&+\frac{\varepsilon W\left(L-L_1\right)}{h_{L1}}\left[\frac{g_m-M_{25}}{M_{24}}\right]
\end{aligned}
\tag{5-42}
$$

5.7 **The Gate-Drain Capacitance**

The gate-drain capacitance is defined as the differential change in the magnitude of the charge under the gate with respect to a differential change in the drain voltage. As shown in Annexure II the total charge under the gate in the linear region is given by the equation:

$$
\begin{aligned}
Q_1 &= \frac{q^2WN_D^2}{3\varepsilon}\left\{\frac{qWN_D\mu_0a}{I_D}-\frac{\mu_0}{v_{sat}}\right\}\left\{h_D^3-h_S^3\right\}-\frac{q^3W^2N_D^3\mu_0}{4\varepsilon I_D}\left\{h_D^4-h_S^4\right\} \\
&-\frac{2\varepsilon qN_DW^2\mu_0}{I_D}\sqrt{\frac{N_A}{N_A+N_D}}\left\{\frac{\sqrt{R_f}\left(2V_f+b\right)-\sqrt{R_i}\left(2V_i+b\right)}{4}\right. \\
&\left.+\frac{\Delta}{8}\ln\left[\frac{2\sqrt{R_f}+2V_f+b}{2\sqrt{R_i}+2V_i+b}\right]\right\}
\end{aligned}
\tag{5-43}
$$

where,

$$
\begin{aligned}
R_f &= \left[(-V_G + V_{bi})U_{bi} + (-V_G + V_{bi} + U_{bi})V_D + V_D^2\right] \\
R_i &= \left[(-V_G + V_{bi})U_{bi}\right] \\
V_f &= V_D \\
V_i &= 0 \\
b &= (-V_G + V_{bi} + U_{bi}) \\
\Delta &= 4(-V_G + V_{bi})U_{bi} - (-V_G + V_{bi} + U_{bi})^2
\end{aligned}
\tag{5-44}
$$

The total depletion charge under the gate in the saturation region is given by the equation as shown in Annexure II:

$$
\begin{aligned}
Q_1 = {} & \frac{q^2 W N_D^2}{3\varepsilon}\left\{\frac{qWN_D\mu_0 a}{I_D} - \frac{\mu_0}{v_{sat}}\right\}\left\{h_{L_1}^3 - h_S^3\right\} - \frac{q^3 W^2 N_D^3 \mu_0}{4\varepsilon I_D}\left\{h_{L_1}^4 - h_S^4\right\} \\
& - \frac{2\varepsilon q N_D W^2 \mu_0}{I_D}\sqrt{\frac{N_A}{N_A + N_D}}\left\{\frac{\sqrt{R_f}\left(2V_f + b\right) - \sqrt{R_f}\left(2V_f + b\right)}{4}\right. \\
& \left. + \frac{\Delta}{8}\ln\left[\frac{2\sqrt{R_f} + 2V_f + b}{2\sqrt{R_i} + 2V_i + b}\right]\right\} + qWN_D(L - L_1)h_{L_1}
\end{aligned}
\tag{5-45}
$$

where,

$$
\begin{aligned}
R_f &= \left[(-V_G + V_{bi})U_{bi} + (-V_G + V_{bi} + U_{bi})V_1 + V_1^2\right] \\
R_i &= \left[(-V_G + V_{bi})U_{bi}\right] \\
V_f &= V_1 \\
V_i &= 0
\end{aligned}
\tag{5-46}
$$

In the linear region of operation, equation (5-40) may be differentiated with respect to the drain voltage to obtain the expression for the gate-drain capacitance:

$$\frac{dQ_1}{dV_D} = \frac{q^2 W N_D^2}{\varepsilon}\left\{\frac{qWN_D\mu_0 a}{I_D} - \frac{\mu_0}{v_{sat}}\right\}\left\{h_D^2\frac{dh_D}{dV_D}\right\}$$
$$-\frac{q^2 W N_D^2}{\varepsilon}\frac{qWN_D\mu_0 a}{I_D^2}\left\{\frac{h_D^3 - h_S^3}{3}\right\}g_{ol}$$
$$-\frac{q^3 W^2 N_D^3\mu_0}{\varepsilon I_D}\left\{h_D^3\frac{dh_D}{dV_D}\right\} + \frac{q^3 W^2 N_D^3\mu_0}{\varepsilon I_D^2}\left\{\frac{h_D^4 - h_S^4}{4}\right\}g_{ol}$$
$$-\frac{2\varepsilon q N_D W^2\mu_0}{I_D^2}\sqrt{\frac{N_A}{N_A+N_D}}\left[\sqrt{R_f}\left(2\frac{dV_f}{dV_D}\right)\right.$$
$$\left.+\frac{1}{2\sqrt{R_f}}\frac{dR_f}{dV_D}\left(2V_f+b\right)+\frac{\Delta}{2}\frac{\frac{1}{\sqrt{R_f}}\frac{dR_f}{dV_D}+2\frac{dV_f}{dV_D}}{2\sqrt{R_f}+2V_f+b}\right]$$
$$+\frac{2\varepsilon q N_D W^2\mu_0 g_0}{I_D^3}\sqrt{\frac{N_A}{N_A+N_D}}\left\{\frac{\sqrt{R_f}\left(2V_f+b\right)-\sqrt{R_f}\left(2V_f+b\right)}{4}\right. \qquad (5\text{-}47)$$
$$\left.+\frac{\Delta}{8}\ln\left[\frac{2\sqrt{R_f}+2V_f+b}{2\sqrt{R_i}+2V_i+b}\right]\right\}$$

where,

$$\frac{dV_f}{dV_D} = 1$$
$$\frac{dR_f}{dV_D} = \left(-V_G + V_{bi} + U_{bi}\right)\frac{dV_f}{dV_D} + 2V_f\frac{dV_f}{dV_D} \qquad (5\text{-}48)$$
$$\frac{dh_D}{dV_D} = \frac{\varepsilon}{qN_D h_D}\left(\frac{dV_f}{dV_D}\right)$$

And finally the gate-drain capacitance in the saturation region is given by the equation:

$$
\begin{aligned}
\frac{dQ_1}{dV_D} &= \frac{q^2WN_D^2}{\varepsilon}\left\{\frac{qWN_D\mu_0 a}{I_D}-\frac{\mu_0}{v_{sat}}\right\}\left\{h_{L1}^2\frac{dh_{L1}}{dV_D}\right\} \\
&-\frac{q^2WN_D^2}{\varepsilon}\frac{qWN_D\mu_0 a}{I_D^2}\left\{\frac{h_{L1}^3-h_S^3}{3}\right\}g_{ol} \\
&-\frac{q^3W^2N_D^3\mu_0}{\varepsilon I_D}\left\{h_{L1}^3\frac{dh_{L1}}{dV_D}\right\}+\frac{q^3W^2N_D^3\mu_0}{\varepsilon I_D^2}\left\{\frac{h_{L1}^4-h_S^4}{4}\right\}g_{ol} \\
&-\frac{2\varepsilon qN_DW^2\mu_0}{I_D^2}\sqrt{\frac{N_A}{N_A+N_D}}\left[\sqrt{R_f}\left(2\frac{dV_f}{dV_D}\right)\right. \\
&\left.+\frac{1}{2\sqrt{R_f}}\frac{dR_f}{dV_D}\left(2V_f+b\right)+\frac{\Delta}{2}\frac{\frac{1}{\sqrt{R_f}}\frac{dR_f}{dV_D}+2\frac{dV_f}{dV_D}}{2\sqrt{R_f}+2V_f+b}\right] \\
&+\frac{2\varepsilon qN_DW^2\mu_0 g_o}{I_D^3}\sqrt{\frac{N_A}{N_A+N_D}}\left\{\frac{\sqrt{R_f}\left(2V_f+b\right)-\sqrt{R_f}\left(2V_f+b\right)}{4}\right. \\
&\left.+\frac{\Delta}{8}\ln\left[\frac{2\sqrt{R_f}+2V_f+b}{2\sqrt{R_i}+2V_i+b}\right]\right\}+qWN_D\left[\left(L-L_1\right)\frac{dh_{L1}}{dV_D}-h_{L1}\frac{dL_1}{dV_D}\right]
\end{aligned}
\tag{5-49}
$$

where:

$$
\begin{aligned}
\frac{dV_f}{dV_D} &= -g_o/M_{13} \\
\frac{dR_f}{dV_D} &= \left(-V_G+V_{bi}+U_{bi}\right)\frac{dV_f}{dV_D}+2V_f\frac{dV_f}{dV_D} \\
\frac{dh_{L1}}{dV_D} &= \frac{\varepsilon}{qN_Dh_{L1}}\frac{dV_f}{dV_D} \\
\frac{dL_1}{dV_D} &= -g_o\frac{M_{11}/M_{13}+1}{M_{12}}
\end{aligned}
\tag{5-50}
$$

5.8 **Results**

The small-signal parameters have been calculated for the ideal device having dimensions similar to that of the device fabricated by Sghaier *et al.* [31], assuming that both the source and the drain resistances are 50 Ω. The transistor has a gate length of 1 μm, a width of 2×250 μm, a buffer layer thickness of 0.3 μm, a

channel thickness of 0.3 μm, a channel doping level of 2×10^{17} cm^{-3} and a buffer doping of 1×10^{16} cm^{-3}. The distance between the source and the gate contact is 1 μm and that between the gate and the drain is 2 μm.

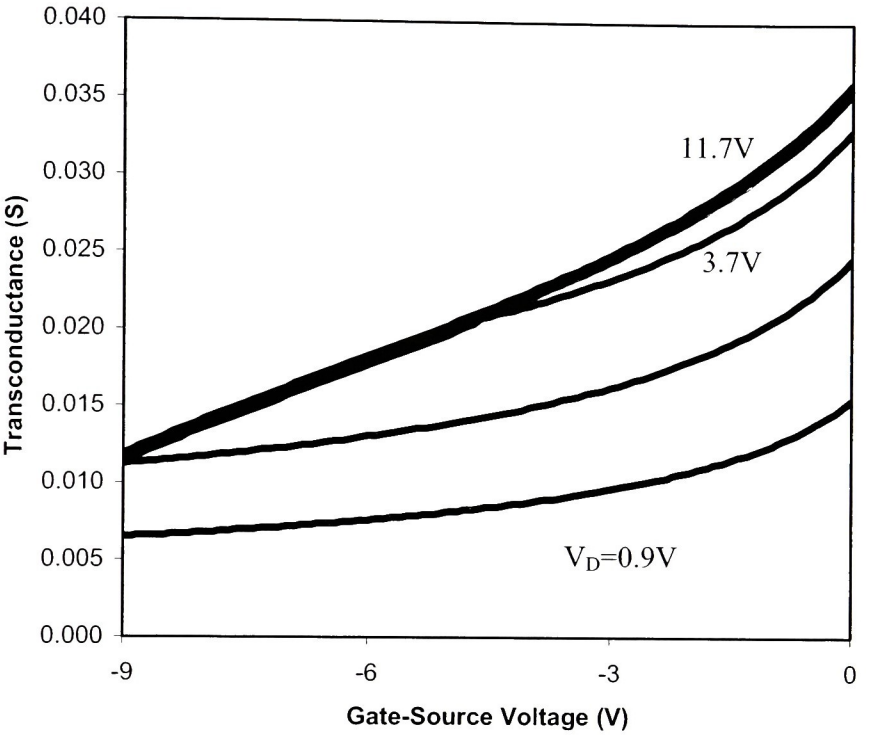


Fig. 5-2. The plot of transconductance as a function of the gate-source voltage with drain-source voltage as a parameter.

Fig. 5-2 depicts the plot of the transconductance of the device as a function of the gate bias with drain bias as a parameter. The transconductance steadily decreases with a decrease in the gate voltage both in the linear and the saturation region. In the saturation region, the transconductance is nearly independent of the drain voltage as may be observed from the lines that are closely packed lines in Fig, 5-2. This indicates that the output resistance in the saturation region is fairly constant. In the linear region however, the transconductance varies significantly with the drain voltage and is indicative of the fact that the slopes of the *I-V* characteristics are different for different drain voltages as expected. An extrapolation of the transconductance curve indicates a threshold voltage of about –12 V. The transconductance is maximum at

a gate voltage of 0 V and has a saturation value of around 35 mS. It decreases fairly linearly in the saturation region to a value of about 12 mS at a gate voltage of –9 V.

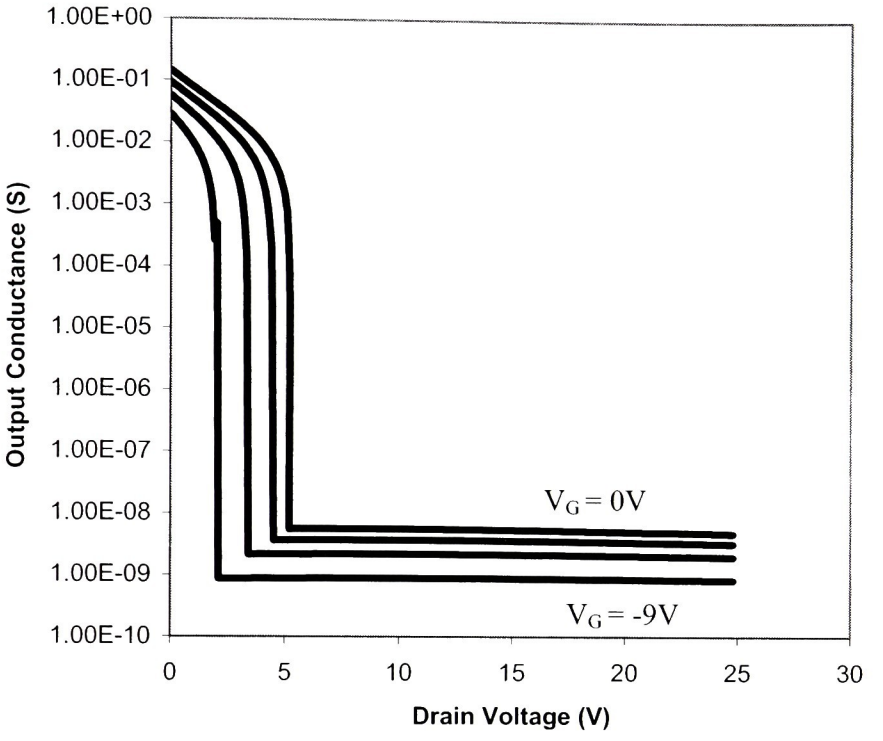


Fig. 5-3. The plot of the output conductance of the device as a function of the drain bias with gate bias as a parameter.

Fig. 5-3 shows the output conductance of the device as a function of the drain bias with gate bias as a parameter. The output conductance specified as the differential change in the drain current that occurs as a result of a differential change in the drain voltage. In the linear region, the current changes rapidly with an application of drain bias and thus it is expected that in the linear region the output conductance is going to be high. In the saturation region however, the drain current changes only slightly with a change in the drain voltage and this results in a very low value of output conductance. The output conductance is several orders of magnitude higher in the linear region than in the saturation region as seen in Fig. 5-4. In the linear region the value of the output conductance is about 0.1 S while in the saturation region the value of the output conductance is between 1×10^{-8} S and 1×10^{-9} S. Further, the output conductance at the gate voltage of 0V is

greater than the output conductance at the gate voltage of –9 V. This is expected since the drain current at a gate voltage of 0 V is greater than the drain current at a gate voltage of –9 V for example.

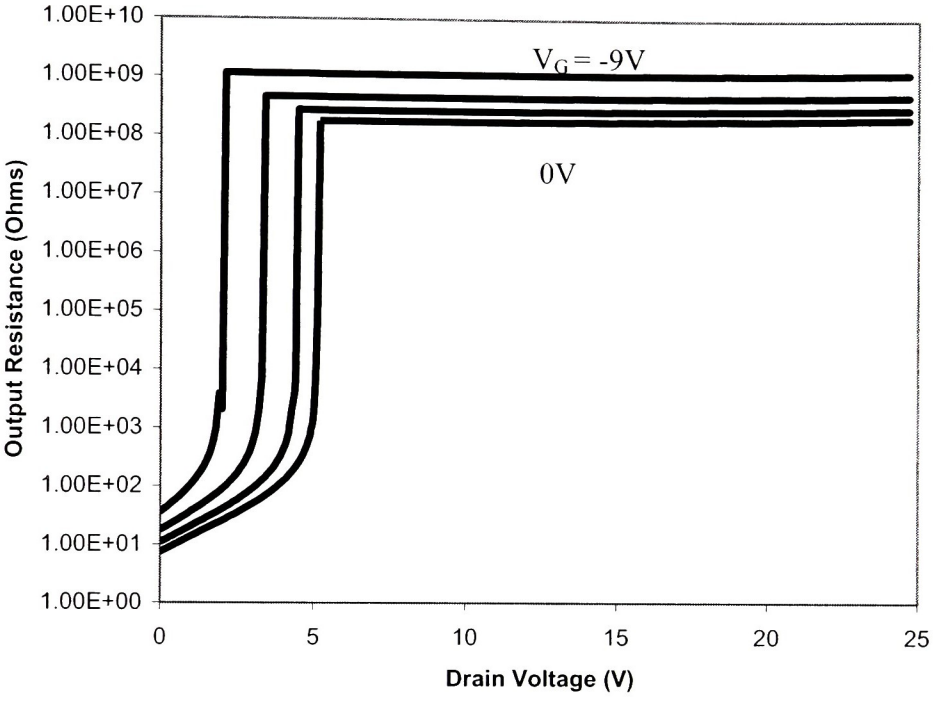


Fig. 5-4. Plot of the output resistance as a function of the drain voltage with gate voltage as a parameter.

Fig 5-4 depicts the output resistance of the device with respect to the drain voltage with the gate bias as a parameter. The output resistance is the inverse of the output conductance and is defined as the ratio of the differential change in the drain voltage with the corresponding differential change in the drain current. That is, it is the slope of the *I*-V characteristics. Here again, it can be seen that in the saturation region the output resistance is constant and independent of the drain bias. The output resistance in the saturation region is minimum for a gate bias of 0 V and steadily increases as the gate voltage becomes more and more negative. In the linear region the output resistance is around 10 Ω that increases to a value of about 10 GΩ at saturation.

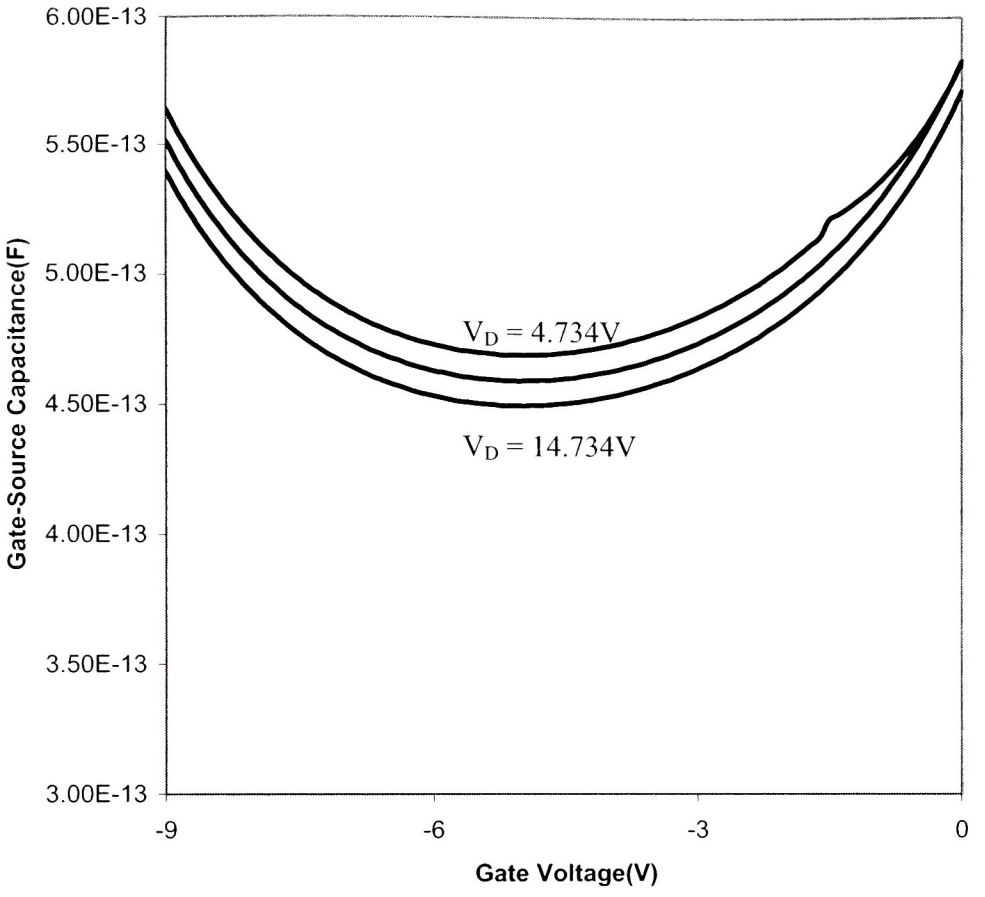


Fig. 5-5. A plot of the gate-source capacitance as a function of the gate-source voltage with drain-source voltage as a parameter.

The gate-source capacitance is plotted as a function of the gate-source voltage, with the drain voltage as a parameter in Fig. 5-5. The gate-source capacitance changes very little with changing gate voltage. It is seen that the capacitance decreases with decreasing gate voltage between gate voltages of 0 V and -5 V and increases thereafter. The capacitance is of the order of 0.5 pF. In the absence of the buffer layer, the gate-source capacitance continuously decreases with decreasing gate bias, while in the presence of the buffer layer it can be seen that the gate-source capacitance after saturation is affected by the increase in the thickness of the lower depletion region and increases with decreasing gate voltage. This is probably due to the following reason: When the drain voltage is held constant and the gate voltage is decreased, the

current decreases as well. In saturation, the channel opening is fairly constant and so the channel resistance is fairly constant also. This results in an overall decrease in the channel potential over most part of the channel. This results in a decrease in the thickness of the lower part of the channel. As a result, a greater amount of space is present for the upper depletion region to expand into. Thus the total charge under the depletion region increases more rapidly, increasing the gate-source capacitance.

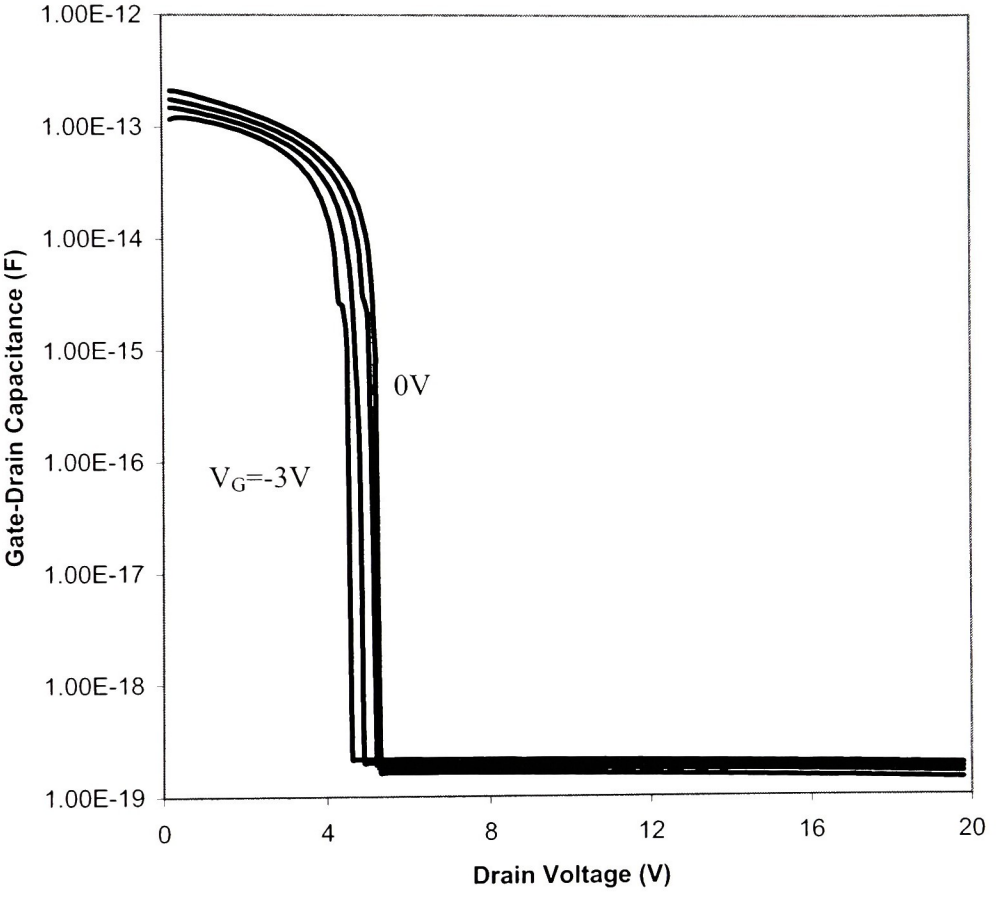


Fig. 5-6. A plot of the gate-drain capacitance as a function of the drain voltage with gate bias as a parameter.

The gate-drain capacitance is plotted as a function of the gate-drain voltage in Fig. 5-6. In the linear region, the capacitance is high and decreases significantly as the drain voltage increases. At saturation the value of the gate-drain capacitance is several orders of magnitude lower than that of the value present at a drain voltage of 0 V. As the drain voltage rises and the channel saturates, the depletion region just under the gate

changes very little and as a result, the gate-drain capacitance is very low. In the linear region very close to a drain voltage of 0 V, the gate-drain capacitance is about 0.1 pF and when the channel saturates, the gate-drain capacitance is about 0.1 aF.

Chapter 6

Conclusions and Future Work

6.1 Conclusion

A physics-based model has been proposed for modeling the non-ideal effects of the SiC MESFET, and small signal parameters have been derived. The model incorporates the effects of surface and substrate traps and thermal degradation of current. It also incorporates source and drain resistances and the depletion region at the channel/buffer interface. The derived *I-V* model has been applied to model two devices. The first device was fabricated and measured by Sghaier *et al.* [31], while the second device was by Huang *et al.* [44].

The device fabricated by Sghaier *et al.* had a very thin buffer, and thus it can be seen that there is significant degradation due to the substrate trapping effects, while the device fabricated by Huang *et al.* had a very thick buffer layer and it may be seen that for this device the substrate trapping effect has been significantly reduced. This is also corroborated from the proposed theory wherein the channel carrier concentration is varied temporally to model the substrate trapping phenomenon. Thus, a thick and highly doped buffer layer is better at avoiding substrate-trapping effects. It can also be seen from Fig. 3-13 that thermal-effects and substrate trapping effects are not independent of each other but need to be considered together if the actual nature of the traps are needed to be modeled.

Surface traps capture electrons and extend the depletion beyond the gate and their effects have been incorporated by assuming a bias-dependent drain resistance. Various methods may be used for mitigating the effects of the surface traps. One method of doing that is to use a trench MESFET structure. This reduces the electric field between the source and the drain. As a result of the reduction of the electric field between the drain and the source, the propensity for surface traps to capture electrons is reduced. Another method of reducing surface trapping is to grow an oxide at the surface. This makes it more difficult for the electrons to

reach the surface traps. A thin layer of nitride at the two ends of the gate can further reduce the effects of the surface traps. Another method of preventing the effect of surface traps is to introduce a spacer layer between the surface and the channel (much like the introduction of the buffer layer between the channel and the substrate.) When surface states capture electrons, the resulting depletion region is formed within the spacer layer and thus does not affect the current flowing in the channel.

The modeling of the trapping has been kept semi-empirical because accurate and complete trapping levels and trap densities were not obtainable for the MESFETs for which the *I-V* relationships were obtained.

A small-signal model has been proposed for the SiC MESFET. The ideal output conductance, transconductance, gate-source and gate-drain capacitance have been derived. The small signal model that has been proposed takes into account the drain and source resistances, and the depletion region at the channel/buffer interface. These may be used for finding the theoretical operational limit of the SiC MESFET.

6.2 Future Work

Derivation of all equations in this thesis has assumed that the depletion approximation shall hold under all circumstances. When the buffer layer concentration is very low, this assumption is not valid. Electronic repulsive forces between the channel electrons influence the behavior of the current, especially in the saturation region. For very lightly doped buffer, there is significant dispersion of the channel electrons and a consequent decrease in the output resistance. The nature of the current dispersion resulting from electron-trap scattering is being investigated.

The proposed model is intended to be used in a device simulator. Device simulators such as Spectre® use device models by SPICE® or BSIM® parameter files. Thus, the model can be used only if either SPICE® or BSIM® parameters of the device are extracted. SPICE® level parameters have not been extracted yet. Extraction of the SPICE® parameters are heuristic in nature and entail semi-empirical measurements tailored to a particular device. Extraction of either SPICE® or BSIM® parameters that can faithfully model a device, the characteristics of which are significantly deteriorated by temperature dependent trapping effects, is inherently difficult. A methodology for extraction of SPICE® or BSIM® parameters of these

devices would be invaluable, since only then can actual circuits using these devices be simulated and verifiable circuit performance obtained. Only then can circuit performance of SiC based devices be tested against circuit performances of devices made of other materials.

The frequency characteristics of a device are determined mainly by the $1/f$ noise of the system. In SiC, the primary cause of the $1/f$ noise is trapping. A tractable mathematical model that physically describes the trapping phenomenon is still absent. A methodology for obtaining dispersion characteristics using basic trapping phenomenon is imminent and shall be undertaken shortly.

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Appendix I

2D Device Simulation

This appendix explains the 2D device simulation that has been used in various places in the thesis. This appendix introduces the method of use of the Atlas® device simulator as a tool for augmenting the theoretical analysis that has been done in this thesis. Section I.1 is a brief introduction of 2D modeling, the different simulators currently in use for device modeling purposes, and a brief introduction of the DeckBuild® package. Section I.2 describes the Atlas device simulator in greater detail. Section I.3 describes the models and model parameters that have been used for simulation purposes. Section I.4 is a brief summary of all the models and parameters.

I.1 Introduction

This chapter describes the physical models used in the Atlas® [57] device simulator for the simulation of the SiC MESFET. Device simulation software provides in-depth insight into the physical mechanisms of the device control the operation. Graphical descriptions of the electric field distributions, potential profiles, carrier charge concentrations and thermal profiles may be obtained. Presently a number of device simulators are commercially available, such as MEDICI [58], PISCES [59] and MINIMOS [60]. In this work, the ATLAS device simulator has been used.

The ATLAS simulation software is part of a much bigger simulation suite from Silvaco International geared toward the simulation of processes, devices and circuits. The suite contains a set of graphical user interface (GUI) based tools for simplifying the use of the simulator itself. These tools are described below:

DeckBuild — This is an integrated simulation environment having a simple and effective GUI. Simulation commands may be directly typed into this environment. It has the capability of running any one of the simulators or tools in the background and executing script files relative to the particular simulator. This obviates the need for having different script files for different simulators. Thus DeckBuild allows for the possibility of having one script

file that creates a structure using a process simulator (ATHENA for example), plots the resultant structure using the plotting tool (TonyPlot), re-meshing the structure using a device-editing tool (DevEdit) and finally simulating the resultant device using a device simulation software (ATLAS) all using the same script file. Furthermore, multiple simulations of the same or different devices may be performed using the same script file. Besides, menus for automatically generating script commands are also provided. These menu items automatically update, depending upon the type of simulator running in the background: Atlas, Athena, etc.

TonyPlot — This is graphing software and is part of the device simulation software suite. It is able to plot one- and two-dimensional structure files generated by any of the simulation tools provided by Silvaco. Apart from plotting structure files, it also has the capability of plotting user datafiles, and log files containing I-V characteristics, C-V characteristics, S-parameters and so on. Real data may be plotted with line plots, complex data can be plotted with polar plots and S-parameter data may be plotted with Smith charts. Apart from plotting, it has various other amenities, such as tools for creating movies, Poisson solvers and integrators for calculating areas under the plots.

DevEdit — This is a GUI based software capable of editing device geometries and meshes. It is useful in changing device geometries created using the ATLAS simulator. It has a number of powerful automated meshing algorithms that may be used for expediting the meshing process based upon various process parameters such as the net and total doping of the structure. Further, meshes can be refined by the user at any point using the refining tools available.

ATLAS is a device-simulation software from Silvaco International [61]. It is a very versatile software incorporating the following simulators:

- S-Pisces, a 2D silicon device simulator,

- TFT2D, an amorphous and polycrystalline device simulator,
- Ferro, a ferro electric field dependent permittivity model,
- Blaze, a 2D and 3D device simulator for advanced materials,
- LASER, a semiconductor LASER diode simulator,
- VCSEL, a vertical cavity surface emitting LASER simulator,
- Luminous, an optoelectronic device simulator,
- Giga, a non-isothermal device simulatior
- MixedMode, a circuit simulator fro advanced devices,
- Quantum, a simulation model for quantum-confinement models, and
- Noise, a 2D small signal noise generator.

ATLAS has the capability of solving numerous types of devices, which may be either one-dimensional or two-dimensional or even three-dimensional. The MESFET is essentially a planar two-dimensional device having lateral symmetry and thus it is both necessary and sufficient (in the present case) to solve a two-dimensional cross-section of the MESFET.

I.2 Device Simulation

The ATLAS device simulator typically solves the following coupled equations in two-dimensions [62]:

- The Poisson equation:

$$\vec{\nabla}\left(\varepsilon\vec{\nabla}\psi\right)=-\rho\,. \tag{I-1}$$

- The electron and the hole carrier continuity equations, and

$$\frac{\partial n}{\partial t}=\frac{1}{q}\vec{\nabla}\bullet\vec{J}_n+G_n-R_n, \tag{I-2}$$

$$\frac{\partial p}{\partial t}=\frac{1}{q}\vec{\nabla}\bullet\vec{J}_p+G_p-R_p\,. \tag{I-3}$$

- The current transport equations,

$$\vec{J}_n=qD_n\vec{\nabla}n-qn\mu_n\vec{\nabla}\psi-\mu_n n\left(kT_L\vec{\nabla}\left(\ln n_{ie}\right)\right), \tag{I-4}$$

$$\vec{J}_p = qD_p\vec{\nabla}p - qp\mu_p\vec{\nabla}\psi - \mu_p p\left(kT_L\vec{\nabla}(\ln n_{ie})\right), \tag{I-5}$$

where ψ is the electrostatic potential, ε is the local permittivity, ρ is the charge density, n and p are the electron and hole concentrations, t is the time, q is the charge of the electron, J_n and J_p are the electron and hole current densities, G_n and G_p are the generation rates of electrons and holes, respectively, R_n and R_p are the recombination rates of electrons and holes, respectively, D_n and D_p are the electron and hole diffusivities, respectively, μ_n and μ_p are the electron and hole mobilities respectively, k is the Boltzmann constant, T_L is the lattice temperature and n_{ie} is the intrinsic carrier concentration. In Atlas, energy balance transport model can be selected instead of simple drift-diffusion model, to account for non-local lattice heating effects using the energy balance equations:

$$\vec{J_n} = qD_n\vec{\nabla}n - \mu_n n\vec{\nabla}\psi + qnD_n^T\vec{\nabla}T_n, \tag{I-6}$$

$$\vec{S_n} = -K_n\vec{\nabla}T_n - \left(\frac{k\delta_n}{q}\right)\vec{J_n}T_n, \tag{I-7}$$

$$\vec{J_p} = qD_p\vec{\nabla}p - \mu_p p\vec{\nabla}\psi + qpD_p^T\vec{\nabla}T_p, \text{ and} \tag{I-8}$$

$$\vec{S_p} = -K_p\vec{\nabla}T_p - \left(\frac{k\delta_p}{q}\right)\vec{J_p}T_p, \tag{I-9}$$

where T_n and T_p represent the electron and hole temperatures, and S_n and S_p is the flux of heat from the carrier to the lattice. While using the simulator, either all of the above equations may be solved simultaneously or, optionally, only relevent equations may be solved to obtain the solution. For example, if a solution for a field-effect device having electrons as the majority carriers need to be obtained, then the equations relating hole currents may be turned off. Similarly, when lattice-heating effects are negligible, the energy-balance equations need not be evaluated and drift-diffusion equations can be selected.

I.3 Models and Model Parameters

The results of the simulation are accurate only if the models used for the simulations and the values of the parameters of the models are properly selected. SiC being a newer material compared to Si or GaAs, the default values of the various model parameters used in the simulator are generally insufficient to correctly

model the current-voltage and other characteristics of the SiC MESFET. In this section, the models that have been used, the reasons for using the models and the values used in the models are presented.

I.3.1 Parameters for Carrier Statistics

These parameters define the type of functions to be used for the probability of occupancy, the density of states, the intrinsic carrier concentration, the energy bandgap, *etc.* Thus, these parameters are used for defining the characteristics of the materials used in the device. The models needed to be set and the values of the parameters used in the equations describing the models are detailed next. These parameters may be changed using the MODELS statement in ATLAS.

The Probability of Occupancy

Boltzmann statistics are used by default in the ATLAS simulator but may be specifically turned on by using the BOLTZMAN parameter of the MODEL command. This is a much simpler model for describing the probability of occupancy of carriers in a subband and is subsequently much faster to implement. Being the simple model, it is not as comprehensive as Fermi-Dirac statistics. For simple and faster analysis Boltzmann statistics has been used in the present work. However, Fermi-Dirac statistics may be used for simulations by using the FERMIDIRAC option in the MODEL statement.

The Density of States

The effective density of states in ATLAS is modeled by the following equations:

$$N_C(T_L) = 2\left(\frac{2\pi m_e^* kT_L}{h^2}\right)^{\frac{3}{2}} = \left(\frac{T_L}{300}\right)^{\frac{3}{2}} \mathrm{NC300}\,, \text{ and} \tag{I-10}$$

$$N_V(T_L) = 2\left(\frac{2\pi m_h^* kT_L}{h^2}\right)^{\frac{3}{2}} = \left(\frac{T_L}{300}\right)^{\frac{3}{2}} \mathrm{NV300}, \tag{I-11}$$

where m_e^* is the effective mass of electrons, m_h^* is the effective mass of holes, h is Plank's constant, **NC300** is the conduction-band density-of-states at 300 K and **NV300** is the valence band density-of-states at 300 K. The values of the density of states for SiC may be specified by setting the **NC300** and **NV300**

parameters of the MODEL statement. For SiC, **NC300** = 1.6887 × 10^{19} cm^{-3} and **NV300** = 2.4942 × 10^{19} cm^{-3} respectively, obtained from the calculation of effective masses of electrons [63] and holes [64].

The Intrinsic Carrier Concentration

ATLAS calculates the effective intrinsic carrier concentration from the density of states and the energy bandgap using the formula:

$$n_{ie} = \sqrt{N_C N_v}\exp\left(\frac{-E_g}{2kT_L}\right), \tag{I-12}$$

and so there is no need to mention the intrinsic carrier concentration explicitly. The energy bandgap needs to be provided, however, and its value is described in the next section.

The Energy Bandgap

The energy bandgap of SiC is given by the equation [2]:

$$E_g(T_L) = E_g(0) - 6.5\times10^{-4}\left[\frac{T_L^2}{T_L + 1300}\right], \tag{I-13}$$

where $E_g(0)$ is the energy bandgap of SiC at 0K. ATLAS models the energy gap in a manner very similar to (I-13) by the equation

$$\begin{aligned} E_g(T_L) &= E_g(0) - \mathrm{EGALPHA}\left[\frac{T_L^2}{T_L + \mathrm{EGBETA}}\right] \\ &= \mathrm{EG300} + \mathrm{EGALPHA}\left[\frac{300^2}{300 + \mathrm{EGBETA}} - \frac{T_L^2}{T_L + \mathrm{EGBETA}}\right]. \end{aligned} \tag{I-14}$$

Comparing the above two equations, the values of **EGALPHA** and **EGBETA** are obtained as 6.5 × 10^{-4} eV/K and 1300 K, respectively. Furthermore, the value of the energy gap at 300K (**EG300**) is 3.23 eV. These values can be set by setting the **EGALPHA**, **EGBETA** and **EG300** parameters of the MODELS statement.

I.3.2 Boundary Conditions

ATLAS solves for numerous boundary conditions. Some of the boundary conditions that ATLAS solves for are: ohmic contacts, Schottky contacts, floating contacts, insulating contacts, *etc.* For the purpose of modeling MESFETs, two ohmic contacts are needed for specifying the boundary conditions of the source and the drain and one Schottky contact for the gate needs to be specified. The following sections detail the parameters necessary for the specification of each type of contact. Although lumped resistances, capacitances and inductances may be specified for each of the contacts, these have been purposefully neglected since the whole intention of the two-dimensional simulations are to be able to observe the nature of the electric field distributions, potential distributions, carrier concentrations *etc.* within the intrinsic device leading to greater insight of the physical mechanisms inside the device itself, rather than obtaining parameter models for the simulation purposes.

Ohmic Contacts

Ohmic contacts are modeled in ATLAS by making the majority and the minority quasi-fermi potential equal to the applied bias, while the surface potential, the hole concentration and the electron concentrations are fixed. This is the Dirichlet boundary condition. For making a contact ohmic, it is necessary to include the statement **NEUTRAL** in the CONTACT statement.

Schottky Contacts

The surface potential at the Schottky contact is defined in ATLAS by the equation:

$$\psi_s = \text{AFFINITY} + \frac{E_g}{2q} + \frac{kT_L}{2q}\ln\left(\frac{N_C}{N_V}\right) - \text{WORKFUNCTION} + \text{V}_{\text{applied}}, \quad \text{(I-15)}$$

where **AFFINITY** is the electron affinity of the semiconductor, $\text{V}_{\text{applied}}$ is the value of the applied bias and **WORKFUNCTION** is the workfunction of the contact, both of which are expressed in eV. The value of the electron affinity of SiC is assumed to be 3.08 eV [65]. In general, the material workfunction is determined from the Schottky barrier height of the metal-semiconductor contact. Generally the barrier height is determined by the type of metal and the type of semiconductor material used for making the Schottky junction and may be readily measured. The barrier heights of several metals with respect to SiC

have been documented [66], some of them being the barrier height between SiC and Au (1.73-1.8 eV), that between SiC and Ni (1.6-1.7 eV) and that between SiC and Ti (1.1-1.15 eV). Generally gate metals are composed of stacks of metals and the process of annealing reduces the total barrier height to the vicinity of 1.2 eV [67]. The **WORKFUNCTION** parameter needs to be specified in the CONTACT statement while the **AFFINITY** parameter needs to be specified in the MODELS statement.

I.3.3 Physical Models

Physical models comprise models for electrical characteristics such as carrier mobility, carrier-carrier scattering and carrier generation and recombination. These models determine the electrical characteristics of devices created of the material. Models that have been incorporated into this work and relevant parameters are discussed in the following sections.

Carrier Mobility Model

Electrons are the majority carriers in the SiC MESFET having an n-type channel. Thus only the electron current density equations of the drift-diffusion model have been solved. The physical parameters are evaluated for electrons only. This is specified in ATLAS® by the statement:

MODELS NUMCARR=1 ELECTRONS

The carrier mobility models that have been used in this work, account for the concentration dependence, the temperature dependence and the field dependence of electron mobility. The concentration dependence and temperature dependence of the low-field mobility is modeled using the Caughey-Thomas model. This model may be selected by using the ANALYTIC parameter of the MODELS statement. The formula used for the Caughey-Thomas [35] model is given by:

$$\mu_{n0} = \mathrm{MU1N.CAUG}\left(\frac{T_L}{300}\right)^{\mathrm{ALPHAN.CAUG}} + \frac{\mathrm{MU2N.CAUG}(T_L/300)^{\mathrm{BETAN.CAUG}} - \mathrm{MU1N.CAUG}(T_L/300)^{\mathrm{ALPHAN.CAUG}}}{1+(T_L/300)^{\mathrm{GAMMAN.CAUG}}(N/\mathrm{NCRIT.CAUG})^{\mathrm{DELTAN.CAUG}}} \quad \text{(I-16)}$$

As shown in Chapter 2, the greater the doping of the material, the lower the mobility. The mobility is maximum in an intrinsic material where N (the doping concentration) is zero. This is given by **MU2N.CAUG**. As doping increases, the mobility steadily decreases until it asymptotically approaches the lowest value which is given by **MU1N.CAUG** . **NCRIT.CAUG** is the doping concentration at which the mobility value is equal to the arithmetic mean of the maximum and minimum values of mobility. The temperature dependence of mobility is given by the parameters **ALPHAN.CAUG**, **BETAN.CAUG**, **GAMMAN.CAUG** and **DELTAN.CAUG**. The value of the parameter **MU1N.CAUG** is 40 cm^2/Vs, that of **MU2N.CAUG** is 950 cm^2/Vs, **ALPHAN.CAUG** is –0.5, **BETAN.CAUG** is –2.4, **NCRIT.CAUG** is 2 $\times$ 10^{17} cm^{-3}, **DELTAN.CAUG** is 0.76 and **GAMMAN.CAUG** is –0.76 [35]. The mobility of electrons and holes decreases at high fields until the carrier velocity saturates. When the electric field (given by the variable E) is zero, the value of the mobility is equal to the low-field mobility (μ_{n0}). At very high values of electric field, the value of the mobility approaches a value equal to the saturation velocity divided by the electric field. The parallel field-dependent mobility is turned on by the FLDMOB parameter of the MODELS statement. This uses the following formula to calculate the field-dependent mobility function:

$$\mu_n(E) = \mu_{n0}\left[\frac{1}{1+\left(\frac{\mu_{n0}E}{\text{VSATN}}\right)^{\text{BETAN}}}\right]^{\frac{1}{\text{BETAN}}}, \qquad \text{(I-17)}$$

where **BETAN** is assumed to be 1. The value of **VSATN**, the saturation velocity of the electrons is calculated using the equation:

$$\text{VSATN} = \frac{\text{ALPHAN.FLD}}{1+\text{THETAN.FLD}\exp\left(\frac{T_L}{\text{TNOMP.FLD}}\right)}, \qquad \text{(I-18)}$$

where the value of **ALPHAN.FLD** is 4.77 $\times$ 10^7 cm/s, **THETAN.FLD** is 0.6 and **TNOMP.FLD** is 600 K [35].

Generation-Recombination Models

ATLAS provides a number of carrier generation-recombination models, primary among them being the SHR recombination model, the radiative recombination model, the Auger recombination model and a surface recombination model. Some of the modes have slight variations in various implementations. For example, ATLAS implements three different types of Auger recombination models – the 'Standard Auger Recombination' model, the 'Klaassen's Carrier Concentration Dependent' model and the 'Narrow Bandgap Auger' model. Further, various impact ionization models are also available to be used in the presence of high electrical stress when impact ionization cannot be neglected. In this dissertation simple SRH and Auger recombination models have been used and impact ionization has been neglected.

SHR Recombination Model

The electron-phonon interaction in the SiC MESFET has been implemented by using the SHR recombination model. ATLAS implements three different types of SHR recombination models. The SHR recombination model used for this dissertation is the concentration independent SHR model. This also happens to be the simplest of the SHR recombination models available in ATLAS. This model is defined in ATLAS by the following equation:

$$R_{SHR} = \frac{pn - n_{ie}^2}{\mathrm{TAUP0}\left[n + n_{ie}\exp\left(\frac{\mathrm{ETRAP}}{kT_L}\right)\right] + \mathrm{TAUN0}\left[p + n_{ie}\exp\left(\frac{-\mathrm{ETRAP}}{kT_L}\right)\right]}, \quad \text{(I-19)}$$

where **TAUP0** and **TAUN0** are the hole and electron lifetimes and **ETRAP** is the difference between the trap level and intrinsic-Fermi level. The value of **TAU0** used for the purpose of the simulations is 6.0×10^{-7} s and that of **TAUN0** is 1.0×10^{-9} s. **ETRAP** is taken as 0.0 since the vanadium-doped SiC substrate has levels very close to the middle of the energy gap. This feature is turned on but the SHR parameter of the MODELS statement.

Auger Recombination Model

As mentioned above, there are three different types of Auger recombination models available to use in the ATLAS® simulator. In this dissertation, the 'Standard Auger' recombination model has been chosen, again

for the sake of simplicity. The standard Auger recombination model has been implemented in ATLAS® using the following equation:

$$R_{Auger} = AUGN\left(pn^2 - nn_{ie}^2\right) + AUGP\left(np^2 - pn_{ie}^2\right), \quad \text{(I-20)}$$

where **AUGN** and **AUGP** are the Auger recombination coefficients at 300 K. Their values for SiC are 5×10^{-31} cm^6/s and 2×10^{-31} cm^6/s respectively [2].

Summary

This appendix enumerated the models and parameters used for the ATLAS® simulator. Tables I-I summarizes the parameters used for defining the various models used for the MODELS® statement. Table I-II summarizes the parameter specification for boundary value specification. Table I-III summarizes the values of the parameters used for the various models used in defining the models in the MODELS statement. This model may be turned on by using the AUGER parameter of the MODELS statement.

Table I-I. Parameters for defining the models in the MODELS statement.

Parameter	Value	Description
BOLTZMAN		Specifies that Boltzmann statistics rather than Fermi-Direc statistics is going to be used during simulations.
NUMCARRIERS ELECTRONS	1	Specifies that only equations for electrons shall be solved.
ANALYTIC		Specifies that the Caughey-Thomas model for the low-field mobility is going to be used during simulations.
FLDMOB		Specifies that the field-dependent model for the mobility is going to be used during simulations.
SHR		Specifies that the concentration independent SHR recombination model is used during simulations.
AUGER		Specifies that the standard Auger recombination model is used during simulations.

Table I-II. Parameters for defining the boundary-value conditions in the CONTACT statement.

Parameter	Value	Description
NEUTRAL		Specifies that the contact in question is an ohmic contact. This is specified for the gate and the drain contacts.
WORKFUNCTION	1.2 eV [12].	Specifies that the contact in question is a Schottky contact. This is specified for the gate contact.

Table I-III. Summary of the values of the model parameters used in the MODELS statement.

Parameter	Variable name in ATLAS	Units	Value	Reference
Material Parameters:				
Conduction band density of states at 300K	**NC300**	cm^{-3}	1.6887×10^{19}	[63]
Valence band density of states at 300K	**NV300**	cm^{-3}	2.4942×10^{19}	[64]
Energy Gap at 300K	**EG300**	eV	3.23	[2]
Parameter representing the temperature dependency of the bandgap	**EGALPHA**	eV/K	6.5×10^{-4}	[2]
Parameter representing the temperature dependency of the bandgap	**EGBETA**	K	1300	[2]
Electron Affinity	**AFFINITY**	eV	3.08	[65]
Low-Field Mobility Parameters: *The Caughey-Thomas Mobility Model*				
Caughey-Thomas mobility parameter	**MU1N.CAUG**	cm^2/Vs	40	[35]
Caughey-Thomas mobility parameter	**MU2N.CAUG**	cm^2/Vs	950	[35]
Caughey-Thomas mobility parameter	**NCRIT.CAUG**	cm^{-3}	2×10^{17}	[35]
Caughey-Thomas mobility parameter	**ALPHAN.CAUG**	-	-0.5	[35]
Caughey-Thomas mobility parameter	**BETAN.CAUG**	-	-2.4	[35]
Caughey-Thomas mobility parameter	**GAMMAN.CAUG**	-	-0.76	[35]
Caughey-Thomas mobility parameter	**DELTAN.CAUG**	-	0.76	[35]
Field-Dependence of Mobility Parameters:				
Field-dependent mobility parameter	**BETAN**	-	1	[35]
Field-dependent mobility parameter	**ALPHAN.FLD**	cm/s	4.77×10^{7}	[35]
Field-dependent mobility parameter	**THETAN.FLD**	-	0.6	[35]
Field-dependent mobility parameter	**TNOMP.FLD**	K	600	[35]
SHR Recombination Parameters:				
Hole lifetime	**TAUP0**	s	6.0×10^{-7}	[2]
Electron Lifetime	**TAUN0**	s	1.0×10^{-9}	[2]
Trap Level for SHR recombination	**ETRAP**	eV	0	
Auger Recombination Parameters:				
Auger recombination coefficient	**AUGN**	cm^6/s	5×10^{-31}	[2]
Auger recombination coefficient	**AUGP**	cm^6/s	2×10^{-31}	[2]

Appendix II

Determination of Q_1

This appendix describes the analysis used for determining the charge in the depletion region in the channel under the gate formed as a result of the applied bias voltages. This charge changes as the gate bias or the drain bias changes. The differential change in the magnitude of this charge with respect to the differential change in the bias voltages defines the capacitance formed between the gate and source and that formed between the gate and the drain. Thus the determination is essential before the capacitances of the device may be obtained.

First, the charge just under the gate is determined for the linear region of operation of the MESFET. It will then be obtained for the saturation region of operation. As may be expected, the basic methodologies of obtaining the solution for Q_1 while the MESFET is operating in the either mode are largely similar to one-another.

Q_1 in the Linear Region of Operation

The charge under the gate is given by:

$$Q_1 = qWN_D \int_0^L h(x)dx . \tag{II-1}$$

The current equation in the linear region of operation is given by:

$$I_D = qWN_D \frac{dV}{dx}[a - h(x) - h_1(x)] \frac{\mu_0}{1 + \frac{\mu_0}{v_{sat}} \frac{dV}{dx}}, \tag{II-2}$$

which may be rewritten as:

$$dx = \left\{ \frac{qWN_D\mu_0}{I_D}[a - h(x) - h_1(x)] - \frac{\mu_0}{v_{sat}} \right\} dV . \tag{II-3}$$

Equation (II-3) may be used for variable substitution in equation (II-1). Assuming source is tied to the ground, the lower limit changes to (0), which is the value of the channel potential at $x = 0$, while the higher

limit changes to (V_D), which is the value of the channel potential at $x = L$. Thus the equation would change to:

$$Q_1 = qWN_D \int_0^{V_D} h(x)\left\{\frac{qWN_D\mu_0}{I_D}\left[a - h(x) - h_1(x)\right] - \frac{\mu_0}{v_{sat}}\right\}dV \,. \qquad \text{(II-4)}$$

The relationship between the channel potential, the height of the depletion region under the gate ($h(x)$) and the height of the depletion region in the channel at the interface between the channel and the buffer ($h_1(x)$) is given by the equations (II-5) and (II-6), respectively.

$$h(x) = \sqrt{\frac{2\varepsilon}{qN_D}\left(-V_G + V_{bi} + V(x)\right)}, \qquad \text{(II-5)}$$

$$h(x) = \sqrt{\frac{2\varepsilon}{qN_D}\left(U_{bi} + V(x)\right)}. \qquad \text{(I-6)}$$

An equation relating the differential change in the height of the depletion region under the gate with a differential change in the channel potential may be obtained by (first squaring both sides of equation (II-5)) and then taking differential of equation (II-5) w.r.t. The resulting equation is given by:

$$\frac{qN_D h(x)}{\varepsilon} dh(x) = dV \,. \qquad \text{(II-7)}$$

Equations (II-5), (II-6) and (II-7) may be used in conjunction with equation (II-4) to obtain the final form of the equation before integration is carried out and is given by:

$$\begin{aligned} Q_1 = {} & qWN_D\left\{\frac{qWN_D\mu_0 a}{I_D} - \frac{\mu_0}{v_{sat}}\right\}\int_{h_S}^{h_D} \frac{qN_D h}{\varepsilon} h\, dh \\ & - \frac{q^2W^2N_D^2\mu_0}{\varepsilon I_D}\int_{h_S}^{h_D} \frac{qN_D h}{\varepsilon} h^2\, dh \\ & - \frac{2\varepsilon qN_D W^2\mu_0}{I_D}\sqrt{\frac{N_A}{N_A + N_D}}\int_{I_D R_S}^{V_D - I_D R_D} \sqrt{\left[(-V_G + V_{bi})U_{bi} + (-V_G + V_{bi} + U_{bi})V + V^2\right]}dV \end{aligned} \qquad \text{.(II-8)}$$

Among the three integral terms in (II-8), integration the first two integrals are trivial. The last integration has been solved using the identities described in Ref. [68]. If $R = a + bt + ct^2$, and $\Delta = 4ac - b^2$, the following relations hold:

$$\int\sqrt{R} = \frac{(2cx+b)\sqrt{R}}{4c} + \frac{\Delta}{8c}\int\frac{dx}{\sqrt{R}}, \text{ and} \qquad \text{(II-9)}$$

$$\int\frac{dx}{\sqrt{R}} = \frac{1}{\sqrt{c}}\ln\left(2\sqrt{cR} + 2ct + b\right) \qquad [c>0] \qquad \text{(II-10)}$$

In the third integral, comparing the coefficients of $\left[(-V_G + V_{bi})U_{bi} + (-V_G + V_{bi} + U_{bi})V + V^2\right]$ and the polynomial R, it is evident that for the present case, $a = (-V_G + V_{bi})U_{bi}$, $b = (-V_G + V_{bi} + U_{bi})$, $c = 1$, $R = \left[(-V_G + V_{bi})U_{bi} + (-V_G + V_{bi} + U_{bi})V + V^2\right]$ and $\Delta = 4(-V_G + V_{bi})U_{bi} - (-V_G + V_{bi} + U_{bi})^2$.

Using the above identity, the solution for Q_1 may be obtained to be:

$$Q_1 = \frac{q^2WN_D^2}{3\varepsilon}\left\{\frac{qWN_D\mu_0 a}{I_D} - \frac{\mu_0}{v_{sat}}\right\}\left\{h_D^3 - h_S^3\right\} - \frac{q^3W^2N_D^3\mu_0}{4\varepsilon I_D}\left\{h_D^4 - h_S^4\right\}$$
$$- \frac{2\varepsilon qN_DW^2\mu_0}{I_D}\sqrt{\frac{N_A}{N_A+N_D}}\left\{\frac{\sqrt{R_f}(2V_f+b) - \sqrt{R_i}(2V_i+b)}{4}\right. \qquad \text{(II-11)}$$
$$\left. + \frac{\Delta}{8}\ln\left[\frac{2\sqrt{R_f}+2V_f+b}{2\sqrt{R_i}+2V_i+b}\right]\right\}$$

In the above equations, V_f is the channel voltage at $x = L$ is given by V_D and V_i is the channel potential at $x = 0$ and is given by the equation *0*. R_f is the value of $R(V)$ at the drain side of the channel, while R_i is the value of R at the source side of the channel given by

$$\left[(-V_G + V_{bi})U_{bi} + (-V_G + V_{bi} + U_{bi})V_D + (V_D)^2\right], \text{ and} \qquad \text{(II-12)}$$

$$\left[(-V_G + V_{bi})U_{bi}\right], \qquad \text{(II-13)}$$

respectively.

Q_1 in the Saturation Region of Operation

Q_1 in the saturation region is divided into two parts. The first part is linear which is the region under the gate from $x = 0$ to $x = L_1$, and the second part is the saturated part between the regions $x = L_1$ and $x = L$. The equation in the integral form is given by:

$$Q_1 = qWN_D \int_0^{L_1} h(x)dx + qWN_D(L - L_1)h_{L_1}. \tag{II-14}$$

The solution to this equation is similar to that of the linear region given by, except that in this equation parameters such as V_f and R_f are different. The final voltage V_f is given by V_1, R_f is given by:

$$\left[(-V_G + V_{bi})U_{bi} + (-V_G + V_{bi} + U_{bi})V_1 + V_1^2\right]$$

and the final equation is given by

$$\begin{aligned} Q_1 = {} & \frac{q^2WN_D^2}{3\varepsilon}\left\{\frac{qWN_D\mu_0 a}{I_D} - \frac{\mu_0}{v_{sat}}\right\}\left\{h_{L_1}^3 - h_S^3\right\} - \frac{q^3W^2N_D^3\mu_0}{4\varepsilon I_D}\left\{h_{L_1}^4 - h_S^4\right\} \\ & - \frac{2\varepsilon qN_DW^2\mu_0}{I_D}\sqrt{\frac{N_A}{N_A + N_D}}\left\{\frac{\sqrt{R_f}(2V_f + b) - \sqrt{R_i}(2V_i + b)}{4}\right. \\ & \left. + \frac{\Delta}{8}\ln\left[\frac{2\sqrt{R_f} + 2V_f + b}{2\sqrt{R_i} + 2V_i + b}\right]\right\} + qWN_D(L - L_1)h_{L_1} \end{aligned} \tag{II-15}$$