2010

Free-carrier effects in polycrystalline silicon-on-insulator photonic devices

Oshoriamhe Ogah

Free-carrier Effects in Polycrystalline Silicon-on-Insulator Photonic Devices

By

Oshoriamhe F. Ogah

A Thesis Submitted in Partial Fulfillment

Of the Requirements for the Degree of

Master of Science in Microelectronic Engineering

Approved by:

Prof. ----------
Dr. Stefan F. Preble (Thesis Advisor)

Prof. ----------
Dr. Karl D. Hirschman (Committee member)

Prof. ----------
Dr. Sean L. Rommel (Committee member)

DEPARTMENT OF MICROELECTRONIC ENGINEERING

COLLEGE OF ENGINEERING

ROCHESTER INSTITUTE OF TECHNOLOGY

ROCHESTER, NEW YORK

FEBRUARY, 2010

Free-carrier Effects in Polycrystalline Silicon-on-Insulator Photonic Devices

By

Oshoriamhe Frederick Ogah

Date: ---------- Author: ----------

Acknowledgements

I would like to acknowledge the following people for their contribution to this work and to my education.

I would like to thank my thesis advisor, Dr. Stefan Preble for the direction and support he has provided along the way. I would also like to thank my committee members, Dr. Sean Rommel and Dr. Karl Hirschman; you have all assisted me with this thesis in various ways.

I would like to thank PhD student, Karthik Narayanan for his invaluable help with the optical test setup

The SMFL staff, particularly Sean O'Brien has given much of his time in certifying me on most of the tools in the cleanroom. Special thanks go to Scott Blondell, Bruce Tolleson, Dave Yackoff, John Nash and Richard Battaglia for their help with the micro-fabrication and wafer dicing tools.

The Microelectronic and Microsystems engineering department staff, Ms. Widlund and Ms. Stevens also helped in bringing the thesis requirements together.

Finally, I want to thank my family and friends for all their support and encouragement.

Free-carrier Effects in Polycrystalline Silicon-on-Insulator Photonic Devices

By

Oshoriamhe F. Ogah

Master of Science in Microelectronic Engineering

Abstract

Photonic systems integrated into microelectronic systems using the well established integrated chips fabrication technologies offer immense opportunity in overcoming the bandwidth and power limitations IC faces. The use of deposited polycrystalline silicon in the fabrication of photonic devices has the potential of offering monolithic integration, promising electrical and optical properties, under optimized micro-fabrication, and lower costs. In this thesis, the design, fabrication and optical testing of waveguide devices on polycrystalline silicon platform is presented. Single mode polysilicon waveguide devices were fabricated at the RIT SMFL. The polysilicon waveguides fabricated successfully coupled and guided light. The transmission was measured over several lengths and the cut back method was used to quantify the free carrier absorption and propagation losses of polysilicon at 1550 nm wavelength. Comparisons were made with data for crystalline silicon. The absorption coefficient for polysilicon was found to be 25.9% higher than that of crystalline silicon.

Table of Contents

List of Tables

List of Figures

Chapter 1

Background

1.1 Introduction

The aim of this thesis is to investigate the design, fabrication of polycrystalline silicon (polysilicon) waveguides and use test results to quantify free-carrier effects in polysilicon. Developments in micro-optic technology, integration trends of electronics and optics, the transitioning of micro-optics to silicon on insulator and deposited silicon technologies and the problems associated will be studied. Several waveguide structures are designed, fabricated and tested on the deposited polycrystalline silicon platform to prove their performance using equipment at the Rochester Institute of Technology (RIT) Semiconductor & Microsystems Fabrication Laboratory (SMFL).

1.2 Impact of micro-optics on electronics

Though microelectronics has been able to achieve unprecedented integration, its limitations such as the need for increased speed and to shrink nodes continue to exist. Optics in theory can complement many of the anticipated drawbacks of electronics as it possesses several key advantages. It involves the manipulation of photons, which are charge-less particles. Because of this optical signals have negligible interference and hence low cross talk. This means several optical beams can be guided in the same medium while retaining their individual properties. This allows for simultaneous optical processing. Light also travels at speeds greater than the electron since it is not inhibited by drift velocity or particle mobility. These factors serve to give optical systems superior bandwidth and speed [1] as compared to equivalent electrical systems.

The limitations for micro-optics are the large size of optical devices and the integration in electronic systems. Though there are still some device and integration problems yet to be solved, optics has a strong potential in solving problems faced by the rapidly evolving electronics industry.

Semiconductor micro-fabrication technology, used in the creation of integrated circuits (ICs) has set the foundation for micro-optical systems fabrication. Semiconductor micro-fabrication consists of patterning a substrate using lithography, thin-film deposition, etching and doping over several steps to produce devices such as transistors. The repeatability of micro-electronic fabrication allows for low cost, high yield, high quality devices that power the electronics industry [2].

Moore's law [3] holds that computing power will exponentially increase over time, doubling every twenty four months. So far this theory has held true, but in the next few years size limitations and RF effects will force a fundamental shift in electronics. Micro-optics is a promising option for the next technology generation. Innovative ideas like optical interconnects and possibly an optical computer in the near future are some of the advancements that will benefit microelectronics.

1.3 Silicon as a micro-photonics platform

Photonics has benefited immensely from advances in process technology and the better understanding of silicon materials. The micro-fabrication infrastructure and process knowledge is already in place; therefore the implementation of photonic devices requires small modifications of existing process technology to yield significant advantages. The ability to accurately etch anisotropically in the nanometer scale provides the foundation

for the fabrication of waveguide structures. The ability to define features and make alignments through photolithography makes integration of photonic devices with other devices possible [2].

The silicon-on-insulator (SOI) substrate is widely used in electronics. It also possesses several advantages in micro-optical systems because it has large index contrast between the silicon and silicon dioxide layers – allowing for strong optical confinement. The refractive index of silicon is 3.45 while that of silicon dioxide is 1.46 [4]. The light is confined in the silicon top layer with the silicon dioxide acting as the lower cladding and the air above as the upper cladding.

Proper cladding allows for Total Internal Reflection which occurs when incident light is completely reflected. The critical angle, the angle for this to occur is the angle to the normal of the surface and is a function of the ration between the materials – as derived from Snell's law. Because photons flow along the path of least resistance, the propagation remains in the region of highest index [5]. Silicon is also optically transparent at wavelengths used for long haul communication (between 1.3 and 1.7 μm). This allows SOI waveguides and others to be easily integrated into existing silica based fiber optic networks [5].

The major advantage of the SOI platform is its ability to integrate seamlessly into existing CMOS process technology. Monolithic integration of electronics and optics on a single substrate will bring together the bandwidth and speed of the optical systems with the well-established fabrication methodologies of Integrated Circuits – creating a superior hybrid [6].

1.4 Problems with SOI platform

Problems facing SOI are the poor optical properties of silicon. A major disadvantage is that compared to the III-V semiconductors, silicon does not exhibit the first order electro-optic effect. The electro optic effect is the change in the optical properties of a material (refractive index, etc) in response to an electric field passing through the material [7]. This effect is the basis for high speed modulators and is the main link connecting electronics and optics. Because silicon does not possess the electro-optic, and higher order effects like the higher order, Kerr effect are too small, direct modulation by an electric field in silicon is difficult. Most times it requires the electric field to exceed the break down voltage of silicon.

Methods of modulating the refractive index in SOI photonic devices are non-linear carrier injection (free-carrier dispersion effect) and the thermal optic effect. The insertion of carriers into silicon causes band shrinkage and band filling, which changes the refractive index of the material [8]. The Thermal Optic Effect modulates the material's index using the temperature. Both of these effects are proven and useful, whoever they provide for decreased bandwidth and modulation speeds in silicon based devices – as compared to the electro-optic effect in capable materials. For example, the carrier injection method for modulation in silicon has a switching limit of 2.5 Giga-bits-per-second (Gbps) [9]. Many other modern modulators, like lithium niobate have switching speeds of over 100 Gbps. Therefore much improvement is still needed for silicon as a modulation medium [10].

Silicon also has undesirable optical properties that have to do with its band structure. The band structure of material describes the series of "allowed" and

"forbidden" electron energy states – and these determine electrical and optical properties like conductivity and transmission [11]. The energy bandgap is the energy difference between the top of the valence band and the bottom of the conduction band [12]. Absorption occurs where the photon energy is close to that needed to excite an electron over the bandgap – hence the larger the bandgap the shorter the absorption wavelength (and vice versa). Silicon has a bandgap of 1.14 eV, which corresponds to absorption in the range of 200 nm to 1.1 μm, with transmission peaks at 1.3 μm and 1.55 μm [13]. In order to detect light a photon must possess sufficient energy to create free carriers by inducing electrons to cross the bandgap [13]. Because silicon's bandgap is too large, detectors can not be made in the 1.3 to 1.55 μm range, which incidentally is where the transmission peaks lie. Photo-detectors are critical in converting optical information into an electrical form, so overcoming this issue is vital.

Methods to address this issue are the doping of silicon with erbium (*Er*), a rare earth element in other to change the absorption spectrum. There is however a limit to the maximum allowable *Er* concentration in silicon [14]. Other approaches such as manipulating the bandgap of silicon by inducing biaxial tensile stress in the lattice have also been attempted. It has been found that inducing stress in improves electron and hole mobility because the potential for ballistic transport is increased due to fewer carrier collisions. Strain can be induced by making use of epitaxial growth of silicon.

Silicon is an indirect semiconductor and is unable to efficiently produce light due to issues originating from its band structure. Indirect semiconductors have indirect band-gaps where electrons in the minima of the conduction band have a different momentum from holes in the maximum of the valence band [15]. This result in electrons having to

first lose momentum in the form of phonons before recombining with a hole – a result of the k-space offset between electrons and holes in this type of material. III-V semiconductors are direct semiconductors and have produce light very efficiently, however they are costlier and harder to integrate into the standard CMOS process flow. As such methods to improve the silicon light emitting properties will be very useful in optical-electronics integration. Several methods have been tried so far such as Stimulated Raman scattering – with limited success.

Losses in SOI devices have an impact on the performance of photonic components. Since it relies on Total Internal Reflection to optically confine light in a waveguide, non-idealities in the structure easily contribute to losses. Examples are absorption, scattering due to refractive index inhomogeneity, interface induced scattering and coupling of guided modes into substrate modes [16]. The coupling of light in and out of devices also account for additional losses.

SOI material also takes up a large amount of real estate from transistors as they share the same silicon layer. The buried oxide thickness in standard SOI is not appropriate for waveguide cladding as it is smaller than the optical wavelength. Hence because of the numerous issues with SOI, there is a need to explore deposited polycrystalline silicon (polysilicon) material. A deposited layer would enable the monolithic integration of optical devices in separate layers of an IC chip and provide optical design flexibility.

1.5 Deposited polysilicon as a solution

The need for device compatibility and real estate for both electronic and photonic devices indicate that separate layers should be used to fabricate each set of devices. It is possible to integrate optics and electronics into an SOI substrate using wafer thinning, metallization and bonding technologies; however it is not cost effective. Depositing silicon layers over the electronic layer and subsequently processing them into optical devices are more practical.

Other deposited films like amorphous silicon and silicon nitride rely on the thermo-optic effect [17], and limit the speeds in the MHz range. Deposited polysilicon utilizing carrier injection (free carrier dispersion effect) is a promising path as good optical and electrical properties are achievable – sub-nanosecond carrier injection and optical modulation [9]. Polysilicon based photonics hence provides a solution for multi-level integration of optical networks in silicon integrated circuits.

One major limitation of polysilicon based photonic devices is that a relatively large propagation loss in polysilicon waveguides due to scattering at the grain boundaries and light absorption [18].

In polysilicon, the fabrication process is a strong factor in determining the amount of propagation loss. Historically, polysilicon waveguides fabricated on directly deposited layers exhibit very large optical losses - greater than 70 dB/cm - which made the material unattractive [19, 20]. The high losses were due to the small grain sizes and the rough surface of the polysilicon layer. After using Chemical Mechanical Polishing (CMP) to smooth the layer, losses were reduced to approximately 34 dB/cm [20].

Using solid-phase crystallization (SPC) of deposited amorphous silicon (a-Si) allowed for smoother surface and larger grain sizes [21, 22]. This further reduced loss to 11 dB/cm. Other techniques like using remote electron cyclotron resonance (R-ECR) plasma hydrogenation and using silicon oxide nitride (SiON) as cladding, instead of regular silicon dioxide allowed for the propagation loss to be reduced even further down to approximately 6 dB/cm [22].

SPC is a very promising technique that has low cost and produces films with high uniformity. It involves depositing amorphous silicon and crystallizing the film into large, grained polysilicon using anneal treatments [23]. One anneal treatment induces nucleation or the crystallization of the film material while the other anneal induces grain growth. Lower temperature recipes can be used to create even larger grain sizes but there is the drawback of having much lower throughput. Using higher temperatures will also be problematic as such high thermal budgets means the polysilicon layer has to be deposited before any doping is done. It is therefore important to reduce the thermal budget for the polysilicon waveguide fabrication without reducing the improved optical loss property.

Polysilicon material differs from the single-crystalline silicon material in three main ways that affect electro-optic systems – optical loss, effective carrier mobility and effective free carrier lifetime [9]. All three parameters are affected by the grain boundaries that populate the polysilicon material, presenting barriers to the flow of carriers and reducing effective carrier mobility [18, 24]. Since the polysilicon material is very resistive, doping is required to induce charge injection. However while the electrical injection is improved when the doping level is increased above the grain boundary trap density, the trade-off is reduced optical propagation due to increased free carrier

absorption. In addition, some of the carriers may fail to contribute to free carrier dispersion – if they fill into grain boundary trap states [18]. This has doubly negative consequence - reducing both the optical and electrical properties as free-carrier dispersion is and charge injection are reduced.

As polysilicon material needs to be doped for improved electrical properties, the optical problems, like free carrier absorption amongst others, that arise due to doping need to be researched more.

1.6 Summary

Despite the various problems, micro-optics integration into electronics faces, there is still considerable promise as fabrication technologies improve. Silicon will make integration of photonic devices into micro-electronics cost-effective once the electrical and optical obstacles are conquered. Polycrystalline silicon as a deposited material holds much promise as it allows for high-speed carrier injection and optical modulation using the free carrier dispersion effect. Though there is a trade-off between optical and electrical properties when using silicon, polysilicon produces a balance that shows much promise and can be improved on. Other than the optical and electrical benefits, the device space, and fabrication simplification are other benefits of utilizing deposited polysilicon material.

1.7 Thesis research

The goal of this thesis work will be to design, fabricate and test several polysilicon waveguide devices. The free-carrier absorption and the optical loss in

polysilicon will be quantified. This will be achieved by doping the polysilicon material and using the cut back method, to measure the transmission at different waveguide lengths for the various carrier concentrations. The viability of efficiently fabricating these devices at the RIT SMFL is examined.

1.8 References

[1] Allen Kent, and James G. Williams, "Encyclopedia of Computer Science and Technology" Volume 27 Supplement 12, New York, Marcel Dekker Inc, pp.181-200, 1999.

[2] Wim Bogaerts, Roel Baets, Pieter Dumon, Vincent Wiaux, Stephan Beckx, Dirk Taillaert, Bert Luyssaert, Joris Van Campenhout, Peter Bienstman, and Dries Van Thourhout," Nanophotonic Waveguides in Silicon-on-Insulator Fabricated With CMOS Technology," J. Of Lightwave Tech., Vol. 23, No. 1, pp. 401-412, Jan 2005.

[3] William J. Dally, and John W. Poulton, "Digital Systems Engineering", United Kingdom, Cambridge University Press, 2000, pp. 12-16.

[4] B. Jalali, S. Yegnanarayanan, T. Yoon, T. Yoshimoto, I. Rendina, and F. Coppinger, "Advances in Silicon-on-Insulator Optoelectronics," IEEE J. Quantum Electron., Vol 4, No. 6, pp. 938-946, 1998.

[5] Timo Aalto, "Microphotonic Silicon Waveguide Components." Doctoral Thesis, Technical Research center of Finland (VTT) in Espoo, Finland, 2004.

[6] C.K. Tang, A.K. Kewell, G.T. Reed, A.G. Rickman, and F. Namavar,

"Development of a library of low-loss silicon-on-insulator optoelectronic devices," Proceedings from IEE Optoelectronics, Vol.143, No.5, pp. 312-315, 1996.

[7] Christopher C. Davis, “Lasers and Electro-optics: Fundamentals and Engineering”, United Kingdom, Cambridge University Press, pp. 472-475, 2000.

[8] S. Abdalla, S. Ng, D. Celo, S. El-Mougy, T. Smy, and B. Syrett, “Optical switching in InGaAsP waveguides using localized index gradients,” Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, Vol. 22, No. 3, pp. 796-799, 2004.

[9] K. Preston, S. Manipatruni, A. Gondarenko, C. B. Poitras, M. Lipson, “Deposited silicon high-speed integrated electro-optic modulator” Optics Express 5118, Vol. 17, No. 7, 2009.

[10] Jon Newey, “Optical modulators get ready for a high-speed network future,” Compound Semiconductor Magazine, March 2002. Available: http://compound Semiconductor.net/ zarticles/magazine/8/3/3/1

[11] Jasprit Singh, “Electronic and Optoelectronic Properties of Semiconductor Structures”, United Kingdom, Cambridge University Press, 2003

[12] William T. Silfvast, Laser Fundamentals, United Kingdom, Cambridge University Press, pp. 174-180, 2004.

[13] Peter Capper, C T Elliott , Infrared Detectors and Emitters: Materials and Devices, Norwell, MA, Springer, 2001.

[14] J. I. Dadap, R. L. Espinola, R. M. Osgood, Jr., S. J. McNab, and Y. A. Vlasov,

"Spontaneous Raman scattering in ultrasmall silicon waveguides," Optical Society of America, Vol. 29, pp. 2755-2757, 2004.

[15] Mitsuo Fukuda, “Optical Semiconductor Devices,” New York, Wiley-IEEE, pp. 37-43, 1999.

[16] A.G. Rickman, G.T. Reed, and F. Namavar, “Silicon-on-insulator optical rib waveguide loss and mode characteristics,” Journal of Lightwave Technology, Vol. 12, No. 10, pp. 1771-1776, 1994.

[17] R. Amatya, C.W. Holzwarth, H. I. Smith, and R.J. ram, “Precision Tunable Silicon Compabitible Microring Filters,” IEEE Photon. Technology Lett. 20, 1739-1741, 2004.

[18] T. Kamins, “Polycrystalline Silicon for Integrated Circuits and Displays”, 2nd ed., Kluwer, 1998.

[19] A. Säynatjoki, J. Riikonen, H. Lipsanen, and J. Ahopelto, “Optical waveguides on polysilicon-on-insulator,” J. Mater. Sci. Mater. Electron. 14(5/7), 417–420, 2003.

[20] J. S. Foresi, M. R. Black, A. M. Agarwal, and L. C. Kimerling, “Losses in polycrystalline silicon waveguides,” Appl. Phys. Lett. 68(15), 2052–2054, 1996.

[21] L. Liao, D. R. Lim, A. M. Agarwal, X. Duan, K. K. Lee, and L. C. Kimerling, “Optical transmission losses in polycrystalline silicon strip waveguides: effects of waveguide dimensions, thermal treatment, hydrogen passivation, and wavelength,” J. Electron. Mater. 29(12), 1380–1386, 2000.

[22] Q. Fang, J. F. Song, S. H. Tao, M. B. Yu, G. Q. Lo, and D. L. Kwong, “Low loss (approximately 6.45dB/cm) submicron polycrystalline silicon waveguide

integrated with efficient SiON waveguide coupler," Opt. Express 16(9), 6425–6432, 2008.

[23] V. Subramanian, P. Dankoski, L. Degertekin, B.T. Khuri-Yakub, K.C. Saraswat, "Controlled Two-Step Solid-Phase Crystallization for High-Performance Polysilicon TFTs", IEEE Electron Device Letters, Vol. 18, No. 8, August 1997.

[24] C. R. M. Grovenor, "Grain boundaries in semiconductors," J. Phys. C 18, 4079-4119,1985.

Chapter 2

Waveguide Primer

2.1 Electromagnetic wave

Micro-optics utilizes electromagnetic radiation in the Near Infrared (NI) frequency range [1]. Electromagnetic waves have the fundamental properties as prescribed in Maxwell's four differential equations. They relate to the electric field (*E*), the magnetic field (*H*), current density (*J*) and charge density (ρ) [2].

$$\vec{\nabla} \times \varepsilon \vec{E} = \rho \tag{2.1}$$

$$\vec{\nabla} \times \vec{E} = -\frac{d}{dt} \mu \vec{H} \tag{2.2}$$

$$\vec{\nabla} \times \vec{H} = -\frac{d}{dt} \varepsilon \vec{H} + \vec{J} \tag{2.3}$$

$$\vec{\nabla} \times \mu \vec{E} = 0 \tag{2.4}$$

Electromagnetic waves travel at the speed of light in vacuum, and micro-optics is concerned with this propagation within the various photonic structures.

Polarization is a very important property of electromagnetic waves. Transverse Electric (TE) and Transverse Magnetic (TM) fields are the most common, though most practically are a superposition of several polarizations. The TE has the electric field perpendicular to the plane of incidence while the TM has the magnetic field perpendicular. The electromagnetic power flow in a given polarization is represented as a vector product of the magnetic and electric components.

2.2 Optical waveguide

An optical waveguide is a structure that has the ability to confine and guide electromagnetic waves [3]. Examples of waveguides are fiber optics used in telecommunications and micro-fabricated ridges used in semiconductor applications. Waveguides rely on a guiding medium, the core of the waveguide, surrounded by a cladding – usually material of lower refractive index. Propagation in waveguides is described by the optics models (Snell's law) as shown in Equation 5.

$$n_1 \sin(\theta_1) = n_2 \sin(\theta_2) \tag{2.5}$$

where n are the refractive indices of each medium and θ_1 and θ_2 are the incident angles and refracted angles respectively. An illustration of this representation is shown in Figure 2.1.

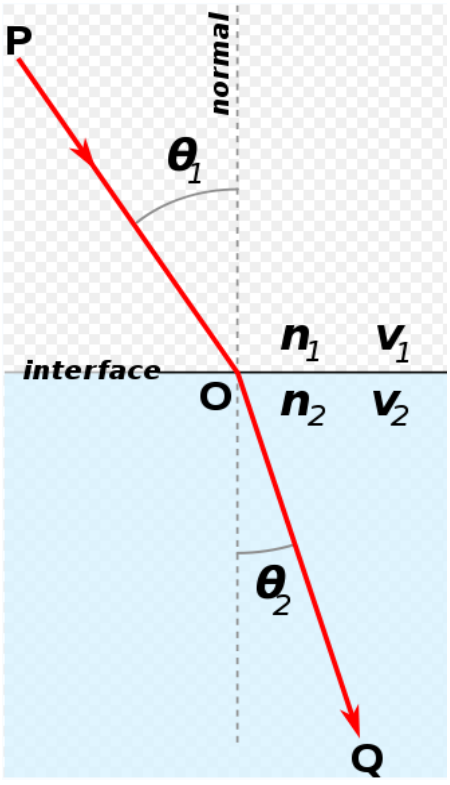

Fig. 2.1: Refraction of light passing through two mediums [4]

If the refractive indices and the incident angle are chosen correctly, it is possible to have the refracted light have an angle of 90 degrees – in other words reflected back into the starting medium. This condition is termed Total Internal Reflection and it occurs at a critical angle of the incident light. The incident angle is calculated as [5]:

$$\theta_c = \arcsin(n_2 / n_1) \tag{2.6}$$

A waveguide works using Total Internal Reflection and at an angle greater than the critical angle to ensure that the light is continually guided in the waveguide's core region. Waveguides therefore have two materials of lower index sandwiching a layer of high index in other to optimize the critical angle and sustain guiding.

The reflection coefficient is a multiplier that relates the amplitude of the incident electric field on a dielectric interface to the amplitude of the reflected field and is described by the Fresnel's equations. These are given for both TE and TM polarizations by in equations 2.6 and 2.7 [5]

$$r_{TE} = \frac{n_1 \cos(\theta_1) - \sqrt{n_2{}^2 - n_1{}^2 \sin^2(\theta_1)}}{n_1 \cos(\theta_1) + \sqrt{n_2{}^2 - n_1{}^2 \sin^2(\theta_1)}}. \tag{2.7}$$

$$r_{TM} = \frac{n_2{}^2 \cos(\theta_1) - n_1 \sqrt{n_2{}^2 - n_1{}^2 \sin^2(\theta_1)}}{n_2{}^2 \cos(\theta_1) + n_1 \sqrt{n_2{}^2 - n_1{}^2 \sin^2(\theta_1)}} \tag{2.8}$$

It can be seen that if the incident angle is smaller than the critical angle, the resulting reflection coefficient is less than 1. However if the angle is larger than the critical angle the absolute value of the reflection coefficient is 1 – entire wave is reflected.

A limitation to the guiding of electromagnetic waves is that not all angles greater than the critical angle allow for propagation, rather propagation is allowed in discrete

angles [5]. These discrete angles are called the mode of propagation and it is a standing wave perpendicular to the propagation direction and a traveling wave parallel to the direction of propagation [6]. The mode concept comes from the fact that the wave vector possesses both parallel and perpendicular components in the waveguide and each time a ray is reflected there is a phase shift of the perpendicular component. Guiding of the wave through a waveguide is possible only when this phase shift is an integer multiple of 2π. Equations for the TM and TE modes as well as an analysis of the slab waveguide are found in [5].

Only a finite number of modes can be propagated in a given waveguide. The number of modes is calculated from the dimensions of the waveguide and the wavelength. The polarization of light also plays a determining role. The fundamental mode carries the most energy and is the case where the integer multiple of standing waves is equal to one [7]. Waveguides are usually excited by Gaussian distribution field and these distributions are represented by a continuum of radiated and guided modes, all orthogonal to each other [7]. The guided modes will guide through perpetually without loss, in theory, while the radiated modes will be lost after some finite propagation length.

Maxwell's equations are used to derive the wave equation that precisely explains phenomena – such as optical coupling. The wave equation is given in equation 2.9 represents the magnetic or electric field while represents the Laplacian operator [5].

$$\nabla^2\psi = \mu_m\varepsilon_m\frac{\partial^2\psi}{\partial t^2} = \frac{1}{\upsilon^2}\frac{\partial^2\psi}{\partial t^2} \tag{2.9}$$

$$\nabla^2 = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2} \tag{2.10}$$

The solution to the wave equation becomes progressively more complex for non-rectangular and multidimensional structures. In order to solve the equation, simulation software packages – like *Optiwave,* are used to find approximate analytic or numeric solutions. [5, 7] provide further information.

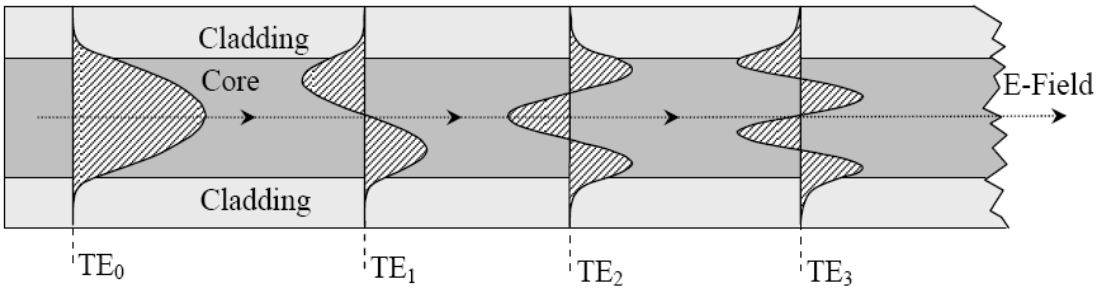

Fig. 2.2: Modal distributions in slab waveguides [8]

Figure 2.2 shows the field distribution for the first four modes of a slab waveguide found by solving the wave equation.

2.3 Single mode waveguide condition

The devices that will be tested in this thesis are single-mode waveguides, so the discussion will be restricted to this condition. The main differences between single and multimode waveguides are that single mode have a smaller core, are used for high speed data transmission for longer distances and are less susceptible to attenuation than multimode. Multimode waveguides on the other hand have much larger cores and are best for shorter distances due to their higher attenuation levels [9].

Using the single mode condition of waveguide structures has several advantages. The single mode condition reduces insertion losses and minimizes the effects of sidewall

interference scattering [9]. For these reasons and because of its simplicity, this will be the only tested waveguide device in this thesis.

Only a small range of waveguide dimensions will allow for the single mode condition. A ridge waveguide has the ability to support propagation under the single mode condition over a wider range of dimensions – removing some of the fabrication limitations of producing single mode devices.

The single mode condition is possible in large dimensioned waveguide devices as higher order modes radiate out of the ridge. A mode matching technique to describe the approximate single mode condition is given in equation 2.11 [10].

$$\frac{a}{b} \leq \left(\frac{q+4\pi b}{4\pi b}\right) \frac{1+0.3\sqrt{\left(\frac{q+4\pi b}{q+4\pi r\cdot b}\right)^2-1}}{\sqrt{\left(\frac{q+4\pi b}{q+4\pi r\cdot b}\right)^2-1}} \tag{2.11}$$

Where a and b represent waveguide height and width factors, λ the free space wavelength, r the ratio of the thin silicon layer to the total waveguide height, $2b\lambda$. The variable q, is defined by:

$$q = \frac{\gamma_0}{\sqrt{n_1^2 - n_0^2}} + \frac{\gamma_2}{\sqrt{n_1^2 - n_2^2}} \tag{2.12}$$

Further details on the dimensions calculation is provided in [10].

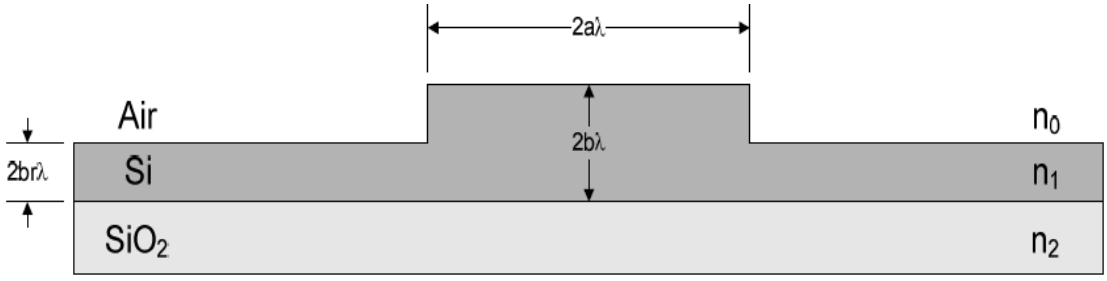

Fig. 2.3: Waveguide structure (without cladding) [10]

Figure 2.3 shows the waveguide ridge structure with width and height factors needed to calculate fabrication dimensions that will ensure the single mode condition.

2.4 Summary

A basic theoretical foundation of the workings of the waveguide structures fabricated and tested in this thesis work. A shallow treatment of the electromagnetic wave, the optical waveguide, coupling and the single mode condition were presented. The single mode waveguide alone was used to collect results so only the single mode condition was treated.

2.5 References

[1] Bhag Singh Guru, and Hüseyin R. Hiziroglu, "Electromagnetic Field Theory Fundamentals," United Kingdom, Cambridge University Press, 2004.

[2] Desmond Rodney Lim Chin Siong, "Device Integration For Silicon Micropotonic Platforms." Doctoral Thesis, Massachusetts Institute of Technology, June 2000.

[3] ATIS, "Optical waveguide," Available: http://www.atis.org/tg2k/_optical_ waveguide.html

[4] Wolf, K. B. "Geometry and dynamics in refracting systems", European Journal of Physics 16: 14-20, 1995.

[5] Graham T. Reed, and Andrew P. Knights, "Silicon Photonics: An Introduction", West Sussex, England, John Wiley and Sons, 2004.

[6] Desmond Rodney Lim Chin Siong, "Device Integration For Silicon Micropotonic Platforms." Doctoral Thesis, Massachusetts Institute of Technology, 2000.

[7] Tamir Theodor, “Guided-Wave Optoelectronics,” Germany, Springer-Verlag, 1990.

[8] OptiFDTD Technical Background and Tutorials on Finite Difference Time Domain Photonics Simulation Software, Optiwave, 2005.

[9] Jinsong Xia, Jinzhong Yu, Yanping Li, and Shaowu Chen, “Single-mode condition for silicon rib waveguides with large cross sections,” Optical Engineering, Vol. 43, No. 9, pp. 1953-1954, 2004.

[10] R.A. Soref, J. Schmidtchen, and K. Petermann, “Large single-mode rib waveguides in GeSi-Si and Si-on-SiO2,” IEEE Journal of Quantum Electronics, Vol. l27, No. 8, pp. 1971-1974, Aug 1991.

Chapter 3

Polycrystalline Silicon Background

3.1 Growth and structure of polycrystalline films

The mechanisms involved in the formation of crystalline states from vapor or liquid phases by condensation depends on the time the clusters of atoms interact to form the bonds in stable structures [1]. Crystallization is the long-range ordering of atoms in a periodic solid phase lattice at close to equilibrium conditions.

Polycrystalline materials possess no unique directionality, in other words have random grain sizes, shapes and orientational packing. The polycrystalline state has a relatively longer short-range order, as compared to amorphous silicon, and the thermodynamic stability is not only dictated by the crystalline bonding configurations with the lowest free energy but also by the grain boundary energy and surface diffusion. The grains in the material are formed by independent nucleation and growth processes randomly oriented and spaced with respect to one another [2].

The grain size is controlled by the number of nucleating sites, which can be manipulated by seeding with additives or rapid quenching. Grain growth ceases when adjacent grains restrict further growth. The shape of the grain is determined by the surface orientations favorable for adatom attachment from the solid, liquid and vapor phases. This surface is determined by the orientation with the lower interfacial energies such as the {110} or [111} orientation for diamond cubic or zinc blende [1] and the {100} orientation for NaCl structures.

In general deposition of these materials will show a high degree of preferential orientation normal to the plane of the substrate.

The growth of polycrystalline films is independent of the substrate, whether amorphous or crystalline. Amorphous material can also be transformed to the polycrystalline state but not vice versa. This irreversibility is because the crystalline state has lower lattice energy. The transition from amorphous to polycrystalline state occurs due to reduction of internal surface energy [3].

Several methods are used to deposit polysilicon: Low Pressure Chemical Vapor Deposition (LPCVD), Plasma-Enhanced CVD (PECVD), or Solid-Phase Crystallization (SPC) of amorphous silicon.

LPCVD involves the pyrolyzing of silane (SiH_4) between 580 and 650 C at very low pressures (0.2 to 1 Torr) [4]. The pyrolysis process releases hydrogen. Critical process variables for polysilicon deposition include temperature, pressure, silane concentration and possibly dopant concentration. Polycrystalline silicon is deposited from silane using equation 3.1 [5].

$$SiH_4 = Si + 2\ H_2 \tag{3.1}$$

The rate of polysilicon deposition follows Arrhenius behavior and increases rapidly with temperature. The activation energy, E_a, for polysilicon deposition is approximately 1.7 eV. Equation 3.2 shows the deposition rate.

$$R = A \exp(-q\ E_a / kT) \tag{3.2}$$

It can be seen that the rate of polysilicon deposition increases with deposition temperature. There will be a temperature however where the rate of deposition becomes faster than the rate at which un-reacted silane arrives at the surface of the wafers. Beyond this temperature, the deposition rate no longer increases with temperature as there is a lack of silane for reaction. When a polysilicon deposition process reaches this state it is

termed ‘mass-transport-limited’ [4] and at this point the reaction rate becomes dependent primarily on reactant concentration, gas flow and reactor geometry.

When the rate of polysilicon deposition is slower than the rate at which un-reacted silane arrives then it is termed ‘surface-reaction-limited’ [4]. This process is primarily dependent on reaction temperature and reactant concentration. Surface-reaction-limited processes result in excellent thickness uniformity and step coverage.

One major difference between amorphous and polysilicon is that the mobility of the charge carriers in polysilicon can be orders of magnitude larger [6]. Also polysilicon shows better stability under light-induced stress and electric field. Amorphous silicon however possesses lower leakage characteristics. Below 575 C, polysilicon deposition rate is too slow while above 650 C, the uniformity suffers greatly and excessive roughness will be encountered because of silane depletion and gas-phase reactions.

PECVD is used to deposit thin films via chemical reactions and with the aid of a plasma. The plasma is generated by RF frequency or DC discharge between two electrodes [6]. In general PECVD allows for lower temperature deposition than LPCVD.

SPC involves the deposition of amorphous silicon which is then crystallized to form the polysilicon [7]. Layers produced in this manner are shown to produces a more conformal layer. This is important when producing waveguide devices on this material as sidewall roughness and layer uniformity are key factors in the optical losses. SPC serves to minimize this factor. There is however the tradeoff that it takes much longer than direct polycrystalline silicon deposition. The two step SPC includes: grain growth and nucleation. Grain growth expands the grain size in the forming crystalline film; this has the positive effect of limiting optical losses that realize at grain boundaries. The fewer

grain boundaries in the deposited film the lower the optical losses. Nucleation is the event that transforms a homogenous structure, in this case amorphous silicon into crystallized material. The nucleation activation energy is extracted from the time to the beginning of crystallization, and this factor dictates the temperature and time of anneal used.

3.2 Grain boundaries in polycrystalline films

The grain boundary region can be represented as a two-dimensional semiconductor with a reduced band gap.

There are two types of grain boundaries – intrinsic and extrinsic grain boundaries. Intrinsic grain boundaries are those with properties controlled by intrinsic effects like lattice distortions. Extrinsic grain boundaries are grain boundaries where second-phase precipitation occurs or where the doping concentration in adjacent crystalline depletion region is appreciably different from that of the bulk crystal dopant concentration. Many of the grain boundary effects observed are extrinsic [2]. Molecular beam epitaxy (MBE) is a very good way of measuring the grain boundary structures. The secco etch is another.

3.3 Summary

A short primer on polycrystalline silicon, the material that will be used in this thesis work was given in this chapter. The general theory of the material structure and the deposition methods available is presented. The next chapter presents the fabrication of the waveguide devices on polycrystalline silicon film.

3.4 References

[1] T. Kamins, "Polycrystalline Silicon for Integrated Circuits and Displays", 2nd ed. Kluwer, 1998.

[2] L.L Kazmerski, "Polycrystalline and amorphous thin films and devices", Academic press, 1980.

[3] F.C. Eversteyn, P.J.W. Severin, C.H.J. van den Brekel, and H.L. Peek, "A stagnant layer model for the epitaxial growth of silicon from silane in a horizontal reactor," J. Electrochem. Soc. 117, 925-931, 1970.

[4] S. M. Sze, "Semiconductor Devices: Physics and Technology", Wiley India, 2008.

[5] J. Plummer, M. Deal, "Silicon VLSI Technology: Fundamentals, Practice and Modeling" Prentice Hall, 2000,

[6] Wolf, Tauber, "Silicon Processing for the VLSI Era," Vol. 1, 2nd Ed, 1999.

[7] V. Subramanian, P. Dankoski, L. Degertekin, B.T. Khuri-Yakub, K.C. Saraswat, "Controlled Two-Step Solid-Phase Crystallization for High-Performance Polysilicon TFTs", IEEE Electron Device Letters, Vol. 18, No. 8, August 1997.

Chapter 4

Fabrication of Waveguide Devices

The fabrication of devices designed in this thesis is accomplished at the Rochester Institute of Technology (RIT) Semiconductor and Microsystems Fabrication Laboratory (SMFL). This chapter will describe the several process steps used for the production of the photonic devices. Problems encountered during the fabrication process and their impact on waveguide operation and possible ways in which some of the problems can be solved in future works are presented. It should be noted that the waveguide structures used in this thesis work were produced from a photolithography mask that was not fully optimized for polycrystalline silicon, single-mode waveguides. The used mask had a number of superfluous photonic structures and only a few single-mode waveguide structures, however it was determined that the number of usable structures was sufficient enough to not warrant the additional cost of producing a new mask altogether.

4.1 Design layout and mask

Before fabrication, the photolithography mask needs to be identified or designed and produced. The mask used in this thesis is the one used by Eric Harvey [1] in his thesis on mono-crystalline Silicon-on-Insulator waveguide devices. For the design of masks, design constraints need to be determined by simulation and overcome by the layout of the structures. The structures were exported from *Optiwave* to the Graphical data systems (GDSII) layout format [2]. The GDS file was then imported into the *IC* VLSI layout software tool where each structure was positioned in the die framework. The

size of the layout is 18.5x18.5mm and it was produced by the MEBES III mask making tool at RIT. A diagram of the full mask layout is shown in Figure 4.1.

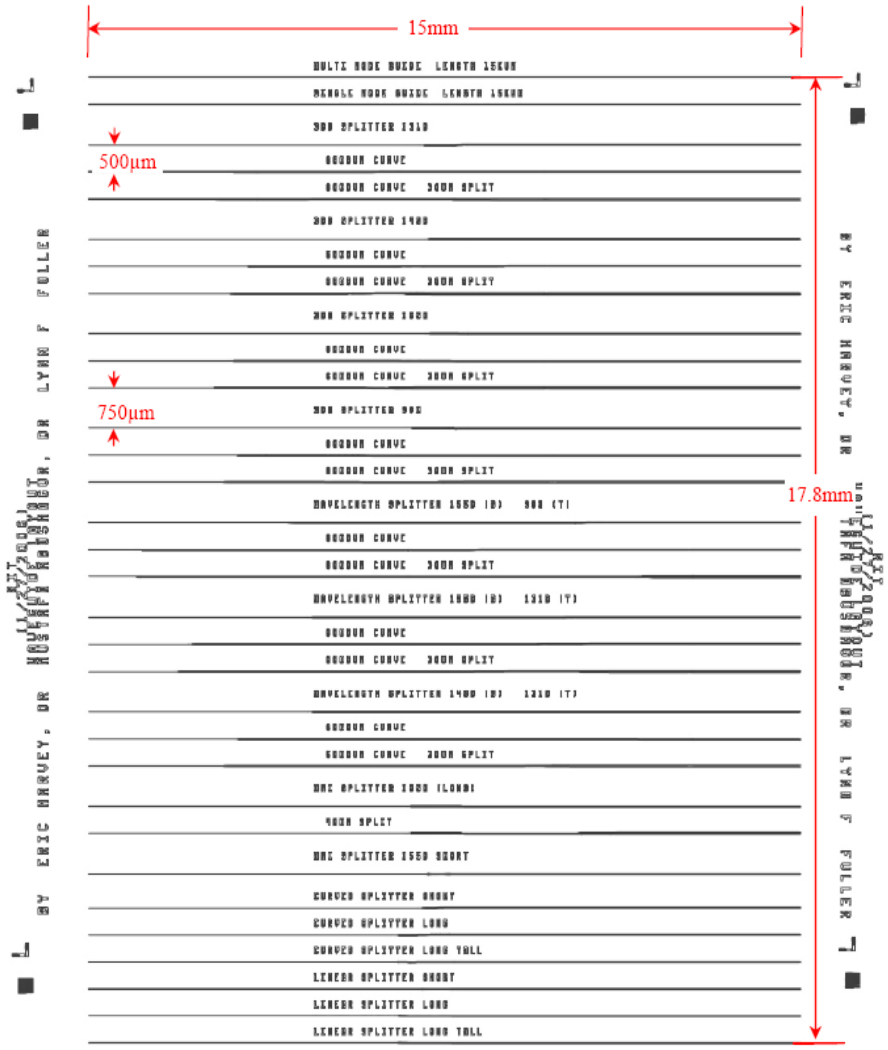

Fig. 4.1: Mask layout of die [1]

Each of the layout structures is 15 mm in length with input and output ports very well aligned to allow for convenient testing on the same die. The devices were separated by 500 µm so that an excited waveguide's evanescent field would cause negligible interaction on neighboring structures. The layout was directly printed by the MEBES III

from the GDSII file and was designed as a clear field mask – the chrome remains only where the structures and text are located and are cleared everywhere else. This in essence means a positive photoresist has to be used as this type of resist becomes soluble when exposed to light from the stepper. The fabricated mask is shown in Figure 4.2.

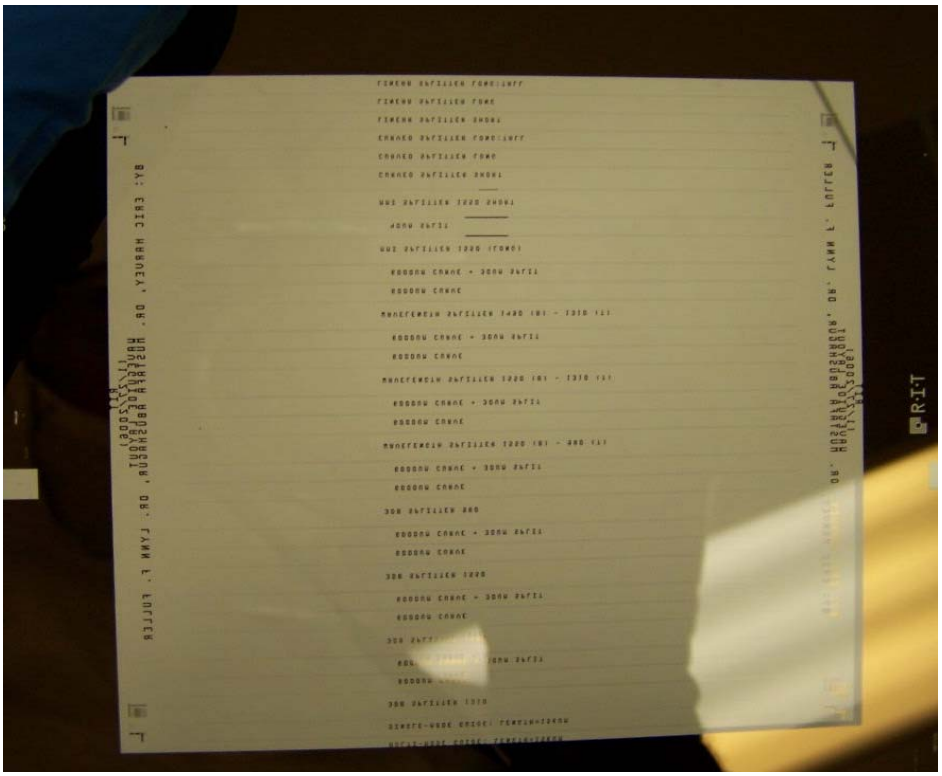

Fig. 4.2: Mask fabricated with the MEBES III

4.2 Wafer processing

Several process steps were utilized to transfer the waveguide structures onto the polycrystalline silicon film. Steps were taken to address issues that might be detrimental to optimized waveguide functionality like non-uniform films, rough waveguide side-walls, implant anneal amongst others. The following sub-chapters will describe the steps used to fabricate the final waveguide devices.

4.2.1 Preparation

The starting substrates are basic 6 inch diameter, <100> oriented, silicon wafers with no deposited films initially. The wafers are scribed for identification purposes and go through the RCA cleaning process. RCA stands for Radio Corporation of America which developed the original procedure in 1965. The RCA clean is a set of cleaning steps standard in the semiconductor industry performed before high temperature process steps such as diffusion, oxidation, chemical vapor deposition (CVD). It includes Standard Clean, SC-1, which removes organic contaminants, and SC-2, which removes metallic (ionic) contaminants [3].

The RCA steps vary slightly from cleanroom to cleanroom but have almost the same components. The steps used at the RIT SMFL and used for this thesis work go as follows:

SC 1: 10 minutes, 1:1:5 solution, $NH_4OH + H_2O_2 + H_2O$ at 75 degrees Celsius.

Rinse in De-ionized (DI) water: 5 minutes.

50:1 Hydrofluoric Acid (HF) dip: 1 minute.

Rinse in DI water: 5 minutes.

SC 2: 10 minutes, 1:1:5 solution, $HCl + H_2O_2 + H_2O$ at 75 degrees Celsius.

SC 1 removes the organic contaminants but produces a very thin layer of silicon dioxide (about 10 Angstroms) and some metallic contaminants. The HF dip step removes the silicon dioxide layer and some of the metallic contaminants. The SC 2 step then removes the remaining metallic contamination. After this step the wafers are then processed in the *SRD* Rinse/Spin Dry tool, which rinses the wafers with DI water and

dries with nitrogen or air. This step prevents the operator from coming into contact with dangerous cleaning chemistry. The RCA wet bench is shown in Figure 4.3.

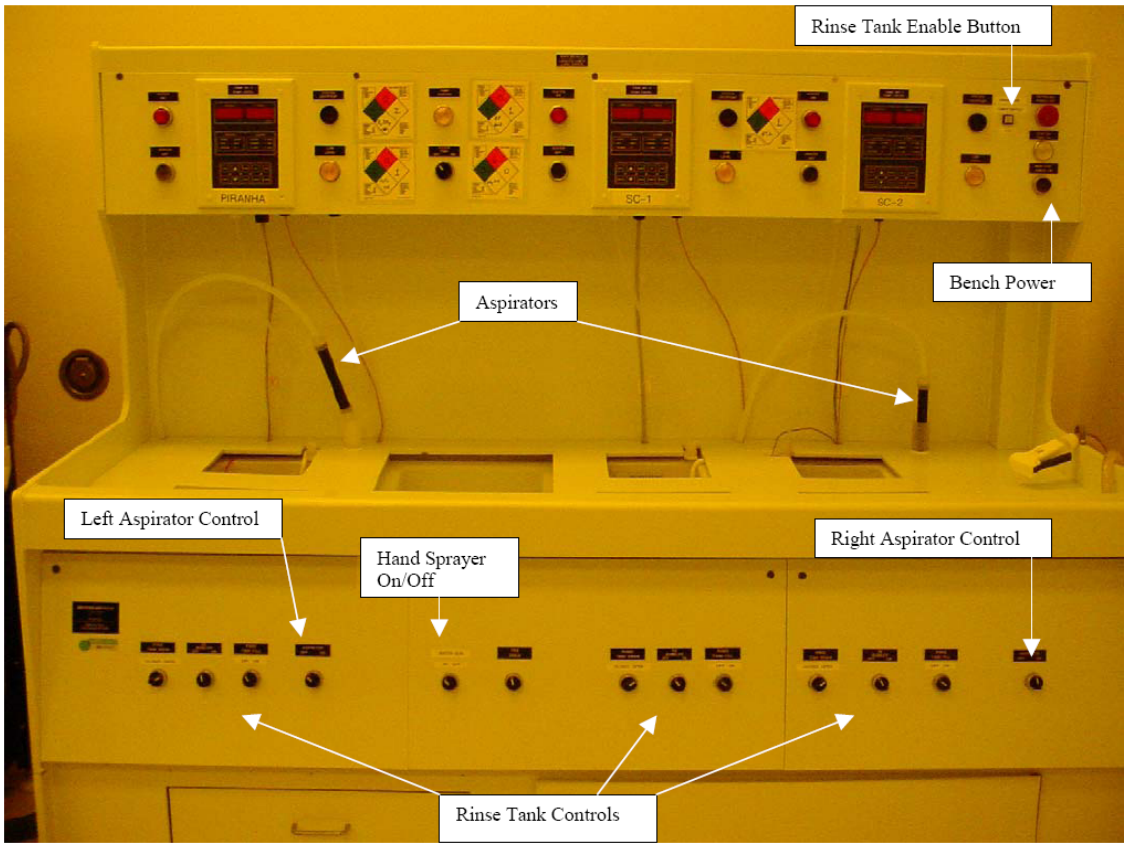

Fig. 4.3: RCA clean wet bench at SMFL [4]

4.2.2 Oxide deposition

The first process step is the deposition of 3 µm of silicon dioxide. This layer acts as the bottom cladding for the device layer – which contains the waveguides. For speed, the *AME P5000* Plasma Enhanced Chemical Vapor Deposition (PECVD) tool was used to deposit Tetraethyl orthosilicate (TEOS) silicon dioxide. Deposition my PECVD takes approximately 1 hour 30 minutes from equipment startup while depositing 3 µm by an oxidation furnace would take over 17 hours. Growing the silicon dioxide by oxidation

would also consume approximately 46% of the silicon substrate [5], a factor that is not present in PECVD. TEOS layers also have excellent conformality and are deposited at a lower temperature - 390 degrees Celsius in this tool. They however have the problem of absorbing water molecules from the air, so care has to be taken to keep wafers contained most of the time [6]. The TEOS layer suffices as a bottom cladding because it has the same refractive index as grown silicon dioxide and hence can provide suitable optical confinement due to index difference with the polycrystalline silicon layer that will be deposited. The *ASME P5000* PECVD tool used to produce this layer is shown in Figure 4.4.

Fig. 4.4: AME P5000 PECVD tool

4.2.3 Polycrystalline silicon deposition

A 270 nm thick layer of amorphous silicon (a-Si) is deposited by low-pressure CVD (LPCVD) at 550 degrees C from SiH_4. This layer is then crystallized into polycrystalline silicon by a two-step thermal anneal process. The first anneal step is at 600 C for 24 hours and then at 1050 C for 10 minutes in pure nitrogen (inert) ambient. This is in accordance with Solid-Phase Crystallization (SPC) and produces a layer of very low surface roughness [7, 8]. The reason, the layer is deposited first as a-Si, then crystallized by SPC is because a layer made in this manner has been shown to possess not only a more conformal layer but a layer that produces waveguides with improved sidewall roughness [8]. Sidewall roughness accounts for a large part of the optical losses in waveguides. Minimizing this factor by using SPC, even though it takes much longer than direct polycrystalline silicon deposition, is a very useful step in getting optimized devices at the end.

The two step SPC includes: grain growth and nucleation. Grain growth expands the grain size in the forming crystalline film; this has the positive effect of limiting optical losses that realize at grain boundaries. The fewer grain boundaries in the deposited film the lower the optical losses. This is performed at 600 C. The grain growth rate is extracted from grain progression data [7, 9] and dictated the anneal time. Nucleation is the event that transforms a homogenous structure, in this case amorphous silicon into crystallized material. In this process, the nucleation is done at 1050 C in a Rapid Thermal Processing (RTP) chamber. The nucleation activation energy is extracted from the time to the beginning of crystallization, and this factor dictates the temperature and time of anneal used. To achieve the largest possible grain, the nucleation energy

(process temperature) can be reduced relative to the grain growth process temperature. The trade-off is that this causes an increase in throughput through (due to slower crystallization).

The process steps taken in this work are very similar to other successful SPC steps in [10]. The *ASM* LPCVD tool used is shown in Figure 4.5. There were some problems with films produced with the RIT SMFL tool with regards to film's optical qualities, so the initial layer was deposited at the Cornell CNF cleanroom facility. The issues that warranted the use of an external facility for this deposition will be addressed later in this thesis.

Fig. 4.5: ASM LPCVD tool at RIT SMFL

The process parameters used for the deposition where:

Temperature: 550 C

Gas used: Silane (SiH_4); Pressure: 300 mTorr; Flow: 50 sccm

Rate of deposition: 35 Angstrom/minute

Total film thickness: 270 nm

The first step of the SPC process was then conducted after an RCA clean. The wafers were annealed in the RIT SMFL oxidation furnace (Bruce furnace). The process was in nitrogen ambient with a maximum temperature of 600 C for 24 hours. The Bruce Oxidation and Annealing furnaces at the RIT SMFL are shown in Figure 4.6.

Fig. 4.6: Bruce Furnace at RIT SMFL

The final step is the nucleation anneal. This is done with the *AG 610* RTP tool. The wafers are annealed at 1050 C for 10 minutes. The AG 610 RTP tool at the RIT SMFL is shown below. Figure 4.7 shows the RTP system.

Fig. 4.7: AG 610 RTP tool at RIT SMFL

4.2.4 Bottom Anti-Reflection Coating (BARC) deposition

After the film depositions, the waveguide structures are transferred unto the wafers by photolithography. Prior to performing lithography, a Bottom Anti-Reflection Coating (BARC) is applied on the wafer surface to help reduce or possibly eliminate standing waves and reflective notching in the photoresist that is applied [11]. A reduction in standing waves improves the side wall roughness of the produced waveguides, making the deposition of BARC a very useful process step. The XLT-20 is the BARC used. It is

spun on using the *CEE* Spin Coater. It is applied at 4000 RPM for 60 seconds; a resist thickness of 2200 Angstrom is obtained. The *CEE* Spin coater used is shown in Figure 4.8. A two step post bake is utilized: first at 100 C for 60 seconds and at 168 C for 60 seconds.

Fig. 4.8: CEE Spin coater at RIT SMFL

4.2.5 Photoresist coating

A layer of photoresist is then applied to capture the mask pattern unto to the wafer. Photoresist is a material which changes properties when exposed to light. A positive resist, Arch OIR 620, is used due to the type of mask selected. The resist is applied using the automated *SSI* coat and develop track. The SSI track is a 6" wafer track is a full process system which contains spinners and hot plates which bake the resist. The SSI track is shown in Figure 4.9.

Fig. 4.9: SSI coat and develop track at RIT SMFL

Since a BARC layer has already been deposited, a recipe without HMDS, a primer, is used. The “NOHMDS” recipe spins the resist at 4150 RPM for 30 seconds and gives a thickness of 9000 Angstrom. A post bake is done at 140 C for 60 seconds to solidify the resist. Full recipe detail is available at [12].

4.2.6 Photolithography - exposure

The photolithography step transfers the layout pattern from the mask to the wafer. This is realized when light of known wavelength is incident on a photoresist layer through a photomask. The light passes un-hindered in areas of the mask without chrome, changing the chemical properties of the resist. The lithography patterning was accomplished using the *i-line Canon* stepper (FPA 2000-il). This tool possesses focus =

0.8 μm, NA = 0.52, resolution = 0.5 μm, and wavelength = 365 nm. The Canon stepper used is shown in Figure 4.10.

Fig. 4.10: Canon stepper at RIT SMFL

Before exposure the number of replications, the die size and spacing between adjacent dies of the mask pattern to be made on the wafer has to be set. This can be done by defining variables in the stepper job file. The die size is done by setting the position of the blades that limit the area of the mask that is exposed to light. The variables are B_L, $B_Г$, B_u, and B_d, which represent the positions of left, right, up and down in a Cartesian coordinate system where the origin is the center of the mask. The die layout on the wafer is shown in Figure 4.11.

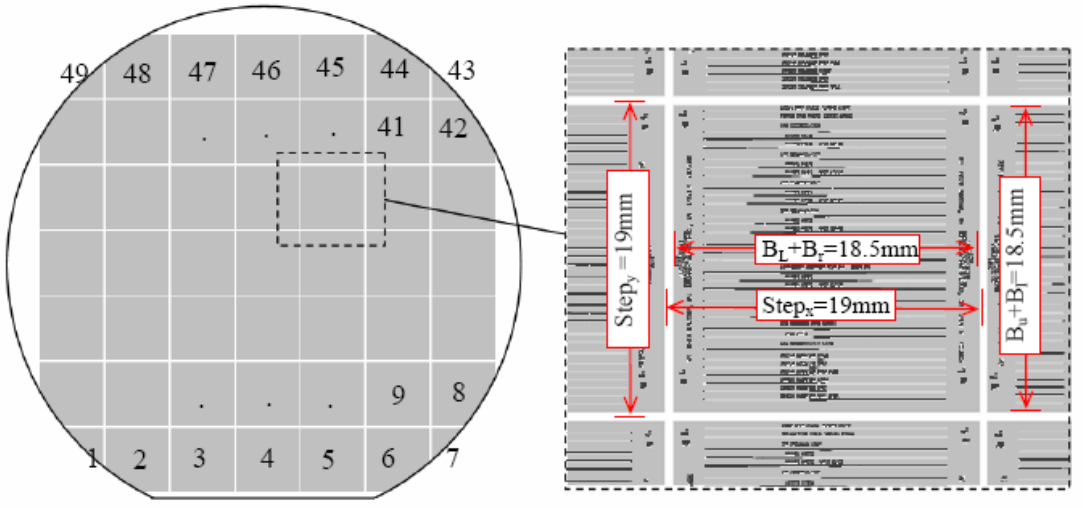

Fig. 4.11: Die layout [1]

The stepper job used in this work has the job name: OGAH, B_L = -9.25 mm, B_Γ = 9.25 mm, B_u =9.25 mm, B_d, = -9.25 mm, focus = 0.1 µm, exposure = 260 mJ/cm^2. The step variables, $Step_x$ and $Step_y$ define the distance between the same points on adjacent dies. In this stepper job, $Step_x$ and $Step_y$ are set as 19 mm. This serves to provide 500 µm spacing between dies. The stepper job shot 7x7 dies on the wafers for a total of 49. The optimal focus and exposure was determined by performing a focus exposure matrix. This is a process using the stepper where the focus is varied between each row, and the exposure between each column.

4.2.7 Photoresist developing

After patterning, the unwanted parts of the photoresist are chemically removed by using a photo developer. As a positive photoresist was used the parts exposed to light get removed. The developer used is the CD-26 which was applied on the SSI coat and develop track and used the "DEVELOP" recipe. The developer was sprayed, and the

wafer spun for 2 minutes, there was then a bake at 120 C for 2 minutes. The full recipe is available at [13].

4.2.8 Reactive Ion Etch (RIE) of polycrystalline silicon

The next step in the process is to etch back 200 nm of the polycrystalline silicon using the photoresist as a mask. The *Trion* RIE etch tool is used for this purpose. RIE is an etching technology that uses chemically reactive plasma to remove materials. RIE generates plasma by using an electromagnetic field at low pressure (vacuum) and inciting high energy ions from the plasma to attack the wafer surface. Specifically, it applies a large RF electric field to the chamber, which strips electrons off the gas moleucules, resulting in plasma. The wafer is DC isolated and the chamber walls are grounded, hence electrons build on the wafer, giving it negative potential. The positive ions of the plasma are then attracted to the wafer surface and as they collide with force they physically etch the target material.

The waveguide structures are formed by etching away 200 nm of poly silicon from the areas not protected by the photoresist mask. The Trion RIE etcher has high anisotropy which allows for relatively smooth vertical side walls. The strong electric field between the wafer and the plasma allow for this anisotropy [14].

The specific recipe used on the Trion RIE etch is “Preble-Si-Etch”. Pressure = 100 mTorr, RF power = 100 W, O_2 flow = 3 sccm, CF_4 flow = 25 sccm and process time = 240 seconds. After this process it was found that 191 nm was etched, meaning this recipe has an etch rate of approximately 48 nm/minute. The Trion Etcher used is shown in Figure 4.12.

Fig. 4.12: Trion RIE etcher at RIT SMFL

4.2.9 Plasma etch of photoresist

The next step is to strip off the photoresist used as a mask for the polycrystalline silicon etch step. This ensures that the resist remaining does not soften up and flow in later high temperature processes. This step also makes for clearer viewing, microscopy and metrology of structures on the wafer. The etching step, also called an ash step is done on the *Branson* L3200 Asher, using the "Hard Ash" recipe. This is an oxygen ash of fixed length used to remove hardened resist. It etches any organic layer (including the BARC), leaving behind just the poly silicon layer. The Branson etcher used is shown in Figure 4.13.

Fig. 4.13: Branson L3200 Asher at RIT SMFL

4.2.10 Measurements

After the waveguides are fabricated, measurements are made to find out if the dimensions match expectations. Planar dimensions like the width of waveguide structures can be measured via a microscope. The height of the structures was found using the *Tencor P2* profilometer as seen in Figure 4.14. The tool works by dragging a fine tip over the surface of the wafer; an accurate depiction of the wafer topography is acquired from the displacement of the tip. This tip displacement is plotted, giving a visual characterization of the step height of the structures and the general uniformity of the wafer and structure surface.

Fig. 4.14: Tencor P2 profilometer at RIT SMFL

4.2.11 Wafer dicing

The next process step is the dicing of the wafers. This involves the sawing or cutting of the wafer to expose a cross section of the devices for testing. In this case, the wafer is diced with the *Karl Suess KS775* wafer saw as shown in Figure 4.15. The decision was made to dice the wafer before the next step, ion implantation, because several samples were needed and only a limited number of wafers were available. Sawing is an automated and accurate way of individualizing the various dies on a wafer. It also does not produce the edge angles that other wafer cutting methods like cleaving cause. A disadvantage though is that sawing produces a certain amount of roughness on the wafer edges. This roughness causes scattering and hence optical losses. There are several issues

that crop up after wafer dicing that affect optical losses and measurements. These factors will be addressed later in this chapter and in the next.

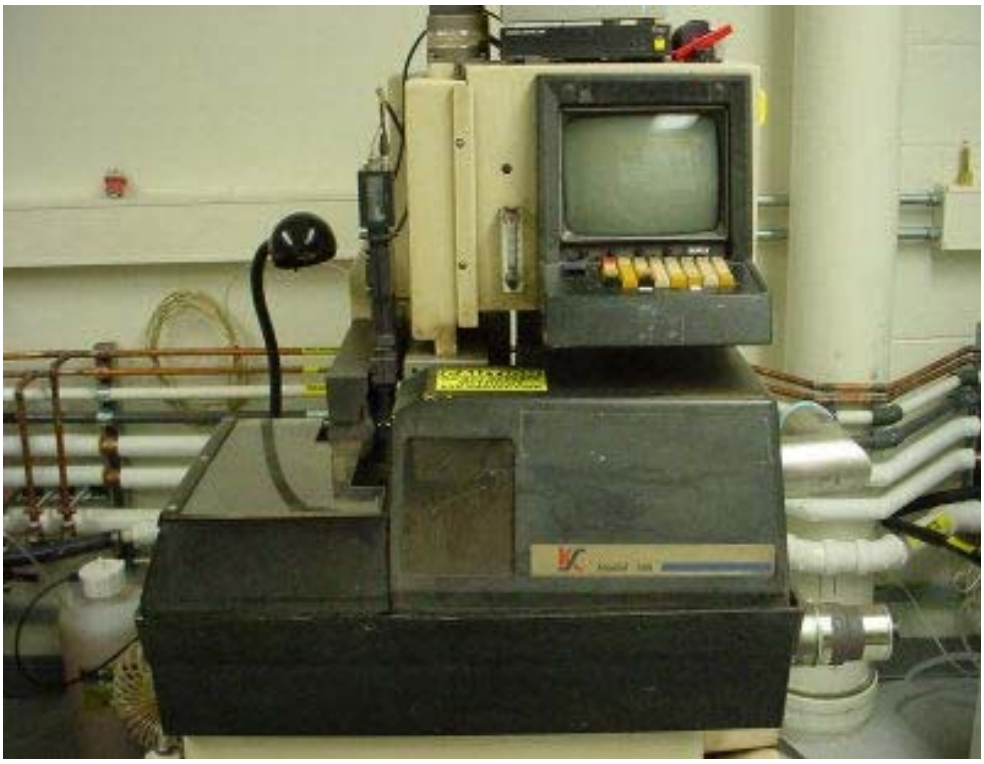

Fig. 4.15: KS775 wafer saw at RIT SMFL

Prior to dicing, a layer of photo resist is deposited on the completed wafer, to serve as protection from air particles, dust and project debris from the saw amongst other impurities in the lab. The dicing is not done in the cleanroom, so the resist deposition is especially important to preserve device integrity. Figure 4.16 shows a wafer after dicing. The blue material in Figure 4.16 is an adhesive used to hold the wafer die together during the cuts.

Before experimental testing, there will be further wafer dicing. It would involve cutting through the ends of the waveguides on both sides, exposing the waveguide cross section for testing. The final devices will be cut down into pieces as small as 2 mm in

length (18.5 mm in width) and cut down even further in a bid to calculate the absorption losses through the material.

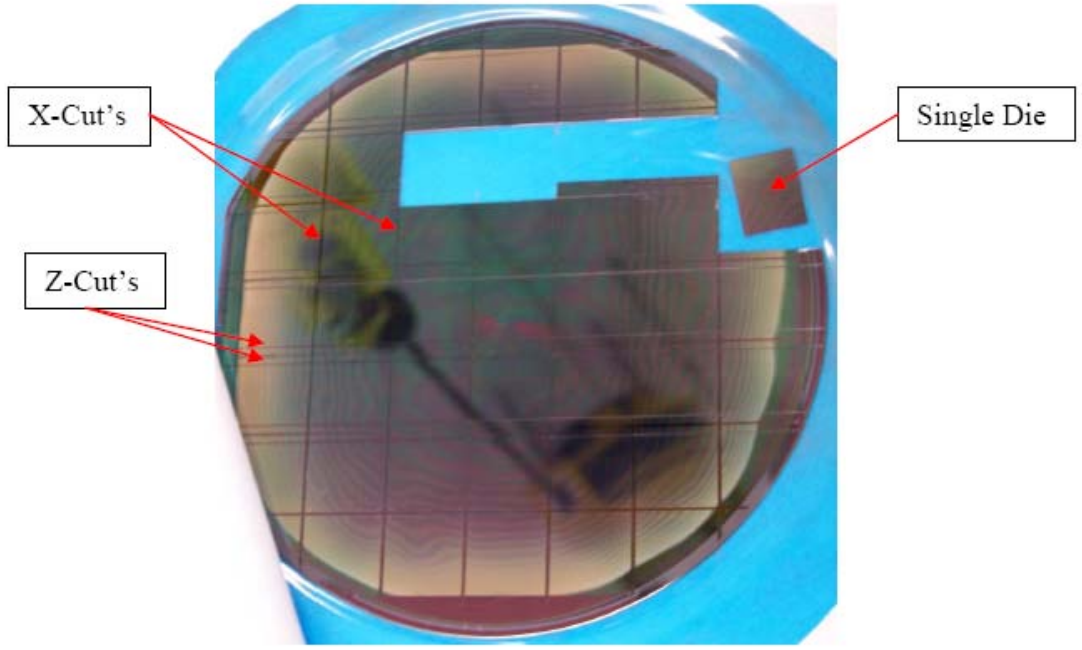

Fig. 4.16: Wafer after dicing step

4.2.12 Ion implantation of device wafers

The penultimate step is the introduction of dopants into the dies. The aim is to have several dies with varying carrier concentrations so that the absorption loss can be calculated after testing. Ion implantation is a process where dopant ions are implanted into a material thereby changing the physical and electrical properties of the implanted material. The crystal structure of the target can also be damaged by the energetic implanting so post-implant annealing is often necessary. Ion implantation is the most accurate method of injecting dopants – it can be used for very shallow implants, very low doses and as a low-temperature process is often more attractive than the furnace drive in

alternative. Ion implantation consists of an ion source, which produces the ions of a desired element, an accelerator, which accelerates ions with high energy electrostatically, and a target chamber, where the target is struck by the ions. The ions are extracted from the source and analyzed through a magnetic field, where Lorentz force takes the ions through a curved path which serves to separate ionic species based on their mass. By adjusting the magnetic field strength only the selected ions enter the accelerating column and eventually reach the wafer.

The amount of implanted material in the target is the integral of the ion current over time, and is called the implant dose [6]. The ion energy as well as the target and ion species used determines the depth of penetration into the target. The average penetration depth is the range, which usually falls between 10 mm and 1 μm. As ions travel through the target, they gradually lose energy due to collisions with target atoms and a small drag from electron orbitals [6]. The eventual loss of ion energy in the target is called stopping. The two types of stopping are electronic and nuclear. Electronic stopping is due to transfer of energy from impacting ion to the electrons of the target material. It does not cause crystal damage. Boron loses its energy mostly by electronic stopping. Nuclear stopping is due to transfer of energy from impacting ion to the nuclei of the target material. Phosphorus and arsenic lose their energy mostly by nuclear stopping. Substantial crystal damage is done on the silicon especially at high doses.

Dopant ions like boron, phosphorus or arsenic are used from a gas source, for higher purity and when implanted create a charge carrier, either hole or electron depending on if it is a p-type or n-type dopant. This modifies the electrical and optical properties of the semiconductor material.

In this work, the polycrystalline silicon waveguides will be implanted with boron (holes) and phosphorus (electrons) using the *Varian 350D* ion implanter as shown in Figure 4.17. Carrier concentrations of $1x10^{16}$ cm^{-3}, $1x10^{17}$ cm^{-3}, $1x10^{18}$ cm^{-3}, $1x10^{19}$ cm^{-3} are implanted for both boron and phosphorus. To achieve this range of carrier concentrations, doses of $4.1x10^{11}$ cm^{-2}, $3.3x10^{12}$ cm^{-2}, $3.4x10^{13}$ cm^{-2}, $3.2x10^{14}$ cm^{-2} and implant energy of 110 KeV are used for phosphorus (P31) implants respectively. Doses of $3.8x10^{11}$ cm^{-2}, $3.1x10^{12}$ cm^{-2}, $3.5x10^{13}$ cm^{-2}, $3.3x10^{14}$ cm^{-2} and implant energy of 40 KeV the boron (B11) implants respectively. The dose and implant energy values were derived via simulations through the Silvaco Athena software.

Fig. 4.17: Varian 350D Ion implater at the RIT SMFL

4.2.13 Post implant anneal and final cladding

The final process steps are the deposition of the top cladding and the post implant anneal used to help repair structural damage and to activate dopant ions. The top cladding is done by depositing 1 µm of TEOS using the AME P5000 as in section 4.2.2. This provides for Total Internal Reflection as the waveguide structures are now sandwiched between two high refractive index silicon dioxide layers. This helps minimize optical losses. After the cladding, the wafer is then annealed in nitrogen ambient in the following steps: 600 C for 30 minutes, 900 C for 15 minutes and 1050 C for 30 seconds. These anneal done on an oxidation furnace and RTP system help reduce structural damage done at implantation and maximizes the amount of dopant ions that are electrically activated [15]. With this step done the wafer are then ready to be diced in preparation for testing. A depiction of the cross section of the final device made is shown in Figure 4.18. Only one waveguide is shown for simplification.

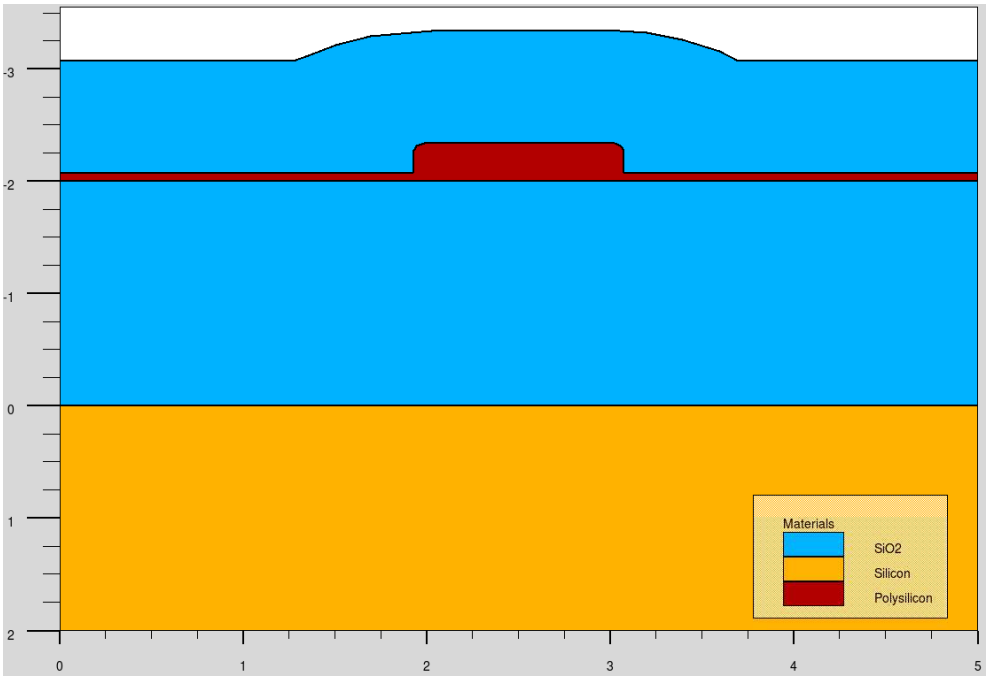

Fig. 4.18: Depiction of cross section of final device fabricated

4.3 Device metrology

After the final process steps, metrology is conducted to determine that the waveguides' integrity is acceptable from a test point of view. It is of experimental interest and future failure analysis to determine that there is not a significant number of waveguide breakages, and that the surface roughness and sidewalls are of a sufficient standard. In this work the structures where examined with microscopes and Scanning Electron Microscopes (SEM). The devices were of a sufficient standard. Figures 4.19 and 4.20 show some of the final device images.

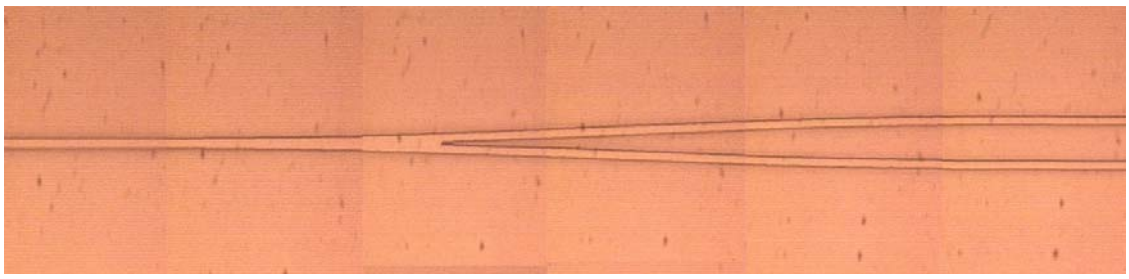

Fig. 4.19a: Devices under microscope examination

Fig. 4.19b: Further microscopy showing resist smudges post dicing

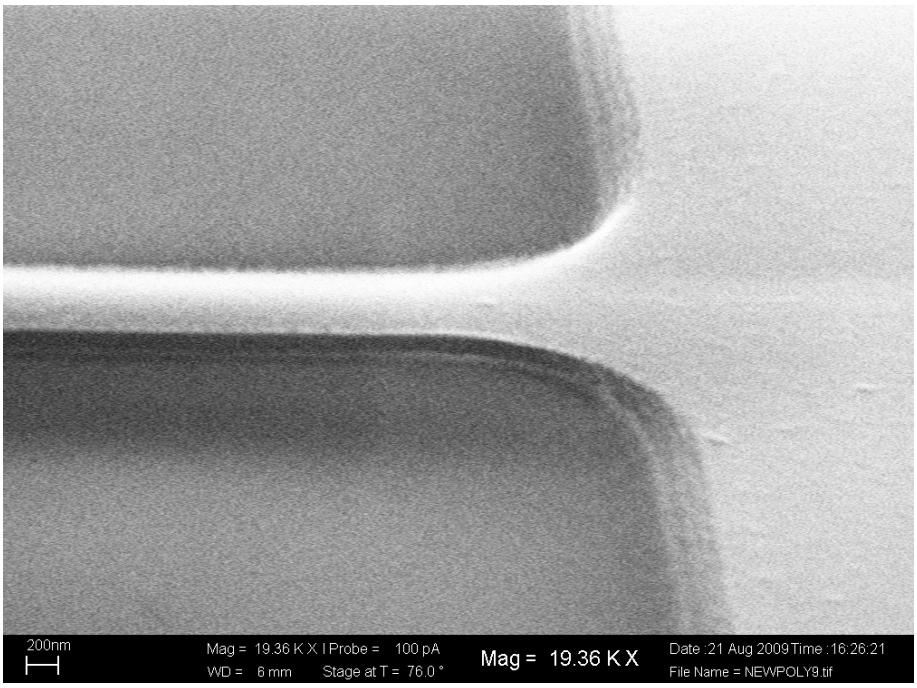

Fig. 4.20: SEM examination

4.4 Problems encountered

During the device fabrication, a significant problem cropped up which delayed the thesis work significantly. The problem encountered was the inability to get optical transmission through the polysilicon waveguides fabricated at the RIT SMFL using the AME LPCVD tool. Initially several etch and anneal recipes were attempted in an effort to optimize optical transmission, without any success. Eventually, a decision was made to produce the same film with the LPCVD tool at the Cornell CNF cleanroom using the exact same recipe. The new film as deposited at the Cornell CNF facility allowed optical transmission. The same anneal steps (furnace and RTP) were performed on wafers from both tools.

Ellipsometry was conducted on the two samples and both gave values of 3.46 at 1550 nm, which is the expected value for silicon. However the ellipsometer used is old

and may not have been able to accurately measure very small changes in the refractive indices of the materials. A small change in refractive index can alter transmission at certain wavelengths.

Atomic Force Microscope (AFM) tests were performed on samples from both facilities and the results are shown in Figure 4.21 and 4.22.

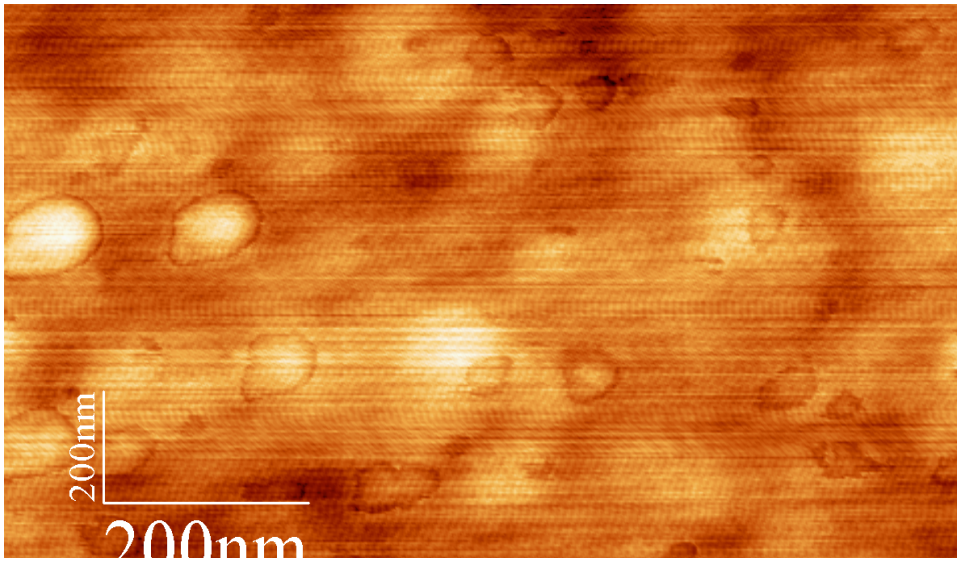

Fig. 4.21: Material produced with the LPCVD tool at the RIT SMFL

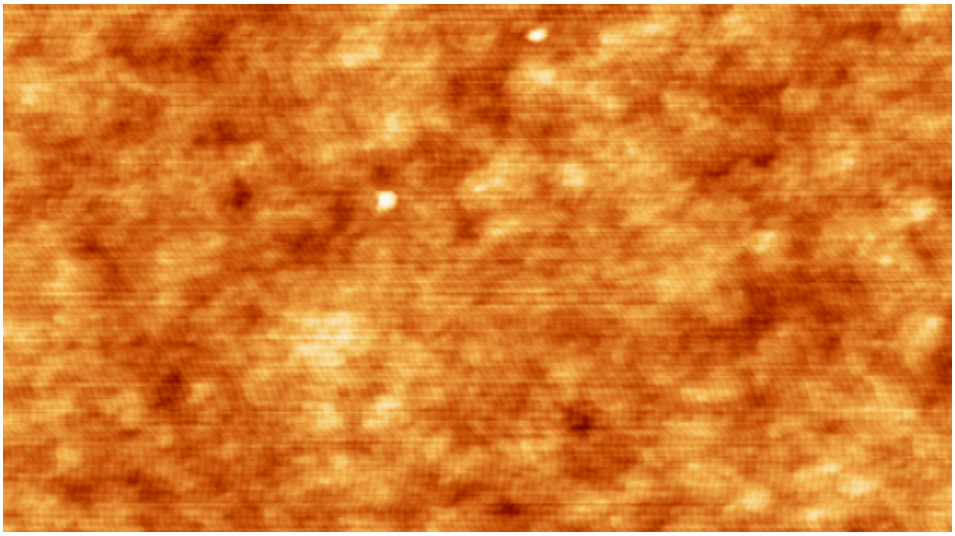

Fig. 4.22: Material produced with the LPCVD tool at the Cornell CNF (same scale as above)

AFM is a type of scanning probe microscopy with a very high resolution – over 1000 times better than the optical diffraction limit – and as such is one of the foremost tools for imaging. The AFM consists of a cantilever, usually made with silicon or silicon nitride [16]. At the end of the cantilever is a sharp tip, with a nano-scale radius of curvature, which serves as a probe. When the tip comes into proximity of the material's surface, several forces (van der Waals, capillary, electrostatic, chemical bonding, mechanical contact, magnetic, Casimir) cause a deflection of the cantilever, obeying Hooke's law. The deflection is measured using a reflected laser from the top of the cantilever and utilizing photodiodes. The AFM scans were done at the RIT Electrical Engineering department.

In the results it is clearly visible that there are approximately 80 nm sized grain-like particles in the film deposited with the SMFL tool. These do not exist on the film produced with the Cornell CNF LPCVD tool. Both Figures 4.21 and 4.22 have the same scale. After some investigation it is found that due to age, the SMFL tool is not completely sealed in. The lack of a full seal during a high temperature process would cause additional and unwanted oxygen and nitrogen into the chamber, adding impurities to the silane decomposition reaction in an uncontrolled manner. The large grain-like structures - which could be localized oxide regions - seem to be an artifact of this.

These grain-like structures would cause additional optical losses – through scattering even before the addition of doping, as losses occur at the boundaries of the materials regular grains. It is therefore my conclusion that these structures are a significant reason the optical losses in the SMFL deposited film is so high.

4.5 Summary

This chapter has shown the full fabrication flow that is implemented to produce the waveguide structures that will be optically tested. The waveguides produced showed good rib height and width uniformity. A lack of uniformity can not strongly affect the design parameters like the coupling coefficient but can also transform a single-mode waveguide into a multi-mode one. Working devices were produced that met expectations from a processing point of view.

4.6 References

[1] Eric Harvey, "Design and Fabrication of Silicon on Insulator Optical Waveguide Devices" RIT Electrical Engineering Dept. August 2006.

[2] Christopher Saint, Judy Saint, "IC Mask Design", New York, McGraw-Hill, 2002. pp. 20-25.

[3] Werner Kern, "Handbook of Semiconductor Wafer Cleaning Technology", p.49, Noyes Publications, New Jersey, 1993.

[4] Manual, "MOS Grade RCA Bench", RIT SMFL.

[5] Richard C. Jaeger, "Thermal Oxidation of Silicon: Introduction to Microelectronic Fabrication", Upper Saddle River, Prentice Hall, 2001.

[6] S. M. Sze, "Semiconductor Devices: Physics and Technology", Wiley India, 2008.

[7] V. Subramanian, P. Dankoski, L. Degertekin, B.T. Khuri-Yakub, K.C. Saraswat, "Controlled Two-Step Solid-Phase Crystallization for High-Performance Polysilicon TFTs", IEEE Electron Device Letters, Vol. 18, No. 8, August 1997.

[8] L. Liao, D.R. Lim, A.M. Agarwal, X.Duan, K.K. Lee, and L.C. Kimerling, "Optical transmission losses in polycrystalline silicon strip waveguides: effects of waveguide dimensions, thermal treatment, hydrogen passivation, and wavelength," J. Electron. Matter. 29(12), 1380-1386 (2000).

[9] K. Zellama, P. Germain, S. Squelard, J. C. Bourgoin, P. A. Thomas, "Crystallization in amorphous silicon," J. Appl. Phys., vol. 50, no. 11, p. 6995, 1979.

[10] K. Preston, S. Manipatruni, A. Godarenko, C. B. Poitras, M. Lipson, "Deposited silicon high-speed integrated electro-optic modulator," Optics Express 5118, Vol. 17, No. 7, 2009.

[11] RIT SFML, ARC product overview. Available: http://appserver.microe.rit.edu/ classes/emcr666_676/reference/arcs/Product_Overview_arcs.pdf

[12] RIT SFML, Process capabilities SSI Track-Coat Process. Available: http://smfl.microe .rit.edu/Process%20Information/SSI%20SMFLCOAT.pdf

[13] RIT SFML, Process capabilities SSI Track-Coat Develop. Available: http://smfl. microe.rit.edu/Process%20Information/SSI%20SMFLDEV.pdf

[14] Jerome J Cuomo, Stephen M Rossnagel, and William D Westwood, Handbook of Plasma Processing Technology, Norwich, New York, William Andrew Inc., 1990. pp. 196-204.

[15] T. Kamins, "Polycrystalline Silicon for Integrated Circuits and Displays*",* 2nd ed. Kluwer, 1998.

[16] P. West, "Introduction to Atomic Force Microscopy: Theory, Practice and Applications," www.AFMUniversity.org

Chapter 5

Experimental Measurements

One of the most important and tasking aspects of waveguide fabrication is the testing of its operation. Focusing and aligning light into a well-diced and polished end facet of a waveguide is complex and time consuming. This chapter will discuss the techniques used to test the polysilicon waveguide devices' operation, the transmission results obtained and the calculated polysilicon absorption values for holes and electrons at 1550 nm. A comparison of obtained results will be made with crystalline silicon values in [1].

5.1 Facet preparations

Before testing, an edge perpendicular to the waveguides that exposes the devices' cross section has to be created. This edge is called an interface facet. It is used to provide a point through which an optical fiber can transmit laser light through the waveguide and have it measured at the output.

The two main methods used to create a facet are by cleaving and sawing. Cleaving involves using a diamond tip pen-structure to break a wafer along its 1-1-1 crystal plane. It can produce very smooth facets if done properly, but can also produce edge angles which can increase optical loss. Sawing utilizes an automated blade to dice the wafer. This avoids edge angles but tend to produce greater edge roughness which can increase scattering and hence losses.

In this work, sawing (dicing) was used as it was more a more accurate and consistent method. This was done using the KS 775 wafer saw. Before any dicing is

done, a layer of photoresist is applied manually to protect the wafer from dicing debris and the non-cleanroom environment of the laboratory in which the wafer saw is located. To help reduce the edge roughness and coupling insertion loss, an extra polishing step was performed after sawing to give a more uniform edge. A rough edge with several cut lines causes scattering which could result in up to 10 dB of optical insertion losses, while a smooth edge has been shown to give as low as 1 dB of insertion loss. A quality polishing step is therefore desirable. The polishing was done with the *Allied Techprep* grinding and polishing system as shown in Figure 5.1.

Fig. 5.1: Allied Techprep grinding and polishing system

A photoresist layer is also necessary while polishing, for the same reasons as when sawing. One of the disadvantages of polishing is that there is a chance of damaging the edge of the wafer or chipping the edge which could remove portions of the waveguide

at the edge of the wafer. After the facets have been prepared, the protective layer of photoresist is removed to prepare for device testing. The resist is removed with acetone, iso-propanol, rinsed with DI water and dried with an air or nitrogen gun.

5.2 Experimental setup

To test the fabricated and prepared waveguide devices, light has to be coupled into the 2 μm wide waveguide with great precision and minimal losses. An optical test setup has to be devised to align a beam of light with the waveguide input end and measure the power received at the output end. The experimental setup designed for this task is comprised of several laser posts, fiber holders, mounting brackets and optical translation tables. An illustration of the test set up used is shown in Figure 5.2.

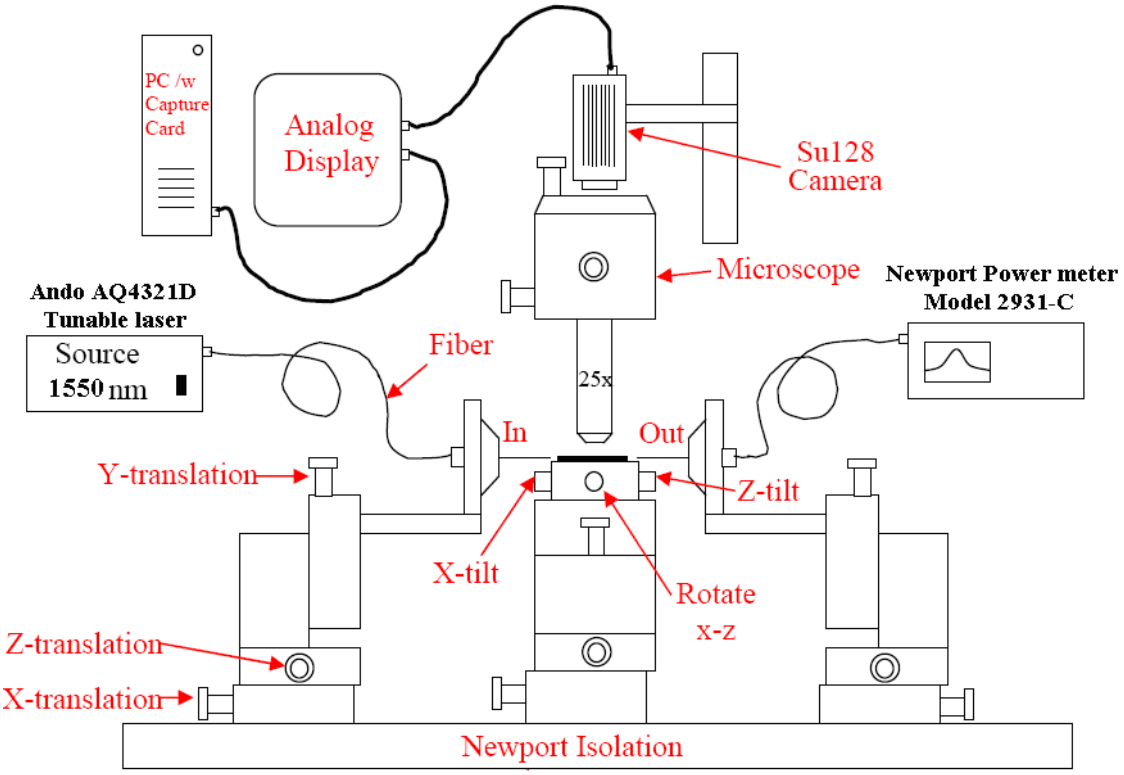

Fig. 5.2: Waveguide test setup

The setup comprises of four x-y-z translation platforms to provide alignment of the die, microscope, input and output fiber. The input fiber has to be stripped and prepared. After preparation, the fiber is mounted onto the fiber holder and aligned with the waveguides with adjustments made through the x-y-z translation stages. The end of the fiber not in proximity to the waveguide is mounted onto a fiber connector and attached to the input source, the *Ando AQ4321D* Tunable laser source. The laser source is shown in Figure 5.3.

Fig. 5.3: AQ4321D tunable laser source

The central stage holds the wafer die and can be moved or tilted. On the right hand side is the output stage which holds a prepared fiber tip to detect the light coming out from the waveguide and transmit it to the measurement device, the *Newport power meter 2931-C*. This is shown in Figure 5.4. This device plots the power of the optical signal coming out of the waveguide output end verses the wavelength chosen.

The microscope is placed above the three translation stages and has been detached from its base and connected to a post in a position directly over the die. The microscope

has its own translation stages and can be moved independently in the x-y-z directions. A picture of the full set up is shown in Figure 5.5.

Fig. 5.4: Newport power meter – 2931-C

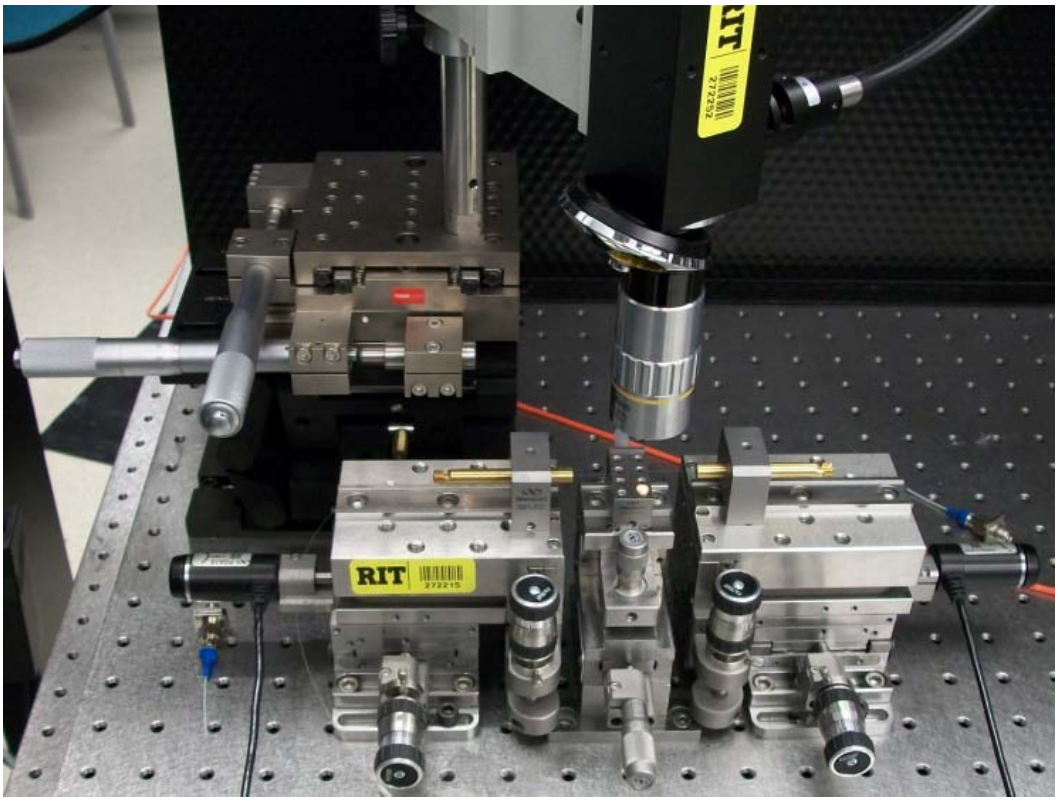

Fig. 5.5: Picture of test setup

Another important factor critical to minimizing insertion losses other than the quality of the facet and the fiber-waveguide alignment is the coupling technique. In this work direct butt coupling with a tapered tip was used. This is made by heating a portion of the fiber and pulling, stretching the fiber thin and forming a tip. The advantage of this is that the tip is smaller than the width of the waveguide, hence allowing for more light to be coupled. A disadvantage is that due to its non-smooth nature, some scattering occurs. The *Ericson FSU975* fiber fuser is used to make the tapers and is shown in Figure 5.6a. An illustrated tapered fiber tip is shown in Figure 5.6b.

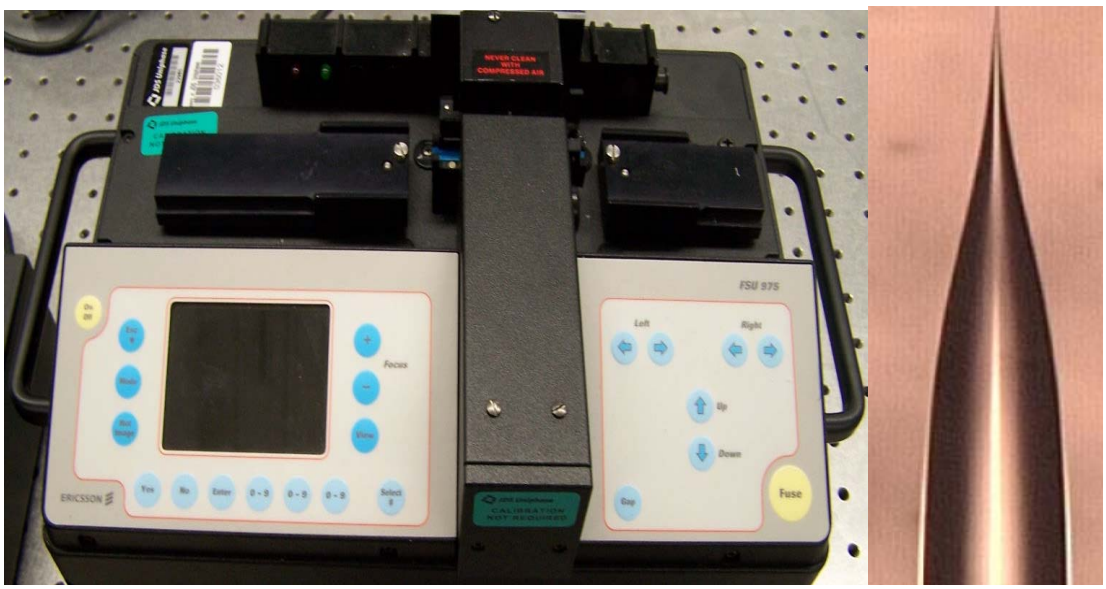

Fig. 5.6: a) FSU975 fuser, b) Tapered optical fiber tip

5.3 Results

To ensure optimal alignment of the input into the waveguide steps are taken. The device die is prepared as discussed above, and placed on the center translation stages; the input fiber is inserted into the fiber holder of the input translation stage with extra care to ensure the tip of the tapered fiber does not hit a solid surface causing it to break. A visual

then camera-based alignment is used to align the optical fiber into the input end of the waveguide structures. The optical fiber carries infrared light, 1550 nm wavelength. The fiber is then maneuvered in the x-y-z direction, to ensure it is actually well aligned to the structures. This can be visually determined by checking for reflections on the facets and is well handled after some experience has been gained. The camera has to be set in focus to capture the structures properly. The camera, on video mode is shown on the CRT connected to it. On the other end of the waveguides, the output fiber is also inserted into its fiber holder and aligned to the output of the waveguides to capture the transmission through the devices. The infrared light is then turned on and transmission measured. Pictures showing the optical fiber illuminating the optical waveguides are shown in Figure 5.8 and 5.9.

Fig. 5.7: Input fiber illuminating device

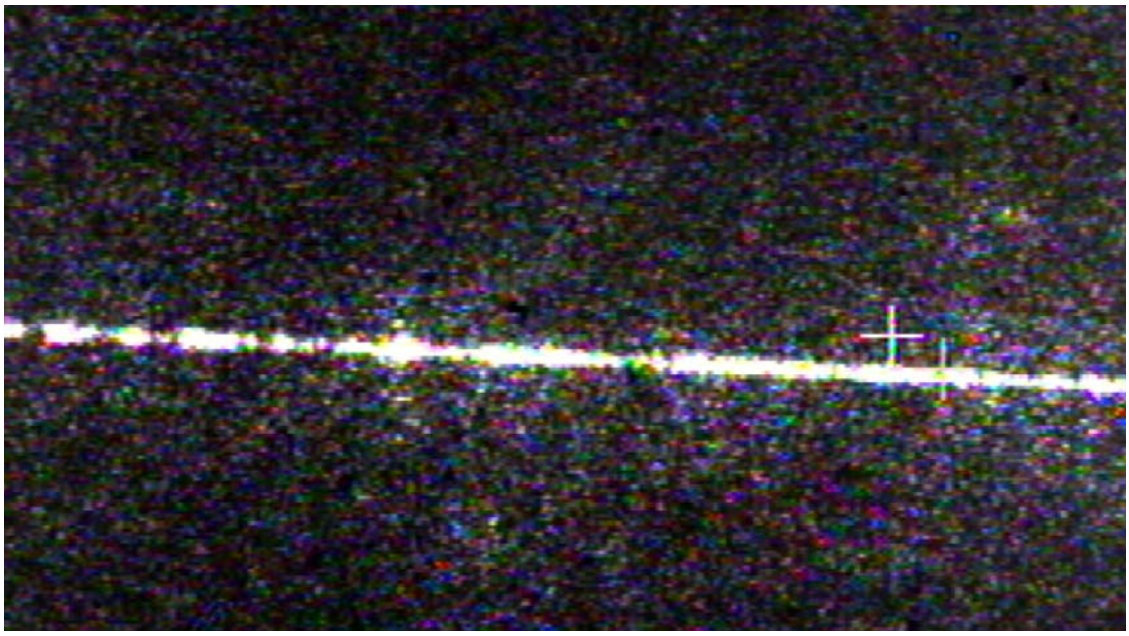

Fig. 5.8: Coupled single mode waveguide

Figures 5.7 and 5.8 show successful coupling of infrared light at 1550 nm wavelength into the waveguide devices. Only single-mode waveguides were tested for consistency in results. The propagation light in the waveguides is clearly visible because there are small amounts of scattering off the edges of the waveguide. The structures were 2mm in length. This length was chosen because it was decided more consistent results could be achieved from smaller lengths. It also allows for fewer waveguide breaks or shorts.

The pieces that were doped with phosphorus (N-type) and boron (P-type) were tested and transmission captured from the output end of the waveguides. After each test, the same piece is diced by an additional 0.25 mm using the K&S saw. The cuts made were the initial 2 mm, 1.75 mm, 1.5 mm, 1.25 mm and 1.0 mm. However at the 1.0 mm cut, significant damage was done to the edges of the waveguide that it was impossible to

couple and light in any of the structures. The pieces were essentially destroyed. The phosphorus and boron doped $1x10^{19}$ cm^{-3} implanted devices showed very high losses and failed to work. Prior to any testing the un-doped pieces was tested to serve as a reference and to aid in absorption calculations afterwards. The same pieces that were tested were then implanted and repeatedly diced. This was done so that the exact same sets of samples were used – improving experimental certainty and reducing wafer processing variations. Tables 1 and 2 show the results received for n- and p-type doped samples.

No doping

Remark: 16.5337 dB/cm loss

Waveguide length (mm)	Normalized Transmission (dB)	Δα (cm-1)
2	-1.2398	
1.75	-0.6394	5.53
1.5	-0.5094	1.2
1.25	0.0000	4.69

Phosphorus – $1x10^{-16}$ cm^{-3}

Remark: 22.7779 dB/cm loss

Waveguide length (mm)	Normalized Transmission (dB)	Δα (cm-1)
2	-1.7098	
1.75	-1.0158	6.39
1.5	-0.8515	1.51
1.25	0.0000	7.83

Phosphorus – $1x10^{-17}$ cm^{-3}

Remark: 29.8662 dB/cm loss

Waveguide length (mm)	Normalized Transmission (dB)	Δα (cm-1)
2	-2.2402	
1.75	-2.5015	-2.39
1.5	-0.8299	1.54
1.25	0.0000	7.64

Phosphorus – $1x10^{-18}$ cm^{-3}

Remark: 43.3423 dB/cm loss

Waveguide length (mm)	Normalized Transmission (dB)	Δα (cm-1)
2	-3.2511	
1.75	-1.7304	1.41
1.5	-1.1804	5.07
1.25	0.0000	10.9

Table 5.1: Transmission data for N-type samples

The average Δα values were 3.81, 5.24, 6.88, 9.98 cm^{-1} for un-doped, $1x10^{-16}$, $1x10^{-17}$, $1x10^{-18}$ cm^{-3} respectively. Plots of these values are shown in Figures 5.9. There is a significant downward slope signifying a decrease in transmission for longer lengths – which is intuitive. The un-doped polysilicon shows a material loss of 16.5337 dB/cm and increases for implanted devices. Further analysis of these results will be expatiated later on in the chapter.

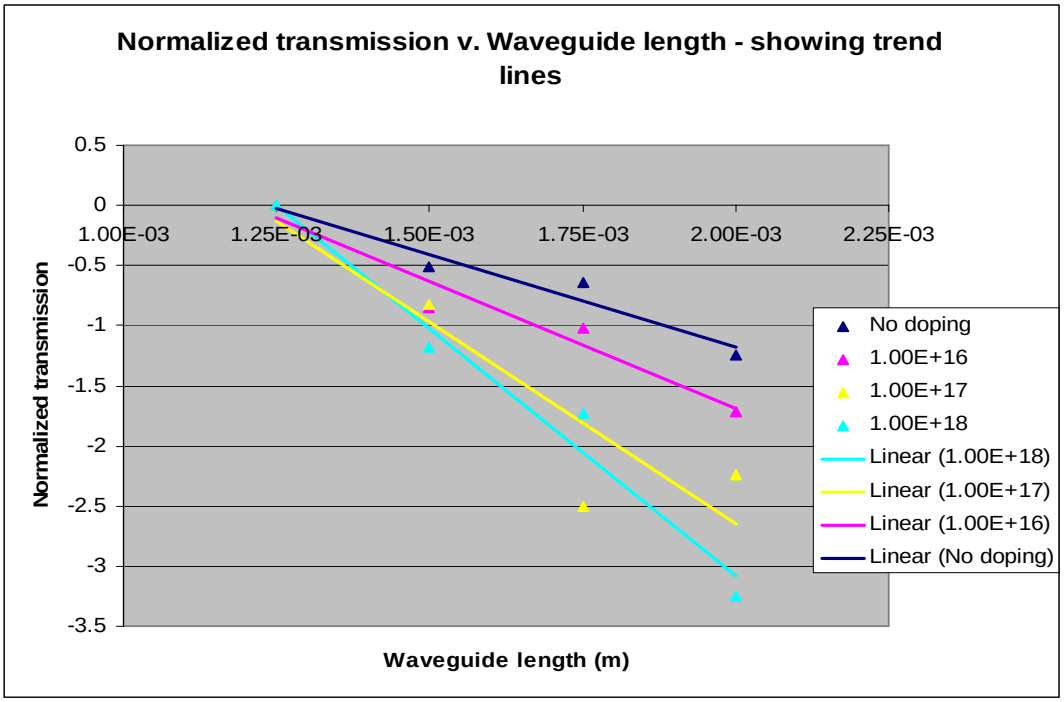

Fig. 5.9: Normalized transmission v. Waveguide length for phosphorus doped samples

The same process steps were used for the boron doped samples. The samples had severe edge chipping by the 1.25 mm dice, so no measurements were taken for that.

No doping

Remark: 14.5 dB/cm loss

Waveguide length (mm)	Normalized Transmission (dB)	Δα (cm-1)
2	-0.726	
1.75	-0.125	5.53
1.5	0.00	1.15

Boron – $1x10^{-16}$ cm^{-3}

Remark: 21.9997 dB/cm loss

Waveguide length (mm)	Normalized Transmission (dB)	Δα (cm-1)
2	-1.10	
1.75	-0.46	6.03
1.5	0.00	4.14

Boron – $1x10^{-17}$ cm^{-3}

Remark: 26.8692 dB/cm loss

Waveguide length (mm)	Normalized Transmission (dB)	Δα (cm-1)
2	-1.34	
1.75	-0.66	6.27
1.5	0.00	6.08

Boron – $1x10^{-18}$ cm^{-3}

Remark: 37.7606 dB/cm loss

Waveguide length (mm)	Normalized Transmission (dB)	Δα (cm-1)
2	-1.89	
1.75	-0.33	1.43
1.5	0.00	3.06

Table 5.2: Transmission data for P-type samples

The average Δα values were 3.34, 5.08, 6.17, 8.69 cm^{-1} for un-doped, $1x10^{-16}$, $1x10^{-17}$, $1x10^{-18}$ cm^{-3} respectively. Plots of these values are shown in Figures 5.10.

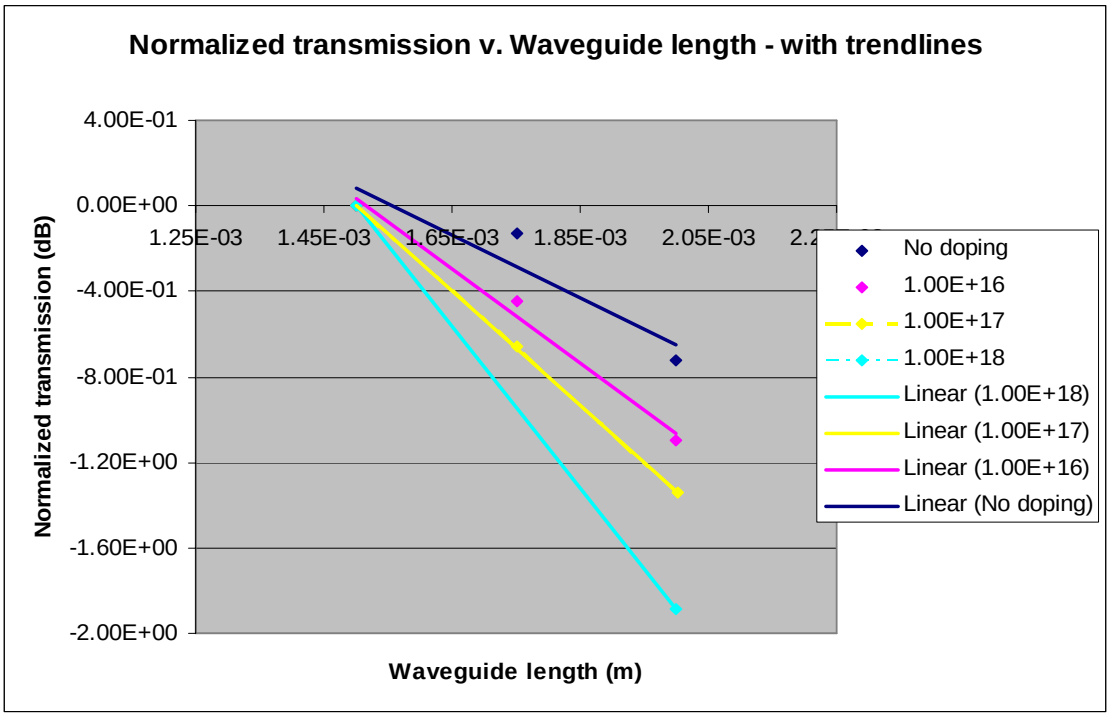

Fig. 5.10: Normalized transmission v. Waveguide length for boron doped samples

To arrive at the various plots several steps were taken to calculate the transmission (in dB) from the output power and eventually obtain the Δα and free carrier absorption. First the output power received is converted into decibel (dB), a logarithmic unit of measurement. This is done using the conversion equation as shown in equation 5.1:

$$T_{dB} = 10 \log_{10}(P_1/P_0) \qquad (5.1)$$

With P_1 and P_o being the output and input powers respectively and T_{dB} the transmission in dB. The data is then normalized with the lowest data point as reference. The values for Δα for each of the implant doses are then calculated by finding the Δα across different lengths, then averaging them. The formula for Δα used is derived from the *Beer-Lambert* equation:

$$T = \exp(-\alpha L) \quad (5.2)$$

$$\Delta\alpha = \ln (P_1/P_2) / (L_2-L_1) \quad (5.3)$$

Where P_1 and P_2 are powers of different length and L_1 and L_2 are the corresponding different lengths. With this method an average Δα value is arrived at for each carrier concentration node.

Now the aim is to find the absorption due to the free carriers alone, removing losses due to other reasons like scattering due to waveguide sidewall roughness, film uniformity or insertion losses. This can be done by removing the intrinsic losses from the total absorption losses.

$$\Delta\alpha_{total} = \Delta\alpha_{intrinsic} + \Delta\alpha_{free\ carrier} \quad (5.4)$$

The $\Delta\alpha_{intrinsic}$ is taken as the Δα value from the un-doped sample. Therefore to get the $\Delta\alpha_{intrinsic}$ for each carrier concentration node the intrinsic (values from un-doped sample) is subtracted from the total. This gives the values as shown in Table 3.

Carrier concentration (cm-3)	N-type $\Delta\alpha_{free\ carrier}$ (cm-1)	P-type $\Delta\alpha_{free\ carrier}$ (cm-1)
$1x10^{-16}$	1.44	1.74
$1x10^{-17}$	3.07	2.83
$1x10^{-18}$	6.17	5.35

Table 5.3: Free carrier absorption for polysilicon

A plot of the values shown in Table 5.3 is illustrated in Figure 5.11 with a trend-line inserted to show the visible increase in the absorption values as the carrier concentration is increased.

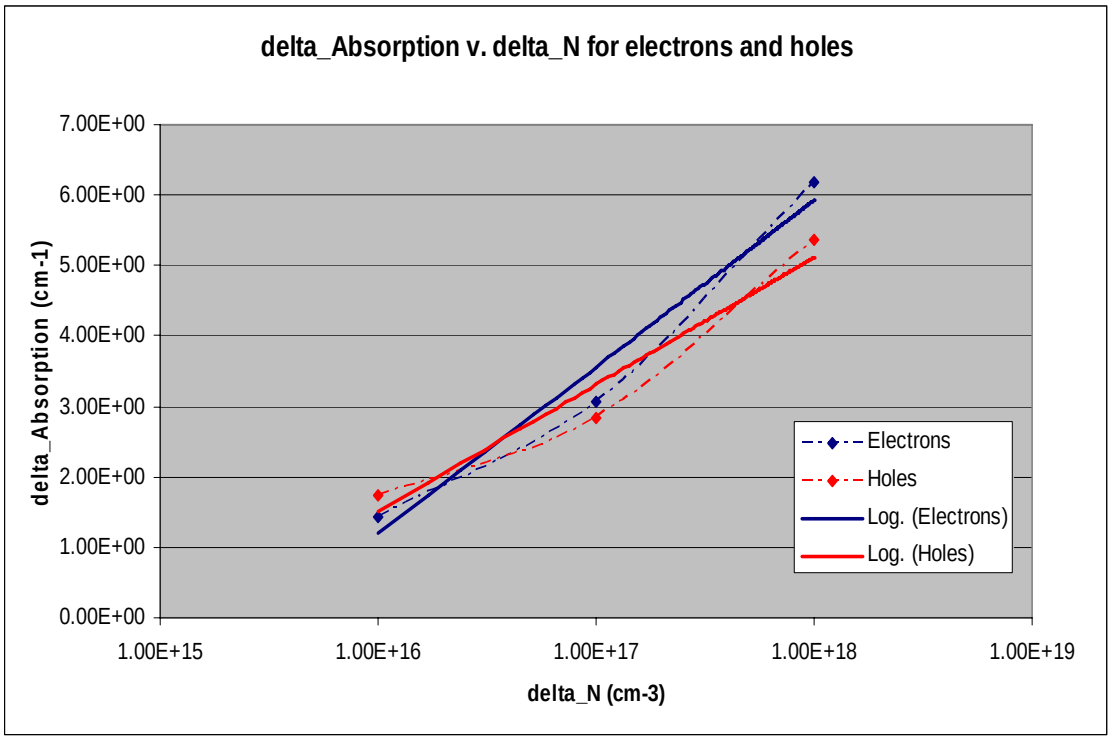

Fig. 5.11: Absorption in polysilicon at 1.55 μm v. free carrier concentration

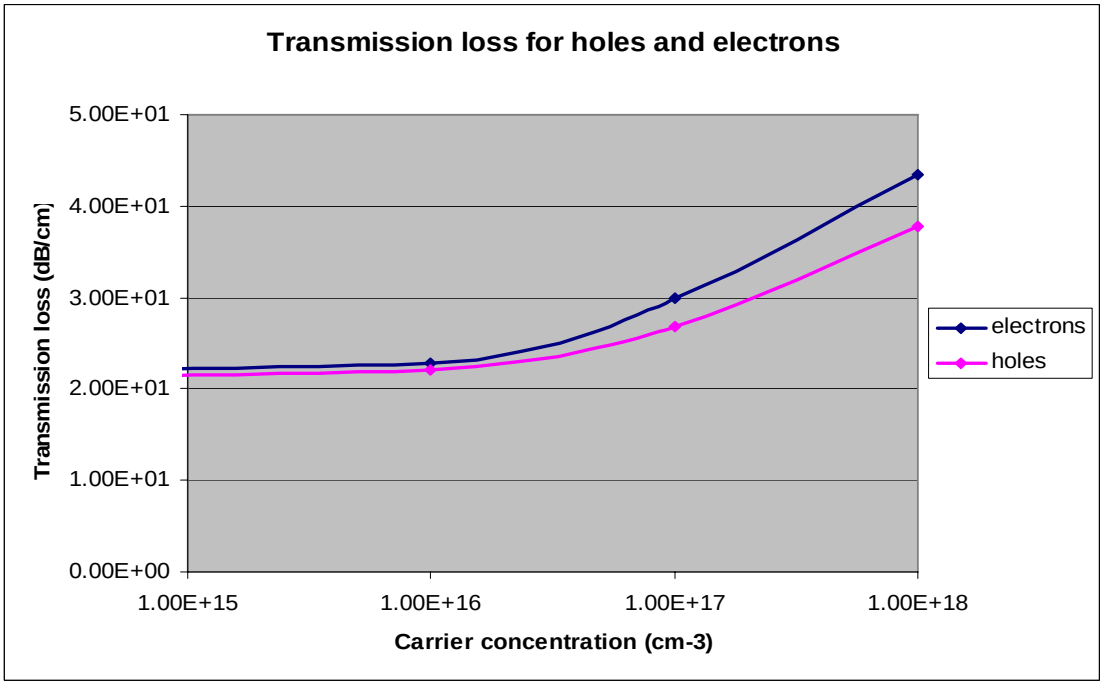

Fig. 5.12: Material transmission loss v. carrier concentration for polysilicon

Figure 5.12 shows the material transmission loss in dB/cm for each node. The values were obtained by averaging out the difference in transmission across several device lengths for each carrier concentration node.

5.4 Analysis

Figure 5.13 shows the Δα value for polysilicon obtained in this thesis work in comparison to the Δα values for c-Silicon as obtained in Soref's work [1].

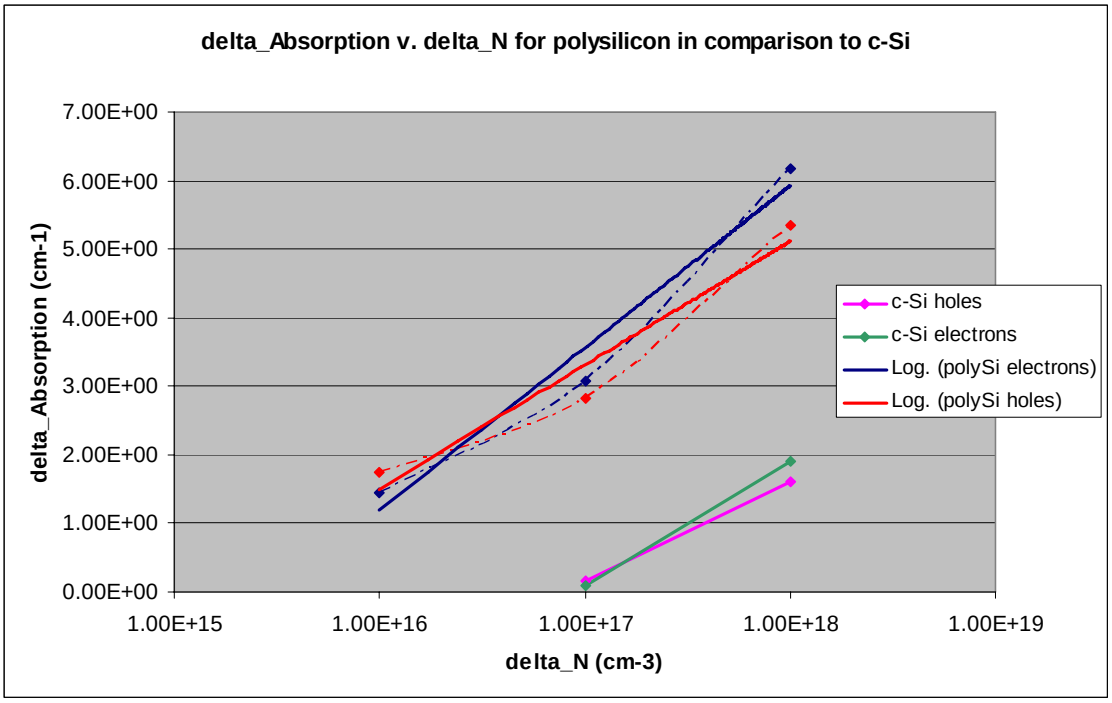

Fig. 5.13: Absorption in polysilicon in comparison to values for c-Si [1] at 1.55 µm

It is seen here that the absorption values for polysilicon is on the other 3 cm^{-1} larger than that of crystalline silicon. This is as expected since the loss is expected to be higher due to the number of grain boundaries that populate polysilicon material and reduce effective carrier mobility [2, 3]. The slope patterns of both sets of data are also

similar, and the polysilicon absorption values follow a trend that is expected, with a sharper increase in absorption between the 10^{-17} and 10^{-18} cm^{-3} nodes than from the 10^{-16} and 10^{-17} cm^{-3} nodes.

The slopes of for the polysilicon and crystalline silicon follow similar trends, however the slope of the polysilicon is slightly higher – a faster increase in absorption with step increase in carrier concentration. Now from [1], we have the Drude model, absorption equation:

$$\Delta\alpha = (e^3 \lambda^2 / 4 \pi^2 c^3 e_o n) [\Delta N_e / m_{ce}^{*2} \mu_e + \Delta N_h / m_{ch}^{*2} \mu_h] \quad (5.5)$$

Where *e* is the electronic charge, e_o is the permittivity of free space, *n* is the refractive index of silicon, m_{ce}^* is the conductivity effective mass of electrons, $m_{ch}^*$is the conductivity effective mass of holes, μ_e and μ_h are the electron and hole mobility respectively.

For crystalline silicon it can be simplified into Equation 5.6 as in [4].

$$\Delta\alpha = 8.5 \times 10^{-18} \Delta N + 6 \times 10^{-18} \Delta P \quad (5.6)$$

Where $\Delta\alpha$ (cm^{-1}), ΔN (cm^{-3}), ΔP (cm^{-3}) are the absorption-coefficient, the free electron and hole density respectively.

For polycrystalline silicon, the values of preceding constants for ΔN and ΔP are derived from the $\Delta\alpha$ slopes - by using Equation 5.7,

$$C = (\Delta\alpha_2 - \Delta\alpha_1) / (N_2 - N_1) \quad (5.7)$$

Where N_1 and N_2 are the different carrier concentrations and C is the slope constant. For my work, I derived the values for polysilicon from my data as:

$$\Delta\alpha = 10.79 \times 10^{-18} \Delta N + 7.47 \times 10^{-18} \Delta P \quad (5.8)$$

This marks a 26.9% increase in absorption due to electrons and a 24.5% increase in absorption due to holes. On average this is a 25.9% increase in free carrier absorption for polysilicon over crystalline silicon.

Comparing experimental data to simulated data, Figure 5.14 is obtained. The simulated theoretical data is obtained using Matlab and mobility values in [2] are used.

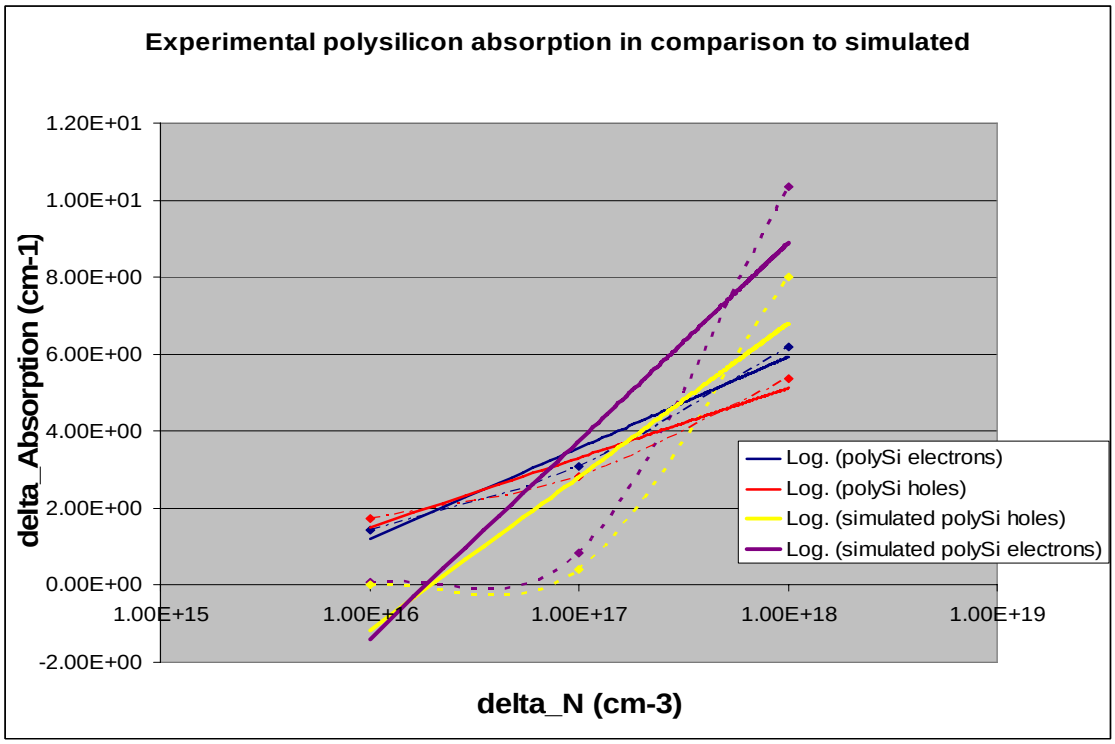

Fig. 5.14: Experimental polysilicon absorption data in comparison to simulated values

It is seen that the experimental values of absorption at low doping levels is much higher than the theoretical data. This changes as the carrier concentration approaches $1x10^{-18}$ cm^{-3}. The higher absorption at low carrier concentrations in the experiment might be due to processing reasons, while the higher absorption in the simulated data at $1x10^{-18}$ cm^{-3} is likely due to an over aggressive modeling of the hole and electron mobility values. There is a large variance in the mobility values given for polysilicon but in the

literature used, the given mobility value for polysilicon at $1x10^{-18}$ cm^{-3} is much lower than my sample would suggest. Also the grain size will play a role in any comparison as differing grain sizes - even by a few 10s of nanometers will give differing mobility and skew any comparisons. However there is a noticeable similarity in trend between the simulated and experimental data. Both crystalline and polysilicon data show the same trends of a small increase between $1x10^{-16}$ cm^{-3} and $1x10^{-17}$ cm^{-3} but a much larger increase between $1x10^{-17}$ cm^{-3} and $1x10^{-18}$ cm^{-3}

Figure 5.15 shows a comparison between the transmission losses of polysilicon as compared to crystalline silicon loss as obtained from [5].

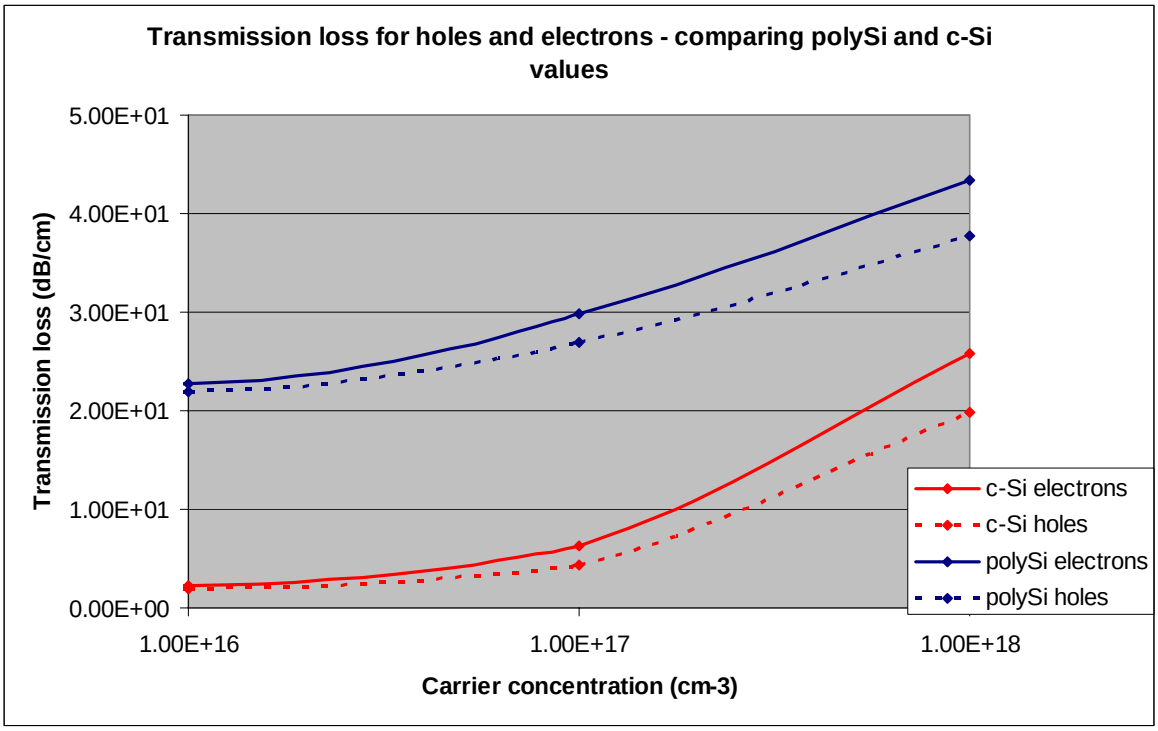

Fig. 5.15: Material transmission loss – comparing polySi and c-Si data

It can be seen that the additional loss induced by boron or phosphorus doping in the polysilicon waveguides increases at a lower rate than in c-Si waveguides. This might

be because some dopants in the polysilicon waveguides are segregated at the grain boundaries and hence do not contribute carriers – or it might also be due to the fabrication processing anneals utilized in [5]. Figure 5.15 shows a normalized plot to more clearly illustrate the difference in the rate of increase in waveguide loss as carrier concentration increases.

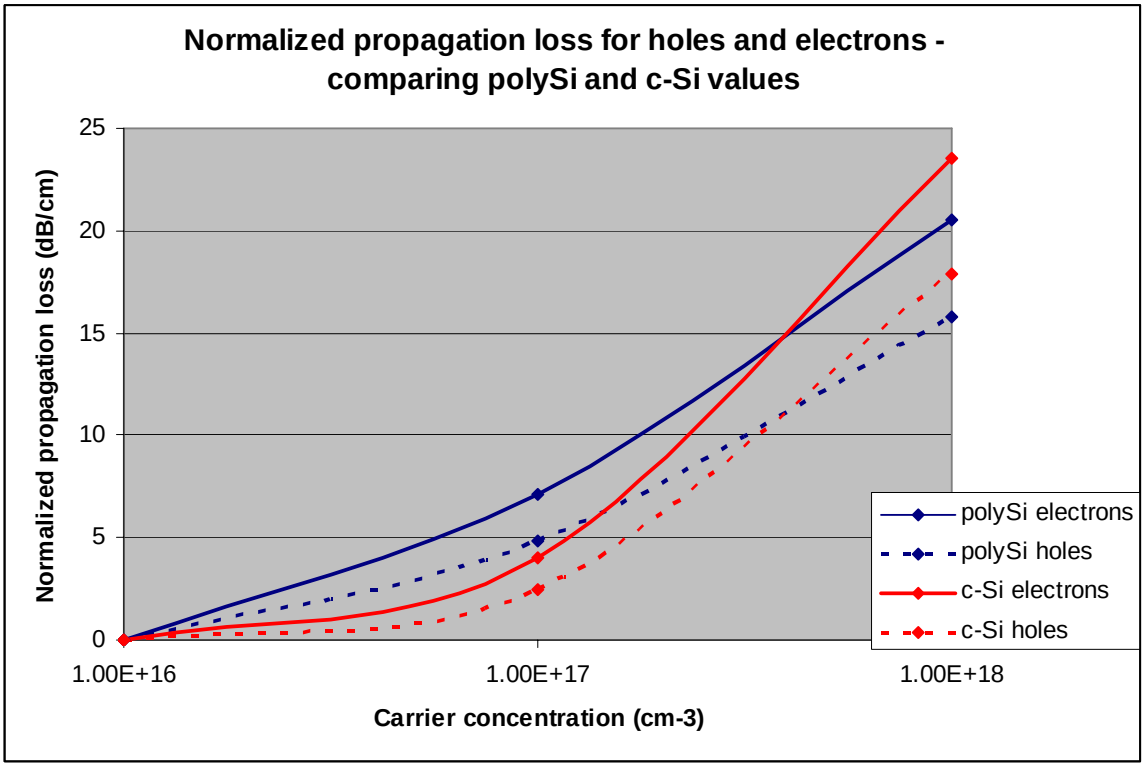

Fig. 5.15: Normalized propagation loss

Hall mobility measurements should be used in future work to help quantify the mobilities for each carrier concentration node.

The free carrier absorption was calculated by subtracting the absorption of the undoped sample from the total absorption and the difference was assumed as the free carrier absorption. However additional factors might come into play – other than free

carriers - that could affect the absorption. For example, a post implant anneal was conducted on the device pieces after implantation to activate the dopants and repair implantation damage. This anneal might have grown the polycrystalline grains further or caused some other physical effect on the material or device structure. Further work done on this topic should take this into account and try to quantify the effects of the anneal on the waveguide structures themselves. This can be done by preparing the undoped sample and measuring the transmission and calculating the absorption both pre and post anneal. This difference can then be subtracted from the free carrier absorption to give a more definitive absorption value.

5.5 Summary

The test apparatus, test process and results have been illustrated in this chapter. Several methods used to prepare the facets and get optimize coupling were presented. Optical testing was successfully performed on the single-mode waveguide devices and the transmission, the absorption coefficient, free-carrier absorption and material waveguide loss for polycrystalline silicon were presented. A comparison was made between the absorption and loss data for polysilicon with that of crystalline silicon. The data obtained followed expected trends from literature. The conclusion that polycrystalline silicon has a higher absorption and transmission loss is quantified.

A simplified Drude's model equivalent equation for polysilicon is given as:

$\Delta\alpha = 10.79 \times 10^{-18} \Delta N + 7.47 \times 10^{-18} \Delta P$.

5.6 References

[1] R. A. Soref, B. R. Bennett, “Electrooptical Effects in Silicon” IEEE Journal of Quantum Electronics, Vol., QE-23, No. 1, 1987.

[2] T. Kamins, “Polycrystalline Silicon for Integrated Circuits and Displays”, 2nd ed. Kluwer, 1998.

[3] C. R. M. Grovenor, "Grain boundaries in semiconductors," J. Phys. C 18, 4079-4119 (1985).

[4] R.A. Soref, and B.R. Bennett, “Kramers-Kronig analysis of E-O switching in silicon,” SPIE Integr. Opt. Circuit Eng. 704, 32-37, 1986.

[5] Y.A. Vlasov, and S.J. McNab, “Losses in single-mode silicon-on-insulator strip waveguides and bends,” Opt. Express 12(8), 1622-1631, 2004.

Chapter 6

Conclusion

6.1 Summary

Photonic systems on silicon integrated chips offer an opportunity to solve the bandwidth and power limitations in microelectronic IC interconnects. The use of deposited polycrystalline silicon holds a lot of promise due to the flexibility it provides in the design of electronic and optical design on different film layers. It also possesses promising electrical and optical properties which can be improved on using advanced micro-fabrication techniques.

In this thesis the potential of polysilicon was reviewed. Single mode waveguide devices were fabricated on polysilicon at the RIT SMFL cleanroom. The devices were then tested at the *Lobozzo* Optics lab at the SMFL.

The polysilicon waveguides fabricated successfully coupled and guided infrared light. The transmission was measured over several lengths and the cut back method was used to determine the free carrier absorption and propagation losses of polysilicon at 1550 nm. The Drude model equivalent plots for polysilicon was calculated and compared to that of crystalline silicon. A simplified absorption coefficient equation was derived for polysilicon. It was found to be 25.9% higher than that of crystalline silicon.

6.2 Improvements and future work

The polysilicon film performance is strongly influenced by the quality of the cleanroom fabrication processing undertaken. Several improvements in the processing should be considered to improve the performance of the polysilicon film.

Areas of equipment improvement are in the area of plasma etching of the waveguide ribs and the deposition of the initial amorphous silicon layer. Using a well-characterized modern etch tool will reduce the sidewall roughness and improve device performance significantly. The amorphous silicon layer problem was corrected in this thesis work – by using another LPCVD tool.

Additional processing improvements that can be undertaken include utilizing chemical mechanical polishing (CMP), remote electron cyclotron resonance (R-ECR) plasma hydrogenation to remove dangling bonds and replacing silicon dioxide with silicon-oxide-nitride to increase high index contrast even further. These steps have been known to reduce propagation loss by greater than 90% (in non-SPC polysilicon films).

Growing oxide on the silicon film and etching with Buffered Oxide Etch (BOE) can also help with the surface and sidewall roughness, reducing scattering. E-beam lithography could also be employed to improve sidewall roughness and to create smaller devices. Future work should also include the use of tapered waveguide ends on the device chips to allow for more efficient coupling and to reduce the insertion losses. To achieve this more advanced etching and dicing technologies are required.

Non-processing improvements that can be made for future works in this field could be to isolate the effect of the post implant anneal on the quantification of the free carrier absorption. This can be done by measuring the change in absorption losses for un-doped devices pre- and post-anneal. This value can then be subtracted from the calculated free carrier absorption to give a more definite representation of the effects of free carriers on the absorption coefficient.

Appendix

```
% Fred Ogah, Masters Thesis
% Drude model simulation - Polysilicon
% February 2010
% Microelectronic Engineering, RIT

e = 1.60217646e-19; % electron charge in coulombs
lambda = 1.550;   % wavelength um
c = 2.99792458e10;   % speed of light cm/s
epsilon_0 =8.854e-14; % permittivity of free space F/cm
n_0 = 3.48;         % refractive index of material
electron_mass = 9.10938188e-31; % electron mass Kg

%constant term
constant = (e^3*lambda^2)/(4*pi^2*c^3*epsilon_0*n_0);

% polysilicon
me_psi = 0.33*electron_mass;  % electron effective mass
mh_psi = 0.55*electron_mass;  % hole effective mass

uh_psi_16 = 40;               % hole mobility cm2/V.s
uh_psi_17 = 30;
uh_psi_18 = 15;

ue_psi_16 = 50;               % electron mobility cm2/V.s
ue_psi_17 = 40;
ue_psi_18 = 25;


% absorption cm-1
sigma_psi_holes_16 = (constant*((1/(mh_psi^2*uh_psi_16))))
sigma_psi_holes_17 = (constant*((1/(mh_psi^2*uh_psi_17))))
sigma_psi_holes_18 = (constant*((1/(mh_psi^2*uh_psi_18))))

sigma_psi_electrons_16 = (constant*((1/(me_psi^2*ue_psi_16))))
sigma_psi_electrons_17 = (constant*((1/(me_psi^2*ue_psi_17))))
sigma_psi_electrons_18 = (constant*((1/(me_psi^2*ue_psi_18))))
```