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Process development for integration of CoFeB/MgO-based magnetic tunnel junction (MTJ) device on silicon

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Process Development for Integration of CoFeB/MgO-based Magnetic Tunnel Junction (MTJ) Device on Silicon

by

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Abstract

Methods of communication and dissemination of information have changed dramatically with the emergence of the Internet and mobile phones. To sustain this revolution, we need reliable mass storage devices which would store information not only in large amount in small space but also for long time. Therefore, realizing high performance memory technologies is very critical for this revolution. This work contributes towards the development of one such technology; Magnetic Random Access Memory (MRAM) based on Magnetic Tunnel Junction (MTJ). The research conducted in this study is primarily focused on the process development for integrating MTJ on silicon. The film stack explored in this work is CoFeB/MgO-based. The relevant issues in this integration such as smooth bottom electrode preparation, low thermal budget, process chemistry and parameters, and MTJ patterning involving ion-milling have been addressed in this work. Ta and NiCr are evaluated as candidates for bottom electrode. Spin-on Glass (SOG)-based low temperature Inter Level Dielectric (ILD) process is developed. MTJ devices with varying sizes with four terminal contacts for on wafer testing have been designed and fabricated using the process developed. The devices exhibited Resistance-Area (RA) product in the range of 1-5 kΩ-μm^2. Recent literature on MgO-based MTJ devices has reported values in a range of 0.1 – 1000 kΩ-μm^2. This data confirms the electrical integrity of the MTJ fabricated. The RA values have been observed to be unchanged on application of magnetic field (+-300Oe). Detailed investigations have been carried out to find possible causes for the absence of magnetic response from these junctions. These include XRD analysis of the MTJ stack for CoFeB crystallization and STEM-PEELS studies to investigate the chemical

composition. “Néel coupling” or “Orange peel coupling” due to interface roughness is thought to be one of the main possible causes for magnetically inactive junctions. Suggestions for future are given on the basis of the results from the process and the experiments. In summary, a process has been developed for fabricating MTJ on silicon yielding desired values for junction resistivity. The magnetic response is extremely sensitive to film roughness at nanoscales and will require control of roughness at each step starting with wafer specification. It is concluded that with a control of surface roughness and recommended modifications in MTJ films, a CMOS compatible process for fabricating MTJ is plausible at RIT.

Dedicated to my parents,
Janardan and Anjali Pandharpure.

Acknowledgement

The success of this work is due to the able and inspiring support by Dr. Santosh Kurinec as advisor. I have learnt a lot during the course of this research because of her. Same thing is true for Dr. Rommel who has been behind me at every stage as a Master's student. I am thankful to him for this guidance. I am grateful to Dr. Feiming Bai for his expert support during the material science related research especially using advanced metrology techniques like XRD and AFM. I thank Dr. James Moon for being in my committee and providing valuable feedback on my work during discussions and thesis review.

This research was also possible due to the generous support of many collaborators. The deposition of MTJ stack was possible due to Dr. Chih-Ling Lee from Veeco Instruments, Fremont, CA and the patterning was done with the help from Ms. Katrina Rook from Veeco Instruments., Plainview, NY. I am deeply thankful to both of them for this support. I would express my gratitude to Mr. Swapnyl Shah and Mr. David McMahon from Micron Technology, Manassas, VA, for excellent STEM and PEELS analysis of the MTJ stack. It helped me getting insight into the stack. Electrical characterization of the stack was possible due to support from Dr. Jonathan Shu from CNS lab , Cornell University and Ms. Liesl Folks from Hitachi Global Storage Systems (HGST) in San Jose, CA. I am thankful to them for taking time in testing the devices.

This work was a team effort and the success of this work would not have been possible without help from my research group colleagues Sankha Mukherjee, SunWoo Lee, Archana Devasia, Stephen Sudirgo, David Pawlik and Raymond Krome. I really cannot imagine current stage of this research without them. I am also thankful to all of the friends from the graduate office for the joyful and fruitful environment in the office as well as in the lab and for the support they have given at the various stages of this project. The fabrication of the devices was done in Semiconductor and Microsystems Laboratory (SMFL) in RIT and I am grateful to SMFL staff: Scott Blondell, Thomas Grimsley, Richard Battlagia, Bruce Tolleson, David Yackoff, Sean O'Brien, and John Nash for providing excellent technical support related to the fabrication tools. The background for doing this research was prepared through coursework taken under faculty in Microelectronic Engineering department and I highly appreciate their guidance in the same.

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LIST OF ABBREVIATIONS

AFM	Atomic Force Microscopy
BEOL	Back End of Line
CMOS	Complementary Metal Oxide Semiconductor
DOS	Density of States
DRAM	Dynamic Random Access Memory
FM	Ferromagnetic
FTIR	Fourier Transform Infrared
GMR	Giant Magnetoresistance
HDD	Hard Disk Drive
ILD	Inter Level Dielectric
ILD	Inter Level Dielectric
JMR	Junction Magneto-Resistance
LTO	Low Temperature Oxide
MR	Magneto-Resistance
MRAM	Magnetic Random Access Memory
MTJ	Magnetic Tunnel Junction
NDR	Negative Differential Resistance
NMOS	N-channel Metal Oxide Semiconductor
PECVD	Plasma Enhanced Chemical Vapor Deposition
PEELS	Parallel Electron Energy Loss Spectroscopy
RA	Resistance Area Product
RBS	Rutherford Backscattering Spectroscopy

RIE	Reactive Ion Etch
RITD	Resonant Inter-band Tunnel Diode
SAF	Synthetic Antiferromagnetic
SIMS	Secondary Ion Mass Spectroscopy
SOG	Spin on Glass
SRAM	Static Random Access Memory
STEM	Scanning Tunneling Electron Micrograph
TEM.	Transmission Electron Micrograph
TMR	Tunneling Magneto Resistance
TMR	Tunneling Magneto-Resistance
TSRAM	Tunneling Static Random Access Memory
XRD	X-Ray Diffraction

Chapter 1

Introduction and Motivation

Information technology has revolutionized the way we live. The methods of communication and dissemination of knowledge have changed dramatically with tools such as the Internet and the mobile phones. To sustain this revolution, we need reliable mass storage devices which would store information not only in large amount in small space but also for long time. This information also should be readily accessible. Therefore, realizing high performance memory technologies is very critical to sustain this revolution. This work aims to contribute in the development of one such technology; Magnetic Random Access Memory (MRAM) based on Magnetic Tunnel Junction (MTJ).

1.1 Existing Memory Technologies: Historical Trend and Comparative Study

Various memory technologies have been developed to cater to different applications. These include Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM) and the recent Floating Gate Memory (Flash), very significant for its capacity augmented with non-volatility. Silicon-based Complementary Metal Oxide Semiconductor (CMOS) device technology has remained the backbone for developing these memories. The miniaturization in CMOS technology for the last 40 years guided by the famous Moore's scaling law [1] propelled these memory technologies in terms of capacity and speed. This is evident from the trend shown in Fig. 1.1 [2].

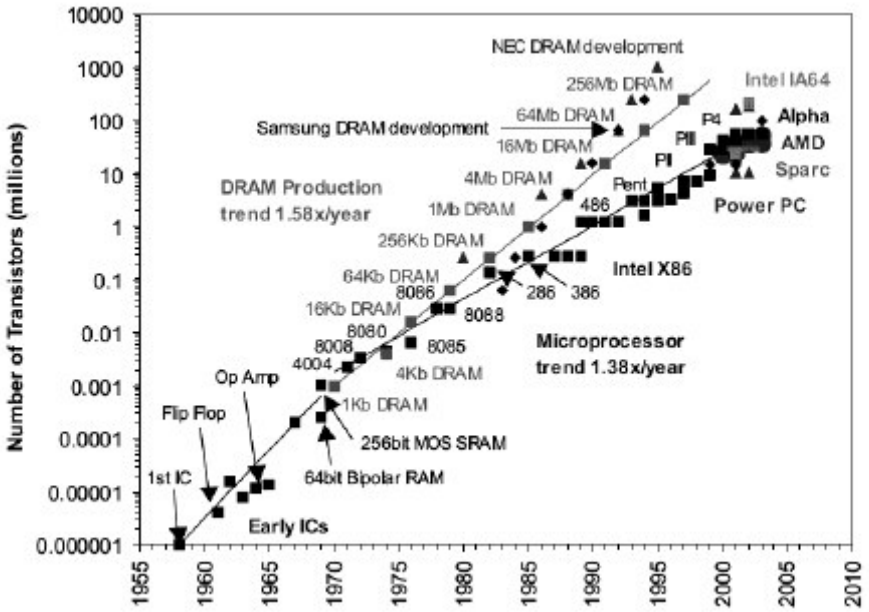


Fig. 1.1 Number of transistors over the years for various generations of DRAM and microprocessor technology [2]

This scaling trend in CMOS, although very effective, is not expected to go forever because of the limitations in getting the expected device performance at the sub 10 nm scale. [3]. There is a need to find an alternative way of achieving the same if not better performance. One of the ways is to use non-conventional device structures such as Resonant Interband Tunnel Diode (RITD), Magnetic Tunnel Junction (MTJ) or use of new materials which can undergo phase change after heating and essentially change the resistance. These structures provide high speed, low power consumption along with non-volatility (phase change and MTJ) and high density, the essential performance benchmarks for universal solid state memory technology.

RITD is based on quantum mechanical tunneling through a potential barrier while MTJ works on the principle of electron spin-dependent tunneling through an insulating barrier sandwiched between two ferromagnetic electrodes. In order to take complete

advantage of these structures and also to seamlessly adopt them with the trend in current silicon-based solid state memory technology, it is necessary to integrate these structures with mature silicon CMOS technology. The performance parameters of such memory architectures along with the conventional ones are shown in Table 1.1. [4].

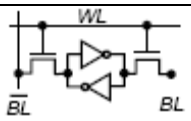
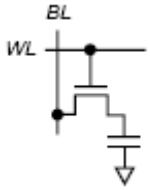
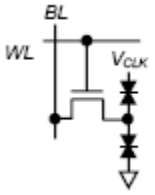
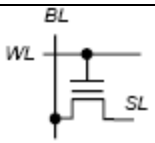
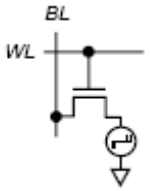
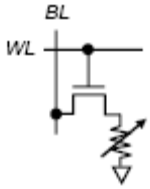
In order to fabricate these device structures in silicon-based platform, it is necessary to develop a robust process which preserves the integrity of these device structures. It is the purpose of this work to develop such a process for the integration of Magnetic Tunnel Junction (MTJ) on Silicon platform.

The challenges/issues related to this integration have been identified and addressed. These include exploration of bottom electrode for MTJ, Spin on Glass (SOG)-based low temperature Inter Level Dielectric (ILD), and patterning techniques for MTJ. The efforts in this work are focused towards finding reliable solutions to these issues. These solutions are assessed by two fold testing strategy. One is the process characterization at various levels and the other is the electrical testing of the fabricated devices.

Recently there has been considerable interest in MTJ based MRAM because of its promising characteristics exhibiting high non-volatility combined with high density and radiation hardness. The MTJ employed in this work consists of CoFeB/MgO/CoFeB sandwich. The chart in Fig 1.2 (Retried from Engineering Village, Elsevier Inc. 2006) shows the number of publications in MgO-based MTJ in the last seven years and the increasing trend is quite obvious. The literature is predominantly concentrated towards device design, characterization and optimization. Therefore, it is the author's opinion that

this work of developing a robust process on silicon-based platform would supplement these efforts effectively.

Table 1.1. Comparative study of various solid state memory technologies [Adopted from [4]]

Memory Technology	**Circuit Diagram**	**Read Time (ns)**	**W/E Time (ns)**	**Non-Volatile**	**Refresh**	**Cell Size (μm^2)**	**Voltage Supply (V)**
SRAM		0.4	0.4	No	No	Large 0.346	1.2
DRAM		<15	<15	No	Yes 64 ms	Small 0.048	2.5
TSRAM		<3	<3	No	No	Small	< 0.5
Flash		14	Slow 10^3 / 10^2	Yes	No	Small 0.169	12/2.5
Phase Change Memory (PCM)		60	50/120	Yes	No	Small 0.249	3
MRAM		<25	<25	Yes	No	Small	1.8

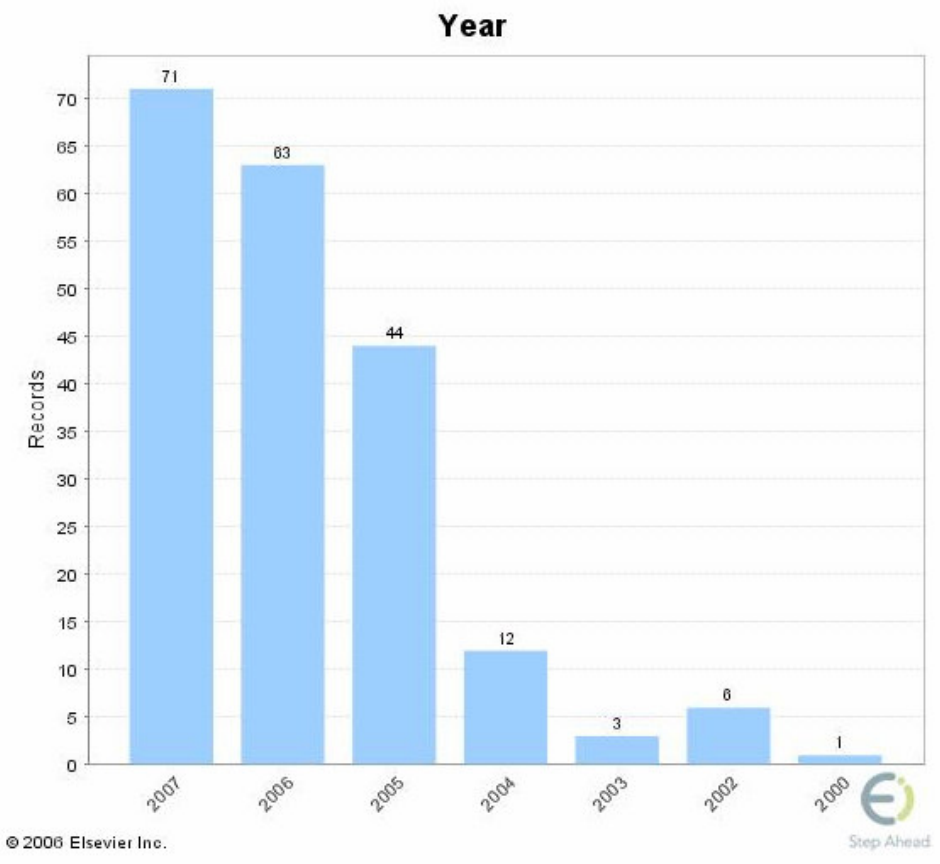


Fig. 1.2 Number of publication on MgO-based MTJ for the last seven years (Retrieved from Engineering Village, Elsevier Inc. 2006)

1.2 Organization of Thesis

Chapter 2 discusses the fundamentals of the spin-based electronics essential to the understanding of MTJ. *Chapter 3* covers the historical development of MTJ technology from its first demonstration to its current status. The process development efforts for integrating the MTJ device with silicon done in this work are covered in *Chapter 4.* The process characterizations performed during the development are presented in *Chapter 5* while the electrical characterization of the fabricated devices is discussed in *Chapter 6.* In the end, in *Chapter 7*, important conclusions from the work and its possible future direction are put forth.

Chapter 2

Spintronics and Magnetic Tunnel Junctions

The technology of *Spintronics* is based on magnetism. Before introducing *Spintronics* it would be appropriate to review the historical development of the understanding of magnetism.

2.1 A Brief Review of Magnetism and Magnetic Materials

Magnetism has been known to human beings since 600 BC when the ancient Greek philosopher Thales of Miletus noticed that the lodestones attract iron. The significant milestones in understanding magnetism and its employment in various technological applications are shown in Table 2.1. [5] [6].

Magnetism of a material is due to the orientation of the tiny magnetic dipoles or kernels in the material. The materials can be classified on the basis of the orientation of these kernels intrinsically in the material, their coupling with each other and their magnetic susceptibility; the way material gets magnetized when the external magnetic field is applied. Following are the categories of the materials,

1. Ferromagnetic
2. Paramagnetic
3. Diamagnetic
4. Ferrimagnetic
5. Antiferromagnetic

All these types are explained in Table 2.2 with their examples. The materials are both natural as well as synthesized and they range from basic elements to alloys and

Table 2.1 Significant milestones in Magnetism*

Time	Significance
600 BC	Greek philosopher Thales describes magnetic properties of lodestones (ferric ferrite)
1086	Chinese astronomer and mathematician Shen Kua reports the use of magnetic compasses for navigation
1600	English Physician William Gilbert publishes De Magnete in which he describes the Earth's magnetism
1819	Danish physicist and chemist Hans Christian Oersted discovers electromagnetism by observing deflection of the compass near current-carrying conductor
1831	English physicist and chemist Michael Faraday discovers electromagnetic induction
1845	Michael Faraday discovers diamagnetism
1856	**Magnetoresistance (MR) effect was first observed by William Thompson**
1881	Nikola Tesla conceives of utilizing alternating currents to produce a rotating magnetic field
1886	American electrician William Stanley develops transformer
1896	**Pieter Zeeman demonstrates that a magnetic field can split the spectral line of a light source into multiple components with different frequencies (the Zeeman effect)**
1907	**French physicist Pierre-Ernest Weiss develops a mean field theory to explain the behavior of iron and other ferromagnetic materials**
1922	**German physicists Otto Stern and Walther Gerlach demonstrate through the use of a molecular beam that the spatial orientation of atomic particles in a magnetic field is restricted (a concept termed space quantization).**
1925	**George Uhlenbeck and Samuel Goudsmit on the basis of Stern-Gerlach experiment postulate the concept of "electron spin" for the intrinsic quantized angular momentum associated with electron**
1934	German inventor Semi Joseph Begun constructs the first magnetic tape recorder used for broadcasting.
1936	**French physicist Louis Néel develops the concept of antiferromagnetism**

Table 2.1 Significant milestones in Magnetism (contd.)*

1941	Invention of ferrites, ceramic magnets with multiple applications in communication devices
1949	Magnetic core memory is introduced and enables a team of scientists and engineers at MIT to construct Whirlwind (completed in 1951), the world's first computer to operate in real time
1951	The first observation of magnetic domains by the Kerr effect is reported
1975	**Tunneling between ferromagnetic film was demonstrated by M. Julliere, basis of Tunneling Magneto Resistance (TMR) concept**
1980	German physicist Klaus Von Klitzing discovers quantum Hall effect
1988	**German and French physicists discover the giant magnetoresistance (GMR) effect, which results from electron-spin effects in artificial multilayers of magnetic materials: Beginning of the field of *Spintronics*, spin-based electronics**

* Milestones which are highlighted essentially developed the necessary foundation for the field of *Spintronics*

Table 2.2 Types of Magnetic Materials

Type	**Net Magnetic Moment\Ordering of Magnetic Dipoles**		**Example**
	Without Magnetic Field	**With Magnetic Field**	
Ferromagnetic	Parallel aligned	Large and positive	Fe, Co, Ni
Paramagnetic	Randomly oriented	Small and positive	Sn, Pt, Mn, O_2
Diamagnetic	No net magnetic moment	Small and negative (opposing)	Au, Cu, Bi, H_2
Ferrimagnetic	Aligned opposite but uncompensated	Large and Positive	Ba – ferrites ($BaO.Fe_2O_3$)
Antiferromagnetic	Aligned opposite but compensated	Large and Positive	Cr, PtMn, IrMn

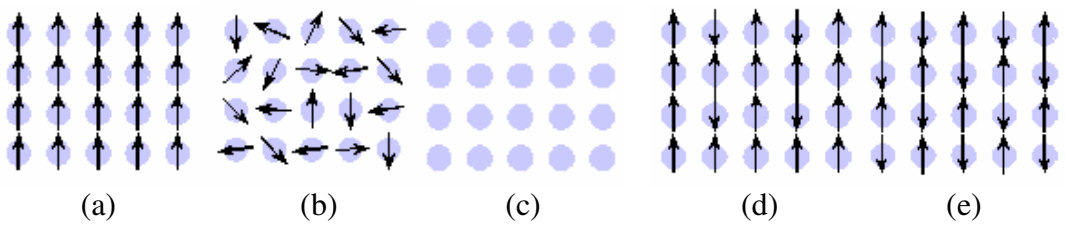


Fig. 2.1 Magnetic dipole orientation in various materials (a) Ferromagnetic (b) Paramagnetic (c) Diamagnetic (d) Ferrimagnetic (e) Antiferromagnetic [7]

compounds. Properties of these materials are optimized to get their best advantage for the given application. Fig. 2.1 shows the magnetic dipole orientations for these type.

2.1.2 Magnetization of Ferromagnetic Materials

The behavior of ferromagnetic materials under varying magnetic field is shown in Fig. 2.2.

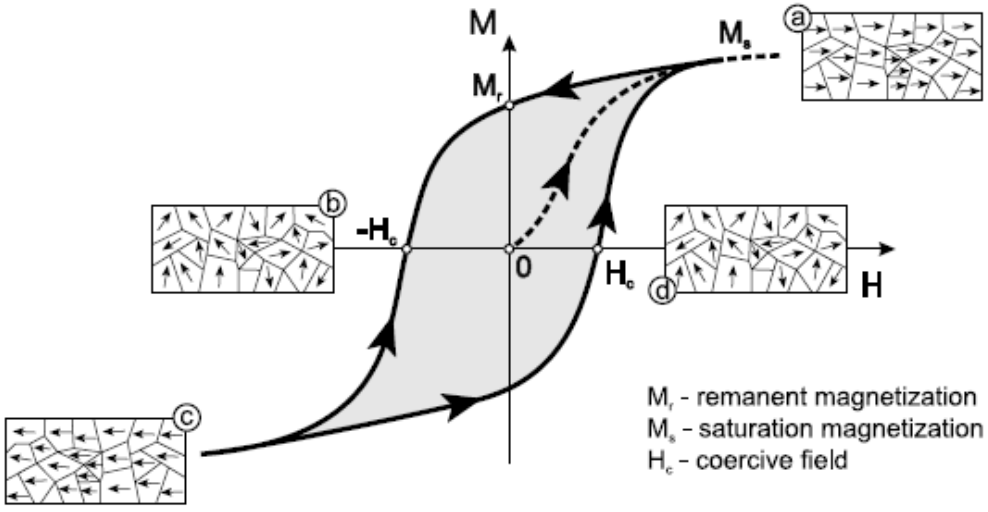


Fig 2.2 Magnetization of ferromagnetic materials (Hysteresis loop). [8]

When the external magnetic field is increased from zero, the material follows the magnetization non-linearly and reaches saturation. At this point all the magnetic domains are aligned to the direction of the applied magnetic field ("a" in Fig. 2.2). Driving external magnetic field to zero keeps some remnant magnetization in the material instead

of retracing the curve back to zero. This property of the material is exploited in memory applications. After the ferromagnetic material is completely saturated in either direction, the field we need to apply to demagnetize it is called the coercive field (H_C) or coercivity of that material ("b" and "d" in the curve). As a result, magnetization of the ferromagnetic material will trace a loop known as a hysteresis loop. The area of the hysteresis loop is related to the amount of energy dissipation after the reversal of the field. The shape of this loop is important when the material is used for various applications.

Narrow hysteresis loop is desirable in applications like transformer where energy dissipation due to magnetization reversal need to be minimized. A Large and square shape loop is desirable for memory applications since it retains a large fraction of the saturation field when the applied field is removed. This is pictorially shown in Fig. 2.3.

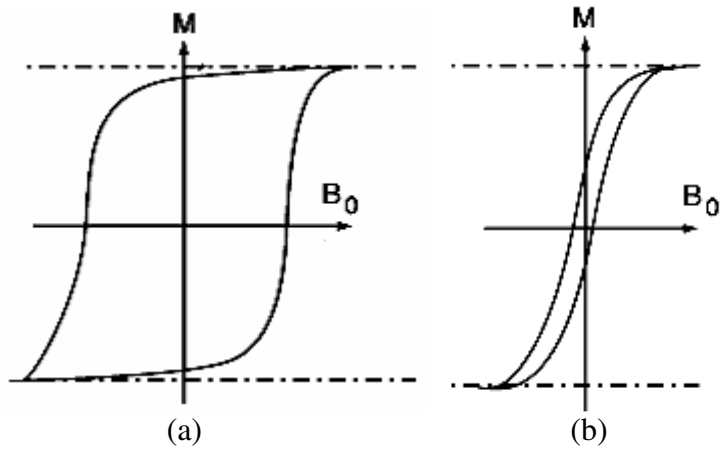


Fig. 2.3 (a) Large Hysteresis loop suitable for memory and recording applications
(b) Narrow Hysteresis loop suitable for transformer and motor applications [8]

On the foundation of this background in magnetism and ferromagnetic materials, the theory of *Spintronics* and engineering of *Magnetic Tunnel Junctions* is developed in the subsequent sections.

2.2 Introduction to Spintronics

The design and operation of any electron device is based on exploiting the properties of the electrons for controlling their transport. The properties which are considered here are

- Charge
- Spin

Conventional electronic devices like MOSFET and BJT are built by manipulating the charge effect of electron and applied electric field is the main parameter to control the transport. These devices are the building blocks of the advanced monolithic integrated electronic circuits in the digital as well as analog domain.

As mentioned in Chapter 1, charge based semiconductor devices have been the mainstay in the development of solid state memory technologies because of the several advantages these devices offer from the performance point of view, such as high density, high noise margin, and low power consumption. One of the desirable attributes of any memory is non-volatility. The solution in semiconductor technology is the floating gate or Flash memory. Though it combines the advantages of high capacity and non-volatility, its operating voltages are high and its degradation is fast [Refer to Table 1.1 in Chapter 1]. It also has long read and write times. When we think of devices based on novel materials having non-volatility as an intrinsic property, magnetic materials-based devices are the main candidates. The memory based on these devices would be superior to non-volatile semiconductor memory like Flash and it might give a strong alternative to magnetic mass storage systems like Hard Disk Drive (HDD).

Magnetism, at its fundamental level, is based on electron spin orientation and therefore its application in electronics is called *Spintronics*. So, unlike MOSFET and BJT, the devices in *Spintronics* are based on the spin manipulation of electron.

2.2.1 Concept of Electron Spin

Electron spin is the quantum mechanical property of the electron related to its intrinsic angular momentum. The concept of electron spin was first postulated in 1925 by Samuel A. Goudsmit and George E. Uhlenbeck on the basis of the Stern-Gerlach experiment in 1921[9] . The set-up of the experiment is shown in Fig 2.4 [10]. The silver atoms are directed through a non-uniform magnetic field and they are received on the photographic plate for detection. The electronic configuration of silver is 2,8,18,18,1 or [Kr] $4d^{10}$ $5s^{1}$. The single electron in the outermost orbit has zero orbital angular momentum ($l = 0$) and so it was expected that the silver atoms would show random/continuous distribution on the photographic plate. But as shown in the figure, the magnetic field separated the beam into two distinct parts indicating two possible magnetic moments for the electron. This was attributed to the intrinsic angular momentum associated with the electron with two possible states and following the pattern of quantized angular momentum, this angular momentum takes values $\pm 1/2$. Classically, an electron can be imagined as a spinning ball of charge with a current loop at its edge which generates the magnetic moment as shown in Fig. 2.5. This reasoning leads to the concept of “electron spin”.

The effective magnetic moment associated with an electron due to orbital angular momentum and intrinsic angular momentum (spin) is called Bohr magneton given by following relation,

$$\mu_B = -(e\hbar/mc)S \tag{2.1}$$

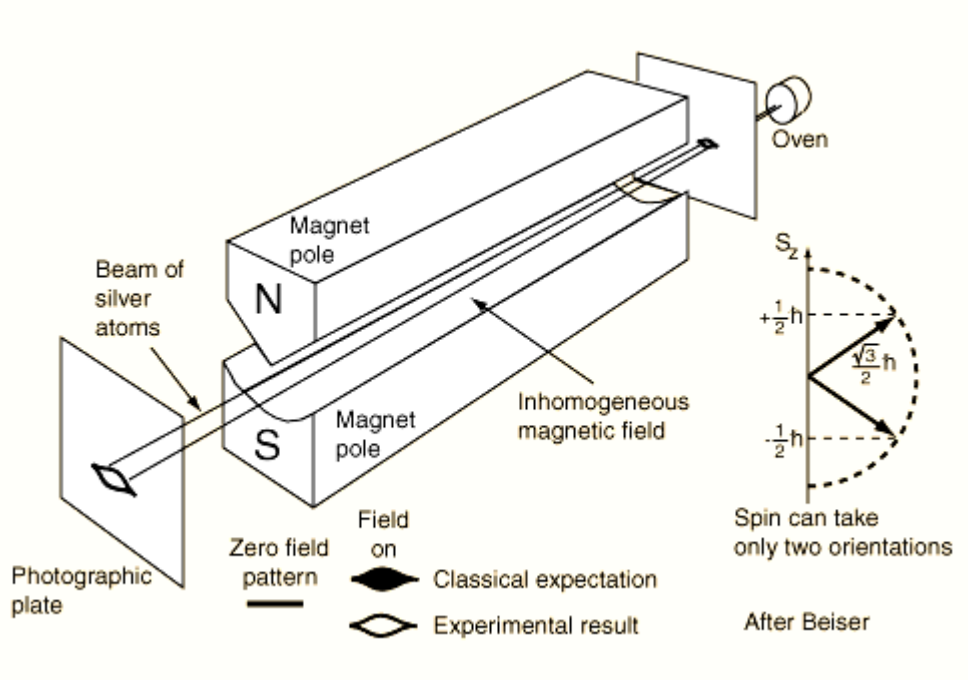


Fig. 2.4 Stern-Gerlach experiment [9]

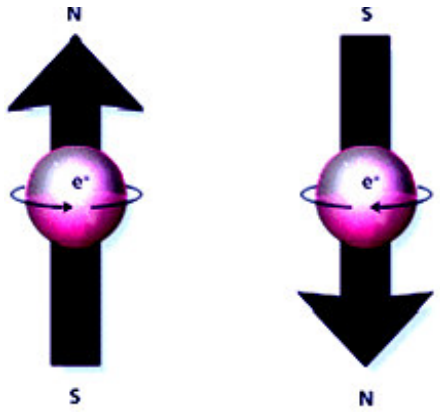


Fig. 2.5 "Electron Spin" and the corresponding induced magnetic moment [10]

μ_B = magnetic moment

m = mass of electron

c = speed of light

S = spin quantum number of electron, which can take values +1/2 and -1/2

2.2.2 Concept of Spin Polarized Current

Conduction in metals can be studied by considering their band structures and density of states (DOS) at the Fermi level which is fundamentally related to the electron configuration. Since the band and, in turn, DOS are split corresponding to two different spins of electrons, the conduction in metals should be studied by taking into account their magnetic properties.

2.2.2A Conduction in Non-Ferromagnetic Metals

All the metals except ferromagnetic metals fall in the category of non-magnetic metals. These metals have at least one partially filled *s* or *p* sub-shell. Examples of such metals are Copper ([Ar] $3d^{10}\ 4s^{1}$) or Tin ([Kr] $4d^{10}\ 5s^{2}\ 5p^{2}$). The conduction band is a free electron parabola as shown in Fig. 2.6 (a). The Fermi level cuts across this band symmetrically, resulting in equal densities of spin up and spin down electron states at the Fermi level.

Conduction is proportional to the DOS at the Fermi level,

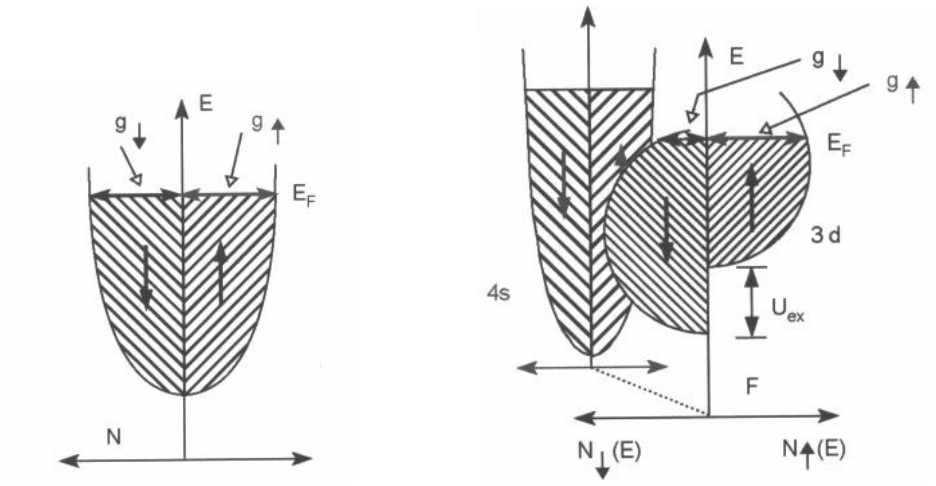
$$g \propto N(E_F) \tag{2.2}$$

Considering conductance for spin up and spin down electrons with their corresponding DOS at Fermi level,

$$\text{(a) } g\downarrow \propto N\downarrow(E_F) \quad \text{(b) } g\uparrow \propto N\uparrow(E_F) \tag{2.3}$$

For non-ferromagnetic metals, density of states for spin up and spin down electrons are the same, $N\uparrow(E_F) = N\downarrow(E_F)$. As a result from Equation (2.3), $g\downarrow = g\uparrow$.

The conductance for spin up and spin down electrons is the same for non-ferromagnetic metals and there is no net spin-polarization to the current.



(a) (b)

Fig. 2.6 Energy band structure of (a) Non-ferromagnetic metals (b) Ferromagnetic metals [11]

2.2.2B Conduction in ferromagnetic metals

Iron, Cobalt and Nickel are naturally occurring ferromagnetic metals. The electronic configuration of all of them is shown in Table 2.3. These ferromagnetic metals have their 3d sub-shell partially filled and 4s sub-shell completely filled. As shown in Fig. 2.6 (b), while 4s is parabolic and symmetric, the 3d sub-shell is not. Fermi level cuts across all of these bands and as a result, the DOS at Fermi level is not the same for spin-up and spin-down electrons, $N\uparrow(E) \neq N\downarrow(E)$.

There are several consequences of this for these metals.

- There is a spontaneous magnetization in the ferromagnetic metals given by
$$M = \mu_B \int_0^\infty [N\downarrow(E) - N\uparrow(E)] f(E) dE \tag{2.4}$$
- Conductances are different for different spin electrons and in turn the electric currents carried by spin up and spin down electrons are not the same.
$$g\uparrow(E_F) \neq g\downarrow(E_F) \qquad J\uparrow \neq J\downarrow \tag{2.5}$$
- The carriers in ferromagnetic metal has net polarization P given by
$$P = (J\uparrow - J\downarrow) \Big/ (J\uparrow + J\downarrow) = (g\uparrow - g\downarrow) \Big/ (g\uparrow + g\downarrow) \neq 0 \tag{2.6}$$

As a result, there is a spin polarized current in ferromagnetic metals.

Table 2.3 Electronic Configuration of Iron, Cobalt and Nickel

Metal	Electronic Configuration
Iron	[Ar] $4s^2$ $3d^6$
Cobalt	[Ar] $4s^2$ $3d^7$
Nickel	[Ar] $4s^2$ $3d^8$

2.3 Magnetic Tunnel Junction (MTJ) Device Structure and Operation

Magnetic Tunnel Junction (MTJ) is formed by sandwiching an insulating barrier between two ferromagnetic films. The structure is shown in Fig. 2.7.

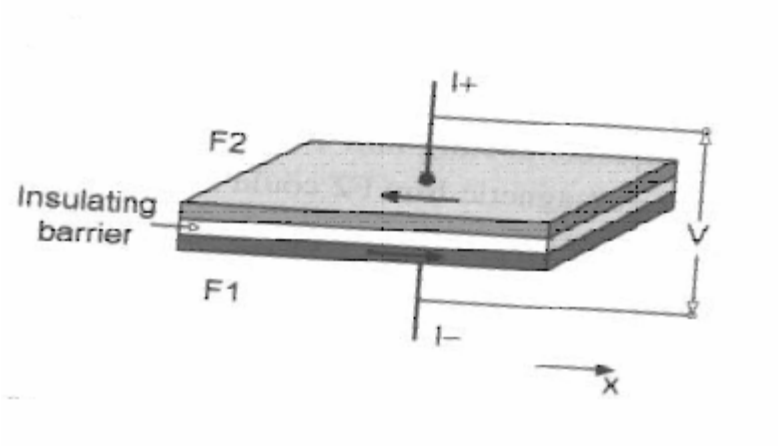


Fig. 2.7 Magnetic Tunnel Junction device structure. F1 and F2 are ferromagnetic films [11]

The structure is designed in such a way that the magnetic coercivity for F1 and F2 are different. In other words, the switching field for one ferromagnetic film is different than the other. The one with lower value of the coercivity is called the “free” layer and the one with higher value is called the “fixed” or “pinned” layer. The typical overlap of the magnetization loop of both of these types of films is shown in Fig. 2.8. The insulating

material is chosen such that its interface with ferromagnetic material is smooth and the electron spin is conserved during tunneling.

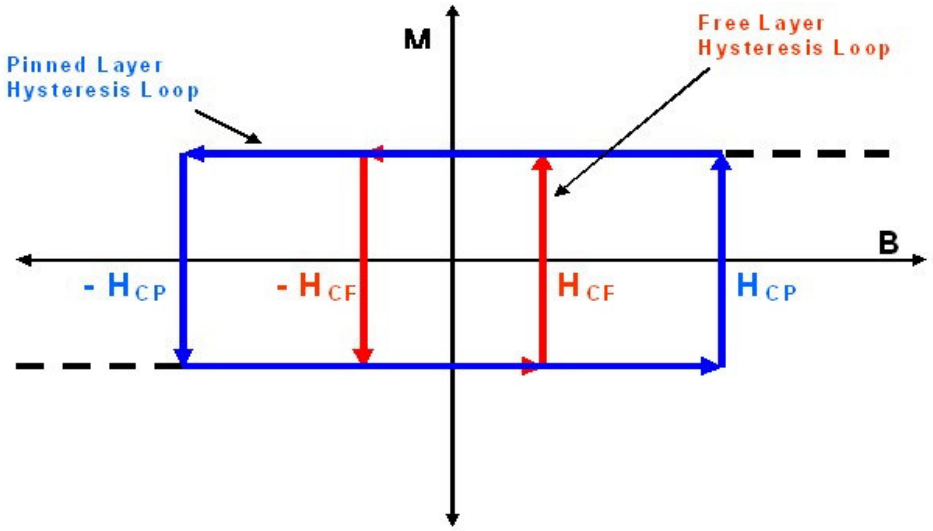


Fig. 2.8 Overlapping idealized hysteresis loops of free and pinned FM layers in MTJ device

After fixing the orientation of the "pinned layer", magnetic field (generally in plane of the films) is varied beyond "free layer" loop but within "pinned layer" loop. This is essentially to flip the orientation of the free layer and, in turn, make the two layers either parallel or anti-parallel with each other as shown in Fig. 2.9. The tunneling current probability through the tunneling barrier and, in turn, the barrier conductance changes during these two conditions and this is the basis of operation of the MTJ device.

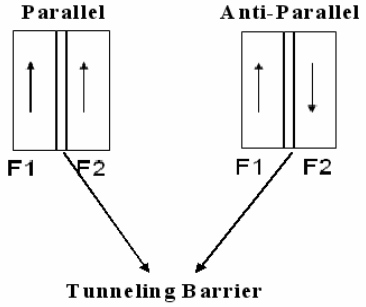


Fig. 2.9 Relative orientation of FM electrodes in MTJ Device

2.3.1 Theory of Spin Dependent Tunneling in MTJ Device

The tunneling current density in MTJ between the FM layers through the insulating barrier is first modeled by M. Julliere [12] in 1975. His model was based on the electrode polarization defined in Equation (2.6). By applying the same principles defined in Section 2.3 for spin polarized current, the tunneling current density through the barrier between the FM electrodes in MTJ device is proportional to the product of the DOS of the FM electrodes at the Fermi level (E_F),

$$J \propto N_{F1}(E_F)N_{F2}(E_F) \tag{2.7}$$

When electric potential is applied across the junction, spin up (down) electrons in one FM electrode can tunnel only to the available spin up (down) states in the other FM electrode.

When the magnetizations are parallel, the majority spin sub-band current density is higher since the corresponding DOS at E_F is higher for the electrodes. $J\uparrow >> J\downarrow$ and, in turn, $J_{parallel} \approx J\downarrow$.

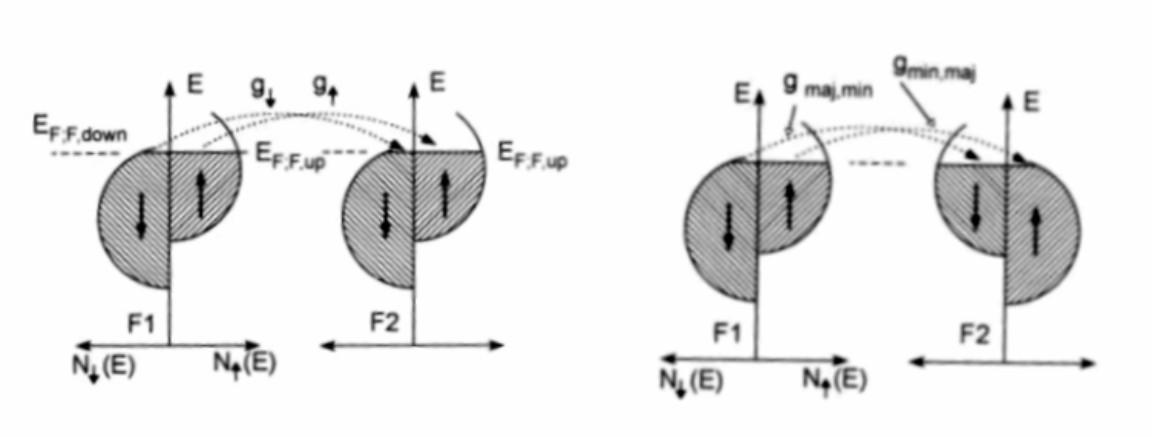
In brief, the tunnel conductance for the majority spin electrons is large and completely dominates the transport.

When the magnetizations are anti-parallel, up and down spin sub-band current densities are the same since corresponding conductances are equal. But the net tunneling current density is smaller as compared to the current when the magnetizations are parallel. For the anti-parallel case, $J\uparrow \propto N_{F1\uparrow}(E_F)N_{F2\uparrow}(E_F) \approx J\downarrow$

In summary, for MTJ device,

$$J_{antiparallel} = J\uparrow + J\downarrow < J_{parallel} \tag{2.8}$$

These two modes of operation for MTJ are shown in Fig. 2.10 for DOS point of view.



(a) (b)

Fig. 2.10 DOS perspective of spin dependent tunneling through MTJ (a) Parallel (b) Anti- parallel cases [11]

Although this model is simple and elegant, it has been long known [13] [14] that this model is inadequate and has limitations. This is due to the dependence of this model on FM electrode polarization which cannot be easily defined and quantified. While this model works for Fe as a FM electrode, it fails for Co and Ni after considering distribution of DOS in minority and majority sub-band [14]. Also, it does not explain completely the high spin-dependent tunneling through crystalline insulating barriers like Magnesium Oxide (MgO) recently under research for MTJ. Extensive theoretical efforts have been currently undertaken [15] [16] to understand and explain the performance of crystalline MTJ structures. For the current work, the Julliere model is used to define various performance parameters for MTJ. In order to correctly model the performance of the device, a more elaborate model would be required to predict the same parameters.

2.3.2 Performance Parameters of MTJ

MTJ is characterized by two different performance parameters. These parameters are based on tunneling junction resistance in parallel (R_P) and anti-parallel (R_{AP}) orientations of ferromagnetic films.

1. Specific Resistivity or Resistance-Area (RA) Product

It is defined as the product of the area of the tunnel junction and tunnel junction resistance

$$RA = (R_P \text{ or } R_{AP})\ x\ A \tag{2.9}$$

2. Tunneling Magneto-Resistance (TMR) and Junction Magneto-Resistance (JMR)

The fractional change in the tunneling conductance/resistance of an MTJ device for the two cases of orientations can be characterized by Magnetoresistive Ratio (MRR). It is defined in two different ways,

1. Tunneling MagnetoResistance (TMR)
2. Junction MagnetoResistance (JMR).

In an MTJ with FM electrodes having spin polarizations *P1* and *P2*, the TMR, according to Julliere model, is defined as,

$$TMR = \frac{2P1P2}{1 - P1P2} = \frac{R_{antiparallel} - R_{parallel}}{R_{parallel}} \tag{2.10}$$

Also, with the same model, JMR is defined as,

$$JMR = \frac{2P1P2}{1 + P1P2} = \frac{R_{antiparallel} - R_{parallel}}{R_{antiparallel}} \tag{2.11}$$

These parameters are especially used to define targets for MTJ-based MRAM.

Chapter 3

Historical Development of MTJ/MRAM Technology

Electron tunneling through thin insulating barriers at low temperatures was demonstrated for the first time by Giaver et al. [17] at GE Research lab in 1960. It was a Nobel-prize winning study that was conducted with superconductors and normal metals. This work was followed by Tedrow and Meservey at MIT in the 1970s [18]. They experimented with ferromagnetic metals instead of normal metals and suggested that the electron spin was conserved in the tunneling and the tunneling conductance is proportional to the spin polarization of the FM films. This was the first demonstration of the spin-dependent tunneling which was extensively referenced in the subsequent development of MTJ technology.

3.1 First Demonstration of Electron Tunneling between FM Films

Spin-dependent electron tunneling between two ferromagnetic films was first established by M. Julliere in 1975 [12] in Fe-Ge-Co tunnel junction. He studied the tunnel conductance variation due to parallel and anti-parallel magnetic alignments of the Fe and Co films as a function of junction voltage. The curve obtained is reproduced in Fig. 3.1. He observed 14 % TMR effect at very low voltages and T = 4.2 K.

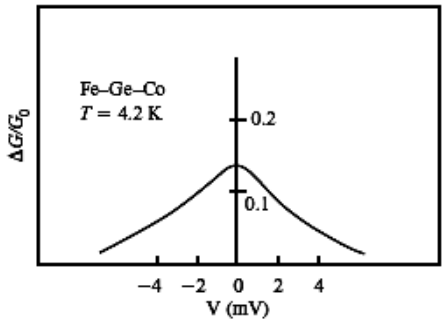


Fig. 3.1 First demonstration of spin-dependent tunneling through FM films [12]

Julliere expected the effect to be 26 % on the basis of work by Tedrow and Meservey. The fall off in the effect with few millivolts of applied voltage is attributed to spin-flip scattering during tunneling. As explained in Chapter 2, Julliere modeled his results on the basis of spin-polarization of FM electrodes and he calculated the relative change in conductance as

$$\frac{\Delta G}{G} = \frac{2P1P2}{1+P1P2} \tag{3.1}$$

where *P1* and *P2* are the spin polarizations of the FM electrodes.

3.2 Evolution of FM/I/FM Tunneling structures to the MTJ Device

The research on tunneling between thin FM films after the first demonstration by Julliere was slow due to many fabrication challenges in depositing the MTJ layers, especially the tunneling barriers.

Later, in the 1980s, Maekawa *et al*. [19] showed this effect in Ni-NiO-Co junctions. They were able to observe only 2 % of TMR at helium temperature. Further research on this device was not conducted due to difficulty in getting reasonable TMR useful for electronic applications.

The discovery of Giant Magnetoresistance (GMR) [20] in 1988 propelled the interest of the research community in investigating ultra-thin magnetic films. This peculiar magnetic phenomenon was observed with Fe/Cr/Fe ultra-thin super lattices in which the two Fe layers were coupled either in parallel or anti-parallel way. The large change in conductance, about 92 % at 4.2 K, was observed in these magnetic stacks depending on the coupling orientation. This work gave a new thrust to the research in FM/I/FM magnetic tunneling structures.

Aluminum oxide (Al_2O_3) as a tunneling barrier between ferromagnetic films was first explored in 1991 by Miyazaki and co-workers at Tohoku University. They reported NiFe/Al-Al_2O_3/Co junctions with TMR of 2.7 % at room temperature [21][22]. Various groups focused on getting artificial tunneling barriers of Al_2O_3 to improve on this value of TMR. In 1995, Miyazaki *et al.* experimenting with Fe- Al_2O_3-Fe got 18 % value while Moodera *et al* at MIT, working simultaneously, got 11.8 % for CoFe- Al_2O_3-Co junctions at room temperature[23][24]. Further advances in MTJ structures were enabled by improvement in growth and fabrication capabilities. With this, the TMR values with Al_2O_3 as barrier were increased more than 40 % [25]. The research in Al_2O_3 based MTJs focused on changes in the material used for free layer electrode have improved TMR values to 60 % [26], especially with CoFeB electrodes. The latest known TMR with Al_2O_3 as tunnel barrier with CoFeB as electrode is 70 % [27]. The TMR vs. Bias voltage curve for these junctions are shown in Fig. 3.2.

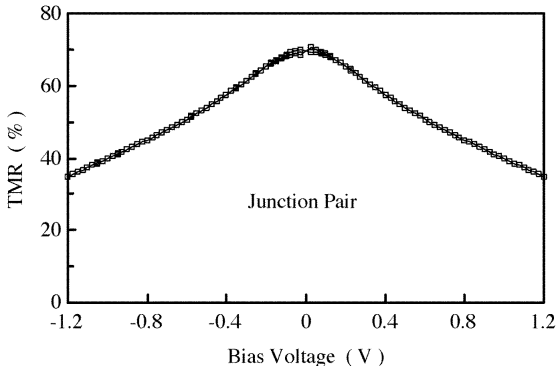


Fig. 3.2 TMR vs. Bias voltage curve for CoFeB-Al_2O_3 based MTJ device [27]

Interest in MgO as a potential tunnel barrier started with the theoretical predictions independently made in 2001 [15] [28] of getting very high TMR values with epitaxial Fe/MgO/Fe. Since then the investigation into this junction gave very high values of TMR at room temperature. Yuasa *et al.* observed the TMR of 180 % in 2004 for Fe-

MgO-Fe junctions [29]. The most promising electrode for MgO based MTJ devices has been found to be CoFeB. The values of TMR observed for CoFeB/MgO/CoFeB based MTJ at room temperature has shown an increasing trend with 230 % of TMR achieved by Djayaprawira *et al.* in 2005[30], 361% by Ikeda *et al.* [31][32] and in 2006, 472 % [33]. This is the highest TMR reported so far in the publications. The TMR versus temperature curve obtained in [33] is shown in Fig. 3.3. CoFeB/MgO/CoFeB MTJ structure is shown to give TMR more than 100 % for temperatures more than 300 ^{0} C [34]. It is important to note here that CoFeB as deposited is amorphous in nature and it is crystallized upon annealing at high temperature to get the epitaxial contact with MgO. This is very crucial in getting high TMR from this particular MTJ device. The details of this annealing process are explained in Chapter 4 in context of process development and integration.

The summary of the developments in MTJ device from Julliere to this work is given in Table 3.1 indicating junctions, their corresponding maximum TMR observed and the coercivity.

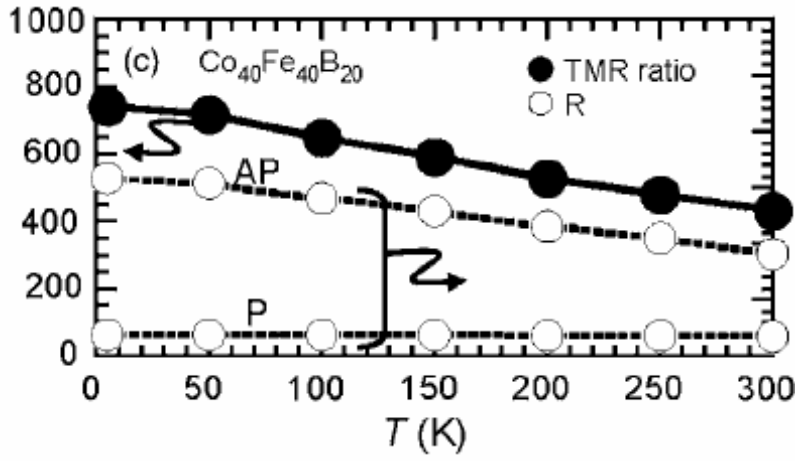


Fig. 3.3 TMR vs. Temperature in CoFeB/MgO/CoFeB MTJ devices [33]

Table 3.1 Development of Magnetic Tunnel Junctions

Device	TMR (%)	H_C (Oe)	Temperature	Reference
Fe/Ge/Fe	14	N/A	4.2	[12]
Ni/Ni-O/Co,Fe,Ni	2	N/A	4.2	[19]
NiFe/Al-Al_2O_3/Co	2.7	N/A	RT	[21][22]
Fe/Al-O/Fe	18	52	RT	[23]
CoFe/Al-O/Co	11.8	200	RT	[24]
CoFeB/Al-O/CoFeB	70	25	RT	[26]
Fe-MgO-Fe	180	25	RT	[29]
CoFeB/MgO/CoFeB	230	25	RT	[30]
CoFeB/MgO/CoFeB	472	25	RT	[33]

Fig. 3.2 shows the trend in TMR ratio for Al_2O_3 and MgO barriers over the years. [35]

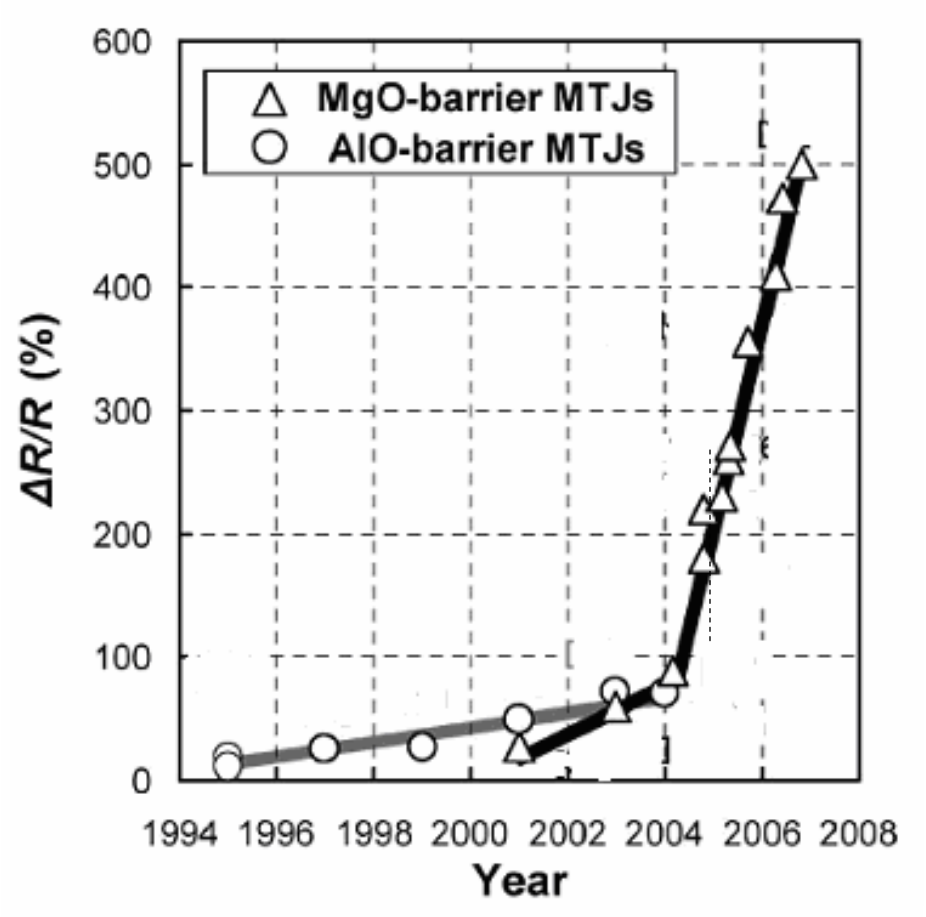


Fig. 3.4 Trend in TMR ratio for Al_2O_3 and MgO barriers [35]

3.3 Engineering MTJ Device structures

The response of the magnetic tunnel junctions needs to be engineered to make it beneficial for memory applications. Different such device structures developed are illustrated in Fig. 3.5. [36] Fig. 3.5 (a) shows the basic MTJ structure explained in Chapter 2. In principle, this structure can be used as memory as long as the coercivity of "reference layer" is higher than the "free layer" as is shown in Fig. 2.8 in Chapter 2. The low field excursions for changing just the "free layer" orientation would give the necessary switching operation of memory. The limitation of just having this structure is that these low field excursions might cause small domains in the high coercivity "reference layer" to permanently reverse in orientation, in turn degrading the performance of the device. [37]

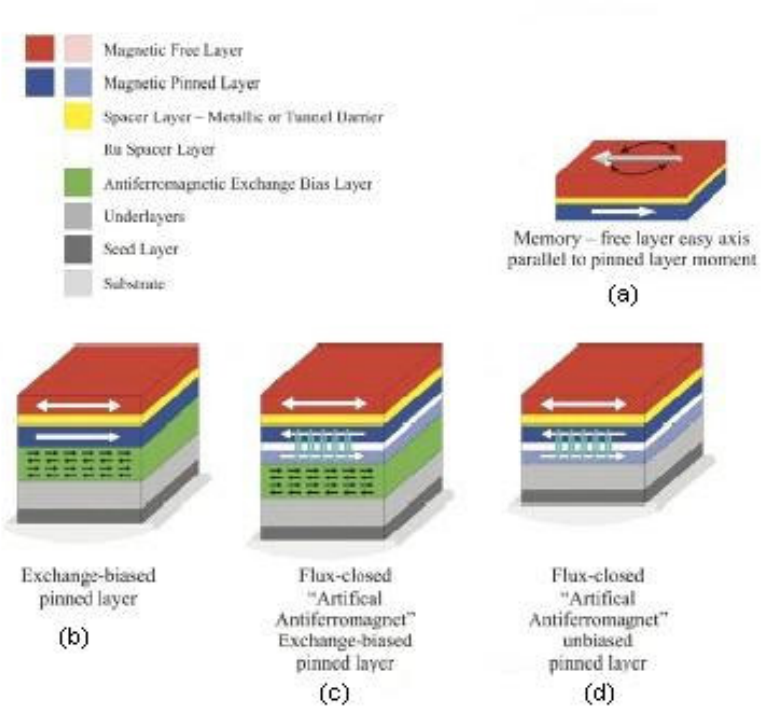


Fig. 3.5 Different MTJ Device Structures [Reproduced from [36]]

The reversal of the "reference layer" can be avoided by pinning the "reference layer" by exchange coupling to an adjacent antiferromagnet layer as shown in Fig. 3.5 (b). [38] The hysteresis loop for such exchange biased "reference layer" along with the "free layer" loop is shown in Fig. 3.6. For this coupling to be effective, the interface between reference layer and antiferromagnetic layer should be very smooth. During low field excursions, "free layer" hysteresis loop would be essentially traced. The problem with this structure is that while biasing "reference layer", there is non-zero magnetic bias on "free layer" as well which would affect the operation of the device during the absence of magnetic field.

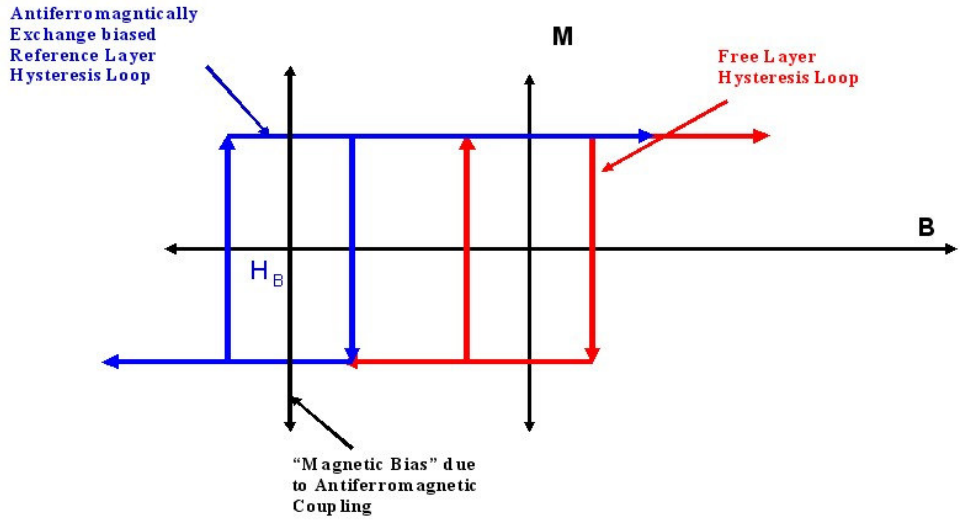


Fig. 3.6 Reference Layer and Free Layer hysteresis loop with exchanged bias coupling

The "reference layer" with no net magnetic bias can be produced by a concept called Synthetic Antiferromagnet (SAF). [39] It is a sandwich comprised of usually CoFe/Ru/CoFe layers with Ru thickness adjusted such that it exchange-couples the moments of the two ferromagnetic layers in opposite directions. This thickness is found

to be around 7-8 Å [39]. The structure with this type of SAF sandwich is shown in Fig. 3.5 (c).

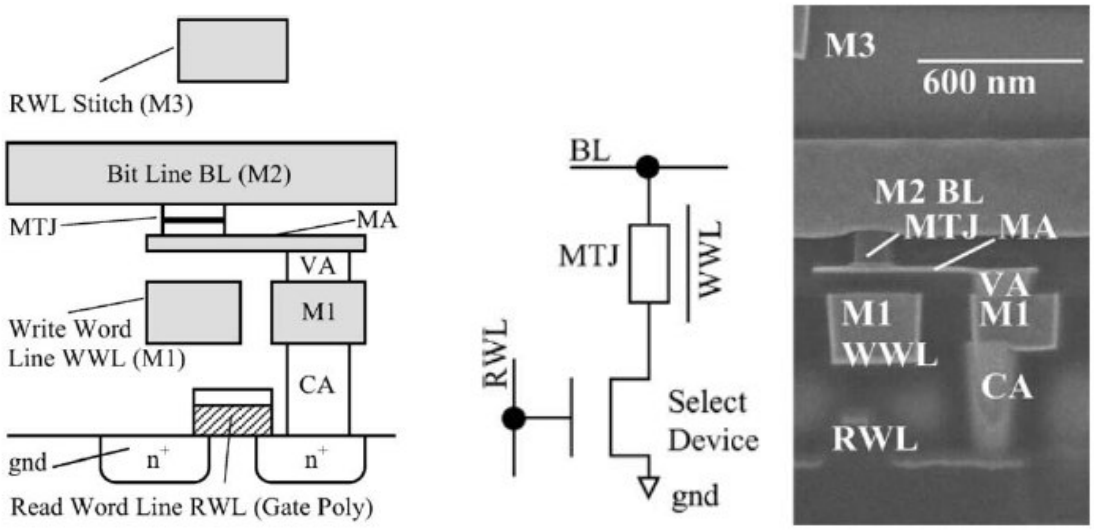
The research in such type of exchange biased structures initially employed FeMn as antiferromagnetic material. This material is antiferromagnetic when grown in a bias field on a magnetic seed layer but it is not stable during annealing. [40] IrMn used subsequently showed the stability up to ~ 230^0 C to 300^0 C [41]. High thermal endurance up to 400 ^{0} C was observed using PtMn as antiferromagnetic material. [42]

The structure in Fig. 3.5 (d) employs SAF sandwich but without exchange biasing by antiferromagnetic layer. The limitations due to the presence of antiferromagnetic layer are avoided in the structure. This type of structure is fabricated and tested in the current work.

3.4 Development of MTJ based Magnetic Random Access Memory (MRAM)

An MTJ changes its resistance depending upon change in magnetic orientation of the "free layer" with respect to "fixed" layer. In order to exploit this variation in resistance and build a memory cell which can be addressed with reliable read and write operation, we need switching elements. CMOS transistors or semiconductor diodes are various choices available for this purpose in order to read the MTJ state (resistance). These switching elements also isolate the MTJ device from the word line when that particular device is not addressed. The need of such switching elements is one of the main reasons why we need to integrate MTJ on a silicon-based platform. Fig. 3.7 shows such integration of NMOS transistor with MTJ to form 1T1MTJ MRAM cell. [43]

These cells are programmed by sending a pulsed current through word (WWL, M1) and bit (BL, M2) line. The intersecting currents would provide MTJ with "in plane" magnetic fields perpendicular to each which are termed "easy" and "hard" axis



(a) (b) (c)

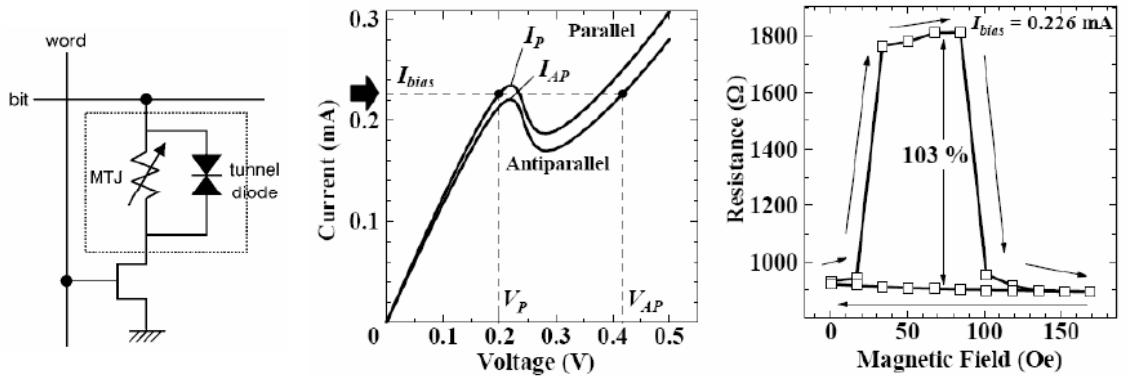
Fig. 3.7 1T1MTJ MRAM cell (a) Cell cross-section (b) Cell Schematic (c) SEM cross-section. [43]

fields. The whole system has to be engineered in such a way that the field from a single pulse on either line is not adequate to flip the orientation of the MTJ "free layer" but the combination of fields generated by these two lines is large enough for switching to occur. The programmed state can be read by the transistor using read line (RWL, Gate Poly, M3) connected to gate of the NMOS transistor.

Recent studies have showed a huge enhancement in TMR if MTJ is integrated with tunnel diodes. [44,45]. This is due to the non-linear characteristics of tunnel diodes with their negative differential resistance (NDR) characteristics. There are two possible

configurations which have been suggested in the studies; one with parallel MTJ-RITD connection [44] and the other with series connection [45].

The parallel configuration is shown in Fig. 3.8 (a). The MTJ acts as a shunt path and changes the total resistance of the parallel connection. For the given bias current (I_{Bias}) while reading from the cell by the access transistor below, the voltage across the parallel connection is affected by tunnel diode characteristics as shown in Fig. 3.8 (b). As a result, the change in the voltage between two conditions of MTJ is substantially large and it significantly enhances the TMR ratio. As shown in Fig. 3.8 (c), the TMR ratio has improved from 10 % to 103 %.



(a) (b) (c)

Fig. 3.8 MTJ-Tunnel diode integration: Parallel Connection (a) Schematic (b) I-V characteristics for FM layers in MTJ parallel and anti-parallel (c) Resistance vs magnetic field response [44]

The limitation of this circuit is that this enhancement is limited to very short range of operating current. Tunnel diode peak to valley current ratio is reduced due to MTJ which, in turn, can affect the whole circuit performance. In summary, tight control on the bias current, MTJ resistance and tunnel diode parameters are required to get the desired performance.

The alternative to this configuration is suggested by the same authors [2] in which tunnel diode is connected in series with MTJ. The schematic is shown in Fig. 3.9 (a). The change in magnetoresistance causes a shift in tunnel diode I-V characteristics as shown in Fig. 3.9 (b). The reported effective TMR due to this is 890% as shown in Fig. 3.9 (c). This is a substantial enhancement as compared to maximum TMR obtained so far with MTJ alone [472 % with MgO based MTJ [33]].

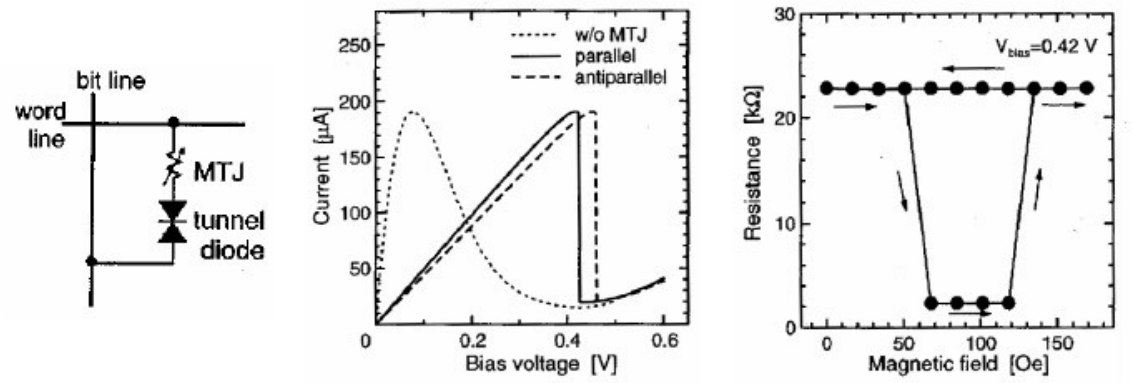


Fig. 3.9 MTJ-Tunnel diode integration: Series Connection (a) Schematic (b) I-V characteristics for FM layers in MTJ parallel and anti-parallel (c) Resistance vs magnetic field response [45]

The integration of MTJ with semiconductor devices is not only necessary but also beneficial for getting high-performance memory operation. The current work would concentrate on developing a robust integration strategy on a silicon-based platform.

Chapter 4

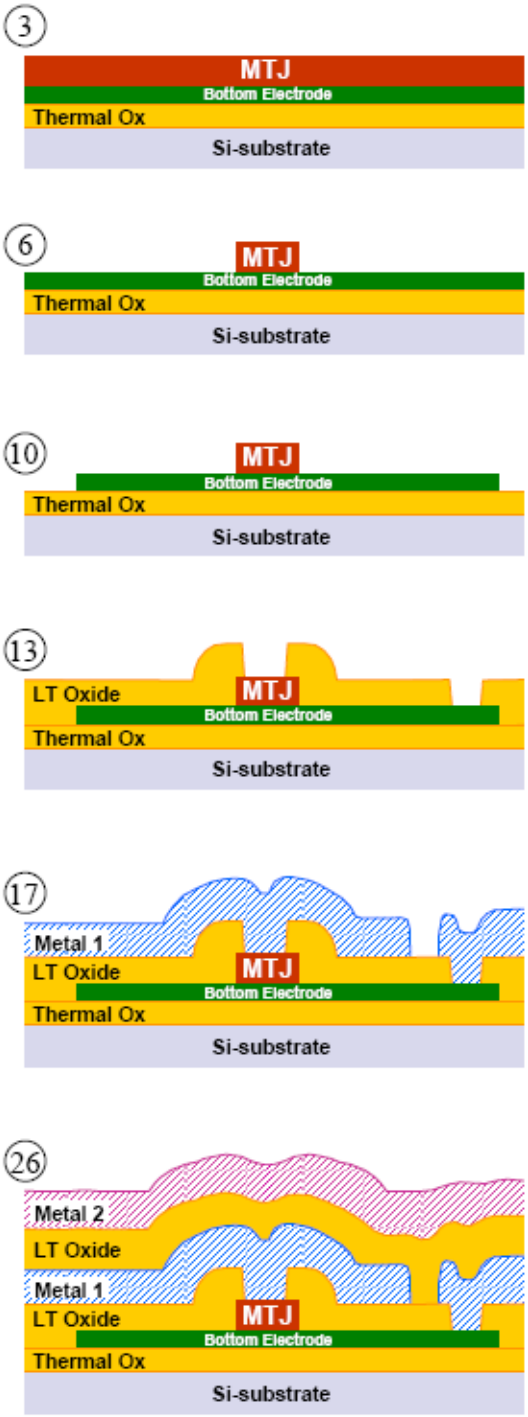
Integration of MTJ Device on Silicon Platform

The need and advantage of integrating MTJ device with semiconductor devices is explained in Chapter 3. There are various issues involved in this integration and also the fabrication of the device itself. It is the purpose of this chapter to cover these issues in detail and find the solution to some of them by designing various experiments and developing processes. In the current work, only the MTJ device is fabricated and integrated on silicon. The overall motivation of the project is to integrate MTJ with Si-based Resonant Interband Tunnel Diodes (RITD) developed previously at RIT [46] to get high TMR. The process developed in the present study is aimed as a foundation for this. However, it is the author's opinion that this process could be for other applications involving of MTJ devices on silicon.

4.1 Previously Designed Process Flow

The process developed previously is depicted in Fig. 4.1 [4]. It is a 6 level process. The mask design and layout for this process was done by Stephen Sudirgo. The layout and the cross section of a 40 μm x 40 μm device are shown in Fig. 4.2. The size of the devices range from 40 μm x 40 μm to 1 μm x 1 μm.

The process steps, apart from those not involving MTJ, are developed using the materials and chemistries used in a standard CMOS process. The steps related to MTJ such as deposition, etching, and pin-annealing are done in Veeco Instruments at Fremont, California and the other steps are executed in the RIT Semiconductor and Microsystems Fabrication Laboratory (SMFL).



1. Grow 500 nm thermal oxide.
2. Bottom electrode deposition: 200 nm of Al by sputtering.
3. MTJ Deposition
4. Field annealing

5. Litho 1: Mesa Definition
6. Mesa etch: ion milling stop at bottom electrode
7. Strip Photoresist
8. Preliminary Test

9. Litho 2: Bottom Electrode Definition
10. Etch Bottom Electrode: wet Al etchant
11. Strip photoresist using O_2 plasma
12. Deposit 300 nm PECVD oxide

13. Litho 3: Contact Cut Definition
14. Contact cut etch: wet HF/dry CHF_3
15. Strip photoresist using O_2 plasma
16. Deposit 200 nm Al via sputtering

17. Litho 4: Metal 1 Definition
18. Metal etch: Al we etchant
19. Strip photoresist using O_2 plasma
20. Deposit 300 nm PECVD oxide

21. Litho 5: Via Definition
22. Contact cut etch: wet HF/dry CHF_3
23. Strip photoresist using O_2 plasma
24. Deposit 200 nm Al via sputtering

25. Litho 6: Metal 2 Definition
26. Metal etch: Al we etchant
27. Strip photoresist using O_2 plasma
28. Field annealing
29. Electrical Test

Fig. 4.1 Previously Designed Process Flow for MTJ fabrication [4]

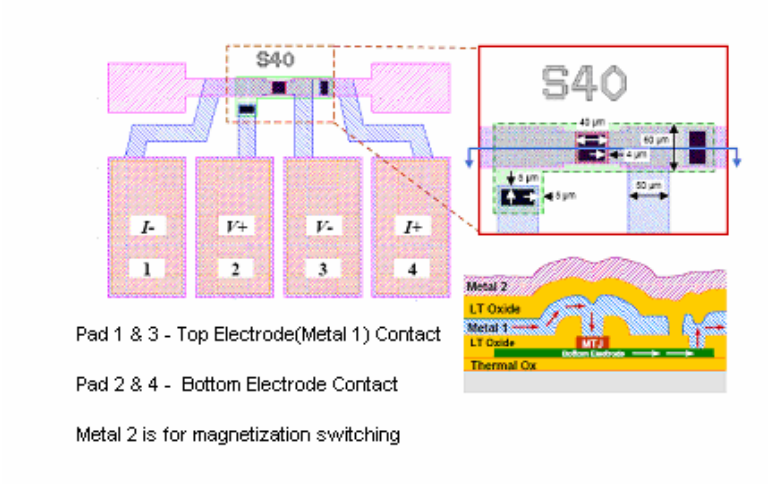


Fig. 4.2 MTJ Device Layout and Cross section [4]

The MTJ stack that is implemented in this process is shown in Fig. 4.3. The purpose of each layer in the MTJ stack is shown in Table 4.1. The MTJ device structure incorporates CoFeB/MgO/CoFeB MTJ stack with unbiased synthetic antiferromagnetic (SAF) sandwich (CoFe/Ru/CoFeB). The stack is capped with Ru along with NiFeCr magnetic buffer layer at the bottom.

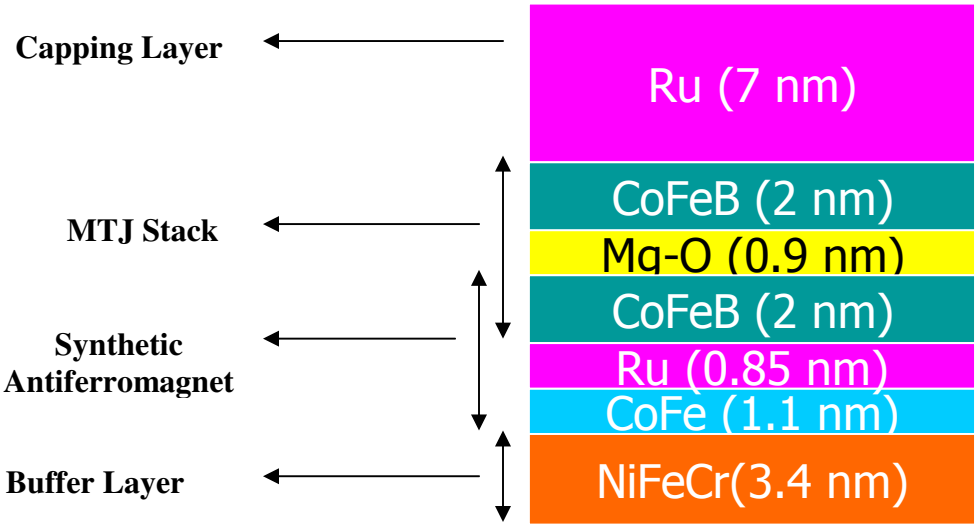


Fig. 4.3 MTJ Stack used in the process

Table 4.1 Purpose of different layers in MTJ stack

MTJ Stack Layers (From Bottom)	Purpose
NiFeCr	Magnetic buffer layer between bottom conduction/contact electrode and top magnetic layers especially SAF
CoFe	Bottom FM layer of the SAF sandwich. Magnetically oriented with annealing
Ru	Antiferromagnetic coupling layer to top FM layer (CoFeB) in SAF sandwich. Its thickness, 0.85 nm, is critical for the purpose of this coupling
CoFeB (Lower)	"Reference layer" in MTJ which is pinned using SAF coupling
MgO	Tunneling barrier in MTJ
CoFeB (Upper)	"Free layer" in MTJ; magnetic orientation of which is flipped in parallel or anti-parallel to the "Reference Layer"
Ru	Capping layer for protecting bottom MTJ layer from oxidation and degradation and as a means to connect to top contact electrode

The enlarged cross-section of the fully fabricated MTJ Device on silicon is shown in Fig. 4.4. Here the Al top electrode is corresponding to the "Metal 1" in the process shown in Fig. 4.1 [4]. The figure is not to scale.

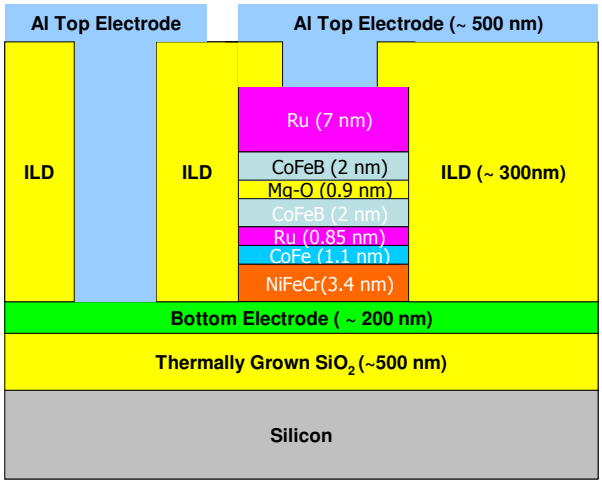


Fig. 4.4 Enlarged cross-section of the fully fabricated MTJ Device on silicon

In the previous attempt to fabricate this device on silicon, various problems were encountered [4].The author also identified some additional issues with the process as well as device design which have been tackled in this work. It is important to find solutions to these issues in order to fabricate this device in a reliable manner and get the expected performance. These problems along with their proposed solutions are covered in detail in the next section.

4.2 Challenges in Process Integration of MTJ Device on Silicon

There are a number of problems associated with the integration of MTJ device on silicon. There are several reasons behind this: one is that the MTJ stack layers are very thin (a few nm) and, therefore, to get the right metallic surface over which they are deposited is very important in getting the desired performance from them; the other reason is the thermal budget of the process which needs to be controlled since MTJ operation is intimately related to the thermal treatment. Also, MTJ structure, being mostly metallic, is prone to getting oxidized which would degrade its performance. The chemistry involved in the process should be carefully chosen in order to prevent this from happening. The specific challenges related to these requirements are covered in subsequent sections.

It is necessary to note here that the basic process flow designed by Dr. Sudirgo as shown in Fig. 4.1 is used for this study. The aspects of the process which are critical considering the constraints mentioned in the earlier paragraph are only considered and researched in the current efforts. The overall process flow with these modifications is in Table 4.11.

4.2.1 Bottom Conduction Electrode: Requirements and Solutions

Interface quality in MTJ stack layers especially at the tunnel oxide barrier interface is critical for getting required performance for various applications [47][48]. A high quality uniform tunnel oxide barrier is desirable in the multilayered MTJ stack for achieving high TMR, high breakdown voltage, good temperature stability, lower interlayer coupling field (H_{in}) between "free layer" and "pinned layer", and uniformity across the wafer. The interlayer coupling field is the shift in the "free layer" hysteresis loop by the effect of "pinned layer" field due to a phenomenon called "Néel coupling" or "orange peel coupling" [49] shown in Fig. 4.5 . It increases with rough tunnel oxide barrier, tends to make the "free layer" and "pinned layer" parallel to each other and degrades the MTJ performance. The interlayer coupling field is given by the following relation

$$H_{in} = \frac{\pi^2}{\sqrt{2}}\left(\frac{h^2}{\lambda \times t_f}\right) M_s \exp[-2\pi\sqrt{2}t_s / \lambda] \tag{4.1}$$

The tunnel barrier uniformity is dependent not only on deposition conditions for the tunnel barrier but also on the "pinned layer" surface roughness. This roughness can be reduced by two different ways:

1. Bombarding the "pinned layer" by ion clusters or ion beam before tunnel barrier formation; [50, 51]
2. Choosing appropriate seed layer materials [52].

The current work considers the second approach while developing the process.

When we consider seed layers on which the MTJ stack is deposited, the bottom conduction electrode plays a dominant role in deciding the interface quality of the MTJ stacks deposited on it. The current work undertakes material exploration for bottom

conduction electrode and develops a process for employing those materials in the process flow.

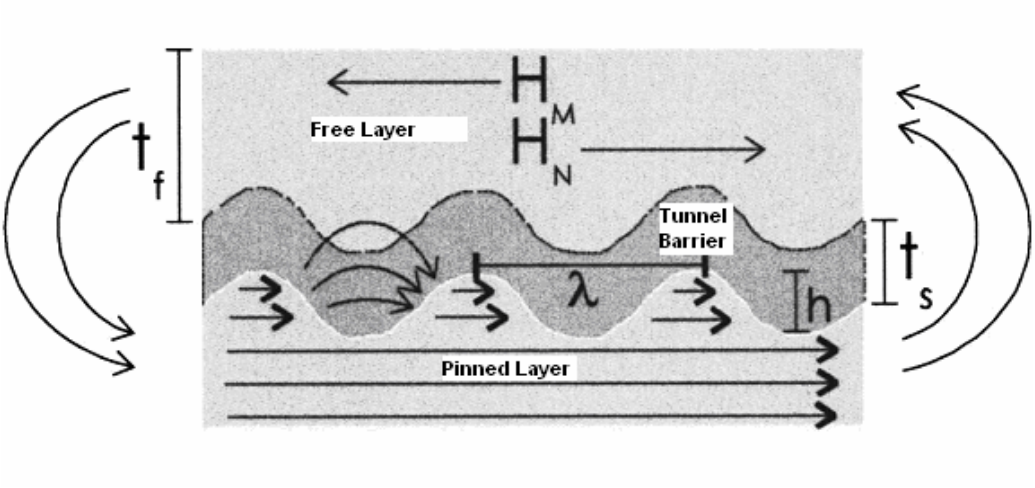


Fig. 4.5 Néel coupling between MTJ "free" and "pinned layer" due to interface roughness [49]

In the process flow developed initially [4], Al was used as a bottom conduction electrode. In fact research has been done [53] to assess the use of Al for this purpose. Though the results indicate some MTJ operation, it is not up to the requirements posed by memory industry in terms of TMR. This is mainly because of the undesirably rough Al surface and high grain size [54] especially in the thicker Al films.

The MTJ device stack layers have sub-10 nm thicknesses and the tunnel barrier thickness in the given design is 1 nm (MgO). Therefore, it puts stringent requirements on the surface morphology of the bottom electrode. In the current work, we decided to explore Ta and NiCr as bottom conduction electrode. Ta and TaN have been historically used as seed layers in the magnetic stacks because they assist the deposition of the thin magnetic films with their excellent surface properties. NiCr alloy, when used as a seed

layer, has shown to improve transport and magnetic properties of PtMn- based spin devices [55].

The deposition of the materials on thermally oxidized silicon wafer is done by means of sputtering process. The deposition parameters are shown in Table 4.2 with the deposition rates obtained using CVC 601 sputtering system in RIT SMFL laboratory. The deposition time is determined for getting ~200 nm of the bottom electrode. The thickness should be enough so that the bottom electrode can be used as an end point during MTJ patterning with ion-milling process without completely etching off the electrode. The 4" targets are used in the deposition process. The NiCr alloy target used in the process has Ni(80):Cr(20) composition.

Table 4.2 Deposition process parameters for NiCr and Ta

Deposition parameter	**NiCr**	**Ta**
Deposition power	300 W	250 W
Sputtering Pressure	3 mTorr	5.5 mTorr
Deposition Rate	165.9 Å/ min	85.7Å / min
Deposition Time	615 s	1680 s

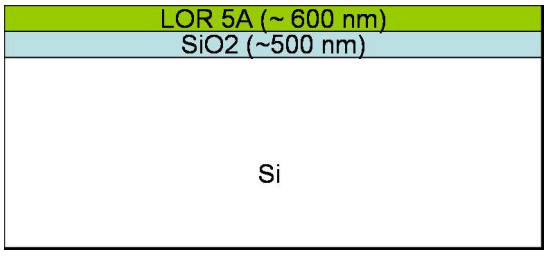
The patterning of these materials is done by developing and employing a lift-off process based on LOR 5A lift-off resist from MicroChem. The steps in the process with their brief description and parameters are shown in Table 4.3. Fig. 4.6 shows these steps with the cross sections. The typical snapshot of the undercut after the resist development step (step no. 4) is shown in Fig. 4.7. Both the bottom electrode materials, NiCr as well as Ta, are successfully patterned by the lift-of process

In addition to developing this process, NiCr alloy is studied in depth as a thin film for verifying its phase, composition and effect on its surface morphology due to

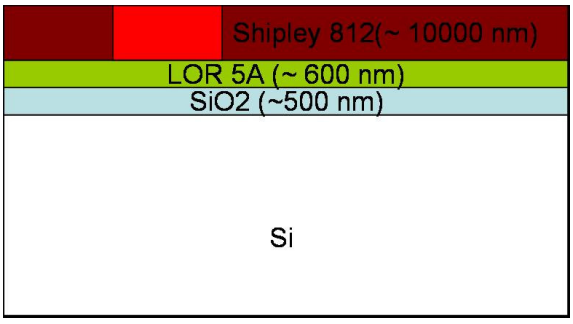
deposition conditions. The study is presented in the Chapter 5 and could be used as a template while researching on the seed layer materials for MTJ.

Table 4.3 Process steps in patterning the bottom conduction electrode using lift-off

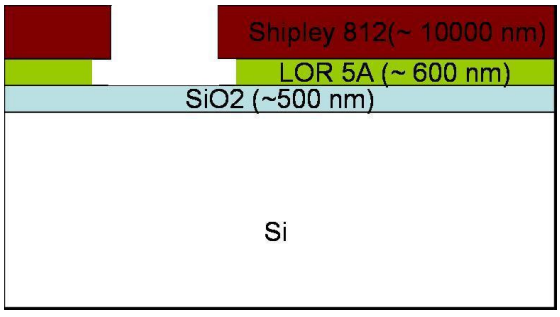
No.	Process Step	Description	Parameters
1	LOR 5A deposition	Coating liftoff resist for getting ~600 nm (3*bottom electrode) thickness	CEE100: 2000 RPM, 45 sec Spin Up: 500 R/S Spin Down: 3000 R/S Post coat bake: 150 °C, 1 min
2	Photoresist Coating	Lithography	SVG Track: 4500 RPM, 45 sec Post coat bake: 125 °C, 1 min
3	Exposure	Lithography	GCA Stepper Job: MTJ
4	Resist Development	Getting required undercuts for lift off process	CEE 100: CD 26 Developer Time: 130 sec
5	Bottom Electrode Deposition	Sputtering the bottom electrode material to get ~ 200 nm of thickness	CVC 601: Parameters given in Table 4.2 for NiCr and Ta
6	Metal Liftoff	Lifting off the Bottom electrode material to pattern it	Treatment with acetone and CD 26 or Nano Remover PG



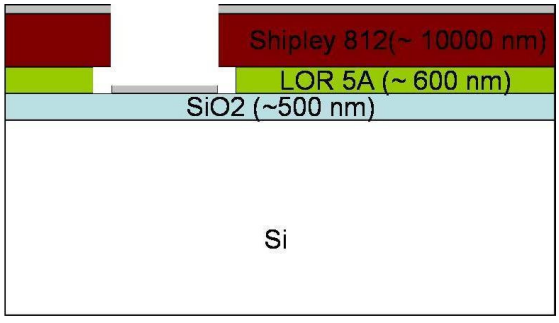
Step 1: LOR 5A Deposition



Step 2 & 3: Resist Coating and Exposure

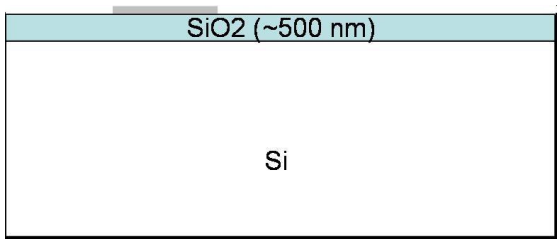


Step 4: Resist Development



Step 5: Bottom Electrode Deposition

Fig. 4.6 Liftoff process steps for patterning bottom conduction electrode



Step 6: Lift off using Acetone and CD 26

Fig. 4.6 Liftoff process steps for patterning bottom conduction electrode (contd.)

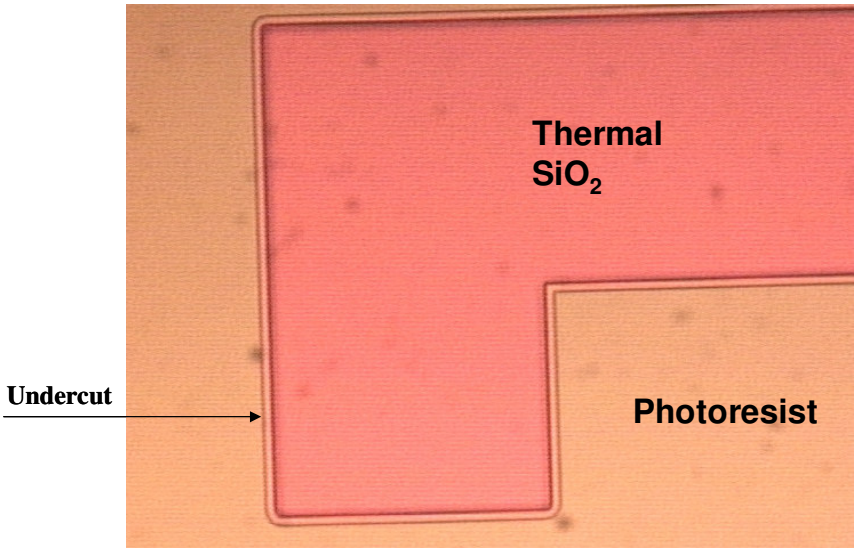


Fig. 4.7 Undercuts after the resist development in lift off process

4.2.2 Thermal Budget Requirements for Post MTJ Process Steps

Thermal endurance of MTJ device is lower than the typical temperatures at which the CMOS process is carried out. The thermal oxide growth at 900-1100 °C or annealing of the deposited oxide at around the same temperature range are some of the examples of the high temperature processing.

The Curie temperature is the temperature at which magnetic moments in ferromagnetic material become random. The Curie temperatures of basic ferromagnetic materials are shown in Table 4.4 [56]. Ferromagnetic CoFe “reference layer” in MTJ, if

already “pinned” should not be subjected to the temperatures beyond 400 °C which would otherwise degrade the MTJ performance.

There is another reason why the thermal budget of the process after MTJ deposition should be controlled below 400 °C. This is mainly applicable to CoFeB/MgO-based MTJ devices. MgO as deposited is polycrystalline in nature with preferential

Table 4.4 Curie temperatures of basic ferromagnetic materials

Material	**Curie Temperature (°C)**
Fe	770
Co	1115
Ni	354
$Co_{50}Fe_{50}$	1327

bcc (001) texture while CoFeB is amorphous. The annealing of these layers(CoFeB/MgO/CoFeB) at temperatures from 350° C to 450° C crystallizes the amorphous CoFeB to bcc (001) matched with MgO [57]. This gives high TMR in this MTJ due to the coherent tunneling at the interface with matched lattice structure. But it has been experimentally shown [58] that at still higher temperature annealing (beyond 400 °C) TMR is reduced. Fig. 4.8 [58] shows the dependence of TMR on annealing temperature for CoFeB/MgO/CoFeB. It should be noted here that this curve is dependent on the composition of CoFeB alloy and MgO thickness. This annealing and, in turn, crystallization of CoFeB layers for the MTJ fabricated in the current work is studied using XRD technique. This study is covered in detail in Chapter 5.

In conclusion, with MTJ on silicon substrate, we cannot execute a process at temperatures above 400 °C. For the given process, we set our limit to 350 °C as suggested by Veeco Inc.

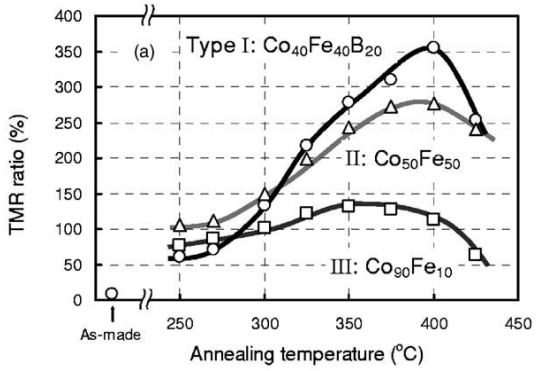


Fig. 4.8 Dependence of TMR CoFe(B)/MgO MTJ on annealing temperature [58]

In order to circumvent this limitation on thermal budget, integration of MTJ with silicon devices is done during Back End of Line (BEOL) process. However, at that level also the necessary inter level dielectric (ILD) process poses a challenge to the integration. The development of low temperature low-k ILD process is necessary and contribution due to the current efforts is presented in the next section.

4.2.3 Development of Low Temperature Low-k Inter Level Dielectric (ILD)

Usually the ILD is realized by Plasma Enhanced Chemical Vapor Deposition (PECVD) of TEOS at 390 °C or by Low Temperature Oxide (LTO) deposition at 600 °C followed by densification. Both are unsuitable given our limit at 350 °C.

According to the published literature, researchers have done the integration of MTJ by sputtering oxide as ILD. While it is certainly a good low temperature choice for integrating large size MTJs, it may not be suitable for high density applications requiring still lower k value.

Spin on Glass (SOG) is considered one of the promising candidates to be used as low-k dielectric [59] in sub 50-nm scale CMOS. In the current work, it is decided to explore SOG as an ILD and experiments are done to investigate its performance as low

temperature low-k dielectric. The SOG material chosen for this purpose is T-11 (311) from Honeywell Inc. The deposition process is developed for getting ~ 300 nm of thickness. The deposition and baking processes are given in Table 4.5. The process parameters are finalized after consulting with Honeywell application engineers. There are various curing techniques that can be employed for ILD and some of them are given in Table 4.6 with their relative merits and demerits.

Table 4.5 SOG deposition and baking process

No.	Process Step	Description	Parameters
1	SOG deposition	Coating on Silicon	3000 rpm, 1 min (SCS P6700 Spinner)
2	SOG baking	Removing solvents from the deposited SOG	80-150-250°C for 5 min each on hot plates

Table 4.6 SOG curing techniques [59]

Method	Advantages	Disadvantages
Thermal	Simple tooling, low cost	Long curing times, poor mechanical properties
E-beam	Fast cure, enhanced mechanical properties	Damage to FEOL, costly, too much demethylation, loss of hydrophobicity
UV/Laser	Fast cure, enhanced mechanical properties	

For a few wafers, we processed only up to baking (250 °C) and proceeded to the succeeding processing steps. The required annealing of the MTJ after the whole device fabrication was done at 355 °C for 2 hours in N_2, We faced a problem of Al film getting delaminating from the wafer due to SOG reflow/contraction at 355 °C. In order to avoid this problem, we decided to cure the baked SOG at 350 °C. The process developed is

shown in Table 4.7 and the corresponding temperature profile from the furnace (Bruce Furnace, Tube 2) is shown in Fig. 4.9.

Table 4.7 SOG curing process

No.	Process Step	Description	Parameters
1	Curing/Annealing SOG	Densifying/Reflowing SOG so that it withstands the field annealing process at the end of fabrication and improves its properties	350 °C, 1 hour, N_2 ambient. (Bruce Furnace: Tube 2, Recipe: shrini 350 C set up)

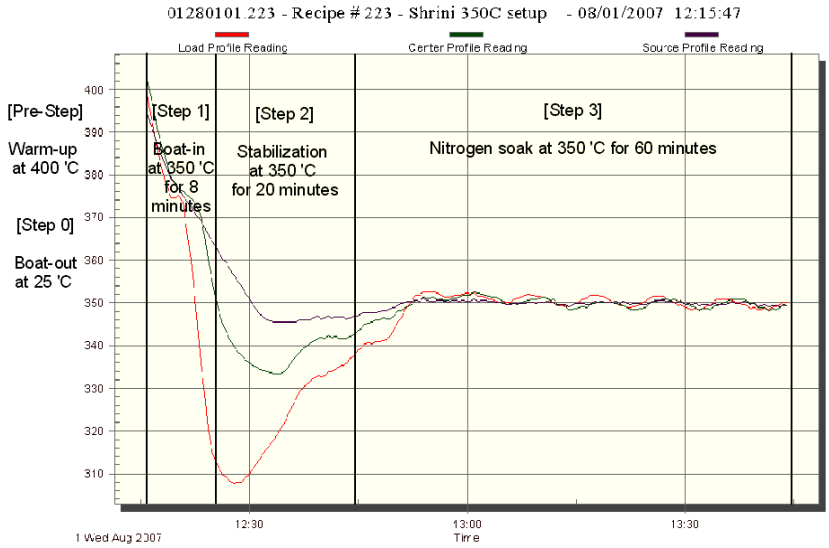


Fig. 4.9 Temperature profile from the furnace for the newly developed SOG curing process at 350 °C

Table 4.8 Steps in the furnace recipe for 350 °C curing of SOG.

Step no.	Description
	Warm Up to 400 °C
0	Boat Out (idle)
1	Boat In (8:45 mins) at 350 °C
2	Stabilization for 20 mins at 350 °C
4	Soak in N_2 for 1 Hour

The steps in the recipe to realize the temperature profile in Fig. 4.9 are shown in Table 4.8. The thickness reduction after curing compared to post-baking confirmed the densification of the glass as shown in Fig. 4.10. Fourier Transform Infrared (FTIR) spectroscopy measurement on the SOG film cured at 350 °C was done and it matches fairly with the one from Honeywell cured at 425 °C. The presence of the necessary Si-O bond along with Si-CH_3 is indicated in the FTIR plot shown in Fig. 4.11.

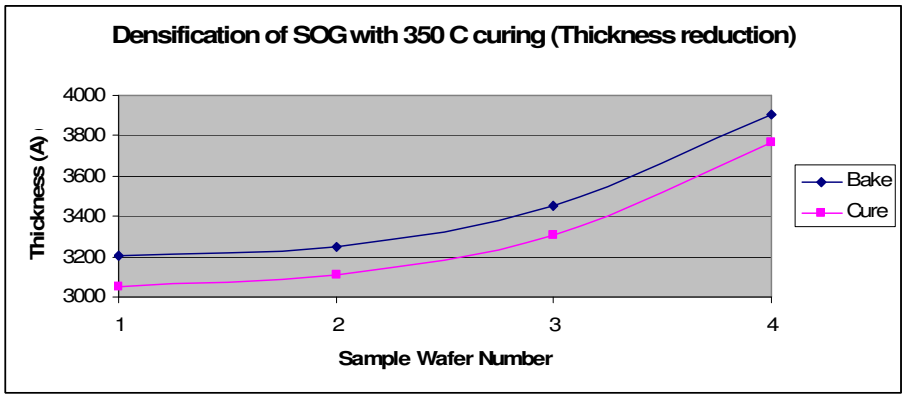
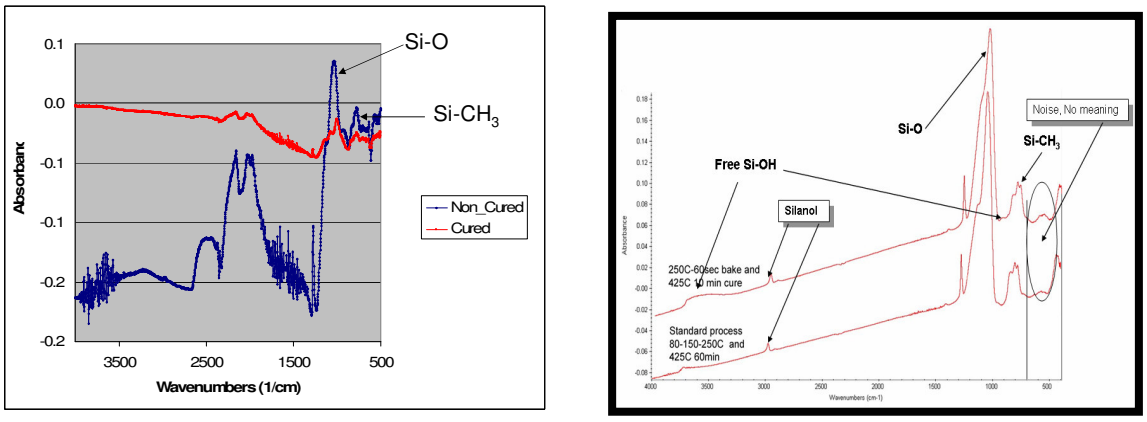


Fig. 4.10 Thickness reduction of SOG with curing confirming densification



(a) (b)

Fig. 4.11 FTIR plot of cured SOG film (a) Cured at 350 °C for 1 hour (In collaboration with Mr. Tim Woods (College of Science, RIT) (b) Cured at 425 °C for 1 hour (Courtesy: Honeywell Inc.)

The contact cut etch recipe for SOG is developed by using Reactive Ion Etch (RIE) based on CHF_3 chemistry for getting required anisotropy. The recipe parameters are given in Table 4.9. The blanket and patterned etch rates we got were ~1200 Å/min and 1000 Å/min, respectively. End point, in other words, etch time is decided essentially on the basis of this etch rate.

We conceived possible damage to the top Ru surface in MTJ stack in case of over etching during RIE due to the presence of Ar. This might cause some performance and yield issues since RIE is non-uniform over the wafer. The possible damage location is illustrated in Fig. 4.12.

Table 4.9 Contact cut etch recipe for SOG with RIE

Parameter	Set value
Power	140 W
CHF_3	65 sccm
O_2	5 sccm
Ar	65 sccm
Pressure	70 mTorr
Blanket etch rate – 1200 Å/min Patterned etch rate – 1000 Å/min	

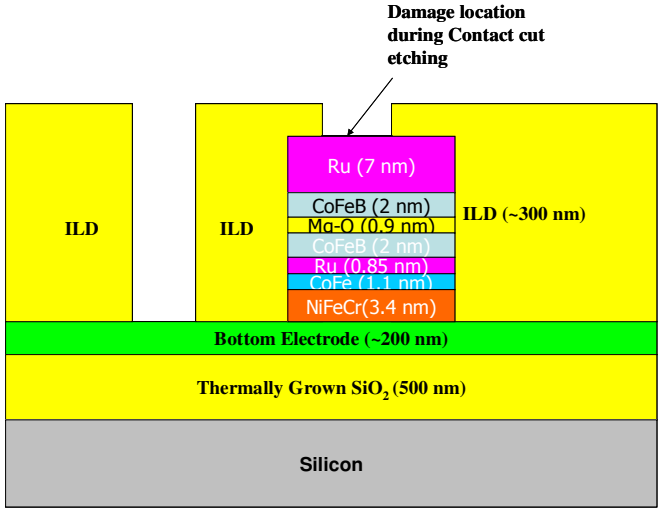


Fig. 4.12 Location of the damage during only dry over etch.

This possibility of damaging the top Ru surface is avoided by developing combination of dry-etch and wet-etch techniques. For dry partial etching, the chemistry in Table 4.9 is used while for wet etching 100:1 HF is used. The time for dry etch is decided so that there is remnant SOG of 500-1000 Å on top of Ru which is removed by dipping into 100:1 HF for 30 sec. This time for HF treatment is the conservative estimate after several controlled experiments on wafers in order to control the undercuts that would develop after the isotropic wet-etch.

The ILD process with the SOG is executed on three device wafers at a time with one monitor wafer. The SOG is kept out in room temperature for 1 hour and deposited on all the three wafers within 15 minutes. A monitor wafer is baked and cured in the same way as the device wafers. Etch time for contact cut etch with RIE is decided on the basis of the thickness measured on the monitor wafer. This procedure is followed for the whole lot by dividing it into sets containing three wafers each. This ensured the same SOG deposition and processing conditions for the wafers in the given set.

4.2.4 Low Power and Low Temperature Photoresist stripping process

The photoresist stripping is a necessary and recurring process in microelectronic fabrication. It is generally done by high power and highly reactive oxygen plasma by ashing the polymer resist. This process is not feasible in this fabrication involving MTJ not only because there is a probable heating of the substrate due to high power but also the possibility of oxidizing the metallic MTJ layers, in turn degrading their performance. The solvent strip with PRS-2000 resist stripper at 90 °C is the option but it cannot be

used when the resist is hardened. This happens in the current process during MTJ MESA etching with ion-milling when photo resist is used a mask as shown in Fig. 4.13.

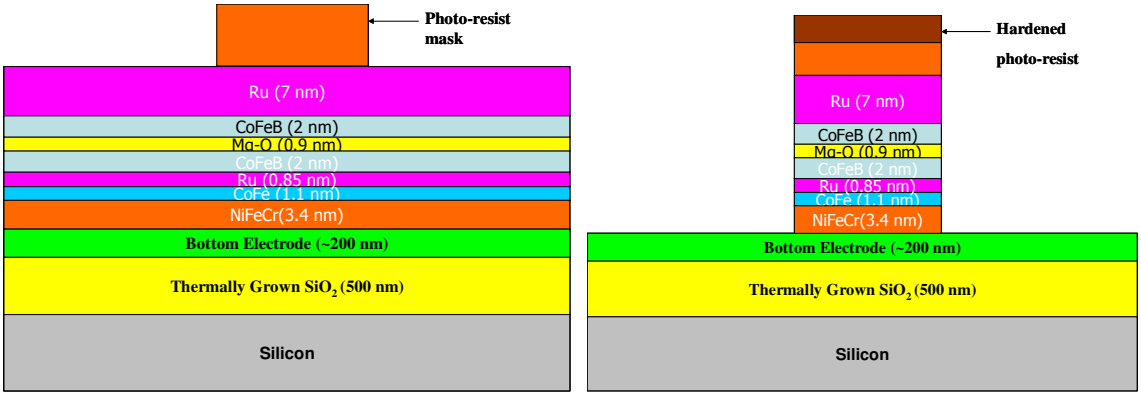


Fig. 4.13 MTJ etching with photo-resist mask (a) Before etching (b) After etching (Hardened resist)

A process is developed to strip this hardened photo-resist with low power low reactive oxygen plasma in RIE chamber. The process parameters are given in Table 4.10. Similar to contact cut etching, combination of dry etch and wet etch techniques are employed in this process to avoid damage to the top surface in the MTJ stack. Therefore, the etch time in RIE chamber is optimized only to strip the hardened resist while the rest is stripped by solvent stripper.

Table 4.10 Resist stripping process after MTJ MESA etching with ion-milling

No.	Process Step	Description	Parameters
1	Dry photo-resist strip	Removing hardened resist after MTJ MESA etching	Power: 150 W O_2: 30 sccm Pressure: 300 mTorr (Drytek Recipe: O2ASH) Time: 390 seconds
2	Solvent Strip	Removing remnant resist	PRS-2000 90 °C 5 mins (dirty) 5 mins (clean) 5 mins DI water rinse followed by SRD

4.2.5 Patterning MTJ: Ion-milling process

MTJ film stacks are patterned by ion-milling process by Veeco Process Equipment Group based in Plainview, NY. The tool used is Nexus IBE located at the Plainview facility. The wafers are mounted on 5 inch AlTiC pucks using Kapton tape and the processing is done using Ar ion beam. Schematic of the Nexus IBE system is shown in Fig. 4.14.

The process needs to be optimized for getting steep side walls for MESA and less re-deposition at the bottom and there is a trade-off between these two aspects. The normally incident ion beam gives steeper side wall angles but more re-deposition. Etching away from the normal incidence gives shallower sidewall angles but less re-deposition. The situations during these two conditions for an arbitrary film are illustrated in Fig. 4.15 [60].

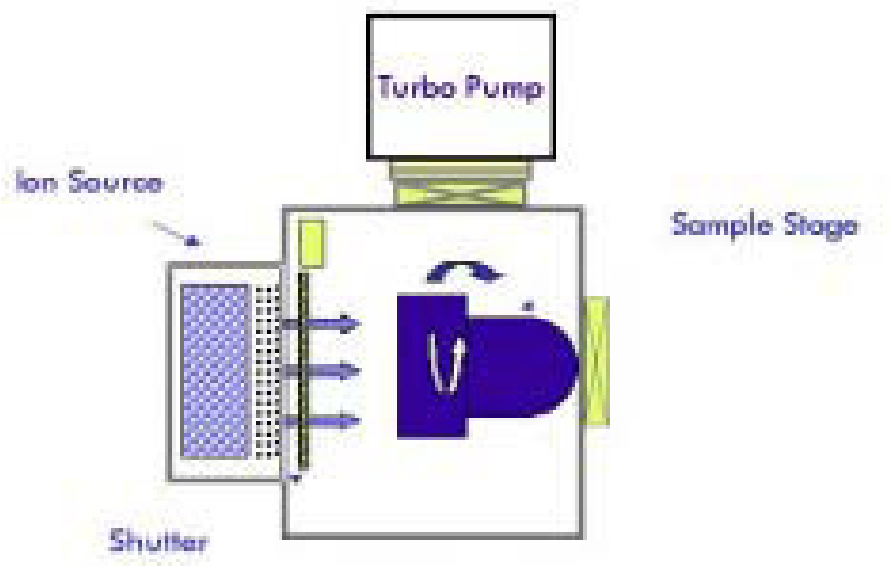
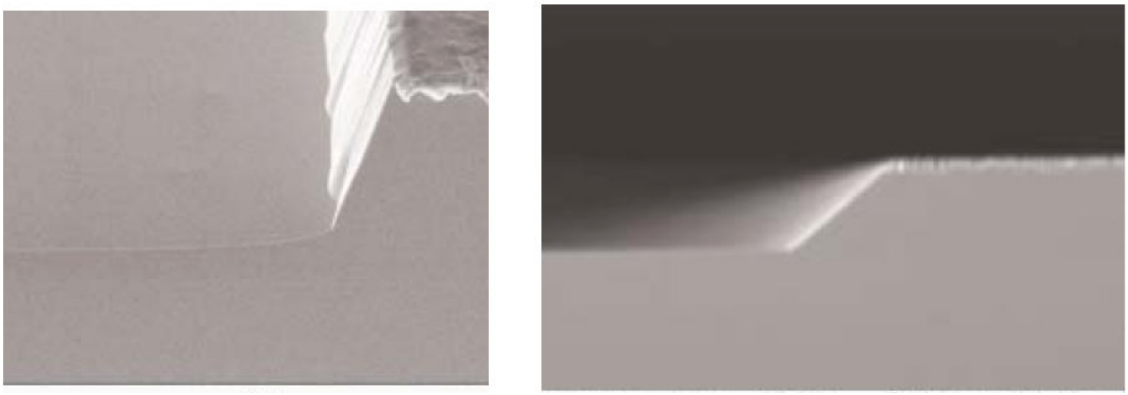


Fig. 4.14 Schematic of Nexus IBE system by Veeco Instruments [60]



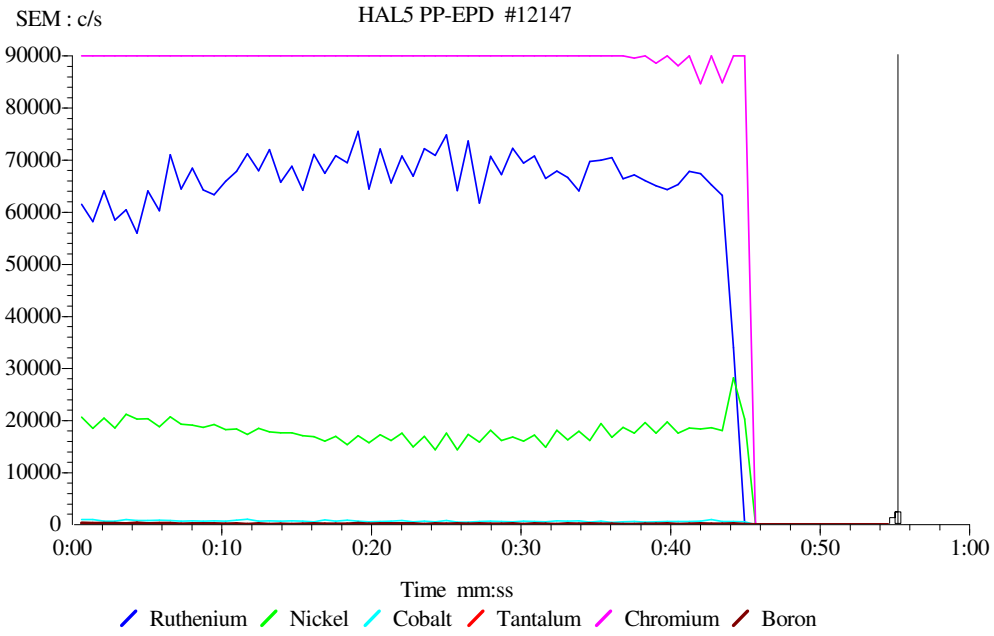
(a) (b)

Fig. 4.15 Ion beam etching of an arbitrary film with different beam angles (a) Normal incidence (Steep sidewall angle) (b) Away from normal incidence (Shallow sidewall angle [60]

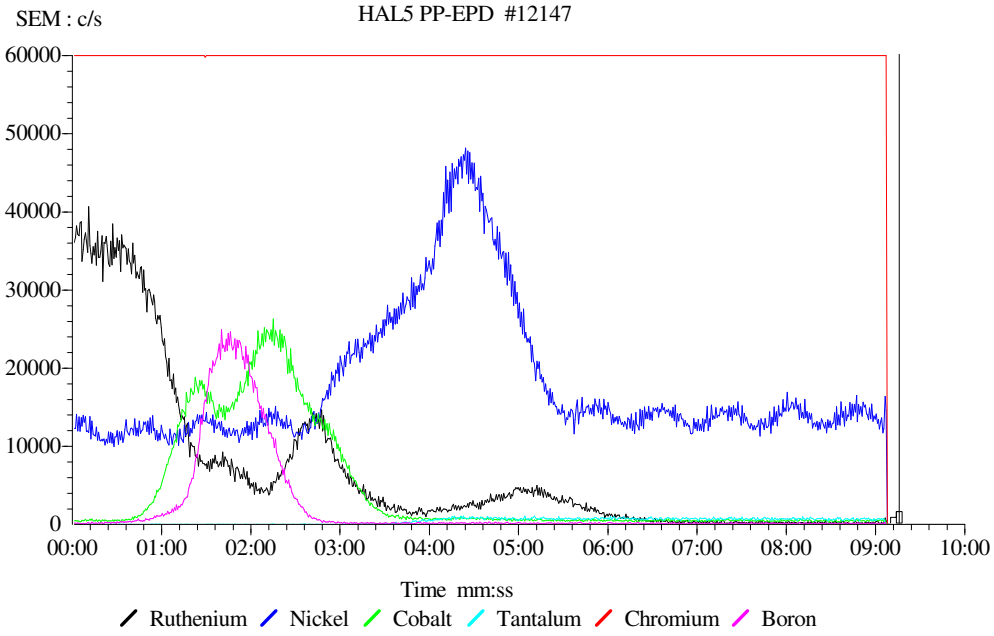
In order to optimize between these trade-offs, the process is carried out using a dual angle scheme. 10° from normal incidence is used until through the top Ru cap layer and after this 50° from the normal incidence until 70 % of NiFeCr is removed. The remainder of the etch is done at normal incidence. Etching is stopped after 20 nm over-etch into the bottom electrode. This over etch is done to remove any remaining foot from the device area and move it into the bottom electrode. The beam parameters 100 V/270 mA/-700 V are used while patterning all the wafers.

Considering the problem of using photo-resist as a mask during ion-milling as explained in Section 4.2.4, it was decided to explore hard mask approach during ion-milling. Refractory metals such as Ta, Cr are suitable to use in hard mask. During the process development in the current work, for few wafers, Ta and Al are explored as a hard mask. Al is chosen because of the ease of processing. Ta is patterned using the same lift-off process explained in Section 4.2.1 using dark field mesa definition mask while Al is patterned by standard ‘Al etch’ wet etchant using positive mask.

The end point in ion-milling process is determined by simultaneous SIMS profile measurements by detecting the occurrence of bottom electrode material. SIMS profiling of wafers with different mask materials are shown in Fig. 4.16 and Fig. 4.17. The profiles are shown for 10° as well as 50° degrees angles from normal of the ion beam. The initial etching with 10° beam angle is done for 1 min and at 50°, it is done for 9 minutes. The profiles are showing the occurrence of various elements in the MTJ stack indicated at the bottom of the traces. Fig. 4.16 shows the SIMS profile for the wafer with photo-resist as mask and Fig. 4.17 is for the wafer with Ta as hard mask. All the profiles are courtesy Veeco Instruments Inc., Plainview, NY.

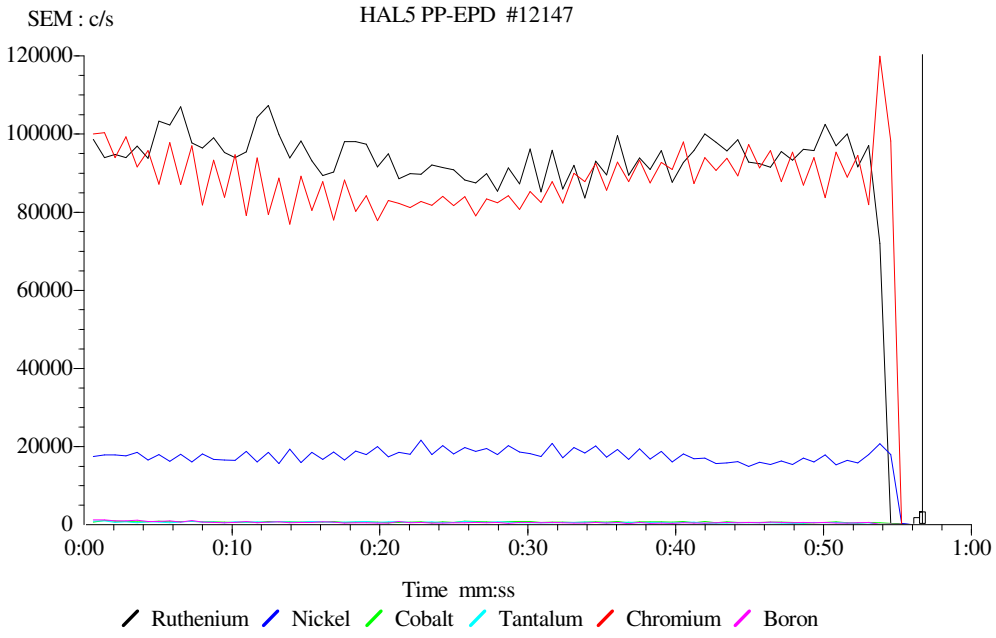


(a)

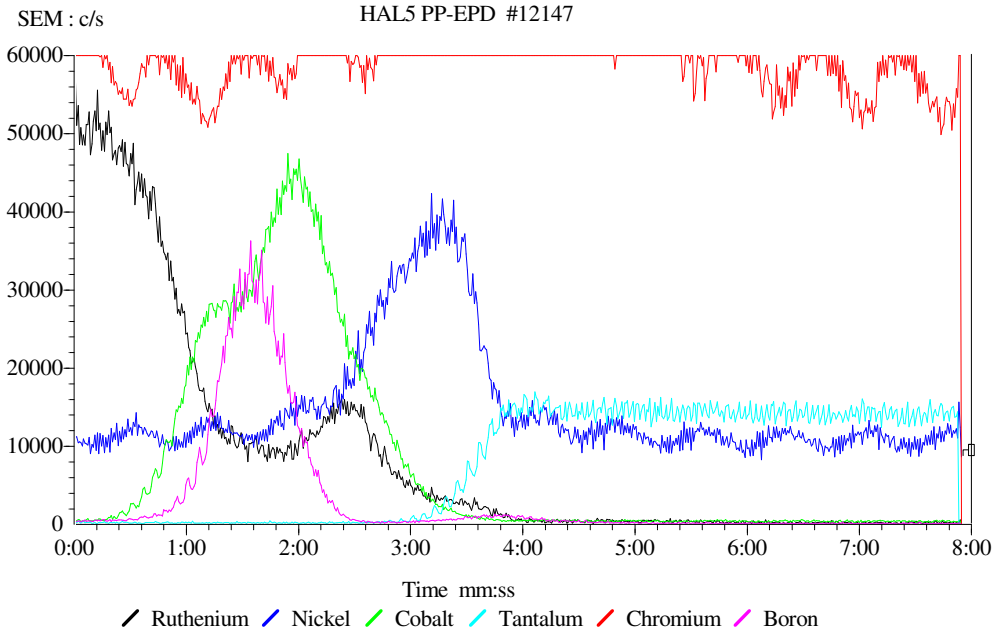


(b)

Fig. 4.16 SIMS trace for wafer with photoresist mask (a) At -10° (b) At -50°
Courtesy: Veeco Instruments Inc. Plainview, NY



(a)



(b)

Fig. 4.17 SIMS trace for wafer with Ta as hard mask (a) At -10° (b) At -50°
Courtesy: Veeco Instruments Inc. Plainview, NY

4.3 Summary of the Process Steps

The new process flow with the developments in the last section is as shown in Table 4.11. The contributions from the current work are highlighted in the table.

Table 4.11 Process steps for the integration of MTJ on silicon

No.	Process Step	Description	Parameters/Tools
1	Scribe	Scribing with diamond pen	--
2	Clean	Standard RCA clean	--
3	Thermal Oxide Growth	Thickness ~ 500 nm	1000 °C, 100 min. Wet Oxide Growth (Recipe 350 for Bruce Furnace Tube 1)
4	Litho. Level 0	Printing alignment marks on Wafer	GCA Stepper: Stepper Job- MTJ
5	Oxide Etch	Getting permanent alignment marks on wafer	10:1 BOE treatment for 10 min.
6	Resist Stripping	--	Branson Asher: O_2 plasma (Recipe: 4" normal)
7	**LOR 5A deposition**	**Coating liftoff resist for getting ~600 nm (3*bottom electrode) thickness**	**CEE100: 2000 RPM, 45 sec Spin Up: 500 R/S Spin Down: 3000 R/S Post coat bake: 150 °C, 1 min**
8	**Photoresist Coating**	**Lithography**	**SVG Track: 4500 RPM, 45 sec Post coat bake: 125 °C, 1 min**
9	**Exposure**	**Lithography**	**GCA Stepper Job: MTJ**
10	**Resist Development**	**Getting required undercuts for lift off process**	**CEE 100: CD 26 Developer Time: 130 sec**
11	**Bottom Electrode Deposition**	**Sputtering the bottom electrode material to get ~ 200 nm of thickness**	**CVC 601: Parameters given in Table 4.2 for NiCr and Ta**
12	**Metal Liftoff**	**Lifting off the Bottom electrode material to pattern it**	**Treatment with acetone and CD 26 or Nano Remover PG**
13	MTJ stack Deposition	At Veeco Instruments Inc, Fremont, CA	Nexus Physical Vapor Deposition (PVD) tool
14	Field Anneal	Pinning the MTJ "Reference Layer"	355C / 2hrs / 5000 Oe field / under vacuum (~1x10-6 Torr).
15	Litho. Level 1	MESA definition: Positive mask – Photo resist mask only	GCA Stepper: Stepper job – MTJ

Table 4.11 Process Steps for the integration of MTJ on silicon (contd.)

No.	Process Step	Description	Parameters/Tools
15A	**MESA Liftoff**	**MESA definition Negative mask: Metal Hard mask**	**Steps 7 to 12 should be followed with MESA liftoff mask**
16	**MTJ patterning**	**MTJ MESA etching using ion-milling. Done by Veeco Instruments Inc., Plainview, NY**	**Nexus IBE tool -10° /-50° dual angle End point: Bottom Electrode Material**
17	**Dry photo-resist strip**	**Removing hardened resist after MTJ MESA etching (Only if photo-resist mask for MTJ patterning)**	**Power: 150 W O_2: 30 sccm Pressure: 300 mTorr (Drytek Recipe: O2ASH) Time: 390 seconds**
18	**Solvent Strip**	**Removing remnant resist (Only if photo-resist mask for MTJ patterning)**	**PRS-2000 90 °C 5 min. (dirty) 5 min. (clean) 5 min. DI water rinse followed by SRD**
19	**ILD deposition**	**Coating on Silicon T-11 (311) SOG from Honeywell Inc.**	**3000 rpm, 1min (SCS P6700 Spinner)**
20	**ILD baking**	**Removing solvents from the deposited SOG**	**80-150-250°C for 5 min each on hot plates**
21	**Curing/Annealing ILD**	**Densifying / Reflowing SOG so that it withstands the field annealing process at the end of fabrication and improves its properties**	**350 °C, 1 hour, N_2 ambient. (Bruce Furnace: Tube 2, Recipe: shrini 350 C set up)**
22	Litho. Level: 2	For contact cut definition	GCA stepper Stepper Job – MTJ
23	**Contact cut dry etching**	**Anisotropic SOG etch using RIE technique (Partial etch to keep 50-100 nm of SOG)**	**Refer Table 4.9 Etch time decided on the basis of monitor wafer thickness**
24	**Contact cut wet etching**	**Etching remnant SOG. Avoids damage top Ru surface**	**100:1 HF treatment for 30 sec. followed by 5 min. DI water rinse and SRD**
25	**Resist Stripping**	**--**	**PRS-2000 90 °C 5 min. (dirty) 5 min. (clean) 5 min. DI water rinse followed by SRD**
26	Top electrode (Metal 1) deposition	Al deposition as top conduction electrode, Thickness ~ 500 nm	CVC 601: 1000 W, 5 mTorr, 16 mins (Dep. rate to be verified)

Table 4.11 Process Steps for the integration of MTJ on silicon (contd.)

No.	Process Step	Description	Parameters/Tools
27	Litho Level 3	Top electrode (Metal 1) Definition	GCA stepper: Stepper job – MTJ
28	Top Electrode patterning	Al etching	With "Al etch" as chemical (normally hot phosphoric acid). Etch rate to be verified for etch time
29	**Resist Stripping**	**--**	**PRS-2000 90 °C 5 min. (dirty) 5 min. (clean) 5 min. DI water rinse followed by SRD**
30	**Field Anneal**	**Pinning the MTJ "Reference Layer" (To be done Only if Step 13 is not done)**	**355 °C / 2hrs / 5000 Oe field / under vacuum (~1x10-6 Torr).**

Chapter 5

Corroborative Experiments during Process Development

MTJ device integration on silicon involved some experimental work for getting insight into the current process and to pave the way for future direction in these efforts. The experiments concentrate on improving and optimizing the current process flow as well as device design. They involve using various advanced metrology tools like XRD, AFM, and TEM.

5.1 Effect of sputtering conditions on surface morphology of NiCr

The importance of a smooth bottom conduction electrode for MTJ is elaborated in Chapter 4. The two materials we have considered in this work are Ta and NiCr. The thin film surface properties of these materials are related to the deposition conditions; sputtering process in this particular case. Therefore, a controlled experiment is designed to study ethe effect of sputtering conditions on the film surface morphology. NiCr is chosen for this study since its properties are measurable by the tools like AFM, XRD.

In order to do this study, the design of experiments approach is adopted. The aim of this experiment is to find the process conditions that will result in surface roughness of the film less than 1 nm and the objective is to assess the influence of deposition conditions on various surface parameters and process outcomes. The input factors and responses are shown in Table 5.1. Since there are two factors, namely sputtering pressure and power, three-level design is implemented in order to get more data points for making a sound decision.

Table 5.1 Input factors and response variables for NiCr DOE

Input Factors	Response Variables
Sputtering Pressure (mTorr)	Grain Size (nm)
Sputtering Power (W)	Surface Roughness (nm)
	Resistivity (ohm-cm)

The design space for the experiment is decided in the following way. A 4" target of NiCr is used and, therefore, sputtering power is limited to 300 W. The lower limit of sputtering power, 200 W, is decided in order to have reasonable deposition rate but still well separated from the upper limit in order to have the responses corresponding to these limits distinguishable. The lower limit of the sputtering pressure, 3 mTorr, is decided on the basis of the ability of the PVD system to form plasma and the upper limit, 13 mTorr, is due to the maximum sputtering pressure to which the deposition system is allowed to operate. The third level for these factors essentially divides the design space evenly. The design matrix with all the treatment combinations of a 3 level 2 factorial design is shown pictorially in Fig. 5.1. The experiment is executed randomly over the time of 3-4 months.

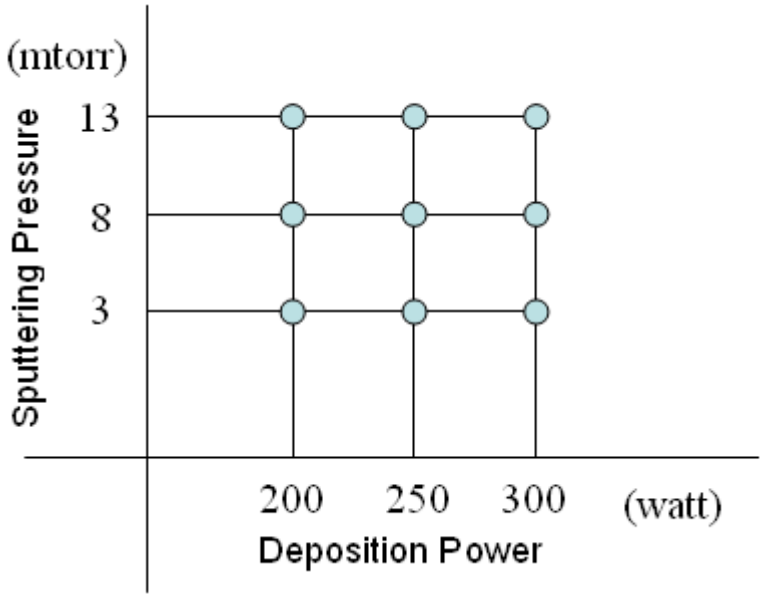
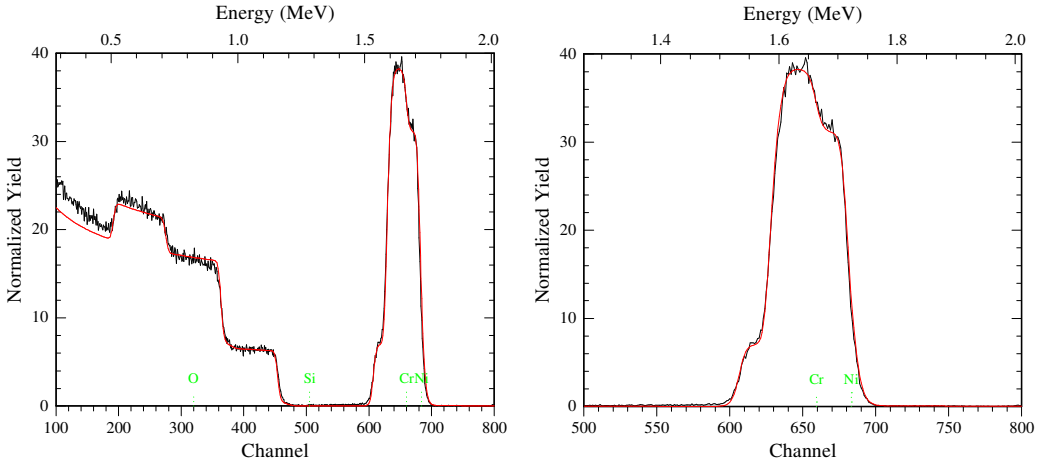


Fig. 5.1 Design matrix for NiCr DOE.

Before this experiment, the composition of NiCr target is confirmed by Rutherford Backscattering Spectroscopy (RBS) in collaboration with Mr. Gabriel Braunstein, University of Central Florida. In this technique, helium ions are made to bombard on the sample which backscatter after collision with sample atoms. On the basis of the number of helium ions backscattered and their energy distribution, the composition of the sample is determined.

The results are shown in Fig. 5.2 which give Ni(77):Cr(23) composition of NiCr. The target composition is Ni(80):Cr(20) and the variation is attributed to the sputtering yield of Ni and Cr.



(a) (b)

Fig. 5.2 RBS trace for NiCr deposited on oxidized Si (a) For the whole sample depth (b) Zoomed in on NiCr peak

As mentioned earlier, the treatment combinations in Fig. 5.1 are implemented randomly. The surface morphology of the samples is analyzed using atomic force microscopy (AFM) from Digital Instruments Division 3000 in Advanced Material Lab with the help from Dr. Feiming Bai. The tapping mode AFM is used with 10 nm silicon

tip. The AFM images, 1 µm x 1 µm in size, are obtained for all the samples and they are shown in the design matrix in Fig. 5.3.

The AFM images were analyzed using WSxM 2.2 for getting required grain size and surface roughness parameters. This is done with the help from Mr. SunWoo Lee.

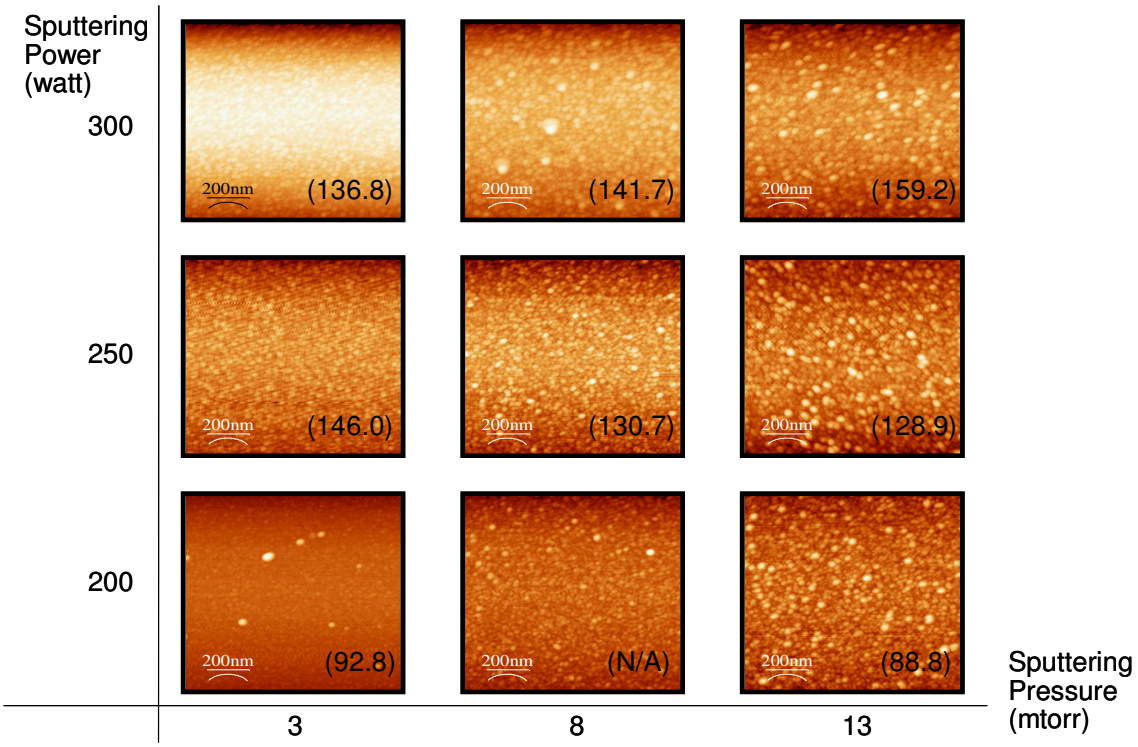


Fig. 5.3 AFM images obtained for various treatment combinations in NiCr DOE (AFM analysis by Mr. SunWoo Lee)

The analysis of the images to get the required data is done by the following steps:

1. Flatten the image to eliminate varying sample tilt contribution over the length of the trace. This is illustrated in Fig. 5.4
2. The surface roughness is measured for the whole AFM image by the software using surface analysis option. One example of such measurement is shown in Fig. 5.5

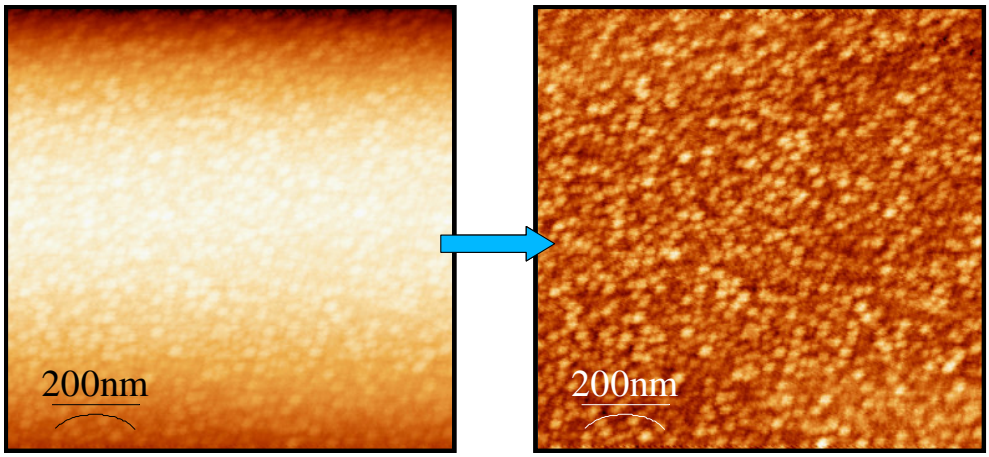


Fig. 5.4 Flattening of the AFM image
(AFM analysis by Mr. SunWoo Lee)

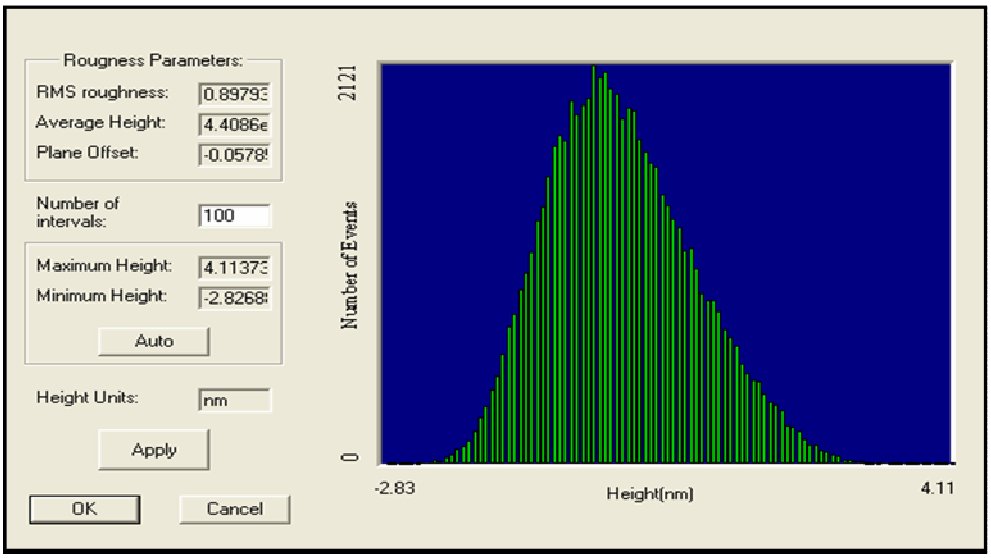


Fig. 5.5 Surface Roughness measurement on AFM image
(AFM analysis by Mr. SunWoo Lee)

3. The grain size is measured by taking section on the AFM image, getting the 2D profile and measuring the peak width as shown in Fig. 5.6

Several such sections are taken at different angles to get the accurate estimate of the grain size for the given sample.

All the treatment combinations and the corresponding measured surface morphology parameters are shown in Table 5.2

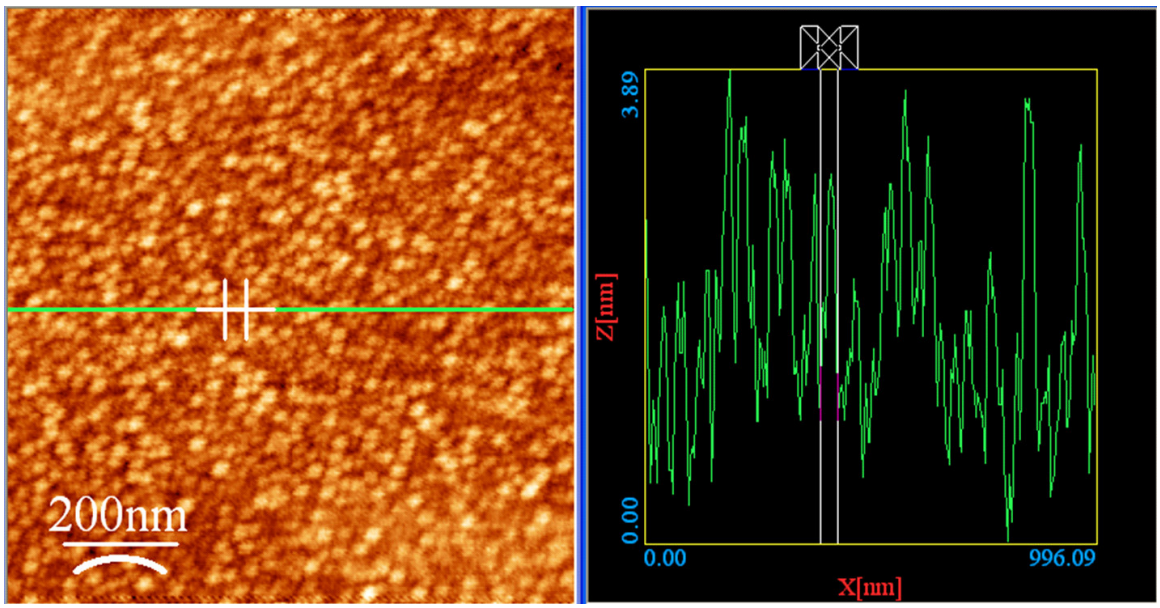


Fig. 5.6 Grain size measurement on AFM image
(AFM analysis by Mr. SunWoo Lee)

.

Table 5.2 Treatment combinations with surface morphology related responses for NiCr DOE

Treatment Combination	Sputtering Power (W)	Sputtering Pressure (mTorr)	Surface Roughness (nm)	Grain Size (nm)
00	200	3	0.896	22.974
01	200	8	1.021	30.374
02	200	13	1.697	38.809
10	250	3	0.716	30.162
11	250	8	1.194	35.073
12	250	13	2.139	41.994
20	300	3	0.898	35.677
21	300	8	1.451	43.350
22	300	13	2.216	46.694

DOE analysis is performed on this data using JMP IN software. The resulting plots are shown in Fig 5.7 and Fig. 5.8 for surface roughness and grain size, respectively.

It can be concluded from the plots that surface roughness is a significant function of sputtering pressure while grain size is sensitive to both, sputtering pressure as well as power.

The data from Table 5.2 also shows that the desired surface roughness of less than 1 nm is obtained for 3 mTorr pressure and the least among them is "250 W, 3 mTorr" combination. Therefore, this is the most suitable condition for NiCr deposition to be used as bottom conduction electrode of MTJ.

The sheet resistance of all the samples is measured using four point probe technique. The data corresponding to the treatment combinations is given in Table 5.3 and DOE analysis using JMP IN is shown in Fig. 5.9.

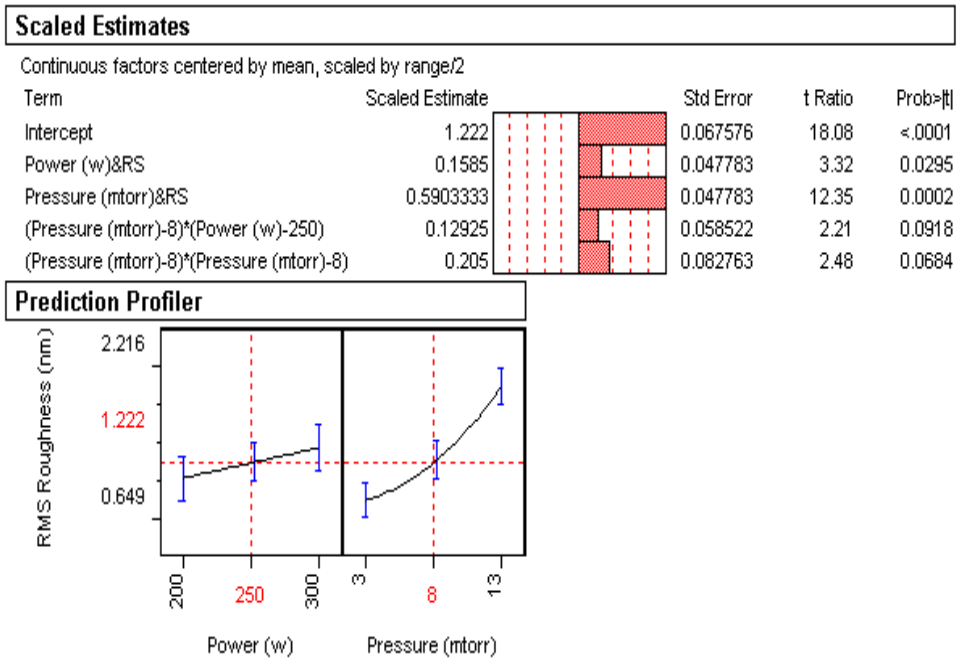


Fig. 5.7 Surface roughness dependence from DOE data analysis in JMP IN for NiCr

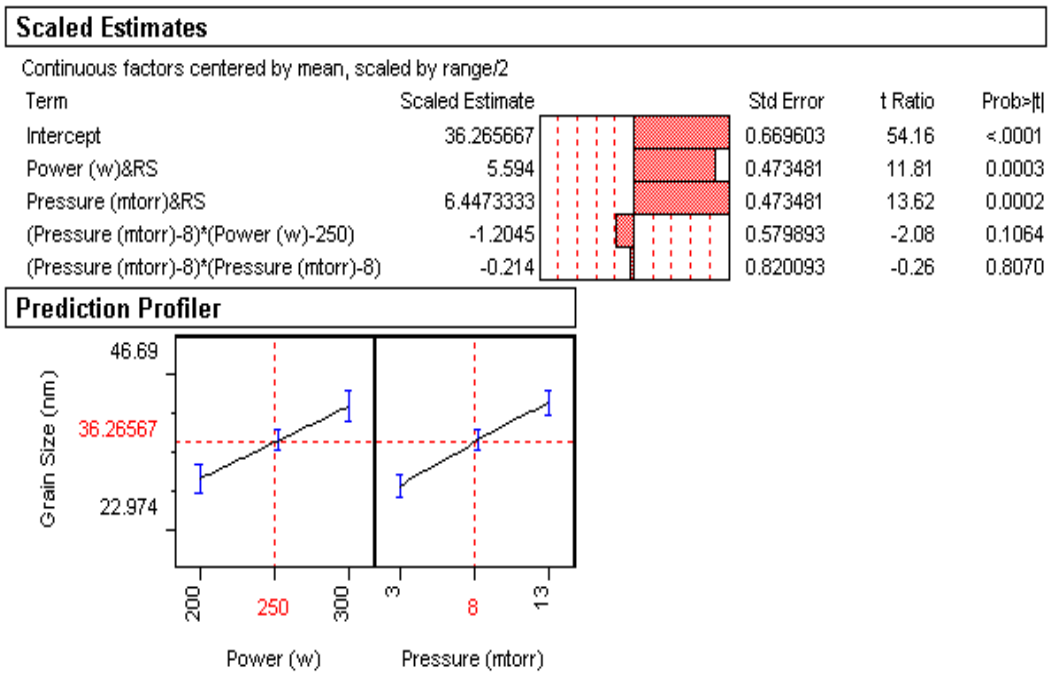


Fig. 5.8 Grain size dependence from DOE data analysis in JMP IN for NiCr

Table 5.3 Treatment combinations with resistivity as response for NiCr DOE

Treatment Combination	Sputtering Power (W)	Sputtering Pressure (mTorr)	Sheet Resistance (Ω/sq.)	Thickness (nm)	Resistivity (Ω-cm)
00	200	3	7.89391	108.3	8.5467e-5
01	200	8	8.76465	N/A	N/A
02	200	13	10.1009	103.6	1.0464e-4
10	250	3	6.42289	170.3	1.0940e-4
11	250	8	6.98364	152.5	1.0649e-4
12	250	13	8.1663	150.4	1.2281e-4
20	300	3	5.4445	159.6	8.6893e-5
21	300	8	5.94153	165.3	9.8225e-5
22	300	13	6.25081	185.7	1.1610e-4

The resistivity shows same type of dependence as surface roughness. It is more sensitive to sputtering pressure than power. The treatment combination “250W, 3mTorr”

yielded the best surface roughness, the resistivity 109 μΩ is low enough to be used as a bottom conduction electrode.

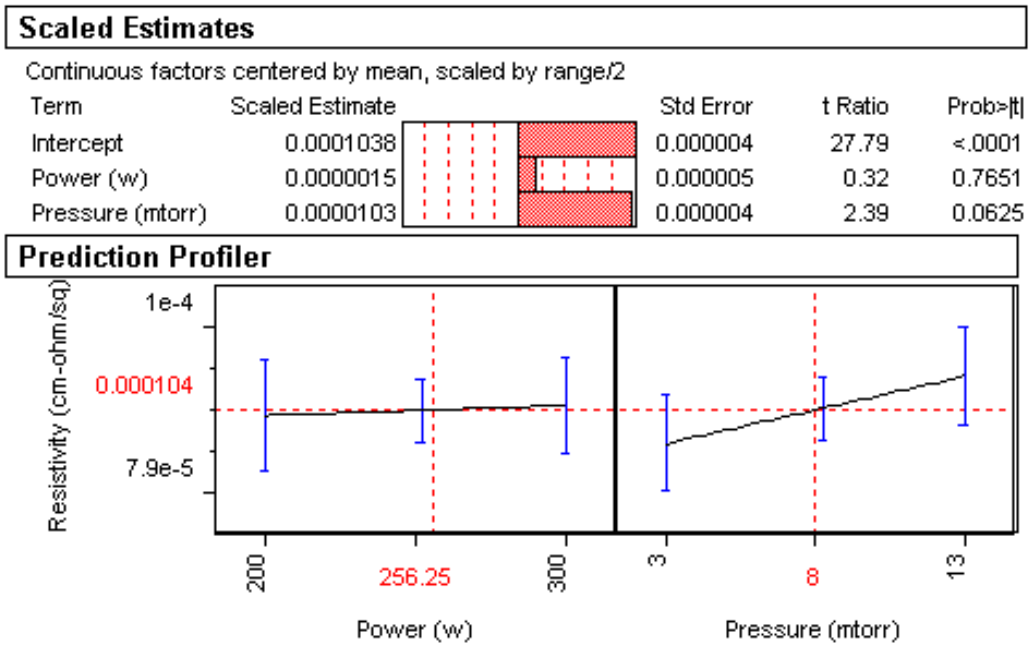


Fig. 5.9 Resistivity Dependence from DOE data analysis for NiCr

5.2 XRD study of MTJ stack with annealing

In Chapter 4, Section 4.2.2, the requirement of annealing the CoFeB/MgO based MTJ stack after deposition is mentioned. As deposited, CoFeB is amorphous in nature while MgO is polycrystalline with preferential (001) bcc orientation. The annealing in magnetic field crystallizes the CoFeB where MgO acts as a template for this crystallization. For getting high TMR, it is expected that CoFeB crystallizes to bcc (001) at the interface with MgO for coherent spin-dependent tunneling to occur. The temperature of annealing is very crucial in realizing this. The illustrative plot of TMR versus annealing temperature is shown in Fig. 5.10. [61]

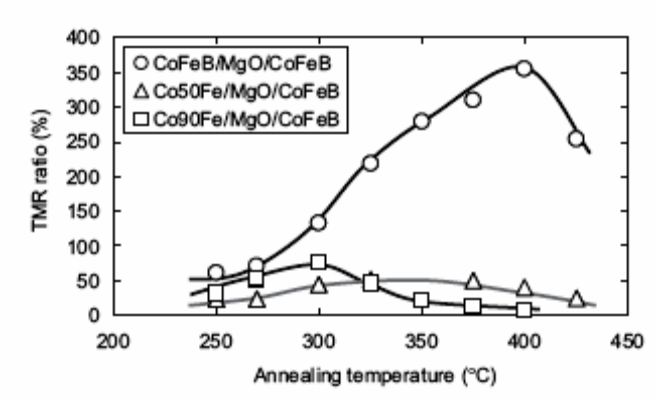


Fig. 5.10 Dependence of TMR on annealing temperature [61]

Fig. 5.10 is dependent on type of ferromagnetic electrode [61], composition of CoFeB electrode [62], as well as the type and thickness of the adjacent layers to the ferromagnetic electrode [63] [64]. The data adopted from [61] shown in Table 5.4 illustrates the TMR as well as RA dependence of various "reference " and "free" layers annealed at optimum temperatures to get the maximum TMR. In summary, optimizing device design and annealing conditions is extremely important in CoFeB crystallization in CoFeB/MgO-based MTJ and, in turn, getting high TMR. Fig. 5.11 shows various factors affecting CoFeB crystallization pictorially.

Table 5.4 Optimum annealing temperatures for different "reference" and "free" layers in CoFe(B)/MgO based MTJ to get high TMR
(Data adopted from [61])

Reference Layer	**Free Layer**	**Optimum Annealing Temperature (^{0}C)**	**TMR**	**RA (Ω-μm^2)**
$Co_{40}Fe_{40}B_{20}$	$Co_{40}Fe_{40}B_{20}$	400	355	547
$Co_{40}Fe_{40}B_{20}$	$Co_{50}Fe_{50}$	400	277	1060
$Co_{40}Fe_{40}B_{20}$	$Co_{90}Fe_{10}$	350	131	714
$Co_{50}Fe_{50}$	$Co_{40}Fe_{40}B_{20}$	325	50	1042
$Co_{40}Fe_{40}B_{20}$	$Co_{50}Fe_{50}$	270	12	740
$Co_{90}Fe_{10}$	$Co_{40}Fe_{40}B_{20}$	300	75	475
$Co_{90}Fe_{10}$	$Co_{90}Fe_{10}$	270	53	571
(Pseudo-spin valve with 1.7 nm thick MgO barrier)				
$Co_{40}Fe_{40}B_{20}$	$Co_{40}Fe_{40}B_{20}$	450	450	3700

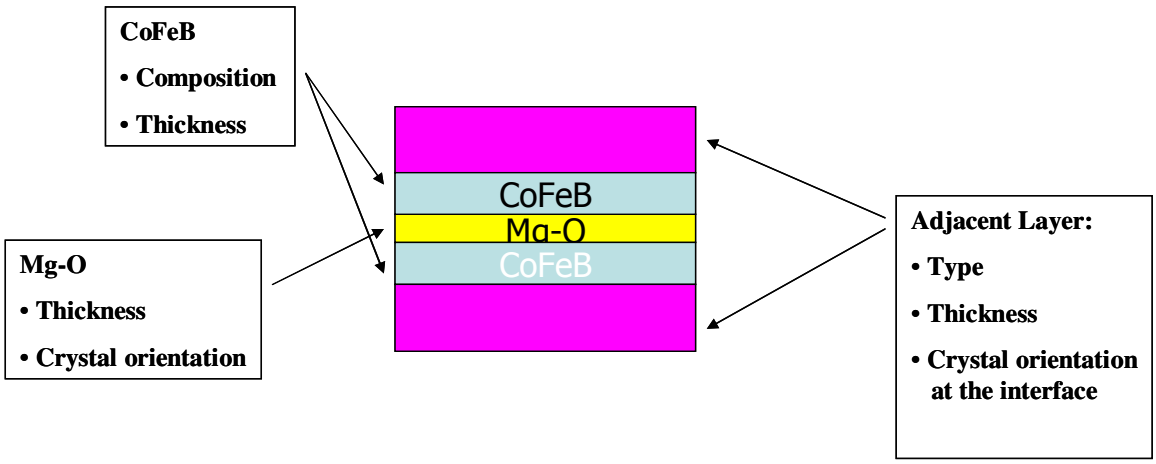


Fig. 5.11 Factors affecting CoFeB crystallization during annealing

It was decided to find the optimum conditions of annealing for the MTJ stack employed in the current work. The method adopted is the in situ annealing of the MTJ stack at different temperatures in N_2 ambient and getting corresponding XRD patterns. It is assumed that the optimum condition is reached when CoFeB (200) peak is visible.

The measurements are done using Bruker D8 Discover XRD incorporating 2D area detector in Advanced Materials Lab in RIT with the help from Dr. Feiming Bai. The sample used for the measurement had a blanket MTJ stack deposited on patterned Ta. In 2D plots, the single crystal/textured sample shows spindle-like intensity while homogenous conic curve indicates polycrystalline sample. Also, all the plots are shown with MTJ stack indicating the corresponding MTJ layer.

Fig. 5.12 shows the XRD done on patterned region where we get strong (002) and weak (202) peaks corresponding to Ta. This confirmed that the Ta bottom electrode is crystalline and highly textured.

Fig. 5.13 shows the XRD plots on streets of the wafer where there is no Ta for two different cases; one is as-deposited and the other is in situ annealed at 350 °C for 1

hour. The peaks correspond to Ru (002) and NiFeCr (111). The relative intensity change after annealing is attributed to the oxidation of top Ru surface. The Ru (002) peak itself is confirmed by changing to $\chi = 32.3^0$ which made Ru (101) peak visible as shown in Fig. 5.14. This angle is calculated by considering hcp Ru structure.

Fig. 5.15 shows the XRD measurement as deposited and annealed at 400 ^{0}C for 1 hour with 3^0 grazing angle of incidence. This angle of incidence is chosen to get more diffracted intensity from the sample. The plot after 400 ^{0}C annealing showed the presence of CoFeB (200) peak. The same peak was not visible at 350 ^{0}C anneal. Therefore, it can be concluded that the crystallization of CoFeB started after 350 ^{0}C. Also, CoFeB is polycrystalline in nature and not textured. It is inferred from this experiment that the optimum temperature for CoFeB crystallization and, in turn, getting better magnetic response is more than 350 ^{0}C and the current 355 ^{0}C field annealing step may not be adequate.

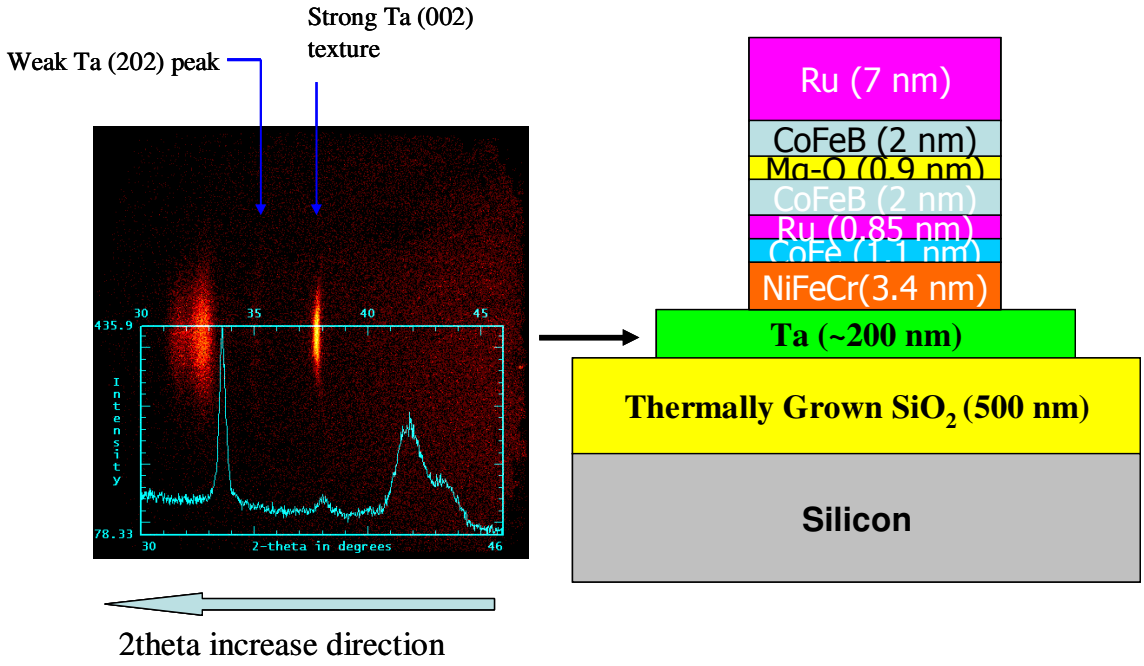


Fig. 5.12 XRD on MTJ stack on Ta

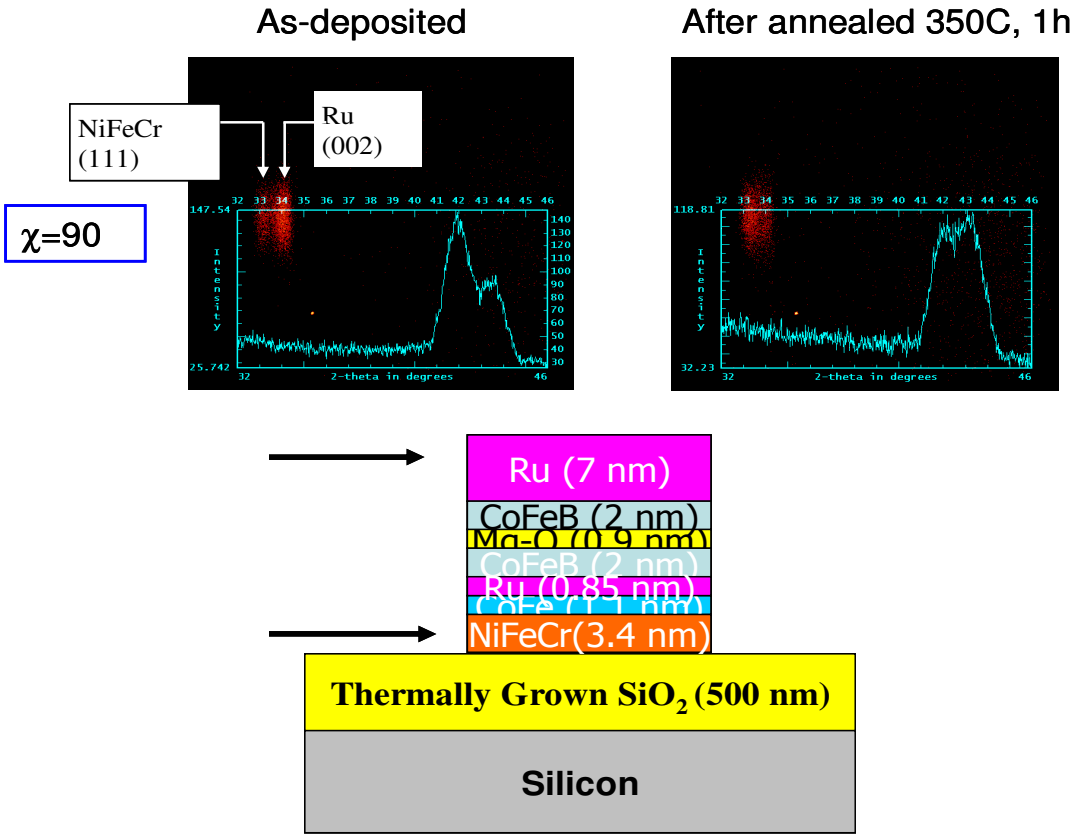


Fig. 5.13 XRD on MTJ stack directly on thermally grown oxide

From this experiment, the peak corresponding to MgO (200) at 43^0 is not observed. It may be because of the presence of other strong peaks corresponding to NiFeCr and Ta. Also, the MgO layer is very thin (0.9 nm) and therefore, the diffracted intensity from the layer won't be very strong.

5.3 XTEM and PEELS analysis on MTJ stack

The MTJ device performance depends on the interface quality and integrity of the thin films. The most critical of them is the MTJ sandwich consisting of tunnel barrier and ferromagnetic electrodes. The experiment performed using the techniques explained in this section investigates the interface and compositional properties of the MTJ stack.

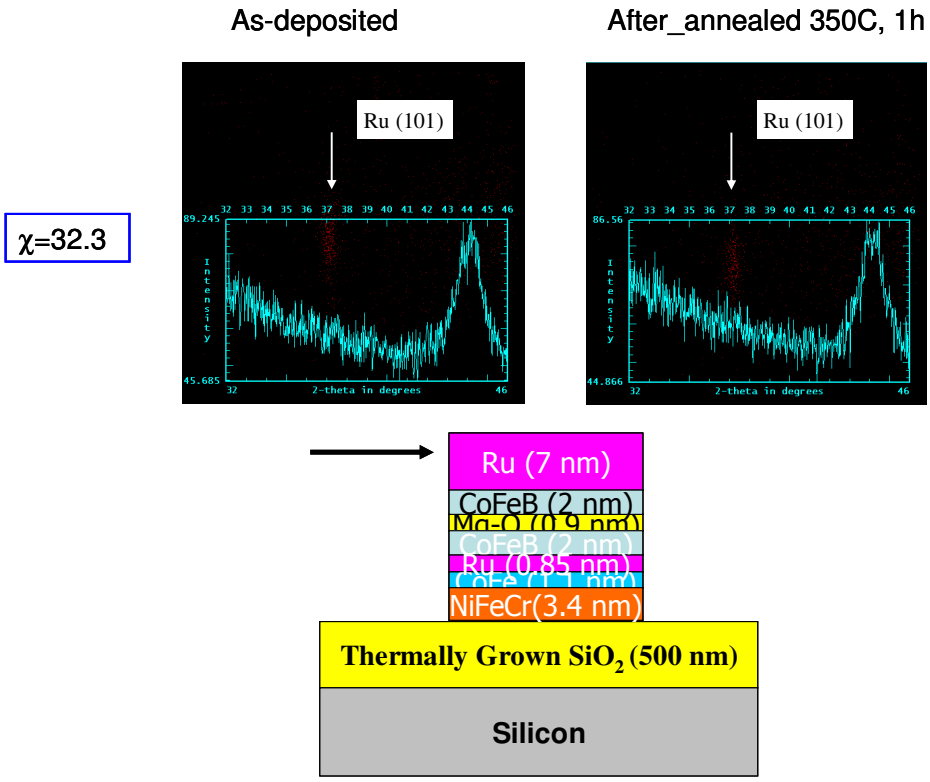


Fig. 5.14 XRD on MTJ stack with $\chi = 32.3$ to extract Ru(101) and confirm its presence

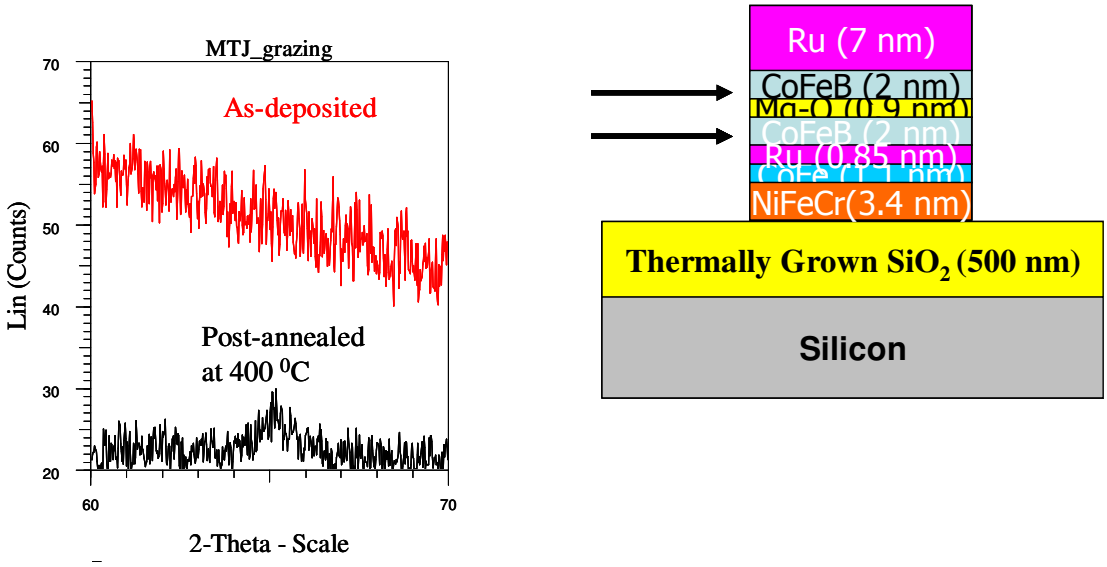


Fig. 5.15 XRD on MTJ stack at 3^0 grazing incident angle showing CoFeB (200) peak

Cross-section Tunneling Electron Microscopy (XTEM) can be employed for studying the interface quality of MTJ thin films. It also can give information about the phase of the films to limited extent. This study is done in collaboration with Mr. David McMahon and Mr. Swapnyl Shah from Micron Technology Inc., Manassas, Virginia. The sample preparation for this measurement is shown in Fig. 5.16. The Focused Ion Beam (FIB) cut is taken exactly on top of the device and the images at various magnifications are taken with Hitachi XTEM tool. Fig. 5.17 shows the electron micrograph of the MTJ with various layers labeled.

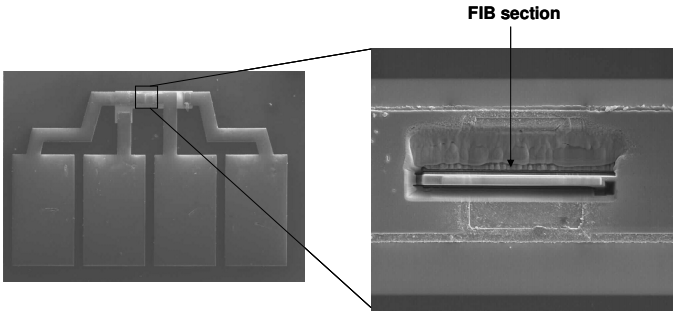


Fig. 5.16 Sample preparation for XTEM measurement

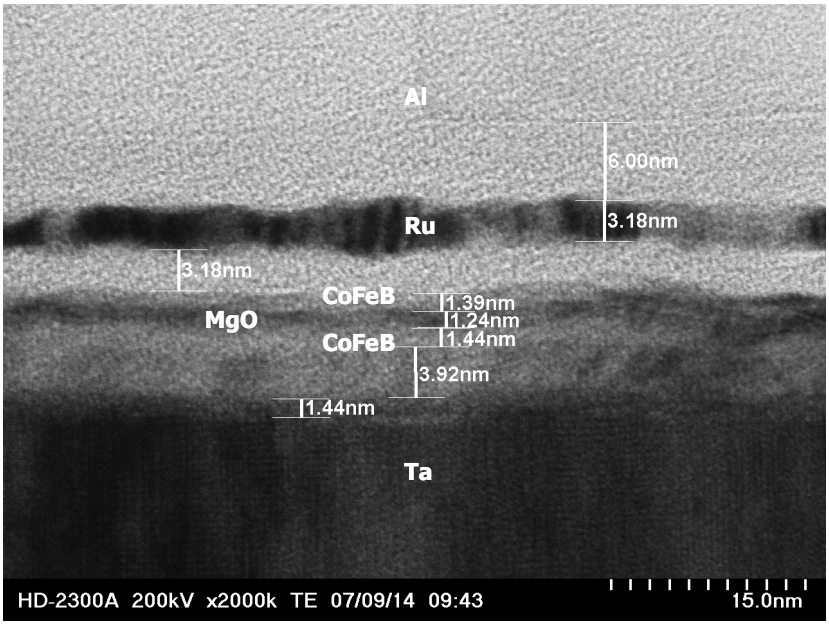


Fig. 5.17 XTEM micrograph of MTJ Device

The layers in the figure are labeled according to the measurement of the thicknesses shown. The measurements show that though the layers are contiguous, some interfacial layers might be getting formed due to inter-diffusion of various elements in the films. Also, we compare the obtained image with the similar taken from the literature as shown in Fig. 5.18, we can conclude that the interface quality may not be good in the fabricated MTJ stack in Fig. 5.18.

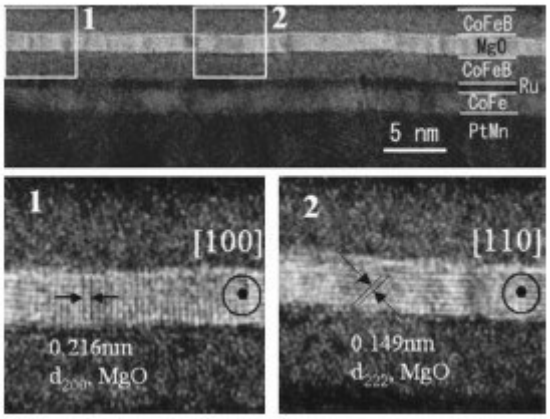


Fig. 5.18 XTEM on MTJ stack with excellent interface quality [65]

Parallel Electron Energy Loss Spectroscopy (PEELS) is the technique used for getting the chemical composition of the MTJ layers. This would be useful in understanding whether there are any inter-diffusions occurring at the interface in the MTJ stack. The PEELS output overlapping the dark field XTEM image is shown in Fig. 5.19. The overlapping curves indicate the presence of various elements in that particular film by the core-loss signal obtained from the PEELS output. The enlarged and labeled output is shown indicates presence of various elements in found in the MTJ stack layers. The elements shown in black are the desired elements in the layer and ones shown in red are undesirable. It should be noted here that the sectioning of the PEELS curves are done one the basis of presence of various elements vis-à-vis MTJ stack and should not be

interpreted as actual thickness of the layers. Following are the salient observations from the analysis are as follows,

1. Absence of Co in the free layer

2. Presence of various undesirable elements in the free layer (Ru), tunneling barrier (Fe, B, F), in the capping Ru layer (Fe, Al), and in the top electrode (O, Fe,F).

From these observations, we can conclude that there is an inter-diffusion occurring between the layers of the MTJ stack either during the deposition or during the fabrication process. The analysis of these observations is presented in the next paragraph.

Co loss in the free layer seems to be the problem during deposition. The layers are deposited by Nexus Physical Vapor Deposition (PVD) tool by co-sputtering technique at Veeco Instruments, Fremont, CA. The power may not have been applied to the Co target during co-sputtering of the CoFeB free layer. The author would want to note here that it is necessary to verify this from the collaborators in Veeco and while this chapter is being written, it has not been verified. If it is proved beyond doubt that there is no problem with the co-sputtering then the only theory that could be valid is the diffusion of Co through MgO into reference layer and in author's opinion, it is very unlikely.

Boron diffusion into MgO during annealing for CoFeB crystallization has been reported in the literature [66] since B is not soluble in CoFe. The presence of Fe into the tunneling barrier may be due to the diffusion from side ferromagnetic electrodes. The literature has also reported formation of Fe oxide at the interface with MgO [66]. This would compromise the interface quality and also would be detrimental to the quality of MgO as tunneling barrier. The presence of Ru in free layer would also make it more "non-magnetic" and jeopardize the performance of MTJ. The presence of Fluorine (F) in

tunneling barrier and top electrode could be from the CHF_3 based chemistry used for contact cut etching. The top electrode is also contaminated with Fe showing that the extent of Fe diffusion is large in this MTJ stack.

The results from these experiments would be useful in analyzing the electrical test results obtained and presented in the next chapte

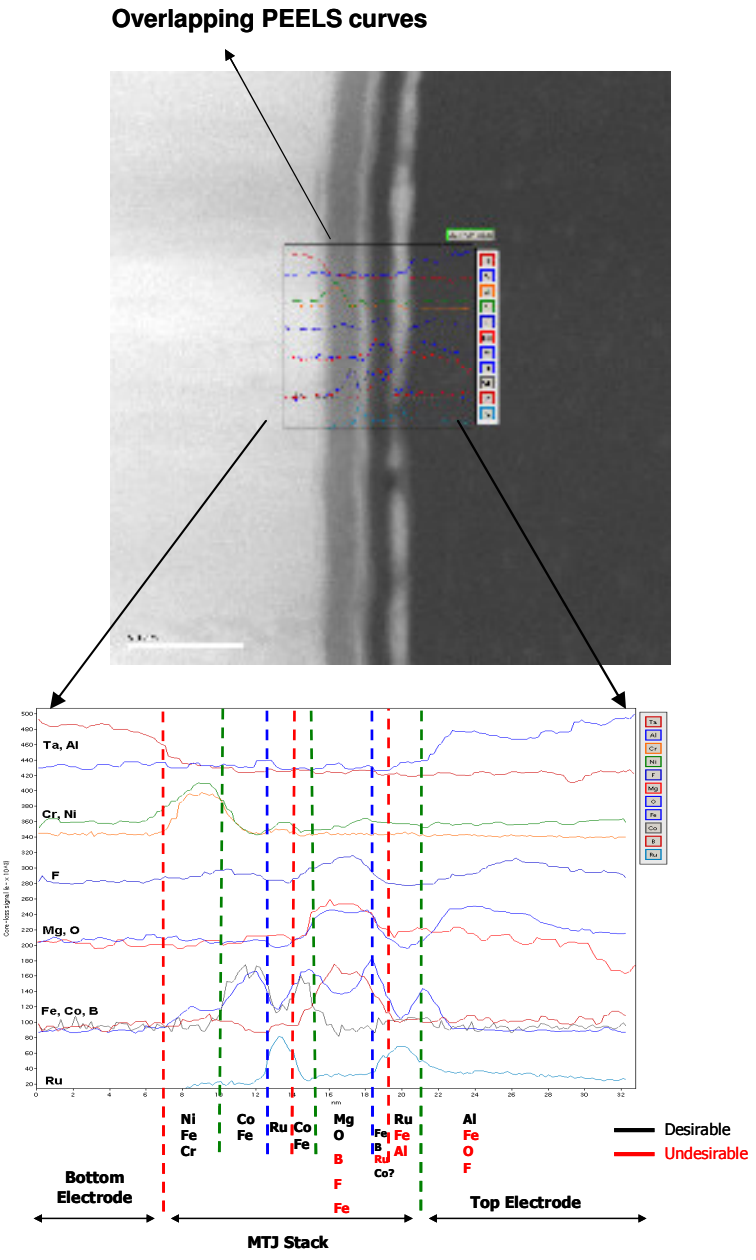


Fig. 5.19 PEELS study on MTJ stack

Chapter 6

Electrical Test Results

The chapter details the electrical testing of the fabricated MTJ. The testing is aimed at studying the variations in process done during the fabrication.

6.1 Testing Method

The MTJ devices are usually tested with a four point probe technique where current is passed through the MTJ stack and the response voltage across the junction is measured.

The layout from the testing point of view is as shown in Fig. 6.1.

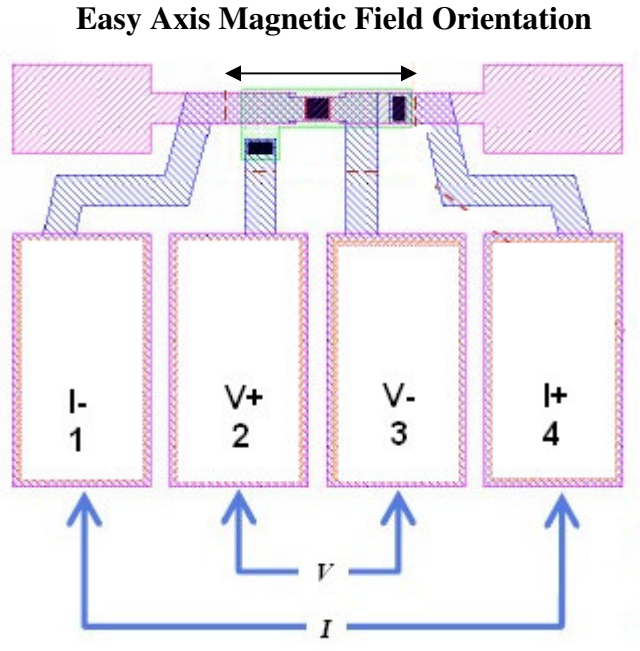


Fig. 6.1 MTJ Layout from testing point of view

Pads 4 and 1 are for forcing the current and Pads 2 and 3 to measure the voltage. The resistance of the junction is measured for the given size of the device and the specific resistivity of the device or RA product is calculated. Since, by default, the FM layers in

MTJ are oriented parallel, low resistance is expected in this measurement and the voltage so developed for the given current is called the "bias voltage" for the device.

The standard steps for the testing with magnetic field are shown in Table 6.1. This testing considers the fact that the magnetic response of the device is dependent on its bias voltage defined in the earlier paragraph and this has been reported in the literature [67]. The typical curve of TMR vs. bias voltage is shown in Fig. 6.2 [67]. The bias voltage dependence is due to the extrinsic scattering of tunneling electrons by phonon and magnon scattering [68]. The left axis shows the dependence of resistance for parallel and anti-parallel case and the right side shows the TMR.

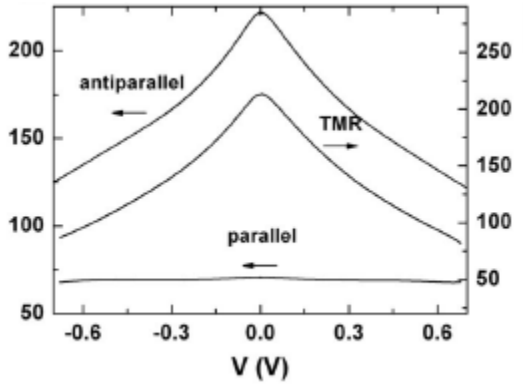


Fig. 6.2 TMR dependence with bias voltage for CoFeB/MgO/CoFeB MTJ [67]

Fig. 6.2 is a decreasing curve on both positive as well as negative sides of zero (where there is a maximum TMR). The bias voltage for our measurement is fixed to 1 mV. The magnetic field is varied in steps to find and trace the free layer magnetic loop along the easy axis direction shown in Fig. 6.1.

Table 6.1 Steps for testing MTJ device under magnetic field

Step No.	Description
1	Adjust the forcing current through Pad 4 & 1 to get 1 mV of output from Pad 2 &3. This is the "bias voltage".
2	Apply magnetic field in easy direction in the steps of 50 Oe from ± 50 Oe to ± 500 Oe in order to find the free layer loop by catching the change in voltage
3	Plot resistance versus magnetic field (R-H) curve and in turn TMR versus magnetic field for the given device
4	Study size, bias voltage, and temperature dependence of TMR

6.2 Test Set up

The measurements of RA products is done by Keithley 6700 tool by four point probe technique. Current is varied from 0-100 μA and the response voltage is measured. The resistance of the junction is extracted from the slope of the curve and it is multiplied with the area of the device to get RA products.

For magnetic measurements, we used the test set up in Cornell and Hitachi for two separate set of wafers. Fig. 6.3 shows general test set up schematic. The specific parts used in Cornell are mentioned in Table 6.2.

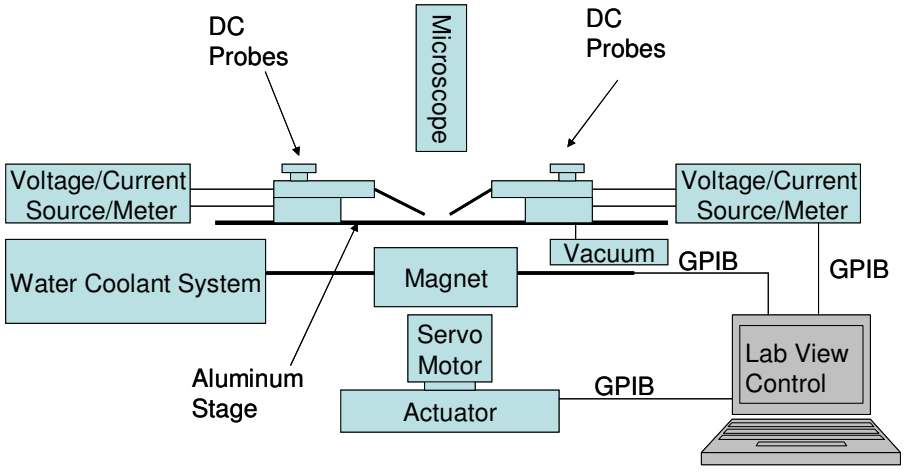


Fig. 6.3 General Test Station Schematic for MTJ testing

Table 6.2 Specific parts in Test station used in Cornell from Test Station schematic

Part	Brand/Make
Magnet	GMW 5201: GMW make
Servo Motor and Actuator	Newport make
Voltage/Current Source/Meter	Keithley 4200 system
DC probes	Cascade MicroTech make
Aluminum stage with Vacuum	In house
Water Coolant system	In house
LabVIEW and GPIB interface	In house

Table 6.2 should act as a starting guideline to build the test set up in RIT.

At Hitachi, the test set up consists of Keithley 2400 system and dV/dI apparatus (SRS locking running with Iac ~ 10 μA). The testing at Hitachi was done in collaboration with Ms. Liesl Folks.

6.3 Test Results

The measurement of RA products without magnetic field is done for various process variations adopted. These measurements are done for the pilot lot wafers. Fig. 6.4 shows the plot of RA product vs. device size for Ta continuous versus patterned bottom electrode. We get relatively high RA products for continuous bottom electrode compared to the patterned one for all the device sizes. However, the standard deviations obtained for these RA products are also very high for the continuous case. It is author's opinion that this is not due to the bottom electrodes being continuous or patterned. It is because of the way those wafers were processed especially at the time of contact cut etching where there is a possibility of top Ru surface getting damaged and its interface with top Al electrode may not be very smooth. This damage won't be uniform across the wafer and

that would possibly explain the large standard deviation obtained in the continuous bottom electrode case.

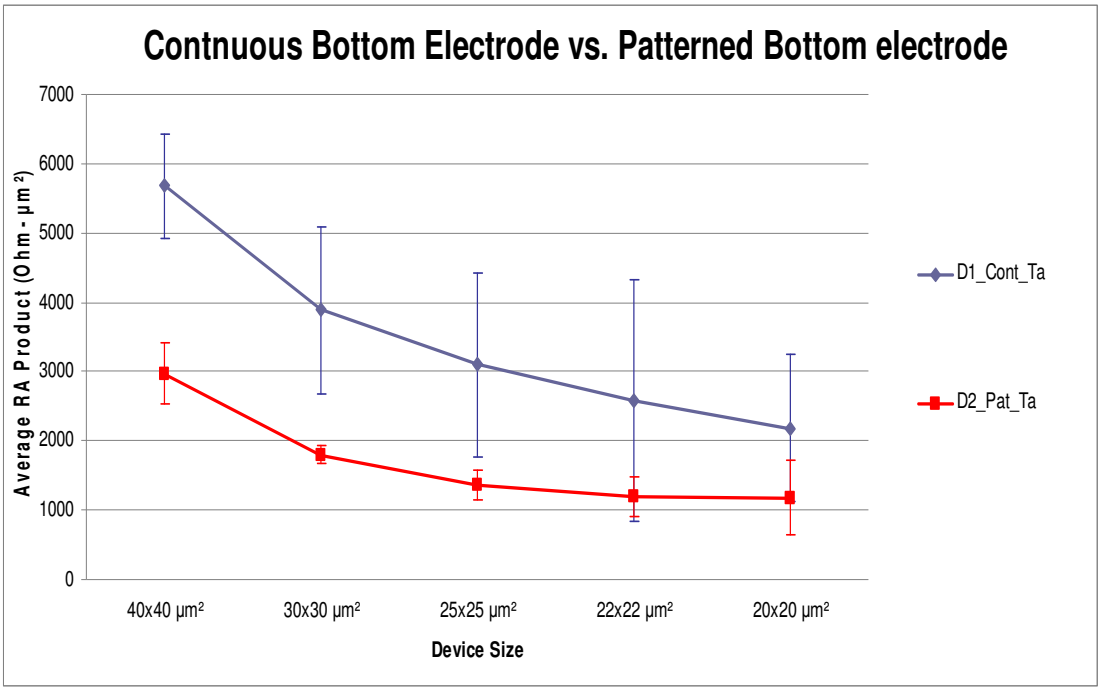


Fig. 6.4 RA product vs. device size for continuous and patterned Ta bottom electrode MTJ devices

The second variation that is tested is NiCr vs. Ta as bottom electrode. Fig. 6.5 shows this comparison for similar type of measurement as done the earlier case. The figure shows NiCr bottom electrode MTJs having higher RA products than the ones with Ta bottom electrodes. The NiCr bottom electrode MTJs also show very high standard deviations. This, again, can be attributed to the process variations and damage during the contact cut etching through spin-on glass-based ILD. Apart from this, it may be due to the local oxidation of NiCr at the contact since the alloy is prone to oxidation due to the presence of Cr.

From the results obtained from the pilot wafers, Ta patterned bottom electrode MTJ has shown very good process repeatability on the basis of small standard deviations

obtained for the RA products of various sizes. These observations are also corroborated by the XRD and STEM measurements where the presence of textured Ta with very good interfacial properties is observed.

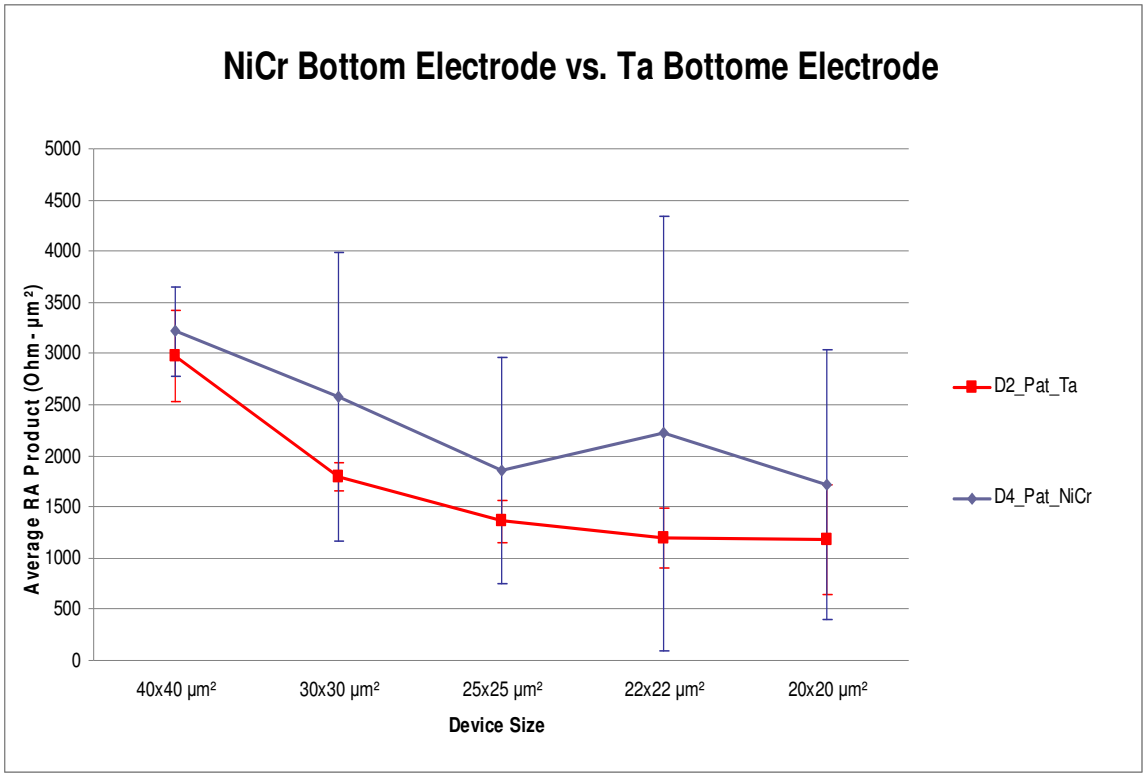


Fig. 6.5 RA product vs. device size for NiCr and Ta bottom electrode MTJ devices

The absolute values of the RA products are comparable to the expected range of RA products in the literature. For MgO-based MTJ where MgO is reactively sputtered like in our case, the expected range of RA products is 0.1-1000 kΩ-µm^2 [69]. This variation can be tuned with the MgO thickness ranging from 0.5 nm and higher where RA product increases with MgO thickness. Given our thickness of 0.9 nm, which is at the lower end, the obtained RA products from 1 to 3 kΩ-µm^2 for patterned Ta bottom electrode case are very promising.

While testing with magnetic field at Cornell as well as at Hitachi, we did not get any magnetic response from these devices in pilot lot as shown in Fig. 6.6 for a device tested in Hitachi. Possible reasons of this absence are elaborated in the next section.

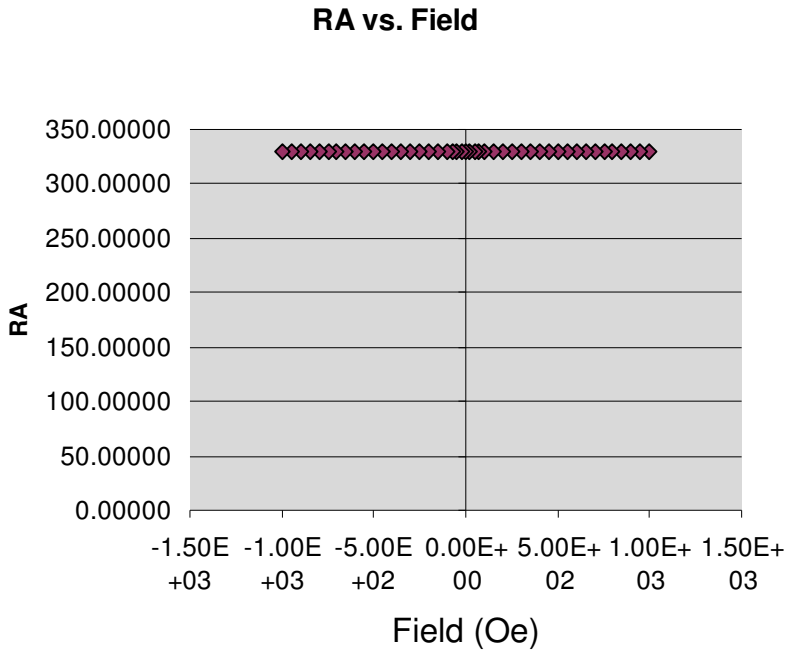


Fig. 6.6 RA product versus magnetic field for a device tested in Hitachi

6.4 Discussion of the Results

On the basis of the corroborative experiments explained in Chapter 5, there can be three reasons for the absence of magnetic response given the fact that our RA products for this lot are fine.

1. Néel coupling or orange peel coupling due to interfacial roughness

Comparison of XTEM results of the fabricated MTJ stack with the one from the literature indicated the possibility of interface roughness in the stack (Fig.5.18 and Fig. 5.19). Such roughness can cause magnetic coupling between the "free" and "pinned" layers known as Néel coupling or orange peel coupling shown in Fig. 4.5 and explained

with respect to bottom electrode requirement in section 4.2.1. This coupling field given by equation 4.1 tends to keep "free" and "pinned" layer in parallel and therefore, the applied magnetic field becomes ineffective.

2. Chemical Composition of MTJ stack layers

The PEELs plot showed the absence of Co in the free layer of the device. This might have many implications for the performance of the device. Though there seems to be the presence of Fe in the free layer, the presence of B would change its phase and may not have the same interfacial properties with MgO. As summarized in Table 5.3, the FM electrodes for MgO-based MTJ devices need to be Co rich for having matched crystalline interface with the tunnel barrier. Additionally, as shown in PEELS analysis in Fig. 5.20, diffusion of Ru in free layer also can make the layer more "non-magnetic" to degrade the performance of MTJ.

The presence of B in MgO is due to the diffusion of B from the FM electrodes during annealing step. This might change the properties of MgO as tunneling barrier. This change may be in phase or band structure which would eventually affect the magnetic response of the device. Similarly, the presence of Fe in MgO would also have the similar effect.

3. Insufficient field annealing of MTJ stack

In the current work, the MTJ devices are field annealed at 355°C for 2 hours in 5 KOe of magnetic field. This annealing step as explained in earlier chapters is important for crystallization of CoFeB electrode for getting matched interface with MgO and, in turn, high TMR response. CoFeB is expected to get crystallized to (001) orientation for this.

The XRD study of the given MTJ stack with in situ annealing shows that the temperature at which the peak corresponding to this orientation appears is at 400°C and not at 350°C. This suggests that the CoFeB might not have got crystallized with the annealing step carried out and therefore the absence of any noticeable magnetic response.

Chapter 7

Conclusions and Future Work

The work presented here started with an aim of integrating CoFeB/MgO-based MTJ device on silicon and it has been achieved with a significant success. Various process issues related to this integration are identified and solutions are implemented as summarized in Table 7.1.

Table. 7.1 Process issues identified and corresponding solutions implemented for integrating MTJ on silicon

Process Issue	**Solution**
Smooth bottom electrode material/patterning	Ta and NiCr-based bottom electrode process are developed with Ta identified as a promising candidate (Section 4.2.1)
Low temperature low-k Inter Level Dielectric (ILD)	Spin on Glass (SOG) based process is developed with material deposition, baking and curing (Section 4.2.3)
Low temperature, low reactive photoresist stripping	Low power, low reactive RIE-based oxygen plasma process is developed and use of the existing PRS-2000 solvent stripper. (Section 4.2.4)
MTJ patterning with ion-milling with vertical side walls and without re-deposition	Dual angle scheme with low angle (10°) to start with followed by higher angle (50°) (Section 4.2.5)

Various corroborative experiments are conducted to assess these solutions and also to get insight into process and device design. The salient achievements with these experiments are:

- Surface morphology in terms of roughness and grain size of thin metallic films as a function of sputtering parameters is understood with Design of Experiments (DOE) approach undertaken for NiCr. This approach can be used

for assessing any material as a candidate to be used as bottom electrode for MTJ and optimizing deposition conditions for the same.

- XRD study on MTJ stack with in-situ annealing to understand the crystallization of CoFeB helped in determining the optimum temperature range at which the annealing of the stack should be carried out to have this phase transformation of CoFeB. Since this process is also intimately related to the characteristics of the MTJ stack layers, it can be used for designing optimum MTJ device.
- STEM of MTJ stack with PEELs analysis gave insight into the MTJ stack composition after the process. The interfacial change and the phase of different thin layers in MTJ stack, whether they are amorphous or crystalline, can also be observed with this measurement.

Overall, with the process development and the corroborative experiments, this research on MTJ device integration at RIT is in a position from where it can be very well taken further for the future development of MTJ based devices and systems such as MRAM.

Recommendations for Future Work

Any work, however meticulously done, always keeps some room for improvement. This research work is no exception. In fact, these efforts have given a clear direction to the future developmental work that should be undertaken to develop spintronic devices.

The device can be redesigned to make it high performing, reliable and robust to the developed process with enough latitude in the process parameters. The steps for achieving that are as follows:

1. CoFeB/MgO/CoFeB MTJ structure optimization.

The importance of MgO thickness for necessary crystallization of CoFeB layers to the preferred bcc (001) orientation has been explained in Chapter 5. A controlled experiment using XRD and in-situ annealing for studying the effect of various MgO thicknesses can be done to finalize this stack. The author suggests multiple levels of CoFeB/MgO stack as shown in Fig 7.1 deposited on at least three wafers having different MgO thicknesses(>1nm but < 2nm) each. The composition and thickness of CoFeB should be kept same for all the wafers. XRD of as deposited films should be obtained with identification of the peaks and then the samples should be annealed in steps from 300 °C onwards for 1 hour in N_2. The step in temperature could be at the most 25 °C and the highest temperature of the annealing may not go beyond 450 °C. The XRD measurements at each step should be taken and the peaks corresponding to CoFeB phases should be identified. The occurrence of CoFeB (002) peak as shown in Fig. 5.16 should be noted and the corresponding temperature should be considered to be the upper limit for annealing. Once the temperature range is found, the annealing could be done in smaller intervals of temperature from the immediate lower step of the limit found earlier. For example, if the upper-limit is 400 °C and 25 °C is the interval then the optimum temperature can be determined between 375 and 400 °C by taking smaller temperature steps. If possible, HRTEM and PEELs study should be done to verify that the CoFeB is crystallizing preferentially at the CoFeB/MgO interface and the boron diffusion into

MgO is minimal. The crystallization of CoFeB can also be studied by electron beam diffraction during these measurements.

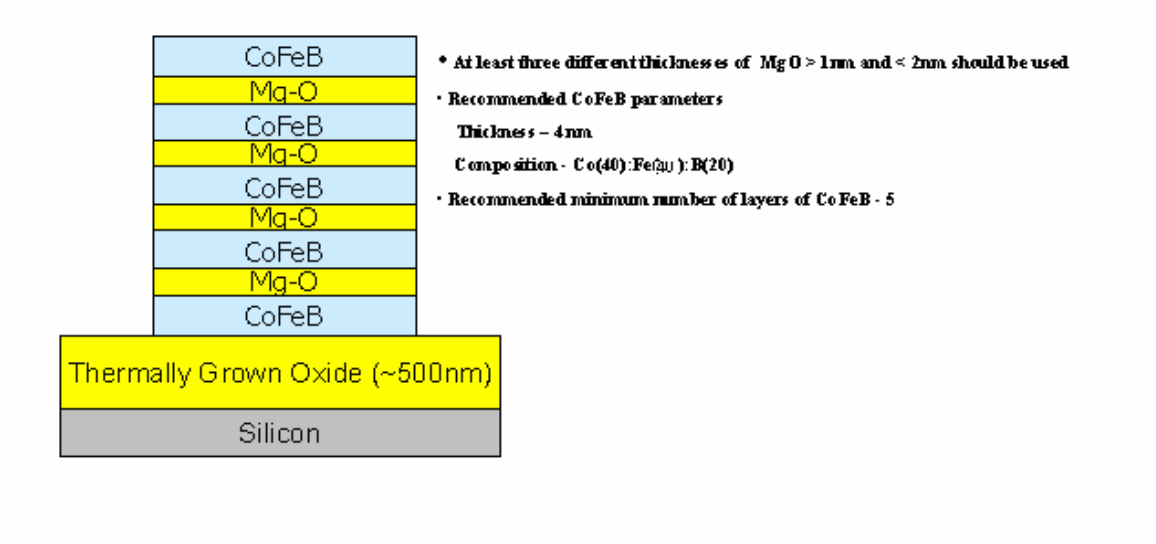


Fig. 7.1 Recommended film stack for optimizing MgO thickness and annealing temperature for MTJ

2. Adjacent layers and bottom electrode design

The adjacent layers of CoFeB/MgO/CoFeB play an equally important role in its performance [61]. As mentioned earlier, a cap layer is required in order to protect MTJ structure from oxidation and other damage. Ru is used in the present study with 7 nm thickness and may be continued to be used. It is author's opinion that an additional small layer of Ta would make it more robust since apart from Ta being refractory metal, it would have reliable contact with Al top electrode and can act as good "mask" during contact cut etching to protect the underlying layers.

At the bottom, below the reference layer, the author would recommend Synthetic Antiferromagnet (SAF) layer with CoFeB/Ru/CoFe sandwich and the current design can be re-used for the same. But, instead of unbiased pinned layer, biased pinned layer by

exchange coupling with natural antiferromagnet would give superior pinning of the reference layer. As discussed in Chapter 3, among the various material options for the antiferromagnet, PtMn has the best thermal endurance [42]. Therefore, PtMn layer in 5-10 nm range of thickness is recommended below CoFe of the SAF sandwich. The magnetic buffer layer of NiFeCr as is there in the current design could be used below the antiferromagnetic layer.

Ta as bottom electrode used in this work has shown to have good film properties and, in turn, the interface integrity of the upper magnetic layers in the stack is maintained. On the basis recent literature [33] [62], a slightly modified stack with Ta/Ru/Ta sandwich as seed layer has shown better surface roughness and interface properties.

On the basis of all the considerations mentioned above, the recommended stack is shown in Fig. 7.2. For some of the layers, the recommended range of thicknesses has been given. This stack should be deposited after the usual bottom electrode deposition and patterning process (step no. 13 from Table 4.11).

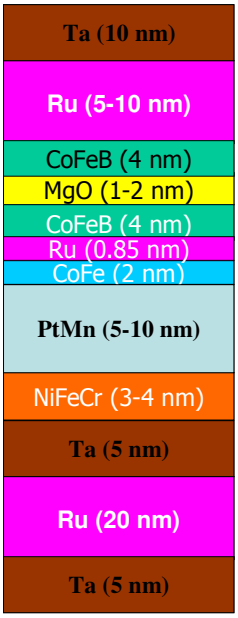


Fig. 7.2 Recommended MTJ stack for future development

3. ILD process optimization and improvement

In this study, SOG based ILD process has been developed. The low temperature curing process developed for this work is furnace-based. Though this technique is simple and gives reasonable characteristics of ILD, it would be better if more sophisticated techniques mentioned in Table 4.6 can be used. These include e-beam and laser annealing. It has been shown experimentally that these techniques, especially e-beam curing [70][71], are not only low temperature (< 200 °C) but also give much better properties of ILD which would be required when designing high density MTJ-based MRAM arrays.

During contact cut etching through ILD, if only dry etching is used, then there is possibility of over-etching which would damage the top Ru surface as mentioned in Chapter 4. Though additional Ta top layer would give more process latitude, reliable end point detection during contact cut etching would be beneficial for the process.

4. MTJ patterning with RIE

Currently MTJ films are patterned by ion-milling process with dual angle scheme as explained in Chapter 4 for optimizing between sidewall angles and re-deposition. Ta hard mask is used during the patterning and it is also author's recommendation that it should be used for future developments.

When Ta or other refractory metal like Ti is used as a hard mask, CH_3OH-based RIE process can be used for MTJ patterning [72]. This process has shown promising results recently [73] with very good selectivity between mask materials (Ta/Ti) and magnetic materials (CoFe/NiFe). The Ta is patterned by CF_4 RIE process followed by CH_3OH RIE. This process does not have tradeoffs in ion-milling process. The author

recommends the future developers to explore this process as an alternative to ion-milling process.

The future of MTJ based MRAM is quite promising and this research work, though a small step, contributes in going near to the ultimate goal of realizing high performance memory based on MTJ.

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Appendix A: Test Chip Design