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Embedded charge for microswitch applications

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Embedded Charge for Microswitch Applications

By

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Abstract

In this work a micro-electro-mechanical system (MEMS) is proposed for radio frequency (RF) switching applications. MEMS devices outperform the traditionally used solid-state devices in areas such as isolation, insertion loss, and linearity. However, micro switches suffer from high actuation voltage, lifetime limitations, and high packaging cost. A novel micro switch design that incorporates embedded charge in a cantilever structure can, in principle, enable low-voltage operation. This was the primary motivation for this study.

The experiments in this investigation explored charge injection and retention in a tri-layer oxide/nitride/oxide (ONO) stack capacitor. High-field injection was used to place charge within the dielectric stack. Capacitance-voltage (C-V) measurements were performed to quantify the effective amount of charge stored. The stability of the trapped charge was studied using elevated temperatures, indicating a room-temperature storage lifetime of several years.

A fabrication process for a free-standing film stack membrane was also developed. The process was designed to be post-charge-injection, and therefore was required to adhere to low thermal budget constrains. A masking process for deep reactiveion etching (DRIE) was established using a thick photoresist process (AZ 9260, t_{PR}=10µm). The fully released ONO stack proved to be mechanically robust: no damage to diaphragms was observed during subsequent processing and handling.

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CHAPTER ONE: INTRODUCTION

1.1 Introduction

This work introduces a concept, which can address the needs of the telecommunication industry and has a potential to advance other fields such as alternative energy sources. The concept is based on the nonvolatile memory technology where charge is embedded into a dielectric film stack using a high electric field. An electret film is created as a result of this charge injection. The electret film is then released to form a freestanding beam, whose position is controlled with integrated metal electrodes. Such a structure is a member of a group of devices known as microelectromechanical system (MEMS). The primary focus of this work is on radio frequency (RF) switching applications. The proposed design may outperform existing technologies in areas such as actuation voltage and packaging cost. This work provides background information on the subject of RF switches, MEMS, the nonvolatile memory technology and electrets. This is followed by a discussion of design and fabrication of microstructure and is accompanied by experimental results.

1.2 RF MEMS in Telecommunication

The financial news journal "Microwaves & RF" reports on a study conducted by a German-based firm Wicht Technologies Consulting [1]. The study predicts a large market growth for radio frequency microelectromechanical systems (RF MEMS) that will reach more than $1 billion by 2007. Some of the applications of RF MEMS include third

generation mobile phones, global positioning systems, and wireless local area networks. One specific application example for RF MEMS is in satellites and radar systems, where they are used in directional antennas. RF switches in conjunction with delay line banks allow steering of the radiated beam of electro-magnetic energy with no need to physically move the antenna. This is accomplished by introducing phase shifts in the signal path to individual radiating elements in an antenna array. The phase shifts provide constructive interference in the desired direction and destructive interference in all other directions. In such systems, RF switches are used to select delay lines corresponding to various degrees of phase shift at the carrier frequency. For example, Figure1.1 shows a three-bit phase shifter, based on 45º/90º/180º set of delay networks, which allow phase shifts of 0º, 45º, 90º, 135º, 225º, 270º and 315º, depending on the combination of the bits used [2].

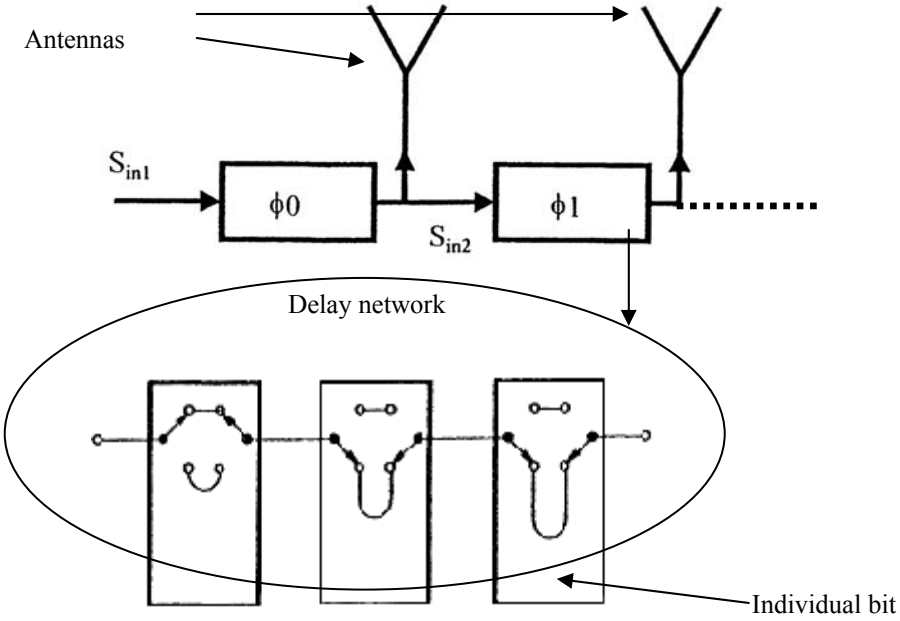

Figure 1.1: Signal transmission diagram: (a) system level view of phased-array antennas (b) switched–line implementation [2].

This approach is more reliable and more cost effective compared to a mechanical antenna. More importantly, it allows for rapid time division multiplexing, which is essential in many multi-user systems including cellular networks.

Other types of phase shifters are constructed using solid-state devices such as PIN diodes and FETs. They offer good performance at frequencies up to around 5-20 GHz and switching time as low as 1 ns depending on the size of the device and the required RF power handling. However, at higher frequencies around 30-100 GHz their performance degrades due to signal losses in the solid-state devices [3]. Also, the fabrication cost of PIN and FET designs is high due to the need for compound semiconductors such as GaAs and InP. The use of compound semiconductors also complicates integration with other system components, driving the cost higher.

Compared to conventional solid-state solutions, RF MEMS structures offer performance benefits such as lower insertion loss, higher isolation, lower power consumption and higher linearity. In addition, they have a potential for integration and miniaturization into microsystems, and monolithic processing of MEMS and electronics on silicon substrate could lead to further cost reduction. Therefore, RF MEMS technology has been investigated as a viable replacement for solid-state components.

The insertion loss represents the amount of signal lost when the switch is turned on. Usually, the insertion loss increases with frequency due to the skin effect. The degree to which skin effect affects signal transmission depends on the frequency, permeability, and conductivity of a medium. At low frequencies the entire cross-sectional area of a conductor is used and no skin effect is present. As frequency increases, the center of the medium results in higher impedance causing greater flow of carries through the perimeter

of the medium [4]. Isolation is a measure of RF signal leakage for an open switch. Higher magnitude of the isolation parameter is desirable. Linearity is also an issue for solid-state devices, and it can be approximately two times lower compared to RF microswitches. Microswitches are intrinsically more linear than solid states devices due to their passive nature combined with 'on' and 'off' operation. Linearity is simply a measure of how well the frequency content of the output signal resembles that of the input signal, and it is represented by the third order intercept point (IP3) [5]. Higher values of IP3 signify better linearity.

1.3 Performance Comparison of FET, PIN Diode and RF MEMS

PIN diodes [6-7], have a relatively low insertion loss compared to FETs [8], but they consume more power and cannot be readily integrated with other electronics. MESFETs use less power but they are expensive to fabricate. Furthermore, their performance declines at high frequencies as a result of high insertion loss and very low isolation. Table 1.1 provides a general overview of the performance parameters related to RF MEMS, PIN diode, and FET switches.

	RF MEMS	PIN	FET
Voltage (V)	20-80	±3-5	3-5
Current (mA)	0	3-20	0
Power Consumption (mW)[a]	0.05-0.1	5-100	0.05-0.1
Switch time	1-300 μs	1-100 ns	1-100 ns
Cutoff frequency (THz)	20-80	1-4	0.5-2
Isolation (1-10)GHz	Very High	High	Medium
Isolation (10-40)GHz	Very High	Medium	Low
Isolation (60-100)GHz	High	Medium	None
Insertion loss (1-100Ghz) (dB)	.05-.2	0.3-1.2	0.4-2.5
IP3(dBm)	+66-80	+27-45	+27-45

Table 1.1: Comparison between properties of FET, PIN diode and MEMS RF switches [9].

Table 1.1 points out the high actuation potential, in the range of 20 to 80 V DC, for electrostatically actuated MEMS devices. This is a major obstacle, since additional high-voltage circuitry and a power source are required to operate these devices. However, from Table 1.1 it is also apparent that MEMS switches offer superior performance compared to solid-state devices in the areas of loss, isolation, IP3, and bandwidth. Therefore, fabricating MEMS switches with lower actuation potentials is an area of intensive research.

1.4 MEMS Technology Background

In 1959 Feynman introduced a new field of study known as system miniaturization. He concluded that the laws of physics do not limit miniaturization; rather, it was our ability to create miniature systems that was the limiting factor [10]. That decade Smith's discovery of the piezoresistance effect in germanium and silicon resulted in the fabrication of piezoresistive sensors for stress, strain, and pressure analysis [11]. In 1966 H.C. Nathanson and his colleagues were the first to monolithically integrate micromechanical structures with electronics using a silicon-based process [12].

Currently, a variety of sensors and actuators are available employing a number of actuation mechanisms. The most common mechanisms are piezoelectric, electrostatic, thermal, and electromagnetic. These methods are found in applications related to the automotive, medical, biotechnological, ink jet printing, magnetic data storage, digital image projection, and telecommunication industries. Each method has certain advantages and disadvantages, which determine its suitability for specific applications. The following section offers an overview of each actuation technique. The primary focus is on the

electrostatic method, and it will become apparent that it is best suited for switching of RF signals.

1.4.1 Electromagnetic Actuation

Electromagnetic actuation is based on the Lorentz force. By applying current through a long wire, which has been wound many times into a tightly packed coil, a magnetic field is established that is perpendicular to the plane of the wire loop as shown in Figure 1.2. Due to the magnetic field, the ferromagnetic cantilever and the rest of the structure become magnetized and the air gap between them is reduced. This provides a closed path for the magnetic flux to travel and lowers the beam. Once the current is turned off, the spring constant of the beam restores it to its original position.

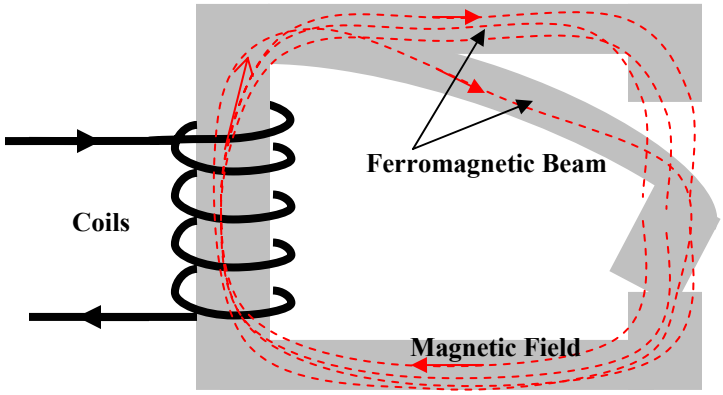

Figure 1.2: A cross section of electromagnetic actuator demonstrating the effect of magnetic flux.

Figure 1.3 shows a top view of a micro-electromagnetic switch. The three circular structures are pancake electromagnetic coils. The long and wide rectangular structure is a ferromagnetic cantilever beam, and the two squares are contact pads. The electromagnetic actuators offer large force and displacement. These electromagnetic actuators can produce forces into the milli Newton range, depending on the coil current.

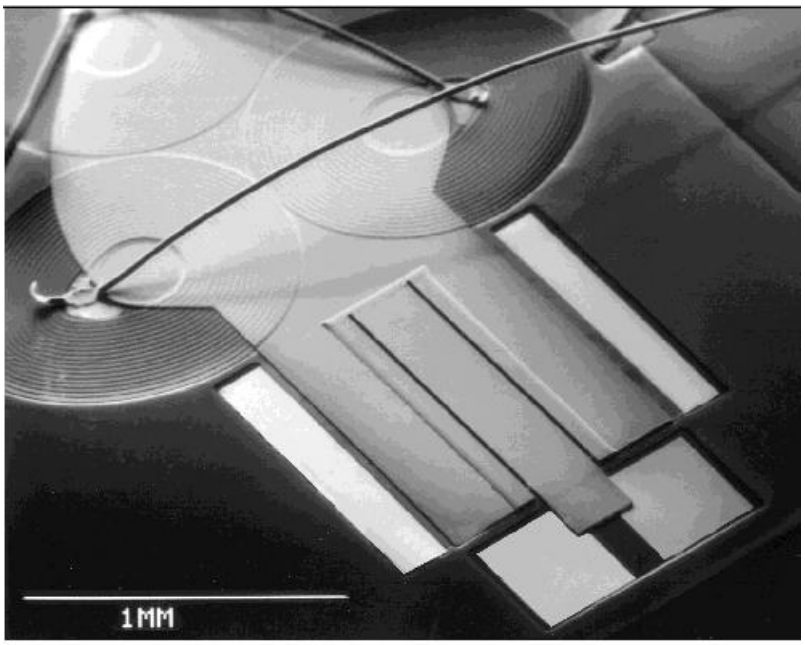

Figure 1. 3: Electromagnetic microswitch [13].

1.4.2 Thermal Actuation

There are various types of thermal actuators the most common of which are shape memory alloys (SMA) and bimorphs. The shape memory alloys are materials that have the ability to return to a predetermined shape when heated. They can be deformed when cooled. SMA materials like NiTi, CuZnAl, and CuAlNi experience two phases known as martensite and austenite in their solid state (see Figure 1.4). The martensite phase occurs at lower temperature. In that phase, the material becomes twinned and can be easily deformed. When the material is heated up, it transitions to the austenite phase. The atoms rearrange themselves to reach the minimum energy state and eventually lead to a shape change on a macroscopic scale. For most shape memory alloys a temperature change of only about 10°C to 20°C initiates the atomic rearrangement [14].

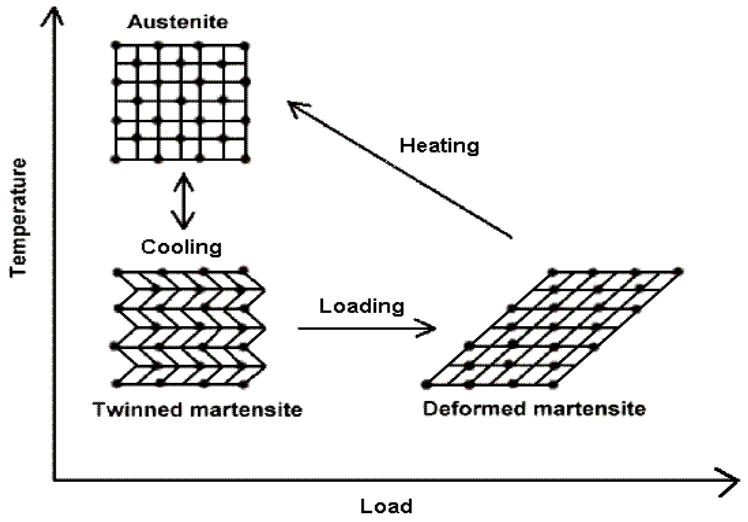

Figure 1.4: The martensite and austenite phases [15].

The bimorph effect is caused by thermal expansion of two materials. When the two materials are heated they expand laterally and unevenly due the mismatch in their linear coefficients of expansion. Since they are fused at their interface, elongation will induce a gradient stress across the bi-layer. As a result of the stress in the bi-layer the structure will bend. Once the temperature returns to its initial value, the beam returns to the equilibrium position. Bimorph actuators typically produce high actuation forces and appreciable deflection. Figure 1.5 shows an example of the bimorph valve made of nickel and silicon.

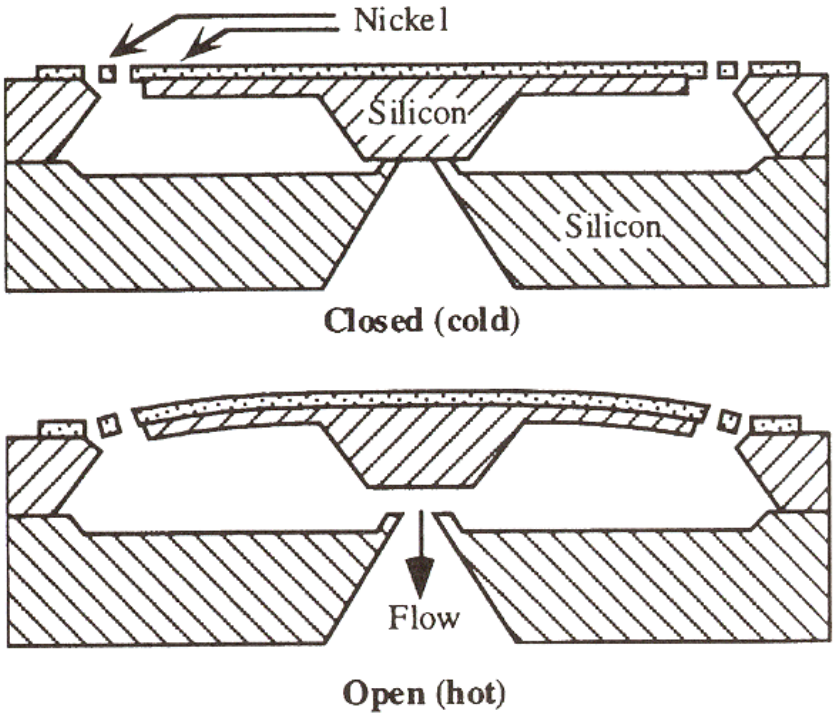

Figure 1.5: Cross section view of a bimorph valve at close and open position [16].

1.4.3 Piezoelectric Actuation

Piezoelectric devices convert mechanical force into induced voltage and vice versus. The piezoelectric effect occurs in certain dielectric crystals such as quartz. Quartz in its equilibrium state has no potential difference. Once pressure is applied to the crystal, its unit cell gets distorted as shown in the Figure 1.6. The distortion induces an electric polarization, and as a result all unit cells become electric dipoles creating a potential difference across a particular face of the crystal. The advantage of piezoelectric materials is that they directly convert mechanical forces such as pressure or vibration into electrical signals. Also, their response time is measured on the order of microseconds.

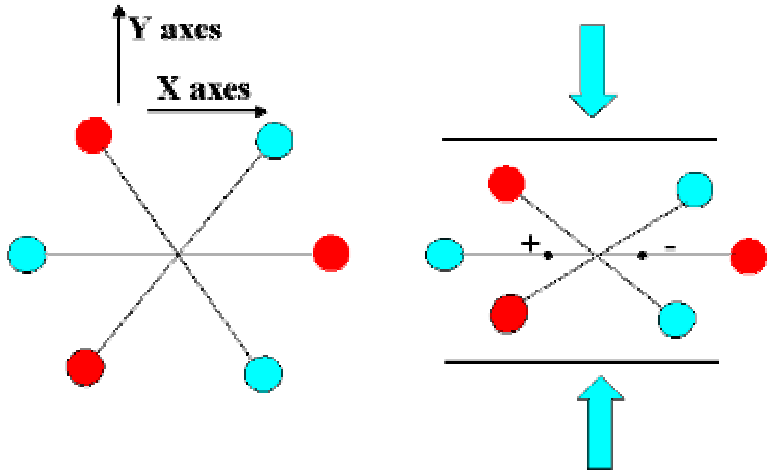

Figure 1.6: Piezoelectric Crystal Relaxed and under Compression [17].

There are typically used in situation involving dynamic strains of an oscillatory nature like micromotors, pumps and acoustic sensors. Piezoelectric devices usually made of exotic material like lead zirconate titanate (PZT) or lead magnesium niobate (PMN).

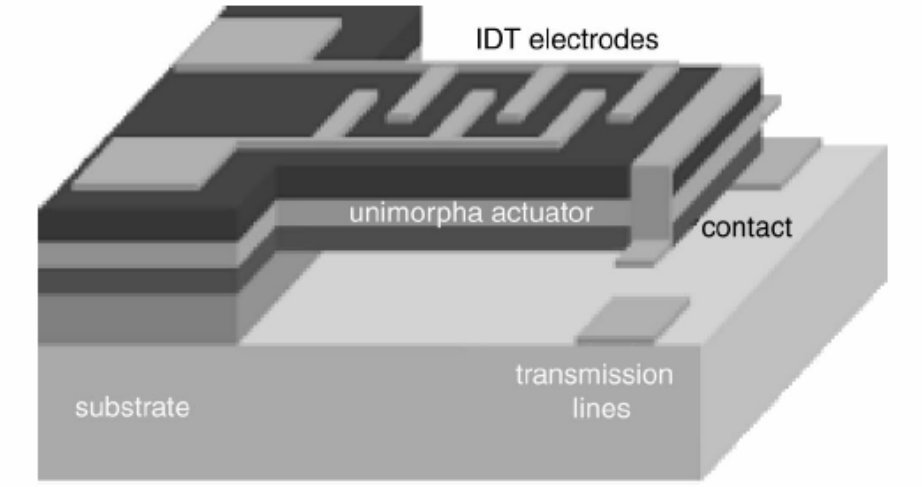

Figure1. 7: An example of piezoelectric microswitch [18].

1.4.4 Electrostatic Actuation

Electrostatic actuation is based on Coulomb's law of attraction between positive and negative charges. Consider a parallel plate capacitor with two constrained metal plates.

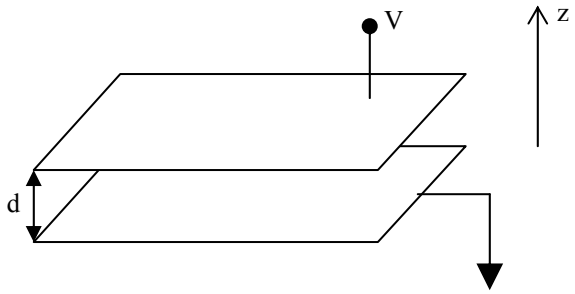

Figure 1.8: Parallel-plate capacitor.

Based on these assumptions, the capacitance in Figure 1.8 is defined as

$$C = \frac{Q}{V} = \frac{\varepsilon A}{d} \qquad \textbf{(1.1)}$$

where Q represents the charge magnitude on each plate, V is the potential difference, ε is the permitivity of the dielectric in the space between the plates, d is the distance separating the plates, and A is the area of each plate. The electrostatic energy U stored in the capacitor is defined as

$$U = \frac{1}{2} C V^2 \qquad \textbf{(1.2)}$$

The force between the two plates is governed by Eq.1.3.

$$F = -\frac{\partial U}{\partial z} \qquad \textbf{(1.3)}$$

where F denotes the electrostatic force between the two parallel plates, and the potential energy is differentiated with respect to the motion in the z direction. Substituting Eq. 1.1

and Eq.1.2 into Eq.1.3, an expression for the force can be derived for this system, as shown in Eq. 1.4.

$$F = \frac{\varepsilon A V^2}{2z^2} \tag{1.4}$$

This equation applies only if the gap between the two plates is much smaller than the area of the two plates, such that the fringing fields can be ignored. Also, it is assumed that the electric field is constant.

Various design geometries of electrostatic actuators are possible, such as cantilevers [19], motors [20], and comb drives [21]. Their popularity stems from their low power consumption, fast response, and ability to be integrated with solid-state devices. One example of an electrostatic actuator is a three terminal microswitch shown in Figure 1.9. The cantilever is made of metal and is connected to the source pad. Signal is passed from source to drain once the switch is lowered, and the contact tip touches the drain. The gate pad controls the motion of the beam [19].

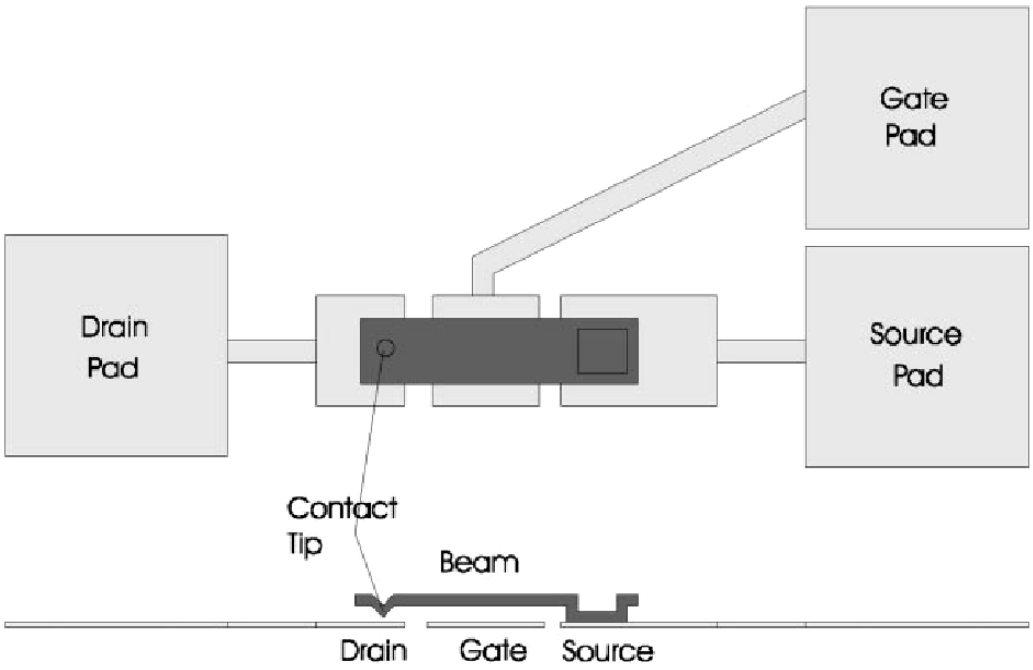

Figure 1.9: A top view and cross section view of an electrostatic Switch [19].

1.4.5 Summary of the Actuation Mechanisms

Currently, microswitch designs implement electrostatic [19], thermal [22], electromagnetic [13] and piezoelectric [23] actuation mechanisms. However, electrostatic actuation is the most prevalent technique at present time. This is due to its low power consumption, which is approximately zero at steady state conditions, as well as small electrode size and short switching time. Table 1.2 summarizes some of the important performance aspects of these different actuation mechanisms.

	Voltage (V)	Current (mA)	Switching time (μs)	Power (mW)	Size
Electrostatic	20-80	0	0	1-200	Small
Thermal	3-5	5-100	0-200	300-10,000	Large
Magnetostatic	3-5	20-150	0-100	300-1,000	Medium
Piezoelectric	3-20	0	0	50-500	Medium

Table 1.2: Performance summary of different actuation mechanisms [9].

For example, thermal actuators are capable of large deflections. Their performance is based on how quickly they can heat up and cool down. Therefore, heat dissipation limits their response time. Typical speeds range between 1 kHz and 10 kHz. They are also power inefficient due to Joule heating [24].

Piezoelectric actuators are capable of response time in the range of low MHz, which is comparable to electrostatic devices [25]. Unfortunately, they offer very small displacement. For example, a high stress of 35 MPa generates a strain of only about 0.1% [18]. Also, in most cases they require deposition of exotic ceramics such as lead-zirconate-titanate, which raises manufacturing costs.

Electromagnetic actuators are capable of generating large forces, but they cannot be easily miniaturized. Also, they are power inefficient compared to electrostatic devices. Manufacturing of electromagnetic actuators is more complicated due to the structure of

the magnetic windings and the metallic core. As in case of piezoelectric films, ferromagnetic materials are not commonly used in IC integrated circuits, which contributes to higher fabrication cost.

1.5 Electrostatic Microswitches

Electrostatic microswitches are categorized by the type of signal coupling and by their configuration in a circuit. There are two types of signal coupling: capacitive and resistive. A resistive switch, also referred to as DC-contact switch [3], operates via direct metal-to-metal contact. It consists of two discontinuous signal lines and a movable cantilever beam. The cantilever has a metal contact that closes the circuit when it is lowered (refer to Figure 1.10). The ohmic contact between the metals allows direct current (DC) as well as high frequency signals to pass. Broadband signal capability is a great advantage of this technology. The shortcomings include limited lifetime of metal contacts. Figure 1.10 shows an example of a resistive RF microswitch designed and manufactured by Motorola.

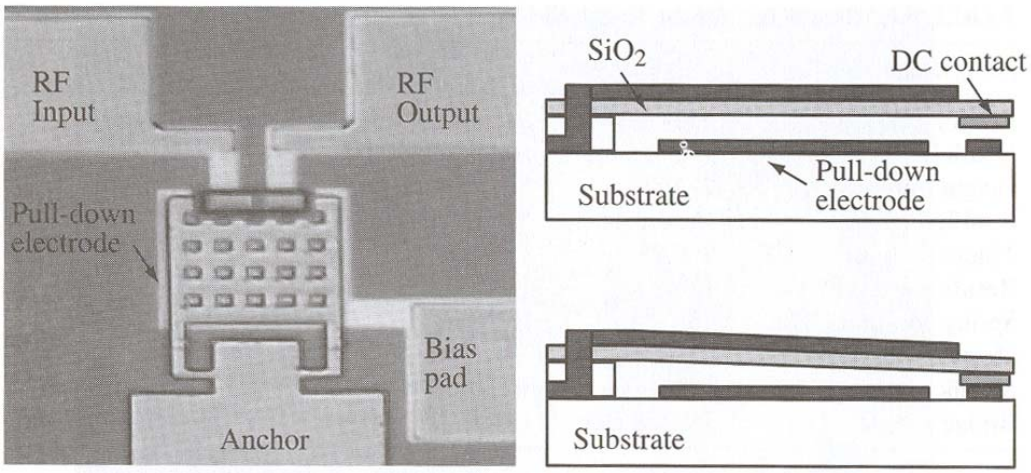

Figure 1.10: Resistive RF Micro Switch [27].

A capacitive switch has a dielectric material and an air gap separating the cantilever and the bottom electrode. The air gap varies as the beam is actuated, which leads to changes in the capacitance between the signal line and the bottom electrode. In a shunt configuration, a large capacitance shunts the signal to ground at high frequencies while a small capacitance allows most of the signal to pass. The advantage of the capacitive switch is longer device lifetime, since there is no contact surface degradation. Capacitive switches can last five to ten times longer then resistive switches [4,8], but they lack low frequency capability. Figure 1.11 shows an example of a capacitive switch designed by Goldsmith et al [28].

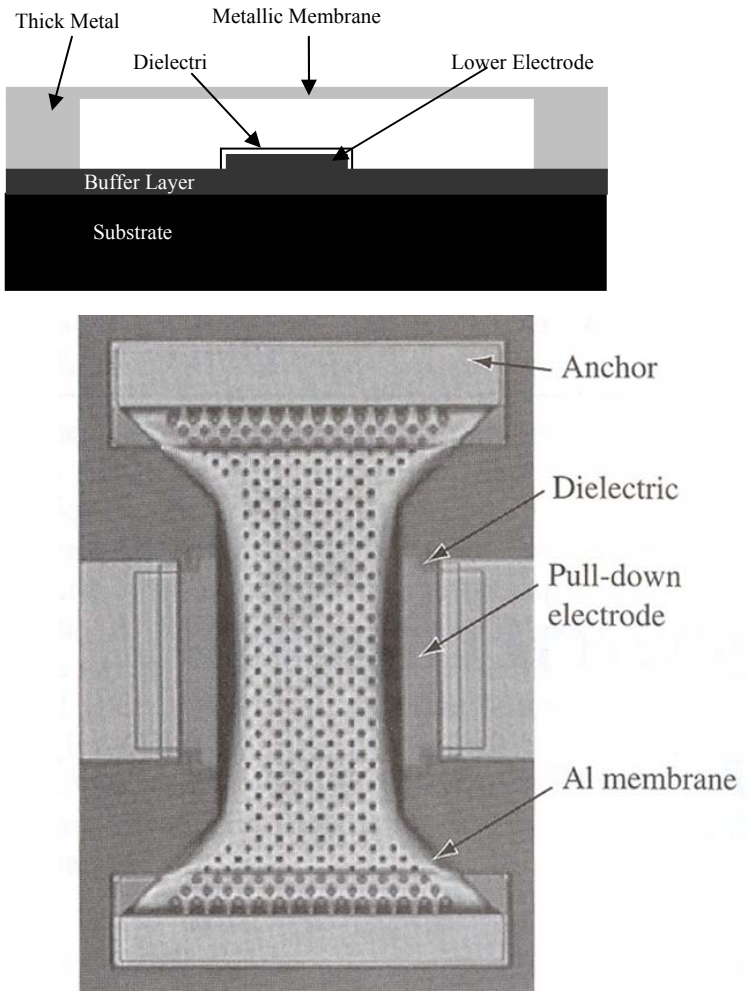

Figure 1.11: Cross section and top view of a capacitive RF Micro Switch [28].

Either a resistive or a capacitive microswitch can be connected in a shunt or in a series configuration with the signal line. As illustrated in Figure 1.12, in the series configuration the switch needs to be 'on' for the signal to pass, and in the shunt configuration the switch needs to be 'off' for the signal to pass. Figure 1.10 shows an example of the series configuration and Figure 1.11 illustrates the shunt configuration.

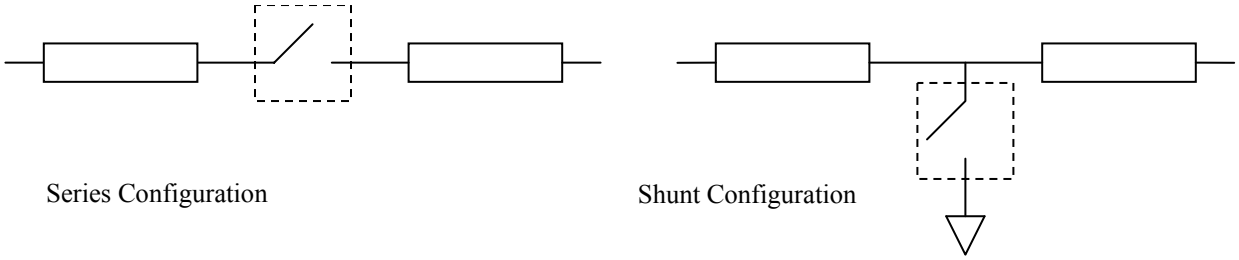

Figure 1.12: Two possible configurations of a microswitch with a circuit

1.6 Challenges of MEMS

MEMS devices such as the electrostatic microswitch offer many benefits including no static power consumption, low signal losses and small size (compared to the currently used solid-state devices). Their primary drawback is the need for high actuation voltage. Other challenges include life cycle, packaging, and final unit manufacturing cost. Lifetimes of MEMS switches are shorter compared to solid-state devices, which can withstand over 100 billions cycles. In case of resistive switches an abrupt failure occurs after about 10 million cycles for hot switching (assuming 40mA signal current) and nearly 100 millions cycles for cold switching [26]. Hot switching refers to opening and closing of a switch with a signal passing through the contact and often through a specified load. Cold switching refers to switching without any signal

applied to the electrodes. The major failure mechanism for resistive switches is the degradation of the contacts. The contacts become pitted and harden due to the impact force during switching. Also, environmental contamination of the contacts reduces their performance. Some capacitive switches have exceeded a 1 billion-cycle mark [4]. In case of a capacitive switch, stiction is the major failure mechanism. Stiction is the undesirable tendency of small parts to adhere to one another. There are several causes for this unwanted adhesion including contamination, friction, Coulombic attraction, capillary action, and van der Waals forces. Also, charge injection into the dielectric, which can occur during the operation of a capacitive switch, is a problem. Depending on the polarity of the injected charge, the beam can either stick or result in an increased actuation voltage. Packaging and unit price are the greatest challenges of today's MEMS technology. Even if the device processing cost is low, the packaging can account for 60% to 90% of the total cost of a MEMS product [6]. Currently, MEMS packaging is done using epoxy glass, glass-to-glass anodic bonding or gold-to-gold bonding. A drawback of the epoxy glass is the outgassing of the sealing material. Another problem is the high temperature of 300-400°C required for the sealing process, which can affect microswitch properties and cause a premature device failure [4].

1.7 Motivation

The proposed electrostatic microswitch offers a possible solution to the issues of high actuation voltage and device packaging by utilizing embedded charge technology and self-packaging of the device. Using embedding charge to create electrets in MEMS is not a new idea, but creating electrets by applying the same technology used to

fabricatenonvolatile memory is quite novel, and it offers endless possibilities for RF switches and other MEMS applications. As mentioned earlier, an electret is a device which can retain electric charge for some amount of time.

The primary difference between the proposed design and the current designs for electrostatic RF microswitch is the charged cantilever. The charge embedded in the cantilever allows control of the deflection of the beam by an external voltage. When a voltage is applied between electrodes, the beam becomes attracted toward the lower electrode and closes the switch gap with the contact, allowing a signal to pass through. By reversing the polarity, the beam will repel the charged cantilever opening the switch (Refer to Figure 1.13).

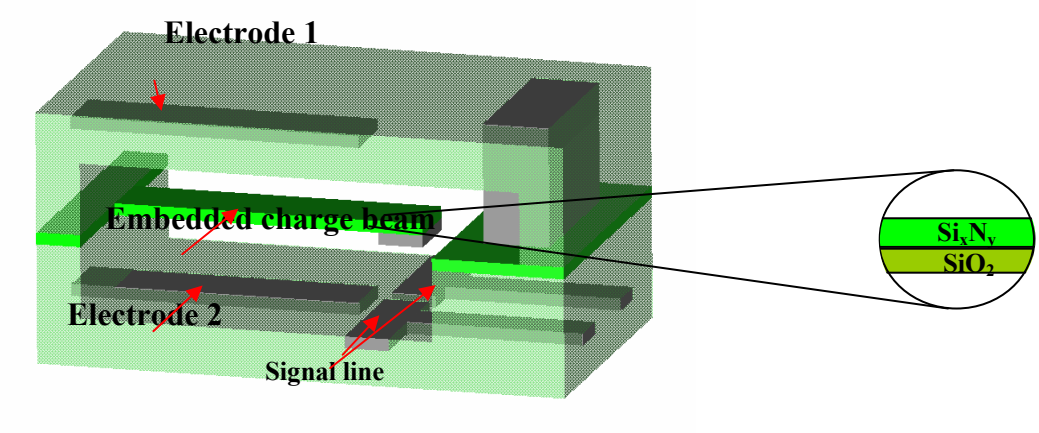

Figure 1.13: MEMS switch based on embedded charge concept using a bi-layer film stack for the cantilever.

The benefits of this device address some of the issues related to MEMS technology. For instance, by using standard CMOS fabrication materials such as SiO_2 and Si_xN_y integration and low cost manufacturing are possible. Also, the device is designed to be self-packaged within a hermetically sealed chamber created during fabrication. The embedded charge switch also offers good control over the beam position, which mitigates

the effects of stiction. Most importantly, the device will actuate at lower voltages compared to the present day MEMS devices.

1.8 Thesis Overview

This thesis consists of four main parts: background, theory of the design, manufacturing of the device and study of high field charge injection. Chapter 1 examines current designs of microswitches. It explains the motivation for the work presented here. Topics such as electrets and nonvolatile memory devices are described in Chapter 2. Also, background information about charge transport mechanisms is provided in this chapter.

Chapter 3 provides the results of the high field charge injection experiments. Chapter 4 focuses on the theoretical analysis of the performance of the electret device. Chapter 5 presents processing details related to the fabrication and the final testing of the device. Chapter 6 concludes this work, summarizes the key findings, and provides recommendations for future work.

References

1. "RF MEMS Market To Top $1B by '07," MRF Microwaves & RF v. 41, no. 12, (2002), pg. 40

2. Hector J. De Los Santos, "Introduction to Microelectromechanical (MEM) Microwave Systems" Artech House ,Boston London, 1999, pg 166-168

3. Gabriel M. Rebeiz ,"RF MEMS theory, design and technology" John Wiley & Sons NJ, 2003, pg 259-262

4. Chris Bowick, "RF Circuit Design", Boston: Newnes, 1982. ,pg 9

5. J. Jason Yao, "RF MEMS from a device perspective Topical review " J. Micromech. Microeng. 10(200) pg R9-R38 printed in UK

6. Bill Doherty, "Pin Diode Fundamentals" MicroNotes Series 701, Microsemi Watertown

7. Robert Pierret, "Semiconductor Devices Fundamentals" Addison Wesley 1996, pg 278

8. Samuel Y. Liao, "Microwave Devices and Circuits", Second edition. Prentice Hall, 1985, pg329-332

9. Gabriel M.Rebeiz, "RF MEMS Theory, Design and Technology", 2003, John Wiley & Sons, pg 4-5

10. Richard P. Fynman,"There's Plenty of Room at the Bottom" presented at the American Physical Socielty Meeting in Pasadena,CA December 1959; J. Microelectromechanical Systems, Vol.2, 1992, pp 60-66

11. Charles H. Smith "Piezoresistance Effect in Germanium and Silicon",Phys. Rev. V94 No1, 1954, pg42-49

12. Harvey C. Nathanson, William E. Newell, Robert A. Wickstrom and John Ransford Davis , "The Resonant Gate Tranisistor" IEEE Transactions on Electron Devices, Vol ED-14, No3, 1967, pg117-133

13. John A. Wrigth and Yu-Chong Tai, "Micro-Minature Electromagantice Switches Fabricated Using MEMS technology, " Proceeding: 46th Annual International Relay Confrence: NARM '98, Oak Brook, Illinois, 1998, pp13-1 to 13-4

14. Marc J. Madou, "Fundamentals of Microfabrication: the science of miniaturization " 2nd Edition, CRC Press LLC NY,2002, pg 591-593

15. http://www.cs.ualberta.ca/~database/MEMS/sma_mems/sma.html SMA/MEMS Research Group, Aug 17, 2001

16. Marc J. Madou, "Fundamentals of Microfabrication, The science of miniaturization", CRC Press LLC, 2002, pg 545-546

17. http://www.tedlind.net/Piezoelectricity.htm Theodore Lind Nov. 24 2000

18. S. J. Gross, S. Tadigadapa, T. N. Jackson, S. Trolier-McKinstry, and Q. Q. Zhang," Lead-zirconate-titanate-based piezoelectric micromachined switch", Applied Physics Letters Vol 83(1) pp. 174-176. July 7, 2003

19. Zavracky, PM., S. Majumder, and N.E. McGruer, "Micromechanical Switches Fabricated Using Nickel Surface Micromachining," J. Microelectromechanical Syst. Vol. 6, 1997, pp.3-9.

20. W.S.N. Timmer and K.J. Gabriel "Design Considerations for a Practical Electrostatic Micro-Motor", Sensor& Actuator Application, vol. 11,pg 189-206 ,1987

21. W.C.K. Tang, "Electrostatic comb drive levitation and control method." Journal of Microelectromechanical Systems, vol. 1, no. 4, 1992.

22. Girbau, D.; Lazaro, A.; Pradell, L,"RF MEMS switches based on the buckle-beam thermal actuator"Microwave Conference, 2003. 33rd European , Vol. 2 , 7-9 Oct. 2003 pg651 - 654

23. Gross, S.J.; Zhang, Q.Q.; Trolier-McKinstry, S.; Tadigadapa, S.; Jackson, T.N "RF MEMS piezoelectric switch"Device Research Conference,June 2003 pg99 – 100

24. Hector J. De Los Santos, "Introduction to Microelectromechanical (MEM) Microwave Systems" Artech House ,Boston London, 1999, pg 26

25. Patrick Johnston, "Free response of piezoelectric crystals in series and in parallel" NASA Langley Research Center, Dec 2003

26. E. A. Sovero, R. Mihailovich, D.S. Deakin, J..A. Higgins, J. J. Yao, J. F. DeNatale and J. H. Hong, "Monolithic GaAs PHEMT MMICs Intergrated with High Performance MEMS Microrelays", SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference Proceedings 1999 p 257-260

27. Gabriel M. Rebeiz ,"RF MEMS theory, design and technology" John Wiley & Sons NJ, 2003, pg 133-134

28. Charles L. Goldsmith Shimino Yao, Susan Eshelman and David Denniston, "Performance of Low Loss RF MEMS Capacitive Switch", IEEE Microwave ands guide wave letters Vol 8, No 8, August 1998,pg269-71

CHAPTER TWO: CHARGE WITHIN INSULATORS

2.1 Introduction

The proposed design of the RF microswitch is comprised of a free-standing electret. The electret is created with oxide and nitride film stack employing the same charge embedding technique, which is commonly used in fabrication of nonvolatile memory devices. In the following chapter some background information is provided on electrets, nonvolatile memory technology, and charge transport mechanisms to facilitate better understanding of the design, fabrication, and operation of the proposed RF microswitch.

2.2 Electrets

Dielectric materials, which retain electric charge for a period of time are referred to as electrets [1]. One of the early applications of electrets was in audio microphones. Currently, a variety of materials are available for creating electrets and they address a broad range of applications. A few examples include a polymer electret, a photo-sensitive electret, and a piezo-ceramic electret. Some of the typical applications of electrets include converting mechanical motion into electricity [1], which is the principle used in audio microphones and will likely find use in nano-scale energy harvesting devices. Other areas where electrets have been used with considerable success include filtering of contaminates [2], lubrication, protective coatings, or as a sealing material [3]. They are also found in the biomedical industry [4].

The first electrets were demonstrated in 1919 by Eguchi [5]. They were produced by melting a mixture of carnauba wax, rosin, and bee's wax and cooling it under a static electric field until it solidified. Such electrets were shown to retain the charge at their initial value (10^{-5} -10^{-4} C/m^2) for three years [5]. Eguchi's technique of making electrets is referred to as thermal heating. This process offers great stability not only on the surface but throughout the bulk of the dielectric, and can be even applied to some non-polar materials like Teflon. The drawbacks of this method are non-uniformity of the lateral charge distribution and the charging speed. There are other techniques of charging and polarizing of organic and inorganic dielectric materials such as contact electrification, which occurs when two dielectrics in contact with each other are in motion relative to each other. Rubbing of two plastic rods is an example of contact electrification. The charging occurs due to electron transfer from one insulator to another. This technique of charging is not popular due to the lack of accurate reproducibility.

Isothermal charging is yet another technique, that depends on electron discharge through an air gap, commonly known as corona charging. The advantages of this method lie in simplicity of the set up and the charging speed. The primary drawback is a large lateral non-uniformity if a special grid electrode is not used.

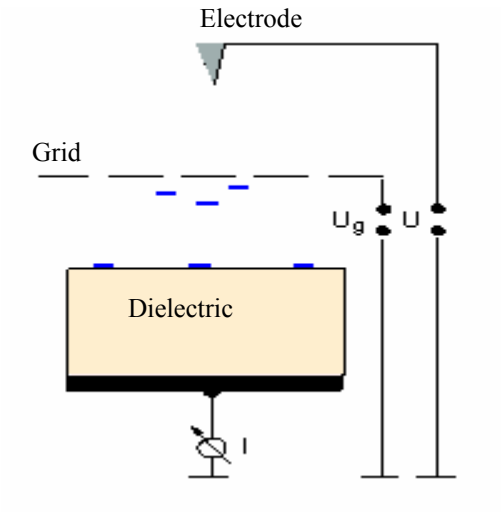

Figure 2.1: Schematic representing corona charging system

Another charging method is based on electron beam injection. As an electron beam strikes the surface, the electrons penetrate the material while scattering within the sample. During the penetration secondary (SE) and backscatter (BS) electrons are generated as shown in Figure 2.2. The secondary electrons exhibit a relatively small energy of 50eV [6]. Some of the secondary electrons escape from the sample and some are trapped close to the surface while all of the backscatter electrons escape from the sample. Due to scattering, the primary electrons (PE) slow down enough to become trapped, resulting in a negatively charged dielectric. The electron beam technique offers a reasonable degree of control over the lateral charge distribution by controlling the energy of the injected electrons via the applied electric potential. Both electron beam and isothermal charging are some of the most popular techniques used for producing electrets [7].

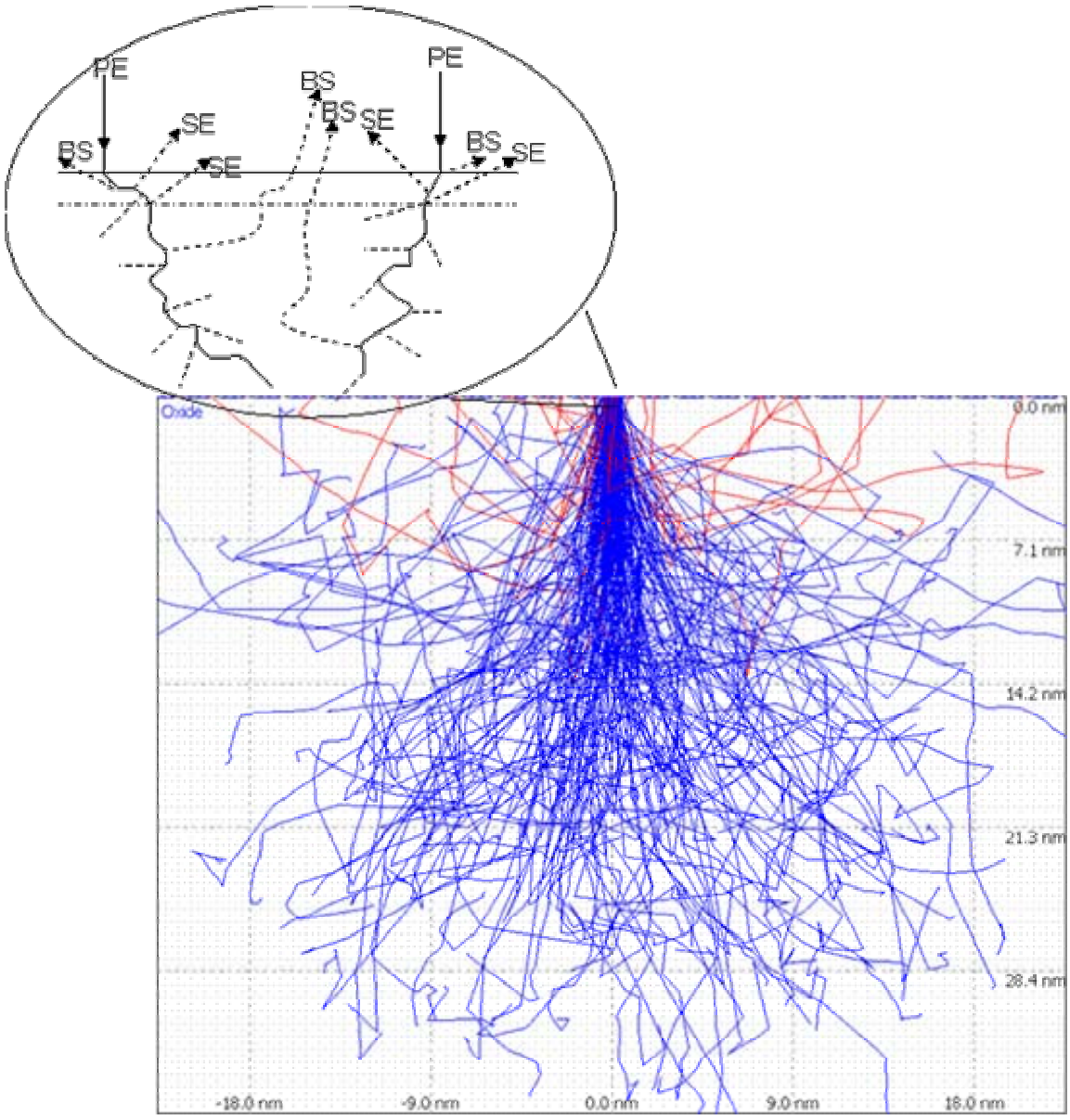

Figure 2.2: Illustration of electron penetration within 1000Å of oxide film using Casino v 2.42 program. The e-beam potential was 1kV, and the beam diameter was 1nm.

2.3 Nonvolatile Memory

The first nonvolatile memory device, which was based on metal-oxide-metal-oxide-semiconductor (MIMIS) configuration, was proposed by Kahng and Sze in 1967 [8]. The initial oxide was very thin (less than 50Å) to allow direct tunneling of electrons from the silicon substrate into the floating gate. The electrons then remained on the

floating gate, since they were insulated by a second, much thicker oxide layer (Figure 2.3). When the potential was removed from the control gate, the field within the thin oxide was too small for back tunneling to occur, and therefore electrons were trapped.

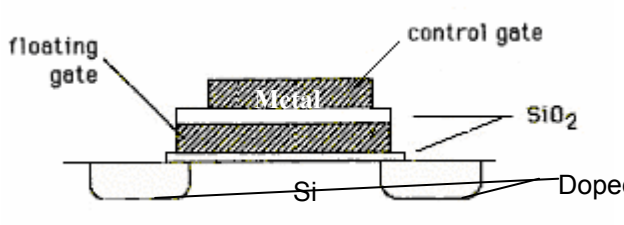

Figure 2.3: MIMS device

Unfortunately, pinholes in the thin oxide layer, which were unavoidable due to the manufacturing limitations at the time, led to charge leakage. This major obstacle was solved by Frohman-Bentchkowsky in 1971 where a thicker oxide and a polysilicon replaced the tunneling oxide and the metal floating gate (Figure 2.4). Instead of direct tunneling, avalanche injection mechanism, which will be explained in section 2.4, allowed charge to be trapped in the polysilicon floating gate. Changing the state of the device was possible using the control gate [9].

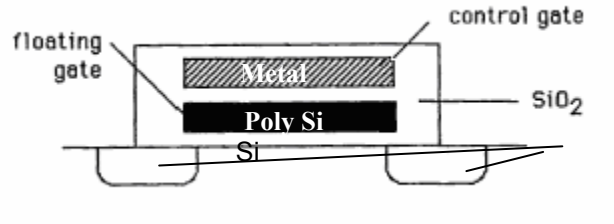

Figure 2.4: Floating gate nonvolatile memory device [10].

Almost concurrently another device using a metal-nitride-oxide-semiconductor (MNOS) configuration, was introduced by Wegner [10]. It was made of thin oxide and nitride films, and a metal gate (Figure 2.5). The nitride and oxide-nitride interface contain many trapping centers where charge can be captured and retained. Even if the

oxide proved to be leaky, some charge would remain due to the deep traps in the oxide-nitride interface and the nitride film.

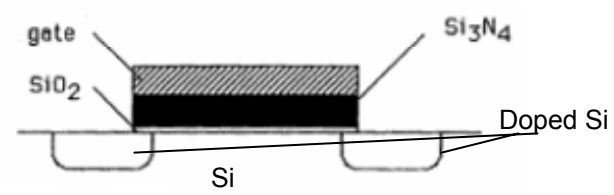

Figure 2.5: Cross section of a MNOS device [10].

Additional development led to the design of a polysilicon-oxide-nitride-oxide-silicon (SONOS) device (refer to Figure 2.6). The additional oxide layer prevented charge injection into nitride during the erasing step. The SONOS device also offers higher trap charge density compared to the MONS device due to its oxide-nitride-oxide stack and its interfaces. It also provided pinhole coverage, which might be present in the thin nitride layer. With the additional interface between the top oxide and the nitride, thinner nitride films were possible, which allowed lowering of the operational voltage for the SONOS device [11].

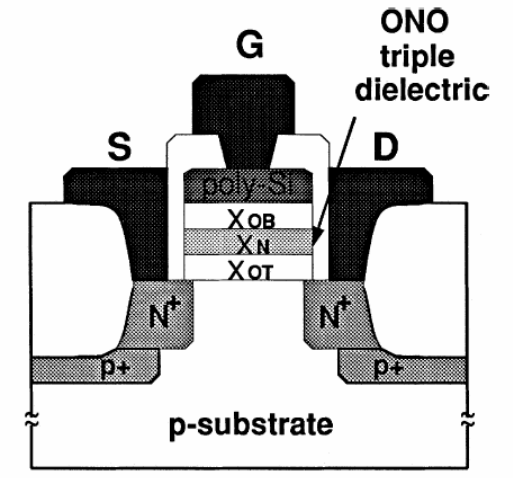

Figure 2.6: Cross section of a SONOS device. Tunneling oxide thickness (X_{OT}) 2 nm, storage nitride (X_N) 4.5nm and blocking oxide (X_{OB}) 5.5nm. Injection voltage of 10V and erasing voltage –9V [11].

2.4 Charge Transport Mechanisms

In an ideal insulator the conduction of the film is assumed to be zero. However, in reality given high enough electric field and/or temperature, a finite carrier current is present. The current in a given material depends on the dominant conduction mechanism present at given conditions as well as on the properties of the film. Figure 2.7 presents a plot of current density versus temperature for three different films (SiO_2, Al_2O_3, Si_3N_4) at a constant electric field. From this plot the transport mechanism at different temperatures can be determined. In the case of Si_3N_4, there are three regions of current conduction. J1 region is due to Frankel-Pool emission, J2 is due to the tunnel emission such as Fowler-Nordheim tunneling, and J3 is due to ohmic conduction [9]. Similarly, Al_2O_3 film illustrates three regions of current conduction similar to Si_3N_4. Finally, SiO_2 film shows some conductivity, which is lower by many orders of magnitude compared to either Si_3N_4 or Al_2O_3 films.

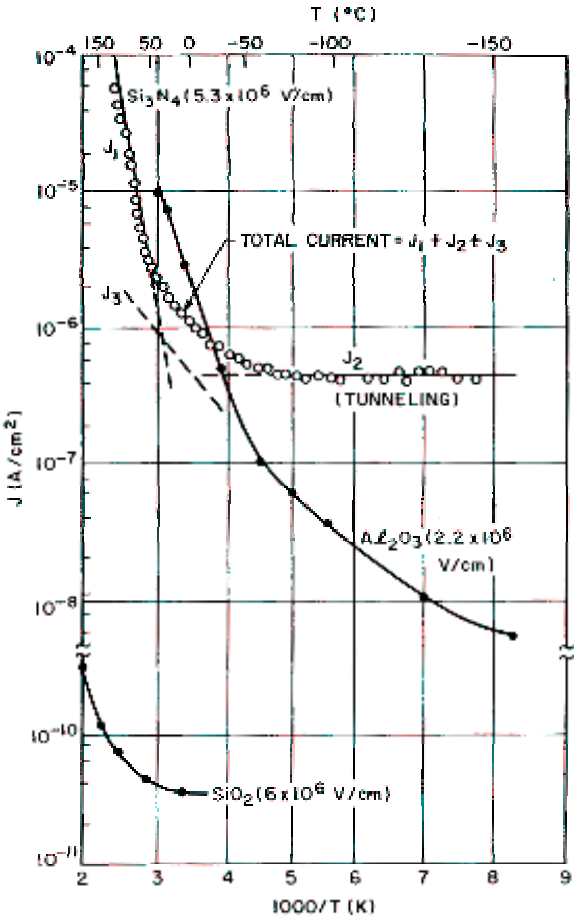

Figure 2.7: Current vs. temperature relationship for various dielectrics (SiO_2, Al_2O_3, Si_3N_4) [9].

At room temperature and high electric field, Frankel-Poole emission transport mechanism dominates in silicon nitride film [9]. The expression representing Frankel-Pool emission is defined in Eq. 2.1.

$$J \sim E \exp\left[\frac{q}{kT}\left(\Phi_b - \sqrt{qE/\pi\varepsilon_i}\right)\right] \qquad (2.1)$$

where J is the current density, Φ_b is the energy barrier of the trap, E is the electric field, ε_i is the permittivity of the insulator, T is the absolute temperature, k is Bolzmann's constant, and q is the charge of a single electron. As Eq. 2.1 demonstrates, the current density is associated with thermionic emission and a field-induced barrier lowering of the trap sites [12]. A trapped charge with a sufficient amount of energy can overcome the

energy barrier of the trap site and jump into the conduction band, where it can drift due to an electric field. However, once it loses energy it can become trapped again. Figure 2.8 illustrates how a trapped charge propagates through the film.

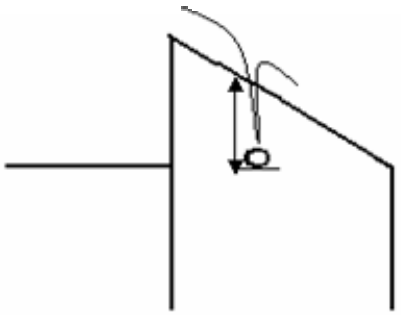

Figure 2.8: Illustration of Frankel-Pool emission where field-induced barrier lowering allows thermally energized charger to escape.

Another transport mechanisms present in Si_3N_4 film is charge-hopping conduction also referred to as ohmic conduction. It dominates at moderate to high temperatures and at low electric fields. The current flow is due to thermal excitation of charges, which hop from one trap site to the next. The current density depends on the density of defect states and their energy distribution. If the localized states are at the band tail states, the ohmic conduction mechanism follows the expression below [13].

$$J \sim E \exp\left(\frac{-E_a}{kT}\right) \tag{2.2}$$

where E_a is the activation energy for electron excitation. Figure 2.9 depicts the charge-hopping transport mechanism, where trap sites are located close to the conduction band.

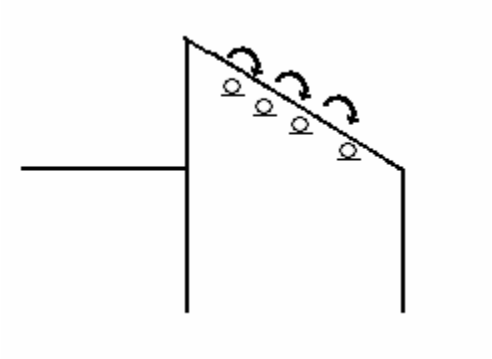

Figure 2.9: Illustration of charge hopping conduction where trap sites are close to the conduction band.

In case of SiO_2 film, the main charge transport mechanism is by charge injection. This is a result of the wide bandgap of 9 eV and low trap charge density found in SiO_2 compared to Si_3N_4 film. There are two types of mechanisms that can feasibly provide charge transport through SiO_2. One is based on quantum mechanical tunneling, and the other one is based on hot electron injection.

The main tunneling mechanisms are Fowler-Nordheim tunneling and direct tunneling. Fowler-Nordheim tunneling dominates at high electric fields and low temperatures. High electric field introduced at the electrodes results in stretching of the bandgap of the dielectric. The stretching distorts the bandgap into a triangular barrier effectively producing a much smaller gap thickness. This is represented as t_f in Figure 2.10. The stretching of the bandgap allows charge to tunnel into the conduction band of the film. Once in the conduction band, the charge gets swept by the electric field. Variablet_{ox} represents the undisturbed oxide band gap thickness, and Φ_B represents the energy barrier.

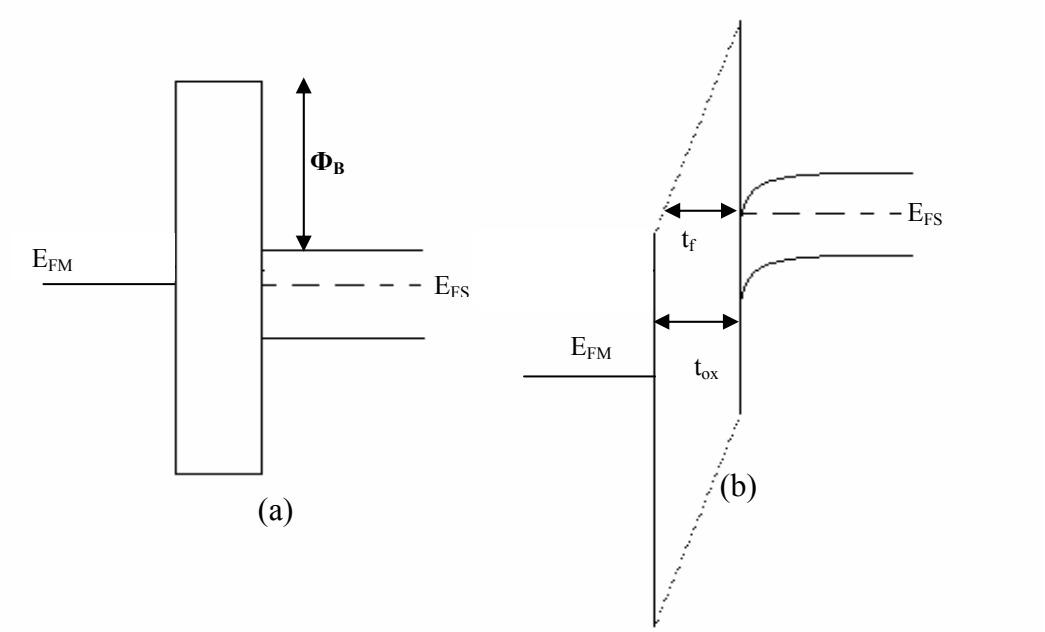

Figure 2.10: (a) equilibrium state (b) Fowler- Nordheim tunneling

The following expressions characterize the Fowler-Nordheim tunneling mechanism [14]

$$J = \alpha E^2 \exp\left[\frac{-\beta}{E}\right] \tag{2.3a}$$

$$\alpha = \frac{q3(m/m^*)}{8\pi\hbar\phi_b} \tag{2.3 b}$$

$$\beta = \frac{8\pi\sqrt{2m^*\phi_b^{\,3}}}{3q\hbar} \tag{2.3c}$$

where h is Planck's constant, $\hbar = \frac{h}{2\pi}$, m^* is the effective mass of an electron in the band gap, m the electron rest mass, q is the chare of a single electron, Φ_b is the energy barrier at the injecting interface, and E is the electric field applied across the dielectrics. Assuming Φ_b =3.80 eV and m/m^* =0.26 for SiO_2 film, the values for α and β are $1.57\text{x}10^{-6}$ A/V^2 and 257 MV/cm respectively [15].

The direct tunneling dominates for low gate voltages and very thin films. In direct tunneling, the charge tunnels directly through full oxide thickness into the empty state in the following material. Figure 2.11 illustrates charge tunneling from conduction band of silicon into the conduction band of silicon nitride.

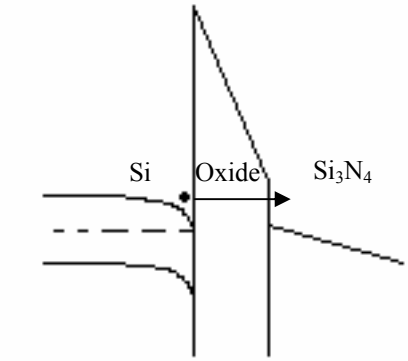

Figure 2.11: Direct Tunneling through thin SiO_2.

Hot carrier injection appears in floating gate nonvolatile memory devices, and it is observed in short channel MOSFETs. It can also affect bipolar transistors and diodes. The hot carriers (a.k.a. avalanche injection) enable charge injection across as much as 1000 Å of gate oxide [16]. The injection process begins with production of the hot carriers. It is accomplished by driving a MOS capacitor into deep depletion by applying a high frequency AC signal, to prevent minority carriers from following (refer to Figure 2.12 (d)). As the amplitude of the AC signal increases, so does the band bending at the silicon interface. When the electric field intensity at the silicon interface becomes sufficiently high, avalanche breakdown occurs. At that point the carries have a sufficient amount of kinetic energy to cause impact ionization. A plasma of electron-hole pairs is created, where a small number of the minority carriers have enough energy to surmount

the interfacial energy barrier and get injected into the oxide. Figure 2.12 illustrates the cycle of charge injection using an AC signal [16].

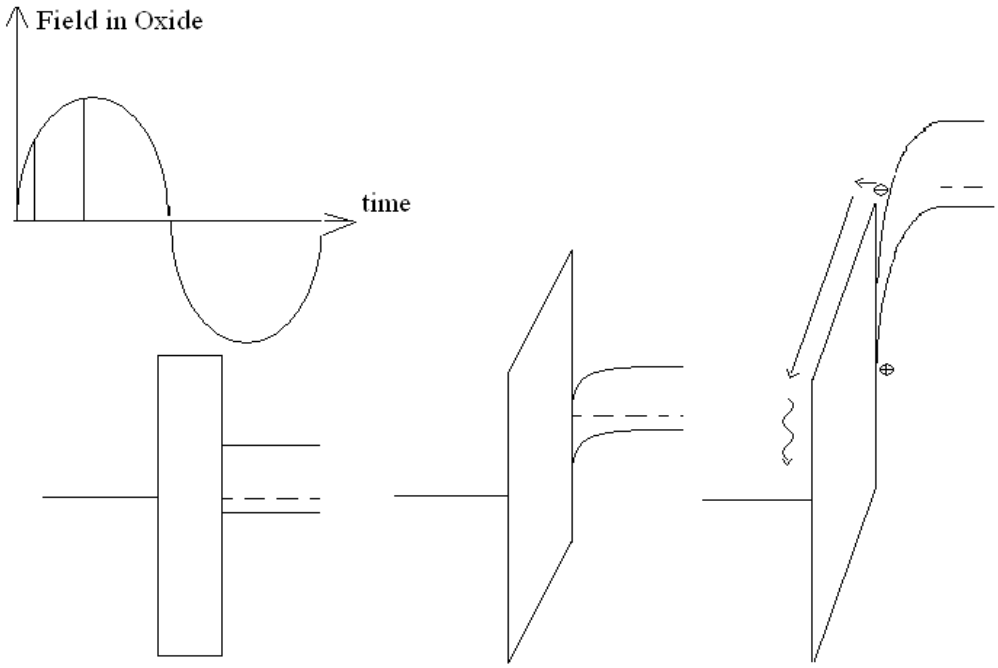

Figure 2.12: Diagram illustrating principles of avalanche injection: (a) voltage applied onto the gate at different stages of avalanch injeciton (b) band diagram at the initial state T=0, (c) band bending due to electric field at T_1, (d) creation of a electron-hole pair and charge injection at T_2. Reprint of Nicollian and Brews [16].

2.5 Charges within the Dielectrics

Presence of trap sites within dielectric films is caused by many factors such as film properties and processing conditions. Understanding the origin of trap sites is important in selecting the specific technology for a given application.

2.5.1 Charge in Silicon Nitride

Silicon nitride (Si_3N_4) possesses excellent properties for charge trapping. It has amphoteric traps [17], which means that both types of charges have an equal probability

of being present in the film. The traps are distributed across the entire dielectric. As a result, silicon nitride provides a large capture cross section for both types of charge**.** The approximate value of dangling bond concentration in CVD nitride film is ~10^{19} cm^{-3} [18]. A benefit of Si_3N_4 is that it is impermeable to mobile ions, such as sodium.

Traps in silicon nitride are formed during the deposition process and are attributed to dangling bonds and bandgap states in the film. Deposition parameters such as temperature have a significant effect on the concentration of hydrogen in the film. Hydrogen effectively passivates dangling bonds lowering the trap site density. CVD films deposited at higher temperatures (above 900 ºC) show 4%-10% concentration of ≡SiH units, whereas films deposited at lower temperatures can contain up to 30% of chemically bonded hydrogen [19].

2.5.2 Charge in Silicon Dioxide

The density of trap sites within silicon dioxide depends on fabrication of the film. Films deposited at low temperatures using LPCVD process are of lower quality and lower density. They have a higher number of traps due to their amorphous structure and therefore more defects such as dangling bonds. Thermally grown SiO_2 is of higher quality compared to a deposited film; however, it too contains some defects. They are caused by thermal processes present in IC fabrication and by imperfections of the silicon crystal, which cause defects in thermal SiO_2. These and other effects contribute to charge trapping in the SiO_2. There are four types of charges present in SiO_2 films: fixed charge Q_f, mobile charge Q_m, oxide trapped charge Q_{ot}, and interface trap charge Q_{it}.

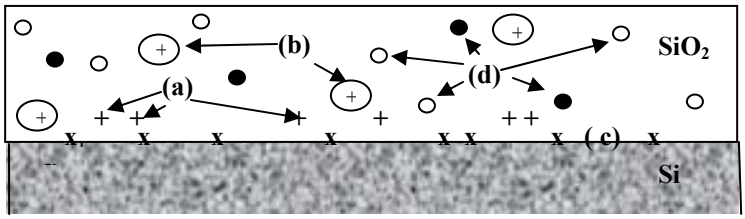

Figure 2.13: Charge and their location for silicon dioxide film. (a) fixed charge, (b) mobile charge, (c) interface trapped charge, (d) oxide trapped charge, Reprint after Deal[20].

The fixed charge is generally positive, and it is located approximately 30Å away from the Si-SiO_2 interface. As the name indicates the fixed charge cannot be altered with applied potential. It is created primarily due to structural defects in the oxide layer. The charge density depends on processing conditions such as oxidation ambient, temperature, cooling conditions, and silicon orientation. Figure 2.14 illustrates the inverse relationship between the final oxidation temperature and the fixed charge density. Higher temperatures result in lower charge density. It is also possible to reduce the charge at lower temperature by annealing the oxide wafer in a nitrogen or argon ambient. The fixed charge density is in the range of $1x10^{11}$ to $9x10^{11}cm^{-2}$[21].

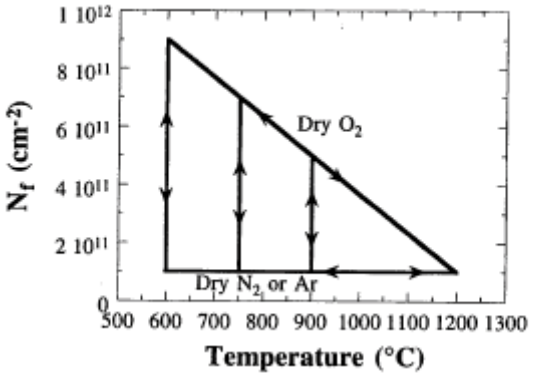

Figure 2.14: "Deal triangle", plot of heat treatment and its effect on reducing Q_f [21].

Mobile charge results from ionic impurities such as Na+, Li+, K+ and possibly H+. Another source of mobile charges is heavy metal impurities. They are located at either the metal-SiO_2 interface or at the SiO_2-substrate interface and when electric field is present these ions drift. This drift occurs because the ions are mobile in relatively low

temperatures. The following experiment preformed by Yon et al. illustrates mobile charge distribution within 5400Å of oxide before and after temperature bias stress. An etch-off technique was used to determine charge density at different thickness. Figure 2.15 (a) illustrates the final charge distribution within the oxide. To confirm results an electrical test was performed. Figure 2.15(b) shows the C-V plot of the oxide before and after the temperature bias stress. The charge density was ~1x10^{12} cm^{-2} [22].

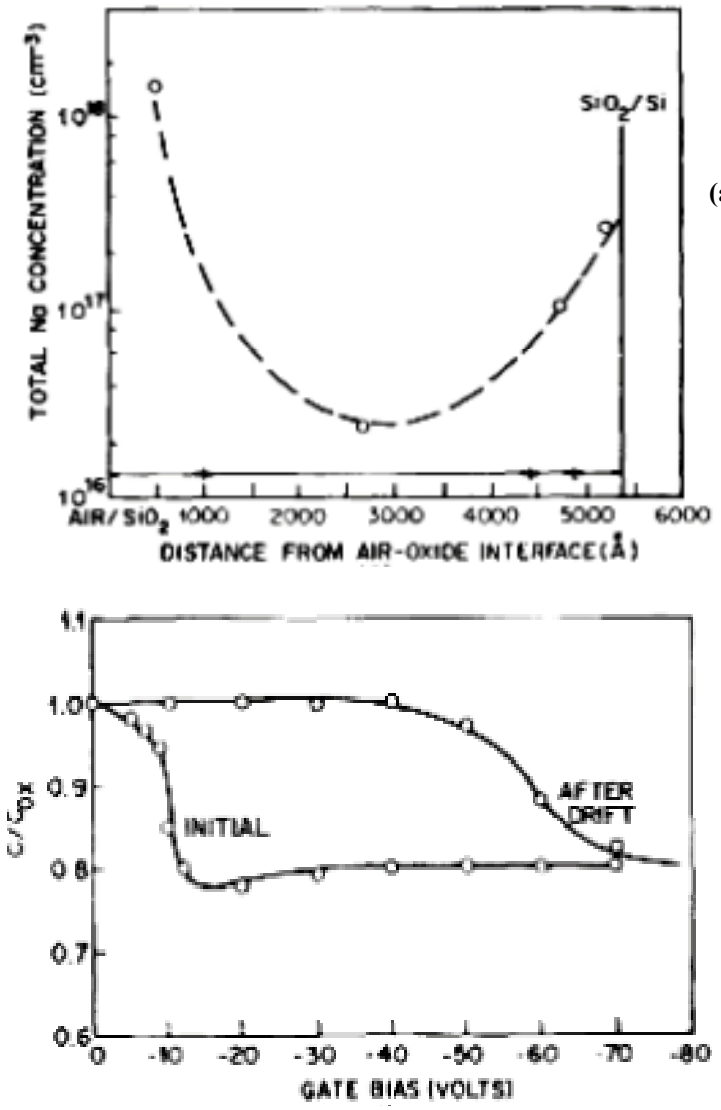

Figure 2.15: (a) Sodium profile within oxide, (b) C-V curve illustrating the before and after bias-temperature drift [22].

Interface-trapped charges are at the boundary of the substrate and SiO_2. They are a result of structural defects such as interruptions at an interface of two materials and bond breaking processes such as radiation and oxidation. The polarity of the charge can vary with gate bias and their energy levels are distributed throughout the band gap. Figure 2.16 illustrates a distribution of interface-trapped charge density over the energy spectrum of thermally grown SiO_2 on (111) and (100) silicon substrate. The interface states above the midgap are considered to be acceptor-like, since they are negative when filled with electrons and neutral when empty. On the other hand, donor-like interface states are neutral when filled with electrons and positive when empty [23]. Also a much higher interface-trapped charge density is observed closer to the conduction and valance bands. Typical interface trap charge densities are in the range of 10^{10} to 10^{12} cm^{-2} [24].

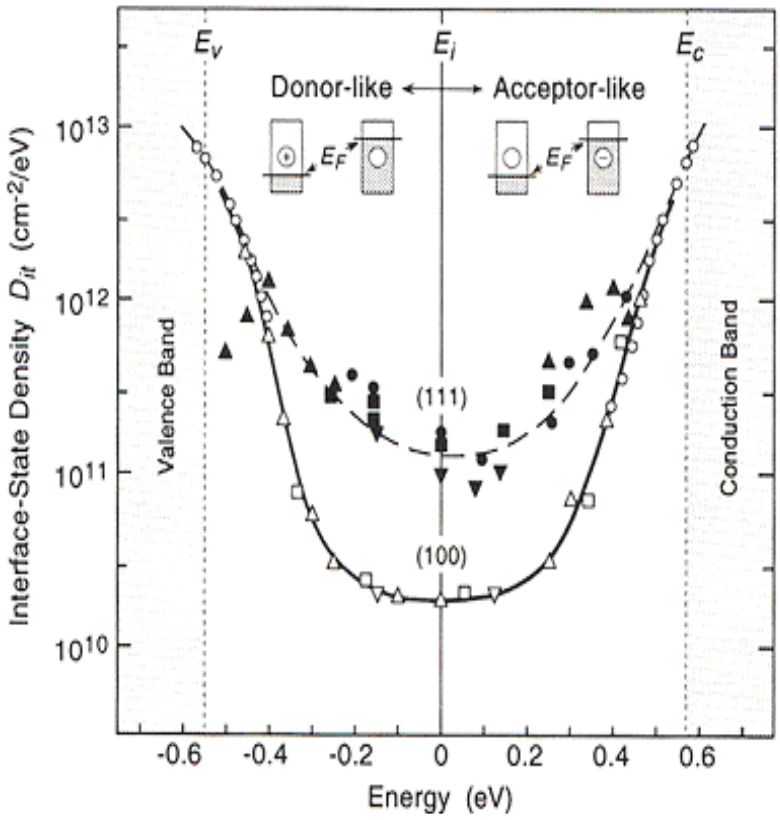

Figure 2.16: Distribution of interface trapped charge density over the energy spectrum of thermally grown SiO_2 on (111) and (100) Si substrate[23].

Oxide-trapped charge is found in the bulk of the SiO_2, and it can either be positive or negative. The most common sources of oxide-trapped charge are hot electron or hole injection, ionizing radiation, or Fowler-Nordheim tunneling. In addition, ion implantation can also lead to oxide-trapped charge [25]. Another source of charge in the bulk oxide is attributed to H_2O. Traps related to H_2O molecules are present in all thermally grown SiO_2 films. The traps are neutral during and after the oxide growth and they cannot be detected until electron injection. Injected electrons initiate a chemical reaction by breaking H_2O, which produces negatively charged centers and hydrogen [26].

2.6 C-V Measurements

Capacitance-Voltage (C-V) measurements are common for characterizing charge within MOS and MOS-like structures. C-V measurements work by applying a DC gate voltage with a superimposed small AC signal of varying frequency. The DC gate voltage changes slowly to obtain a continuous curve showing regions of accumulation, depletion, and inversion. The charge variation due to the AC signal gives rise to a measurable capacitance, as given in Eq. 2.4, where Q represents the semiconductor charge, V represents gate voltage, and C represents the capacitance.

$$C = -\frac{dQ}{dV} \tag{2.4}$$

Accumulation region (Figure 2.17) for the n-type metal-oxide-semiconductor capacitor (MOS-C) occurs when a positive voltage is applied to the gate. The positive polarity causes majority carriers to be attracted toward the gate. Due to the presence of dielectric the carriers accumulate at the Si-SiO_2 interface. In the accumulation region the

capacitance is constant and represents the oxide capacitance C_{max} from which thickness of the film can be extracted.

A depletion region results when the gate voltage in the n-type MOS-C moves toward negative values. The negatively biased gate electrostatically repels majority carriers from the silicon interface. The carrier-depleted area creates another capacitor. As a result, there are two capacitors in series, one due to the oxide and another one due to the depletion layer in the substrate. As the voltage decreases further, the depletion zone penetrates more deeply into the semiconductor, decreasing the total capacitance.

As the gate voltage decreases beyond the threshold voltage of the n-type MOS-C, there is an accumulation of minority carriers at the Si-SiO_2 interface creating an inversion layer. In this stage, at low frequencies the total capacitance is the same as in the accumulation region, but at high frequencies the relatively sluggish generation-recombination of minority carries will not be able to respond to the fast varying AC signal, and the depletion region remains fixed at its maximum thickness.

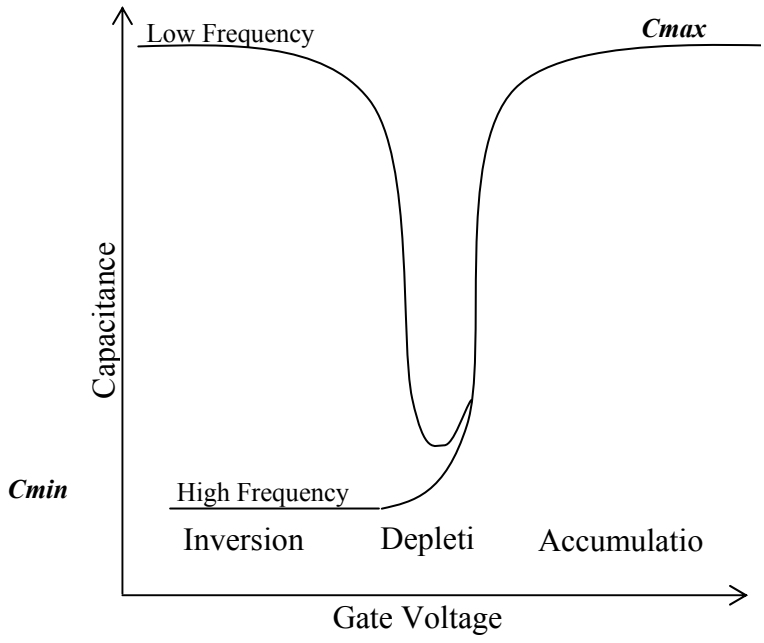

Figure 2.17: C-V curve example for n-type MOS-C.

C_{max} can be obtained from the C-V curve in Figure 2.17, or it can be calculated using Eq. 2.5. If the dielectric is silicon oxide, the C_{max} is

$$C_{\max} = \frac{\varepsilon_{ox}}{t} \tag{2.5}$$

where C_{ox} is the oxide capacitance (F/cm^2), ε_{ox} is the permitivity of the oxide film, and t is the thickness of the dielectric. If there is more then one dielectric film, C_{max} is a series combination of capacitances made of individual dielectric layers as shown in Eq. 2.6:

$$C_{\max} = \left(\frac{1}{C_{ox}} + \frac{1}{C_{other}} \right)^{-1} \tag{2.6}$$

where C_{other} represents the capacitance due to the other film. C_{min} is the combination of C_{max} and C_{dep} capacitance:

$$C_{\min} = \left(\frac{C_{\max} C_{dep}}{C_{\max} + C_{dep}} \right) \tag{2.7}$$

where C_{dep} is the depletion capacitance in the semiconductor, which in turn is defined as:

$$C_{dep} = \frac{\varepsilon_s}{W_{dep}} \tag{2.8}$$

where ε_s is the permitivity of the substrate, while W_{dep} is the substrate depletion width, which can be calculated using Eq. 2.9. Eq. 2.9 represents the maximum depletion width for any given doping concentration N_x.

$$W_{dep} = 2\sqrt{\frac{\varepsilon_s \left| \phi_f \right|}{qN_x}} \tag{2.9}$$

In the above equation ϕ_f is the Fermi potential of the substrate. In case of an n-type doped substrate ϕ_f is:

$$\phi_f \approx -\frac{kT}{q}\ln\left(\frac{N_d}{n_i}\right) \tag{2.10a}$$

and in case of a p-type doped substrate ϕ_f is:

$$\phi_f \approx \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) \tag{2.10b}$$

where Boltzman's constant k =1.38×10^{-23} J/K, T is the temperature in degrees Kelvin, q=1.606*10^{-19} C is the charge of an electron, N_a and N_d are the doping concentrations of the substrate, and n_i= 10^{10} cm^{-3} is the carrier concentration in intrinsic semiconductor at the room temperature.

Flatband voltage V_{FB} is the external voltage applied to cancel the built-in potential of the MOS capacitor. As a result, all energy bands are flat and the total potential of the system is zero. It is defined by a work function difference, fixed charge Q_f, mobile charge Q_m, oxide trapped charge Q_{ot}, and interface trap charge Q_{it}. The fixed charge and the interface trap charge are fixed in space and are close to the Si-SiO_2 boundary. The mobile charge and the oxide trap charge may be distributed anywhere within the oxide.

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{ox}} - \gamma\frac{Q_{ot}}{C_{ox}} - \gamma\frac{Q_m}{C_{ox}} - \frac{Q_{it}}{C_{ox}} \tag{2.11}$$

where γ represents charge distribution within insulator. The distribution of the charge in the proximity to the semiconductor is important, since it will affect the flatband voltage value. For example, charge that is closer to the silicon will result in a greater flatband voltage shift [27]. Hence, γ is defined as:

$$\gamma = \frac{\int_0^{tox} \left(\frac{x}{t_{ox}} \right) \rho(x) dx}{\int_0^{tox} \rho(x) dx} \tag{2.12}$$

where $\rho(x)$ is the mobile charge or the oxide trapped charge per unit volume, x represents the distance from the gate metal-oxide interface down to the substrate, and t_{ox} is the oxide thickness [27]. When $\gamma = 1$ the charge is at the Si-SiO_2 interface, and when $\gamma = 0$ the charge is at the gate-SiO_2 interface. Flatband voltage also takes into account the work function difference ϕ_{MS}, which is defined in terms of the work functions of the bulk material and the gate material. The work function is a measure of the energy between Fermi level and vacuum level.

$$\phi_{MS} = \phi_{bulk} - \phi_{gate} \tag{2.13}$$

In case of MOS-C, the value for $\phi_{\text{bulk material}}$ is the Fermi potential that is calculated using equations 2.10(a) or 2.10(b), depending on the type of doping. The values for $\phi_{\text{gate material}}$ for various materials are listed in Table 1.1 in the appendix [28].

Another way of obtaining the flatband voltage is by calculating the flatband capacitance and extracting the voltage from the C-V curve. The flatband capacitance C_{FB} is defined as:

$$C_{FB} = \frac{C_{OX} C_{FBS}}{(C_{OX} + C_{FBS})} \tag{2.14}$$

where C_{OX} is the oxide capacitance, and C_{BFS} is the flat band capacitance of the depletion region in the substrate. C_{BFS} is defined as:

$$C_{FBS} = \frac{\varepsilon_S}{\lambda} \tag{2.15}$$

where ε_s is the permittivity of the substrate material, and λ is the Debye's length, which is in turn given as:

$$\lambda = \left(\frac{\varepsilon_s kT}{q^2 N_x} \right)^{1/2} \tag{2.16}$$

where kT is a constant and its value at room temperature is 4.046×10^{-21} J, q is the electron charge 1.60219×10^{-19} C, and N_x represents doping of the substrate. This method is widely used due to its simplicity [29].

2.7 Charge Distribution within Multi-Layer Insulators

According to Bu et al. [30] a thin nitride layer and a blocking oxide layer provide trap charge storage at their interface. Yang et al. [18] studied the silicon nitride layer as the charge storage layer. Roy's and White's paper [31] concentrates on modeling of charge trapping within the nitride layer of ONO device, which is the dominant charge trapping center in this case. The actual charge distribution within a given ONO device will vary depending on processing parameters, the film stack thicknesses, and the charge injection technique.

The two commonly used methods to determine the trap charge distribution within oxide or any other dielectric are etch-off and IV photoemission. With the etch-off technique, the remaining film is measured for traps or impurities at each etch step. Also, with this technique charged area can be distinguished visually. An experiment by Nicollian et al. found that the oxide etch rate in buffered HF is slightly slower for charged oxide compared to uncharged oxide [32]. The drawback is a possible removal of the

charge region during the decremented etches. Another problem lies in depositing a new gate after the etch step to perform electrical measurements. Metal can penetrate 20Å into the oxide possibly perturbing the trap charge region. Also, possible misalignment of the new gate will lead to inaccurate results.

IV photoemission is based on photons exciting electrons, either in silicon or metal, which then drift through SiO_2. As the frequency of the incident light increases, a critical frequency is reached at which the valence electrons have enough energy to overcome the energy barrier of SiO_2. These electrons drift toward the gate or bulk silicon, depending on the polarity of the potential applied to the gate, creating a photocurrent that is measured with an external circuit. The IV photoemission technique is more accurate and nondestructive compared to the etch-off method. Also, it can provide information about the energy barrier between different materials as well as their band gap energy [32]. Another technique used to measure charge distribution is thermal pulse method. The equivalent electret voltage is measured immediately after a heat pulse is applied. The heat wave propagates through different layers of the dielectric while contributing to the equivalent voltage. The charge distribution is derived from this voltage [18]. Yet another technique is the Faraday cup method, which makes it possible to study the dynamics of film charging. It is also used to determine the total charge within an electret [19]. This technique might be helpful in determining the total charge within the released structure.

References

1. Vladimir. N. Kestelman, Leonid S. Pinchuk, Victor A. Goldade, "Electrets in engineering: fundamentals and application" 2000,Kluwer Academic Pulishers pg. 66

2. Bozena Hilczer andJerzy Malecki, "Studies in Electrical and Electronic Engineering 14: Electrets" Elsevier, New York, 1986, pg 341-342

3. Vladimir. N. Kestelman, Leonid S. Pinchuk, Victor A. Goldade, "Electrets in engineering: fundamentals and application" 2000,Kluwer Academic Pulishers pg. 91-163

4. G. M. Sessler, "Electrets" Volume 33 Physics Principles, Springer-Verlag Berlin Heidelderg, Germany 1987. 340 pg

5. B. Hilczer and J.Malecki, "Studies in Electrical and Electronic Engineering 14: Electrets" Elsevier, New York, 1986, pg 2-6,

6. Joseph I. Goldstein, Dale E. Newbury, Patrick Echlin, David C. Joy, Charles E. Lyman, Eric Lifshin, Linda Sawyer, and Joseph R. Michael, "Scanning Electron Microscopy and X-Ray Microanalysis", 3rd ed., Kluwer Academic/Plenum Publishers, New York, 2003

7. G. M. Sessler, "Electrets" Volume 33 Physics Principles, Springer-Verlag Berlin Heidelderg, Germany 1987. 34 pg

8. S.M. Sze, "Physics of Semiconductor Devices", John Wiley & Sons, 1981 pg 496

9. S.M. Sze, "Physics of Semiconductor Devices", John Wiley & Sons, 1981 pg 402-407

10. William D. Brown and Joe E. Brewer, "Nonvolatile Semiconductor Memory Technology" IEEE Press, 1998 pg 6-8

11. Yang Yang, Marvin H. White" AHrge retention of scaled SONOS nonvolatile memory devices at elevated temperatures", Solid State Electronics, vol. 44 , pg 949-958, 2000

12. D. K. Schroder, "Semiconductor Material and Device Characterization" 1998, John Wiley & Sons pg 278

13. Karl D. Hirschman, " Fabrication, Characterization and Integration of Oxide Passivated Nanocrystalline Silicon Light Emitting Device" University of Rochester,2000

14. William D. Brown and Joe E. Brewer, “Nonvolatile Semiconductor Memory Technology” IEEE Press, 1998 pg 10-14

15. D. K. Schroder, “Semiconductor Material and Device Characterization” 1998, John Wiley & Sons pg 391-94

16. E.H. Nicollian and J. R. Brews, “MOS (Metal Oxide Semiconductor) Physics and Technology “, John Wiley & Sons, 1982, pg. 495-498

17. M.H. White and C.C Chao “Statistics of deep-level amphoteric traps in insulators and at interfaces” Journal of Applied Physics Vol 57 no 6 , March 1985,pg 2318-2321

18. Yang Yang, Ansha Purwar, Marvin H. White, “ Reliability consideration in scaled SONOS nonvolatile memory devices” Solid State Electronics 43 (1999) 2025-2032

19. A. John Robertson, Martin J. Powell, “Gap states in silicon nitride “Applied Physics Letter 44(4) February 1984

20. B. E. Deal “Standardized Terminology for Oxide Charges Associated with Thermally Oxidized Silicon” IEEE Trans. Electron Devices ED-27, March 1980, 606-608

21. B.E. Deal, M. Sklar, A. S. Grove, and E.H. Snow, “ Characteristics of the Surface – State Charge (Qss) of Thermally Oxidized Silicon,” Journal Electrochem. Soc. 114, March 1967, 266-274

22. E. Yon, W. H. Ko, and A. B. Kuper, "Sodium Distribution in Thermal Oxide on Silicon by Radiochemical and MOS Analysis," IEEE Trans. Electron Devices ED-13, 276-280 (1966)

23. T. Hori, “Gate dielectrics and MOS ULSIs: Principles, Technologies, and Applications” Springer Series in Electronics and Photonics, Vol 34

24. E.H. Nicollian and J. R. Brews, “MOS (Metal Oxide Semiconductor) Physics and Technology “, John Wiley & Sons, 1982, pg. 285-318

25. D. K. Schroder, “Semiconductor Material and Device Characterization” 1998, John Wiley & Sons pg 339

26. E.H. Nicollian and J. R. Brews, “MOS (Metal Oxide Semiconductor) Physics and Technology “, John Wiley & Sons, 1982, pg532-544

27. D. K. Schroder, “Semiconductor Material and Device Characterization” 1998, John Wiley & Sons pg 347-348

28. Yannis Tsividis, “Operation and Modeling of The MOS Transistor”, 1999, WCB/McGrawHill pg. 50-55

29. E.H. Nicollian and J. R. Brews, “MOS (Metal Oxide Semiconductor) Physics and Technology “, John Wiley & Sons, 1982, pg. 487

30. Jiankang Bu and Marvin H. White, ”Retention reliability enhanced SONOS NVSM with scaled Program Voltage” Aerospace Conference Proceedings, IEEE , Vol 5 , 2002, 2383 –2390

31. A. Roy and M. H. White, “ Determination of the Trapped charge Distribution in Scaled Silicon Nitride MONOS Nonvolatile Memory Devices by Tunneling Spectroscopy ” Solid State Electronics Vol 34, No. 10, 1991,pg 1083-1089

32. E. H. Nicollian, C. N. Berglund, P. F. Schmidt, and J. M. Andrews, ”Electromechnical Charging of Thermal SiO2 film by injection electron currents ”,Appl. Phys. 42,1971,pg 5654 -5663

CHAPTER THREE: HIGH FIELD CHARGE INJECTION

3.1 Introduction

Chapter 2 introduced a few techniques of trapping charge within dielectric materials. In the following section the focus will be on charge injection using a high electric field applied through a metal electrode and a semiconducting substrate. Based on the initial work, this technique proved to be feasible and most promising. The experiments presented here will provide a better understanding of this technique and its effectiveness in charging an oxide-nitride-oxide (ONO) stack.

3.2 Tool Setup

The test setup used for C-V characterization consisted of: a Keithley 595 Quasistatic C-V Meter, Keithley 590 C-V Analyzer, and a Keithley 230 Programmable Voltage Manager as shown in Figure 3.1. Also, a temperature controller was connected to the chuck. The system specifications and its block diagram are listed in appendix B. In addition, Figure 3.1 also shows the setup for film breakdown analysis, which consisted of a HP 4145B parameter analyzer.

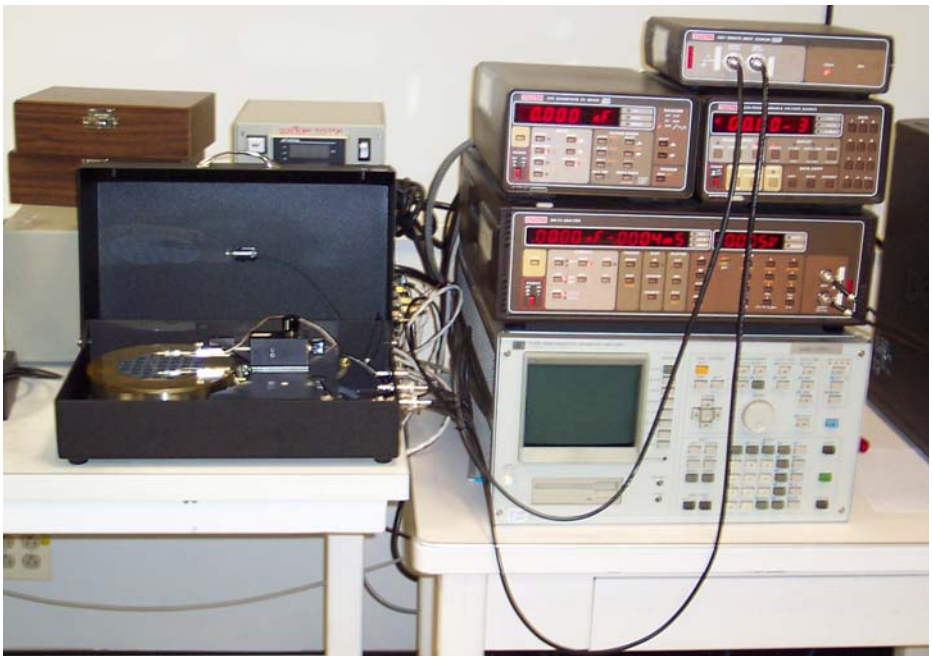

Figure 3.1: I-V and C-V instrumentation located at RIT.

The test setup for high field charge injection consisted of a Tektronix 370 programmable curve tracer and a probe station. Signal cables from the curve tracer were affixed to the chuck on which wafers were placed and probed. The tool specifications are listed in appendix B. An oscilloscope was implemented for an accurate measurement of the applied potential.

Figure 3.2: High-field charge injection setup located at RIT.

3.3 Thin-Film Characteristics

Preliminary work did not demonstrate successful charge retention of capacitors made of oxide-nitride film stack after high field charge injection. The failure was attributed to poor quality of the silicon nitride film. Typical dielectric strength of a silicon nitride film is on the order of 6 - $10x10^6$ V/cm [1]. In an article by Takahiro [2], who studied various properties of silicon nitride film by varying the ammonia gas flow in a LPCVD system, it was demonstrated that a 10:1 ratio of ammonia (NH_3) to dichlorosilane (SiH_2Cl_2) produces a high quality stoichiometric silicon nitride film. The composition of silicon nitride was also correlated to the index of refraction. The refractive index of stoichiometric silicon nitride is 1.987, but as the ratio of NH_3 to SiH_2Cl_2 decreases the refractive index and the leakage current of the insulator increase [2]. Since silicon nitride fabricated in preliminary studies exhibited high leakage current, a new recipe was developed for silicon nitride films with reduced SiH_2Cl_2 flow. To investigate the leakage of the new film, a current vs. voltage (I-V) measurement was performed. A 6“ LPCVD system was used with the following gas flows; NH_3 of 50sccm, and SiH_2Cl_2 of 4sccm. This was followed by evaporation and pattering of aluminum, and finally the removal of the nitride film from the backside of the wafer. The thickness of the silicon nitride film was 770Å. Figure 3.3 shows two I-V measurements performed on the same capacitor fabricated using the new silicon nitride recipe, with an area of $1x10^{-2}$ cm^2.

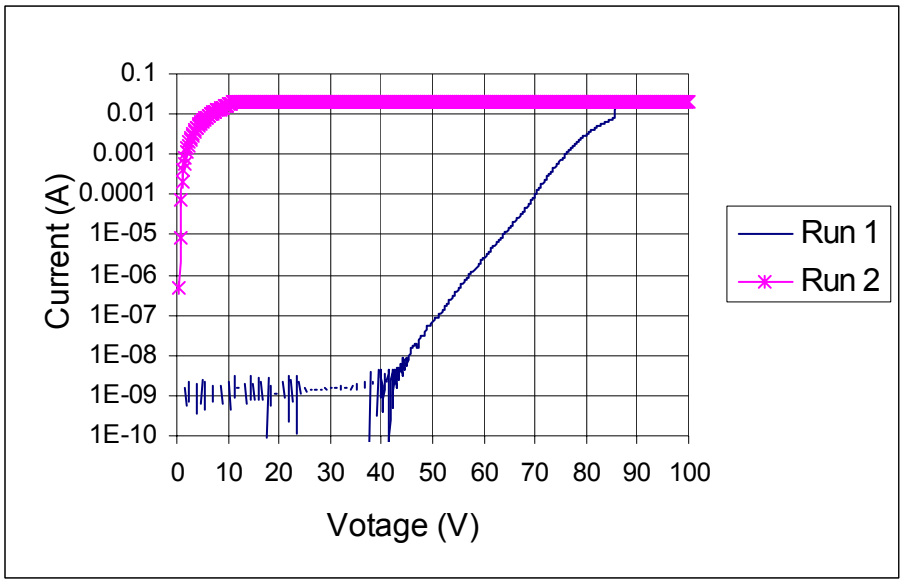

Figure 3.3: Breakdown plots of silicon nitride film of 770Å thick deposited using a 50sccm of NH_3 and 4sccm of SiH_2Cl_2. Run 1 illustrates partial breakdown at ~85V. Run 2 illustrates a catastrophic breakdown at ~ 5 V of the same capacitor.

The breakdown of a low temperature oxide (LTO) film was also investigated (Figure 3.4). Using the standard SMFL recipe (refer to appendix A for details) in a 6" LPCVD system, LTO was deposited on a wafer. This was followed by evaporation and pattering of aluminum, and finally the removal of oxide from the backside. The thickness of the silicon dioxide film was measured as 730Å and the area of the capacitor was $1.5x10^{-2}$ cm^2. In literature, dielectric strength of an oxide film is on the order of 1MV/cm up to 10MV/cm and its resistivity on the order of 10^{15}-10^{17} Ωcm[3].

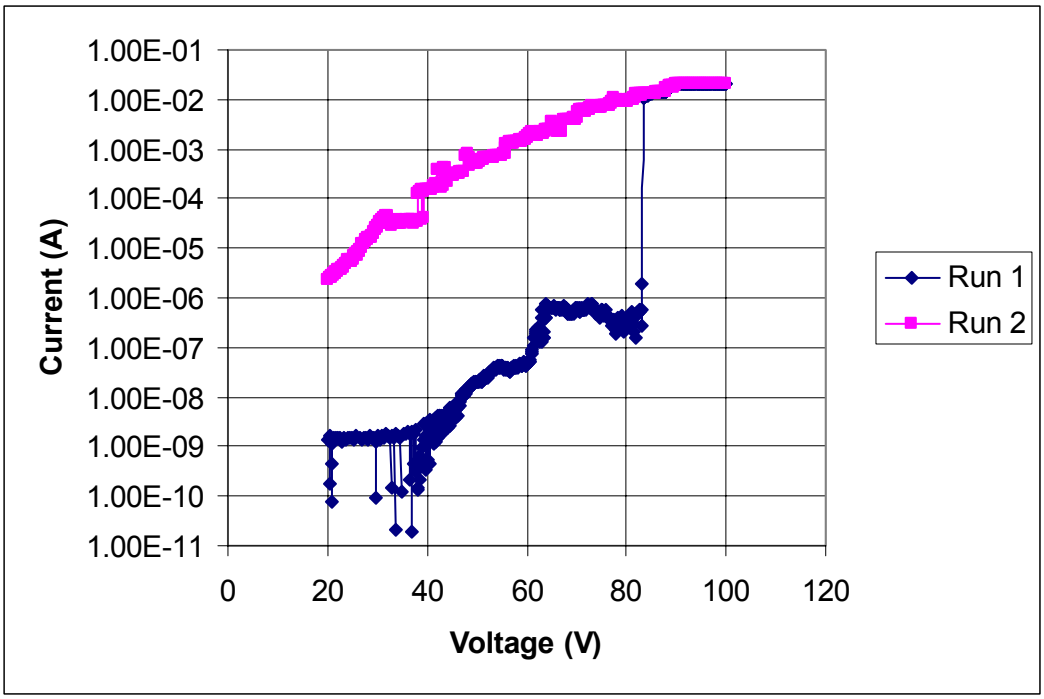

Figure 3.4: Breakdown plots of LTO film of 730Å deposited using the standard SMFL recipe. Run 1 illustrates partial breakdown at ~85V. I-V plot of Run 2 illustrates increased in leakage current resulting eventually in catastrophic breakdown at ~ 90 V.

Discussion:

The silicon nitride breakdown (Figure 3.3) shows constant current from 0V up to 40V. The region between 40V and 85V shows Fowler-Nordheim tunneling and a partial breakdown is measured above 85V [4]. The LTO breakdown (Figure 3.4) illustrates a constant current up to 40V. Above 40V the plot illustrates a region, where trap assisted tunneling [5] and possibly other mechanisms contribute to the current conduction. Above 85V a soft breakdown is present resulting in partial breakdown of the film [6]. Neither Figure 3.3 nor Figure 3.4 shows a hard breakdown of the dielectrics, since the first voltage sweep did not result in a catastrophic failure of the films. Therefore, actual dielectric strength cannot be determined from these figures. Fowler-Nordheim tunneling and thermionic emission processes exhibit a field dependent resistivity, however the low-field (ohmic) resistivity of both oxide and nitride films can be utilized for film analysis.

In case of the oxide film the resitivity in the 20V-30V range is approximately $3.5x10^{13}\Omega cm$, which is two orders of magnitude lower compared to cited values 10^{15}-$10^{17}\Omega cm$ [3]. In case of silicon nitride the measured resistivity is approximately $4x10^{13}\Omega cm$ in the 0V-40V range, again two orders of magnitude lower compared to the reported values 10^{15}-$10^{17}\Omega cm$ [2]. Effectively, the films in Figure 3.3 and Figure 3.4 show a somewhat leaky behavior. The failure to reach a catastrophic breakdown is attributed to the current leakage, which protects the films from destructive breakdown, even at fields higher than reported breakdown values. The quality of the films has a direct influence on the charge injection process, and the capability of retaining the injected charge.

3.4 Capacitance – Voltage Analysis

In the following section, analysis of an uncharged ONO stack capacitor using the C-V characterization system is described. Also, the amount of fixed charge within the tri-layer film stack was measured.

Sample Preparation:

An n-type wafer with $5x10^{14}$ cm^{-3} doping was scribed and RCA cleaned before deposition. All the dielectric films were deposited in the 6" LPCVD system. Using the standard SMFL LTO recipe, the oxide film was deposited for 4 min. The deposition time for the SMFL stoichiometric nitride was 27 min. For LTO the edges were thicker than the center with approximately 38% full-range-uniformity (FRU). Eq. 3.1 was used to calculate the FRU for all film thicknesses and etch rates.

$$FRU = \frac{M_{\max} - M_{\min}}{M_{\max} + M_{\min}} * 100 \qquad \textbf{(3.1)}$$

For the nitride film, the FRU was about 5%. The first layer of LTO averaged 520Å in thickness. The average thickness for the nitride layer was 508Å. The second LTO layer averaged 450Å. A micron of Al was then evaporated using the CHA Evaporator. The ONO was stripped from the backside of the wafer to achieve an electrical contact. This was done by coating the device side of the wafer with a photoresist and submerging it into buffered HF. Using SMFL nitride 4" recipe on the Lam 490 for 30 sec the nitride layer was etched off. This was then followed by another 1min buffered HF dip. The resist was stripped using acetone followed with a spin, rinse and dry. A new coating of photoresist was applied, so it could be exposed on the GCA using the CVTEST mask. Next, the wafer was developed. Both coating and developing were done using program 1 on the SVG track, and the aluminum was wet etched until the pattern was clearly visible. After the aluminum etch, the resist was stripped off using acetone followed by a spin rinse and dry. Details regarding the recipes are listed in appendix A.

Procedure:

The C-V measurements were done using a test setup with the following parameters: AC signal at 100KHz, steps size of 20mV, delay of 200msec and 70msec. The voltage was swept from -10V to 10V and from 10V to -10V.

Results:

Positive and negative sweeps with 200ms delay per measurement are plotted in Figure 3.5. Figure 3.6 shows the same sweeps with a 70ms delay.

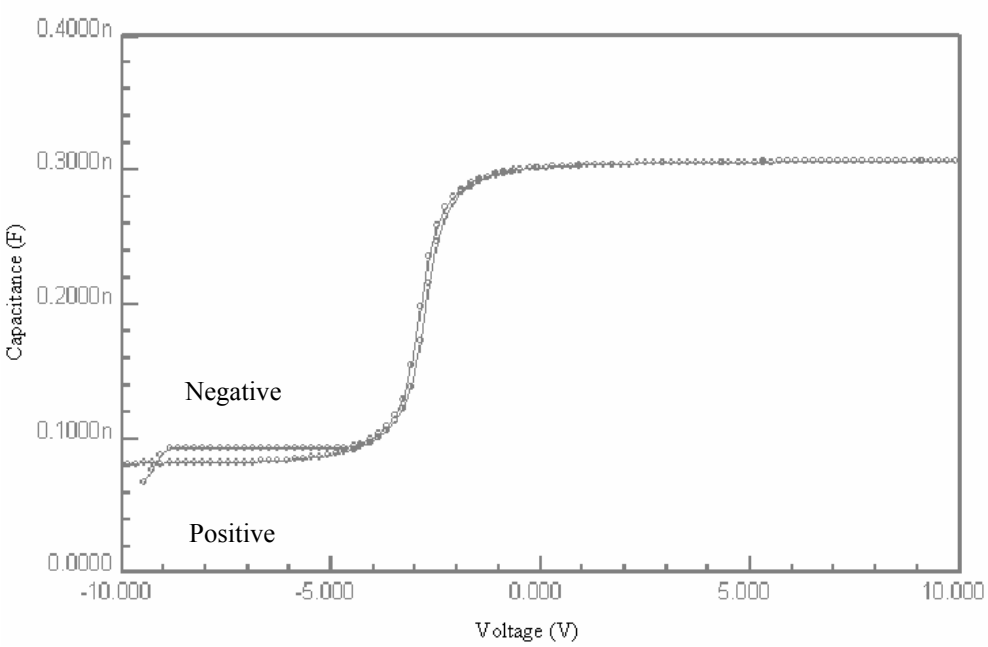

Figure 3.5: Positive and negative sweep with 200ms bias delay for C-V measurement using a tri-layer film stack of 520Å oxide, 508Å nitride and 450Å oxide.

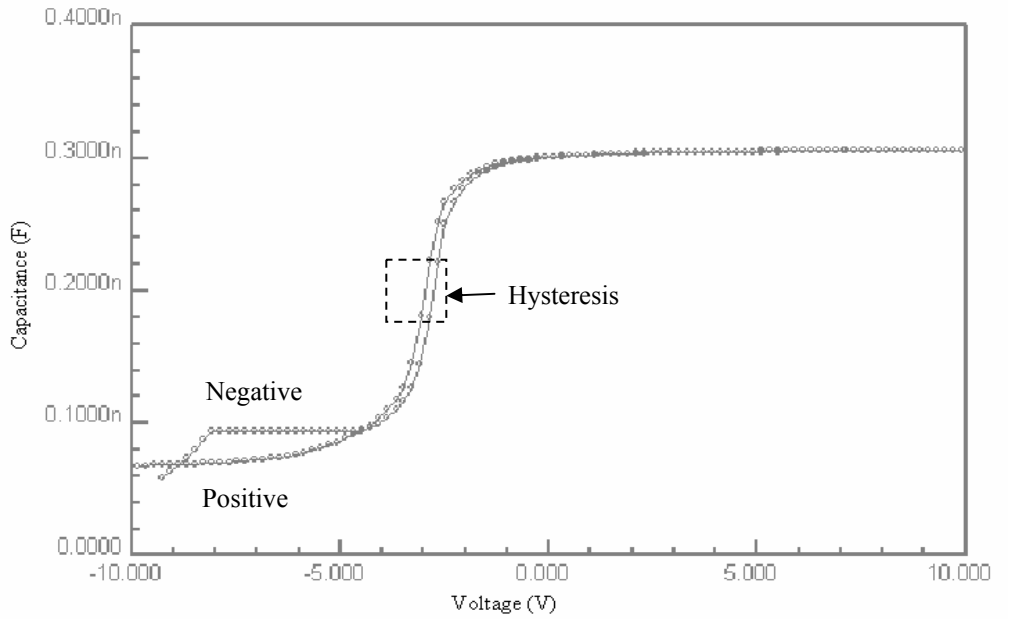

Figure 3.6: Positive and negative sweep with 70ms bias delay for C-V measurement using a tri-layer film stack of 520Å oxide, 508Å nitride and 450Å oxide. The hysteresis is attributed to the presence of interface charge.

Discussion:

All four curves show average flatband voltage of 2.3V. To measure the flatband voltage flatband capacitance was determined from equations 2.14, 2.15 and 2.16. The shift is caused by the presence of fixed charge (Q_f). The fixed charge is positive and it is located within 30Å from the Si-SiO_2 interface. The magnitude of the charge is represented by equation 3.2

$$Q_f = (\phi_{ms} - V_{FB})C_{\max} \qquad \textbf{(3.2)}$$

where V_{FB} is the measured flatband voltage and C_{max} is the maximum capacitance. Knowing the approximate values of these parameters, Q_f is determined to be about $4x10^{11}cm^{-2}$.

Both Figure 3.5 and Figure 3.6 show some hysteresis in the C-V curves, but it is more pronounced in Figure 3.6. The hysteresis is related to the presence of interface charge, and to minimize this effect the sweeps should be performed at a slow rate to maintain steady state conditions [7]. To determine the value of the interface charge density more measurements are required utilizing the quasi-static method [8].

Figure 3.5 and Figure 3.6 also show a variation of C_{min} value. The variation is a consequence of sweeping the DC voltage too fast during the high frequency measurements. As the DC voltage sweeps from the positive to the negative bias and into the inversion region, the minority carriers are too slow to follow. Since the system needs to reach charge neutrality, donors ionize and the depletion width becomes wider than in thermal equilibrium, creating what is referred to as a deep depletion region. To reduce this effect one can sweep very slowly, allowing the system to reach equilibrium, but this dramatically increases the duration of the measurement, and could influence time

dependent experiments. Another option is to perform C-V measurements for n-type wafers sweeping the voltage from negative to positive (inversion to accumulation) [8]. By sweeping from the negative potential, the C_{min} value would be closer to that of thermal equilibrium.

3.5 Mobile Ion Charge Density

Chapter 2 discussed the origins and types of charge within the nitride and oxide films. This experiment focused on determining if mobile charge was present within the ONO film stack and its magnitude. Bias temperature stress method was used in conjunction with Eq. 3.3 to determine charge density of the mobile ions, where ΔV_{FB} represents the potential difference between the two experimentally determined C-V curves [8].

$$Q_m = -\Delta V_{FB} C_{\max} \qquad \textbf{(3.3)}$$

Procedure:

An n-type wafer of $1x10^{15}$ cm^{-3} doping was scribed and RCA cleaned before growing dry oxide in a 6-inch Bruce furnace following standard SMFL recipe 512. Due to some issues with the tube in the 6-inch LPCVD system, the nitride film was deposited in a 4-inch LPCVD tool for 17 min. The LTO film was also deposited in the 6-inch LPCVD system following SMFL LTO recipe for 10 min. The thickness of each layer was: 1039Å for dry oxide, 560Å for Si_3N_4, and 480Å for LTO. Next, 1μm of Al was evaporated using the CHA Evaporator. For electrical contact the tri-layer was striped from the backside of the wafer. This was done using an oxide recipe on Drytek Quad 482 RIE system to remove the oxide layers and using SMFL nitride 4-inch recipe on 490 Lam

for 30 sec to remove the nitride layer. Photoresist was dispensed onto Al layer, then exposed on GCA using the CVTEST mask and then developed. Both coating and developing were done using program 1 on the SVG track. Next, aluminum was wet-etched until a clear pattern was visible. After the Al etch, the resist was stripped using acetone followed by a spin, rinse and dry. The wafer was cleaved into pieces for charge analysis. Details regarding the recipes are listed in appendix A.

Using the setup in Figure 3.1 the device was biased as shown in Figure 3.7 while the temperature of the chuck was increased to 200ºC. After 7 min, the heating element was turned off to allow cooling of the chuck while the DC bias was applied to the capacitor. Once the temperature of the chuck dropped to 35ºC the C-V test was performed. The polarity of the tested capacitor was reversed and the same thermal stress steps followed to obtain the second C-V curve.

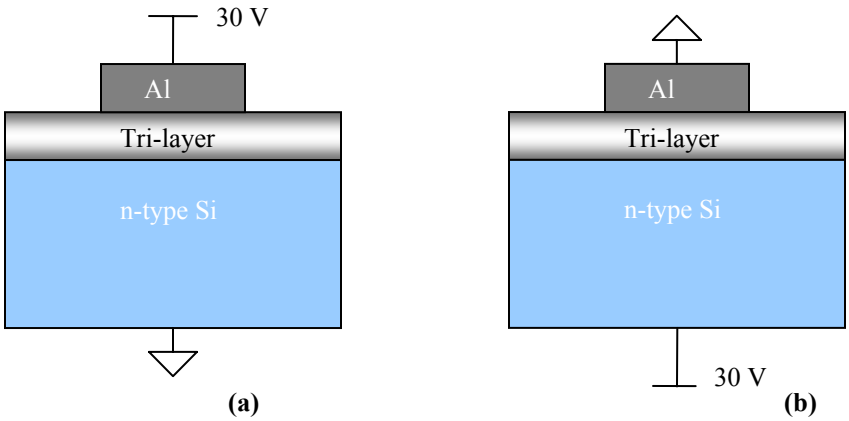

Figure 3.7: Polarity diagrams of the capacitor used in mobile ions experiment with (a) positive bias (accumulation mode), and (b) negative bias (inversion mode).

Results:

Figure 3.8 presents the effects of the thermal stress experiment on a capacitor under positive and negative bias. The measured voltage shift between the two curves was

1V, which is approximately equivalent to $10^{11}cm^{-2}$ of charge. The apparent change in C_{max} is attributed to inconsistence in the backside contact, which was not metallized.

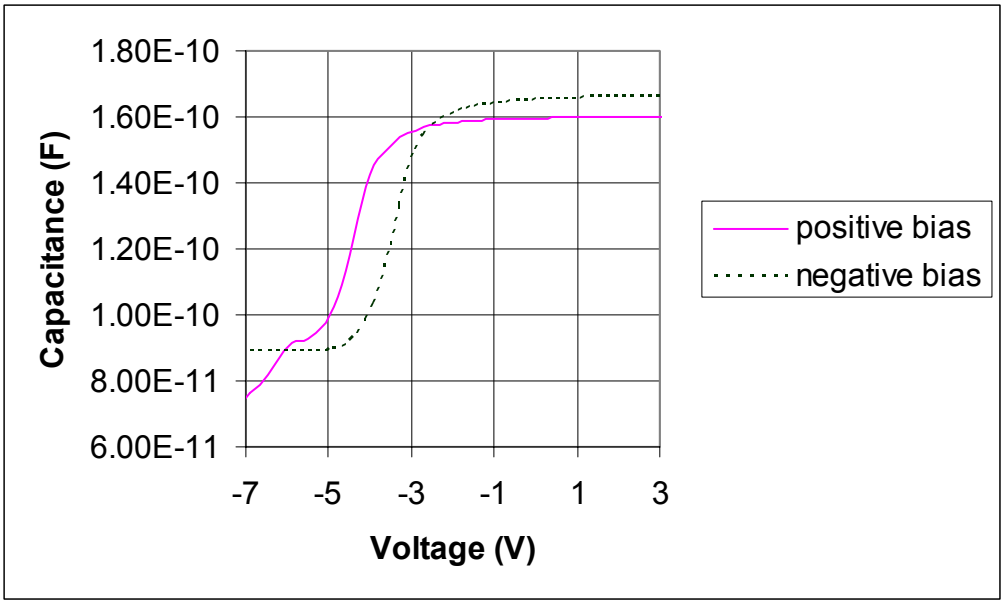

Figure 3.8: Plot of C-V curves representing voltage shift caused by presence of mobile ions within the tri-layer film stack.

Discussion:

The observed shift is most likely caused by the presence of mobile ions within the dry oxide, which is the layer closest to the substrate. This is because the nitride is effective in blocking mobile ions, and if any ions are within the LTO layer they have a much smaller influence on the C-V measurements. The 1V shift is minimal compared to the total injected charge acquired through high electric field injection. Therefore, the influence of mobile ions is neglected in following experiments.

3.6 High Electric Field Charge Injection

The effects of different charging signals on an ONO film stack are described in the following section. Initial and final C-V curves were recorded and plotted for analysis.

Throughout this study, the most effective charge injection process was determined. Also, a general understanding of the charging characteristics of the film stack was gained.

Procedure:

Utilizing the same wafer as in section 3.4, initial C-V curves were plotted and stored. Next, the wafer was charged using various input signals. For all charge injections, backside of the wafer was grounded. Also, the physical dimensions of the capacitors used for the measurements were $1x10^6$ μm^2. Once a given die was charged, the C-V traces were generated. By monitoring the flatband voltage shift in the C-V curve, the optimal charging potential was determined for the ONO devices.

Results:

Figure 3.9 shows a voltage shift when a negative DC bias was applied. The maximum voltage applied was -116V, causing voltage shift of about 12V. Figure 3.10 demonstrates charge injection done by applying a positive DC bias. The maximum voltage shift measured was 25V when 100V was applied. Also, at 120V stretching of the C-V curve took place, which is visible in Figure 3.10. A 120Hz rectified sinusoidal signal of positive polarity was used to charge the ONO capacitor dots. At 120V the maximum voltage shift of 38V was measured, as shown in Figure 3.11. Figure 3.11 also shows C-V curve stretching as well as a decrease in voltage shift.

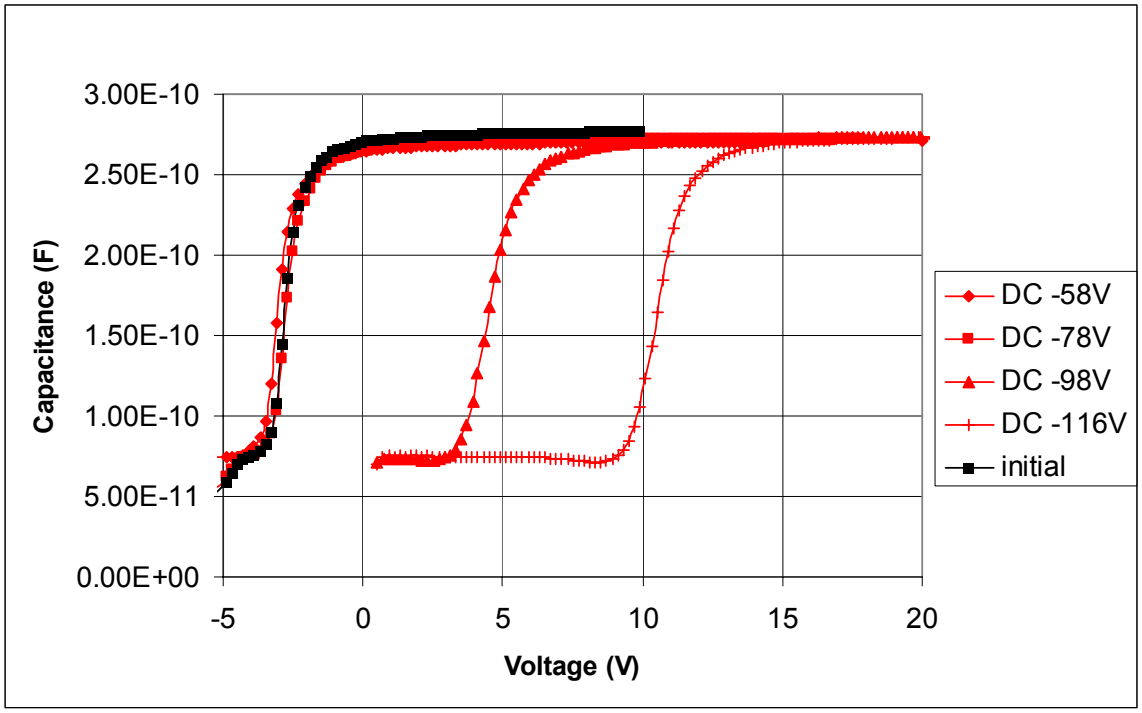

Figure 3.9: Plot of C-V curves showing flat band voltage shift due to charge inject with various negative DC biases.

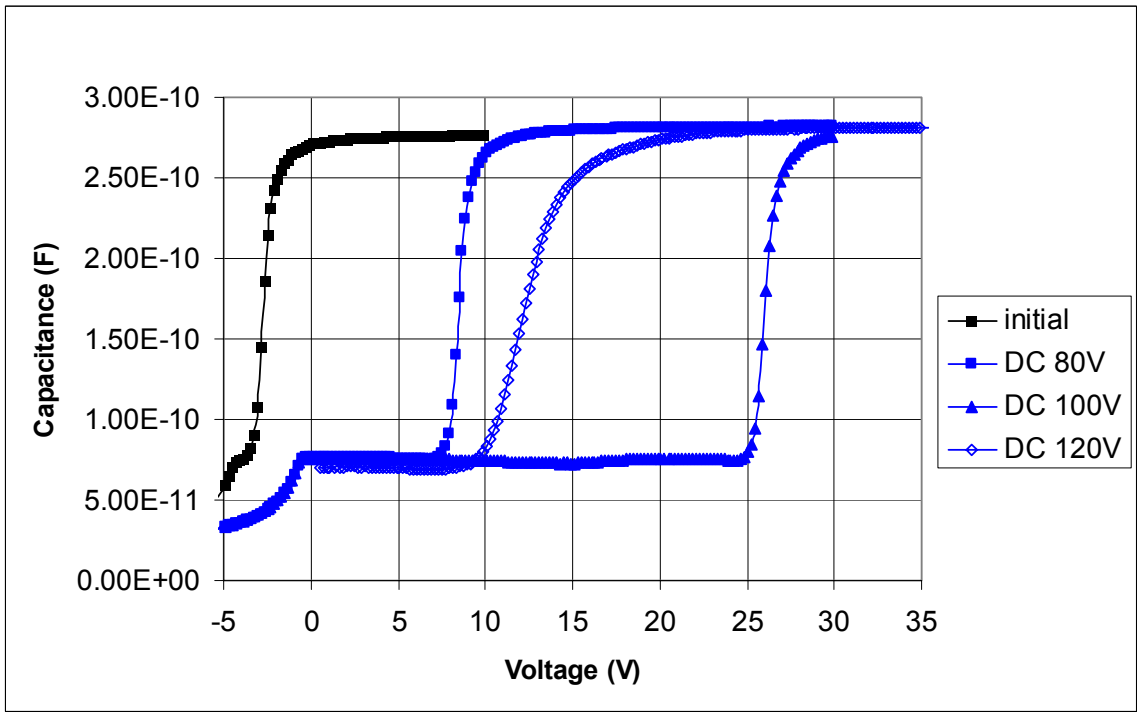

Figure 3.10: Plot of C-V curves showing flat band voltage shift due to charge inject with various positive DC bias where DC 120V C-V curve illustrates stretching as well as a decrease in voltage shift.

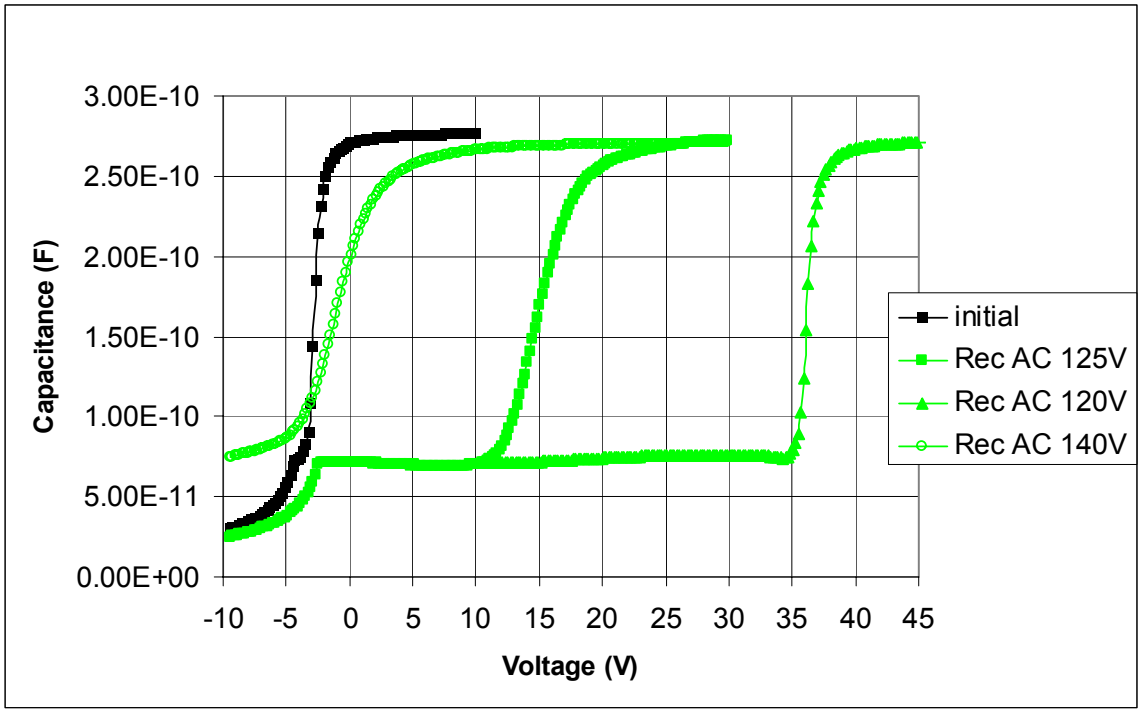

Figure 3.11: Plot of C-V curves showing flat band voltage shift due to charge inject using a positive rectified AC signal of various amplitudes, where Rec. AC 120V and Rec AC 140 V C-V curves illustrate stretching as well as a decrease in voltage shift.

It is also worth mentioning that the same experiment was performed on a p-type wafer. The experiment showed lower voltage shifts compared to the n-type wafer. Also, the positive rectified AC signal produced highest voltage shifts for the p-type wafer. A summary of these results is presented in Table 3.1.

	Max Voltage Shift	
	N-type	P-type
Negative DC	12 V at -116V	10 V at -140V
Positive DC	25 V at 100V	19 V at 140V
Positive AC	38 V at 120V	27 V at 160V

Table 3.1: Summary of the charge injection results for n and p type wafers.

Discussion:

Throughout the experiments, various degrees of charge injection into the ONO stack were measured. Also, stretching of the C-V curves at higher potential was observed.

Those curves do not show a catastrophic breakdown, however with a further increase in the potential, evidence of permanent physical damage becomes clearly visible, as shown in Figure 3.12.

Figure 3.12: Summary of the charge injection results for n and p type wafers.

The maximum observed voltage shift was 38V, and it was charged with a rectified sinusoidal signal of positive polarity. From these results, it appears that the rectified sinusoidal signal provides highest voltage shift compared to DC bias of positive polarity. The possible reason for higher proficiency in charge injection for rectified sinusoidal signal is charge relaxation. Every half cycle the amplitude of the signal drops to zero during which the injected charge redistributes it self spatially within the tri-layer. It is possible that during DC bias the charge build up can occur, limiting further charge injection. More experiments are needed to better understand this phenomenon.

A higher voltage shift was observed when a positive DC polarity was applied as opposed to a negative DC polarity. The difference in voltage shift between the negative DC voltage and the positive DC voltage could be attributed to charge distribution within the tri-layer stack capacitor. All the C-V curves show a positive voltage shift which is attributed to negative charge injection into the ONO stack. Therefore at positive bias, electrons are injected from the substrate and at negative bias the electrons are injected from the gate. Assuming that charge is trapped at the first oxide-nitride interface and

knowing that the interface closer to the substrate will have greater effect on the C-V measurements, it is reasonable to conclude that capacitor charged with a positive bias would have a greater voltage shift. To illustrate the significance of this effect, Eq. 2.11 is used. The oxide trap charge, which is assumed to be a uniform sheet of charge, is likely to be located at one of the two interfaces. The magnitude of trapped charge is much greater than the fixed charge density, interface charge, mobile charge, and ϕ_{ms}, and consequently these can be ignored in this calculation, which simplifies Eq. 2.11 to:

$$V_{FB} = -\gamma \frac{Q_{ot}}{C_{ox}} \qquad \textbf{(3.4)}$$

where γ represents the location of trap charges and is derived from the tri-layer film thicknesses as shown in Figure 3.13. The possible values of γ include 0.7 for the positive DC bias, and 0.3 in the case of negative DC bias.

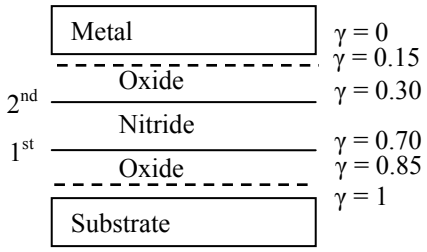

Figure 3.13: γ represents the centroid of charge for a film stack of 520Å oxide, 508Å nitride, 450Å oxide. In this case, four possible locations are indicated.

Considering the voltage shift of 26V obtained at 100V (refer to Figure 3.10) and voltage shift obtained at -100V (refer to Figure 3.9) and γ factors from Figure 3.13 , approximate charge densities are calculated and presented in Table 3.2 for comparison.

Tri-layer of 520Å oxide, 508Å nitride, 450Å oxide				
	γ	Sheet charge density	γ	Sheet charge density
Positive Bias	0.70	6.38e12 e/cm^2	0.85	5.22e12 e/cm^2
Negative Bias	0.30	2.80e12 e/cm^2	0.15	5.69e12 e/cm^2

Table 3.2: Charge density at possible locations within tri-layer film stack.

The sheet charge densities calculated using γ factors of 0.7 and 0.3 are of different values. Since voltage of the same magnitude was applied in each case, it is expected that the injected charge would be of similar magnitude. By adjusting the γ factor it was found that approximately same sheet charge density could be present within 170Å of the first oxide layer. Unfortunately, without another technique to measure either the total charge density or the charge distribution within the tri-layer film stack, the charge densities in Table 3.2 are only representative possibilities.

The experiments also showed a maximum voltage shift at a certain charging bias level; any further increase in the bias resulted in a decrease in the voltage shift and stretching of the C-V curves. This occurs when the electric field across an oxide film increases beyond 6MV/cm and Fowler-Nordheim injection takes place [9]. Refer to Figure 3.14 for visual aid. It is proposed that highly energetic electrons are created which overcome the oxide bandgap and produce electron-hole pairs by impact ionization. Some of the injected electrons progress to the opposite electrode, some are captured by trap sites, and the rest recombine with generated holes. The remaining generated holes move towards the cathode where they get captured near the Si-SO_2 interface [9]. The holes trapped at the Si-SiO_2 interface add to the net charge and cause a voltage shift as well as C-V curve stretching.

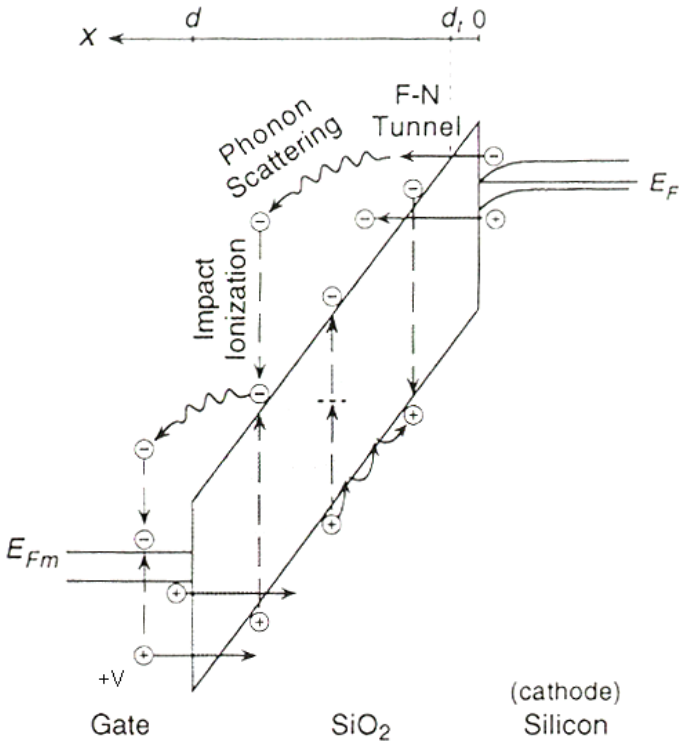

Figure 3.14: Band diagram of a possible process taking place during charge injection [9].

3.7 Charging of Thick Dielectric Films

According to the literature, various types of tunneling mechanisms contribute to charge injection into nonvolatile memory devices such as silicon-oxide-nitride-oxide-silicon (SONOS) [10-11]. The initial design focused on the tri-layer with oxide, nitride, and oxide films each 500Å thick; charge trapping was successful, possibly due to the tunneling mechanisms through the oxide layer and thermal emission through the nitride layer [12]. The maximum measured voltage shift was 45.5 V, charged using a rectified AC signal of 114 V.

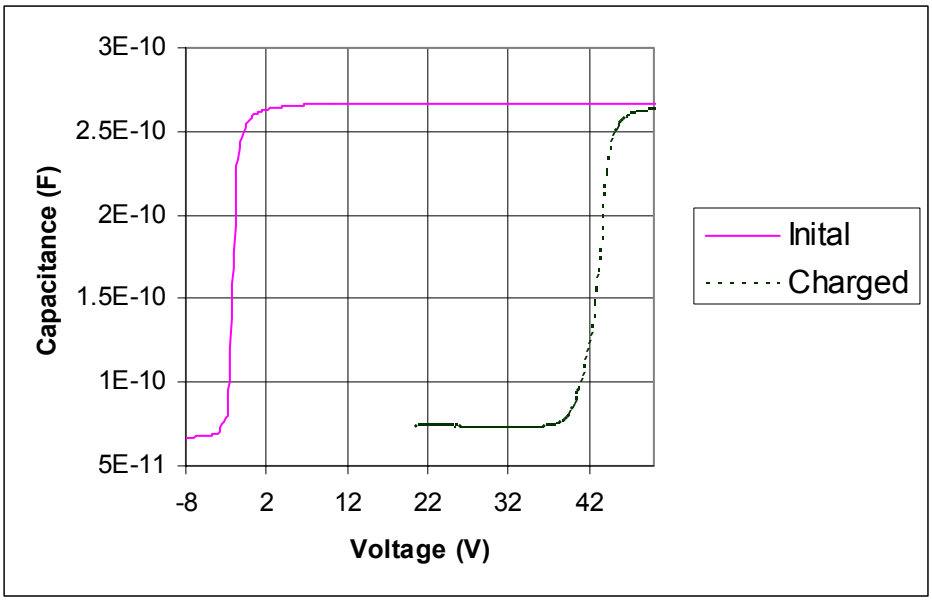

Figure 3.15: C-V plot showing maximum voltage shift for ONO tri-layer stack of ~500Å/500 Å/500Å. Charged using a rectified AC signal of 114 V which measured voltage shift of 45.5 V.

It was determined that a membrane made of a thicker film stack offered greater strength and minimized the total stress of the released device (refer to section 5.2 for details). In a new design with a much thicker ONO film stack the field assisted tunneling mechanism is no longer applicable, being limited to thinner oxide films [13]. This led to an experiment to determine the feasibility of injecting charge into 1000Å oxide film using the available equipment.

Sample preparation:

One piece of a wafer with a film stack consisting of 1039Å of dry oxide, 560Å of Si_3N_4, and 480Å of LTO was utilized for this study. Processing details are provided in procedure in Section 3.5.

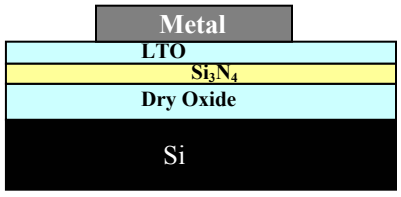

Figure 3.16: Capacitor made film stack consisting of 1039Å of dry oxide, 560Å of Si_3N_4, and 480Å of LTO.

Procedure:

Using the setup for C-V characterization, the initial curves were captured for four capacitors. The capacitors were then charged at 140V, 160V, 180V, and 200V using a rectified AC signal. The charged devices were measured again with the same C-V setup.

Results:

At 140V only a 5.5V shift was recorded. A shift of 17V was measured at 160 V, and the maximum shift of 33V was observed at 180V, as shown in Figure 3.17. At 200V a catastrophic breakdown occurred in the capacitor.

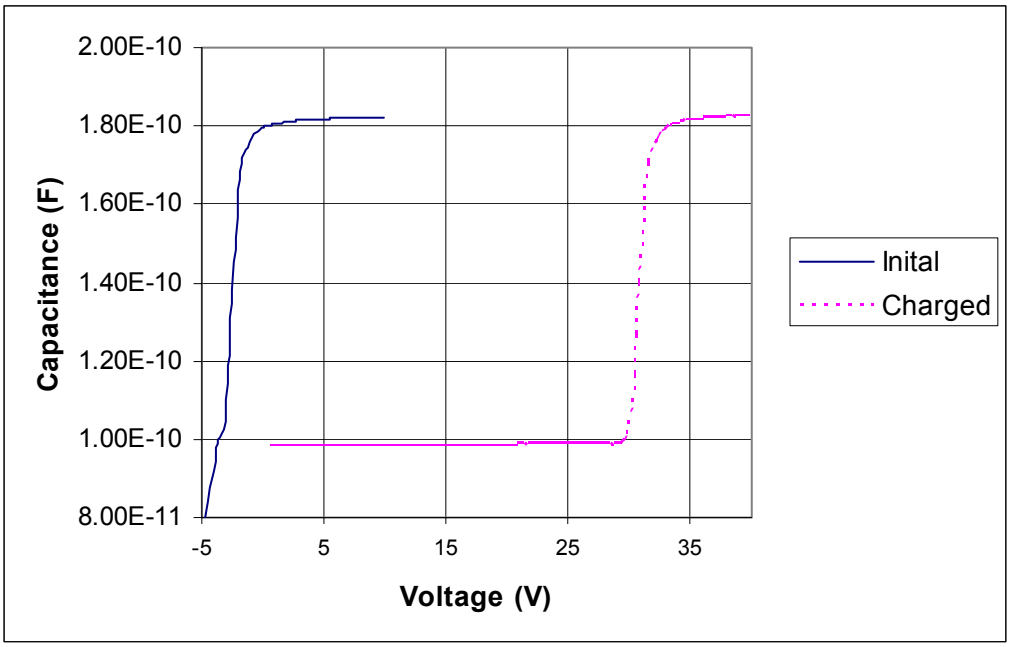

Figure 3.17: C-V plot showing maximum voltage shift for ONO tri-layer stack of 1039Å/560Å/480Å. Charged using a rectified AC signal of 180 V which measured voltage shift of 33 V.

Discussion:

This experiment has shown the feasibility of charge injection into much thicker oxide films. The possible charge transport mechanisms for a 1000Å oxide film are trap-assisted tunneling [13] and charge hopping [14].

The 33V shift is lower compared to the 45.5V shift in the case of the thinner ONO stack, but this could be attributed to the relative distance of the trapped charges from the Si and SiO_2 interface. As mentioned in Chapter 2, C-V measurements are more influenced by the charge located closer to the interface between the semiconductor and the insulator.

3.8 Retention of Charge

Lifetime of the trapped charge within electrets is one of the key parameters in device characterization. The electret charge lifetime is defined as charge decay over time and is approximated by an exponential relationship in the following equation.

$$q = q_o e^{\left(\frac{-t}{\tau}\right)} \qquad \textbf{(3.5)}$$

where τ is the relaxation time constant, t is the elapsed time, q_o the initial charge, and q the charge at time t. The relaxation time constant of electrets can range from 1 year to 10^5 years, depending on the kind of material and the method used to charge the film. For a Teflon FEP electret, τ is on the order of 50 to 200 years [15].

Procedure:

Another piece of the wafer with the 1039Å / 560Å / 480Å film stack was used for this study. The complete manufacturing process of the wafer is described in Section 3.5. After high field injection, three sets of C-V measurement were made.

To determine the lifetime constant Eq. 3.5 is utilized. By considering charge q_1 and q_2 measured at time t_1 and t_2 and assuming the constant temperature during all measurements Eq.3.6 was derived.

$$\frac{q_1}{q_2} = \frac{q_o}{q_o} \frac{e^{\frac{-t_1}{\tau}}}{e^{\frac{-t_2}{\tau}}} \tag{3.6}$$

By rearranging Eq. 3.6 and substituting the q_1 and q_2 for V_{FB1} and V_{FB2}, since charge is directly proportional to $C_{max}\,\Delta V_{FB}$ the final equation is:

$$\frac{V_{FB1}}{V_{FB2}} = e^{\frac{t_2 - t_1}{\tau}} \tag{3.7}$$

Using Eq 3.7 lifetime constant is derived

$$\tau = \frac{t_2 - t_1}{\ln\left(\frac{V_{FB1}}{V_{FB2}}\right)} \tag{3.8}$$

Results:

All collected data points were normalized and are plotted in Figure 3.18. The voltage shifts were extracted from the C-V curves and were used to determine the lifetime constant at room temperature by employing Eq 3.8.

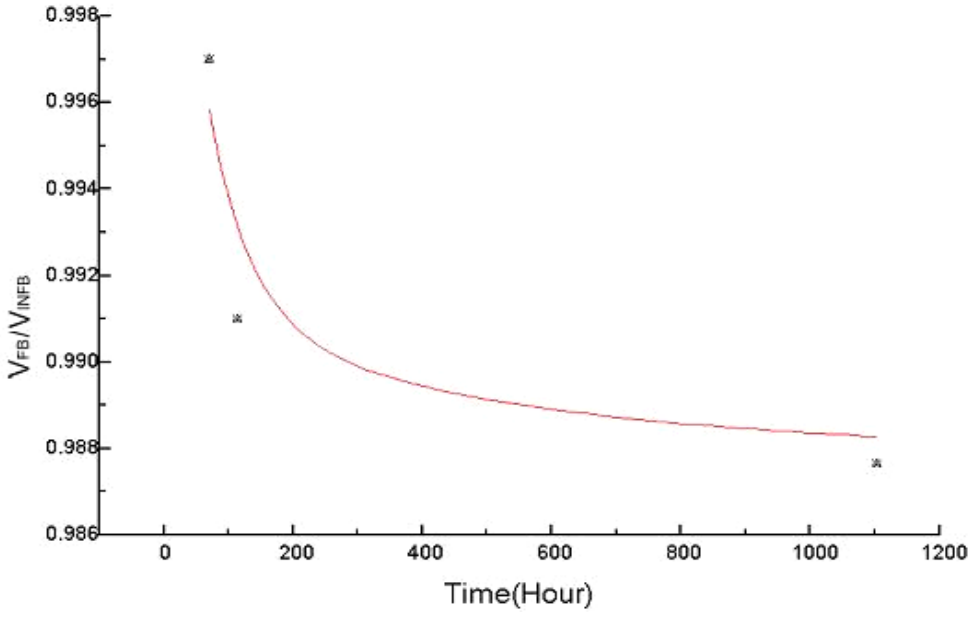

Figure 3.18: Charge retention within the ONO stack, shown by plotting the normalized voltage shift vs. time.

Discussion:

The extrapolated lifetime was approximately 18,000 hours, as derived from the values in Figure 3.18. Two years is a relatively short period for charge retention compared to other studies conducted with similar film stacks. For example Figure 3.19 demonstrates decay of four dual layer stacks made of oxide-nitride films and single oxide film, all charged using an isothermal process [16].

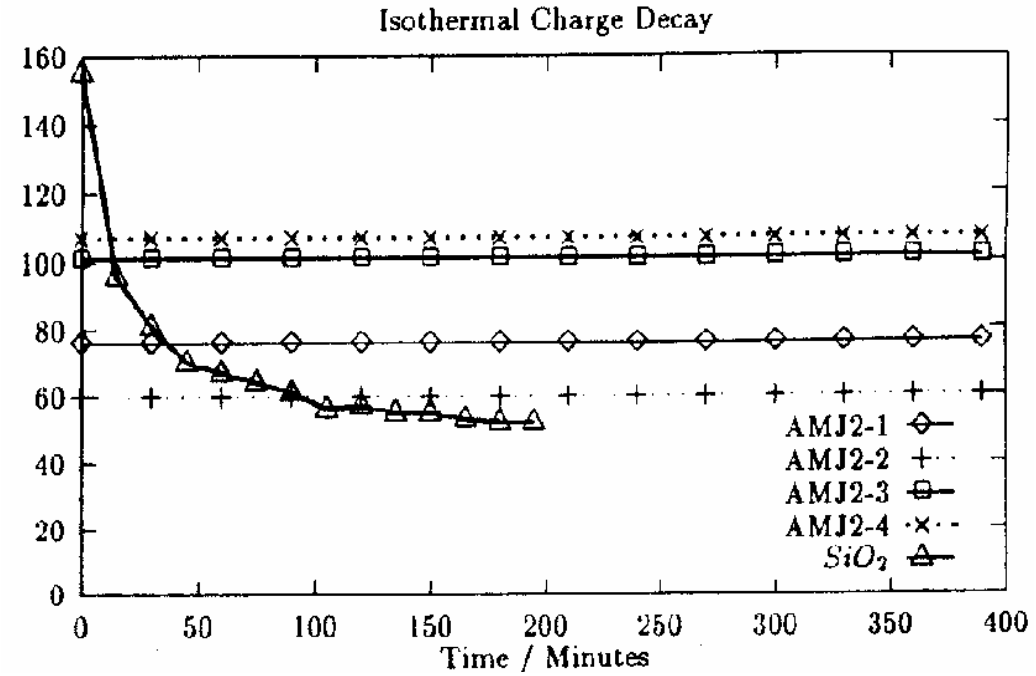

Figure 3.19: Normalized charge decay of oxide and oxide-nitride film. The nitride film thickness was 150nm for all four samples. Dry oxide thickness for AMJ2-1 was 150nm and AMJ2-2 was 250nm. Wet oxide thinness for AMJ2-3 was 250nm and for AMJ2-4 was 500nm. The surface potential was measured every 30 min at 300°C. None of the oxide-nitride film stacks showed any charge decay, effectively demonstrating high charge retention even at elevated temperatures. The decay curve observed corresponds to a single layer of oxide [16].

3.9 Thermal Detrapping

Experiments were performed to investigate the energetic distribution of the trap sites within the ONO stack. The trap site depth is characterized by its activation energy.

Since the charge loss is dependent on temperature through an Arrhenius relationship, the activation energy can be represented as follows:

$$R(T) = R_0 e^{\left(\frac{-E_a}{kT}\right)} \qquad \textbf{(3.9)}$$

In this equation, E_a is the activation energy, k is the Boltzmann's constant, T is the temperature in degrees Kelvin, R_o is the frequency factor, and R(T) is the rate constant at a given temperature, which in this case corresponds to the thermal relaxation of trapped charge.

Procedure:

A capacitor with film stack consisting of 1039Å of dry oxide, 560Å of SiN and 480Å of LTO was utilized for this study. The complete manufacturing process of the wafer is described in Section 3.5. A C-V measurement was taken before and after charging of the capacitor. The chuck used for voltage shift measurements has a heater, which was used to elevate the temperature of the wafer in increments of 10ºC up to 320ºC at intervals of 3 min. The wafer was C-V tested during each 3 min warm-up period. From the C-V curves voltage shift were determined.

To derive the rate constant, Eq. 3.7 was rewritten into Eq. 3.10 where $\tau(T)$ is temperature dependent variable and Δt is constant.

$$\frac{V_{FB1}}{V_{FB2}} = e^{\left(\frac{\Delta t}{\tau(T)}\right)} \qquad \textbf{(3.10)}$$

By substituting $\tau(T)$ with $\tau_0 e^{\frac{Ea}{kT}}$ into Eq.3.10 and the final equation is derived

$$\ln\left(\frac{V_{FB1}}{V_{FB2}}\right) = \frac{\Delta t}{\tau_0} e^{\left(\frac{-E_a}{kT}\right)} \qquad \textbf{(3.11)}$$

Temperature (C°)	V_{FB} (V)
20	20.40
130	21.2
140	21
150	20.44
160	19.89
170	18.97
180	18.25
190	17.34
200	15.62
210	14
220	11.27
230	10.6

Table 3. 3: Data points collected through thermal relaxation of a charged tri-layer capacitor experiment. V_{FB} obtained from C-V curves during incremental increase in temperature.

Result:

Table 3.3 presents data points obtained from thermal relaxation experiment. Data points from Table 3.3 are plotted in terms of $\ln\left(\frac{V_{FB1}}{V_{FB2}}\right)$ and $\frac{1}{kT}$ in Figure 3.20. A straight line was fitted through the plotted points with a slope of 0.6eV, which corresponds to the activation energy.

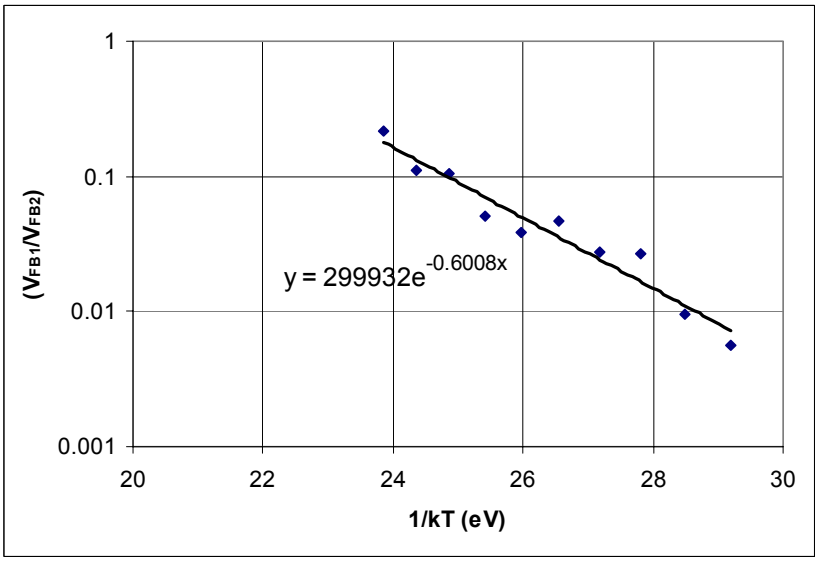

Figure 3.20: Plot of the rate constant vs 1/kT used to determine the activation energy. Data points plotted for 130°C to 230°C.

Discussion:

It is assumed that the potential applied during C-V measurements has a minimal impact on the activation energy measurements. This is based on previous high electric field charge injection experiments, which showed no charge injection when 25V was applied. Based on data points in Table 3.3, approximately 50% of the total charge was lost between 130ºC and 230ºC, which exhibits an activation energy of 0.6 eV. It is also quite possible for trapped charges to exist at deep energy levels, which could be experimentally determined at higher temperatures. This experiment was limited to 240ºC; however, once the system cooled down to room temperature the final C-V measurement was taken and is plotted in Figure 3.21, which reveals a voltage shift of approximately 5.7V after incremental heating of the sample up to 320ºC.

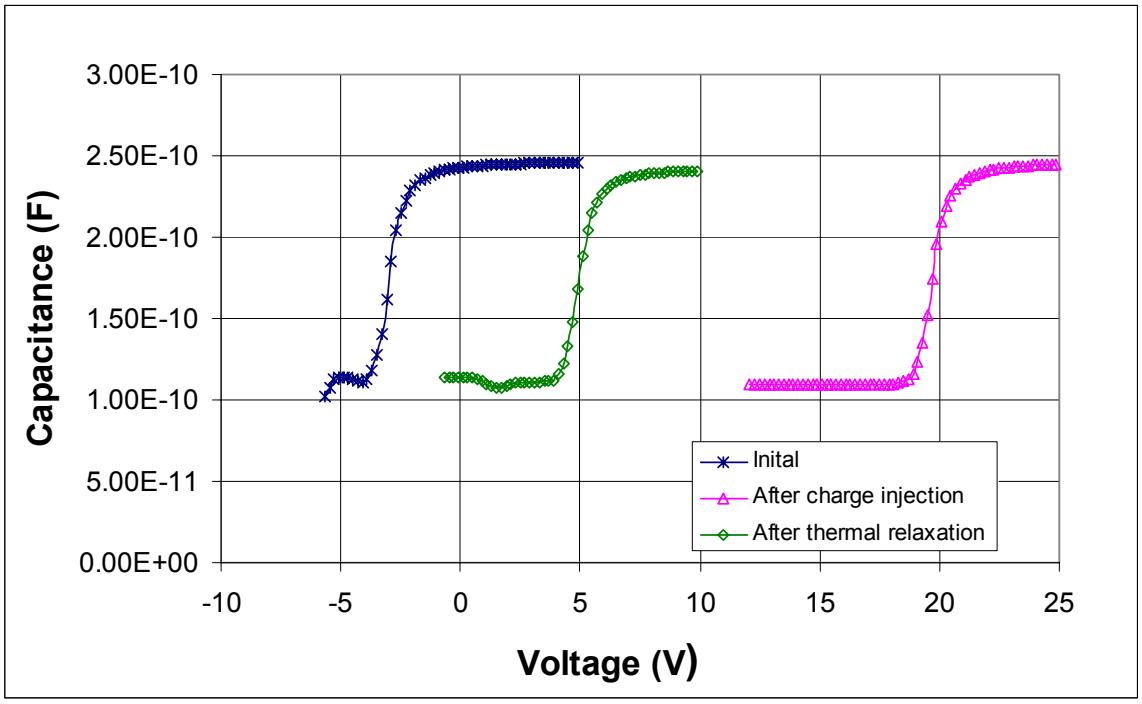

Figure 3.21: C-V measurement of tri-layer at the beginning of the experiment, after high field charge injection, and after cooling down to room temperature from 320ºC. All the C-V curves were performed at room temperature.

Interestingly one kind of defect found in floating gate non-volatile semiconductor memory (NVSM) devices has activation energy of 0.6eV. This defect is related to leakage of charge by oxide-hopping conduction [17]; it is expected that a hopping mechanism is operative within the studied film stack. More experiments are required to fully understand energetic distribution of other possible types of defects that might be present within ONO film stack. For optimal charge retention performance, the detrapping activation energy must be higher; NVSM devices exhibit a thermal activation energy of 1.4eV [17] which is associated with a thermal emission mechanism.

3.10 Summary

This work shows a successful charge injection and charge retention within the ONO film stack capacitors. The highest voltage shift of 45.5V was achieved with film stack on the order of 500 Å each. A film stack on the order of 1000Å/ 500Å/ 500Å LTO produced a 33V shift. Presence of mobile charge and fixed charge were measured, and the effective density was an order of magnitude smaller than the charge injected using a high electric filed. In addition, the lifetime of the trapped charge was estimated to be 18,000 hours, and demonstrated a thermal activation energy of 0.6eV. More measurements, such as total charge and space charge distribution, are required to properly characterize the ONO device.

By knowing a total charge density or embedded charge distribution within tri-layer film stack and with help of the model which will be described in Chapter 4, one can estimate the actuation voltage for a given device. Chapter 4 also offers insight into the operation of the device.

References

1. S. Wolf and R.N. Tauber, “Silicon processing for the VLSI ERA Vol 1- Process Technology” Lattice Press, Second Edition, 2000, pg 203.

2. Takahiro Makino, “Composition and Structure Control by source gas Ratio in LPCVD SiNx” Journal of Electrochemical Society Volume 130, Number 02 February 1983, pg 40-454

3. E.H. Nicollian and J. R. Brews, “MOS (Metal Oxide Semiconductor) Physics and Technology “, John Wiley & Sons, 1982, pg. 741

4. B.Stannowski, J.K. Rath and R. E.I. Schrop, ”Hot-Wire Silicon Nitride for Thin – Film Transistors” IEEE workshop/ Proceedings of the SAFE, Nov. 2000, pg145-148

5. Jiankang Bu and Marvin H. White “Retention Reliability Enhanced SONOS NVSM with Scaled Programming Voltage”, Aerospace Conference Proceedings, IEEE, Volume 5, 2002, pg 2383- 2390

6. Kin P. Cheung,” Soft breakdown in thin gate oxide-a measurement artifact”IEEE/ 41st Annual International Reliability Physics Symposium 2003, pg 432-436

7. T. Hori, “Gate Dielectric and MOS ULsis : Principles, Technologies, and Applications” Springer Series in Electronics and Photonics, Vol 34, pg 55-56

8. Dietter K. Schroder, “Semiconductor Material and Device Characterization” 1998, John Wiley & Sons pg 344-368

9. T. Hori, “Gate Dielectric and MOS ULsis : Principles, Technologies, and Applications” Springer Series in Electronics and Photonics, Vol 34 pg 169

10. Jiankang Bu, Marvin H. White, “Electrical characterization of ONO triple dielectric in SONOS nonvolatile memory devices”, Solid State Electronic 45, 2001, pg 47-51

11. Yang (Larry) Yang, Ansha Purwar, Marvin H. White, “Reliability considerations in scaled SONOS nonvolatile memory devices”, Solid State Electronic 43, 1999, pg 2025-2032

12. William D. Brown and Joe E. Brewer, “Nonvolatile Semiconductor Memory Technology” IEEE Press, 1998, pg 9

13. Robert F. Pierret, “Semiconductor Device Fundamentals”, Addison Wesley, 1996 , pg 268

14. T. Hori, “Gate dielectrics and MOS ULSIs” Principles, Technologies, and Applications” Springer Series in Electronics and Photonics, Vol 34, pg44-47

15. Bozena Hilczer and Jerzy Malecki, “Studies in Electrical and Electronic Engineering 14: Electrets” Elsevier, New York, 1986, pg 309

16. Houman Amjadi and Gerhard M. Sessler, “Inorganic electret layer for miniaturized devices” Electrical Insulation and Dielectric Phenomena, Annual Report., Conference on , 22-25 Oct. 1995 Pages:668 - 671

17. William D. Brown and Joe E. Brewer, “Nonvolatile Semiconductor Memory Technology” IEEE Press, 1998 pg 375

CHAPTER FOUR: DESIGN AND MODELING OF EMBEDDED CHARGE MICROSWITCH

4.1 Theory of Operation

The ultimate goal of RF microswitch research is to produce devices that are small, lightweight, and low cost, while still offering a high level of electrical and mechanical performance. They need to be compatible with standard integrated circuit (IC) fabrication technology, self packaged, and most importantly be able to operate from typical IC power supplies, which are in the range of 3-5 volts. This chapter provides the theoretical background for designing RF microswitches that meet these demands.

The main component of the proposed RF microswitch design is an electret cantilever. An electret can be created by applying a high electric field to a stack of two different dielectrics: SiO_2 and Si_xN_y in this work. As discussed in Chapter 3, the electric field causes charge injection and the charge remains trapped at the interface between the two insulators and/or in the nitride film. Once charged and sealed, the cantilever is actuated by an external voltage applied to the electrodes. Figure 4.1 shows a schematic of the proposed device.

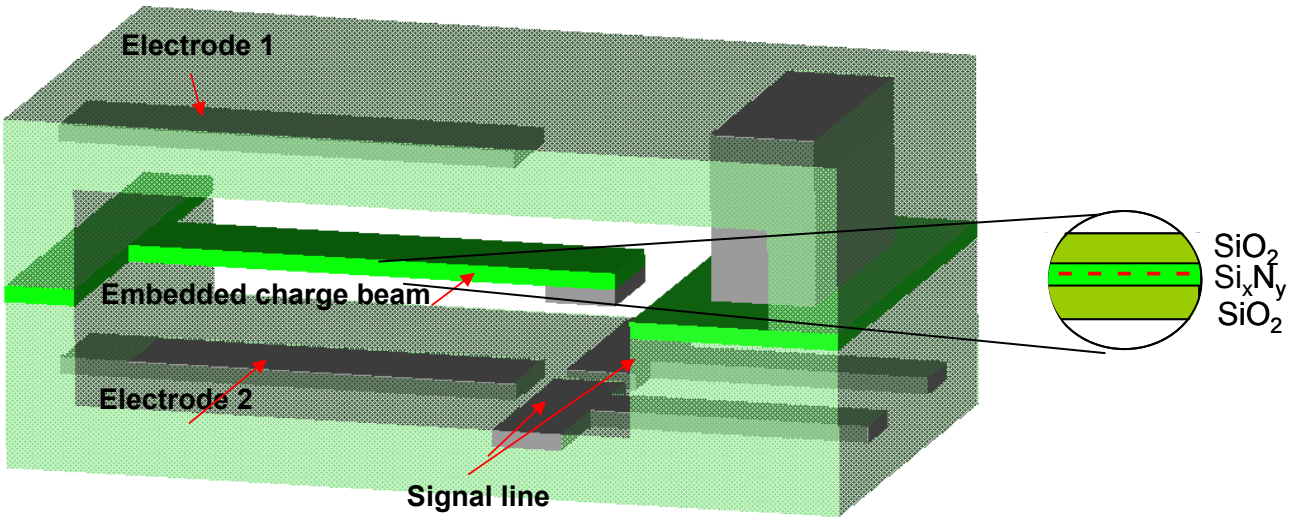

Figure 4.1: MEMS switch based on embedded charge concept using a tri-layer film stack for the cantilever.

4.2 One-Dimensional Model

The modeled system is a simplified representation of the embedded charge microswitch shown in Figure 4.1, and it facilitates the analysis of the electrostatic properties and the effect of the embedded charge on the system. Also, an analogy between the derived model and a typical parallel plate capacitor model is shown to better illustrate the advantages of the embedded charge.

A simplified representation of the embedded charge design is presented in Figure 4.2, where the top and bottom plates are metal electrodes of opposite polarity with a thin sheet of positive charge positioned in between. The two electrode planes are fixed in space while the sheet charge is free to move in the z direction. To simplify calculations,

the electric field is assumed to be constant in the x-y plane, fringing effects are ignored, and the sheet of charge is assumed to have a uniform charge distribution. Also, free space permittivity is assumed for the dielectric materials.

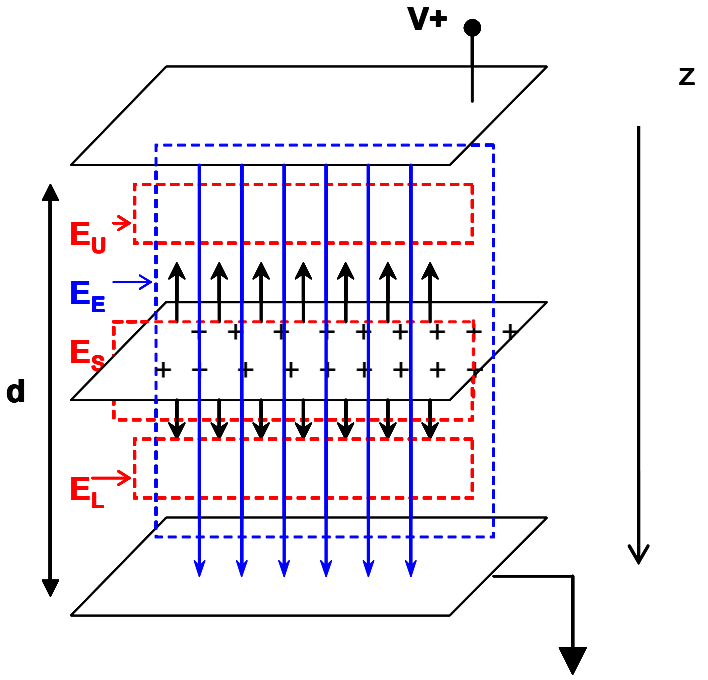

Figure 4.2: Parallel plate capacitor with embedded charge.

The dashed rectangles in Figure 4.2, labeled as E_U (E-field upper) and E_L (E-field lower) represent the total electric field in those regions, where E_E represents the E-field component due to the voltage applied across the metal electrodes. E_S is the E-field component due to the sheet charge plane. By superposition, the electric fields in the regions above and below the charge plane, E_U and E_L respectively, are given below.

$$E_U = E_E + (-E_S) \quad \textbf{(4.1)}$$

$$E_L = E_E + E_S \quad \textbf{(4.2)}$$

Using a Gaussian surface, the electric field associated with the plane of sheet charge is calculated as

$$E_S = \frac{\rho}{2\varepsilon_0}, \tag{4.3}$$

where ρ represents the sheet charge density and ε_o free space permittivity. Another way of expressing the electrostatic conditions in the structure is with the potential drop between the metal electrodes. By Kirchhoff's voltage law, the sum of the potentials in regions E_U and E_L is equal to the external potential, V, applied across the two electrodes.

$$V = E_L z + E_U (d - z) \tag{4.4}$$

where z is the displacement variable. Combing Eq. 4.1, Eq. 4.2 and Eq. 4.3, and substituting into Eq.4.4 yields:

$$V = \frac{\rho}{2\varepsilon_0}(d - 2z) + E_E(d) \tag{4.5}$$

Rewriting Eq. 4.5 gives the expression for E_E:

$$E_E = \frac{1}{d}\left(V + \frac{\rho}{\varepsilon_0}\left(z - \frac{d}{2}\right)\right) \tag{4.6}$$

Finally, the force acting on the charge plane can be expressed in terms of electric field and sheet charge density.

$$\frac{F}{A} = E_E \rho \tag{4.7}$$

Combing Eq. 4.6 and Eq.4.7, Eq. 4.8 is obtained, which represents the total force exerted on the charge plane as a function of position.

$$F = \frac{A\rho}{d}\left(V + \frac{\rho}{\varepsilon_0}\left(z - \frac{d}{2}\right)\right) \tag{4.8}$$

To illustrate the advantages of the embedded charge parallel plate capacitor a comparison is made with a typical parallel plate capacitor (refer to Chapter 1). The

comparison looks at the plane displacement vs. the applied voltage. To enable such comparison a spring force is added to both Eq. 4.8 and Eq. 1.4 resulting in equation 4.9 which represent the embedded charge capacitor and equation 4.10 which represents the standard capacitor

$$F = k\left(z - \frac{d}{2}\right) = \frac{A\rho}{d}\left(V + \frac{\rho}{\varepsilon_0}\left(z - \frac{d}{2}\right)\right) \tag{4.9}$$

$$F = kz = \frac{V^2 A\varepsilon_0}{2z^2} \tag{4.10}$$

where k is the spring constant which represents mechanical properties such as Young's Modulus, the moment of inertia, and the length of the beam. The specific value of the spring constant is related to the boundary conditions for a given cantilever design and force distribution applied to the beam [1]. For these calculations the spring constant (k) was taken to be 1 Nm, used in both relationships given in Eq. 4.9 and 4.10.

Cross sections of two capacitors (1-D models with and without embedded charge) are presented in Figure 4.3. The diagrams include the mechanical restoring force represented by springs connected to the movable plates. In this arrangement, the bottom plate is stationary while the top plate is free to move. In case of the embedded charge capacitor both bottom and top electrodes are stationary while the middle plate moves. For both capacitors the initial gap between the moving planes and the metal electrodes is given by distance (d/2).

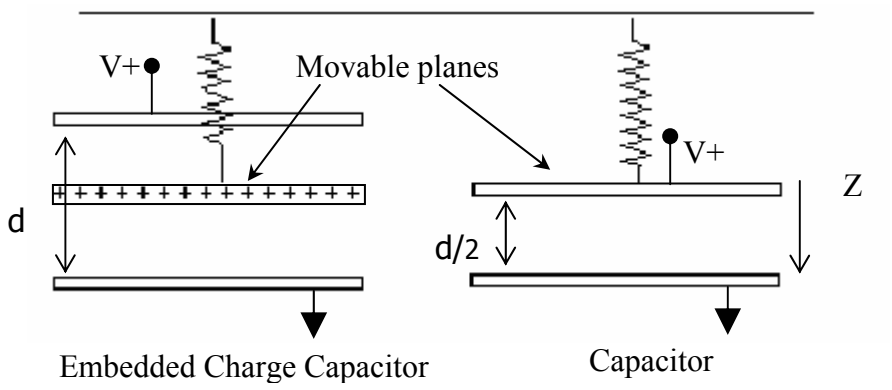

Figure 4.3: Physical representation of the two parallel plate capacitors with and without embedded charge.

The parameters used for the purpose of comparison are listed in Table 1. Parameter ρ is the sheet charge density is equivalent to 1.31×10^{12} cm^{-2}, which is a reasonable value compared to an as-deposited fix charge density of ~ 10^{11} cm^{-2} (refer to Chapter 2) or compared to charge density of ~ 7×10^{12} cm^{-2} (refer to Chapter 3) obtained from the charge injection experiments within the ONO film stack. The designed area for the capacitor plate is $A = 2.5 \times 10^{-8} cm^2$ representing the area of a cantilever of following size: 0.5μm wide and 5μm long.

Constant	Value	Units
P	1.85×10^{-7}	C/cm^2
D	1×10^{-4}	cm
ε_o	8.85×10^{-14}	F/cm
A	2.5×10^{-8}	cm^2

Table 4.1: Values used in equations 4.9 and 4.10

The plot in Figure 4.4 shows the relationships between the applied voltage and the displacement of the movable planes. As illustrated in Figure 4.3, the initial position of the planes is z=0 and when the plane contacts the negative electrode the position is d/2, which in this case is 0.5 μm.

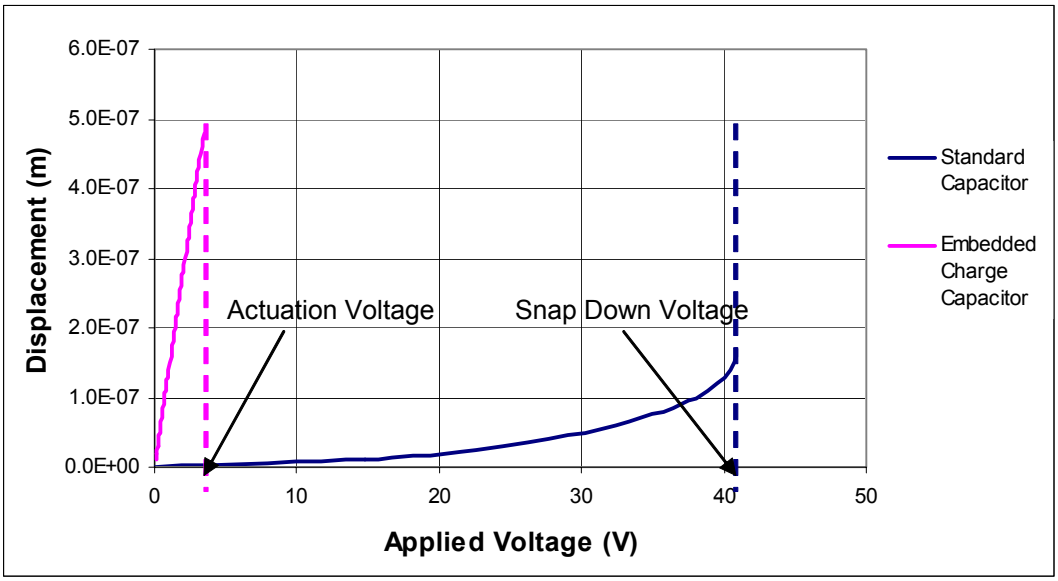

Figure 4.4: Comparison of embedded charge and conventional parallel plate capacitor

The displacement vs. applied voltage relationship is quadratic for a conventional capacitor plot. For a given electrode voltage, the attractive force between the plates is increased as the distance is reduced, and at 1/3 the way down the quadratic nature of this relationship overcomes the mechanical restoring force and the beam snaps down. The snap-down occurs approximately at 42V for the conventional capacitor and is represented by a dotted line in Figure 4.4. On the other hand, the embedded charge structure demonstrates actuation of 4V and a linear relationship between the applied voltage and the displacement. The 4V of actuation potential could be reduced even further with larger embedded charge density, however with a further increase in trap charge density the beam will no longer operate in the linear mode. To illustrate how the variation in embedded charge density within a capacitor affects actuation voltage, a relationship between the injected charge and applied voltage is plotted in Figure 4.5. The curve was plotted using the parameters listed in Table 4.1, assuming displacement of beam to the lower electrode.

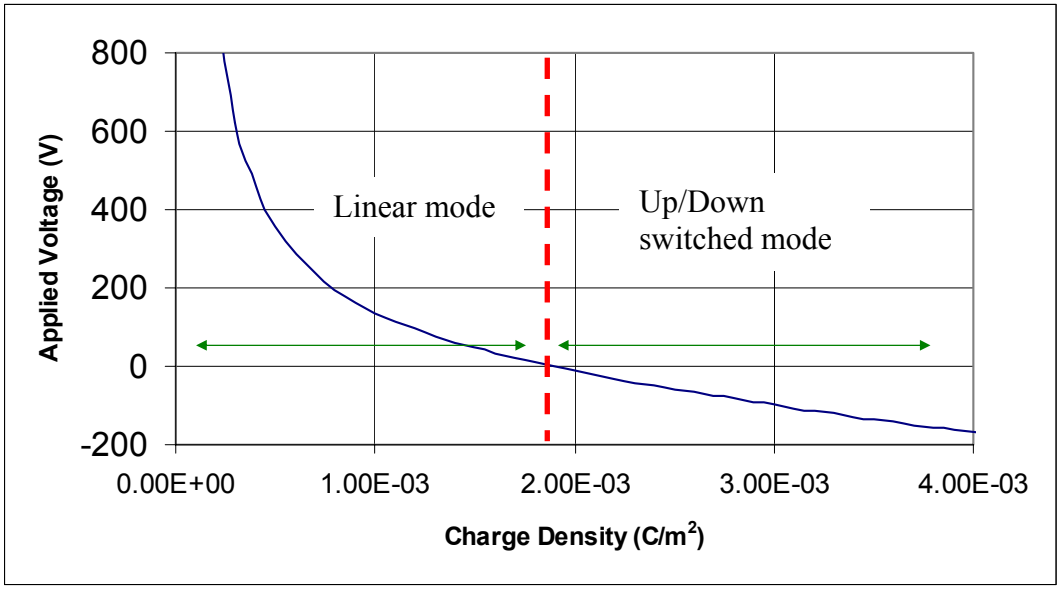

Figure 4.5: Relationship between injected charge density and the actuation voltage for device parameters noted in Table 4.1.

A dashed line in Figure 4.5 marks two different modes of operation of the embedded charge capacitor. The curve to the left of the dashed line illustrates the linear mode. The curve represents the potential required to lower the beam to the bottom electrode for a given charge density. The linear mode of operation can be utilized in a variety of analog circuit applications which need high frequency variable capacitors. Some of the examples include voltage-controlled oscillators, band select filters, and many other tuned microwave circuits. The curve to the right of the dashed line represents the up/down switched mode of operation, in which the beam is either at the upper or the lower electrode even if no potential is applied. To move the beam to the opposite electrode, a potential of appropriate polarity is required, in this case a negative voltage as shown in Figure 4.5. Note, that as charge density increases, higher potential is required to snap the beam to the opposite electrode. Applications for the up/down switched mode of operation could be found in digital circuits due to its binary behavior. In addition,

eliminating static power dissipation and reducing dynamic power dissipation are important design considerations in digital design, which can be satisfied by the switch with a higher injected charge density.

By rewriting Eq. 4.9 one could better illustrate the behavior of the embedded charge capacitor. Equation 4.11 shows two expressions.

$$F_{total} = \left(\frac{A\rho^2}{\varepsilon_0 d} - k \right)\left(z - \frac{d}{2} \right) + \frac{A\rho}{d} V = 0 \qquad \textbf{(4.11)}$$

The expression $\frac{A\rho}{d} V$ includes the applied voltage and the sheet charge terms and is constant. The expression $\left(\frac{A\rho^2}{\varepsilon_0 d} - k \right)\left(z - \frac{d}{2} \right)$ includes the sheet charge and the spring constant of the beam. Both terms in this expression are dependent on the beam's displacement. Also, the two terms indicate the mode of operation for a given device. In the linear mode the spring constant is of a greater magnitude compared to the charge density, which assures beam control at any position.

$$\frac{A\rho^2}{d\varepsilon_0} - k < 0$$

In the switch mode the sheet charge density term is greater than the spring constant, and the spring constant has little effect on the displacement of the beam. As a result the beam moves abruptly, either in up or down, depending on the applied voltage polarity.

$$\frac{A\rho^2}{d\varepsilon_0} - k > 0$$

When both terms are equal, in theory the beam can be located anywhere and it will remain in that location. However, in reality such equilibrium is impossible to maintain, and the beam would be either at the upper or lower electrode.

4.3 Summary

The model presented in this section provides some insight on the operation and performance of the RF microswitch. The parameters used in the model were based on a preliminary design of an RF microswitch; final device dimensions will depend on specific fabrication details which will be described in Chapter 5. Chapter 5 also will provide information on thickness variation and total stress of the films used in the final device.

Reference

1. F.P. Beer and E.R. Johnston," Mechanics of Materials", Second Edition McGraw-Hill, New York, 1992, pg 486-525

CHAPTER FIVE: FABRICATION OF THE ELECTRET MEMBRANE

5.1 Introduction

Applications of electrets in MEMS have been found primarily in microphones. Some are constructed by spinning a thin layer of Teflon [1-2] or polytetrafluoroethylene (nano-PTFE) polymer [3] on an appropriate substrate; some use Mylar foil attached by an adhesive polymer to the device framework [4]. All of the above processes require additional materials, fabrication steps, and tools to create a microphone structure. By using common IC fabrication materials like SiO_2 and Si_3N_4, the production of electrets can be made more economical. Also, a design with multiple layers of SiO_2 and Si_3N_4 has a potential for much higher charger storage capacity compared to the conventional electrets.

The discussion will now focus on the fabrication of the cantilever for the RF microswitch. The proposed design consists of a tri-layer membrane, made of oxide, nitride and oxide (ONO) films. The membrane has injected charge and is suspended over the etched-through silicon substrate. Figure 5.1 shows the final structure with a probe, which would be used for testing. Note, that the figure is not drawn to scale, since thickness of the membrane is about a thousand times less then the silicon substrate or the probe diameter.

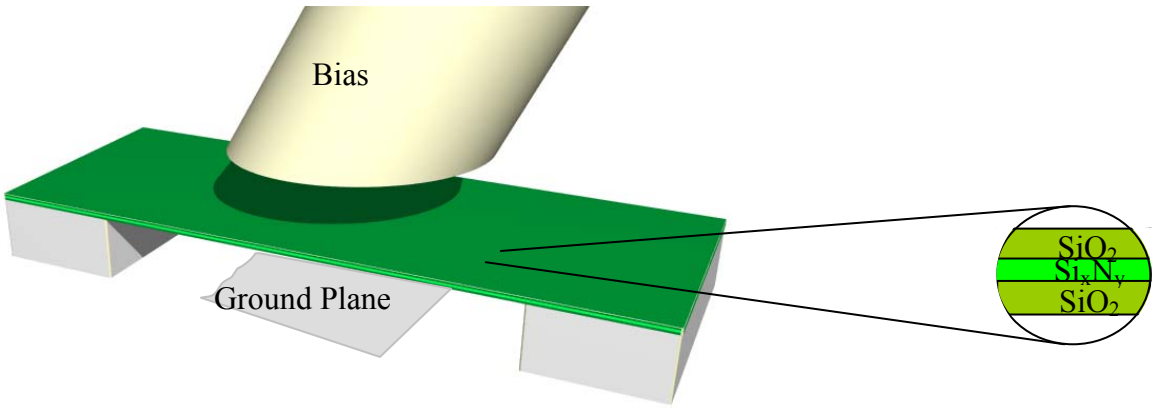

Figure 5.1: Membrane Design where the membrane is composed of oxide-nitride-oxide film stack.

5.2 Membrane Fabrication

The goal of these processing experiments was to develop relatively simple method of fabricating a tri-layer membrane as a starting point for analysis which could be further optimization into a microswitch. In the following section, the results of the processing experiments and the corresponding discussions, as well as detailed descriptions of the structure fabrication steps are presented.

5.2.2 Processing Development

A) Masking Layer

In order to selectively etch through about 500μm of silicon substrate, a masking layer is needed. There are numerous materials, which could be utilized as a masking layer; however photoresist offers some important benefits. Specifically, by using a photoresist as a masking layer a number of processing steps can be eliminated. In addition it offers design process flexibility and protection from deep reactive ion etch (DRIE).

According to Stanford Nanofabrication staff, selectivity ratio of resist to silicon is 75:1 and photoresist etches at about 250-600Å/min, depending on the post-exposure

treatment. Thick resist of about 7μm or more is recommended for etching through a 500μm thick silicon wafer [5].

In this experiment AZ 9260 photoresist was used, which can provide a coat of up to 17 μm thick. Using recommendations from the data sheet the first masking layers were processed with the following parameters: soft bake time of 2 min at 110ºC, exposure dose 1500mJ/cm^2 and develop time of 2 min. Baking temperature of 110ºC proved to be too high causing the surface of the photoresist to become rough, as it is show in Figure 5.2. Based on these observations, the soft bake temperature was lowered to 90ºC. The exposed wafers were under-developed, and as a result the exposed resist did not clear completely. It was determined that the optimal develop time is 4 to 5 minutes. Figure 5.3, shows a successful pattern transfer. The bright area is the silicon surface and the gray region is the 10μm thick resist. Curing of the resist presented yet another issue due to non-uniform cure.

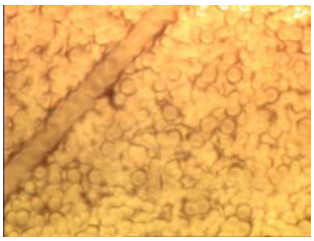

Figure 5. 2: Burned resist

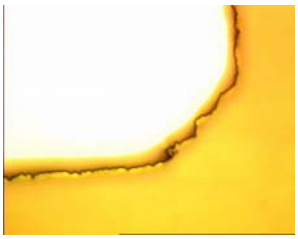

Figure 5.3: Successful pattern transfer

After the first DRIE run, the wafer revealed a pattern of cracks across a wafer, which corresponded to a non-uniform heat transfer from the hotplate. In the subsequent runs the wafers were baked in Hereaus oven for 30 min at 125ºC with good results. The final recipe of this process is included in appendix A. It should be mentioned that the resist thickness before curing is approximately 10μm, but after 30 min of cure, the film

thickness is reduced to about 8μm. This thickness proved to be sufficient to withstand etch-through of a silicon wafer using the DRIE process.

B) Thin Film Stress Investigation

Stress is always present in thin films, even if no external load is applied. Stress in a film can be either compressive or tensile. The compressive stress elongates the film parallel to the substrate causing the substrate to buckle. The tensile stress contracts the film at the substrate causing substrate to the curve inwards.

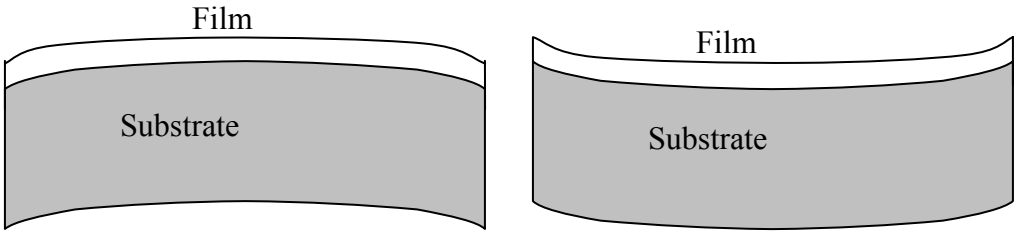

Figure 5.4: (a) Tensile stress **(b) Compressive stress**

The total stress comprises of external stress, thermal stress and intrinsic stress.

$$\sigma_{total} = \sigma_{ext} + \sigma_{th} + \sigma_{\text{int}} \qquad \textbf{(5.1)}$$

External stress refers to the external pressure applied to the film, which can be the result of being in contact with another film. The thermal stress results from the difference in coefficients of thermal expansion between the film and the substrate. Films which are prepared at an elevated temperature and then cooled to the room temperature will be thermally stressed. The thermal stress can be represented by Eq. 5.2 [6],

$$\sigma_f(T) = \frac{(\alpha_s - \alpha_f) * \Delta T * E_f}{1 - v_f} \qquad \textbf{(5.2)}$$

where α_s and α_f are linear coefficients of thermal expansion for the substrate and the film, ΔT represents the temperature difference between the process temperature and room temperature, E_f is Young's modulus of the film and v_f the Poisson's ratio of the film.

The intrinsic stress is much more complicated to represent since it can be affected by numerous factors such as film thickness, deposition rate, deposition temperature, ambient pressure, method of film deposition, type of substrate, thermal cycling, etc. As an example, Chen et al. [7] show effects of thermal cycling on intrinsic stress in silicon dioxide. In this paper, the SiO_2 film is relaxed through thermal cycles. After completing a thermal cycle the net change of thermal stress should be zero. However, that was not always the case observed due to the intrinsic stress. This finding is consistent with the literature [8] where stress of oxide film can vary from tensile to compressive depending on the process conditions.

Several models that explain the origin of the intrinsic stress have been proposed, but there is no closed-form quantitative model. Therefore, to design a membrane with minimal stress, the mechanical properties of the ONO stack need to be investigated experimentally.

The initial design of the tri-layer called for a thickness of 500Å for each layer. The actual deposited thicknesses were LTO 566Å, SiN 604Å, and LTO 638Å. The wafer was patterned with masking photoresist and etched in the STS DRIE system. The etch process was terminated after just 375 cycles due to the rupture of the membranes which were partially released. The recipe details are available in appendix A. The photograph in Figure 5.5 shows examples of a burst membrane and a structure that was not

completely released. The premature rupture could be caused by the stress present within the tri-layer combined with over-etching of the ONO stack.

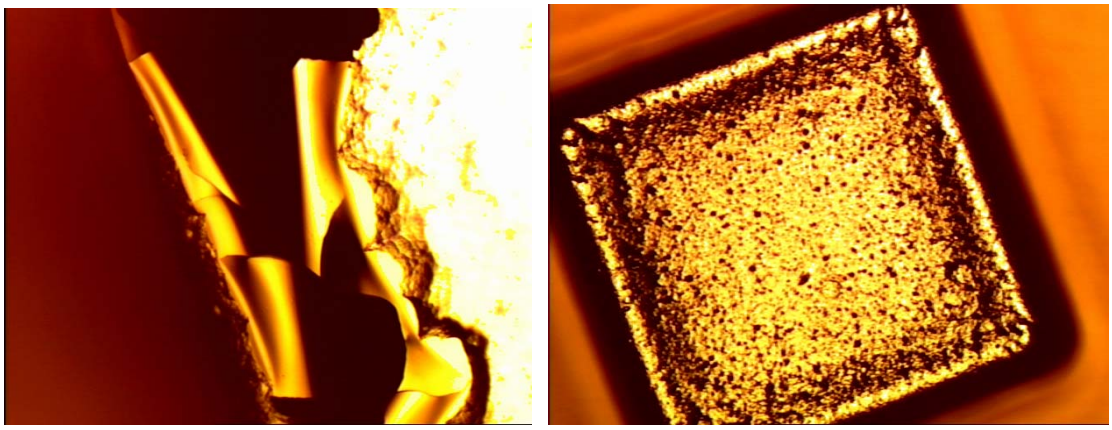

Figure 5.5: Backside of a wafer after deep silicon etch (a) partially released structure (b) not yet released structure.

Subsequently an experiment was designed to determine the minimal stress conditions and assure greater film strength by varying thicknesses of the tri-layer films. The design was reduced to a single-nitride thickness and three different oxide thicknesses. The design matrix is displayed in Table 5.1.

Film Stack	First Oxide	Nitride	Second Oxide
1	1000 Å	500 Å	1000 Å
2	1500 Å	500 Å	1500 Å
3	2000 Å	500 Å	2000 Å

Table 5.1: Design matrix for different film stack.

Procedure:

Fifteen, n-type, 100mm wafers of <100> orientation had initial stress measured using the Tencor P-2 profilometer tool. Also, the thickness of the wafers was measured using a micrometer. The wafers were RCA cleaned before dry oxide was grown in Bruce furnace tube 4 at RIT. The wafers were divided into three groups according to oxide

thicknesses: 1000 Å, 1500 Å, and 2000 Å. Process parameters are available in the appendix A. The oxide thickness was measured using patter in figure 5.6

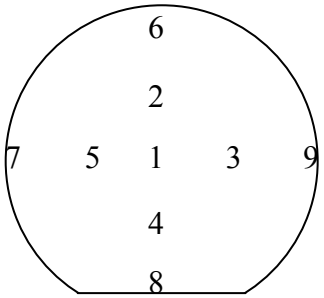

Figure 5.6: Pattern 3 layout for ellipsometry.

The oxide layer on the backside of the wafers was etched using the Drytek Quad (refer to appendix A oxide etch recipe). Stress measurements followed after oxide removal from the backside. The LPCVD system at RIT was not available during this experiment; wafers were sent to the Cornell Nanofabrication facility for stoichiometric silicon nitride deposition (see appendix A for deposition recipe). Following nitride deposition, the monitor wafers were measured to determine the film thickness and the index of refraction of the film. Before measuring stress, the nitride film was removed from the backside of the wafers using the Lam 490 (refer to appendix A nitride etch recipe). Stress was measured on all the wafers. The wafers were then RCA cleaned and LTO-oxide films were deposited in the LPCVD tool, followed by repeating the same procedure for obtaining thickness, index of refraction, and stress measurements.

Results:

All measurements are documented in Tables 5.2 and 5.3. Multiple measurements were performed, and the average value is reported for dry oxide group, as shown in Table 5.2. Thickness and index of refraction for nitride and LTO films were measured from monitor wafers. Table 5.3 presents the stress data. The film stress was measured on the

multi-layer device wafers as well as on the monitor wafers. Eq. 5.3 was used to determine full-range-uniformities (FRU) for all film thicknesses and etch rates.

$$Full - Range - Uniformity = \frac{M_{\max} - M_{\min}}{M_{\max} + M_{\min}} * 100 \qquad \textbf{(5.3)}$$

	Dry Oxide			Nitride			LTO		
Wafers ID	Thick (A)	FRU	Index	Thick (A)	FRU	Index	Thick (A)	FRU	Index
1-2	1008	2.88%	1.46	348	± 2%	2.03	944	31 %	1.55
8-10	1554	2.19%	1.46	372	± 2%	2.03	1109	37 %	1.48
5-7	1769	1.70%	1.46	374	± 2.7%	2.03	X	X	X

Table 5.2: Summary of the thicknesses of oxide, nitride and LTO films.

	Stress measured on multi- layer device wafers (MPa)			**Stress measured on monitor wafers (MPa)**	
Wafers	Oxide	Si_xN_y	LTO	M-S_xiN_y	M-LTO
1-2	-297	-1	-121	1191	-268
8-10	-276	-98	-147	N/A	N/A
5-7	-270	-121	N/A	N/A	N/A

Table 5.3: Summary of stress measurements, where oxides are compressive and silicon nitride is highly tensile. Oxide, Si_xN_y, LTO columns represent stress measured on the device wafers after deposition of each film. M-Si_xN_y and M-LTO columns show stress of Si_xN_y and LTO film which were deposited on the plane silicon wafer with the device wafers.

Discussion:

The tabulated results show that dry oxide and low temperature oxide are compressive, while the stoichiometric silicon nitride is highly tensile. Also, Table 5.3 shows an inversely proportional relationship of stress in the dry oxide to its thickness. In the case of the oxide-nitride film stack, the compressive stress increased with the initial oxide thickness, since the same silicon nitride film was deposited on all of the wafers. Another interesting observation gathered from the table is the difference between the monitor film stress and the film stress measured on the multi-layer film wafers. It shows that nitride on silicon is of higher tensile stress than nitride on silicon dioxide, and that oxide on nitride appears to be less stressed than oxide on silicon substrate. The trends

observed from this experiment indicate that either thinner silicon dioxide films (top & bottom) are needed to reduce the compressive stress, or a thicker silicon nitride film is needed to increase the tensile stress within the tri-layer film stack. Since a thinner film stack is not acceptable due to its fragile nature, a thicker silicon nitride film is applied in subsequent experiments.

C) Etching of Silicon

There are many possibilities for the removal of silicon, however a constraint on the proposed process is that it must not damage or remove the tri-layer, or alter its charge trapping and charge retention properties. One of more popular ways to etch silicon is by potassium hydroxide (KOH) solution; its popularity stems from low tooling cost. In addition, KOH solution etches preferentially along specific crystal planes, allowing a highly directional etch. The key shortcoming of this method is that it does not offer sufficiently high selectivity of etching silicon over oxide. Also possible diffusion of potassium, a mobile ion, into tri-layer dielectrics would prove to be devastating to the device. Therefore, the KOH process is not suitable for device release.

Reactive ion etch (RIE) is commonly used in the industry for removal of poly-silicon as well as other films. Plasma is required in this technique, since most of the gases used to etch thin films do not react spontaneously with those materials. Plasma assists the creation of reactive species; the species then diffuse down to the surface of the material where they are adsorbed and react with the material, forming a volatile product. Next, the reacted product leaves the material by desorption and diffusion. Figure 5.7 shows the complete reaction mechanism of RIE process.

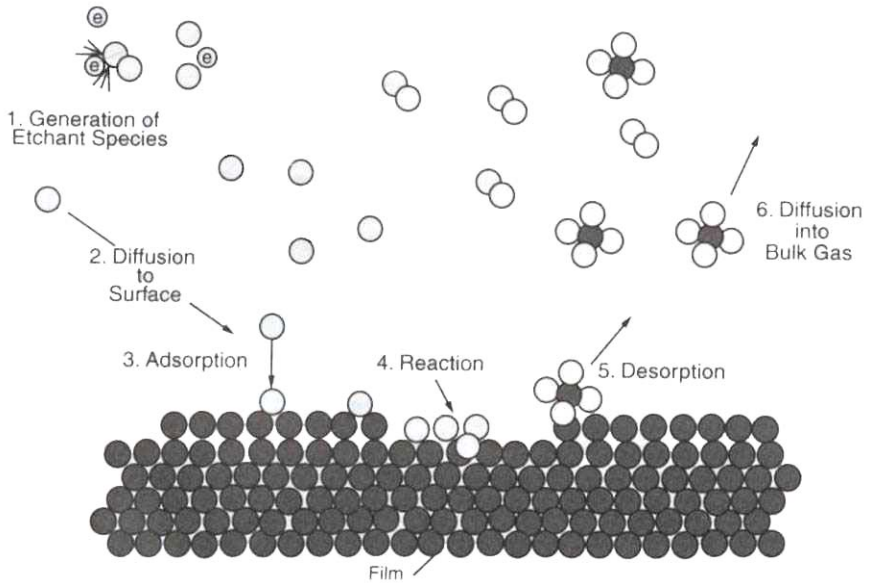

Figure 5.7: Complete reaction mechanism of RIE process [9].

Fluorine and chlorine based gases work effectively for Si etching. The drawback of using choloro-fluoro-carbon gases is the potential for polymer deposition, which hinders the etching. However, at a certain concentration of oxygen the polymerization is eliminated, and a high etch rate can be sustained, but at the cost of higher removal rate of the photoresist.

A more advanced technique for silicon removal is deep reactive ion etching (DRIE). This technique is specifically used for high-aspect-ratio dry etches and it utilizes an inductively coupled high density plasma source. The DRIE tool is designed to generate high density plasma without bombarding the substrate with highly energetic and potentially damaging ions. Also, the system operates in the molecular flow pressure regime, which reduces the number of ion collisions and effectively improves directionality of the ion flux. A popular process utilizing DRIE is the Bosch process, which involves repeated exposure of etchant plasma (SF_6) alternated with passivation plasma (C_4F_8) [5]; consequently the etch is very directional. During the passivation step, a polymer is deposited which protects the silicon sidewalls during the etch step. To

improve directionality of the etch step, a bias is applied to the substrate. The drawback of this process is the scalloping predominately observed at the top of trenches [5].

XeF_2 is another dry etch process that offers high selectivity with respect to oxide, nitride, Al, and hard baked photoresist films [10]. It is isotropic in nature, and requires no plasma, since even at room temperature the XeF_2 readily reacts with Si according to the following reaction: $2XeF_2 + Si \rightarrow 2Xe + SiF_4$. The drawbacks of the XeF_2 etch process are related to surface roughness of etched silicon and formation of HF if water is presents. Hydrofluoric acid etches oxide and can reduce the extremely high selectivity between silicon and the oxide layer.

Three different etch techniques are investigated in the following section: RIE, DRIE, and XeF_2 etch. Selectivity and uniformity results are presented, as they are of primary importance for the properties of the proposed structure.

Procedure:

Three, n-type 100mm wafers of <100> orientation were used. The wafers were RCA cleaned before LTO was deposited in 6" LPCVD system for 16 min. The oxide thickness was measured using the Nanometrics® Nanospec; the average thickness was 1386Å with FRU of 28% (see Eq. 5.3). Next, the wafers were coated with 1μm of Shipley photoresist (program 1 on SVG track). The wafers were then exposed using the Karl Suss MA-150 with an exposure dose of $43mJ/cm^2$. Figure 5.8 shows the design of the backside mask. Half of the mask was covered with a non-transparent film, so the removal rate of the oxide layer could be accurately monitored in the experiment.

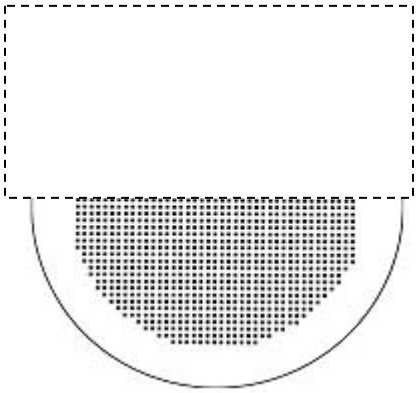

Figure 5.8: Mask design used for RIE, DRIE, XeF_2 etch characterization.

The wafers were then developed using SVG program 1. After patterning the photoresist, a 3 min buffered HF dip was performed, followed with a rinse, spin, and dry, which left bare silicon on the backside and patterned oxide on the front of the wafers. The resist layer was then removed using an oxygen plasma in the Branson 3200 asher. A new coat of AZ 9260 masking photoresist followed on the front side of the wafers using a standard masking recipe. There was approximately 25μm of misalignment in the y-direction between the patterned oxide and the masking resist pattern, which allowed monitoring of the selectivity of oxide and silicon. The total open area in the mask was 1394mm^2; approximately 230mm^2 of that was bare silicon and 1164mm^2 was the oxide.

After patterning and curing of the masking resist one of the wafers were sent to Xactix® for a XeF_2 isotropic etch; the wafers were measured upon return. The second wafer was etched at RIT using the STS MESC Multiplex ICP tool [5]; the wafer was etched for 25 cycles. The third wafer was also etched at RIT using the Lam 490 following SMFL polysilicon recipe (3min, SF_6 plasma) using a 6-inch wafer adapter to accommodate 4-inch wafers. The details for all recipes are included in the appendix A.

To measure the selectivity between oxide and silicon the masking resist was stripped off in the Branson 3200 asher, followed by an acetone soak to remove any remaining resist, then a DI water spin-rinse and dry. The oxide thickness was measured using the Nanospec™. In the case of the etched silicon, the step height was measured using the Tencor® P-2 profilometer.

Results:

Figures 5.9 and 5.10 show the quality of XeF_2 and DRIE etch. XeF_2 etch is isotropic in nature and in Figure 5.9 a small arrow indicates a sidewall etch. Both techniques show rough etched surface at the bottom of the etch window.

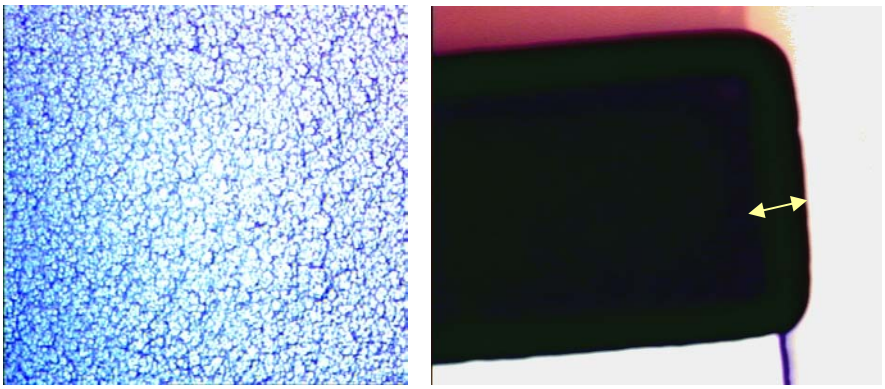

Figure 5.9: Wafer etched using XeF_2 at Xactix where the arrow indicates the sidewall etch. Image taken with 10x objective.

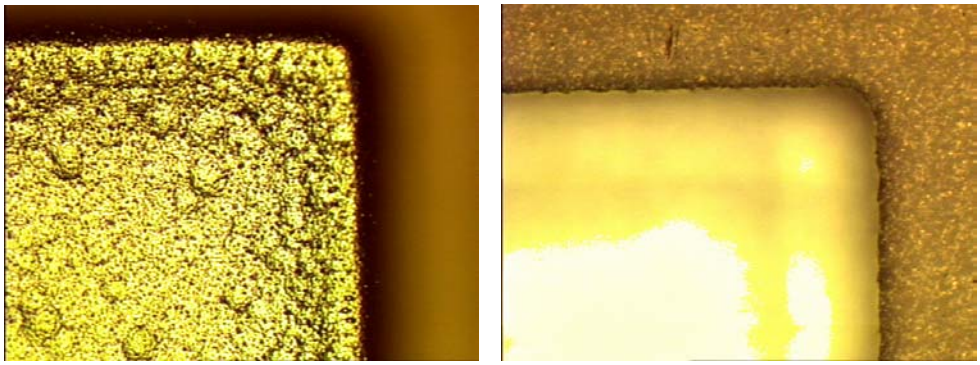

Figure 5.10: Wafer etched on STS DRIE system at RIT. Image taken with 20x objective.

Figure 5.11 presents the information on the location and the amount of the oxide removed during XeF_2, DRIE and RIE etch obtained by subtracting the final thickness from the initial measurement of the oxide film in units of Å.

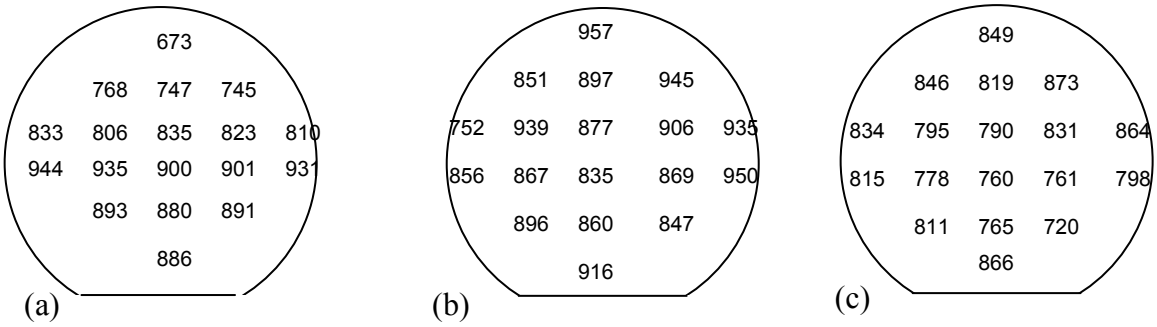

Figure 5.11: Amount of oxide removed in angstroms for (a)XeF2 etch, (b) DRI E process, and (c) RIE process

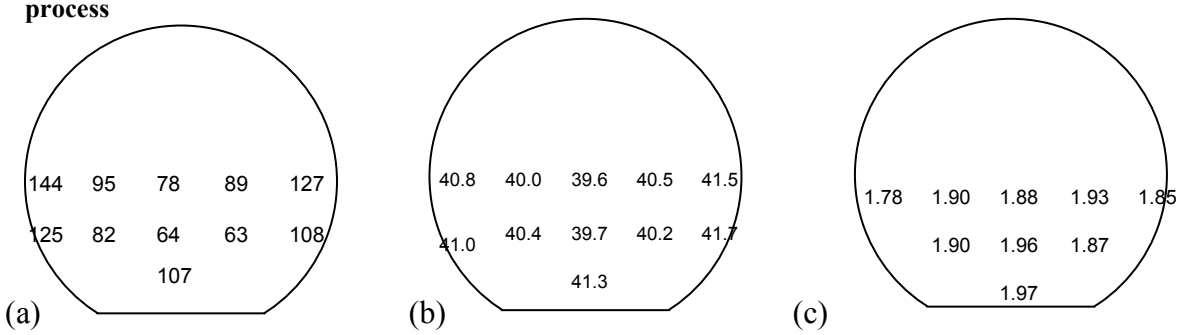

Figure 5.12: Amount of silicon removed (um) for (a)XeF2 etch, (b) DRIE porcess, and (c) RIE process

Figure 5.12 shows how much silicon was removed in units of microns. In case of XeF_2, the etch rate FRU is 40%. For silicon, the edge of the wafer is etched faster than the center. In the STS system, the FRU of etch rate is 2.6%. The FUR of RIE process is 5%, with a higher etch rate observed near the edge of the wafer.

	Xactix system		STS		Lam 490	
	Silicon	LTO	Silicon	LTO	Silicon	LTO
Avg. Removed (um)	98.38	0.0844	40.60	0.0883	1.892	0.0810
Full Range Uniformity	40%	17%	2.6%	12%	5%	7%
Etch Rate (um/min)	1.968	0.0017	7.495	0.0164	0.631	0.027
Selectivity of Si to LTO	1165:1		458:1		23:1	

Table 5.4: Summary of Results for different silicon etch systems.

The values for uniformity, selectivity, and etch rates are summarized in Table 5.4 for Lam 490, STS system, and XeF_2 etch. Note that the resist selectivity was not included due to insufficient sampling.

Discussion:

The above experiment demonstrated that XeF_2 offers the highest selectivity out of the three techniques that were investigated. However, a fairly high non-uniformity and slow etch rate of the XeF_2 etch might not be suitable for the silicon release. The STS system offers higher etch rate and better uniformity, but selectivity with respect to the oxide is much lower compared to the XeF_2 etch.

In the current experiment the total silicon area exposed to the various etching processes was 230mm^2. The total wafer area with devices would be 1394mm^2, thus loading effects may need to be considered. Loading effects result from the depletion of etching gas at the surface of the etched film, consequently lowering the etch rate and affecting the uniformity of the process. Some of the factors that can influence this include: total surface area exposed to the etching gas, recombination of the etching gas, and the gas-pumping rate. In summary, both XeF_2 and DRIE techniques appear to be suitable for removal of the remaining silicon.

D) Deep Reactive Ion Etch

Part of the process development involved investigation of two DRIE systems; one located at Eastman Kodak Company at the MEMS research facility in Rochester NY, and one located at RIT. Two wafers were used for this study; one of the wafers had ONO stack of ~500Å/500Å/500Å, and the second wafer was bare silicon. Both wafers had a

photoresist masking layer applied. The ONO wafer underwent a partial etch in the RIT STS system, followed by additional etching in the Kodak system. The bare silicon wafer (for process development) was patterned and etched using only the Kodak system.

An initial examination indicated a dome-like structure in the partially etched regions, approaching the ONO stack. Figure 5.13 shows the top view of the partially etched region. The center of the dome was about 18-30μm higher than the edge within each etched square. Both wafers were then mounted on the 6-inch carriers and etched at Kodak. The etching process was iterative, where the etch was interrupted and wafers were examined frequently throughout the process.

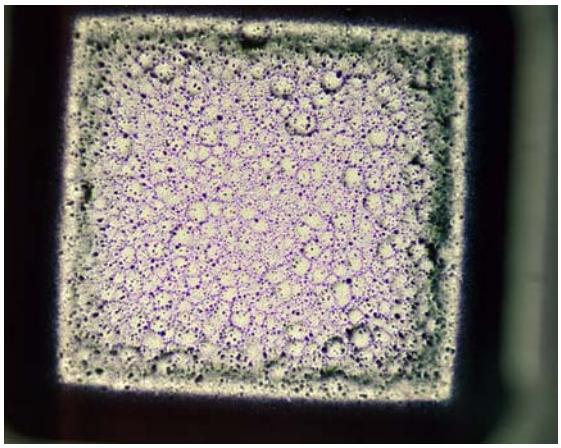

Figure 5.13: Pre-existing dome shape of an etch window created by the RIT etch process.

Results:

The bare silicon wafer was cross-sectioned through an etch window and photographed for analysis as shown in Figure 5.14. At the bottom of the etched region, features resembling a grassy surface are visible. In addition, a thin layer of about 1000Å of polymer was measured. There are also blotch-like defects close to the top of the etch window. An enlarged image of these defects is shown in Figure 5.15. The dark region is the polymer and the rough region is the etched silicon on the sidewall.

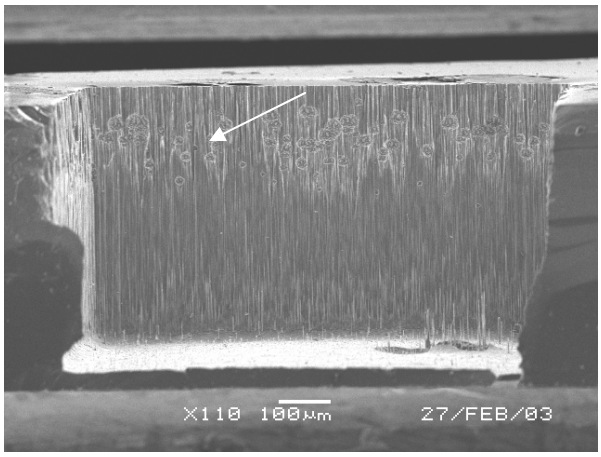

Figure 5.14: Cross sectioned etch window after DRIE.

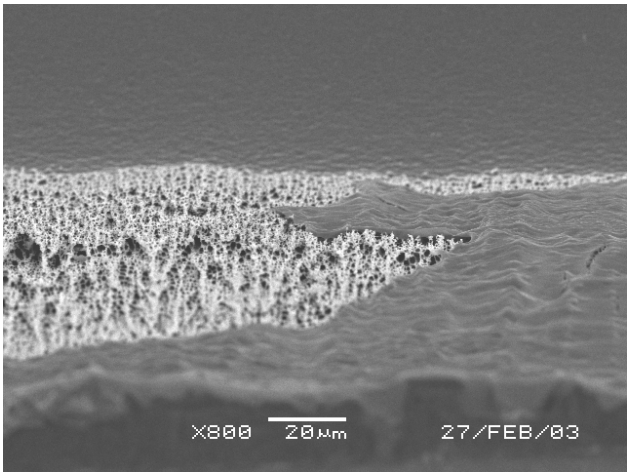

Figure 5.15: Magnified view of the marked region from Figure 5.14.

As the etch window deepens the deposition and etch mechanisms change [11]. In the beginning of the process the aspect ratio is small and the etch appears more isotropic, creating rough sidewalls. As the etch progresses, the ratio of depth to width increases, and the ion bombardment of the sidewalls diminishes. As a result, there is a polymer buildup either on top creating a bottleneck, or in the bottom of the etch window in the form of grass-like structures. Adjusting the process for different aspect ratios can eliminate these surface features [11].

Next, the partially etched silicon wafer was etched further toward the frontside ONO film stack. Figure 5.16 illustrates the etch pattern of the ONO wafer. It is apparent that the initial dome shape can be eliminated by adjusting the etch process. This is a very important observation for preventing the overetching of the tri-layer film. No grass features were present during this run, but unfortunately a radial non-uniformity was not eliminated as shown in Figure 5.16.

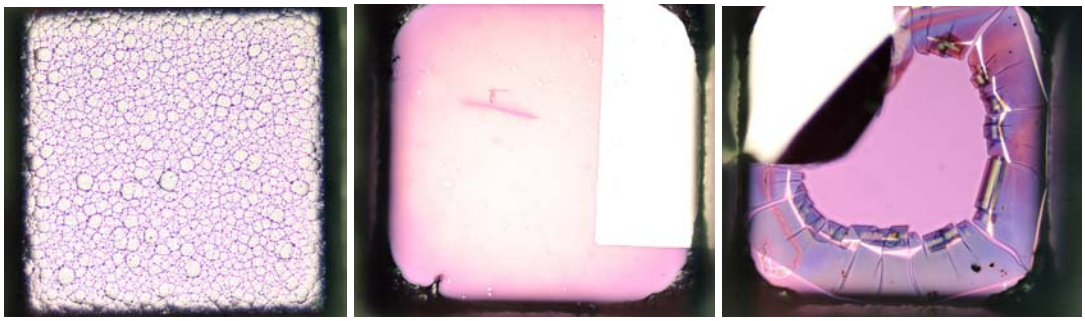

Figure 5.16: ONO stack after DRIE etched at Eastman Kodak. Image taken (a) at the center of the wafer, (b) midway, and (c) at the edge of the wafer.

E) The Effect of Etching on Charge Retention

The purpose of this experiment was to determine feasibility of charging up a device before release of the tri-layer membranes. Such capability would simplify processing by eliminating some of the fabrication steps. Unfortunately, due to limited use of the DRIE system, only RIE and XeF_2 etches were investigated.

Procedure and results for RIE experiment:

N-type wafer had tri-layer films deposited with the 6" LPCVD system, using a standard SMFL LTO recipe and SMFL stoichiometric nitride recipe. This wafer had the tri-layer striped from the back side using DryTeck for etching LTO films and Lam 490 for etching silicon nitride film. Wafer's tri-layer thicknesses were LTO 520Å, stoichiometric silicon nitride 508Å, and the second layer LTO 450Å. Next, aluminum

evaporation and pattering created ONO capacitors. Details regarding the processing of the ONO capacitors are provided in section 3.4. The capacitors were charged and an initial C-V curve was obtained. The wafer was then processed in Lam 490 using poly-silicon recipe for successive time periods of 2.5min, 3min, and another 3min. The poly-silicon recipe is provided in appendix A.

After each etch, C-V measurements were taken. Figure 5.177 shows a summary of the C-V measurements. The charge loss observed in Figure 5.177 after first 2.5 min was 12% and 17% after 5.5 min. Any further measurements were not possible due to degradation of the aluminum gates during the plasma etch. However, from the available data the lifetime constant was approximated to be 35 min, which means that after 35 min 63% of the embedded charge would be lost and only 22μm of silicon would be etched away. Using the same recipe a dummy wafer with thermal strips attached to it was processed for duration of 1 min, 3 min, and 4 min to measure the temperature of the wafer. After one minute the temperature was 53ºC, and after 3 min the temperature stabilized at 83ºC.

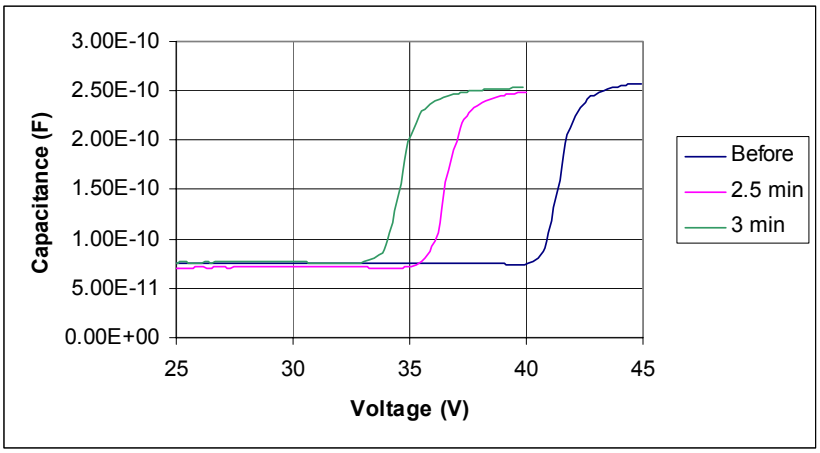

Figure 5.17: Charge retention during silicon etch in Lam 490 system.

Procedure and Results for XeF_2 Experiment:

An N-type wafer was used for this experiment. The first dielectric layer was soaked for 100 min. The nitride layer was deposited in a 4-inch LPCVD for 17 min. The third dielectric layer was deposited using a standard SMFL LTO recipe in a 6-inch LPCVD for 10 min. Thicknesses of the ONO tri-layers were 1039Å for dry oxide, 560Å for stoichiometric silicon nitride, and 480Å for LTO. Refer to appendix A for recipe details. Wafer had the tri-layer stripped from the backside using DryTek for etching LTO films and Lam 490 for etching the silicon nitride film. The wafer backside was coated with masking layer and partially etched using DRIE for 300 cycles (refer to appendix A for recipe). The backside was ashed for 10 sec in Lam 490 to remove any polymer that might have formed on the bottom of the vias during DRIE, which might prevent XeF_2 etch. Next, an aluminum film was evaporated and patterned on the front side of the wafer using the inverse pattern of the one used to pattern the masking layer. Blanket aluminum was evaporated on the backside of the wafer. Acetone was used to remove photoresist from the front of the wafer. Next, the capacitors were charged followed by a removal of all the metal using a wet etch process. The wafer was dried using compressed air and then sent to Xactix to be etched by XeF_2. The wafer was etched using the recipe summarized in Table 5.5.

Process parameters	
Cycle	30 sec XeF_2etch, 7 sec pump down
Pressure	800 mtorr
Temperature	35 C
Time	440 min

Table 5.5: Parameters used for XeF_2 etch at Xactix of a partially etched wafer.

After 160min, the first membrane was cleared and it did not rupture. The etching was resumed in an attempt to clear most of the membranes, and then the wafer was sent back to RIT. Unfortunately, only a very thin silicon grid remained of the wafer. The measured selectivity for this run was 250:1 oxide to silicon. The low selectivity during the XeF_2 etch was attributed to the presence of water, which resulted from the rinse after the aluminum etch combined with insufficient drying. The resulting removal of substrate material could have been caused by the etching of the polymer passivation layer, using an oxygen ash, prior to the XeF_2 etch. The removal of the passivation layer from the sidewalls would effectively increase the etch surface area and decrease the etch rate. Also, a significant amount of silicon remaining after DRIE would interfere with the isotropic etch. The lesson learned from these experiments is that charging before releasing the tri-layer membrane may not be an effective technique. Consequently, charging of the released tri-layer was considered in the subsequent experiments.

5.2.3 Fabrication and Release of a Charged Membrane

The following section will describe fabrication and testing of the final device. The fabrication process was design based on the knowledge gained from the above process experiments as well as from the high field charge injection experiments.

Procedure:

A lightly doped n-type wafer was scribed, profiled (Tencor P-2) and RCA cleaned before dry oxide was grown. The nitride layer deposition followed using the 4-inch LPCVD for 17 min. The third dielectric layer was deposited using a standard SMFL LTO recipe in a 6-inch LPCVD for 10 min. The measured thicknesses of the tri-layer films were oxide 1024Å, nitride 570Å, and LTO 1017Å. Each time a film was deposited the backside of the wafer was stripped and film stress was measured. This was done using an oxide recipe on Drytek Quad 482 RIE system, SMFL nitride 4-inch recipe on 490 Lam for 30sec and Tencor P-2 profilometer.

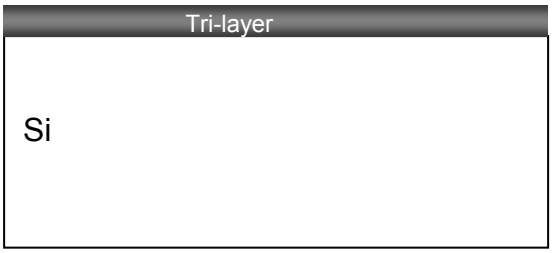

Figure 5.18: Silicon wafer after tri-layer deposition and etch of the backside.

The wafer was then coated and patterned with AZ926 masking resist, followed with a deep substrate etch using the STS DRIE system for 300 cycles. An optical microscope was used to approximately determine the etch depth. At the center of the wafer etch depth measured as 350 μm and about 420 μm near the edge. The initial wafer thickness was ~550um.

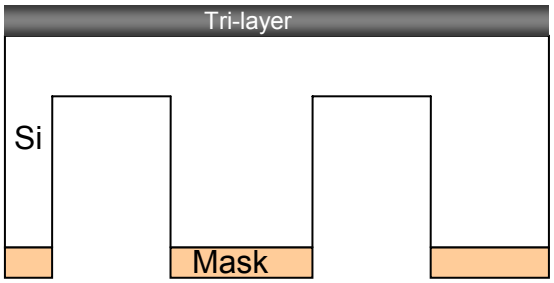

Figure 5.19: Partial etch of the silicon substrate using DRIE.

Aluminum was evaporated using the CHA evaporator. Photoresist was applied using a manual spinner. The wafer was then baked in Hereaus oven to reduce the solvent content of the resist at a temperature of 80ºC for 5 min. Next, the wafer was exposed on Karl Suss contact aligner and developed by hand. At this point, the wafer was wet etched to transfer pattern to the Al layer. Next, DRIE was performed using the Kodak system; the recipe details are provided in appendix A. The wafer was monitored throughout the etch process, and the etch was terminated after the first few membranes were released.

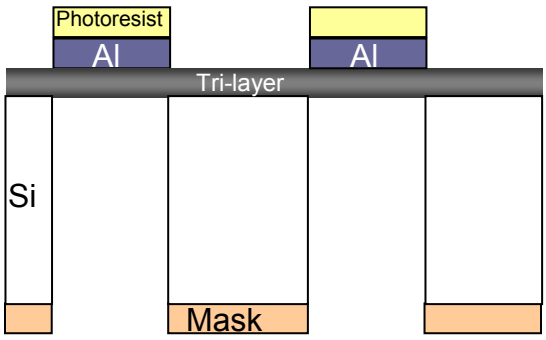

Figure 5.20: Fully etch substrate with metal gate.

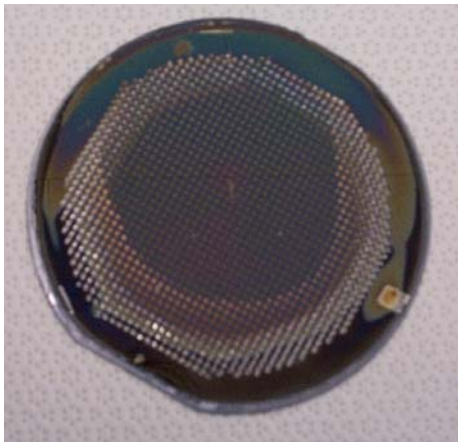

Figure 5.21: Image of the actual wafer with released membranes.

Figure 5.21 shows the wafer after the removal of silicon. Only devices at the edge of the wafer were released, and none of them ruptured. The wafer had the resist stripped in an acetone bath, and then a blanket of aluminum was evaporated onto the backside. With the patterned Al on the front and blanket Al on the back the wafer was cleaved into smaller subsections in preparation for high field charge injection.

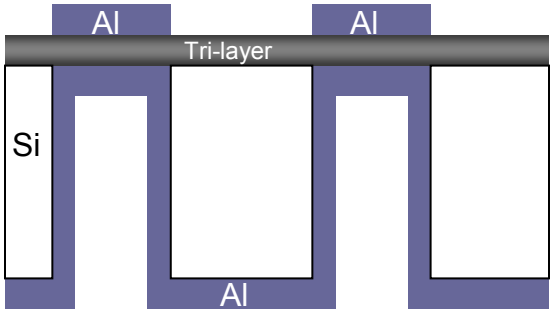

Figure 5.22: Cross section view of the released membrane ready for charge injection.

A rectified AC signal with amplitude of 100V to 180V was used to charge the devices. To avoid damage to the membranes the probe tip was lowered on the part of aluminum pad supported by the silicon substrate. A detailed map of the sample was produced to keep a record of charge injection parameters. Aluminum was then removed by dipping

the pieces into a wet etch bath for 20min, followed with a rinse in DI water and drying with compressed air. This did not remove all water, and the pieces were left to air dry overnight prior to testing.

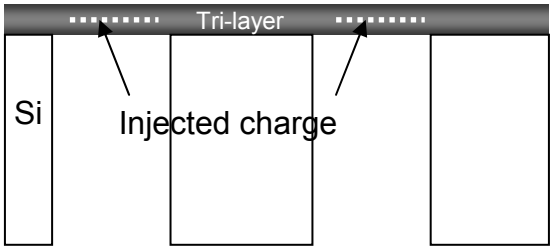

Figure 5.23: Charged and free standing membranes.

The testing of the charged device is based on a simple electrostatic principle, which states that charges within an electric field will be attracted toward the electrode of opposite polarity, as illustrated in Figure 5.24.

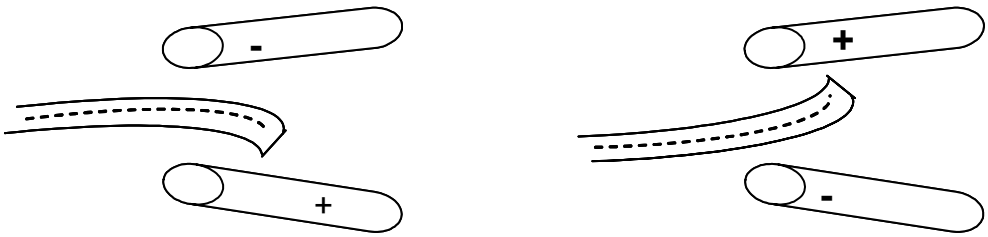

Figure 5.24: Test set up for the final examination of the charged in a freestanding tri-layer film stack.

The first attempt was to actuate the complete membrane structure, but its large size made it difficult to test. By breaking the membrane, the remaining suspended pieces were much easier to test according to the method illustrated in Figure 5.24. They were place between two probes, where one of the probes was grounded while the second one had a positive or negative DC bias applied.

Results and Discussion:

Summary of the stress measurements of the device wafer are provided in Table 5.6. All measurements were taken on the device wafer after each film deposition. The total stress of this structure was found to be 57MPa compared to the tri-layer film stack (1008Å/348Å/944Å), which measured -121MPa. The reduction in total stress within the structure is attributed to the thicker nitride film.

	Thickness (Å)	Stress (MPa)
Si-Oxide	1024	-370
Si_xN_y	570	+91
Si-LTO	1017	**+57**

Table 5.6: Summary of stress measurements of the final device.

During the charge injection step some of the membranes ruptured. The ruptures were result of catastrophic breakdowns, which only took place in the areas where the patterned aluminum was present on top of released membranes as shown in Figure 5.25. Catastrophic breakdown occurred around 160V, where a capacitor of similar film stack (SiO_2 1039Å, Si_3N_4 560Å SiO_2 480Å) ruptured at 200V. The premature breakdown of the released devices might be caused by over etching of the tri-layer film stack during silicon substrate etch. C-V measurements demonstrated that the membranes were successfully charged. Although measurements were not taken directly on the freestanding membranes, measurements were taken on adjacent regions where aluminum overlapped the unreleased tri-layer. Before & after C-V curves indicated a voltage shift of 5V.

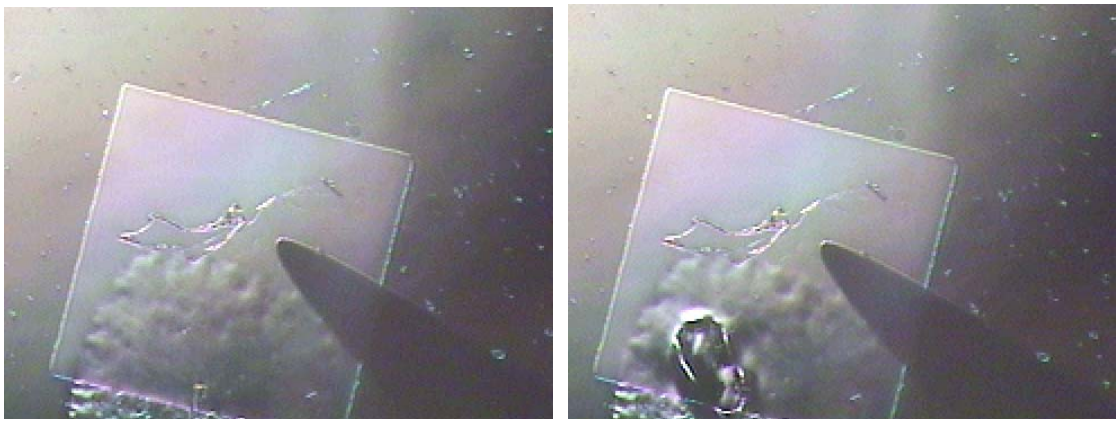

Figure 5.25: Catastrophic breakdown of the released tri-layer of the ONO stack at ~180V (a) before charging (b) after charge injection.

The pictures in Figure 5.26 were extracted from a movie recording of the device testing. The test consisted of applying a potential difference between the two probes. The horizontal distance between the two probes was approximately 50μm. The applied potential ranged from 0V to 180V. At 180V a movement was recorded. The membrane subsection moved towards the positively charge probe suggesting the presence of trapped electrons. Due to the restoring spring force, it returned to its original position when the potential was reduced to 0V. Next, a negative potential was applied. Unfortunately, at about -180V the spring moved towards the probe with a negative polarity. The test was repeated for an uncharged film and other charged devices at different voltages, and they all behaved in the same manner.

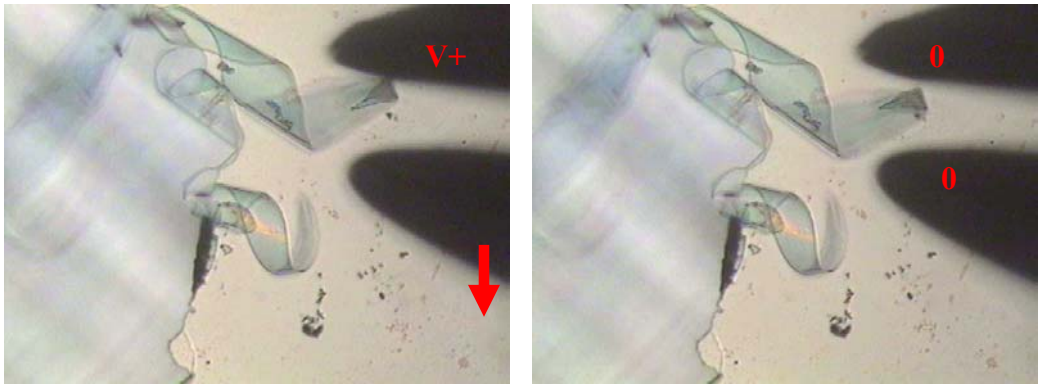

Figure 5.26: (a) Subsection of a membrane placed within the electric field moved towards positive bias, (b) With electric field off it retract to its original position.

5.3 Summary

The final testing of the device did not support the presence of charge within the released ONO stack. Various factors could have contributed to such an outcome. It is possible that the injected charge was neutralized due presence of water [12], or the high field charge injection was not as effective in injecting charge into the membrane. Detailed reasons are discussed further in Chapter 6.

References

1. W. H. Hsieh, T. Y. Hsu, and Y. C. Tai, "A Micromachined Thin-film Teflon Electret Microphone," Technical Digest, 1997 International Conference on Solid-State Sensors and Actuators (Transducers '97), Chicago, IL, Vol. 1, pp. 425-428, Jun. 16-19 (1997).

2. Voorthuyzen, J.A.; Olthuis, W.; Bergveld, P.; Sprenkels, A.J., "Research and development of miniaturized electrets" Dielectrics and Electrical Insulation, IEEE Transactions, Volume: 24 , Issue: 2 , April 1989 pg255 – 266

3. Schwodiauer Reinhard, Neugschwandtner, Gerhard S., Bauer-Gogonea Simona, Bauer Siegfried, Rosenmayer Tom. "Dielectric and electret properties of nanoemulsion spin-on polytetrafluoroethylene films", Applied Physics Letters (2000), 76(18), pg 2612-2614

4. J.A. Voorthuyzen, P. Bergveld and A.J. Sprenkels, "Semiconductor Based Electret Sensors for Sound and Pressure", IEEE Transaction and Electrical Insulations Vol. 24 No 2 April 1989 pg 267-276

5. Web page by Stanford Nanofabrication Facility, last modified 03/22/2004 http://snf.stanford.edu/Equipment/stsetch/stsfaqs.html

6. Milton Ohring, "The Materials Science of Thin Films" Academic Press, 1992 pg. 419

7. Kuo Shen Chen, Xin Zhang, Shih Yuan Lin, " Intrinsic stress generation and relaxation of plasma-enhanced chemical vapor deposition oxide during deposition and subsequent thermal cycling" Thin Solid Films 434 (2003),pg 190-202

8. S. Wolf and R.N. Tauber "Silicon Processing for the VLSI Era " Volume I. Second edition Lattice Press, 2000, pg 296

9. Marc J. Madou, "Fundamentals of Microfabrication: The science of Miniaturization " CRC Press, New York, 2002, pg94

10. Marc J. Madou, "Fundamental of Microfabrication: The science of miniaturization", CRC Press, New York,2002, pg107-108

11. Martin J. Walker, "Comparison of Bosch and cryogenic processes for patterning high aspect ratio features in silicon", Oxford Instruments, 2001

12. E.H. Nicollian and C.N. Berglund "Electrochemical charging of thermal SiO2 films by injected electron currents" Journal of Applied Physics, Vol 42 Numb 13, 1971 pg 5654-5663

CHAPTER SIX: CONCLUSION

6.1 Summary

The ultimate goal of embedded charge RF microswitch research is to produce actuators that are of low cost and are able to operate in the range of 3-5 volts. The most important component of the described RF microswitch design is the embedded charge cantilever. This investigation focused on a freestanding electret for this application. The research was divided into three phases. Phase one dealt with studying of charge injection and possibility of long term retention of the injected charge within multilayer dielectrics (refer to Chapter 3 for details). Phase two looked into the physics of the device (refer to Chapter 4 for details). Phase three focused on the fabrication and charging of a freestanding thin-film membrane (refer to Chapter 5.2.3).

Electrical analysis of the oxide-nitride-oxide (ONO) film stack capacitors was performed, and the following observations were noted. Experiments showed successful charge trapping within the thicker ONO film stack. The highest voltage shift of 45.5V was achieved with film stack on the order of 500 Å each. A film stack on the order of 1000Å/ 500Å/ 500Å LTO produced a 33V shift. Presence of mobile charge and fixed charge were measured, and the effective density was an order of magnitude lower than the estimated charge injected using a high electric field. In addition, the room-temperature lifetime of the trapped charge was estimated to be 18,000 hours, with charge leakage characterized by a thermal activation energy of 0.6eV. Details of this investigation are provided in Chapter 3.

Theoretical analyses of the embedded charge microswitch offered deeper understanding of the device. A simplified one-dimensional model was used to study the relationships between actuation voltage, sheet charge density, and cantilever displacement. The analysis did show the possibility of building a low actuation voltage device with appropriate sheet charge density. Refer to Chapter 4 for details.

The fabrication process was successful in creating a free-standing membrane. Deep reactive ion etch (DRIE) was the most effective process for removing silicon, and 10μm of AZ 9260 photoresist proved to be a sufficient masking layer for DRIE. The 1000Å / 500Å / 500Å stack showed a high degree of mechanical strength, and no released diaphragms broke during further processing and handling. Also, a substantial force was required to rupture the ONO stack for testing. Unfortunately, the final testing of the device did not conclusively support the presence of charge within the released ONO stack. Refer to Chapter 5 for details.

Various factors could have contributed to such an outcome. One possible factor could have been related to charge injection. Once a device is released, high electric field charge injection is performed. Since the membrane was released, the charging occurred through a metal layer, tri-layer, and another metal layer. All previous work related to charge injection was done on a silicon substrate, where C-V characterization allowed for monitoring of the density of charge trapped within a capacitor. With the silicon substrate removed, there was no accurate way to determine the presence of charge within ONO film stack. Therefore, one can only speculate the amount of charge injected into the device.

Another possible explanation is related to water presence within the film stack. After the charge injection, the metal is removed using a wet etch followed by rinsing in deionized water. Compressed air could not remove all water and the sample was left to air dry. It is possible that water could have diffused through the released aluminum-free surface and discharged the device [1].

6.2 Suggestions for Future Experiments

One of the future experiments could focus on further improvement in quality of the silicon oxide and silicon nitride films. It's been shown that, the number of trap sites within the oxide film could be reduced. Experiments involving high temperature anneals in presence of various ambient gases suggest that such improvements are possible for silicon oxide films [2-3]. Also, deposition at higher temperatures or post-deposition annealing could improve quality of the silicon nitride films by reducing the number of hydrogen bonds [4-5].

Another experiment could focus on charge retention during release of the tri-layer film stack. The study would investigate the effects of long-term exposure of a charged device to a plasma etch with or without annealing prior to the etch. In experiments which have been done to similar devices, a charged device which was annealed showed no charge loss even at an elevated temperature [6]. The study would include experiments to determine how DRIE system affects charge retention. Also, XeF_2 etch would be revisited in this study to see if one could reduce presents of water by using doped polysilicon instead of aluminum. To further limit device exposure to water, a chemical surface treatment such as an HMDS vapor prime could be investigated [7].

Additional measurements to quantify the total charge and space charge distribution are required to properly characterize the ONO device. Many methods exist to obtain these measurements, and were discussed in Chapter 2. Also, in Chapter 2 various techniques for creating electret films were mentioned. In this work, only the high field charge injection method was investigated. However, corona charging might also be an effective technique worth investigating further [10].

6.3 Concluding Remarks

The research presented here focused on developing a charged thin-film membrane comprised of an oxide/nitride/oxide (ONO) tri-layer dielectric stack. The fabricated membrane represents the cantilever within a microswitch, and it contains injected charge, which aids in controlling the deflection with an externally applied voltage. In this work all three phases of the described research were completed and the initial results look promising. However, further work is required to successfully merge charge injection technology with the structure release process to fabricate a fully functional microswitch.

A multi-layer insulator structure with trapped charge may be a viable approach for making microswitches and could also be used in other applications that benefit from a lower actuation voltage. Hopefully, the lessons learned in this investigation will provide insight for future research.

Reference

1. E.H. Nicollian and C.N. Berglund "Electrochemical charging of thermal SiO2 films by injected electron currents" Journal of Applied Physics, Vol 42 Numb 13, 1971 pg 5654-5663

2. N. M. Ravindra, Dariush Fathy and J. Narayan J. K. Srivastava and E. A. Irene, "Two-step oxidation processes in silicon" Materials Letters, Vol 4, Issue 8-9 , 1986, pg 337-342

3. R.P. Sivoththaman, S. De Schepper, P. Laureys, W. Nijs, J.F. Mertens, "Improving low-temperature APCVD SiO_2 passivation by rapid thermal annealing for Si devices" Electron Device Letters, IEEE, Vol 19 , Issue: 12, 1998,pg 505 - 507

4. H.J.Stein, "Hydrogen-implanted silicon nitride" Journal of the Electrochemical Society Vol 129, Number 08 August 1982 pg 1782-1791

5. V. J. Kapoor, R.S. Bailey, H.J. Stein, "Hydrogen-related memory traps in thin silicon nitride films", Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films 1, pg 600-603 (1983)

6. Houman Amjadi and Gerhard M. Sessler, "Inorganic electret layer for miniaturized devices" Electrical Insulation and Dielectric Phenomena, Annual Report., Conference on , 22-25 Oct. 1995 Pages:668 - 671

7. H. Amjadi "Electret membranes and backelectrodes for application in micromechanical transducers", Journal of Electrostatics, vol. 48 ,2000, pg 179-191

8. Bozena Hilczer and Jerzy Malecki, "Studies in Electrical and Electronic Engineering 14: Electrets" Elsevier, New York, 1986,pg 214-224

9. G. M. Sessler "Electrets" Volume 33 Physics Principles, Springer-Verlag Berlin Heidelderg, Germany 1987. pg 39

10. H.Amjadi and G.M. Sessler, "Charge Storage in APCVD Silicon Nitride", IEEE Annual Report, Conference on Electrical Insulation and Dielectric Phenomena, 1997 pg 64-67

Appendix A: Processing Recipes

Process	**Etch of Nitride Film**
Tool	**Lam 490 RIE**
RF Power	130 W
Pressure	375 mtorr
SF_6 Flow	70 sccm
He Flow	5 sccm
Gap	1 cm

Process	**Etch of Oxide Film**
Tool	**Drytek 482 RIE**
RF Power	300 W
Pressure	70 mtorr
CHF_3 Flow	70 sccm
O_2 Flow	5 sccm

Process	**Etch of Poly-Si Film**
Tool	**Lam 490 RIE**
RF Power	140 W
Pressure	325 mtorr
SF6 Flow	150 sccm
O2 Flow	45 sccm
Gap	1.25 cm

Process	**XeF_2 Etch of Silicon at Xactix**	
	Etch Step	Pump Step
Gas	XeF_2	0
Pressure	800 mTorr	800 mTorr
Time	30 sec	7 sec

Process	**Etch of Silicon Substrate**	
Tool	**Kodak STS**	
	Deposition Step	Etch Step
Flow	C_4F_8 85 sccm	SF_6 130 sccm
Coil Power	600 W	600 W
Platen Power	0 W	12 W
Pressure	18-20mTorr	29-32mTorr
Etch Time	8 sec	12 sec

Process	**Etch of Silicon Substrate**	
Tool	**RIT STS MESC Multiplex ICP**	
	Deposition Step	Etch Step
Flow	C_4F_8 85sccm	SF_6 130 sccm
Coil Power	600 W	600 W
Platen Power	0 W	15 W
Pressure	5mTorr	5mTorr
Etch Time	7 sec	13 sec

Process	**Deposition of LTO**		
Tool	**6 inch LPCVD**		
Temperature	Zone 1	Zone 2	Zone 3
	405 ºC	425 ºC	425 ºC
Gas Flow	O_2	96 sccm	
	SiH_4	80 sccm	
Pressure	300 mtorr		

Process	**Deposition of Nitride**		
Tool	**6 inch LPCVD**		
Temperature	Zone 1	Zone 2	Zone 3
	800 ºC	800 ºC	800 ºC
Gas Flow	SiH_2Cl_2	4 sccm	
	NH_3	50 sccm	
Pressure	300 mtorr		

Process	**Deposition of Nitride**		
Tool	**4 inch LPCVD**		
Temperature	Zone 1	Zone 2	Zone 3
	790ºC	800 ºC	810 ºC
Gas Flow	SiH_2Cl_2	50 sccm	
	NH_3	500 sccm	
Pressure	300 mtorr		

Process	**Deposition of Dry Oxide**			
Tool	**Bruce Furnace 4**			
512	SMFL 1000Å dry Ox		Temp.	Gas Flow
STEP	description	time	(ºC)	(lpm)
0	Bout out	0	25	5 N_2
1	Start	:00:01	800	10 N_2
2	Push In	:12	800	10 N_2
3	Stabilize	:20	800	10 N_2
4	Ramp Up	:20	1000	5 O_2
5	Stabilize	:05	1000	5 O_2
6	Soak	2:25	1000	10 O_2
7	N_2 Purge	:05	25	15 N_2
8	Ramp Down	:35	25	10 N_2
	Total time	4:17		

Process	**Deposition of Dry Oxide**			
Tool	**Bruce Furnace 4**			
508	SMFL 500Å dry Ox		Temp.	Gas Flow
STEP	description	time	(ºC)	(lpm)
0	Bout out	0	25	5 N_2
1	Start	:00:01	800	10 N_2
2	Push In	:12	800	10 N_2
3	Stabilize	:20	800	10 N_2
4	Ramp Up	:20	1000	5 O_2
5	Stabilize	:05	1000	5 O_2
6	Soak	:45	1000	10 O_2
7	N_2 Purge	:05	25	15 N_2
8	Ramp Down	:35	25	10 N_2
	Total time	2:34		

Process	**Masking Layer for DRIE**
Steps	
1	Prime the wafer using SVG recipe 1
2	Dispense a quarter size puddle of AZ 9260
3	Spin the wafer at 500 RPM 5 sec and 1500 RPM 45 sec
4	Bake the wafer at 90ºC for 2 min on hotplate
5	Expose the wafer on Suss MA 150 Aligner: 90 sec which is about 1500mJ/cm2 using soft contact
6	Develop wafer with CD 26 developer for 4 min
7	Bake the wafer on the top plate of the Hereaus oven for 30 min at 125ºC

Appendix B: Tool Specifications

Keithley C-V characterization station

High Frequency Capacitance 100kHz			
Range	**Resolution**	**Accuracy**	**Noise**
200 pF	10 fF	0.7+0.05	180 fF
2 nF	100fF	0.9+0.5	1800fF
High Frequency Capacitance 1MHz			
200 pF	10 fF	0.9+0.05	200 fF
2 nF	100fF	1.4+0.5	400 fF
Quasistatic capacitance			
200 pF	10 fF	1+0.1	0.12%rdg +0.13pF 100mV/StepV +0.1pF
2nf	100 fF	0.8+0.2	0.09%rdg +0.13pF 100mV/StepV +0.1pF
Voltage source			
voltage	**p-p noise**	**resolution**	
≤ 20V	150 μV	10mV	
>20V to 120V	250 μV	100mV	
Maximum sweep span $\|V_{START}-V_{STOP}\|$:40V			
Maximum output current: ±2mA			
Sweep Step Voltage Selections: 10mV,20mV,50mV,100mV			
DC output Resistance: <10Ω			

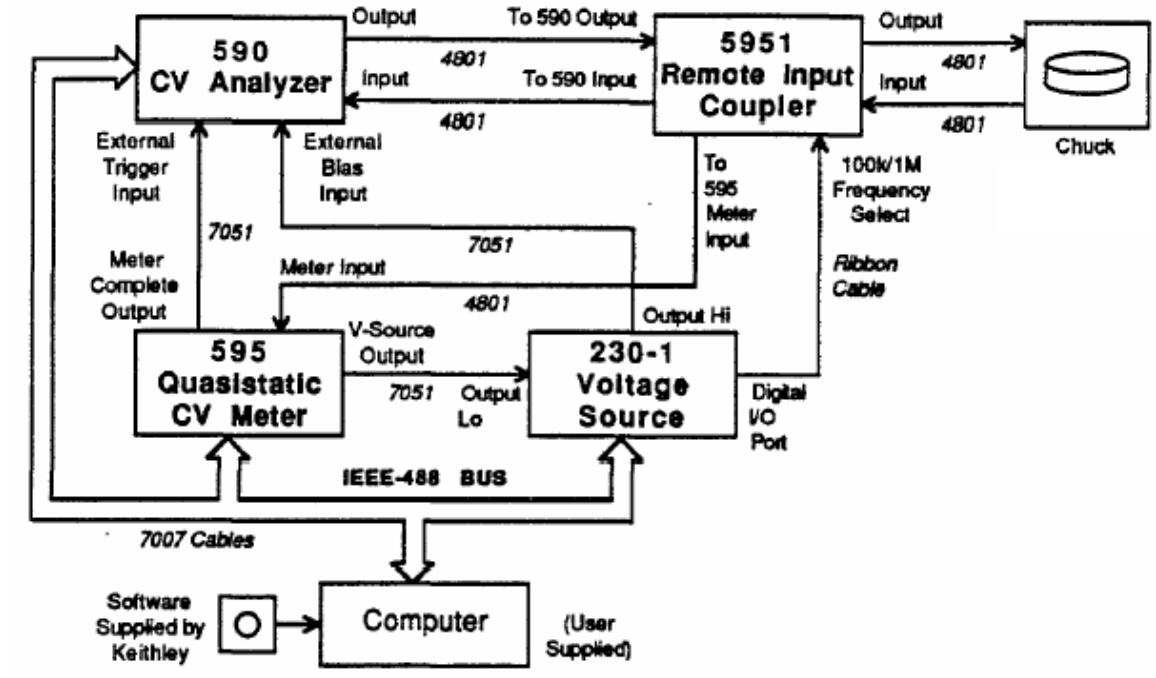

Figure 1 Block diagram of CV setup

Semiconductor Parameter Analyzer Model HP 4145B

Maximum capacitive load: 1000 pF

SMU Voltage Range, Resolution and Accuracy

Voltage Range	Resolution	Accuracy[1,2]	Max. Current
±20V	1mV	±(0.1%+10mV+0.4×Io)	100mA
±40V	2mV	±(0.1%+20mV+0.4×Io)	50mA
±100V	5mV	±(0.1%+50mV+0.4×Io)	20mA

*I_{O-V} is SMU output current in amps.

SMU Current Range, Resolution and Accuracy

Current Range	Resolution	Accuracy[1,2]	Max. Voltage
±100mA	100μA	±(0.3%+100μA+2μA×Vo)	20V(>50mA) 40V(>20mA)
±10mA	10μA	±(0.3%+10μA+200nA×Vo)	100V(≤20mA)
±1000μA	1μA	±(0.3%+1μA+20nA×Vo)	
±100μA	100nA	±(0.3%+100nA+2nA×Vo)	
±10μA	10nA	±(0.3%+10nA+200pA×Vo)	
±1000nA	1nA	±(0.5%+1nA+20pA×Vo)	
±100nA	100pA	±(0.5%+100pA+2pA×Vo)	
±10nA	10pA	±(1%+15pA+200fA×Vo)	
±1000pA	1pA	±(1%+6pA+20fA×Vo)	

*V_{O-V} is SMU output voltage in volts.
**50 fA resolution in current monitor mode.

1. Accuracy specifications are given as ±% of reading or setting value ±% of range.
2. Accuracy tolerances are specified at 25°C ±5°C, after a 40 minute warm-up time, with AUTO CAL on, and specified at the rear panel connector terminals referenced to SMU common. Tolerances are doubled for the extended temperature range of 10°C to 40°C.

SMU Voltage/Current Compliance

Maximum voltage compliance: 20 V, 40 V, or 100 V, depending on the output current range.

Maximum current compliance: 20 mA, 50 mA, or 100 mA, depending on the output voltage range.

Compliance setting resolution: same as current and voltage output/measurement resolution. Maximum current compliance resolution, however, is 50 pA.

Compliance accuracy: voltage compliance accuracy is the same as voltage output/measurement accuracy. Current compliance accuracy is current output/measurement accuracy ± (1% of range + 10 pA).

Tektronix 370 programmable curve tracer

Range	**16 V**	**80 V**	**400 V**	**2000 V**
Max Peak Current	10 A	2 A	0.4 A	0.05 A
Peak Current Pulsed	20 A	4 A	0.8 A	0.1 A
Min. Series Res.(Ω)	0.26	6.4	160	20 K
Max.Series Res.(Ω)	800	20 K	500 K	12.5 M
Collector/Emitter Current				
Measurement range is 100 nA/div (1 nA resolution) to 2 A/div for collector current and 100 pA/div (1pA resolution) to 2 mA for emitter current.				
Collector/Base/Emitter Voltage				
Measurement range is 5 mV/div (50μV resolution) to 500 V/div for the collator and 5mV/div (50μV resolution) to 2V/div for base emitter voltage.				

Appendix C: Approximate contact potential of materials to intrinsic silicon

Material	ϕ_J
Ag	−0.4
Au	−0.3
Cu	0.0
Ni	+0.15
Al	+0.6
Mg	+1.35
Degenerate p^+ polysilicon	−0.56
Degenerate n^+ polysilicon	+0.56
Extrinsic Si	$-\phi_F$
Intrinsic Si	0

†The values given for metals and polycrystalline silicon are only approximate. Accurate values are difficult to obtain, and, in fact, different measuring techniques can yield values which differ by a large fraction of 1 V.