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Development and Characterization of High Performance Transistors on Glass

By

Robert L. Saxer Jr.

A Thesis Submitted

in Partial Fulfillment

of the Requirements for the Degree of

Master of Science

in

Microelectronic Engineering

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COLLEGE OF ENGINEERING

ROCHESTER INSTITUTE OF TECHNOLOGY

ROCHESTER, NEW YORK

SEPTEMBER 2005

Development and Characterization of High Performance Transistors on Glass

By

Robert L. Saxer Jr.

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Robert L. Saxer	September 29th, 2005

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ABSTRACT

Currently, the electrical drivers behind active-matrix flat-panel displays are polysilicon or amorphous silicon based thin-film transistors (TFTs). The ability to integrate transistors onto the glass substrate offers certain design and performance advantages over package-level integration with bulk silicon ICs; this is commonly referred to as system-on-glass (SOG) or system-on-panel (SOP). System on glass may also lower the manufacturing costs of the entire product. Cell phones, personal digital assistants, and entertainment systems are examples of applications that would benefit from system on glass integration.

This project is a joint effort between the Microelectronic Engineering Department at RIT and Corning Incorporated. Thin-film transistors have been fabricated on a new substrate material which consists of a high-quality silicon layer on Corning's Eagle 2000 flat-panel display glass. The substrate material has the potential of yielding transistors with higher performance than commercialized polysilicon and amorphous silicon thin film transistor technologies. The primary focus of this investigation was to solve the engineering challenges of dopant activation, deposited dielectric quality and interface charge associated with a low-temperature (LT) process. A process that is compatible with the thermal constraints of the glass has been designed and demonstrated through the fabrication of MOS transistor. While the device characteristics demonstrate the on-state and off-state behavior of standard bulk-silicon devices, there are unique features which required an extensive study to understand and explain the governing physics. Device simulation was used to develop a comprehensive model of operation for the devices.

TABLE OF CONTENTS

Title Page i
Library Release ii
Acknowledgment iii
Abstract v
Table of Contents vi
List of Figures........ viii
List of Tables xv
1. Introduction 1
   1.1. Motivation 1
   1.2. Partnership with Corning 2
   1.3. Process and Device Engineering 3
   1.4. Initial Demonstration of CMOS 4
   1.5. Summary and Outline of Thesis 6
2. Thin Film Transistor Technology 7
   2.1. Introduction 7
   2.2. TFT Technology 8
      2.2.1. Polysilicon Grain Boundary Theory 10
   2.3. SOI Technology 16
   2.4. Device Considerations 18
3. Low-temperature Process Development 19
   3.1. Introduction 19
   3.2. Silicon Mesa Isolation 21
   3.3. Oxide Study 22
   3.4. Molybdenum Gate Process 25
   3.5. Implant / Anneal Study for Low Temperature Dopant Activation 27
      3.5.1. Implant Activation Experiment........ 28
   3.6. Constraints of Silicon on Glass 33
      3.6.1. Dimensional Stability 33
      3.6.2. Contamination 34
      3.6.3. Wafer Handling Requirements for SiOG 35
      3.6.4. Low Thermal Conductivity of Glass 35
      3.6.5. Preparation for Process Challenges 35
   3.7. Concluding Remarks 36
4. TFT Process Integration and Device Simulation 37
   4.1. Introduction 37
   4.2. Test Chip Layout 38
   4.3. Starting Substrate Preparation 40
   4.4. Process Design & Fabrication Flow 41
   4.5. TFT Device Design 63
      4.5.1. Charge Analysis Simulation 64
      4.5.2. Analysis of Initial Design Space with Simulation 68
      4.5.3. Final Design Refinement with Simulation 71
   4.6. Concluding Remarks 75

5. TFT Device Characterization and Modeling …..…….………………………….. 76
5.1. Introduction …………………………..………………………………… 76
5.2. First Demonstration of Transistors on Glass …….……….…………….. 77
5.3. TFT Parameter Extraction …..…….………………………………….... 81
5.3.1. On-State Characterization …..……….……………………………. 81
5.3.2. Off-State Characterization …………..……….…………………… 83
5.4. Process Run #2: L1B Thin-Film Transistors ……..……………………... 83
5.4.1. NMOS TFT Characteristics ……………………..……….……….. 84
5.4.2. PMOS TFT Characteristics …………………………..……….….. 90
5.5. Process Run #3: L2A Thin-Film Transistors …..……….……………….. 92
5.5.1. L2A NMOS TFT Characteristics ……………..…….……………. 93
5.5.2. L2A PMOS TFT Characteristics …………………..…….……….. 99
5.5.3. L1B & L2A Device Summary …..…………………………….….. 106
5.6. CMOS Inverter DC Characteristics …………..……….………………… 109
5.6.1. CMOS Inverter Frequency Response ………..…….…………….... 111
6. Summary of Research ……………………………………..…….………… 113
6.1. Process Development ……………………………………………..……... 114
6.2. SiOG TFT Process Integration …..…….………………………………… 115
6.3. TFT Characterization …………………..……….………………………... 116
6.4. Feedback from Corning ……………………..……….…………………... 119
6.5.Concluding Remarks …………………………………..…….…………... 120
Bibliography…………………………………………………………..…….….…….. 121
APPENDIX

LIST OF FIGURES

1.1 Typical L = 24μm W = 4μm transistor from initial process. 4

1.2 LT-CMOS Voltage Transfer Characteristic . 5

2.1 Typical TFT configurations for display applications. (a) Etch stopper configuration. (b) Etch back configuration. The pixel ITO represents area reserved for the display device. 9

2.2 Grain boundary energy band diagram. 12

2.3 Schematic representation of (a) partially depleted and (b) fully depleted SOI transistors. 16

3.1 Illustration of the theoretical SiOG device. Unit processes that required development and characterization are highlighted. 20

3.3 Silicon etch profile. 22

3.3 Oxide charge vs. oxide type and anneal treatment. With a 450°C H_2N_2 sinter or 600°C 1hr anneal, the TEOS oxide results look similar. The average charge levels observed for TEOS oxide were 9.8E11cm^{-2} with a sample standard deviation of 2.5E11 cm^{-2} (35 samples). TEOS samples that received no anneal or sinter did not measure on the SCA. LTO samples had low enough charge levels to be measured, averaging 8.9E11cm^{-2} with no sinter or anneal and a standard deviation of 7.5E10cm^{-2} (108 samples). A two hour oxygen anneal of LTO at 600°C provided the lowest charge levels averaging 5.9E11cm^{-2}, with the tightest distribution having a standard deviation of 7.5E10cm^{-2}. 23

3.4 Typical LTO high-frequency (100kHz) CV characteristics from a p-type, 3E15 silicon wafer with an oxide thickness of 450?. Traces C1 and C2 are measured results, and Series1 and Series2 show theoretical low-frequency and high-frequency characteristics, respectively. The capacitance increase in inversion is due to the lack of field isolation. The mask defined capacitor size was 200kμm^2. The sample had a calculated fixed charge level of -4E10cm^{-2}, and negligible acceptor-like or donor-like interface trap charges. The flatband voltage was measured to be -0.44V, with a positive threshold voltage of 0.56V. 24

3.5 Ion ranges and collision events for 170Kev argon ions into 1000? screen oxide and crystalline silicon. 29

3.3 Ion ranges and collision events for 75Kev fluorine ions into 1000? screen oxide and crystalline silicon. 29

3.7 Boron implant and anneal experimental results for source and drain dopant activation. 31

3.8 Phosphorous implant and anneal experimental results for source and drain dopant activation. 31

4.1 6x6 µm device with a SOI style body contact. Note the body contact and gate polygons are arranged to maximize overlay tolerance. 38

4.2 Test chip layout for TFT development. Process characterization structures include Van-Der-Pauw, cross bridge Kelvin resistors, capacitors, diodes, and a large width inverter for cross section. Transistors of varying length and width are included for parameter extraction. 39

4.3 Starting silicon "Well" profile after implant and drive-in. A specific and uniform doping profile was desired before sending silicon to Corning for their proprietary SiOG process. 40

4.4 Starting SiOG substrate after silicon bonding, done by Corning, Inc. 42

4.5 Protective LPCVD LTO deposition 42

4.6 Backside molybdenum deposition 42

4.7 PECVD TEOS Backside protective oxide deposition 44

4.8 Photoresist coat 44

4.9 First level lithography, mesa isolation/active definition 44

4.10 HF oxide removal 46

4.11 Mesa isolation etch 46

4.12 Photoresist strip 46

4.13 Protective oxide strip 48

4.14 Gate oxide deposition 48

4.15	Gate metal deposition	48
4.16	Photoresist coat	50
4.17	Gate photo patterning	50
4.18	Molybdenum etch	50
4.19	Photoresist strip	52
4.20	Protective oxide deposition	52
4.21	Photoresist coat	52
4.22	N+ source and drain lithography	54
4.23	N+ source and drain implant	54
4.24	Photoresist strip	52
4.25	Photoresist coat	56
4.26	P+ source and drain lithography	56
4.27	P+ source and drain implant	56
4.28	Resist strip and clean	58
4.29	Inter-layer dielectric oxide deposition	58
4.30	Photoresist coat	58
4.31	Contact cut lithography	60
4.32	Contact cut etch	60
4.33	Resist strip	60
4.34	Aluminum metal deposition	61
4.35	Resist coat	61
4.36	Metal 1 photolithography	62
4.37	Aluminum etch	62

4.38 Final structure 63

4.39 ID-VG sweep of initial NMOS simulation. Regions A, B, and C provide insight into how a large amount of backside charge could influence device behavior. 65

4.40 (a) Simulated structure at $V_G = -2.0$ volts, $V_{DS} = 0.1$ volts. (b) Hole and electron concentration plot from point 1 to point 2. 66

4.41 (a) Simulated structure at $V_G = -1.0$ volts, $V_{DS} = 0.1$ volts. (b) Hole and electron concentration plot from point 1 to point 2 67

4.42 (a) Simulated structure at $V_G = 2.0$ V, $V_{DS} = 0.1$ V. (b) Hole and electron concentration plot from point 1 to point 2. 68

4.43 BCC analysis for NMOS simulation without a body contact. The plot displays leakage current and threshold voltage as a function of silicon thickness (Xsi in μm), gate oxide thickness (Xox in μm), substrate doping (Nsub in cm^{-3}), silicon/gate oxide interface charge (Qtop in cm^2), and silicon/glass interface charge (Qbot in cm^2). 69

4.44 BCC analysis for NMOS simulation with a channel contact (body contact) directly below the channel region. Plot displays leakage current and threshold voltage as a function of silicon thickness (Xsi in μm), gate oxide thickness (Xox in μm), substrate doping (Nsub in cm^{-3}), silicon/gate oxide interface charge (Qtop in cm^2), and silicon/glass interface charge (Qbot in cm^2). 70

4.45 Simulated NMOS characteristics without a body contact. Silicon thickness has a large effect on device characteristics 72

4.46 Simulated NMOS device cross section that displays electron and hole concentration at a gate bias of -2, 0, and 3 volts. The silicon thickness is 1500. Note that at -2 volts there is no channel formed, and the device is 'off' 72

4.47 Simulated PMOS characteristics without a body contact. 74

4.48 A Simulated PMOS cross section showing electron and hole concentrations at three different gate bias (-3V, 0V, 2V). With 1E11 cm^{-2} backside charge and 800? of silicon allow this pseudo PFET to function as a transistor and not a resistor. 74

5.1 Family-of-Curves characteristics for typical NMOS (a) and PMOS (b) TFTs fabricated in L1A, with a silicon layer thickness X_{Si} ~ 300nm. The channel dimensions were L = 24µm & W = 6µm for the NMOS device and L = 24µm & W = 12µm for the PMOS device. Note that the NMOS device tested utilized a grounded body contact to suppress floating-body effects. Gate bias conditions are indicated, showing that the NMOS TFT is enhancement mode and the PMOS TFT is depletion mode. Also note that the V_{GS} = 10V condition on the PFET resulted in dielectric failure. 78

5.2 L1A bulk-Si control wafer (C2) NMOS device, L = 24µm & W = 24µm The threshold voltage V_{Tn} ~ 1.5V. 80

5.3 Example of linear mode mobility calculation using an I_{DS}-V_{GS} sweep of the transistor (a). The mobility of this bulk silicon device was found to be 683 cm^2/V-sec (b). An example of a 'two-stage' V_T is shown in figure (c), with the associated transconductance shown in (d). 82

5.4 Example of typical SiOG NMOS subthreshold characteristic. 83

5.5 Characteristics of a L1B, L = 6µm W = 24µm, thick-X_{Si} (300nm) NFET TFT for a (a) ID-VD sweep where the threshold voltage appears to be around ~2V and (b) ID-VG sweep where the full turn-on is not realized until ~11V. 84

5.6 I_{DS}-V_{GS} Characteristics of a L1B, L = 24µm & W = 24µm Thick-X_{Si} (300nm) NMOS TFT clearly showing the 2-stage turn-on characteristic, as well as hysteresis in the *stage-1* portion comparing forward and reverse sweeps. Note that this is a DC sweep (HP4145 Parameter Analyzer, long integration mode), thus the traps are exhibiting a slow time response. The *stage-1* V_T is ~ 1V, with a *stage-2* V_T ~ 6V. The channel mobility extracted from the *stage-2* transconductance, μ_n ~ 100 cm^2/V-sec. 86

5.7 Bulk-silicon LT NFET, L=4µm & W=24µm, I-V Characteristics: (a) Linear-mode I_{DS} vs. V_{GS} (b) Linear transconductance vs. V_{GS} (c) Log mode I_{DS} vs. V_{GS} (d) Family-of-curves. The extrapolated threshold voltage is ~ 1.1V, and the electron channel mobility μ_n ~ 620 cm^2/V-sec, extracted from the linear-mode transconductance. 87

5.8 I_{DS}-V_{GS} characteristics of a thin-X_{Si} (150nm) NMOS TFT, L=24µm & W=24µm, shown on a linear scale (a) and log scale (c) which emphasizes the 2-stage behavior. The second-stage threshold voltage is extrapolated to be ~ 5V, and the linear-mode transconductance (b) yields a channel mobility μ_n ~ 200 cm^2/V-sec. The log-scale plot shows reasonable *stage-1* sub-threshold slope, where SS ~ 400mV/dec. 89

5.9 Linear-scale characteristics of *thin-X_{Si}* (a - c) and *thick-X_{Si}* (d - f) PMOS TFTs. (a) The *thin-X_{Si}* device (X_{Si} ~ 150nm, L=24µm & W=24µm) exhibits an extrapolated V_T ~ -1V, and an extracted mobility μ_p ~ 100cm^2/V-sec. (d) The *thick-X_{Si}* device (X_{Si} ~ 300nm, L=4µm & W=24µm) exhibits an extrapolated V_T ~ -3.5V, and an extracted mobility μ_p ~ 65cm^2/V-sec. Although not obvious, the two-stage behavior is apparent in (e) as shown by the plateau in the transconductance (g_m). Two-stage PMOS TFT subthreshold characteristic is evident in (b) for the *thin-X_{si}* device. The log-scale plot shows a poor sub-threshold slope, where SS ~ 2V/dec. However, with a gate voltage of +5V the current was reduced to the noise floor of the HP4145 current measurement capability. 91

5.10 Linear I_{DS}-V_{GS} characteristics of L2A and L1B NFETs, showing measured characteristics with 2-stage behavior, and device models with top-side Qss adjusted to match the stage-2 response. 93

5.11 A linear scale magnified view of the I_{DS}-V_{GS} sweep in the low current range for L1B & L2A NFETs. 95

5.12 Linear regime I_{DS}-V_{GS} sweep on log scale for L1B & L2A. 96

5.13 Subthreshold comparison of L1B measured and modeled for a liner regime I_{DS}-V_{GS} sweep displayed on log scale. 97

5.14 Subthreshold comparison of L2A measured and modeled, linear regime I_{DS}-V_{GS} sweep displayed on log scale. Model parameters are given in the following discussion. 98

5.15 Linear regime I_{DS}-V_{GS} plot of L1B & L2A measured and modeled PFET characteristics, using a single value for top-side Qss. 99

5.16 Linear regime I_{DS}-V_{GS} plot of L1B & L2A measured and modeled PFET characteristics on a log scale plot. 101

5.17 Linear regime I_{DS}-V_{GS} plot of L1B & L2A measured PFET characteristics. 102

5.18 Linear regime I_{DS}-V_{GS} plot of L1B & L2A measured PFET 103

characteristics plotted on a log scale.

5.19 Linear regime I_{DS}-V_{GS} plot of L2A measured and modeled PFET characteristics. An extremely good fit at low current levels is obtained when bottom charge is taken into consideration. 104

5.20 Linear regime I_{DS}-V_{GS} plot of L2A measured and modeled PFET characteristics plotted on a log scale. Note the good fit obtained when bottom charge is taken into consideration. 105

5.21 A CMOS voltage transfer characteristic (VTC) for common length transistors of 4μm, and widths of 18μm and 45 μm for the NFET and PFET respectively. The VTC is for X_{Si} ~300nm. The calculated linear mode mobility for the NFET was μ_n ~ 148cm^2/V-sec and μ_p ~ 65cm^2/V-sec for the PFET. 109

5.22 CMOS Inverter 110

5.23 CMOS inverter frequency response (L=4μm Wp=45μm Wn=18μm). The input signal signal was a 6V p-p sinusoid, with a period of ~760μs, operating at a measured frequency of 1.3kHz. The circuit supply voltage was 8V (Vdd), and the output signal was measured at 7.8V peak to peak. 111

5.24 CMOS inverter characteristic at 13.1KHz. The input signal was a 14V peak to peak sinusoid. The circuit was operated with a 8V power supply and 7.4V peak to peak was measured at the output. 112

6.1 Illustration of the theoretical SiOG device. 115

6.2 6x6 μm device with a SOI style body contact. Note the body contact and gate polygons are arranged to maximize overlay tolerance. 116

6.3 A CMOS voltage transfer characteristic (VTC) for common length transistors of 4μm, and widths of 18μm and 45 μm for the NFET and PFET respectively. The VTC is for X_{Si} ~300nm. 117

6.4 CMOS inverter frequency response (L=4μm Wp=45μm Wn=18μm). The input signal signal was a 6V p-p sinusoid, with a period of ~760μs, operating at a measured frequency of 1.3kHz. The circuit supply voltage was 8V (Vdd), and the output signal was measured at 7.8V peak to peak. 118

LIST OF TABLES

Table	Description	Page
2.1	Approximate operating characteristics of amorphous and poly-silicon.	16
3.1	Etch conditions.	21
3.2	LPCVD LTO deposition conditions.	24
3.4	Stopping and range calculations for the studied ions into molybdenum using SRIM software. Worst case conditions were considered, 200Kev acceleration voltage, and 3800? was chosen, so consideration would not need to be given again to ion stopping by the gate metal.	25
3.5	(a) Molybdenum sputter deposition conditions. Deposition rate under these conditions was approximately 143?/min. (b) Reactive ion etch conditions used for molybdenum. The etch rate was approximately 2300? /min.	26
3.6	Initial implant and anneal experiments for source and drain dopant activation.	28
4.1	LPCVD LTO deposition conditions.	41
4.2	Piranha clean recipe.	47
4.3	Molybdenum deposition conditions.	47
4.4	Conditions representing potential 'worst-case' levels of backside charge for device simulation.	64
4.5	NMOS Simulation Conditions.	71
4.6	PMOS simulation conditions.	73
5.1	SiOG TFT input parameter level settings.	77
5.2	L1B and L2A *thin-X_{Si}* Device results	92

CHAPTER 1

INTRODUCTION

1.1. MOTIVATION

Low temperature CMOS is an active area of research for system integration applications. In recent years, society has demonstrated an enormous market for integrated microsystems, such as cell phones and flat panel displays. Currently, the electrical drivers behind the displays are polysilicon or amorphous silicon based thin-film transistors (TFTs). To support the trend to a more compact product size, designers are integrating classically bulk silicon based components onto the display with TFTs. This is commonly referred to as system-on-glass (SOG) or system-on-panel (SOP). SOP would lower the manufacturing costs of the entire product. Cell phones, personal digital assistants, and entertainment systems are examples of applications that would benefit from SOP integration. Advances in SOP technology would occur more rapidly if the performance (carrier mobility) of thin-film transistors were improved beyond that currently available in amorphous silicon or low-temperature polysilicon technology. The goal of this study was to develop and characterize high performance transistors on glass; in this context "high performance" refers primarily to the electrical carrier mobility.

1.2. PARTNERSHIP WITH CORNING

Thin-film display is an area where research activities are rapidly advancing the technology. In addition to being a leader in the telecommunication industry, Corning Inc. leads the industry in providing high quality glass to flat panel display manufacturers. Corning had recently expressed an interest in evaluating the device quality of their proprietary silicon-on-glass (SiOG) substrate material. The process development and characterization work required for this project matched exceedingly well with the teaching and research interests of the Microelectronic Engineering Department at RIT. In addition, the Semiconductor and Microsystems Fabrication Laboratory (SMFL) at RIT offered the equipment set and process capabilities required to realize CMOS devices, which includes microlithography, ion-implantation, chemical vapor deposition (CVD), plasma etching, rapid-thermal annealing (RTA) and diffusion furnaces.

Corning's TFT substrates are expected to yield devices with superior characteristics than current generation polysilicon or amorphous devices. While specific details on the manufacture of Corning's proprietary substrate material are not public knowledge and will not be described in this thesis, it must be noted that the silicon layer is single-crystal and has the potential of demonstrating carrier mobility comparable to that of bulk silicon. Thus, the TFTs have the potential of demonstrating device performance comparable to those fabricated on silicon on insulator (SOI) substrates, making it the ideal platform for system on glass applications. The specific interest of Corning was to evaluate the device quality of their substrate material, and identify the improvements required in order to present this new substrate material as an option to potential customers in the flat-panel display industry.

1.3. PROCESS AND DEVICE ENGINEERING

There were several key challenges presented by using glass as a substrate. Although procedural, wafer handling of glass substrates had to be addressed as many of the tools use capacitance sensors, and/or optical edge sensors which do not function properly with a transparent glass substrate. In addition, the glass used in the Corning substrate contains Alkaline Earth Boro-Aluminosilicate [1]. Impurities that may leave the glass during processes such as thermal annealing or wet chemistry could contaminate other processes and have catastrophic effects; glass processing must be segregated from standard front-end MOS device fabrication.

In regards to thermal annealing, the devices must be processed within the strain point of the substrate which is 666°C [1], beyond which the glass experiences irreversible structural changes. Even if the strain point of the material is not exceeded, there can be dimensional changes during thermal process procedures. Dimensional changes due to thermal cycling of the substrate at temperatures approaching the strain point may introduce defects in the silicon material, as well as present processing issues such as wafer handling, lithography alignment and pattern registration.

The practical temperature constraint for thermal annealing is 600°C, with rapid-thermal processes up to 650°C. The RIT baseline CMOS process exceeds this constraint during 12 thermal process steps, thus completely new process techniques had to be developed. Processes that are affected the most by temperature constraints are ion-implanted dopant activation and formation/treatment of the gate dielectric. Several experiments were performed in order to develop processes for the source/drain formation and the gate dielectric that offered acceptable device characteristics, as verified on bulk silicon devices. This low thermal-budget (LT) process was then implemented for TFT fabrication (see fig. 1.1).

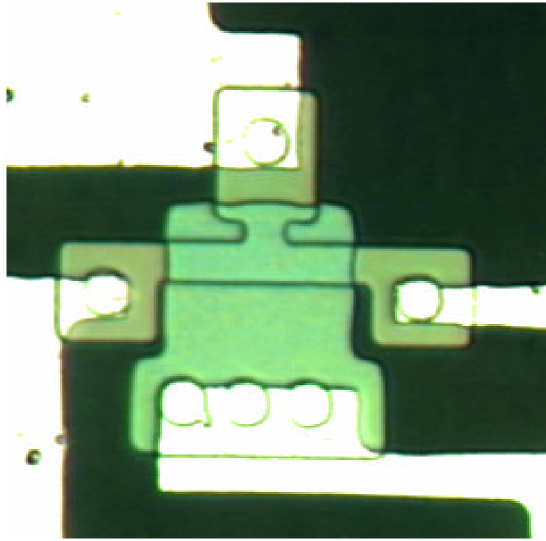


Figure 1.1: Typical L = 24µm W = 4µm transistor from initial process.

1.4. INITIAL DEMONSTRATION OF CMOS

Although process verification was performed on bulk silicon wafers, there was no guarantee that results would correlate with the thin-film SiOG devices. This presented another engineering challenge; the analysis of process results and device characteristics on the glass substrates was always confounded with the quality of the substrate preparation procedures that were done by Corning. Nevertheless, the first process run showed that the process was feasible; both working NMOS and PMOS devices were realized. A demonstration of functional CMOS inverters was accomplished on the second process run! Figure 1.2 shows the voltage-transfer characteristic (VTC) of an inverter fabricated using the LT-CMOS process. The Vin-Vout relationship has a textbook appearance; showing full-rail output and excellent gain (slope) at an inversion voltage of approximately $V_{DD}/2$.

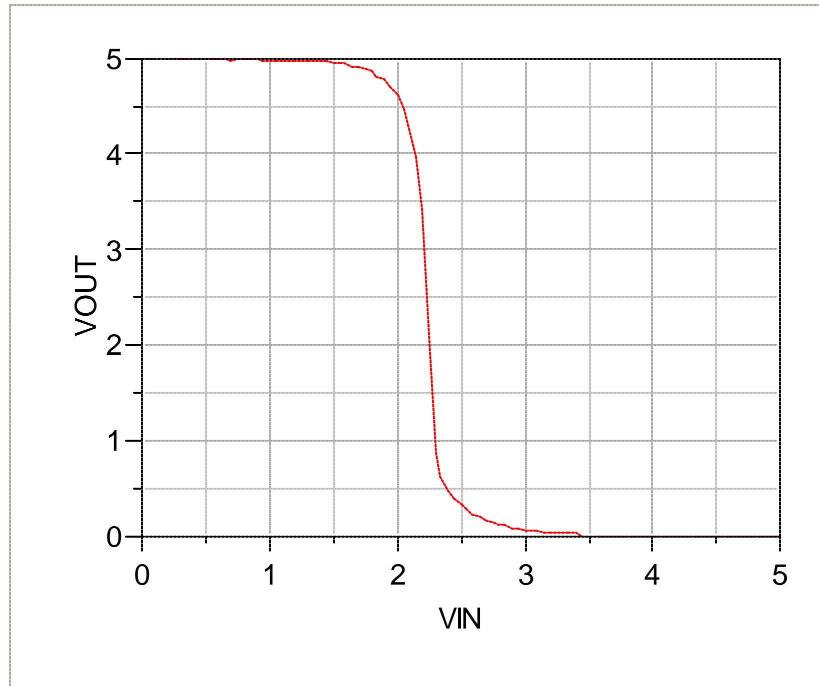


Figure 1.2: LT-CMOS Voltage Transfer Characteristic

The VTC matches the characteristic of a nearly balanced inverter with symmetric threshold voltages at +1V and -1V for the NMOS and PMOS transistors, respectively; this is actually not the case. While the VTC appears almost ideal, a closer inspection of the short-circuit current indicates an issue with the output-low condition. The PMOS transistor should be in an off-state with a high on the input; however, there is a fairly significant current flowing. The fact that this process run yielded a functioning inverter at all is actually quite remarkable. The SiOG layer was the same boron doping concentration for both the NMOS and PMOS transistors, and both resulted in enhancement-mode devices! With no differences in the gate material, and no threshold voltage adjustment implants, it was expected that the PMOS transistors would operate as a depletion-mode device. Another detail which is not obvious from the VTC is that the on-state threshold voltages of the transistors were approximately +/-6V; the entire VTC is actually within the subthreshold region of transistor operation! While this unexpected

demonstration of CMOS was encouraging, there were many questions surrounding the devices that needed to be answered, several of which have been addressed in this work.

1.5. Summary and Outline of Thesis

There were many challenges encountered in fabricating and understanding the behavior of NMOS and PMOS transistors on this substrate material still under development. A significant engineering effort has been invested in the successful realization of functional transistors. This has been the basis of this thesis, through which the understanding of the mechanisms of operation of these devices has begun.

This thesis is presented over the six remaining chapters. Chapter 2 provides background information on TFT technology, and motivation for the research. Chapter 3 provides information on the process development work for the LT-CMOS process; results of unit-process experiments are presented and analyzed. Chapter 4 discusses the details of process integration, with fabricated TFT device characteristics presented and analyzed in chapter 5. Chapter 6 presents a summary of the work, and reiterates the conclusions made following the investigations described throughout the process development and device characterization sections.

CHAPTER 2

THIN FILM TRANSISTOR TECHNOLOGY

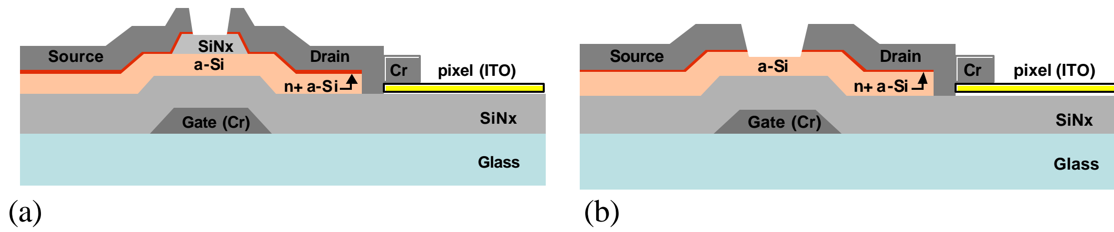
2.1. INTRODUCTION

Currently the flat screen display market is dominated by amorphous silicon TFTs. Recently display manufacturers have been pursuing technology that would enable higher levels of integration on the display backplanes, reducing off glass components (system on panel or SOP). Amorphous silicon technology cannot support the demands of complex logic circuitry; primarily due to low mobility. Devices fabricated on Corning substrates should demonstrate certain performance characteristics comparable to SOI devices; however, TFT fabrication restrictions must be imposed. The electron and hole channel mobilities are expected to be improved over polysilicon or amorphous silicon thin film transistors. For this reason devices fabricated on the Corning substrate have enormous potential for enabling SOP technology. This section will briefly review the state of the technology for TFT and SOI devices, and topics of specific interest to this investigation will be emphasized.

2.2. TFT TECHNOLOGY

Low-temperature polysilicon TFT technology has demonstrated a significant performance improvement over amorphous silicon, showing more than a ten-fold increase in carrier mobility. One of the most identifiable applications of polysilicon thin film transistors is in the flat panel display area. The requirement of large-area flat panel displays is addressed by using a thin-film polysilicon on glass as the substrate. The fabrication of working MOS devices in polysilicon on an inexpensive substrate was demonstrated by T.I. Kammins *et al*, in the early 1980s [2].

High-quality low-temperature polysilicon (LTPS) TFTs are usually prepared by amorphous-silicon (a-Si) deposition, followed by excimer laser pulsed annealing which melts the a-Si locally, minimizing heat transfer to the substrate. The annealing process is critical for uniform display characteristics. A low-hydrogen containing a-Si layer is required for adequate and consistent re-crystallization, which the deposition process must provide. Current low-temperature polysilicon (LTPS) processes offer high mobility and current drive TFTs for flat panel displays. However, it has been shown that transistor variation over the display area can translate into variation in pixel brightness [3]. The use of a-Si TFT technology for displays offers an alternative to the costly and difficult LTPS approach. Disadvantages in a-Si TFT performance include lower carrier mobility and threshold voltage stability, due to defect state creation and charge trapping [4]. Recent reports indicate, however, that with appropriate drive circuitry they can meet the performance criteria for display backplanes [5,6,7]. Current-programmed drive circuits that provide compensation for Vt shifts have been developed [7]. Figure 2.1 shows typical TFT configurations for display applications.



(a) (b)

Figure 2.1: Typical TFT configurations for display applications. (a) Etch stopper configuration. (b) Etch back configuration. The pixel ITO represents area reserved for the display device.

The basic TFT structure consists of (1) glass substrate, (2) bottom gate metal film, (3) gate insulator (SiNx), (4) semiconductor layer (a-Si), (5) contact layer (n+ a-Si) and (6) metal source/drain contacts. Figure 2.1 shows structures with and without an etch stop for the metal/contact definition. Once the gate metal is patterned, layers 3, 4 and 5 can be deposited sequentially without breaking vacuum in a PECVD system. Metal sputtering, photolithography and a combination of wet and dry (RIE) etching are done to define the source/drain regions. The n+ a-Si layer is doped during deposition.

A n+ contact TFT device turns on by applying a positive bias (referenced to the source electrode) on the gate electrode (V_{GS}), establishing a conducting channel that enables electrons to flow from the source to the drain with an appropriate drain bias. The device turns off by swinging V_{GS} to zero (or negative), depleting the channel, thus eliminating the conduction path.

In addition to display technologies, polysilicon TFT technology can be used in printer heads or image sensors. One desirable area for TFTs is in three-dimensional integration of static random access memory (SRAM) using a TFT as a load transistor above the single crystalline substrate [8]. To the author’s knowledge, this application has been limited so far to a research curiosity due to performance issues and process complexity.

2.2.1. POLYSILICON GRAIN BOUNDARY THEORY

Complex logic circuitry is not included on display panels with amorphous or polysilicon back planes for one main reason: low mobility. Reduced mobility severely reduces NMOS performance compared to crystalline silicon, and virtually eliminates the possibility of a useful PMOS device. Therefore complementary logic, CMOS is not feasible. Complex logic can be performed using NMOS only circuitry, but because load devices are required for the pull up network, NMOS only circuits use considerable current. For this reason NMOS only circuits are power hungry – not a good choice for the mobile community of electronic devices.

To understand mobility in amorphous or polysilicon silicon devices, a brief look into grain boundaries and grain boundary theory is provided. Polysilicon or any polycrystalline material is made up of many small crystalline pieces joined together at grain boundaries [9]. The grains are the crystalline regions that exhibit periodic arrangements of atoms. Grain boundaries are the transition regions. In the transition regions, differently orientated grains attempt to align; this creates a disorderly arrangement of atoms and dangling bonds. The grain boundaries are the primary reason that polysilicon transistors are inferior to devices fabricated in crystalline silicon. Disorder at the grain boundaries presents a significant hindrance to channel conduction due to trap states at the grain boundaries. The traps seize carriers, reducing the number of carriers available for current conduction. Charge builds up at the trap location, causing a potential barrier [9].

In 1975, John Seto reported two lines of reasoning as to why grain boundaries affect electrical properties. The first idea is that grain boundaries act as sinks for

impurity atoms, reducing doping in the grains, and increasing grain resistance. This idea has a critical flaw because dopants, such as boron, do not segregate into the boundaries until extremely high concentrations are reached (atomic percentage doping levels). The second idea is that due to the disorder at the grain boundaries, there are a large number of defects at the boundaries. Therefore, there is a large number of trap states in the boundary. The traps are thought to seize carriers, reducing the number of carriers for current conduction. Charge builds up at the trap location, causing a potential barrier [9]. This is generally regarded as the prime hindrance of channel conduction in polysilicon TFT.

Traps at the grain boundaries inhibit carrier movement by reducing the number of free carriers and building up charge, causing a potential barrier. To derive expressions for barrier height E_B and mobility, some simplifying assumptions are made [9,10]. The crystalline grains are all assumed to be of equal length. All traps are located at a single trap energy level E_t in the grain boundary. The traps are initially neutral and become charged upon trapping a carrier. The length or thickness of a grain boundary is considered much less than the length of a grain. It is also assumed that the polysilicon is uniformly doped, and that the impurity atoms are completely activated, or ionized. The problem is treated as one dimensional, a line in the channel cutting through grains, and intersecting grain boundaries.

Now, the depletion approximation can be applied to the grain boundary. This assumes that all free carriers are outside the depletion width or trapped in the grain boundary sites. With the preceding assumptions, a charge distribution plot as a function of x can be constructed. From the charge distribution, it is qualitatively seen that an

electric field is present, and the electric field will cause energy band bending as shown in figure 2.2. The bending of the bands causes a barrier for current flow, in this case, a barrier for holes.

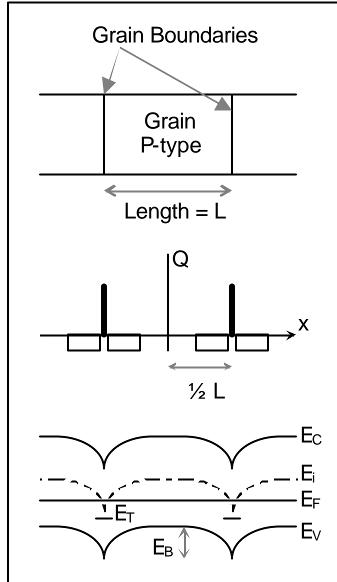


Figure 2.2: Grain boundary energy band diagram

To find the height of the barrier, or the barrier potential (V_L), we can follow the analysis by Seto, 1975 [9]. Using the depletion approximation, and applying Poisson's equation from 0 to ½ L, equation 1 is found [9].

$$\frac{d^2V}{dx^2} = \frac{qN_A}{\boldsymbol{e}}$$

Equation 2.1

Equation 2.1 can be integrated twice using a boundary condition that potential is continuous and equal to the 'bulk' crystalline potential (V_{V0}) at the depletion edge (x = ld). Furthermore, electric field is zero at l_d. The application of these boundary conditions yields an equation for potential as a function of x.

A crystal grain can either be fully depleted or partially depleted. For a given length grain, this depends on doping and trap concentrations. The number of traps must be greater than the product of doping concentration and grain length in order to be fully depleted. Similarly, the number of traps must be less than the doping length product to be partially depleted. When a grain is fully depleted, the depletion boundary is located at x = 0. Barrier potential can then be determined, recognizing that V_B is the difference of the max and min of the energy band plot (V(0) and V(½L)). Equation 2.2 gives the potential barrier when the grain is completely depleted, according to Seto [9].

$$V_B = \frac{qL^2 N_A}{8\boldsymbol{e}}$$

Equation 2.2

When the grain is partially depleted, the potential barrier can be determined by equation 2.3. The maximum potential occurs when the number of traps (N_T) is equal to the doping length product.

$$V_B = \frac{qN_t^{\,2}}{8\boldsymbol{e}N_A}$$

Equation 2.3

Potential varies linearly with doping up to the maximum barrier potential. The maximum occurs when the number of traps is equal to the doping length product. After the maximum, V_B decreases as 1/N [9]. With the barrier potential defined, resistance of polysilicon is better understood. Polysilicon resistance is made up of a grain boundary component (R_{GB}) and a grain component (R_G). R_{GB} is much greater than R_G due to the barrier associated with the grain boundary. Therefore, the resistance associated with the grain can be neglected in this analysis. For carriers to pass the barrier, it is necessary for

them to go over the barrier (thermionic emission), or tunnel through it (field emission). Thermionic emission will occur when a carrier gains energy greater than the barrier and sufficient momentum. Tunneling can occur for a narrow and tall barrier. In this case, the carrier may have less energy than the barrier, but the width of the barrier must be thin enough to have a sufficient probability for quantum-mechanically tunneling. As noted by Seto, the potential barrier in polysilicon is too wide for a significant probability of tunneling [9]. Tunneling will be neglected in this treatment.

Equation 4 is a general equation for current density due to thermionic emission across a grain boundary [9]. Equation 2.4 assumes that there is negligible scattering in the depletion regions of the grain boundary.

$$J = q \cdot p_o \cdot v_c \exp\left(\frac{-E_B}{kT}\right)\left[\exp\left(\frac{qV_d}{kT}\right) - 1\right]$$

Equation 2.4

In Equation 4, v_c is the thermal collection velocity, V_d is the bias voltage across the grain boundary, p_o is the average free carrier concentration, and E_B is the energy barrier ($E_B = qV_B$). Because equation 2.4 neglects scattering, it is only valid for small currents, therefore, V_d must be small.

With an applied bias much less than the thermal voltage ($V_d << kT$), equation 2.5 can be used [9], [10].

$$J = q^2 p_o \left(\frac{v_c}{kT} \right) \exp\left(\frac{-E_B}{kT} \right) V_d$$

Equation 2.5

In this form conductivity can be easily found, and then mobility as shown in equations 2.6 and 2.7.

$$\sigma = \frac{L \cdot J}{V_d} \qquad \mu = \frac{\sigma}{q \cdot p_o}$$

Equation 2.6 Equation 2.7

From this interpretation, it appears that mobility is represented as an exponential function of the energy barrier. Levinson et al. proposes instead that carrier concentration is an exponential function of energy barrier. His equations are not in contradiction with Seto's, it is simply a difference in interpretation of the expression.

Mobility in polysilicon transistors has been shown to be a direct function of grain size and gate length. To achieve maximum mobility the grains must be large and the channel region placed within the grain. Within-grain placement of each transistor may be accomplished by laser re-crystallization. Single crystal silicon can, however, provide even higher mobility with reduced process complexity.

A comparison table of typical amorphous and polysilicon operating characteristics for a display backplane is shown in table 2.1. Note the high operating voltages, and comparatively low mobility/on current compared to a crystalline silicon process which could have mobilities up into the thousands, with greater on current at only 5 volts.

	Amorphous-silicon	Poly-silicon	
Mobility	0.5 - 1	50 - 200	cm^2/Vs
On Current	0.1	15	μA/μm
VDD	20	20	V

Table 2.1: Approximate operating characteristics of amorphous and poly-silicon [11]

2.3. SOI TECHNOLOGY

The semiconductor industry has adopted SOI technology in production for many microelectronic applications. This is because there are many benefits to SOI over bulk silicon. The reduced junction capacitance, from reduced source drain junction area, increases the maximum frequency of operation. Low power consuming, high-speed circuits are possible since the load capacitances are reduced. CMOS latch-up is eliminated with SOI, as each device is totally isolated. Improved isolation also enables the integration of high frequency passive components.

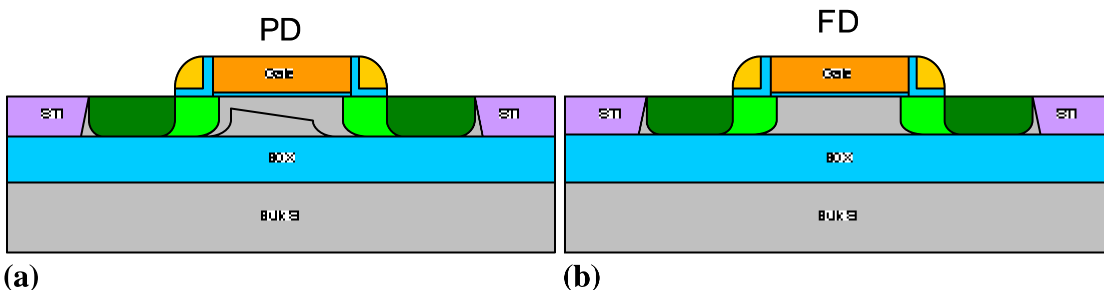


Figure 2.3: Schematic representation of (a) partially depleted and (b) fully depleted SOI transistors.

SOI devices body regions can be either partially depleted (PD) or fully depleted (FD). A SOI device is fully depleted when the body is depleted of carriers, and the depletion charge is constant and will not extend further. Partially depleted devices are similar to bulk silicon devices in that there is body under the gate that is not depleted.

An advantage of PD devices is that well established features such as retrograde wells, halo implants, and S/D extensions can be used to control short channel effects. Without a body contact, however, the body of a PD device is electrically floating. Body contacts are not desirable as they take up valuable real-estate. During normal operation the body will charge and discharge, which occurs by generation and recombination of carriers created via impact ionization at the drain end of the channel. This sets the body at a particular voltage, thus V_{BS} and V_{BD} will not be the expected values; this is known as the history effect [12]. Several adverse effects on device behavior can occur. The history effect causes a variation in gate delay. Body charging can forward bias the body-source pn junction resulting in a parasitic shunt bipolar transistor. The parasitic BJT effectively lowers the SOI device threshold voltage. The floating body also causes drain induced barrier lowering (DIBL) to increase; as the body charge increases, V_T decreases causing additional barrier lowering. Body charging can also be attributed to gate induced drain leakage (GIDL); band to band tunneling between the body and drain in the off state [13].

FD SOI devices offer several advantages over PD SOI devices, including steeper sub threshold slope (better off-state characteristics), larger saturation current at the same applied bias, reduced power consumption at a lower operating voltage, and no floating body effects. Fully depleted SOI transistors do exhibit increased short channel effects,

however, these can be suppressed if the silicon film thickness is much smaller than the depletion depth [14].

2.4. Device Considerations

Process details that must be engineered and thoroughly characterized for device modeling include dopant activation and dielectric quality, both of which will directly impact the device operation. Well formation and threshold voltage control via ion implantation is hardly possible due to the challenge of low-dose dopant activation. The developed process must ensure a well controlled and/or minimum level of interface charge for device consistency. Interface charge on both the glass-silicon and deposited oxide-silicon will influence the operation of the transistors, both of which will be investigated. This is particularly important in a fully-depleted device design. For a CMOS capability, a single-type semiconductor is the likely strategy for implementing both nfets and pfets, unlike standard CMOS processes. A metal gate which allows workfunction engineering for threshold voltage control may also be investigated.

CHAPTER 3

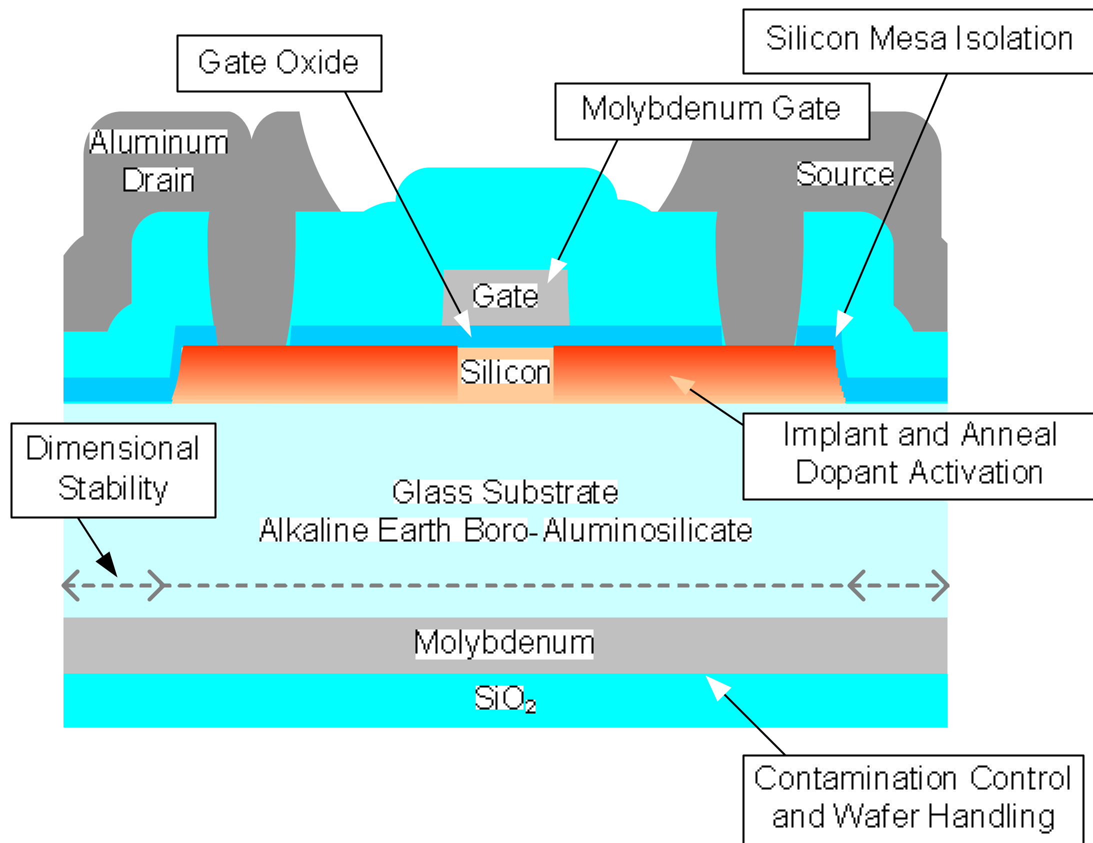
LOW-TEMPERATURE PROCESS DEVELOPMENT

3.1. INTRODUCTION

Thermal limitations of the Corning substrate required modification and development of typically standard CMOS process steps. The main technical process challenge associated with processing glass substrates was the low-temperature (LT) requirement. Procedural challenges included cross contamination of other standard CMOS processes and wafer handling. In this chapter the development of the unit processes specific to the Corning substrate are revealed.

Many of the LT unit processes could be developed on bulk silicon wafers. A simple isolation scheme, mesa (or island) isolation, was chosen. The silicon profile was carefully engineered to avoid a sharp profile; to preserve the integrity of a conformal oxide deposition. Within the temperature constraints of the substrate, thermal oxide cannot be grown at atmospheric pressures; therefore a deposited oxide was used. A self-aligned source/drain was desired, thus a gate material was needed that could withstand

dopant activation anneal temperatures. Molybdenum, a refractory metal, was developed as the gate metal to fulfill this requirement. Perhaps the most important unit process developed for this SiOG was low temperature activation of dopants. Research was conducted to enhance the percentage of dopant activation at low temperatures by using pre-amorphization implants. Other procedural areas that needed to be addressed for the Corning substrates were glass contamination of standard CMOS processes, glass dimensional stability at process temperatures near the glass strain point, and wafer handling of glass substrates in silicon wafer tools. Figure 3.1 displays the process areas that are discussed in detail in the remaining sections of this chapter.



3.2. SILICON MESA ISOLATION

The isolation scheme developed for this process was mesa, or island isolation. The silicon was to be etched down to the glass surface, isolating it from other devices. This scheme could be further enhanced with a post trench etch filling with an oxide and chemical-mechanical planarization (CMP). For this process, the sidewall roughness and profile was a primary concern. It was desirable to have a smooth transition from the silicon mesa surface to the glass surface to prevent formation of thin gate oxide regions during gate deposition, which could lead to device failure.

A LAM490 plasma system was used to define the mesa; the isotropic etch was engineered to provide shallow sidewall angles. Power, pressure and gas flow were modified systematically to find an optimum profile. A LEO EVO 50 cross-sectional SEM was used to image the samples after etch. The etch recipe shown in table 3.1 produced ~ 56.5° sidewall angle, desirable results for conformal thin film coatings. The resulting silicon profile is shown in figure 3.2.

Etch Conditions	
SF6	150 sccm
O2	100 sccm
Gap	1.24 cm
Power	100 W

Table 3.1: Etch Conditions

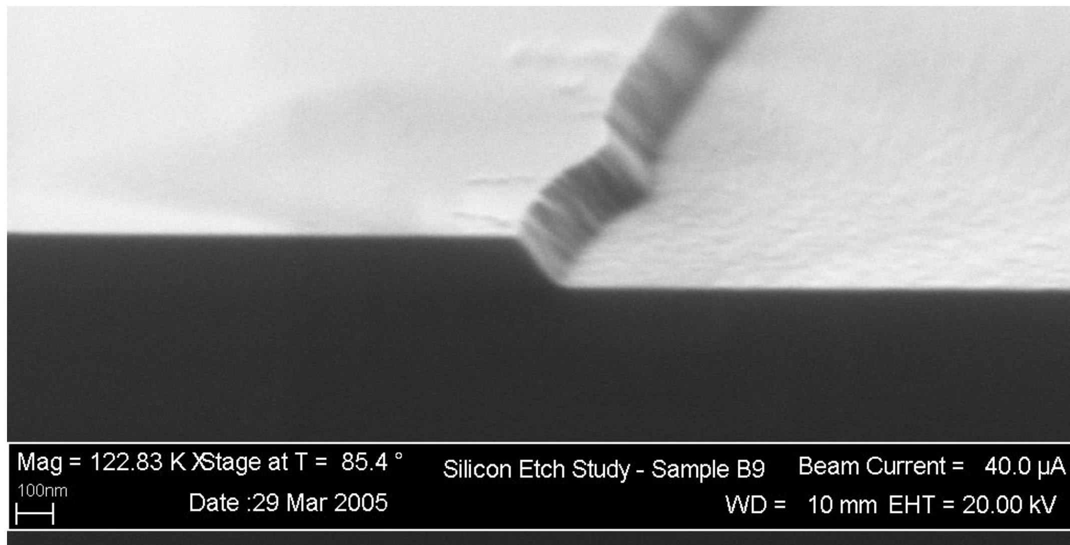


Figure 3.2: Silicon etch profile

3.3. OXIDE STUDY

At temperatures near 600°C, thermal oxide growth was not considered. Deposition methods that were investigated include LPCVD low temperature oxide (LTO), PECVD nitride, and PECVD TEOS-precursor oxide. For the available oxide options, the level of interface charge was the most important parameter. Interface charge can have a very significant effect on the threshold characteristics of a MOS device. The magnitude of the interface charge will determine how much of a shift in the threshold voltage there is while the polarity will make it shift either positive or negative. Typically, low levels of interface charge are on the order of 10^{10} cm^{-2} for a thermally grown oxide; deposited oxides tend to be higher. LPCVD LTO was found to have an interface state density of 6E11 cm^{-2} (after 2hr 600°C N_2 anneal) as measured with a SemiTest surface charge analyzer (SCA-2500). The PECVD TEOS had an interface charge of 1E12 cm^{-2} (after 1hr 600°C N_2 anneal) also measured by SCA. The deposition parameters for the LTO, however, had a larger thickness variation than the TEOS oxide film. The gate oxide

thickness contributes to the threshold characteristics of MOS devices. It is much easier to quantify threshold changes due to dielectric thickness variation than it is via interface charge levels. Thus LTO was chosen for initial SiOG process runs because it had less interface charge, with less variation compared to TEOS. Silane (SiH_4) and oxygen are used to form low temperature oxide. Table 3.2 provides the deposition conditions used.

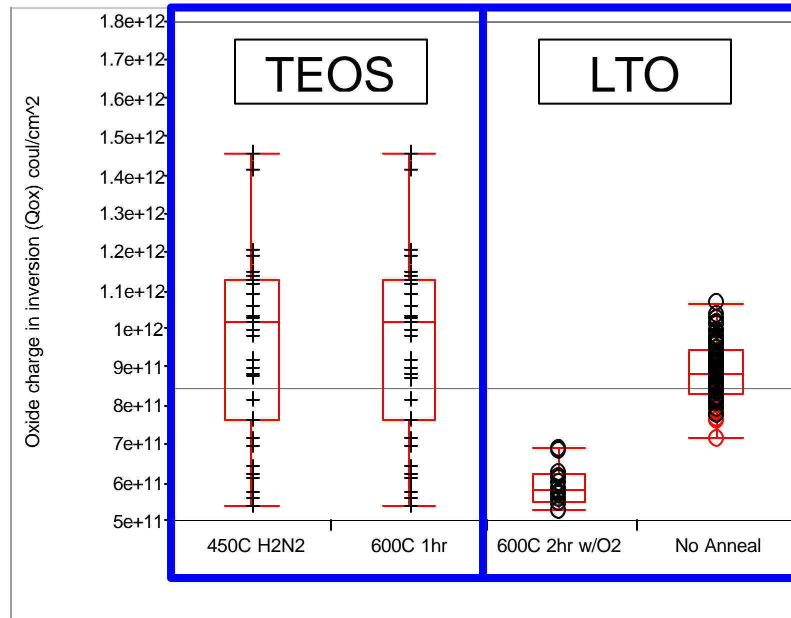


Figure 3.3: Oxide charge vs. oxide type and anneal treatment. With a 450°C H_2N_2 sinter or 600°C 1hr anneal, the TEOS oxide results look similar. The average charge levels observed for TEOS oxide were 9.8E11cm^{-2} with a sample standard deviation of 2.5E11 cm^{-2} (35 samples). TEOS samples that received no anneal or sinter did not measure on the SCA. LTO samples had low enough charge levels to be measured, averaging 8.9E11cm^{-2} with no sinter or anneal and a standard deviation of 7.5E10cm^{-2} (108 samples). A two hour oxygen anneal of LTO at 600°C provided the lowest charge levels averaging 5.9E11cm^{-2}, with the tightest distribution having a standard deviation of 7.5E10cm^{-2}.

LTO Recipe	
Temp	425℃
SiH_4	100 sccm
O_2	120 sccm
Dep Rate	125?/min

Table 3.2: LPCVD LTO deposition conditions

Capacitors fabricated on LTO with a 600°C post-deposition anneal showed excellent characteristics. Figure 3.4 displays a typical C-V characteristic from the 500? LTO process on a 3E15 p-type silicon wafer.

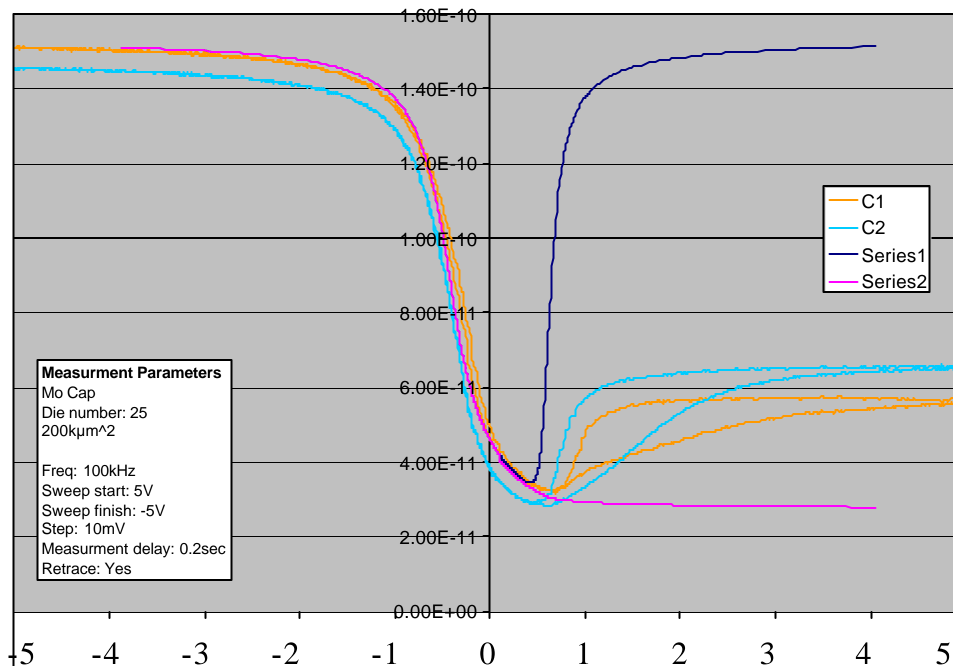


Figure 3.4: Typical LTO high-frequency (100kHz) CV characteristics from a p-type, 3E15 silicon wafer with an oxide thickness of 450?. Traces C1 and C2 are measured results, and Series1 and Series2 show theoretical low-frequency and high-frequency characteristics, respectively. The capacitance increase in inversion is due to the lack of field isolation. The mask defined capacitor size was 200kµm^2. The sample had a calculated fixed charge level of -4E10cm^{-2}, and negligible acceptor-like or donor-like interface trap charges. The flatband voltage was measured to be -0.44V, with a positive threshold voltage of 0.56V.

Results shown above suggest that LTO provides acceptable gate dielectric characteristics for MOS transistor applications. Integration of LTO into the LT CMOS process is given in chapter 4.

3.4. MOLYBDENUM GATE PROCESS

Polysilicon was not investigated as a gate material for the TFTs. It was hypothesized that the standard doping and diffusion process for a low resistivity poly would not be effective at temperatures around 600°C. Molybdenum was investigated as the gate metal for several reasons. First, it is a refractory metal with a high melting point of 2623°C [15] (compared to aluminum at 660.32°C). This allows Mo to be used in a self aligned process, much like polysilicon in a standard CMOS process, but with the benefit of a much lower resistivity. SRIM simulations were conducted to verify that the gate metal thickness would be enough to stop the dopant ions.

200 Kev Ion Implantation into Molybdenum		
Ion	**Projected Range ?**	**Longitudinal Straggle ?**
Argon	767 ?	414 ?
Phosphorus	951 ?	536 ?
Flourine	1520 ?	794 ?
Boron	2162 ?	859 ?

Table 3.3: Stopping and range calculations for the studied ions into molybdenum using SRIM software [16]. Worst case conditions were considered, 200Kev acceleration voltage, and 3800? was chosen, so consideration would not need to be given again to ion stopping by the gate metal.

A molybdenum deposition process was developed and characterized on a CVC-601 DC magnetron sputter deposition tool. Table 3.4(a) shows the deposition conditions. Molybdenum was dry etched in a reactive ion etch (RIE) Drytek Etch tool. A small designed experiment was conducted to find desirable etch conditions. The final etch conditions are shown in table 3.4(b). Timed etches were used for the final process with a

verification of end-point by visual changes in plasma wavelength. This system provided enough control to leave ~100? of oxide in the etched regions.

Mo Sputter Conditions	
Power:	300W
Pressure:	6.9mT
Argon:	26.2 sccm
Time:	~1600s

(a)

Mo Etch Conditions	
Power	100W
Pressure:	60mTorr
O2:	4 sccm
CF4:	29 sccm

(b)

Table 3.4: (a) Molybdenum sputter deposition conditions. Deposition rate under these conditions was approximately 143?/min. (b) Reactive ion etch conditions used for molybdenum. The etch rate was approximately 2300?/min.

In addition to the benefits already mentioned, the workfunction of molybdenum can be tuned through various techniques [4]. This allows for greater control of the threshold voltage of MOS devices. For the experiments encompassed in this thesis work, the normal workfunction of ~4.5V was investigated

Molybdenum was used as the gate metal, and also as a reflective/conductive backside layer to trigger wafer handlers on certain fabrication tools. One negative attribute of molybdenum is that it will oxidize readily at low temperatures, much more so than polysilicon when exposed to an atmosphere containing oxygen. A nitrogen rich atmospheric furnace contains enough oxygen to oxidize molybdenum. During the first anneal step of an initial lot, after molybdenum was deposited, all of the metal oxidized flaked off. Upon this observation, the problem was corrected by depositing a capping layer on top of the molybdenum film. For this process, a thin 1000Å PECVD TEOS based oxide was used.

3.5. Implant / Anneal Study for Low Temperature Dopant Activation

The primary goal for this investigation of dopant activation was to create low resistance source and drain regions. In conventional amorphous silicon or polysilicon, source/drain regions are formed via in-situ doped silicon deposition. While this is appropriate for traditional TFT fabrication, this study involved selectively modifying the electrical characteristics of an already-prepared silicon layer. This must be done using ion-implantation and activation annealing. Electrical activation level of dopants is known to be lower at 600°C than at typical CMOS process temperatures (T = 900°C). The percent activation of boron at 600°C from 1 second through 30 minutes was studied by Mokhberi, Griffin, and Plummer [18]. They reported approximately 10-20% activation of a given boron dose, depending on the time. The following parameters were included in this study: implant dose, pre-amorphization implant, anneal temperature, and anneal time. Both n-type and p-type (phosphorous and boron) implants were investigated.

An investigation on ion implantation and thermal activation was centered on creating low resistance source and drain regions. Toward that end, primarily high dose implants were investigated. Previous studies have shown that pre-amorphization of silicon can improve dopant activation [19,20]. This is typically done by implanting an isoelectronic impurity such as germanium or silicon itself. For these experiments, the options available for pre-amorphization included argon (inert carrier gas) or fluorine (available from the BF_3^+ spectrum). Several treatments were conducted to determine the impact on the degree of dopant activation as measured by a 4-pt probe. These treatments were repeated for the phosphorous activation study to determine whether they would offer improved activation or have negative consequences.

3.5.1 IMPLANT ACTIVATION EXPERIMENT

Phosphorus-doped n-type wafers were used to investigate boron implant activation, allowing for a sheet resistance measurement to quantify the level of dopant activation. Likewise, boron-doped p-type wafers were used to investigate phosphorous activation. The starting substrates were Cz-grown with a resistivity of 40-43 Ω-cm and 3-5 Ω-cm for the n-type and p-type wafers, respectively. The starting resistivity was mapped using the 4-pt probe technique followed by the deposition of 1000Å PECVD TEOS-oxide. A pre-amorphization implant was performed on two treatments; a 1E15 cm^{-2} fluorine implant at 75 KeV, and a 5E14 cm^{-2} argon implant at 170 KeV. The remaining treatments received no pre-amorphization implant. Next the primary dopant was implanted at 4E15 cm^{-2} with an implant energy of 34 KeV or 92 KeV, for the boron (B11) or phosphorous (P31) ions respectively. The dopant was then activated with a 600°C anneal; in addition two treatments were at annealed 550°C and 650°C. Note one treatment received an 8E15 cm^{-2} primary implant with no pre-amorphization and the nominal anneal at 600°C. The implant designed experiment is shown in table 3.5.

Pre-amorphization Implant			Primary Implant		Anneal
Species	Dose cm^{-2}	Energy (KeV)	Dose cm^{-2}	Energy {B11/P31}	Temp (°C)
None			4.0E+15	34/92	550
None			4.0E+15	34/92	600
Fluorine	1.0E+15	75	4.0E+15	34/92	600
Argon	5.0E+14	170	4.0E+15	34/92	600
None			4.0E+15	34/92	650
None			8.0E+15	34/92	600

Table 3.5: Initial implant and anneal experiments for source and drain dopant activation

Pre-amorphization implant doses and energies were calculated using SRIM [16] software. The energy was determined by placing the damage peak near the center of the primary implant (boron or phosphorous) profile. Dose was determined by using the dose required to displace more than $5x10^{22}$ silicon atoms/cm^3. At this dose, the crystalline structure is completely destroyed.

$$\frac{Displacments}{cm^2} = \left(\frac{\frac{Number}{Ion}}{Angstrom} \right) * Dose * 1 \times 10^8$$

Equation 3.1: Calculation of displacements from collision events

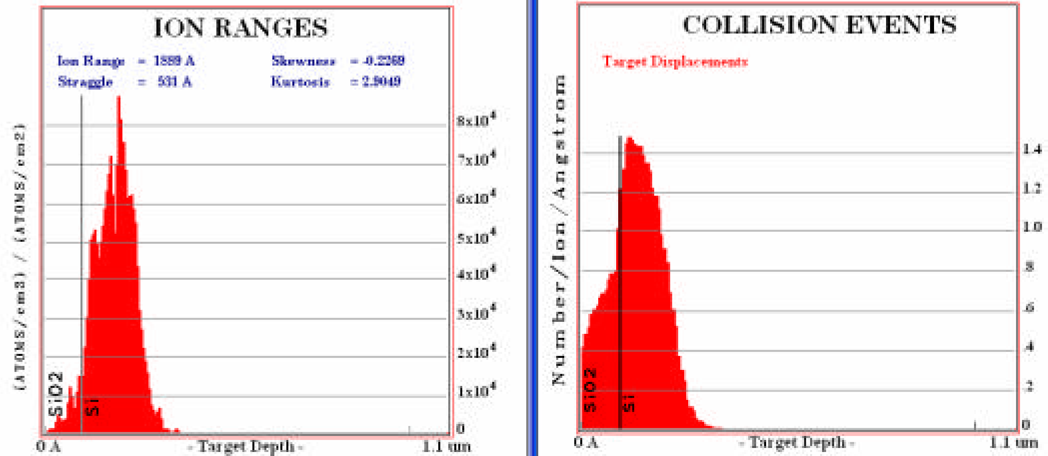


Figure 3.5: Ion ranges and collision events for 170Kev argon ions into 1000? screen oxide and crystalline silicon.

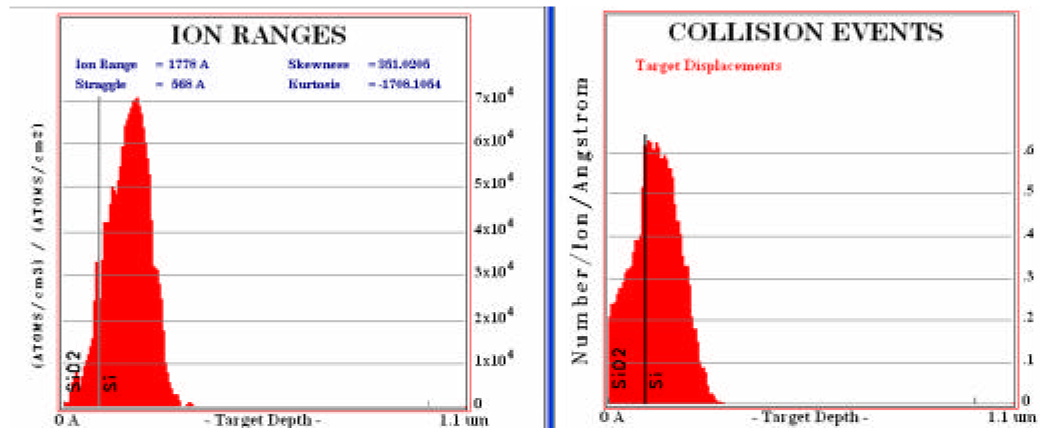


Figure 3.6: Ion ranges and collision events for 75Kev fluorine ions into 1000? screen oxide and crystalline silicon.

It is determined that for a 3.0E15 fluorine dose, approximately $1.5x10^{23}$ silicon atoms per cm^3 are displaced (up to 1000 ? into the silicon surface) using equation 3.1 and the results from SRIM simulation shown in figure 3.6. Therefore, the silicon structure up to that depth is completely amorphous. After the wafers were implanted with the specified doses, they were annealed at the times and temperatures shown in table 3.4. In addition to the times shown, much longer anneals (up to 24 hours) were completed to determine an appropriate experimental window.

Once annealing of the implanted substrates was completed, the screen oxide was removed and the sheet resistance was measured again. This sheet resistance value was used as a metric for determining the amount of dopant activation. To quantify the results the percent activation was plotted against dose, temperature and time. Note that the activated profile was simplified as a dose-scaled version of the implanted profile. While this simplification may not be entirely accurate, as in the case of approaching an electrically-active solubility limit, it was most useful in providing a relative comparison. It also must be noted that within the sheet resistance parameter is both carrier mobility and carrier concentration; these components cannot be isolated with this measurement technique. The amorphization and re-crystallization processes depend upon both the implant dose and damage distribution, however the relationships are quite complex and interaction effects were found to be significant.

As shown in figure 3.7, both argon and fluorine pre-amorphization implants demonstrate a large impact in the amount of boron activation. Also note that anneal temperature within the design space did not significantly affect activation. Figure 3.8 shows that both anneal temperature and the pre-amorphizing implants have little or no effect on the amount of activation for phosphorous. The lack of an effect on pre-amorphization is reasonable since the phosphorous ion (P31) will self-amorphize at the given dose.

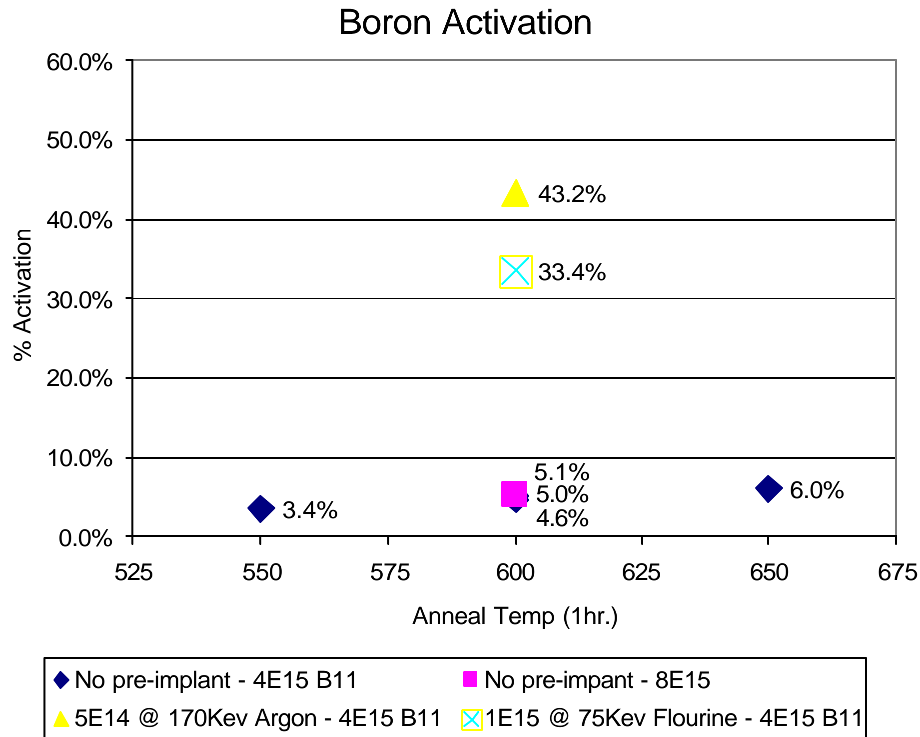


Figure 3.7: Boron implant and anneal experimental results for source and drain dopant activation

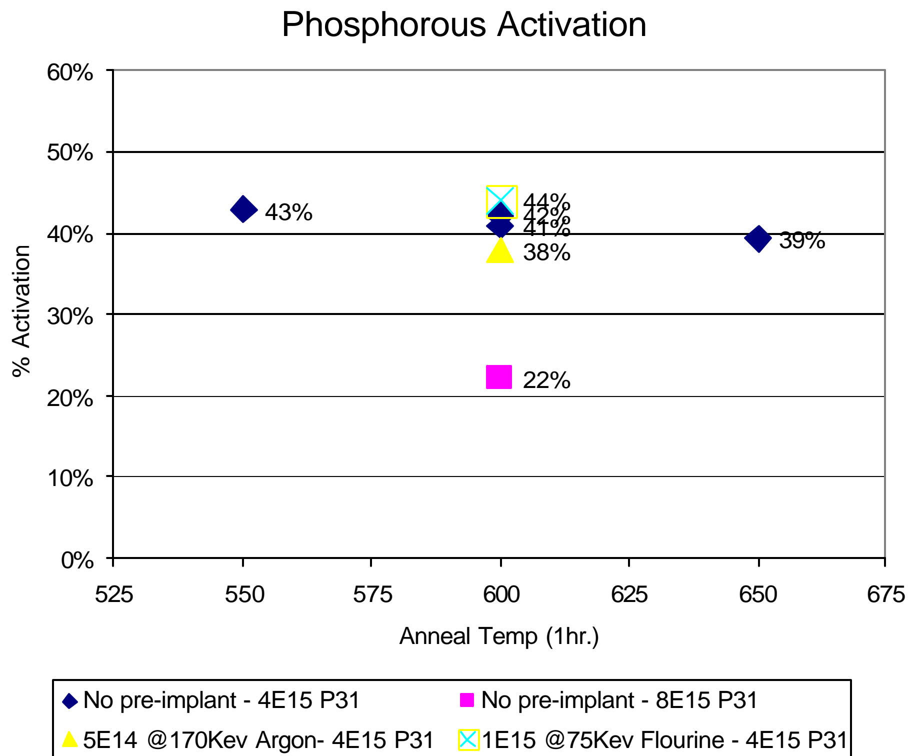


Figure 3.8: Phosphorous implant and anneal experimental results for source and drain dopant activation

A furnace anneal at 600°C for 1 hour demonstrated consistent results, and appeared to offer the same level of electrical activation as the 650°C anneal. Therefore, 600°C was chosen for the LT-CMOS process; well within the glass processing constraints.

Since both argon and fluorine pre-amorphization had a similar enhancement of boron activation, fluorine was chosen as the amorphization species due to the common introduction of fluorine from BF_2^+ molecular implants in standard CMOS processes. Additional experiments with a fluorine pre-amorphization implant of 3E15cm^{-2} demonstrated boron activation of ~ 50% at an implanted dose of 4E15cm^{-2}, thus an effective electrically-active dose of ~ 2E15cm^{-2}. An optimum implant recipe for the p+ boron-doped regions was determined to be F^+ 3E15cm^{-2} amorphization implant at an energy of 60KeV, followed by B^+ 4E15cm^{-2} at 40KeV. Note that the activation of BF_2^+ molecular implants was also investigated; results demonstrated a lower degree of activation compared to using a separate fluorine pre-amorphization implant.

The phosphorus results had the same effective electrically active dose of ~ 2E15cm^{-2} for both 4E15cm^{-2} and 8E15cm^{-2} phosphorus implants, indicating that the actual electrically-active profile is at a solubility limit. An optimum implant recipe for the n+ phosphorus-doped regions was determined to be P^+ 4E15cm^{-2} at an energy of 110KeV with no pre-amorphization.

The sheet resistance values obtained using the prescribed implant dose of 4E15cm^{-2} were 55Ω/sq and 100Ω/sq for n+ and p+ regions, respectively, formed on bulk silicon. Note that a portion of the implanted dose is blocked due to the 1000Å screen oxide present. The n+ layer formation had similar results on SiOG, where typical sheet resistance values were measured to be between 55-65Ω/sq. However the p+ layer formation on SiOG resulted in sheet resistance values between 250-300Ω/sq. It is

expected that the fluorine pre-amorphization extends throughout the silicon layer thickness (1500Å - 3500Å) and that subsequent annealing results in a polycrystalline phase due to lack of a crystalline seed region, thus an increase in the measured sheet resistance. For transistor fabrication the channel region remains undamaged, from which solid-phase epitaxy can originate during the source/drain anneal. The p+ layer sheet resistance on SiOG that represents the actual transistor source/drain regions has yet to be established; Vander Paw structures which will have undamaged silicon surrounding the p+ region will be included in the next testchip design.

3.6. CONSTRAINTS OF SILICON ON GLASS

Corning's silicon on glass (SiOG) substrate poses several unique process constraints. These constraints include, but are not limited to: dimensional stability, cross contamination, wafer handling, and gate stability. Each of these issues will be discussed in subsequent sections.

3.6.1. DIMENSIONAL STABILITY

Temperature constraints of the glass prohibit the use of high temperatures, found in traditional CMOS processing, for the fabrication of devices. The temperature constraint of the glass is limited to 666°C; this temperature is known as the strain point [1]. At and above this temperature, the glass will deform significantly causing substrate warpage or other non-desirable effects. Changes in the substrate, however, can still occur just below the strain point causing a dimensional shrinkage, on the ppm scale, of the glass substrate. This was observed during annealing at 600°C. This kind of dimensional instability will cause small changes in global registration (314 ppm in x and y) when doing alignment for photolithography processing. In the initial fabrication runs, the

photolithography stepper job was modified to compensate for the shrinkage caused by 600°C thermal steps. The die spacing was adjusted, and overlay tolerances were built into the devices to provide passing alignment within die. After a thermal step at 600°C it was found that subsequent thermal steps did not cause considerable registration variation. In subsequent processing, the starting substrates were heat treated for 8 hrs at 600°C before initial fabrication steps. This step prevented measurable registration change during thermal process steps.

3.6.2. CONTAMINATION

Fabrication of the devices took place in RIT's SMFL cleanroom facilities. Consideration for other active research and fabrication work had to be taken while fabricating SiOG TFT devices.

Because Corning's Eagle 2000 is an Alkaline Earth Boro-Aluminosilicate, there was a general concern of cross contamination issues with the bulk silicon based CMOS processes that are run at RIT's SMFL. Fabrication of MOS devices ranging from a 10µm PMOS process to a submicron CMOS process occurred at regular intervals at RIT. Consequently, the glass surface (backside) was sealed, and the most sensitive tools were not used on the route. Deposited SiO_2 was used to seal the backside. After exposing the front glass surface (post isolation etch), SiO2 was deposited to seal the front surface. Furnace operations were at high risk for cross contamination from the glass, so a furnace tube was dedicated to SiOG processing. Similarly, a separate wet chemical hot pot was used to clean SiOG wafers.

3.6.3. Wafer Handling Requirements for SiOG

RIT's SMFL toolset is designed to handle 100mm and 150mm silicon wafers. Many of the tools use capacitance sensors, and/or optical edge sensors which do not function properly with a transparent glass substrate. 3800? of molybdenum sputtered onto the backside of the glass is sufficient to provide an opaque appearance. The deposited backside film was successful in triggering both the optical and capacitive sensors of tools in the SMFL, allowing for fabrication to take place.

3.6.4. Low Thermal Conductivity of Glass

During the initial stages of process development, consideration was given to the low thermal conductivity of glass and its effects on photolithography. Bake times and temperatures were discussed, investigated, and modified to ensure desirable resist profiles. Substrate heating during ion implant, however, was not considered. In RIT's Varian 350D implant system the wafer chuck is cooled. This provides adequate cooling for silicon wafers, but not for SiOG wafers. Heat build up on the front side of the glass wafers cannot be transferred to the cooled chuck as efficiently. Excessive surface heating burnt resist films and caused stress in the thin silicon layer. The stress resulted in micro-cracks in some areas of the wafer. The burnt resist was removed via oxygen plasma, and processing continued. Successive implants were done at much lower beam currents to reduce the amount of in-situ heating.

3.6.5. Preparation for Process Challenges

Before testing the process design, it was understood that unforeseen challenges would arise. Corning was also in the early learning stages of substrate fabrication. Early simulation work showed that a higher doped substrate (higher than Corning had available

at the time) would significantly reduce the influence of top (gate oxide/silicon interface) and bottom (silicon/glass substrate) interface charge. The first fabrication runs were done using the available substrates provided by Corning Inc. The intention with Lot 1A and 1B was to determine any process related issues and provide initial learning. Lot 1B made use of the knowledge gained from 1A and provided insight into the top and bottom charge mechanisms.

Lot 2 was fabricated with a substrate that had the desired doping level, prepared jointly by RIT and Corning. These wafers were prepared such that they had a surface concentration of 5E16 cm^{-3} surface concentration of boron. The process is very similar to a well formation in a conventional CMOS process. Details about the substrate fabrication are discussed in section 4.4. Because a simple structure was desired for the initial investigation, channel implants were not considered; the influence of a channel implant would have been confounded with the presence of expected interface charge.

3.7. CONCLUDING REMARKS

In the preceding sections, the development of foundry processes necessary for successful SiOG transistor realization was detailed. Major obstacles associated with the low temperature constraints of the glass such as finding a suitable gate dielectric, and activation of dopant were understood and an appropriate solution found. Other non-technical problems such as wafer handling, substrate dimensional stability, and contamination concerns were also addressed. With the developed unit processes, a MOS device could be designed and implemented on the Corning substrate.

CHAPTER 4

TFT PROCESS INTEGRATION AND DEVICE SIMULATION

4.1. INTRODUCTION

A low-temperature process was designed to demonstrate that the Corning substrate could yield working CMOS devices. The fabrication process sequence will be described in completion in this chapter. Differences between the first and second process runs will be emphasized where improvements were significant.

Overall processing of TFTs at low temperature has many similarities to traditional processing of CMOS transistors; there are, however, a few significant deviations as follows. Thermal oxide could not be grown at the required low temperature (T<600°C) thus a LPCVD LTO gate dielectric was implemented. Molybdenum gate material was a thermally stable substitute for in-situ doped polysilicon, which was not available at RIT and would have required an out-source service. Low-dose implants (i.e. well, channel-stop, threshold adjust) were avoided since their impact on carrier mobility and transistor performance was not certain.

4.2. Test Chip Layout

A test chip for the TFT process was designed to allow flexibility in process design, and to provide thorough characterization of the fabricated devices. The following features and devices were designed into the maskset: i-line and g-line compatible lithography alignment marks, body contacts (to the channel), full field inverter, dense and isolated lines for SEM work, complementary MOS devices of various dimensions, and the unofficial / unauthorized "Team Eagle" group logo. Figure 4.1 shows a 6x6 μm (LxW) device with a body contact. The active region (green) defines the silicon mesa isolated structure.

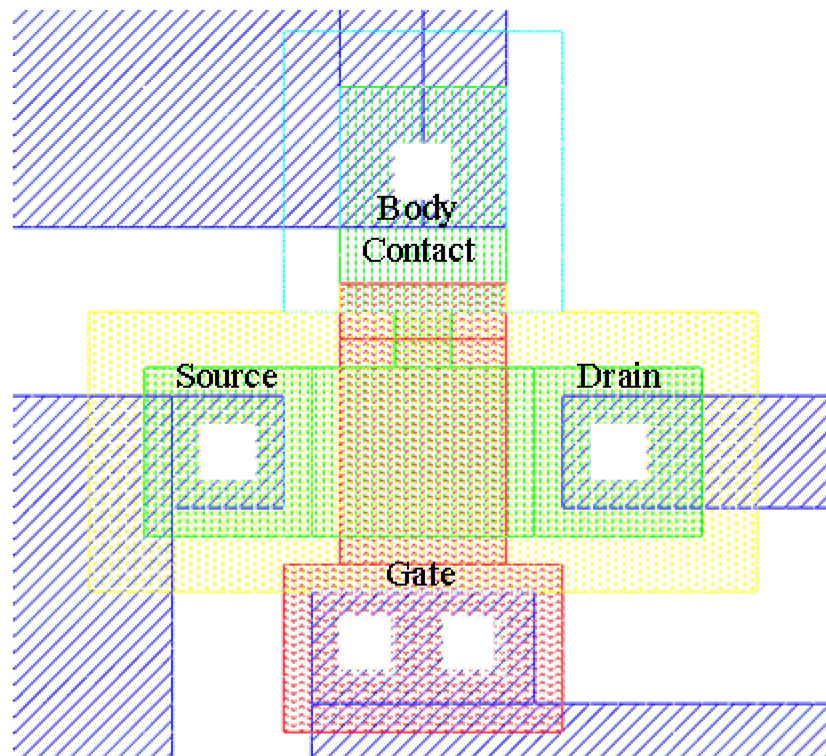


Figure 4.1: 6x6 μm device with a SOI style body contact. Note the body contact and gate polygons are arranged to maximize overlay tolerance.

Initial research was conducted on a g-line stepper. Although some gates were realized as small as 1μm, the smallest features were typically larger than 2μm, with contact cuts defined as 4x4μm to increase lithography CD and overlay tolerance. A set of devices with contact cuts at 2x2 μm was also designed, with gate lengths down to 0.3 μm. This was intended for use on one of RIT's higher resolution steppers (i-line, 365nm or DUV, 248nm). This provided a mask set that could be used for several generations of TFT research (see fig. 4.2).

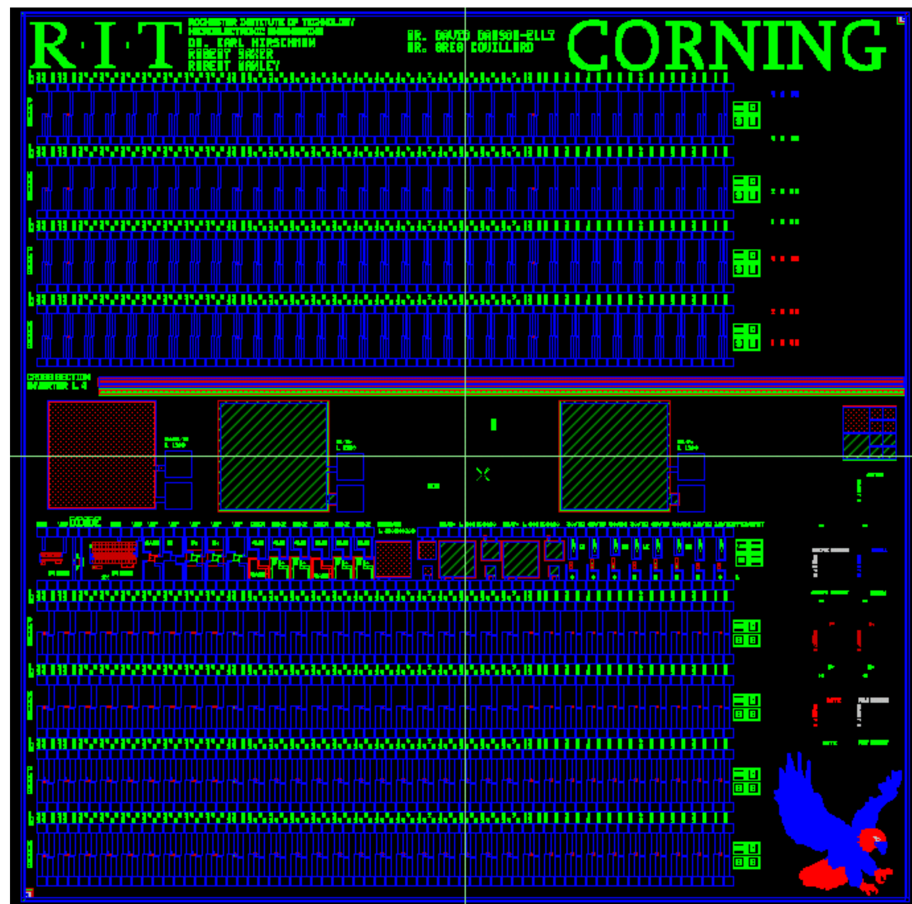
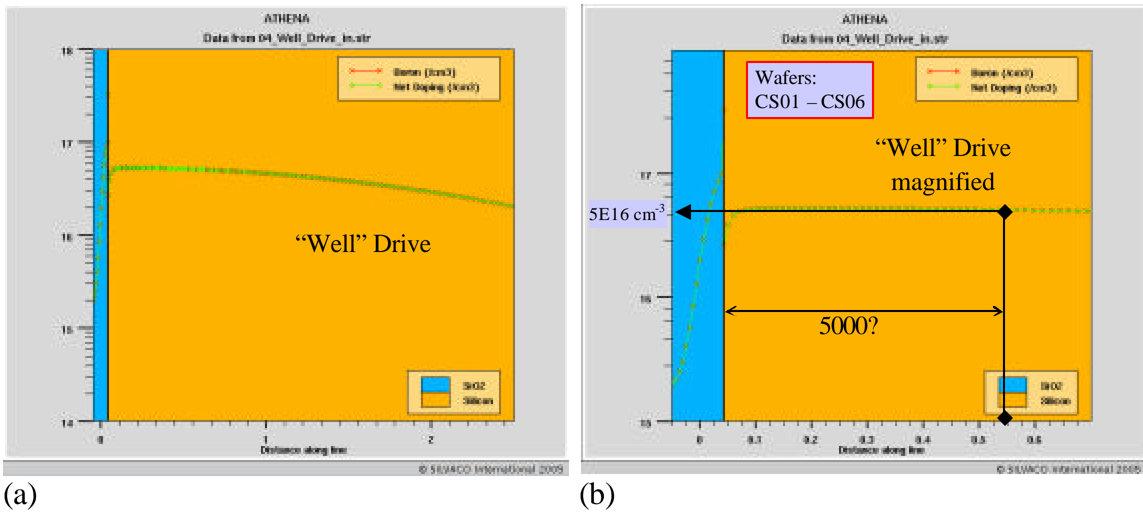


Figure 4.2: Test chip layout for TFT development. Process characterization structures include Van-Der-Pauw, cross bridge Kelvin resistors, capacitors, diodes, and a large width inverter for cross section. Transistors of varying length and width are included for parameter extraction.

4.3. STARTING SUBSTRATE PREPARATION

The SiOG wafers Corning had available for initial fabrication runs were of high resistivity. Their substrates were created using a proprietary process. It was desirable to have lower concentration substrates with a very specific doping value, thus n-well and p-well regions were not implemented. Since tight doping tolerances on standard silicon wafers were not readily available, substrates with custom doping characteristics were created at RIT. Starting with p-type 40ohm cm wafers, a 1000? wet oxide was thermally grown. A blanket 'well' was implanted into the wafers (B11, Dose = 1.6E13cm^{-2} Energy = 170Kev) then drove in for 22 hours at 1100°C. This created an extremely flat doping profile as shown in figure 4.3(b).



(a) (b)

Figure 4.3: Starting silicon "Well" profile after implant and drive-in. A specific and uniform doping profile was desired before sending silicon to Corning for their proprietary SiOG process.

4.4. PROCESS DESIGN & FABRICATION FLOW

The actual process design is displayed in the following figures. The figures are arranged in sequential processing order. The first processing step is illustrated in figure 4.5. A protective oxide layer (SiO_2) was deposited on the surface. The oxide served the following two purposes: it protected the silicon surface from contamination during initial processing, and it was a test run for subsequent gate oxide deposition. Consequently, the deposition was done on the same tool and with the same parameters as the gate oxide deposition, 500? of LPCVD LTO. Deposition parameter is shown in table 4.1.

LTO Recipe	
Temp	425℃
SiH4	100 sccm
O2	120 sccm
Dep Rate	125?/min

Table 4.1: LPCVD LTO deposition conditions

Molybdenum was sputtered onto the backside of the substrate (see fig. 4.6). This step facilitated wafer handling in the processing equipment. The same recipe was used as in the gate metal deposition (300W, 6.9mT from table 3.4), once again to verify deposition rate and yielding approximately 3800? of molybdenum. This thickness is sufficient to provide an opaque appearance, and molybdenum is conductive, thus allowing the substrate to be handled in tools with optical and/or capacitive sensors.

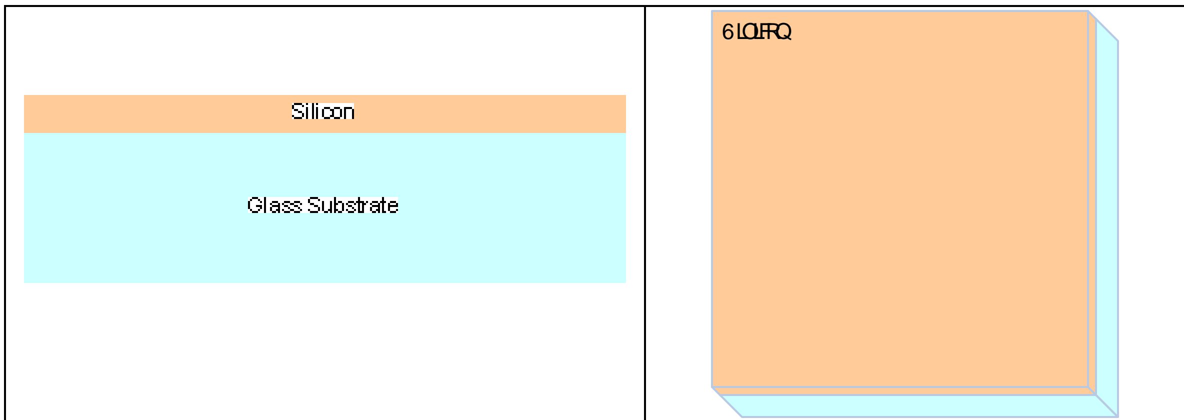


Figure 4.4: Starting SiOG substrate after silicon bonding, done by Corning, Inc.

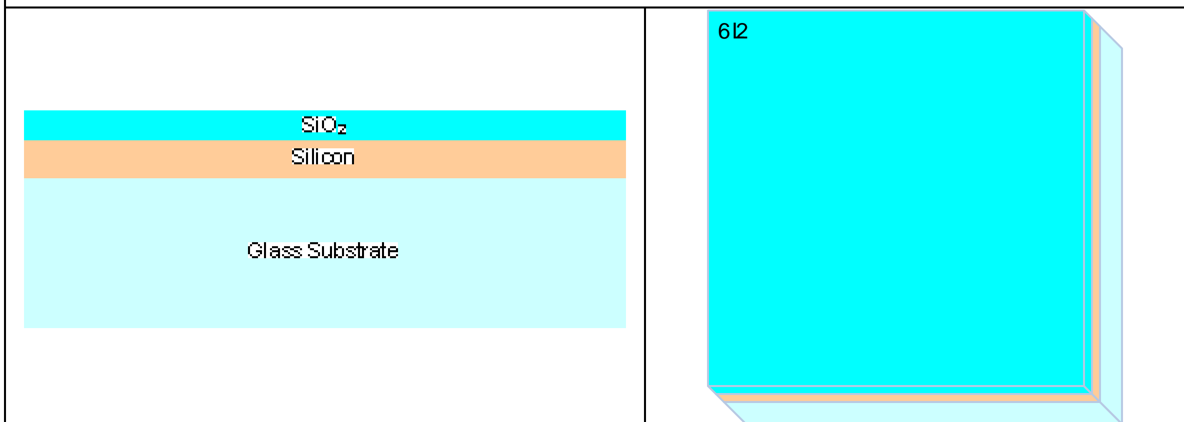


Figure 4.5: Protective LPCVD LTO deposition

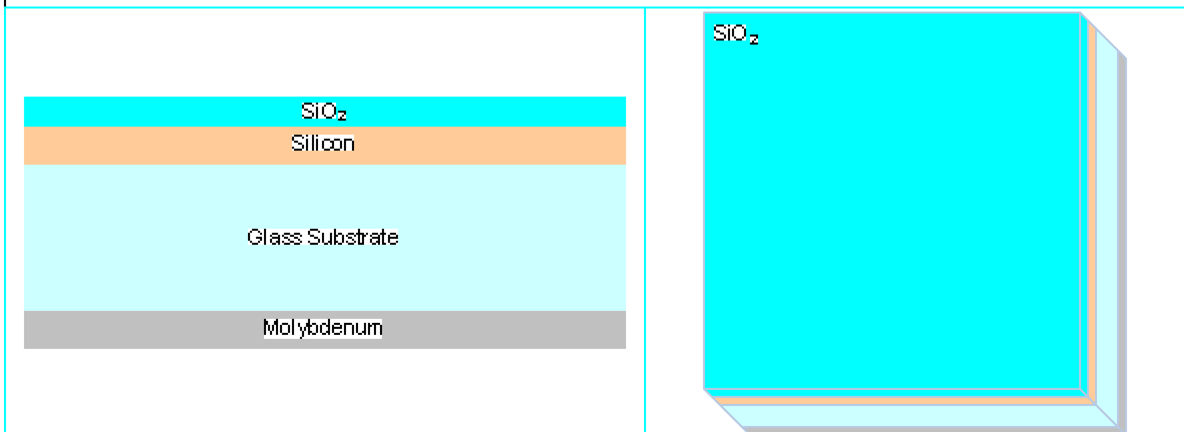


Figure 4.6: Backside molybdenum deposition

Molybdenum will oxidize rapidly in an atmospheric furnace at temperatures near 600°C. Oxygen plasma or chemical baths with hydrogen peroxide will also readily oxidize molybdenum. A TEOS PECVD oxide was chosen to cap the molybdenum on the backside of the wafer (see fig. 4.7). Due to subsequent HF acid dips, the thickness was set at 2μm so not to completely remove the protective backside oxide. This cap protected the molybdenum, and ensured that there was no potential of molybdenum contamination in the general SMFL toolset.

Photoresist was spun onto the wafers using a standard coat recipe (see fig. 4.8). It was found that there was no need to adjust the coat process. The standard coat recipe uses a HMDS prime and Rohm & Haas 1813 photoresist. In this study, g-line lithography was used (see fig 4.9) allowing imaging down to approximately 1 μm. Since glass is a good thermal insulator, the post develop hard bake time was lengthened from the standard process by a minute to insure an adequate thermal treatment.

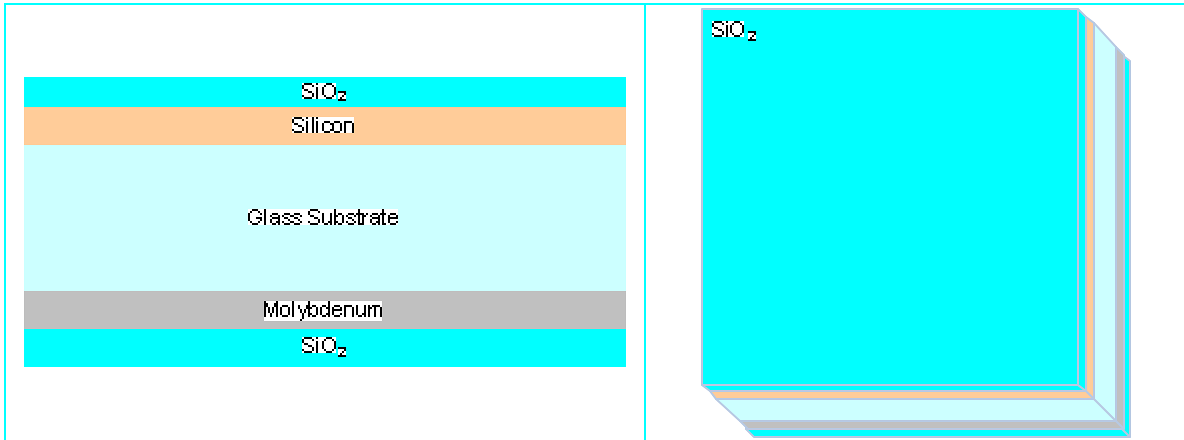


Figure 4.7: PECVD TEOS Backside protective oxide deposition

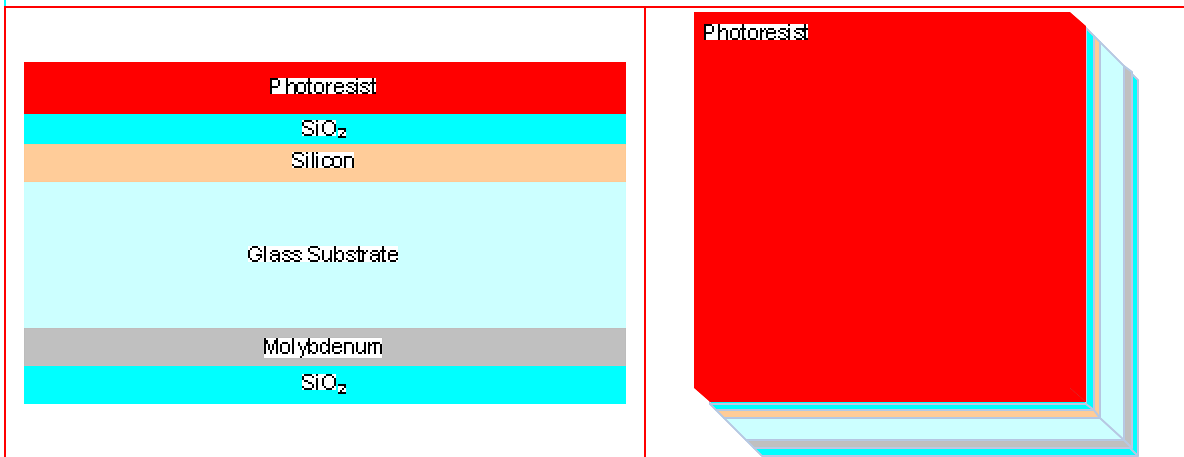


Figure 4.8: Photoresist coat

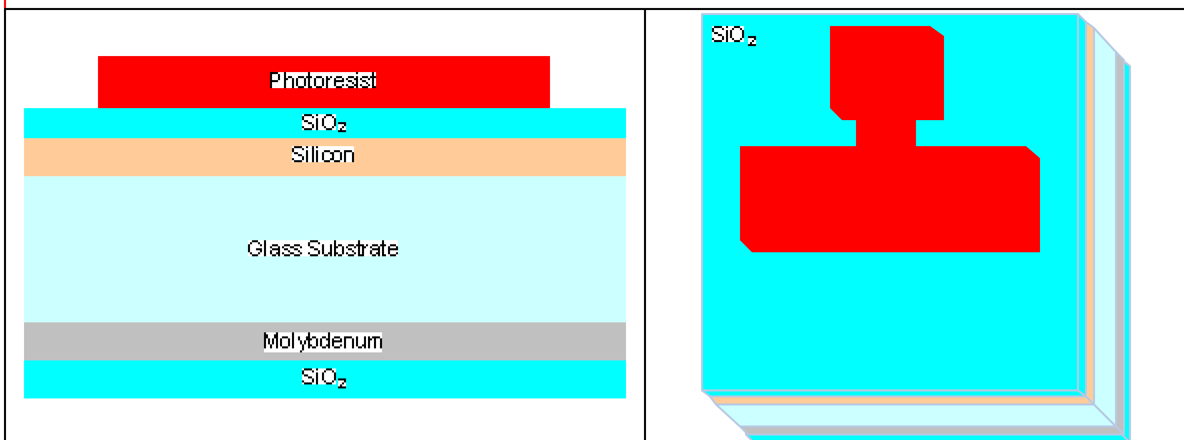


Figure 4.9: First level lithography, mesa isolation/active definition

The protective oxide was removed using a wet HF dip (see fig. 4.10), outside of the active area. The HF was 10:1 H_2O:HF, for a length of ~30sec.

An SF_6 and O_2 plasma was used to etch silicon, defining the mesa structure (see fig. 4.11). This scheme of isolation was chosen because it is effective and simple to implement. The primary goal of this etch step was to create a rounded edge, to gradually grade from silicon mesa to glass. This would allow for a more conformal deposition of the gate dielectric. A sharp transition point would lead to a thin region of gate dielectric causing increased gate leakage or a catastrophic failure. An experiment was run to determine optimum recipe conditions (see section 3.6). The photoresist was removed in a heated solvent strip bath (see fig. 4.12).

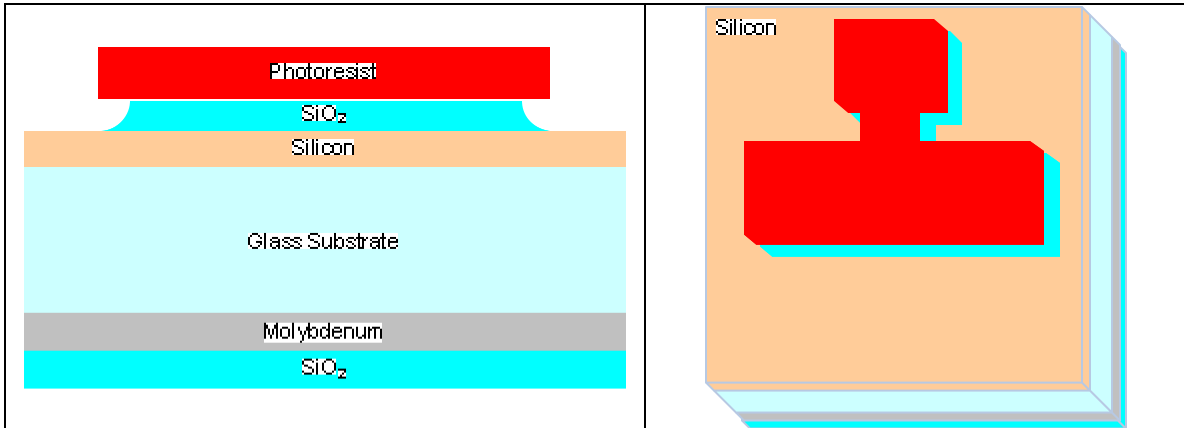


Figure 4.10: HF oxide removal

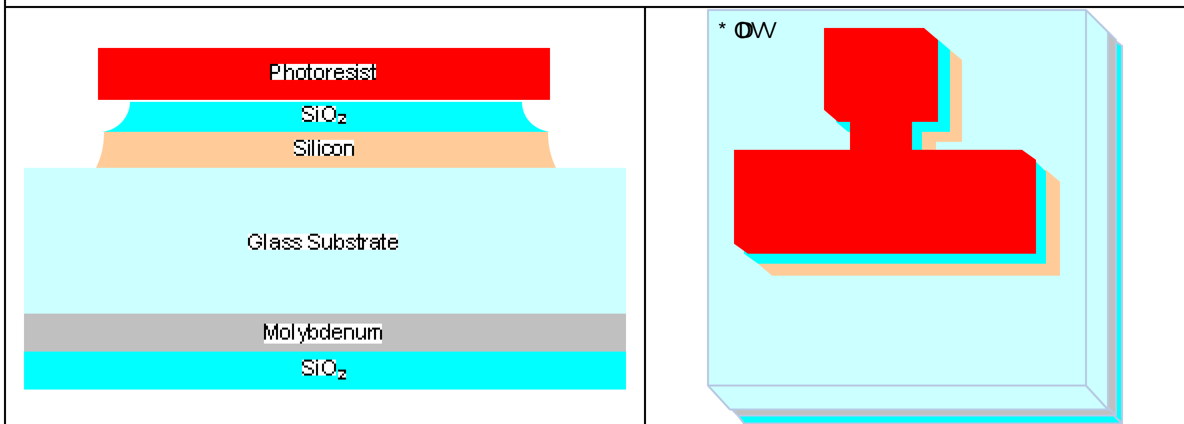


Figure 4.11: Mesa isolation etch

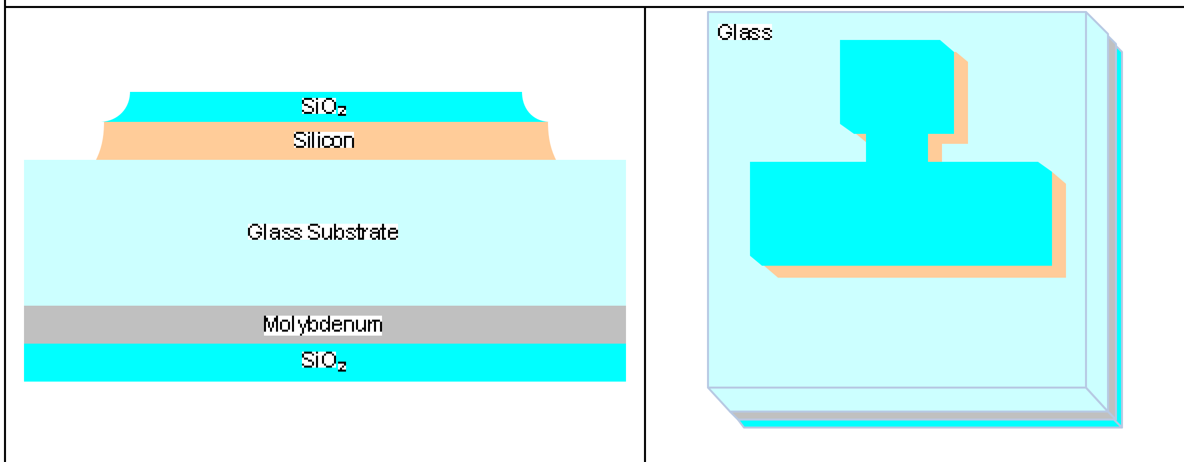


Figure 4.12: Photoresist strip

Following removal of resist, the protective oxide was completely removed (see fig. 4.13). This was accomplished with another HF acid dip. At this point the silicon channel region was cleaned using a heated bath of sulfuric acid and hydrogen peroxide (piranha etch). Piranha clean details are shown in table 4.2.

Piranha Clean	
H_2SO_4	5000 ml
H_2O_2	100 ml
Temp	130°C
Time	10 min

Table 4.2: Piranha clean recipe

The LTO gate oxide was deposited directly after the clean (see fig. 4.14). A LPCVD system was used to deposit the dielectric film onto the devices. The uniformity of LTO at the RIT SMFL is greater that ±5%, however, for this study this range of thickness was sufficient. The main benefit of LTO (over PEVCD oxide) was lower interface charge and trap densities (see chapter 3, section 3.3).

Next the molybdenum gate was sputtered using an RF sputter system (see fig. 4.15). Approximately 3800? of molybdenum was sputtered on the substrates. Table 4.3 shows the molybdenum deposition conditions (same as table 3.4, repeated for convenience).

Moly Deposition	
Power:	300W
Pressure:	6.9mT
Argon:	26.2 sccm
Time:	~1600s

Table 4.3: Molybdenum deposition conditions

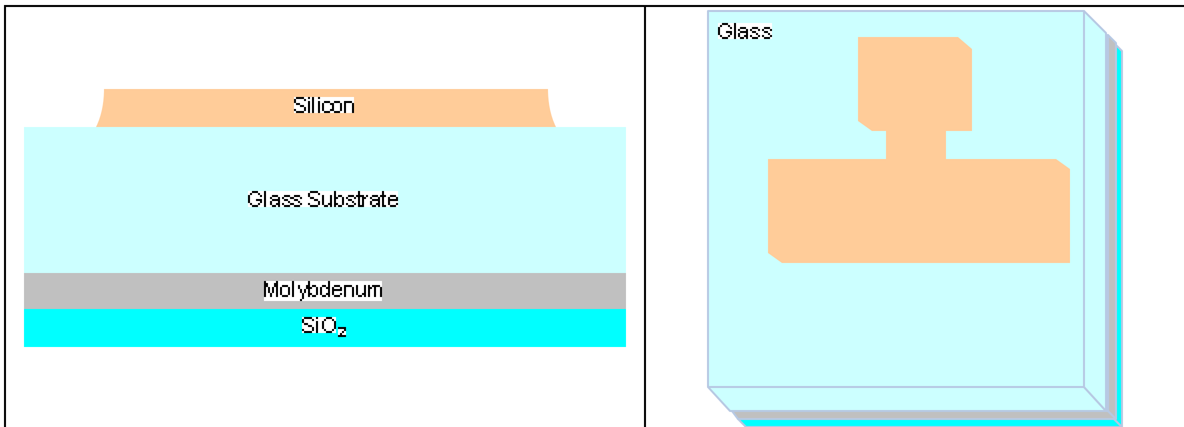


Figure 4.13: Protective oxide strip

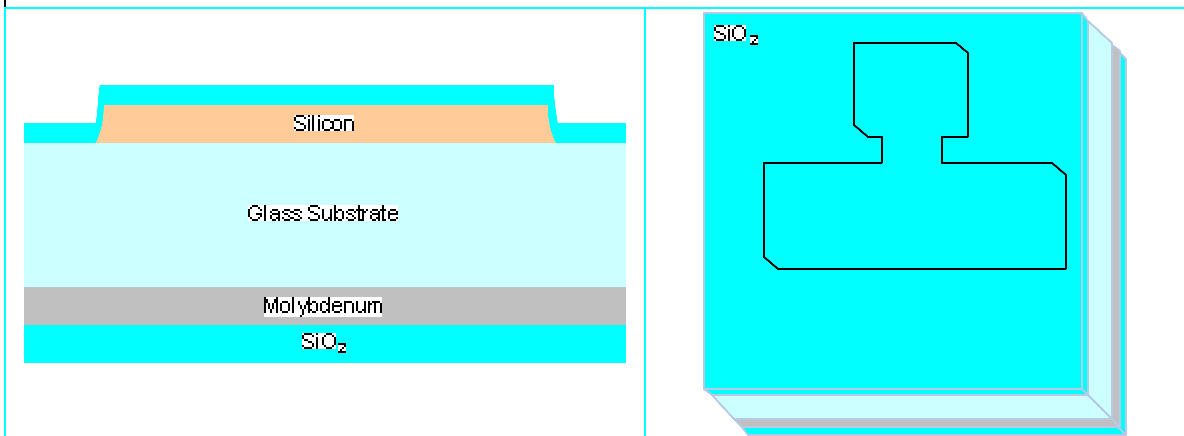


Figure 4.14: Gate oxide deposition

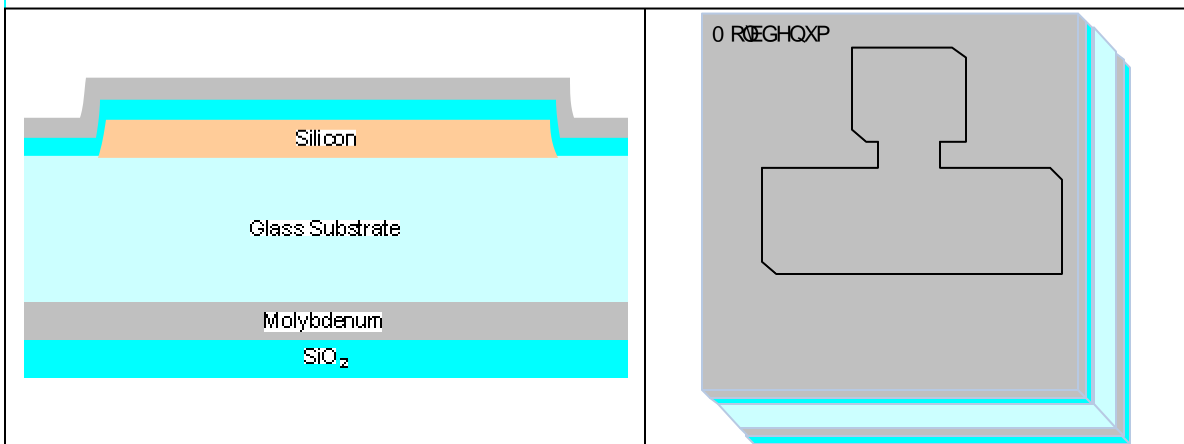


Figure 4.15: Gate metal deposition

Photoresist was coated on the wafers in preparation for gate lithography (see fig. 4.16). The resist was then exposed with the gate pattern (see fig. 4.17). In Lot 1 and Lot 2 the smallest dimension desired was a 1 μm gate, this requirement is within the performance capabilities of g-line lithography.

A RIE tool was used to etch the molybdenum (see fig. 4.18). Plasma chemistries were CF4 and Oxygen (section 3.5). Gate etch also defines the S/D region implant region, allowing them to be self-aligned to the gate.

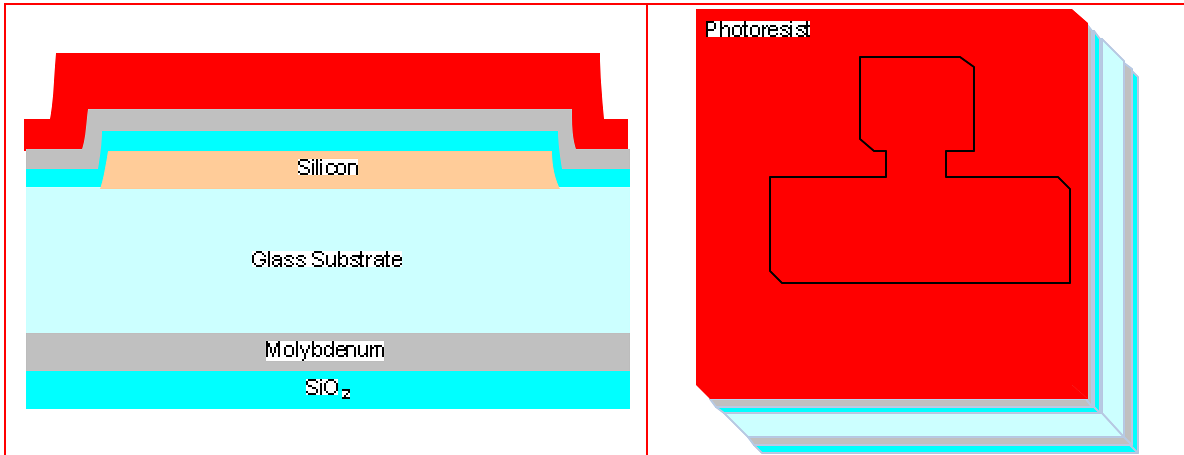


Figure 4.16: Photoresist coat

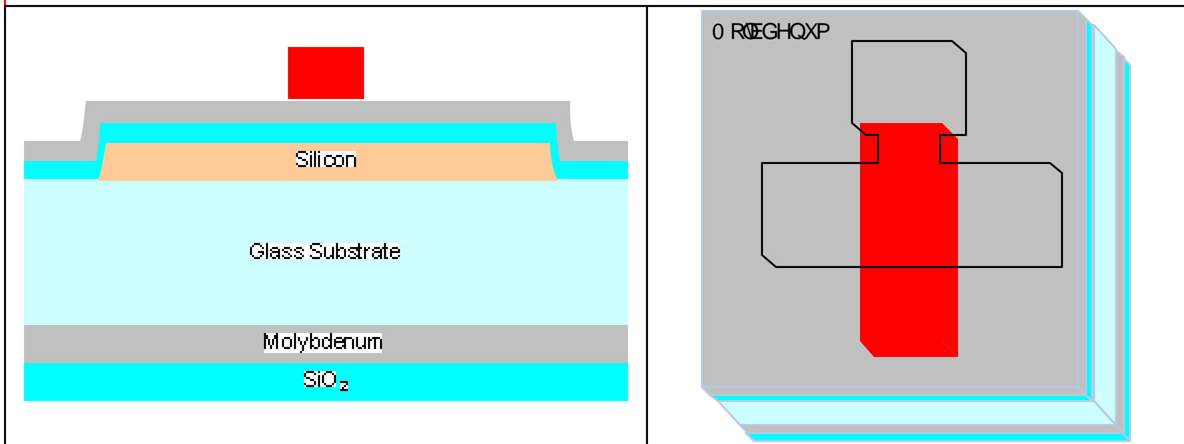


Figure 4.17: Gate photo patterning

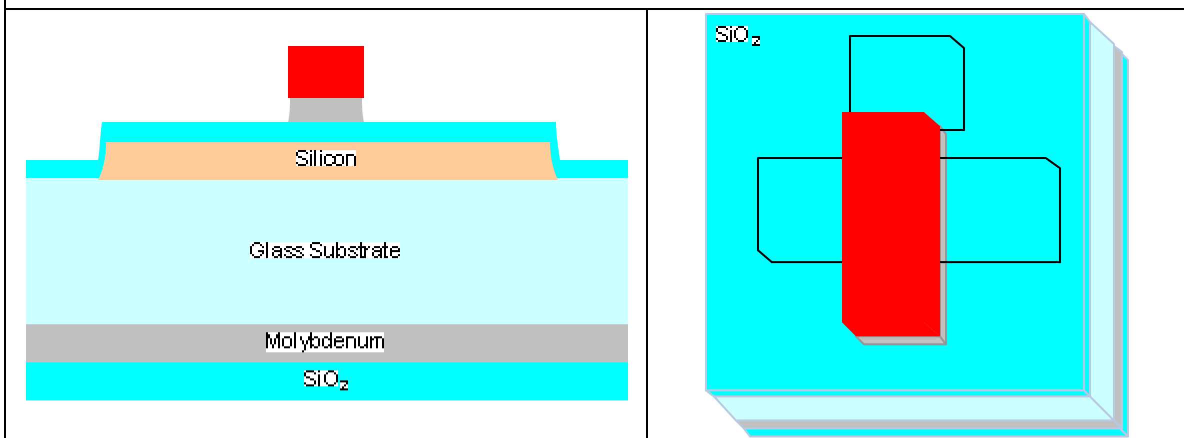


Figure 4.18: Molybdenum etch

The photoresist was removed in a heated solvent strip bath (see fig. 4.19) following the gate etch.

Oxide was deposited via TEOS based PECVD, to protect the molybdenum gates during subsequent anneal (see fig. 4.20). In addition, this oxide layer served as an implant screen for the source and drain implants. The target implant energy was increased by using a thicker screen, allowing both implants to occur within a normal operating range for the equipment at RIT's SMFL.

Next photoresist was coated on the wafers (see fig. 4.21).

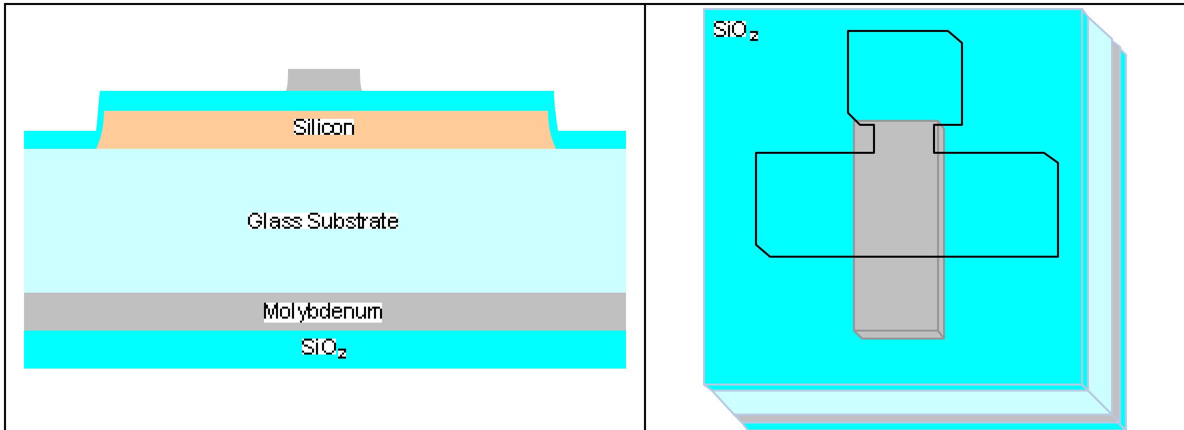


Figure 4.19: Photoresist strip

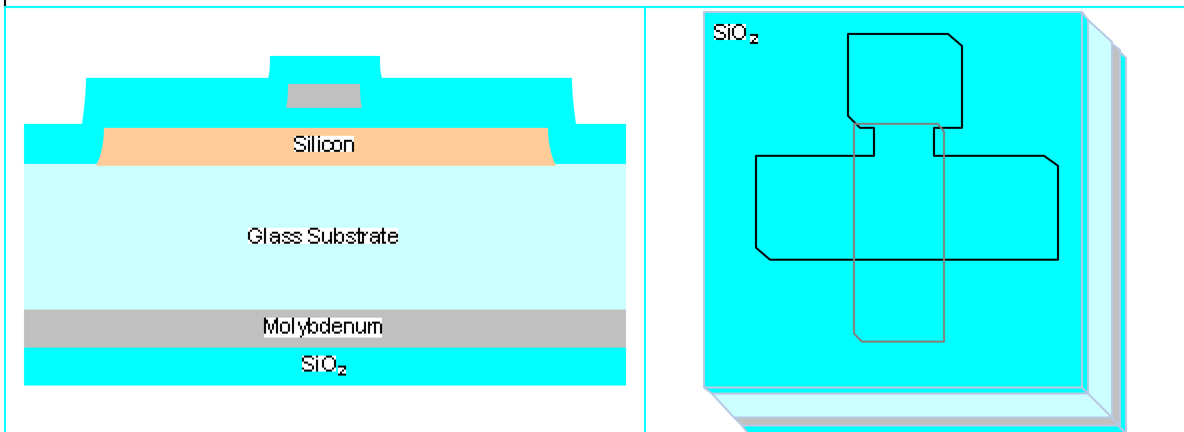


Figure 4.20: Protective oxide deposition

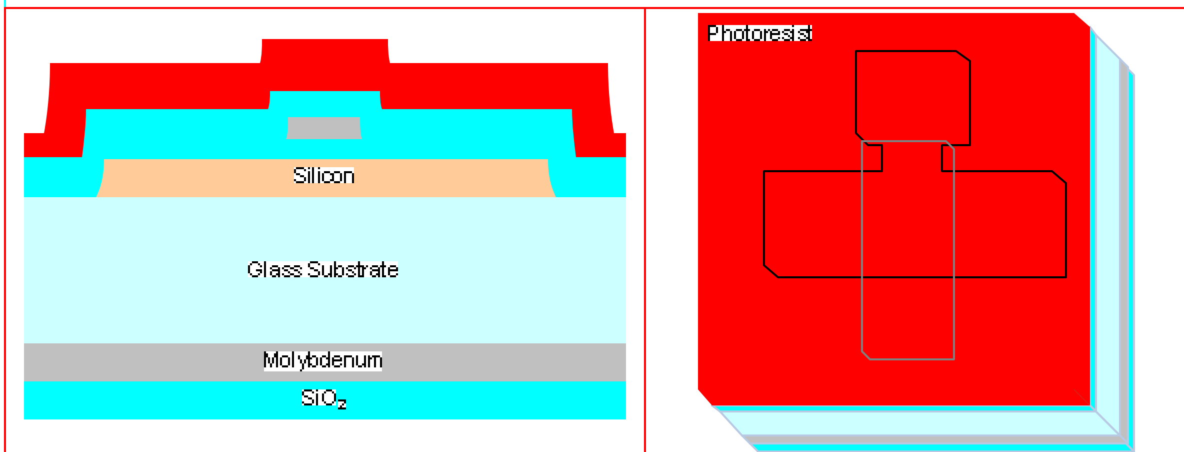


Figure 4.21: Photoresist coat

The N+ source and drain lithography defined the nfet device (see fig 4.22). Also, the N+ body contact for the pfet was pattered at this step.

The N+ implant is a single phosphorous implant (see fig. 4.23). A pre-amorphizing implant was not necessary as phosphorous is a large enough ion to self-amorphize. SRIM simulation software was used to model the projected range for phosphorous [16].

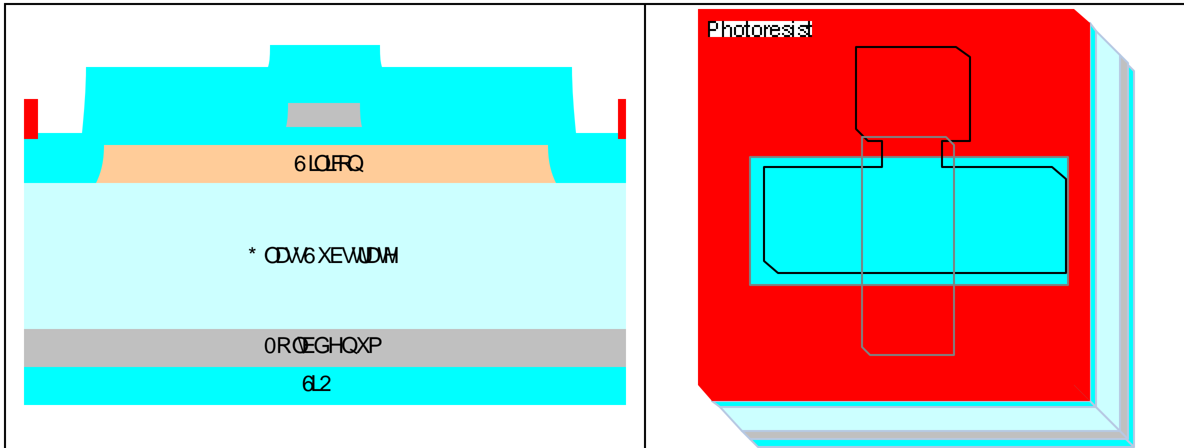


Figure 4.22: N+ source and drain lithography

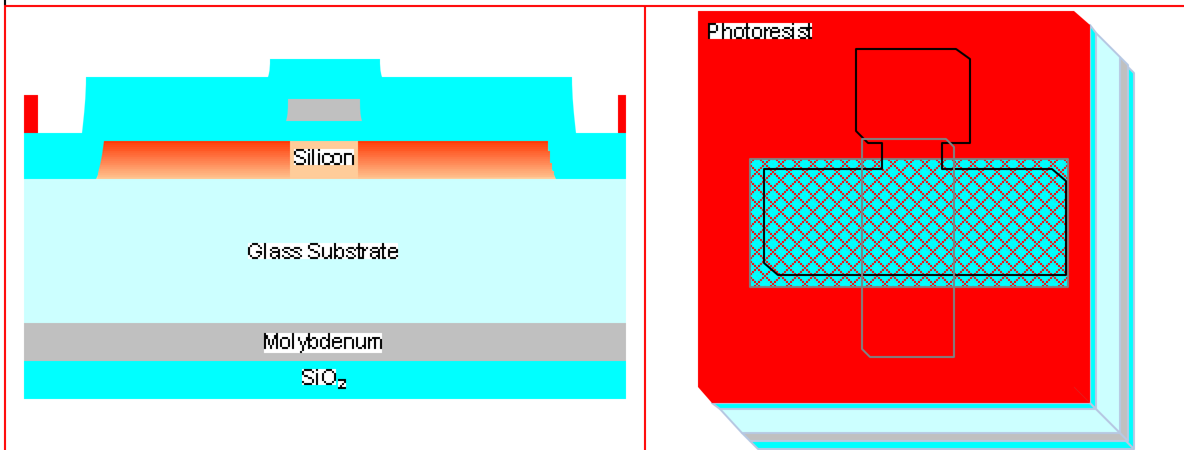


Figure 4.23: N+ source and drain implant

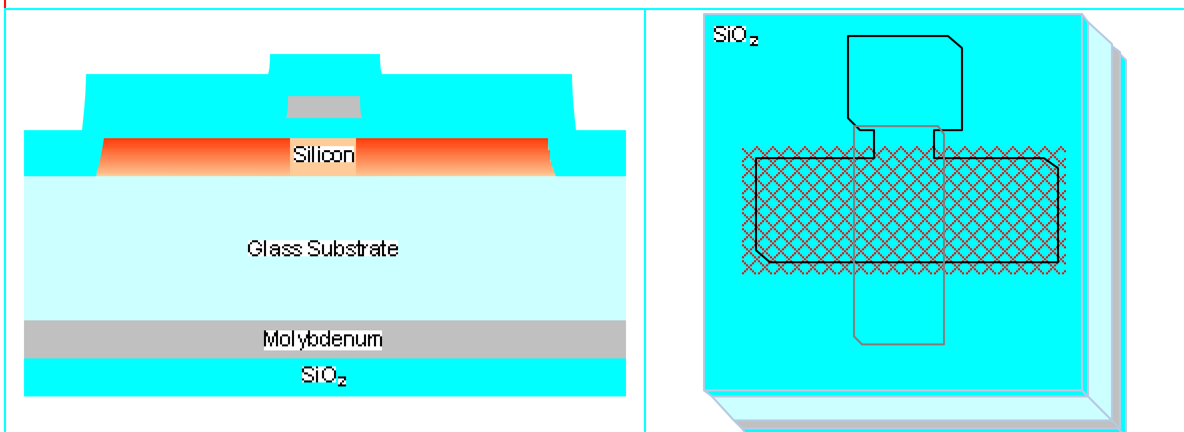


Figure 4.24: Photoresist strip

Figure 4.25 shows the next photoresist coat. The next step was the P+ source and drain lithography (see fig. 4.26). The P+ body contact for the nfet is also patterned at this step.

The P+ implant consisted of two implants, first the pre-amorphization implant using a fluorine species, followed by a p-type dopant implant of B_{11} (see fig. 4.27). As discussed in section 3, fluorine amorphizes the crystalline structure of the silicon. Upon annealing, the silicon film re-crystallizes, incorporating dopant ions into lattice. The amorphous structure helps to permit higher levels of dopant activation.

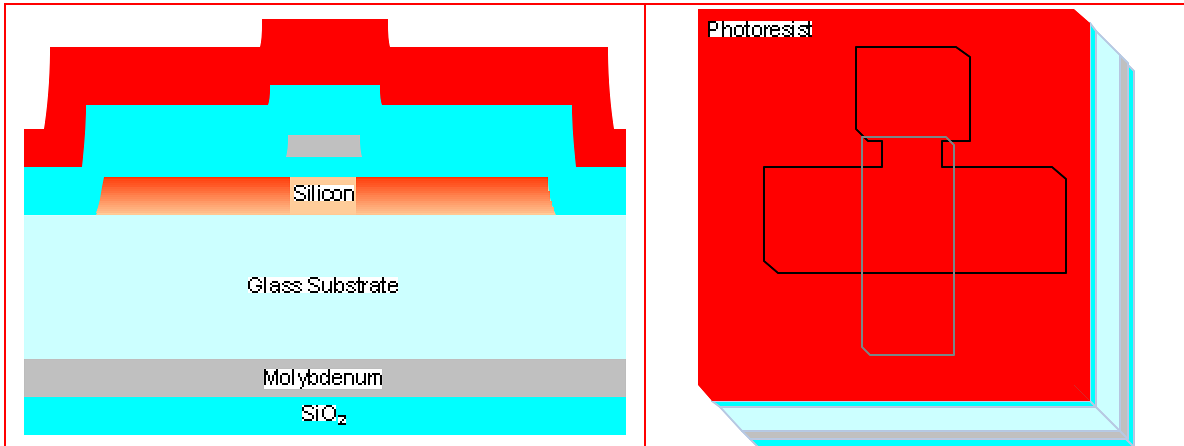


Figure 4.25: Photoresist coat

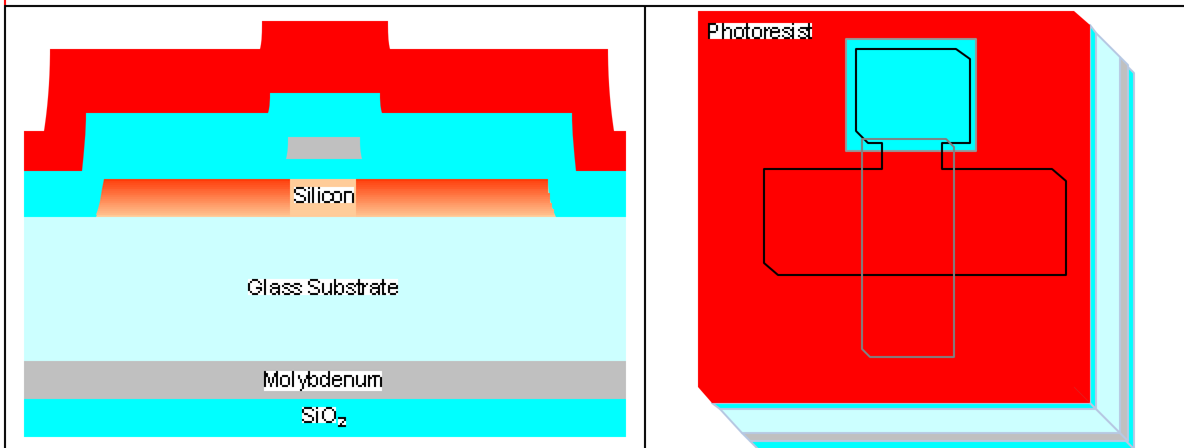


Figure 4.26: P+ source and drain lithography

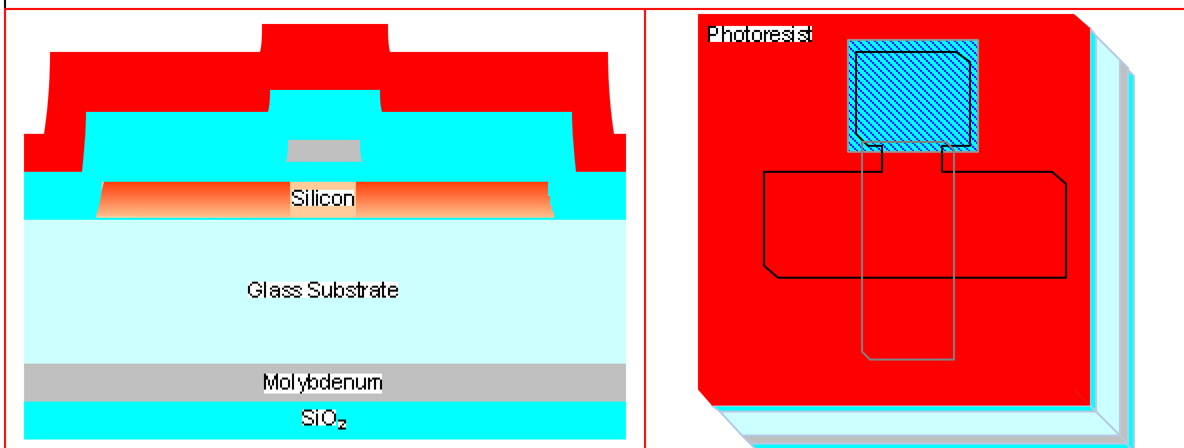


Figure 4.27: P+ source and drain implant

After implant, photoresist was removed and the wafers were cleaned in a heated piranha bath (see fig. 4.28). The wafers were annealed in a horizontal furnace at 600°C for 1 hour. Following anneal the additional PECVD TEOS oxide was deposited to make up the rest of the interlayer dielectric. This oxide isolates the devices from the first level metal (see fig. 4.29). Next, resist was coated (see fig. 4.30) for contact cut lithography.

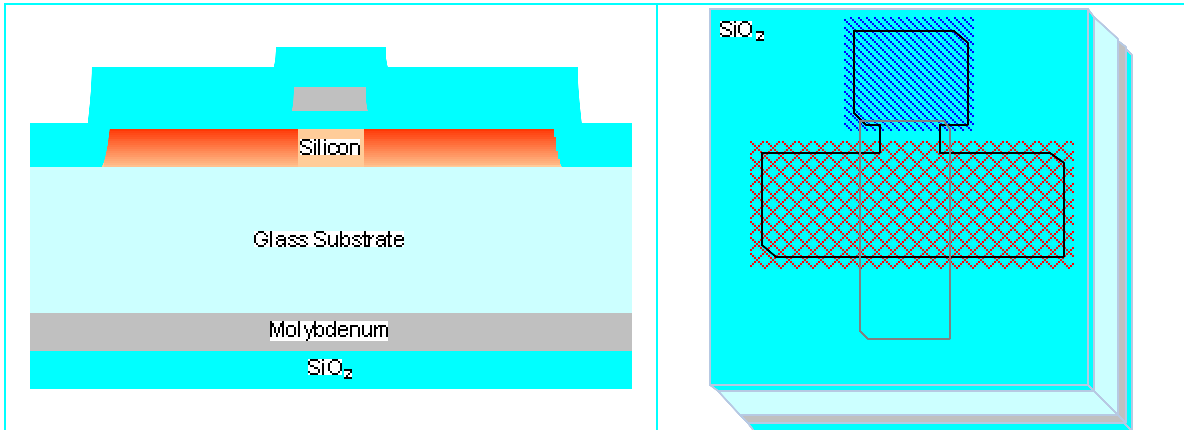


Figure 4.28: Resist strip and clean

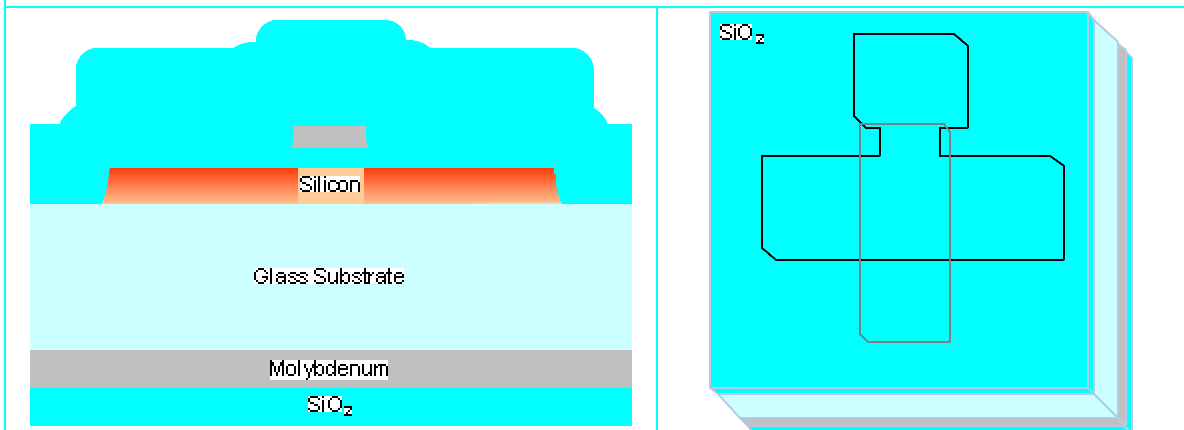


Figure 4.29: Inter-layer dielectric oxide deposition

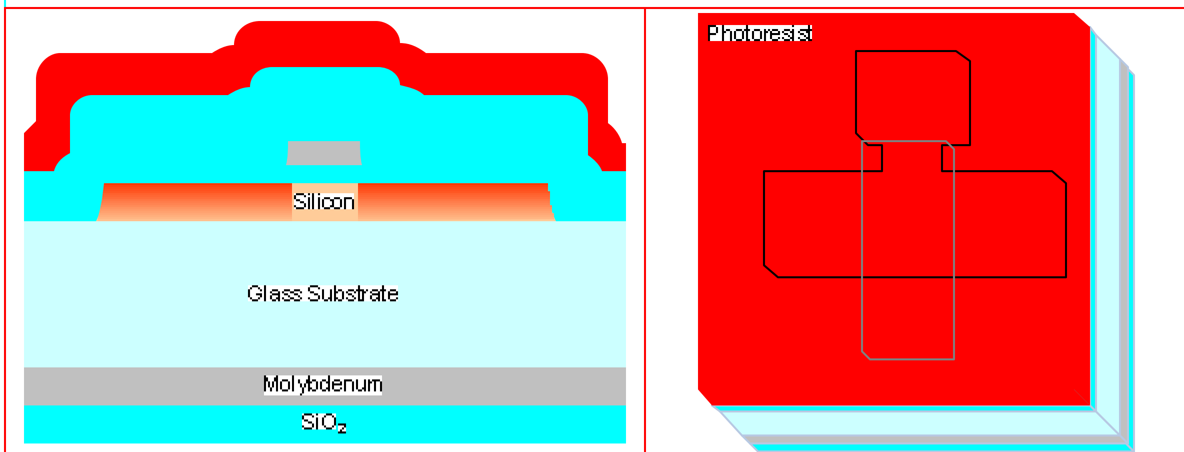


Figure 4.30: Photoresist coat

Contact cut lithography opened up windows in the resist for the contact cut etch (see fig. 4.31). The oxide was etched using Pad Etch (see fig. 4.32). Pad Etch is made up of acetic acid, ammonium fluoride and surfactants.

The resist was stripped using a heated solvent bath (see fig. 4.33). To ensure that all oxide had been removed in the contact regions, an additional dip in buffered oxide etch was done immediately before metal deposition.

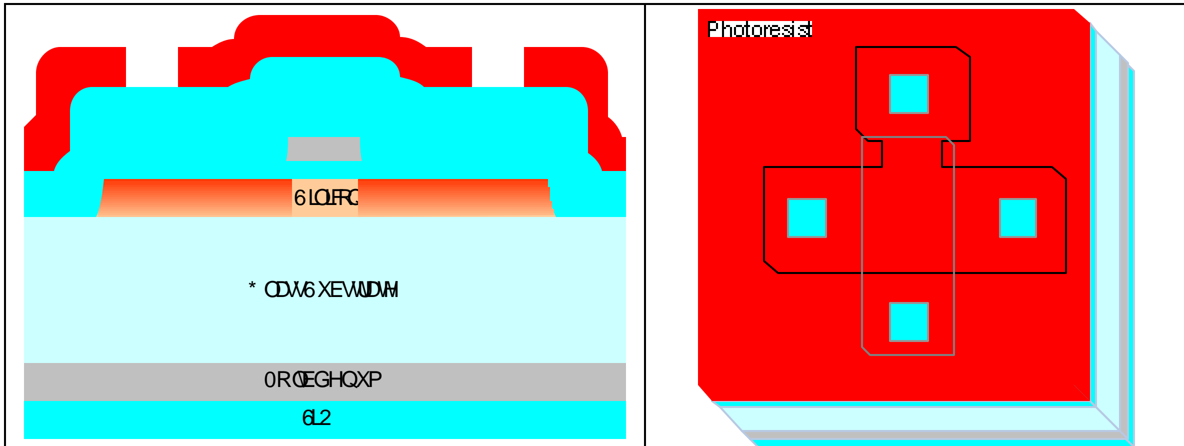


Figure 4.31: Contact cut lithography

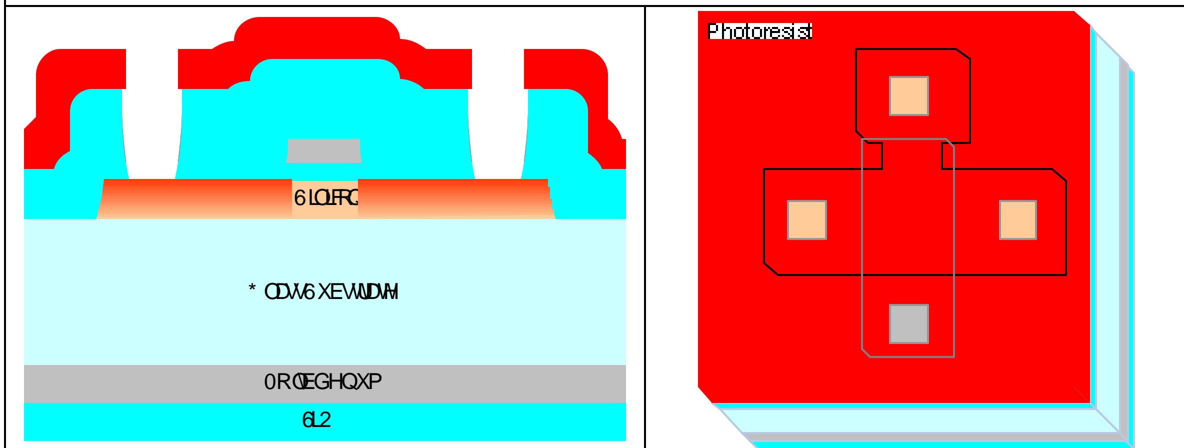


Figure 4.32: Contact cut etch

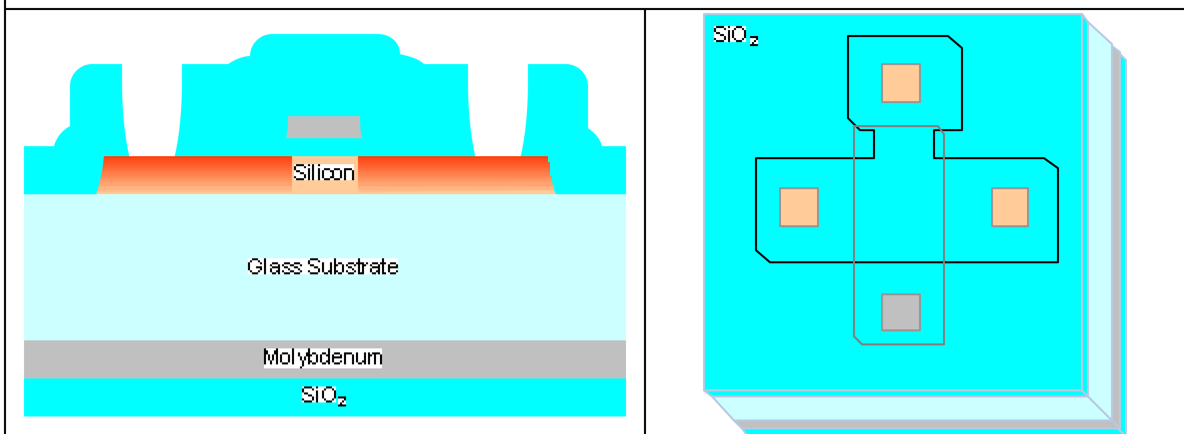


Figure 4.33: Resist strip

Approximately 7500? of aluminum was sputtered onto the wafers using an RF sputter tool (see fig. 4.34). Aluminum is the primary interconnect layer, and is also the primary metal for the bondpads.

Figure 4.35 shows the succeeding photoresist coat.

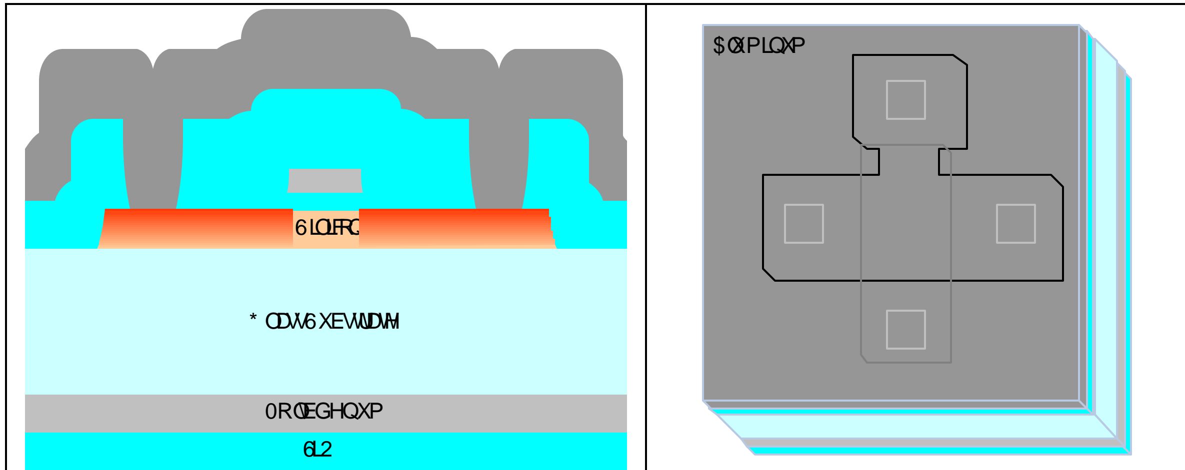


Figure 4.34: Aluminum metal deposition

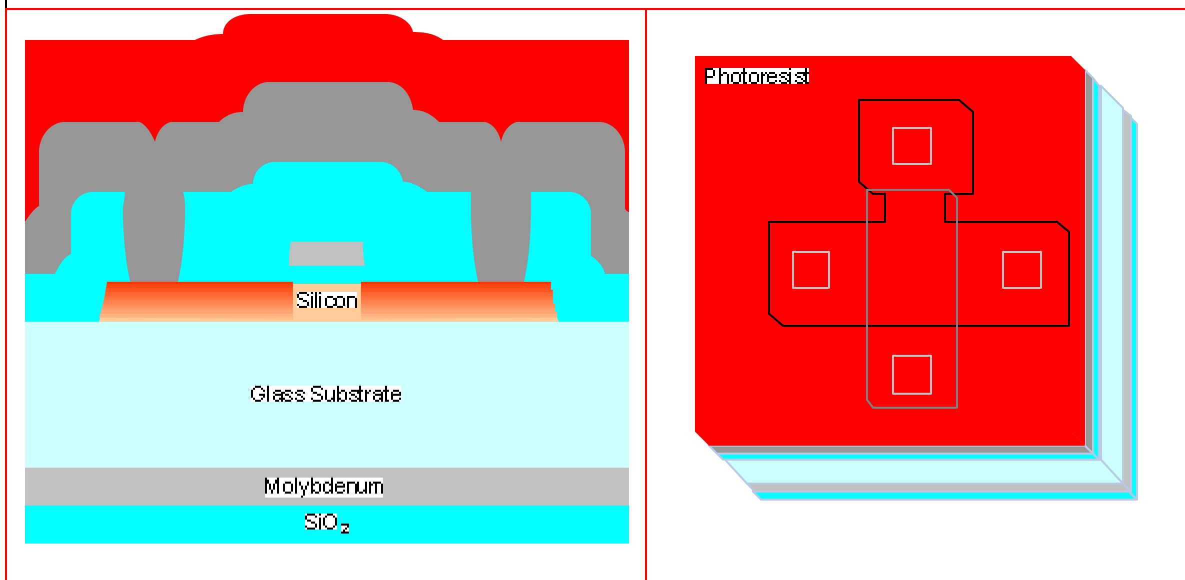


Figure 4.35: Resist coat

The aluminum was patterned with metal 1 lithography (see fig. 4.36). The aluminum was then etched with Transene Type A aluminum etch (phosphoric, nitric and acetic acid) (see fig. 4.37).

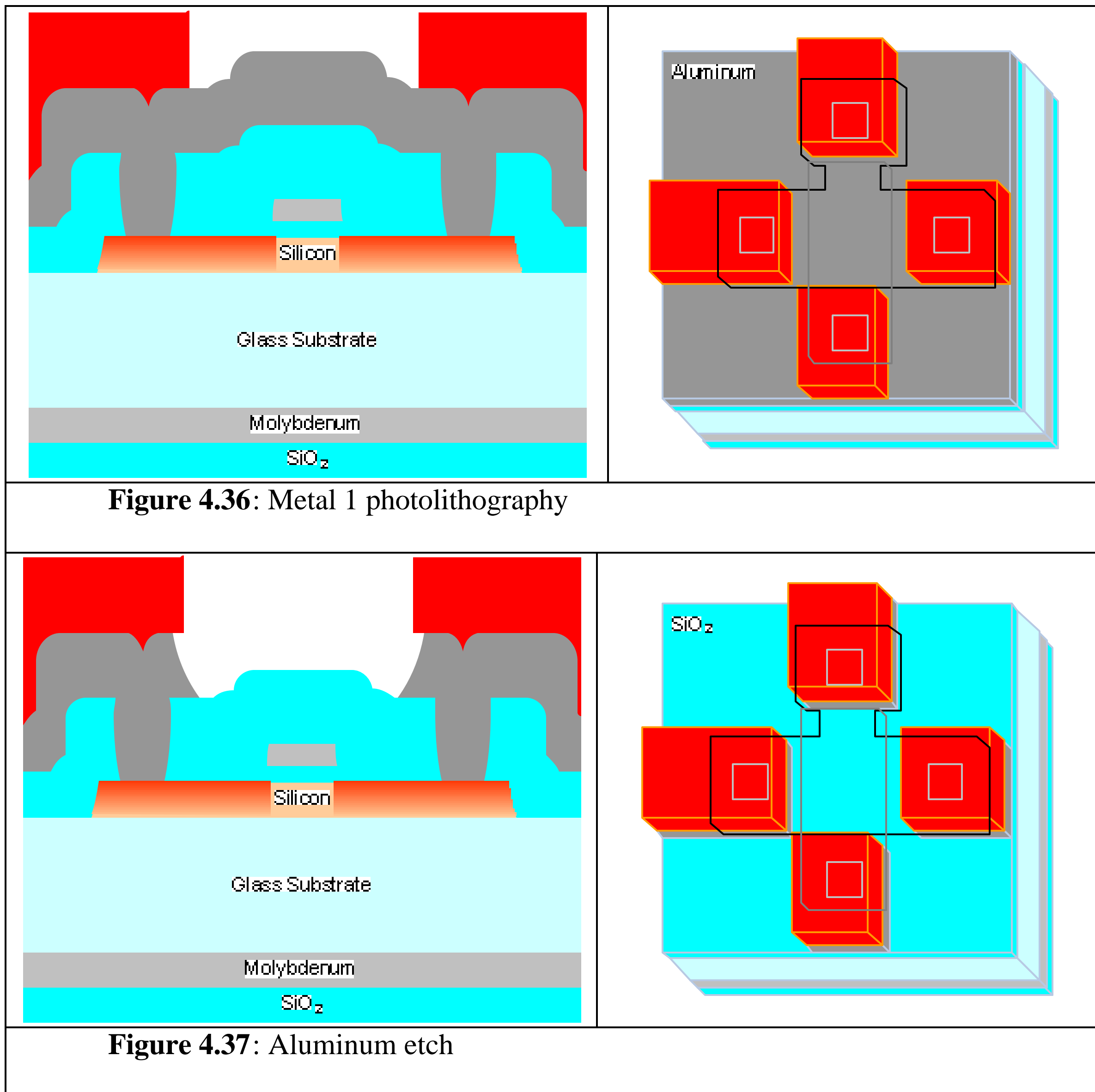


Figure 4.36: Metal 1 photolithography

Figure 4.37: Aluminum etch

Finally, resist was removed in heated solvents and then the wafers were sintered in forming gas H_2 N_2. Figure 4.38 shows the final device structure.

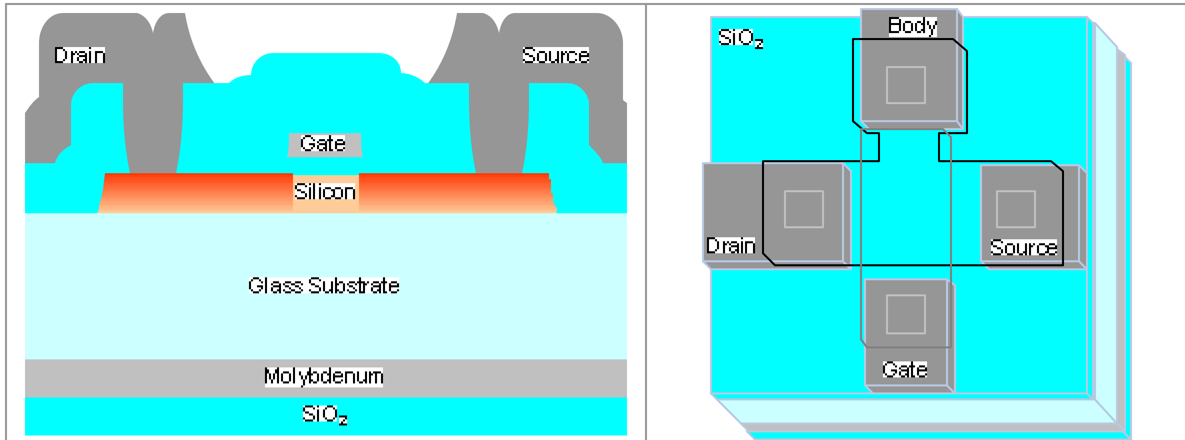


Figure 4.38: Final structure

4.5. TFT DEVICE DESIGN

The Silvaco licensed ATLAS simulation software package was used extensively to model device operation. Due to the uncertainty in backside interface charge levels on the starting substrates, a large range of simulations was conducted at various charge levels to understand what *could* happen. More importantly this capability allowed a device to be designed with a large tolerance, considering an unknown level of backside charge. In the remaining sections device design through simulation will be covered.

4.5.1. CHARGE ANALYSIS SIMULATION

In the design of the device, several key variables could be specified, including silicon thickness, oxide thickness, and substrate doping. Major variables that could not be certain (process dependent) were top and bottom interface charge levels. The quantity of charge was unknown for the top and bottom interface, increasing the complexity in designing functional devices. To design the device, simulation was used and all variables were adjusted to arrive at a final structure based on potential worst-case values for top and bottom charge. Table 4.4 shows initial simulation conditions.

N-channel Device	
Xsi:	1500?
Xox:	400?
Lmet:	0.72 µm
Nsub:	5E16 cm^{-3}
N+ S/D	1E20 cm^{-3}
Qtop:	1E11 cm^{-2}
Qbot:	8E11 cm^{-2}

Table 4.4: Conditions representing potential 'worst-case' levels of backside charge for device simulation.

The backside charge level of 8E11 cm^{-2} was chosen to promote a backside channel (undesirable). The simulated top charge level was set to represent possible interface charge associated with a deposited oxide. A silicon layer thickness of 1500? was used to explore a fully depleted device. Finally, a conservative 400? oxide was used to ensure conformal coverage of the mesa silicon. Note that the reported metallurgical channel length (Lmet) corresponds to structures used only for device simulation.

Simulation of the structure was conducted using Silvaco's ATLAS software [21,22]. An ID-VG sweep of the simulated structure is shown in figure 4.39.

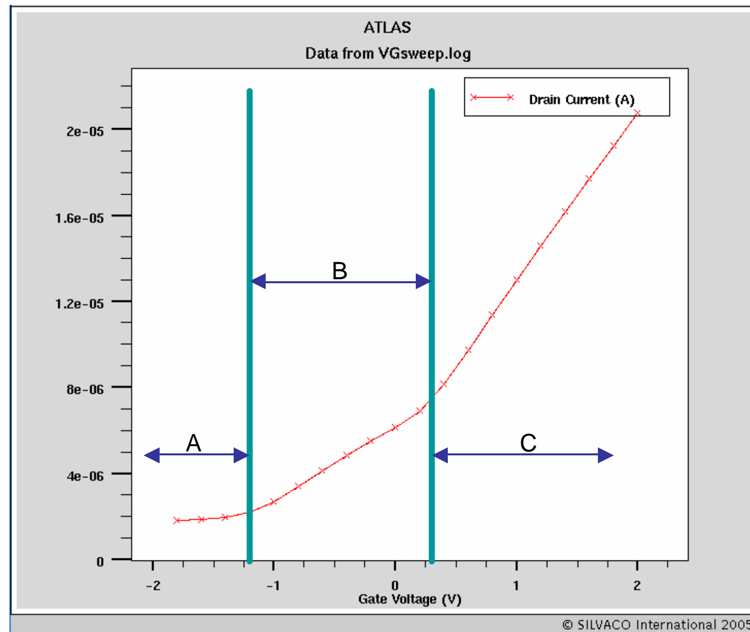


Figure 4.39: ID-VG sweep of initial NMOS simulation. Regions A, B, and C provide insight into how a large amount of backside charge could influence device behavior.

At the specified charge values, the ID-VG sweep revealed some interesting operating behavior. The sweep appears to be divided into three distinct regions. In region A there is a small inverted channel (electrons) on the bottom of the silicon layer due to the positive backside interface charge (8E11 cm^{-2}); this causes a conductive pathway. Figure 4.40 shows a cross section of the simulated structure and associated electron and hole concentrations at $V_G = -2$ V. Notice that the electron concentration in the bottom-channel region is slightly higher than the net doping concentration, indicating an inverted region on the bottom of the channel. Additionally, the hole concentration at the surface is slightly higher than the net doping concentration; this is the typical accumulation region. The accumulated holes prevent the electric field from influencing the bottom of the device. As a result, the electron channel on the bottom of the device

cannot be removed. Figure 4.40(a) shows a simplified ATLAS structure. Simulation nodes were used for the oxide and silicon regions only. The glass was modeled as SiO_2, and S/D regions were 'block' regions, with a Gaussian distribution for the dopant profile (1E20 cm^{-3} max concentration). The gate metal is simulated as a sheet with zero thickness above the channel and gate oxide. Likewise, the source and drain metal contacts are represented as a sheet in intimate contact with the source and drain silicon at y=0.

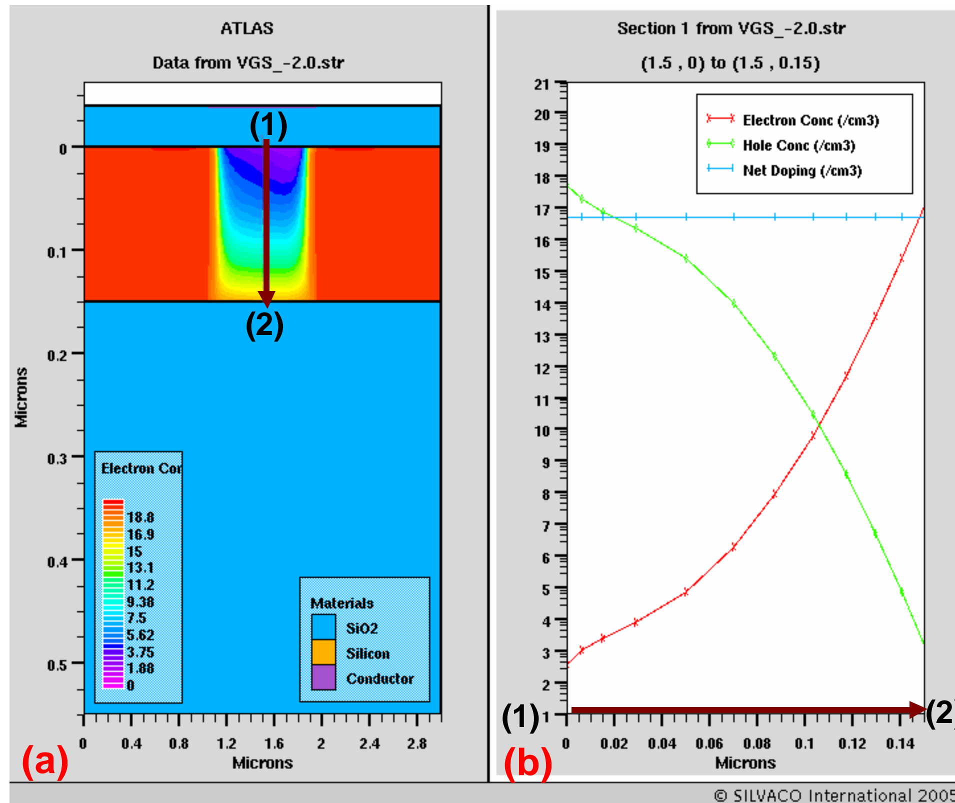


Figure 4.40:(a) Simulated structure at V_G = -2.0 volts, V_{DS} = 0.1 volts. (b) Hole and electron concentration plot from point 1 to point 2.

In region B of fig. 4.39, the bottom-channel is affected by the gate potential; the body is beginning to be depleted by the gate, and bottom channel current becomes a

function of gate potential. In this region the bottom channel is influenced by the gate through a series combination of gate capacitance and body capacitance. Figure 4.41 shows the electron hole concentrations of the structure at $V_G = -1.0$ V.

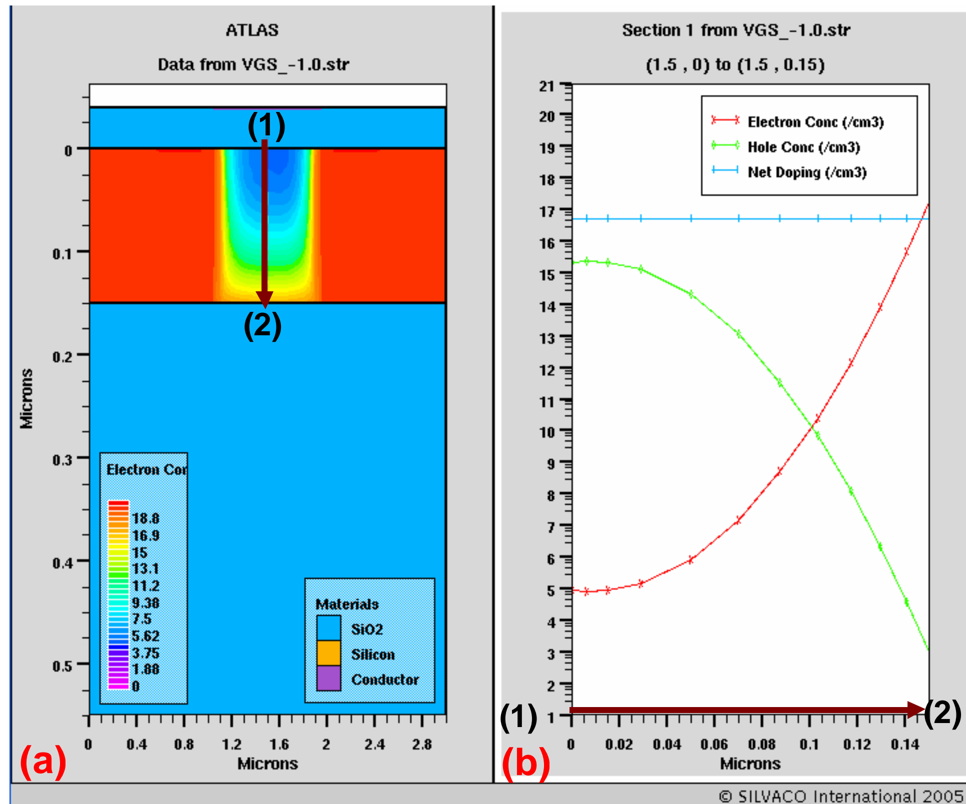


Figure 4.41: (a) Simulated structure at $V_G = -1.0$ volts, $V_{DS} = 0.1$ volts. (b) Hole and electron concentration plot from point 1 to point 2

In region C of figure 4.39, the top of the silicon layer inverts and an additional conduction path (primary topside channel) is formed. In this region of operation the backside channel is not influenced significantly by the gate. The ID-VG slope increases in region C because the topside channel is directly coupled to the gate. The slope increases as the capacitance increases during the transition from region B to region C. Figure 4.42 shows the structure at $V_G = 2.0$ V.

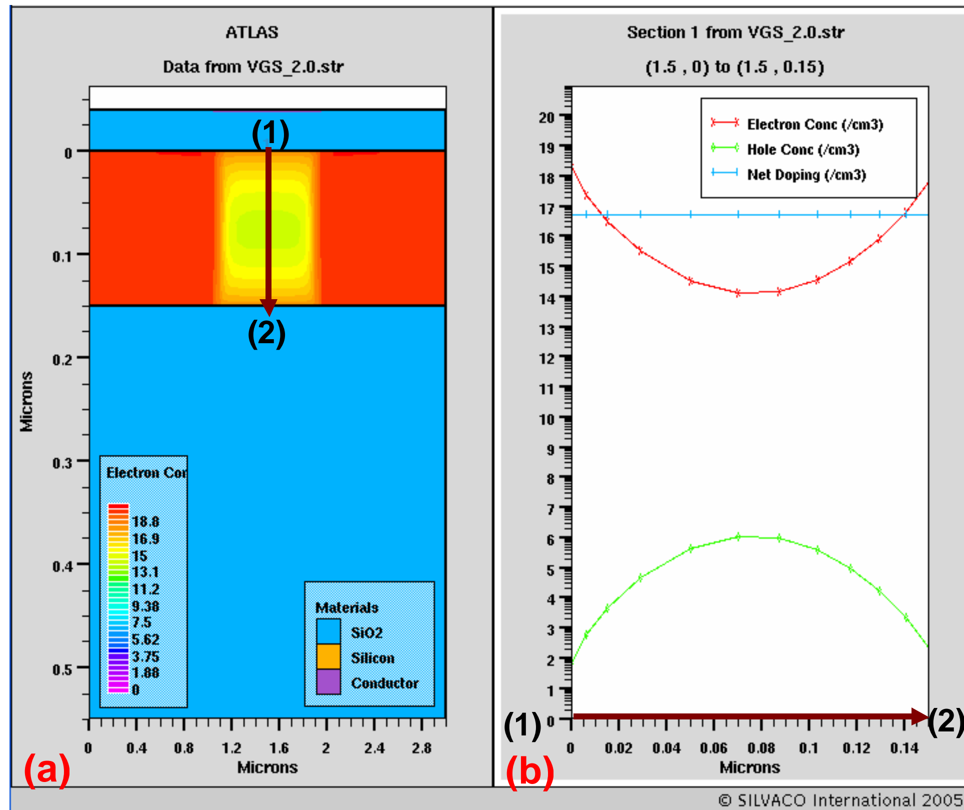


Figure 4.42: (a) Simulated structure at $V_G = 2.0$ V, $V_{DS} = 0.1$ V. (b) Hole and electron concentration plot from point 1 to point 2.

The bottom channel was a serious concern when designing the device. Since the backside charge levels were unknown, it was important to consider the worst case scenario.

4.5.2. Analysis of Initial Design Space with Simulation

A simulation matrix was created and analyzed to aid in understanding the primary and interaction effects of the following major design parameters: silicon thickness (Xsi), gate oxide thickness (Xox), substrate doping (Nsub), top interface charge (Qtop), and bottom interface charge (Qbot). The responses were threshold voltage (Vt) and off state current level (Ioff). A simplified ATLAS 'block' structure similar to figure 4.42 was used. The simulation matrix was conducted for NMOS and repeated for structures with

and without a simulated body contact. The body contact was simulated as a sheet contact under the channel at the silicon-glass interface. The drawback of simplifying the structure to two dimensions is that the body contact is not a very accurate representation of a physical device. It is not possible to have a metal contact directly under the channel. Additionally, a body contact located adjacent to the device (as in a real structure) will have a reduced influence on the channel region in comparison ideal backside contact. In the extreme case of a fully depleted channel, an adjacent body contact will not have any effect directly under the gate. A body-centered central composite designed experiment was setup and executed. Figures 4.43 and 4.44 show the prediction profiler, an analysis tool provided with JMP statistical software [23]. Off state current was represented on a log-scale due to the exponential behavior of leakage current.

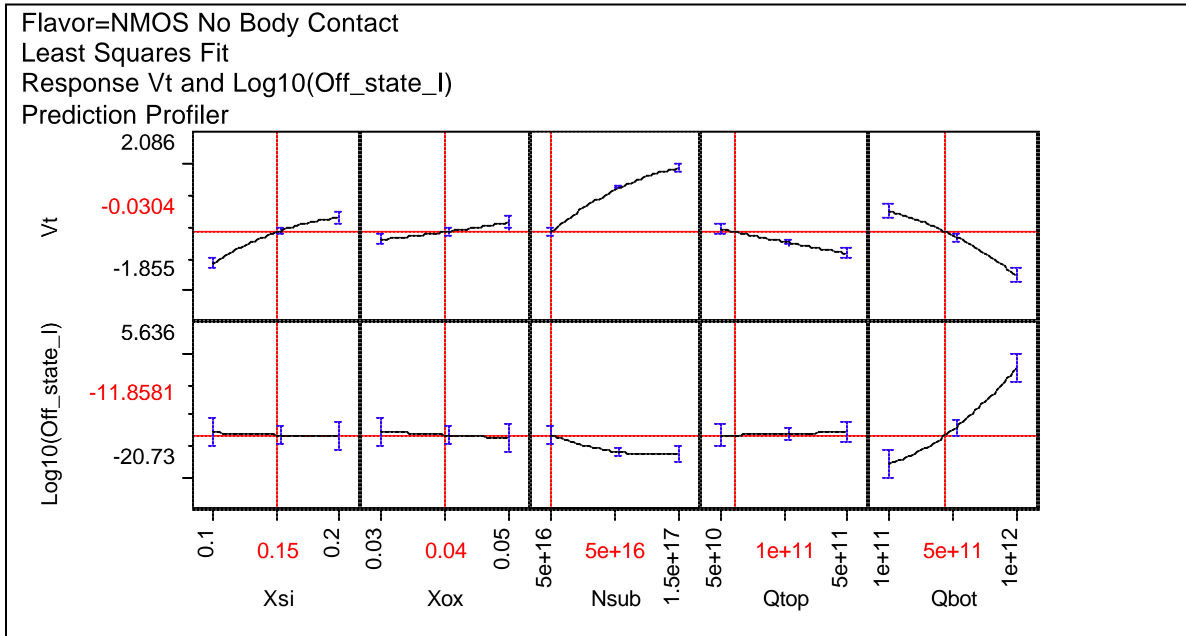


Figure 4.43: BCC analysis for NMOS simulation without a body contact. The plot displays leakage current and threshold voltage as a function of silicon thickness (Xsi in µm), gate oxide thickness (Xox in µm), substrate doping (Nsub in cm^{-3}), silicon/gate oxide interface charge (Qtop in cm^{2}), and silicon/glass interface charge (Qbot in cm^{2}).

The interaction effect between Nsub and Qbot is not apparent by looking at figure 4.43; if Nsub is raised, Qbot is observed to have less influence on leakage. Regardless, without a body contact it is apparent that bottom charge plays a large role in supporting leakage current. Figure 4.44 shows the same analysis with a backside body contact.

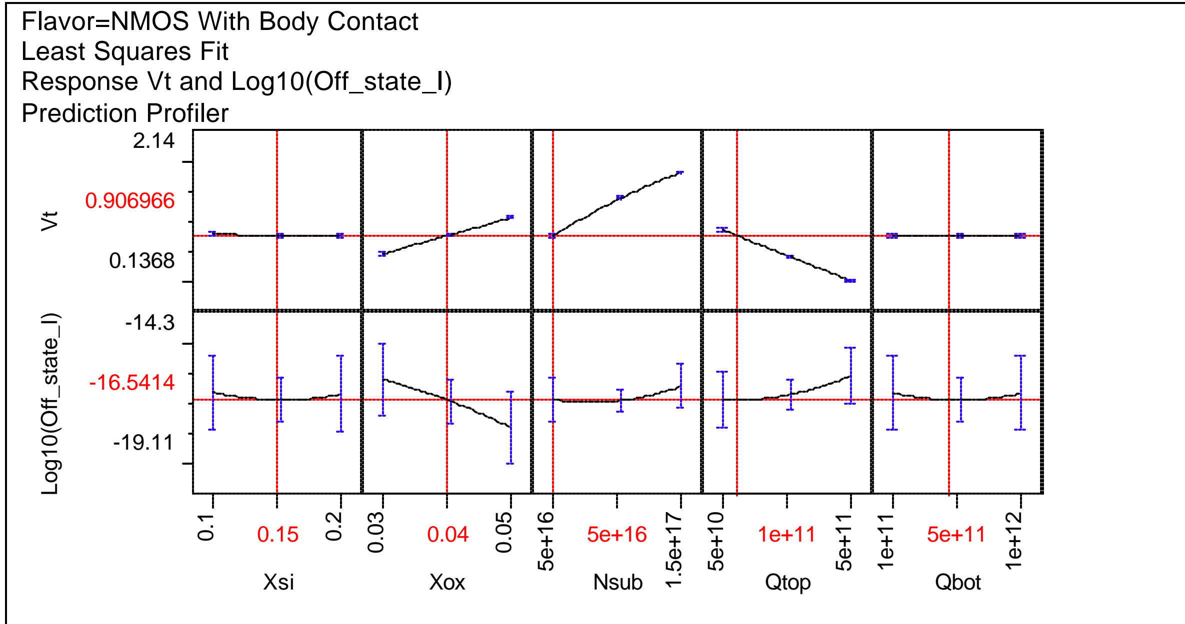


Figure 4.44: BCC analysis for NMOS simulation with a channel contact (body contact) directly below the channel region. Plot displays leakage current and threshold voltage as a function of silicon thickness (Xsi in μm), gate oxide thickness (Xox in μm), substrate doping (Nsub in cm^{-3}), silicon/gate oxide interface charge (Qtop in cm^2), and silicon/glass interface charge (Qbot in cm^2).

Bottom charge is almost completely eliminated by adding a body contact. This may not be the case with a 'real' body contact, especially in a thin body fully-depleted device. On a thicker body device (~300nm), with a fairly high substrate doping, an adjacent body contact would still enable a backside bias and effectively suppress the influence of backside charge.

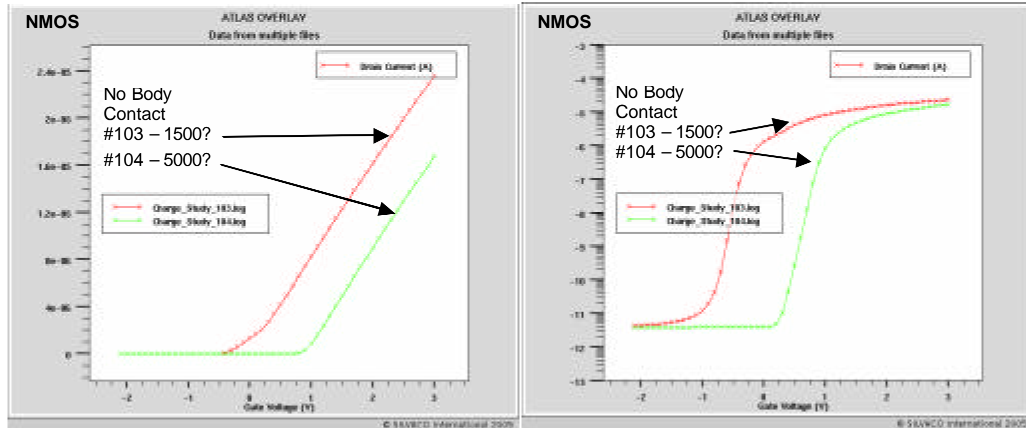
4.5.3. FINAL DESIGN REFINEMENT WITH SIMULATION

The initial simulations provided insight into the interactions of design input variables, however a more focused investigation was necessary to define the final design. Specific treatment combinations were analyzed, assuming values for top and bottom charge. Close attention was given to the on-state and off-state electrical characteristics. Table 4.5 shows the NMOS simulation conditions.

NMOS Device	
Xsi:	1500? vs 5000?
Xox:	400?
Lmet:	0.72 μm
Nsub:	5E16 cm^{-3}
Qtop:	1E11 cm^{-2}
Qbot:	5E11 cm^{-2}

Table 4.5: NMOS Simulation Conditions

The primary device of interest was the NFET. The NMOS device was designed to be tolerant to high levels of backside charge. A thick body, with high p-type doping would reduce the influence of a positive backside charge. NMOS electrical simulation results are shown in figure 4.46 and a view of the electron and hole concentrations at three key bias conditions are shown in figure 4.47.



(a) (b)

Figure 4.45: Simulated NMOS characteristics without a body contact. Silicon thickness has a large effect on device characteristics

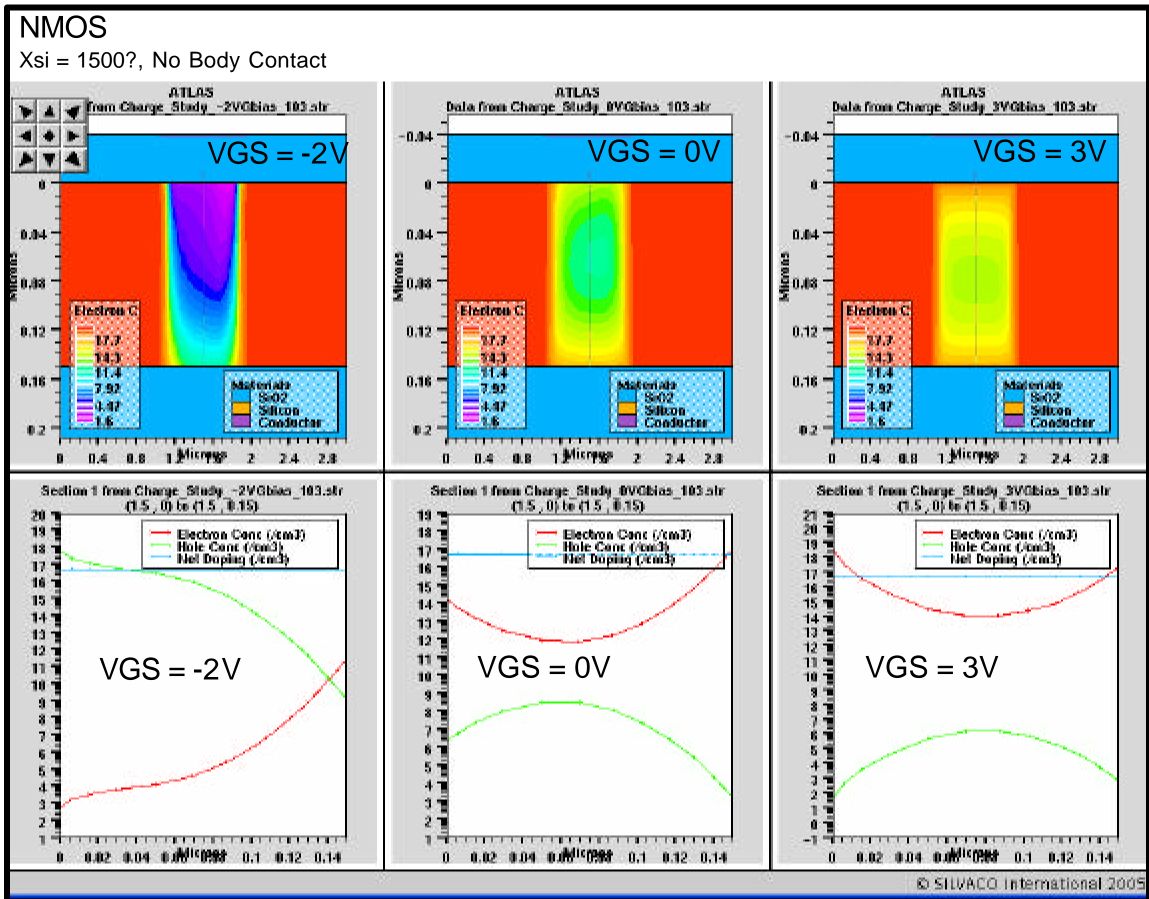


Figure 4.46: Simulated NMOS device cross section that displays electron and hole concentration at a gate bias of -2, 0, and 3 volts. The silicon thickness is 1500. Note that at -2 volts there is no channel formed, and the device is 'off'.

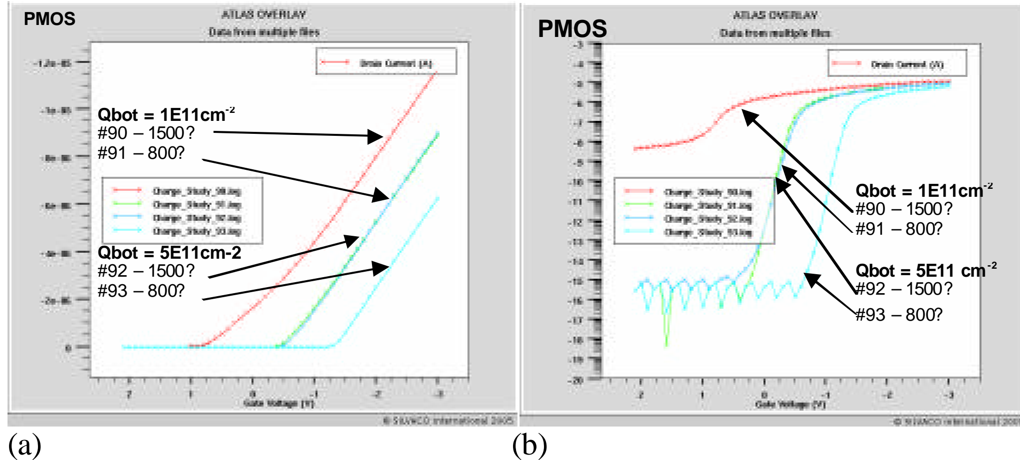
A PMOS device was also investigated to determine if CMOS would be feasible for any doping/charge levels. A PMOS device designed with a p-type body must operate as a buried-channel device where the body region is hole-depleted in the off-state. A thin silicon body along with positive backside charge supports a p-type body that is fully-depleted of hole carriers. Note that a body contact is not an option for a buried-channel PMOS device, where all device regions are fabricated in a common p-type layer. Table 4.6 shows the input parameters for the PMOS simulation.

PMOS Device	
Xsi:	1500? vs 800?
Xox:	400?
Lmet:	0.72 µm
Nsub:	5E16 cm^{-3} (p-type)
Qtop:	1E11 cm^{-2}
Qbot:	5E11 cm^{-2} vs. 1E11 cm^{-2}

Table 4.6: PMOS simulation conditions

For the PMOS device to act as a transistor, and not as a resistor, it is necessary to deplete the majority carrier (holes) in the channel region while in the off state. In order of effectiveness the three ways to accomplish this are choice of an appropriate gate metal workfunction, decreased silicon layer thickness, and a high level of backside charge. A high level of backside charge (positive charge) for the PMOS device will promote hole depletion. In the initial design phase it was necessary to make a few assumptions about the starting material, to create a starting design. In this simulation two backside charge values were investigated. In figure 4.48 it is evident that a thin body PFET with a high level of backside charge provides the best characteristics. Figure 4.49 show that the hole population is depleted in the off state. The worst possible condition for the PFET is a thicker body combined with low backside charge. However, if the Corning substrates

where found to have low levels of backside charge, a PMOS device would still be possible by lowering the doping level and/or reducing the silicon thickness.



(a) (b)

Figure 4.47: Simulated PMOS characteristics without a body contact

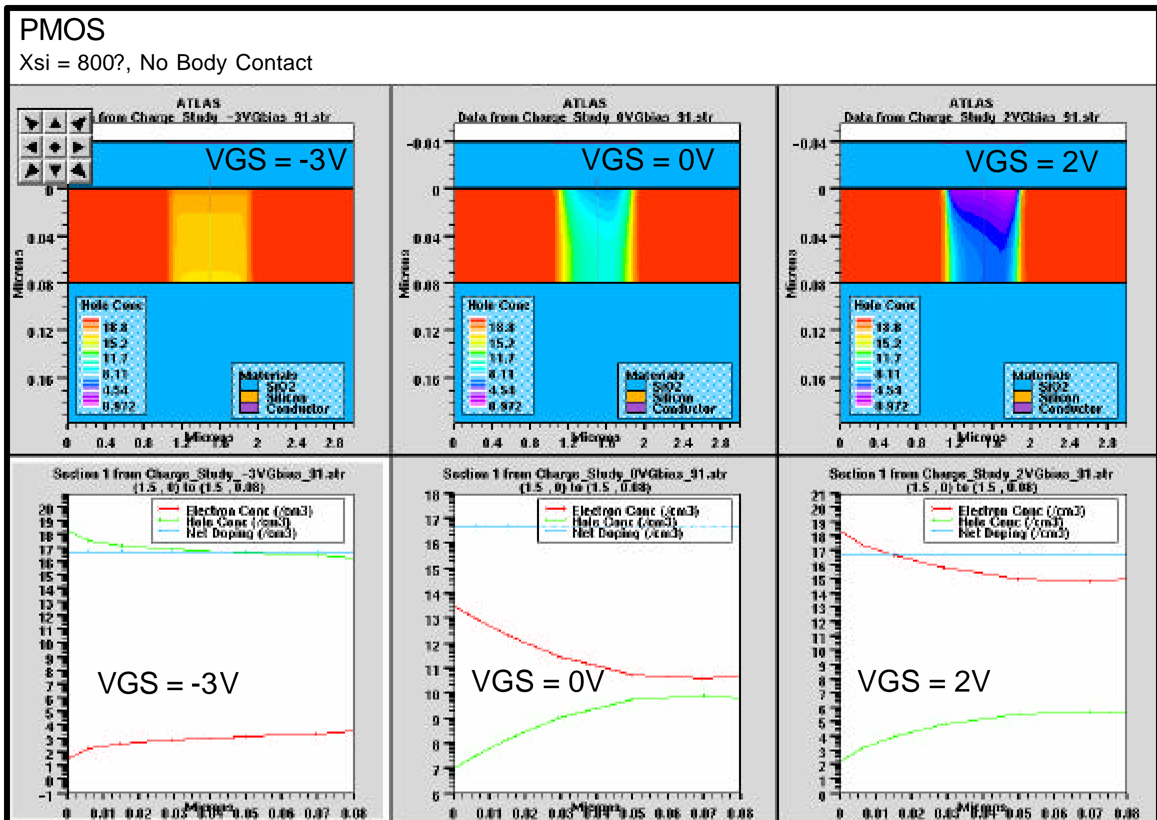


Figure 4.48: A Simulated PMOS cross section showing electron and hole concentrations at three different gate bias (-3V, 0V, 2V). With 1E11 cm^{-2} backside charge and 800? of silicon allow this pseudo PFET to function as a transistor and not a resistor.

Simulation shows that the p-channel PFET works only with moderate substrate doping, thin silicon thickness, and the assistance of bottom charge. The conditions that make the PFET device operate are directly opposite of those to optimize the NFET. Since it was desirable to have both NMOS and PMOS operate with the same substrate doping and type, without wells, it was necessary to slightly compromise device performance for each device. With an estimated backside charge of 5E11 cm^{-2} the simulation parameters that provided optimal device characteristics for both devices were found to be 400? oxide, 1500? silicon body thickness, and a global p-type doping of 5E16 cm^{-2}. While the actual values of interface charge and process results were not yet established, the device simulation results provided insight into several possible scenarios prior to initiating device fabrication.

4.6. CONCLUDING REMARKS

In the preceding sections, a low-temperature CMOS process was designed. The fabrication process sequence was described and processing details unique to the SiOG technology were identified. Simulation was used to determine initial values for process design parameters, and to explore the influence of parameters that could not be controlled. A mask set that would be useful for several generations of SiOG TFT research was designed, and engineered silicon was sent to Corning for substrate fabrication.

CHAPTER 5

TFT DEVICE CHARACTERIZATION AND MODELING

5.1 INTRODUCTION

The analysis of electrical characteristics of fabricated TFTs will be presented in this chapter. There were three SiOG process runs (or lots) that will be discussed; L1A, L1B and L2A. The lot number corresponds to the batch of SiOG material prepared by Corning. The silicon layer thickness and doping concentration were each fixed at two levels, and the thickness of the LTO gate dielectric was fixed at 500Å. Table 5.1 provides the level settings for the lots processed. L1A and L1B were fabricated on SiOG wafers previously prepared by Corning, which used relatively lightly-doped ($\rho \sim 10\Omega$-cm) p-type bulk-silicon wafers as the silicon layer source. L2A was fabricated using substrates with an implanted p-well profile as the silicon source wafer, which provided a higher level of control on the dopant concentration compared to a vendor-supplied starting substrate.

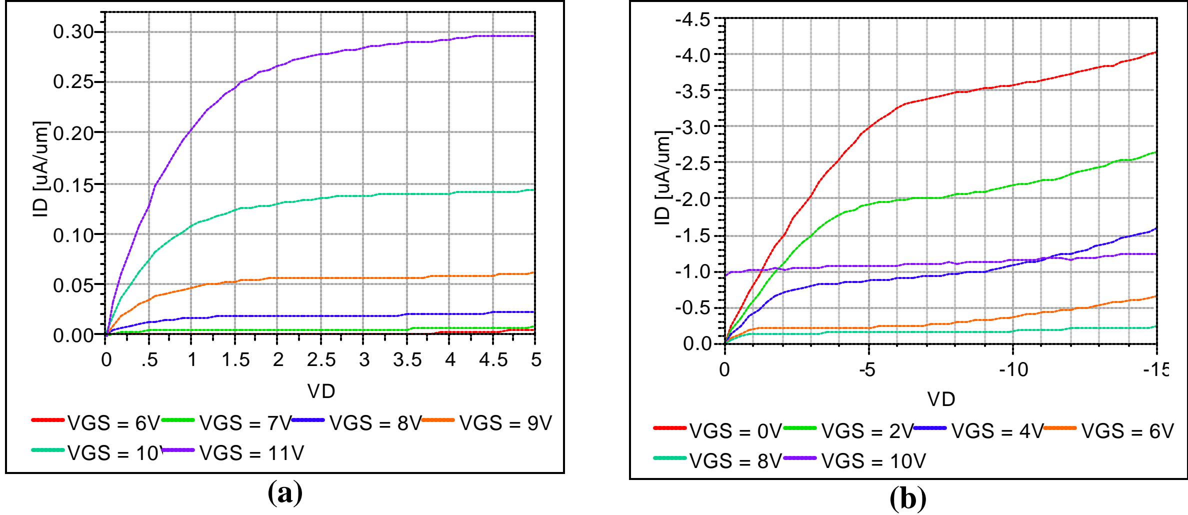
Lot #	Xsi (nm)	Xox (?)	Nsub (cm^{-3})
L1A	300	500	5.00E+14
L1B	150, 300	500	5.00E+14
L2A	150, 350	500	5.00E+16

Table 5.1: SiOG TFT input parameter level settings

The first process run (L1A) was used as an instrument to find and fix fundamental process issues, as well as an initial verification of the LT-CMOS process on glass substrates. There were various processing issues (i.e. rework cycles, alignment overlay offset) that had an impact on the device operation, and the electrical results are not a true representation of the designed process. Thus, the electrical results will not be discussed beyond the initial demonstration of operational transistors. The two subsequent process runs (L1B and L2A) will be discussed at length, along with the investigation that revealed the mechanisms that influenced device behavior. Device modeling and simulation has been used extensively in developing an operational model of the NMOS and PMOS transistors.

5.2 FIRST DEMONSTRATION OF TRANSISTORS ON GLASS

There were a number of process issues surrounding the fabrication of L1A, which was not unexpected since this was the first SiOG lot to experience the LT-CMOS process. Among these were alignment overlay error that exceeded the design tolerance, and a low-quality LTO dielectric with a relatively low breakdown field strength (~ 2 MV/cm). Nevertheless, the process yielded working NMOS and PMOS devices, with typical "family-of-curves" characteristics shown in figure 5.1.



(a) **(b)**

Figure 5.1: Family-of-Curves characteristics for typical NMOS (a) and PMOS (b) TFTs fabricated in L1A, with a silicon layer thickness X_{Si} ~ 300nm. The channel dimensions were L = 24µm & W = 6µm for the NMOS device and L = 24µm & W = 12µm for the PMOS device. Note that the NMOS device tested utilized a grounded body contact to suppress floating-body effects. Gate bias conditions are indicated, showing that the NMOS TFT is enhancement mode and the PMOS TFT is depletion mode. Also note that the V_{GS} = 10V condition on the PFET resulted in dielectric failure.

The device of primary interest in L1A was the NMOS TFT. The operating characteristics were difficult to predict due to the lightly-doped silicon layer and the uncertainty of interface and bulk oxide charge which could alter the turn-on and turn-off characteristics significantly. It was anticipated that due to positive charge centers, the NMOS TFTs may behave as depletion-mode devices. In contrast, the device clearly turned out as an enhancement-mode transistor with a threshold voltage V_{Tn} ~ 6V, which is much higher than the doping concentration alone would support; the ideal V_{Tn} for 500Å oxide, molybdenum gate workfunction and a substrate doping of 5E14cm^{-3} is ~ +0.3V. At this point it was speculated that this large positive shift in the NFET threshold was due to a source of negative charge; either at the LTO/silicon interface or bulk charge in the LTO dielectric. However, charge centers at the silicon/glass interface were not considered as a likely candidate for the NMOS V_T shift due to an established body contact.

The PMOS transistor demonstrated characteristics that were mostly consistent with the NMOS behavior. The PMOS TFTs were designed to operate as depletion-mode buried-channel devices, and in fact due to the silicon layer type (p-type boron-doped) and thickness (300nm) they were not expected to have reasonable turn-off characteristics. This was further enhanced by the same mechanism that influenced the NMOS operation; although the PMOS TFTs exhibited transistor behavior, a gate bias of +8V was not able to completely turn off the device. A further increase to +10V caused a destructive failure of the LTO gate dielectric, as shown in figure 5.1(b).

A noted difference between the NMOS and PMOS transistors was the current drive available on equal length devices within the given bias range; the PMOS transistors appeared to be much less resistive than the NMOS transistors. This was mainly attributed to the effective (V_{GS}-V_T) values, which are actually much higher for the depletion-mode PFET, even at $V_{GS} = 0$. The NMOS and PMOS threshold voltages observed indicated a high level of negative charge influencing the carrier concentrations; located at either the top region (oxide/silicon interface) or the bottom region (silicon/glass interface) of the silicon layer.

Current drive is also related to the channel mobility; the L1A SiOG devices demonstrated a field-effect electron and hole mobility of $\mu_n \sim 60cm^2/V\text{-sec}$ and $\mu_p \sim 70cm^2/V\text{-sec}$, respectively. Although significantly less than typical bulk silicon values, the results showing that the hole mobility is slightly higher than the electron mobility is not unreasonable considering that the hole carriers in the PMOS device are expected to have less of an interaction with the surface (silicon-oxide interface) in comparison to

electrons in the surface-channel NMOS transistor. Details of channel mobility and extraction methods will be discussed in section 5.3.

The fact that L1A exhibited working transistor characteristics was quite remarkable, considering the process issues that were experienced. These issues also influenced the bulk-silicon control wafer (C2), however C2 was successful in yielding bulk-silicon NMOS transistors with characteristics that were closer to those expected, as shown in figure 5.2.

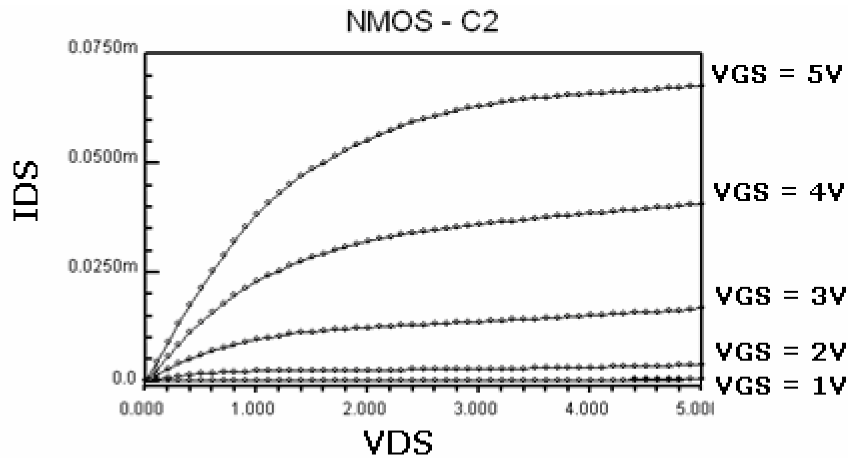


Figure 5.2: L1A bulk-Si control wafer (C2) NMOS device, L = 24μm & W = 24μm. The threshold voltage V_{Tn} ~ 1.5V.

The bulk-silicon NMOS transistors did not exhibit the level of interface charge that was demonstrated by the SiOG devices, however the threshold voltage of ~ +1.5V reflects a fairly significant level of *negative* interface charge states (Nss ~ 5E11cm^{-2}). This indicated that independent from the starting substrate quality, there were needed improvements in the LT-CMOS process; specifically targeting the oxide deposition and annealing processes.

5.3 TFT PARAMETER EXTRACTION

Due to the non-ideal device characteristics often observed throughout this investigation, it was essential to choose appropriate operational parameters and develop methods of parameter extraction that would provide a consistent and meaningful assessment of the device performance. First-order parameters that were used to describe the device operation were the threshold voltage (V_T), linear-mode transconductance (g_m), and the extracted carrier mobility (μ_n & μ_p) for on-state characteristics, as well as the sub-threshold swing (*SS* in mV/dec) and minimum current level (I_{min}) for off-state characteristics.

5.3.1. ON-STATE CHARACTERIZATION

A single threshold voltage value was not adequate to define the characteristics of many of the SiOG devices measured in this study. Many of the devices had a two step turn on, as shown in figure 5.3, that required separation of the two distinct operating modes. A single V_T does not adequately represent the device operation; it is necessary to consider the entire operating range. Theories on the physics behind the two modes will be presented in subsequent sections.

Although the devices exhibited non-ideal threshold characteristics, the electron and hole field-effect mobilities were extracted from the linear-mode transconductance using equation 5.1, derived from the linear-mode current equation when V_{DS} is small.

$$\boldsymbol{m} = \frac{g_{m(\max)} \cdot Length}{Width \cdot V_{DS} \cdot Cox}$$, where $g_{m(max)}$ is the maximum transconductance

Equation 5.1

Although the lateral field is low, this method of mobility extraction results in an *effective* field-effect mobility which is influenced to some extent by both normal-field degradation and source/drain series resistance. The amount of normal-field degradation depends upon the gate bias condition around the $g_{m(max)}$ point, which can vary depending on the turn-on characteristic. The carrier mobility will also be significantly influenced by other scattering mechanisms at the silicon surface, such as interface charge or surface defects. A relative comparison of this effective mobility provides a metric for evaluation purposes.

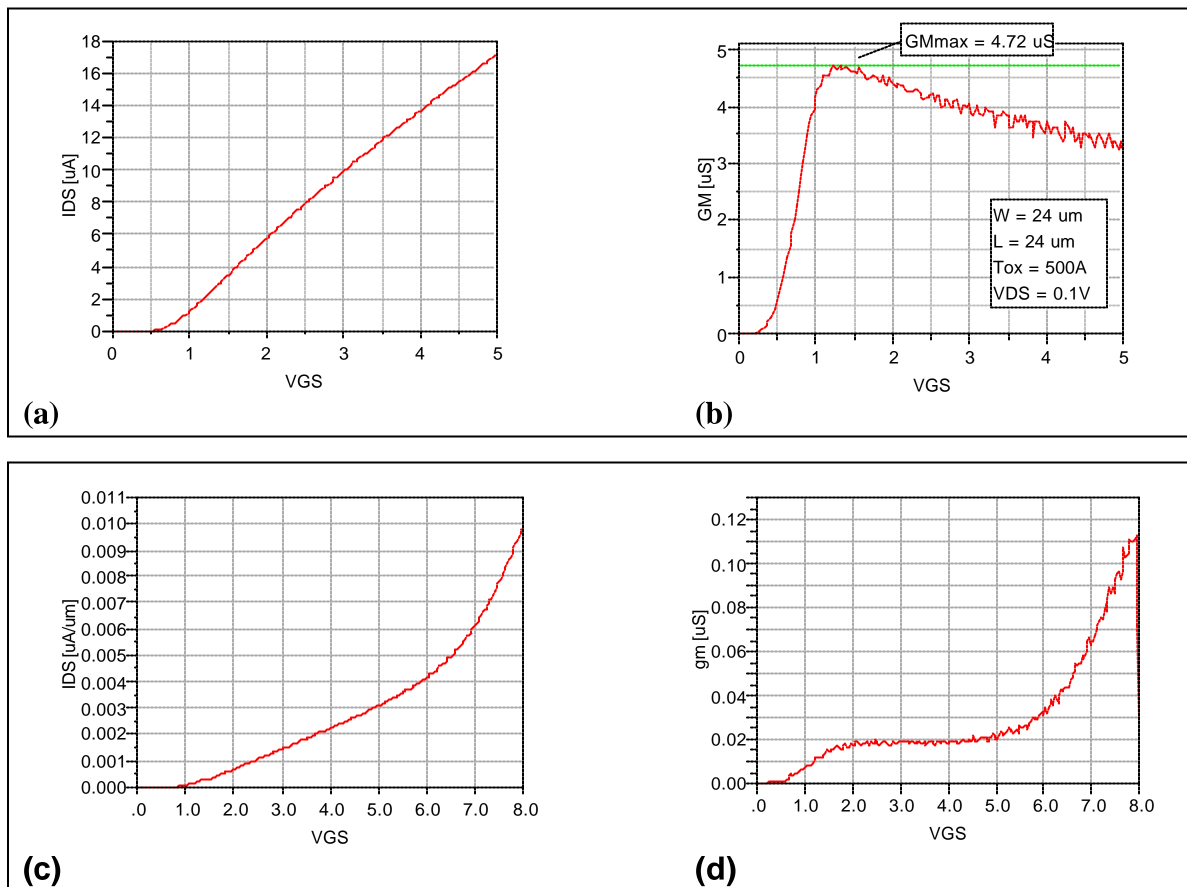


Figure 5.3: Example of linear mode mobility calculation using an I_{DS}-V_{GS} sweep of the transistor (a). The mobility of this bulk silicon device was found to be 683 cm^2/V-sec (b). An example of a 'two-stage' V_T is shown in figure (c), with the associated transconductance shown in (d).

5.3.2. OFF-STATE CHARACTERIZATION

Subthreshold or off-state characteristics of the SiOG transistors also required 'full-sweep' characterization. As shown in figure 5.4 the 'two-step' phenomena is also observed in the typical subthreshold characterization methods. Two sub-threshold numbers can be reported for regions below the *two* threshold voltages. The minimum current reported (I_{min}) was an effective measurement of leakage, that is independent of threshold voltage.

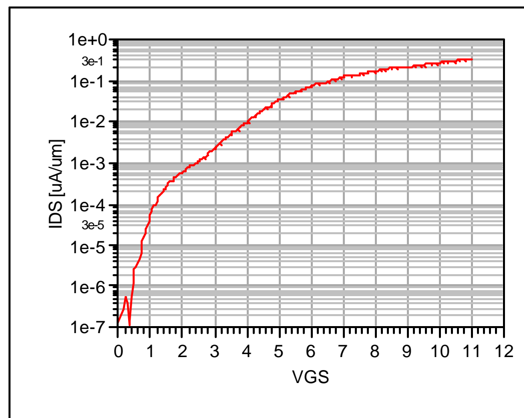


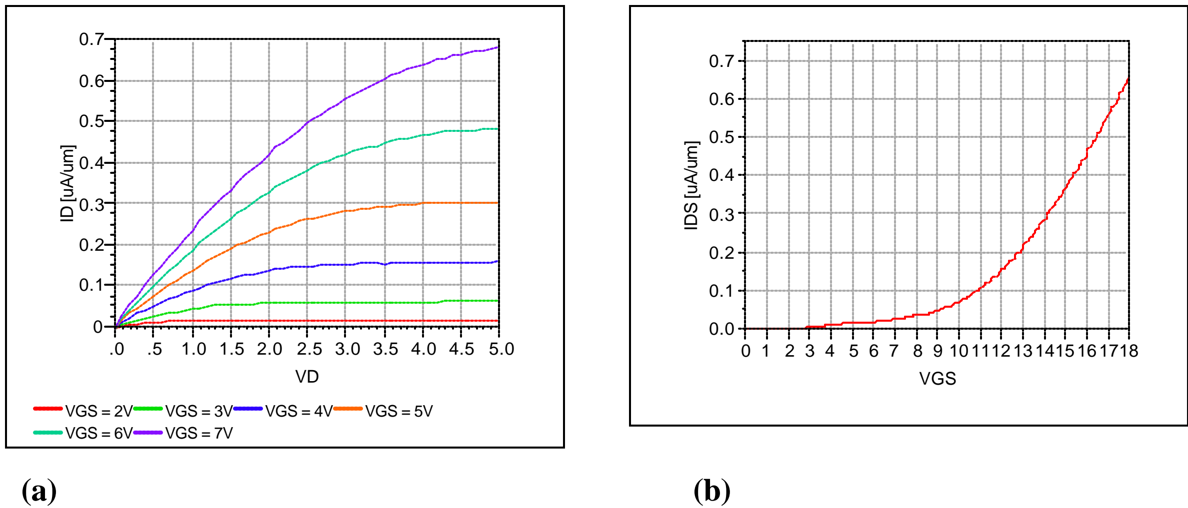
Figure 5.4: Example of typical SiOG NMOS subthreshold characteristic.

5.4 PROCESS RUN #2: L1B THIN-FILM TRANSISTORS

The substrates in L1B had the same boron doping concentration as L1A, with both thin (150nm) and thick (300nm) silicon layers. Without the process issues that plagued L1A, L1B yielded devices with much improved physical appearance and operating characteristics. The oxide breakdown field strength was ~4.5MV/cm, attributed to both improved processing procedures and adjustments in the post-LTO thermal annealing conditions (increased time from 1-hour to 2-hours).

5.4.1 NMOS TFT CHARACTERISTICS

A family of curves for an NFET transistor with a length of 6μm and width of 24μm is shown in Figure 5.5a. This particular wafer had a silicon thickness of approximately 300nm. Note that the device appears to be turning on at a reasonable gate voltage, slightly higher than 2 volts. However the ID-VG threshold sweep does not appear consistent with this interpretation; the V_{Tn} from Figure 5.5b (same device) appears to be around 11 volts.



(a) **(b)**

Figure 5.5: Characteristics of a L1B, L = 6μm W = 24μm, thick-X_{Si} (300nm) NFET TFT for a (a) ID-VD sweep where the threshold voltage appears to be around ~2V and (b) ID-VG sweep where the full turn-on is not realized until ~11V.

An explanation for this difference in extraction of threshold voltages can by determined by further analysis of the subthreshold and transconductance characteristics of the ID-VG sweep. Figure 5.6 shows an enlargement of the linear-mode ID-VG sweep (a,b) with the transconductance plotted in figure 5.6c. The turn on of the device appears delayed (with respect to the gate voltage sweep) and a reasonable threshold voltage cannot be easily extracted via a linear extrapolation. The transconductance shows a two-

stage characteristic not observed in bulk silicon NFETs. The device has a low-voltage turn-on *(stage-1)* followed by a higher-voltage turn-on *(stage-2)*. In the *stage-1* transition region the transconductance is low. After the second turn-on the device exhibits a reasonable on-state g_m. If a threshold voltage is extracted using the first local maximum g_m , a threshold voltage of ~ 2V is obtained, which agrees with the family of curves in Figure 5.5a. These transistors appear to have two distinct turn-on regions that describe the device operation. It was hypothesized that the "spread-out" turn-on behavior was due to interface trap charging; understanding why there were these two regions required a detailed investigation. The likely suspects were top charge present at the LTO/Si boundary, and/or bottom charge present at the silicon/glass interface. The possibility that these trap states were filling and emptying in response to changes in the gate bias was highly probable due to the deposited oxide quality, in comparison to thermal oxide, and limited thermal for post-LTO annealing. The mechanism of trap states is supported by the hysteresis observed in figure 5.6.

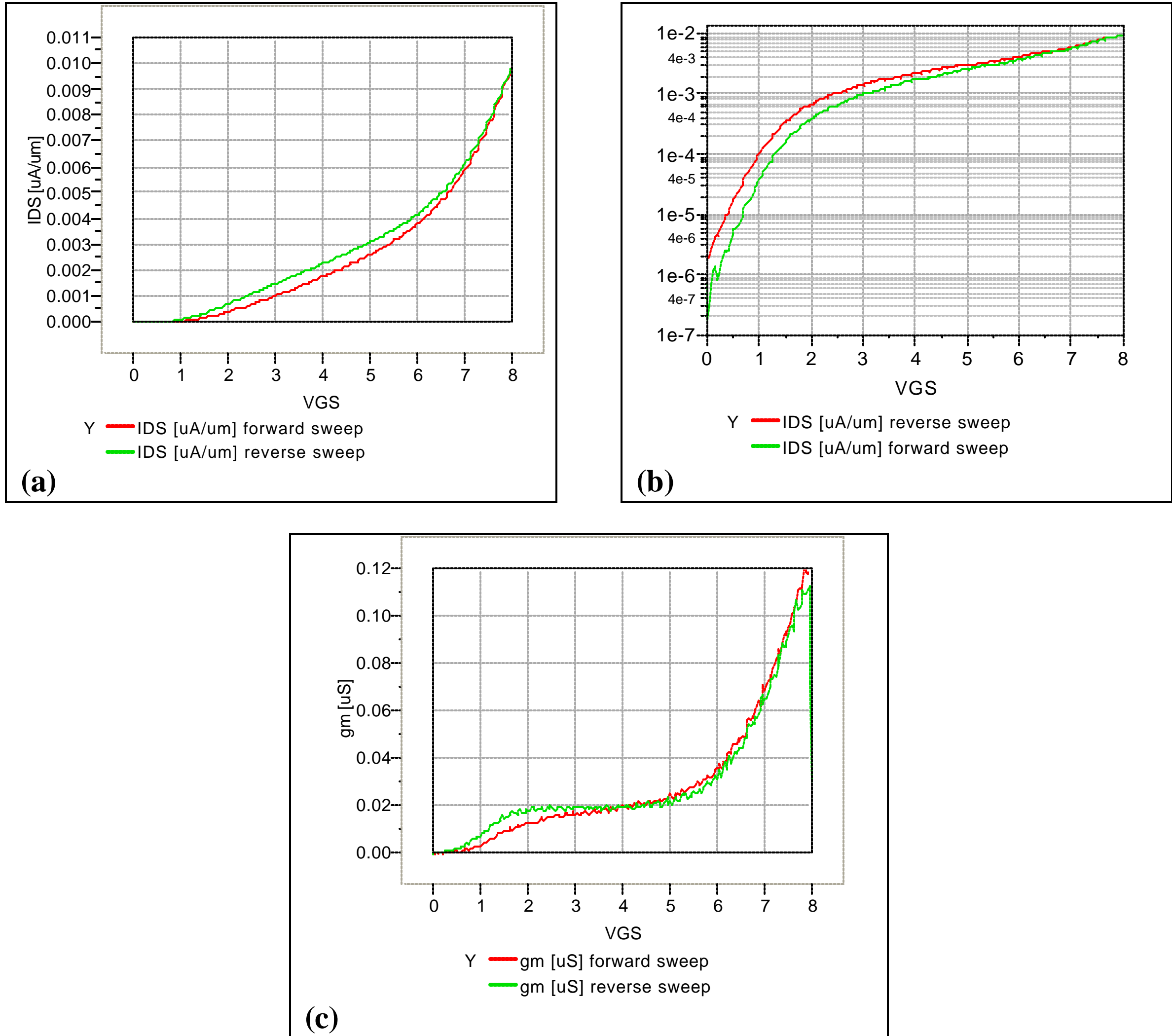
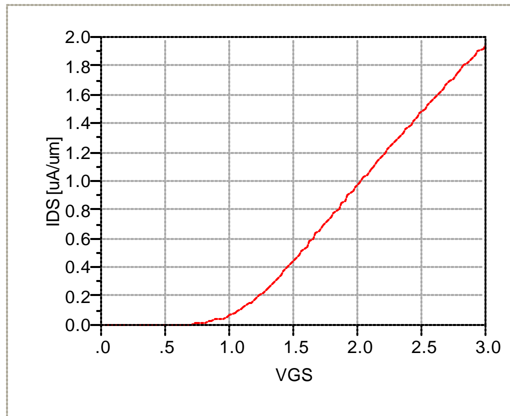
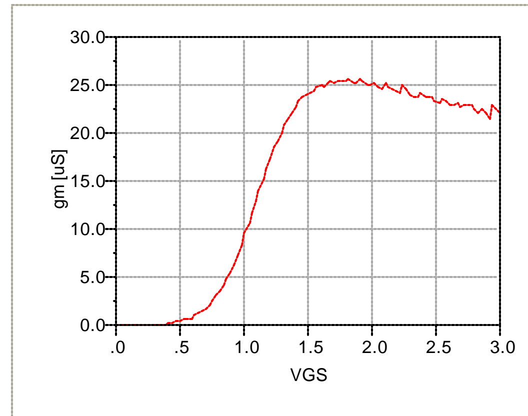


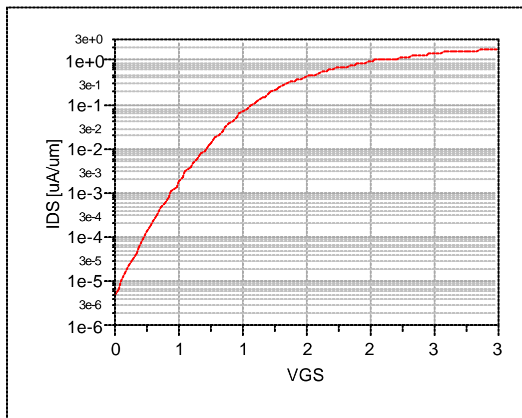
Figure 5.6: I_{DS}-V_{GS} Characteristics of a L1B, L = 24μm & W = 24μm Thick-X_{Si} (300nm) NMOS TFT clearly showing the 2-stage turn-on characteristic, as well as hysteresis in the *stage-1* portion comparing forward and reverse sweeps. Note that this is a DC sweep (HP4145 Parameter Analyzer, long integration mode), thus the traps are exhibiting a slow time response. The *stage-1* V_T is ~ 1V, with a *stage-2* V_T ~ 6V. The channel mobility extracted from the *stage-2* transconductance, μ_n ~ 100 cm^2/V-sec.



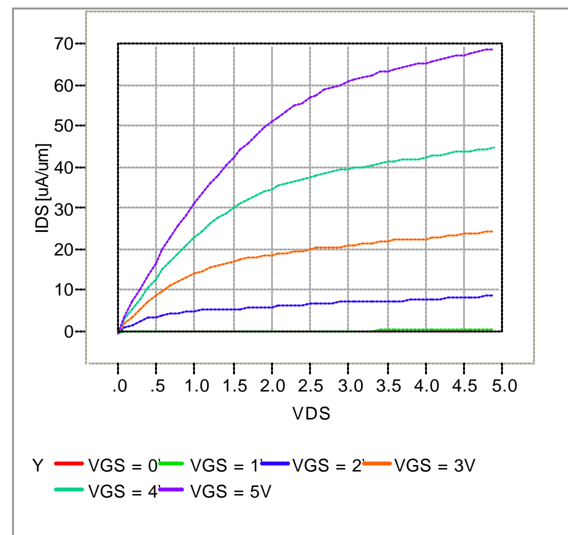
(a)



(b)



(c)



(d)

Figure 5.7: Bulk-silicon LT NFET, L=4μm & W=24μm, I-V Characteristics: (a) Linear-mode I_{DS} vs. V_{GS} (b) Linear transconductance vs. V_{GS} (c) Log mode I_{DS} vs. V_{GS} (d) Family-of-curves. The extrapolated threshold voltage is ~ 1.1V, and the electron channel mobility μ_n ~ 620 cm^2/V-sec, extracted from the linear-mode transconductance.

Note that the bulk silicon monitor wafer shown in figure 5.7 did not show signs of hysterisis, which indicated that the shifting may be due to bottom charge, or some difference between the LTO/silicon interface on bulk-silicon versus SiOG. These results were not conclusive and further study was required to separate the influence of top charge and bottom charge.

Thin-X_{Si} (150nm) NMOS TFTs were also fabricated and demonstrated a trend toward lower threshold voltage, higher transconductance (and thus, channel mobility) and improved sub-threshold characteristics, as shown in figure 5.8. The linear-scale ID-VG characteristic does not exhibit a pronounced two-stage turn-on behavior, however the log-scale plot shows that this feature is still present. The extracted electron channel mobility determined from the stage-2 transconductance was ~ 200cm^2/V-sec; approximately a factor of two higher than the thick-X_{Si} NMOS TFTs. While it was expected that the thin-X_{Si} devices would exhibit a moderately higher transconductance, at the given doping concentration (N_A ~ 5E14cm^{-3}) the silicon layer approaches the maximum thickness that supports a fully-depleted body, and a factor of 2 was surprising. The higher mobility found on thin-X_{Si} devices may also be due to differences in the substrate preparation. Similar trends were observed on the PMOS TFT characteristics, although the mechanisms of device operation are actually quite different, as will be discussed in the following section.

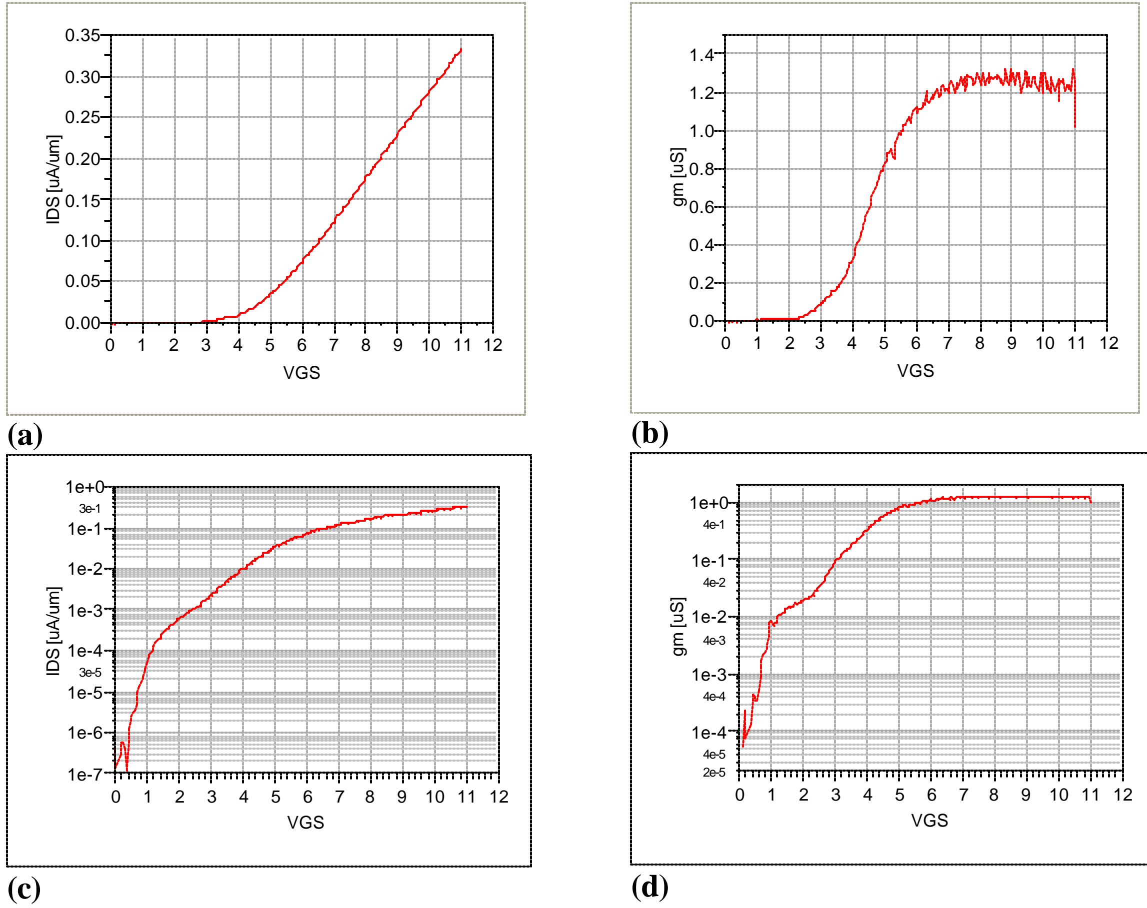


Figure 5.8: I_{DS}-V_{GS} characteristics of a thin-X_{Si} (150nm) NMOS TFT, L=24µm & W=24µm, shown on a linear scale (a) and log scale (c) which emphasizes the 2-stage behavior. The second-stage threshold voltage is extrapolated to be ~ 5V, and the linear-mode transconductance (b) yields a channel mobility μ_n ~ 200 cm^2/V-sec. The log-scale plot shows reasonable *stage-1* sub-threshold slope, where SS ~ 400mV/dec.

5.4.2 PMOS TFT CHARACTERISTICS

While L1A demonstrated a depletion mode PMOS TFT, process run L1B exhibited an enhancement mode PFET in both 150nm and 300nm film thickness variations. This was highly unexpected, due to the fact that the same silicon layer provided enhancement-mode NMOS TFTs, and there were no V_T adjustment implants performed. Figure 5.9 shows the ID-VG characteristics. The thin-X_{Si} PMOS TFTs exhibited a threshold voltage of ~ -1V, with a linear-mode extracted hole channel mobility μ_p ~ 100cm^2/V-sec.

The *thin-*X_{Si} PMOS TFT had a lower magnitude threshold voltage (V_T ~ -1V) compared to the *thick-*X_{Si} PMOS device (V_T ~ -3V). This trend was also highly unexpected; a thicker p-type silicon layer should require a more-positive gate bias (or rather, negative bias of lower magnitude) to deplete the layer of hole carriers. This suggests that interface charge is depleting the silicon layer of holes, and that the gate voltage must compensate for this effect to bring holes back into the channel; initiating from the bottom of the layer (buried-channel turn-on) and extending toward the surface as the magnitude of the gate voltage is increased. If there is positive charge located at the bottom silicon/glass interface, the magnitude of the gate voltage required to override this charge and establish a hole-conducting channel should be higher for a *thick-*X_{Si} device than for a *thin-*X_{Si} device; experimental observations support this explanation. This also is consistent with the obvious fact that without interface charge, the PMOS TFTs fabricated on p-type silicon with a gate workfunction approximately that of intrinsic silicon should demonstrate enhancement-mode operation; especially the *thick-*X_{Si} devices. Enhancement mode PMOS TFT operation is shown in figure 5.9, with subthreshold characteristics showing a similar two-stage transition as the NMOS TFTs (figure 5.8).

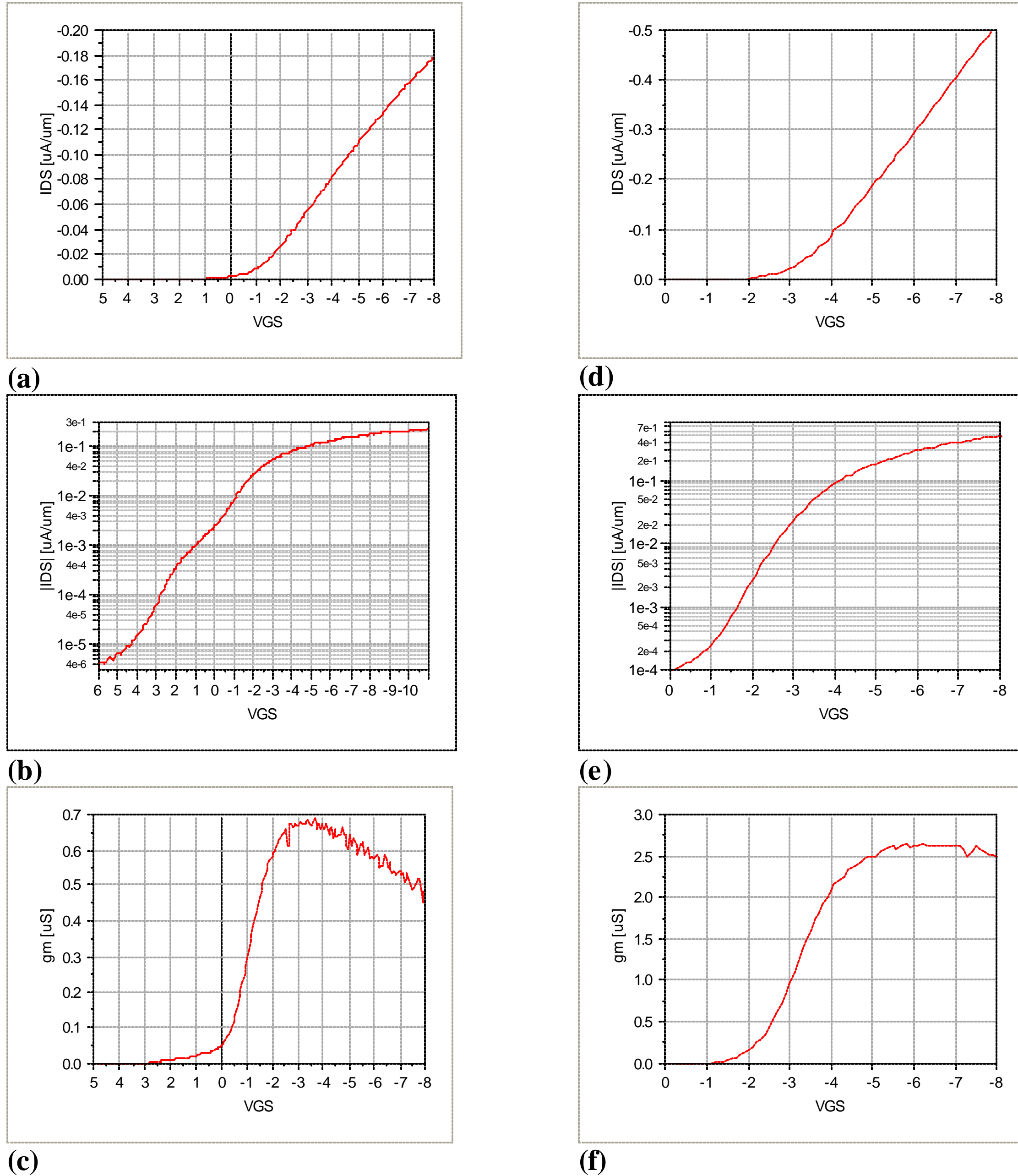


Figure 5.9: Linear-scale characteristics of *thin*-X_{Si} (a - c) and *thick*-X_{Si} (d - f) PMOS TFTs. (a) The *thin*-X_{Si} device (X_{Si} ~ 150nm, L=24µm & W=24µm) exhibits an extrapolated V_T ~ -1V, and an extracted mobility μ_p ~ 100cm^2/V-sec. (d) The *thick*-X_{Si} device (X_{Si} ~ 300nm, L=4µm & W=24µm) exhibits an extrapolated V_T ~ -3.5V, and an extracted mobility μ_p ~ 65cm^2/V-sec. Although not obvious, the two-stage behavior is apparent in (e) as shown by the plateau in the transconductance (g_m). Two-stage PMOS TFT subthreshold characteristic is evident in (b) for the *thin*-X_{si} device. The log-scale plot shows a poor sub-threshold slope, where SS ~ 2V/dec. However, with a gate voltage of +5V the current was reduced to the noise floor of the HP4145 current measurement capability.

The subthreshold characteristics of the PMOS TFT are very poor in comparison to the NMOS counterpart. A relatively poor off-state transconductance presents a fundamental limitation of the buried-channel PMOS TFT; the effective gate capacitance is reduced due to the series combination of the gate LTO-oxide and the partially-depleted silicon layer as hole-carriers are depleted throughout the silicon layer thickness. A two-stage linear-scale (on-state) I_{DS}-V_{GS} characteristic is actually reasonable for this type of device.

5.5 PROCESS RUN #3: L2A THIN-FILM TRANSISTORS

	Type	N	VT
PFET	2a TFT	5.00E+16	+2.0
	1b TFT	5.00E+14	-2.0
NFET	**Type**	**N**	**VT1 / VT2**
	2a TFT	5.00E+16	1V / 6V
	1b TFT	5.00E+14	1V / 6V

Table 5.2: L1B and L2A *thin-*X_{Si} Device results

The table above shows representative results from L1B and L2A *thin-*X_{Si} (X_{Si} = 1500Å) devices. In the case of PFETs the threshold voltages appear to be consistent with the specified doping concentration where L1B is an enhancement-mode device and L2A is a depletion-mode device. However, the NFET results show that the devices appear to be strikingly similar, even though the doping concentration differs by two orders of magnitude.

This section provides plots which show I_{DS}-V_{GS} measurements and simulation models taken at low drain bias, which provide insight on the device operation. The measurements shown for both NFETs and PFETs are taken on large-area devices with

LxW = 24x24μm. The models have been made using a simplified TFT structure in Silvaco Atlas, where L = 2μm. The actual current values have been simply scaled to match the on-state current behavior, which represents a change in the "β", or (W/L)(μCox'), to match the actual device. The off-state current is assumed to scale the same as the on-state current, which is adequate considering that the drain bias is high enough to allow the current to be limited by the gate bias, but low enough to maintain linear-mode operation in the on-state and avoid any short-channel behavior.

5.5.1 L2A NMOS TFT CHARACTERISTICS

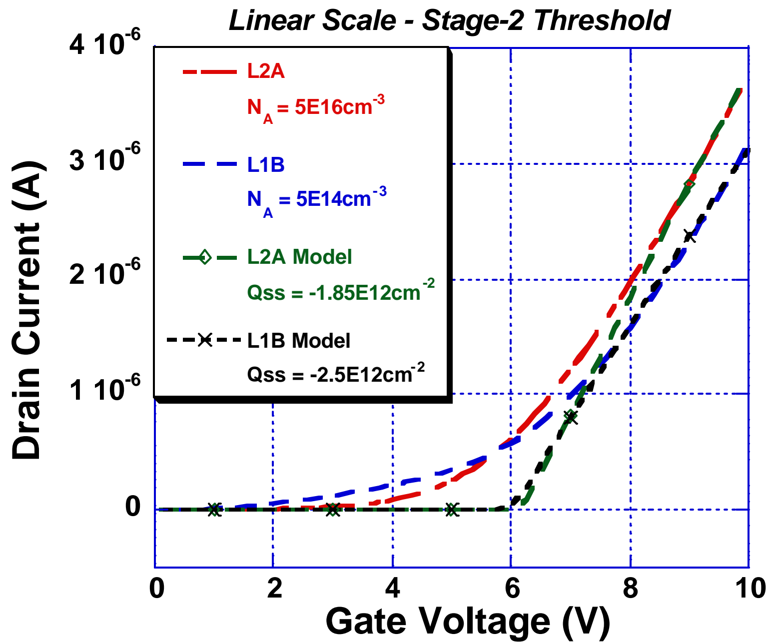


Figure 5.10: Linear I_{DS}-V_{GS} characteristics of L2A and L1B NFETs, showing measured characteristics with 2-stage behavior, and device models with top-side Qss adjusted to match the stage-2 response.

This figure shows typical I_{DS}-V_{GS} characteristics of L2A and L1B NFETs. The linear-scale plot demonstrates a stage-2 threshold of approximately 6V for both devices, despite the difference in doping concentration. The stage-2 threshold is dominated by

charge-state changing interface traps that reach ***negative*** values in the range of $10^{12}cm^{-2}$. The simulated characteristics use the given doping concentrations, and assume a constant level of interface charge to match the linear portion of the on-state behavior. While the difference in the effective interface charge in the linear region of operation ($V_{GS} > 8V$) may be significant, the percentage difference does not seem unreasonable. The higher transconductance shown on L2A may also be dominated by the level of interface charge rather than the doping concentration. A higher doping concentration should result in a lower carrier mobility, however the effective channel mobility can be influenced significantly by scattering events at interface states. At lower gate bias ($V_{GS} < 6V$) the characteristics represent a different stage-1 behavior, which is further emphasized in figure 5.11. The interface states that are operative in spreading out the characteristics in the stage-1 region are acceptor-like, and become negative as the gate bias increases, pushing the apparent threshold (stage-2) out considerably.

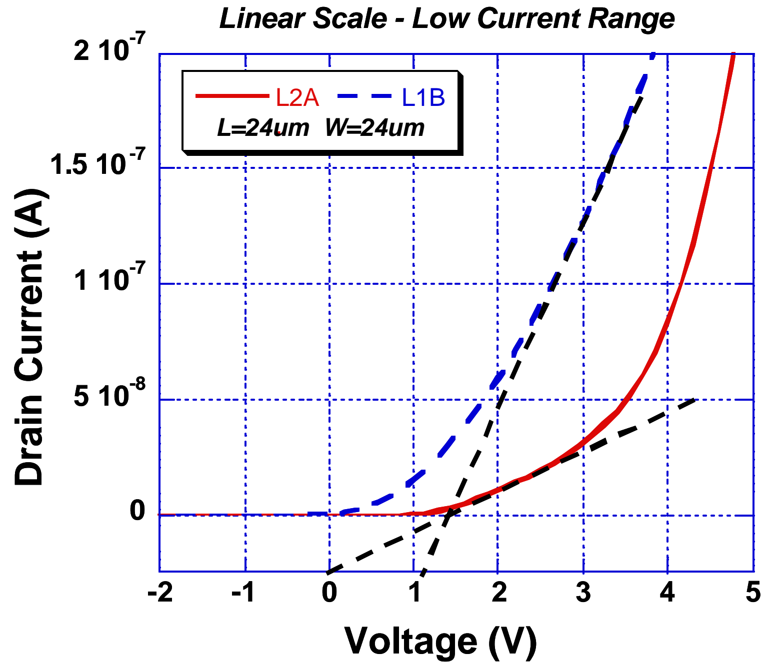


Figure 5.11: A linear scale magnified view of the I_{DS}-V_{GS} sweep in the low current range for L1B & L2A NFETs.

This figure shows a low-current range plot of L2A and L1B NFETs. The delayed turn-on behavior reflects the high level of state-changing interface traps. There are obvious differences between the two characteristics. An extrapolated stage-1 threshold could be interpreted around 1.4V for each characteristic, however the differences demonstrate that this extrapolated value is meaningless; the full characteristic is needed to describe the device behavior in this region of operation. L1B shows an apparent linear-scale turn-off (where I_{DS} goes to zero) at V_{GS} ~ 0.3V, while L2A shows a turn-off at V_{GS} ~ 1.3V, which seems to be consistent with the respective boron concentration. Differences in the energy distribution of interface traps are the probable explanation for the shape of the characteristics through the stage-1 to stage-2 transition.

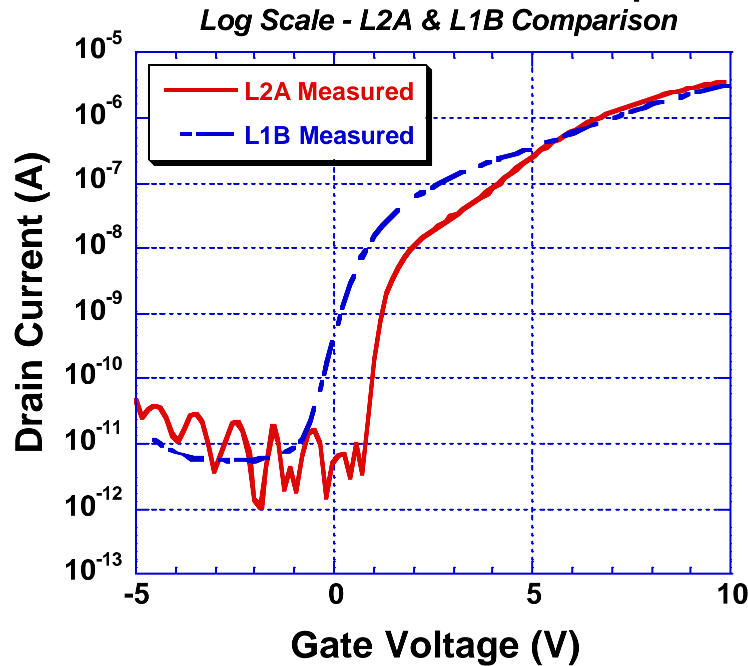


Figure 5.12: Linear regime I_{DS}-V_{GS} sweep on log scale for L1B & L2A.

Figure 5.12 shows the same I_{DS}-V_{GS} characteristics on a log-scale for comparison. The 2-stage behavior is more pronounced on the L2A device; however it is also apparent on the L1B device. The subthreshold characteristic is steeper on the L2A device, which is consistent with a lower concentration of lower-energy interface traps. As the devices are swept from subthreshold into strong-inversion, the filling of interface traps follows the gate bias according to the particular energy distribution. Figures 5.13 and 5.14 show the L1B and L2A measured characteristics separately, along with simulation models.

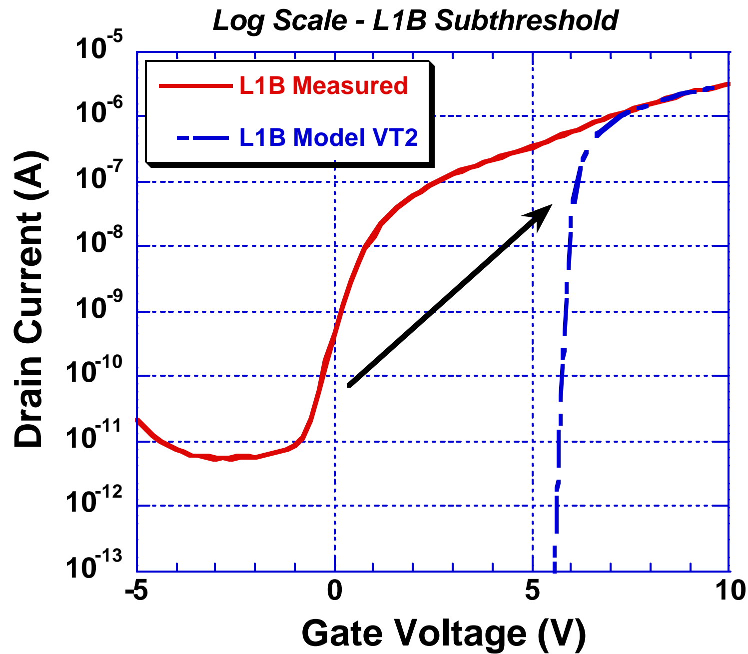


Figure 5.13: Subthreshold comparison of L1B measured and modeled for a linear regime I_{DS}-V_{GS} sweep displayed on log scale.

Figure 5.13 shows a log-scale plot of the same measured and modeled characteristics from L1B shown in figure 5.10. The measured subthreshold behavior is relatively poor, and is not consistent with a threshold voltage of 6V. The arrow represents a transition from the subthreshold regime to the modeled characteristic in the stage-2 region of operation. This same comparison for L2A is shown in figure 5.14, with an added modeled characteristic for the stage-1 behavior.

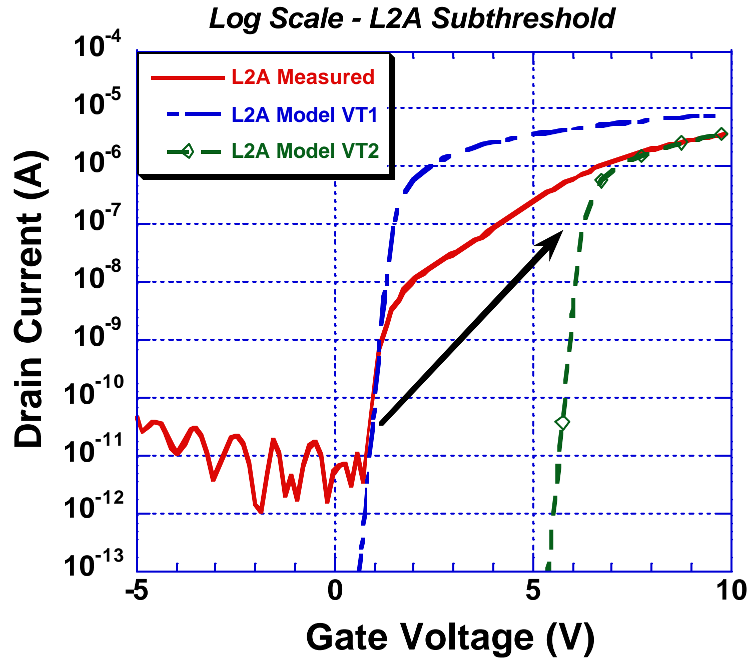


Figure 5.14: Subthreshold comparison of L2A measured and modeled, linear regime I_{DS}-V_{GS} sweep displayed on log scale. Model parameters are given in the following discussion.

The L2A device subthreshold behavior is much steeper than the L1B device, and is consistent with the modeled characteristic with a threshold voltage of 1.3V, where Qss is taken to be +2E11cm^{-2}. Unlike the L1B device, the level of interface charge appears to be at this constant level until the gate bias is increased above 1.3V when interface traps begin to dominate the effective interface charge level. The arrow represents a transition from the subthreshold model (VT1, Qss = +2E11cm-2) to the on-state model (VT2, Qss = -1.85E12cm^{-2}).

5.5.2 L2A PMOS TFT CHARACTERISTICS

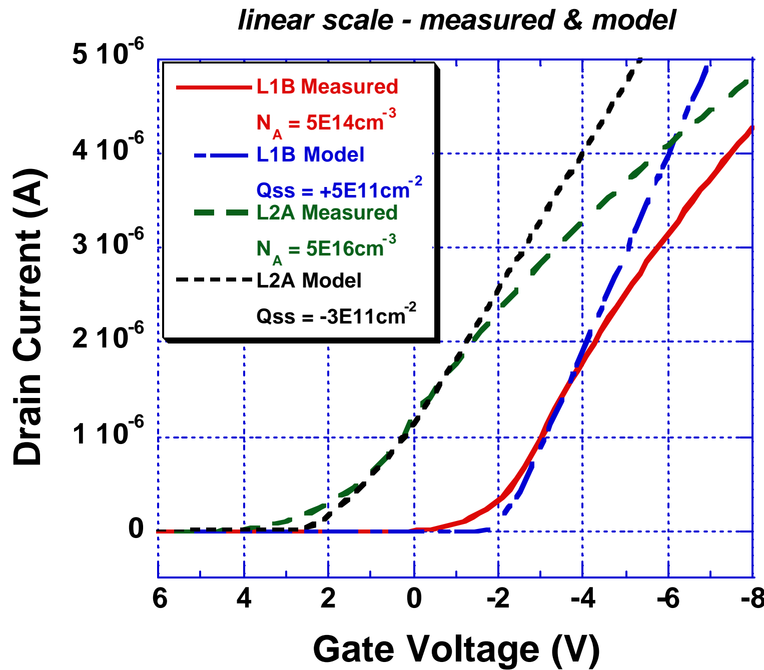


Figure 5.15: Linear regime I_{DS}-V_{GS} plot of L1B & L2A measured and modeled PFET characteristics, using a single value for top-side Qss.

The L1B and L2A PFETs demonstrate enhancement-mode (L1B) and depletion-mode (L2A) threshold voltage characteristics that appear to be consistent with the substrate doping concentration with reasonable levels of interface charge. The effective interface charge (Qss) which provides a reasonable fit to the on-state device characteristic is positive for L1B, and negative for L2A.

The positive value of Qss taken for L1B promotes hole depletion and causes the threshold voltage to increase in the negative direction. The boron concentration in the silicon layer is taken to be 5E14cm^{-2}, which corresponds to the higher end of the vendor-specified resistivity range of the source wafer (1-10 Ω-cm). A higher doping concentration would require a higher level of positive charge for the same on-state

characteristic. Although the value of Qss taken for L2A is negative, the actual Qit is changing and the taken value of Qss as a constant is only useful for comparison.

Note that for the moment, the models are attributing all V_T shifts to top-side charge at the silicon/LTO interface, whereas bottom-side charge at the silicon/glass interface which may be influencing the device operation is not considered at this point. Also note that as the gate bias is swept from on-state to off-state, the characteristics are spread out considerably compared to the device models which are using a constant value for Qss. As in the NFET discussion, this spreading is attributed to a changing level of interface traps. When the gate is swept from off-state to on-state, donor-like interface hole-traps may increase the level of positive interface charge, however this effect appears to be minimal. The change in interface charge appears more apparent in the PFET off-state (see figure 5.16) whereas this seemed to dominate the NFET on-state behavior. The subthreshold region spreading appears to be due to hole-emptying (electron backfilling) of donor-like states and/or the electron-trapping of acceptor-like states as the gate bias increases in the positive direction.

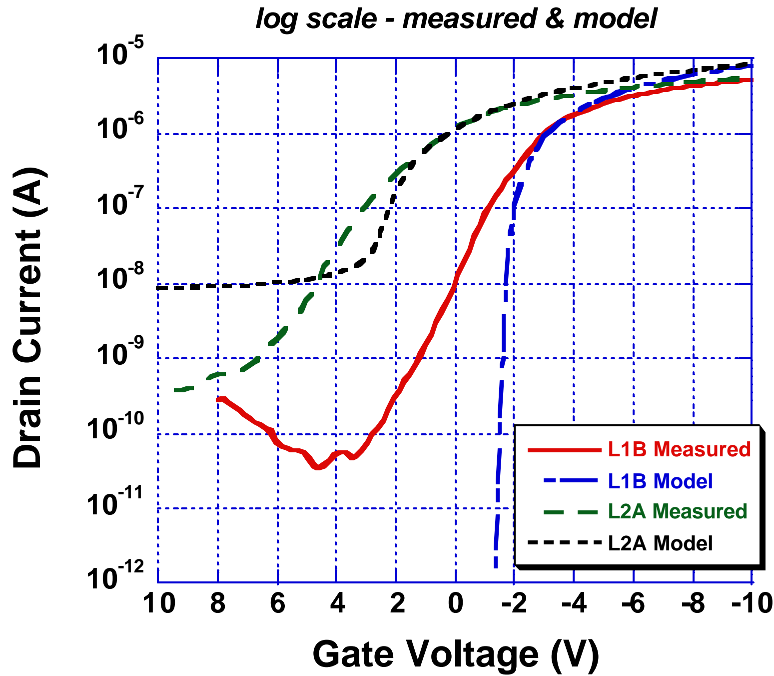


Figure 5.16: Linear regime I_{DS}-V_{GS} plot of L1B & L2A measured and modeled PFET characteristics on a log scale plot.

Figure 5.16 shows the off-state characteristics of L1B & L2A devices using the same models shown on the linear-scale plot (fig. 5.15). The L1B measured characteristic has a much lower subthreshold slope than the L1B model, which also translates to a much higher subthreshold current at zero gate bias. The L2A measured characteristic shows some off-state spreading, however the comparison to the model identifies a feature of more importance; the ultimate off-state current measured is lower than the simulated model with a boron doping concentration of 5E16cm^{-3}. This suggests that there may be some influence of positive back-side charge that results in this improved turn-off behavior. The influence of backside charge and interaction effects with the boron doping concentration and the silicon layer thickness has been discussed previously in section 4.5.3.

Although most of the PFET devices from L2A were depletion-mode, there were several devices that demonstrated enhancement-mode behavior with excellent off-state characteristics. While assumed values of top-side charge can shift the threshold voltage arbitrarily, the ultimate level of off-state current is defined only by the boron doping concentration and back-side charge level. Figure 5.17 shows the on-state characteristics of representative enhancement-mode and depletion-mode (shown previously) PFETs.

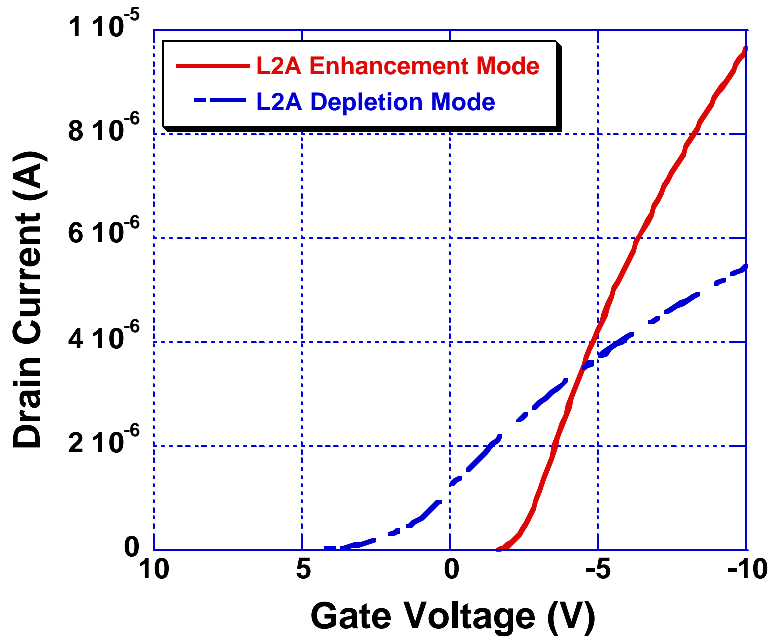


Figure 5.17: Linear regime I_{DS}-V_{GS} plot of L1B & L2A measured PFET characteristics.

The L2A enhancement-mode device shown demonstrates a threshold of approximately 2.5V, and a higher transconductance than the depletion-mode device. Hole carriers in the depletion-mode device channel appear to have significant mobility degradation, likely due to the quality of the silicon surface. The hole carriers in the enhancement-mode device shown demonstrate less mobility degradation, however

variation over the measurement samples taken could account for this difference. Regardless, the importance of the depletion-mode and enhancement-mode device comparison is shown in figure 5.18, which plots the same characteristics on a log scale.

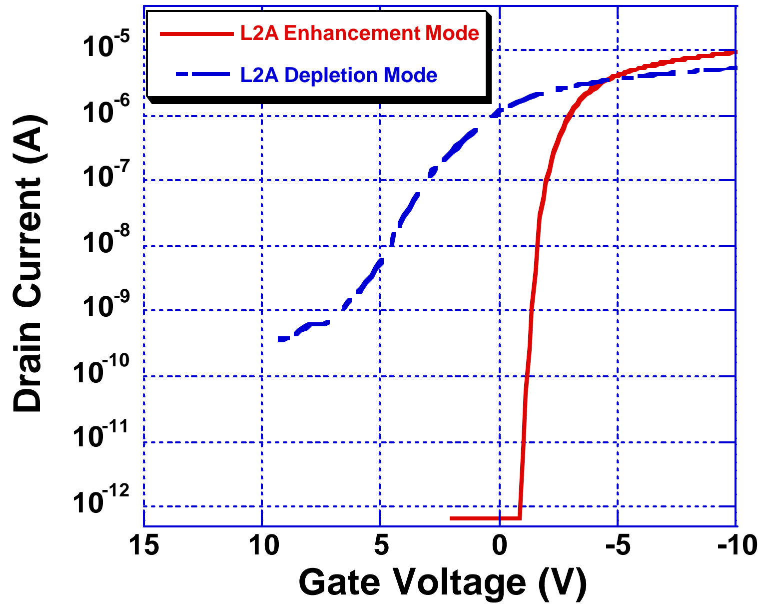


Figure 5.18: Linear regime I_{DS}-V_{GS} plot of L1B & L2A measured PFET characteristics plotted on a log scale.

It is most interesting that the measured L2A enhancement-mode characteristic looks strikingly similar to the L1B device model in figure 5.16. Not only is the subthreshold slope much steeper on the enhancement-mode device, but the ultimate subthreshold current is at the noise floor of the HP-4145 parameter analyzer. Electrical simulation was used to determine how this enhancement-mode device characteristic could even be possible, considering the known boron concentration of 5E16cm^{-3}.

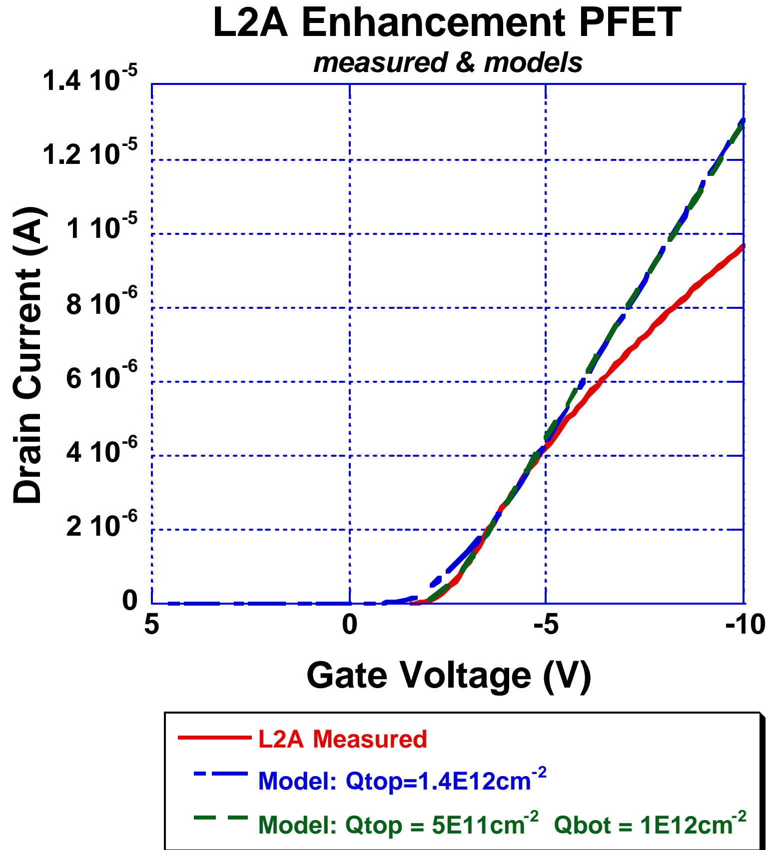


Figure 5.19: Linear regime I_{DS}-V_{GS} plot of L2A measured and modeled PFET characteristics. An extremely good fit at low current levels is obtained when bottom charge is taken into consideration.

Figure 5.19 shows on-state models that match fairly well with the measured characteristic, both with significant levels of positive charge added. The model which has Qtop set to 1.4E12cm^{-2} matches the linear-mode behavior, however the model which has both Qtop and Qbot shows a better match to the characteristic at low current levels. This is much more apparent on the log-scale plot in figure 5.20.

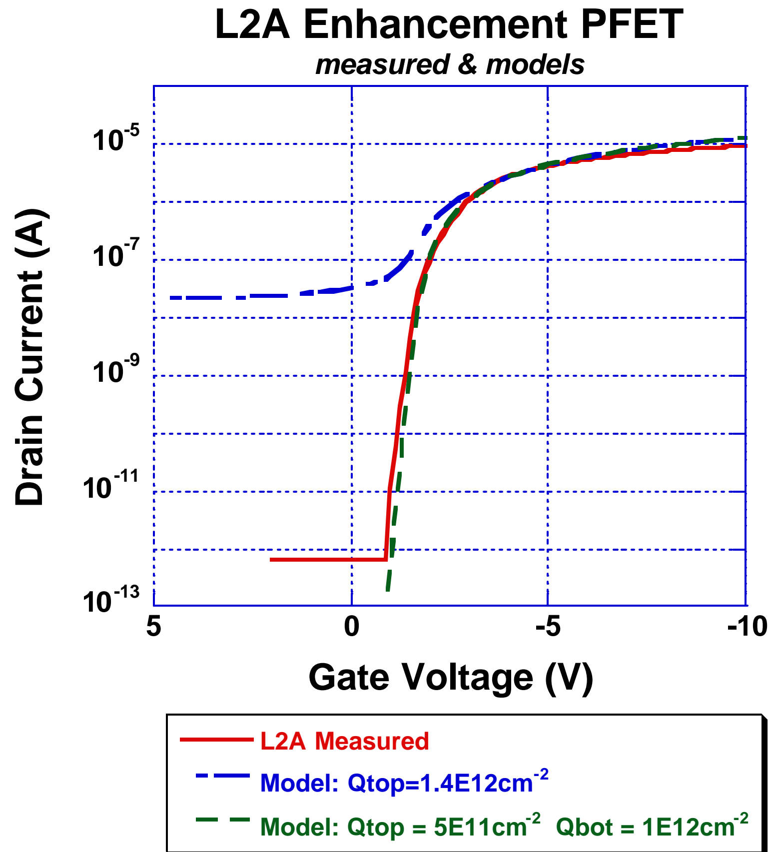


Figure 5.20: Linear regime I_{DS}-V_{GS} plot of L2A measured and modeled PFET characteristics plotted on a log scale. Note the good fit obtained when bottom charge is taken into consideration.

With the addition of both Qtop and Qbot at appropriate levels, the enhancement-mode characteristic was matched with a remarkable fit. Note that with the given value of doping concentration and silicon layer thickness, there is a unique combination of Qtop and Qbot that will provide the best fit to model both on-state and off-state behavior. Another interesting detail is that the L2A enhancement-mode device can be adequately modeled without considering any influence of bias-dependent interface charge, however this is most likely a coincidence since there should not be any correlation between the level of Qbot and the nature of top-side Qit. The level of Qtop used for this model (+5E11cm^{-2}) may be an appropriate assessment of fixed top-side charge for L2A

substrates. While this seems high for a dry O_2 grown thermal oxide, it is typical for a steam-grown oxide and quite reasonable for a deposited LTO dielectric.

5.5.3 L1B & L2A DEVICE SUMMARY

The investigation on L1B and L2A devices revealed several details that are critical in understanding the nature of the NFET and PFET operation, and also has identified areas of concern where improvements are required. The following is a summary of these findings:

1. The transistor operation depends heavily on the influence of interface charge, which has been demonstrated to exist at both the silicon/oxide (top-side) and the silicon/glass (bottom-side) interfaces.
2. NFET transistors fabricated on substrates with significantly different silicon doping concentrations can exhibit quite similar linear-scale IDS-VGS characteristics, with distortion due to acceptor-like interface traps (fill and become negatively-charged) that dominates the turn-on behavior.
3. The distortion in the IDS-VGS characteristic in both the on-state and off-state (subthreshold) regions depends upon the energy distribution of interface traps that are changing charge state in response to changes in the gate bias. This distortion can extend over several volts of gate bias.
4. NFET devices that demonstrate steep subthreshold characteristics exhibit an effective top-side interface ***fixed*** charge of ***positive*** $10^{11}cm^{-2}$ level, however final on-state values are ***negative*** and in the $10^{12}cm^{-2}$ range.
5. The influence of bottom-side charge on the NFET operation was not distinguishable from the influence of top-side charge, and may have some contribution to the level of fixed charge observed. Note that a very high level of positive backside charge would result in a depletion-mode NFET behavior; this was not observed in either L1B or L2A.

6. There can be a significant amount of within-wafer variation in the transistor operation; thus the presented NFET and PFET data is representative. In addition, transistors (NFETs and/or PFETs) fabricated on the same wafer need not have the same amount of interface charge. Fixed charge levels may vary, and interface trap levels that influence the NFET and PFET on-state behavior are dependent on trap states on the opposite side of the bandgap.
7. The level of ***fixed*** charge found to explain the behavior of the p-body (buried-channel) PFET devices, taken to be at the top-side interface, is in the $10^{11}cm^{-2}$ range, and may be either positive or negative.
8. Buried-channel PFETs seem to have on-state characteristics that are dominated by the doping concentration. While there may be significant spreading in subthreshold due to interface traps, the amount of distortion in the on-state is not nearly as prominent as the NFET.
9. Variation in the influence of interface charge can result in depletion-mode and enhancement-mode PFET behavior within the same wafer, as shown in L2A. The interface charge may be at the top-side (silicon/oxide) or bottom-side (silicon/glass) interface, or some combination thereof.
10. The influence of bottom-side (silicon/glass) interface charge can vary between insignificant (as on L1B) to high levels ($10^{12}cm^{-2}$) that can dominate the PFET device behavior, as in the case of enhancement-mode devices found in L2A. Enhancement-mode PFET operation with a moderately doped p-body (L2A, N_A = 5E16cm^{-3}) that exhibit excellent turn-off behavior can only be explained by a high level of bottom-side ***positive*** (hole-depleting) interface charge.

The investigation on devices characterized in L1B and L2A have revealed an extensive amount of information on the nature of interface charge and state-changing interface traps in these devices. Having both NFET and PFET devices has allowed the influence of top-side and bottom-side charge to be assessed independently, on specific devices sampled, with a reasonable level of confidence. Identifying and quantifying

concentrations of bottom-side and top-side charge has been extremely important in determining areas for improvement in the substrate manufacturing process.

The level of bottom-side charge characterizes the quality of the silicon layer attachment on the glass material. Changes in this procedure should reduce the observed variation; these changes may include a thermally grown oxide atop the silicon prior to bonding. Interface trap charge is associated with both the nature of the silicon layer surface finish, as well as the low thermal-budget process; specifically the deposited LTO oxide and thermal annealing processes. These traps may be reduced significantly by improvements to the top surface finish after bonding. Experiments that are investigating the influence of specific bonding procedures and surface preparation conditions on the device operation are currently in progress.

5.6. CMOS Inverter DC Characteristics

Although the transistors characteristics were far from ideal, the enhancement mode NMOS and PMOS devices on lot 1B demonstrated that a CMOS inverter was feasible. Figure 5.21 *D25INV7129B* shows an inverter voltage transfer characteristic operating with a 5 volt supply; note the full rail high and low.

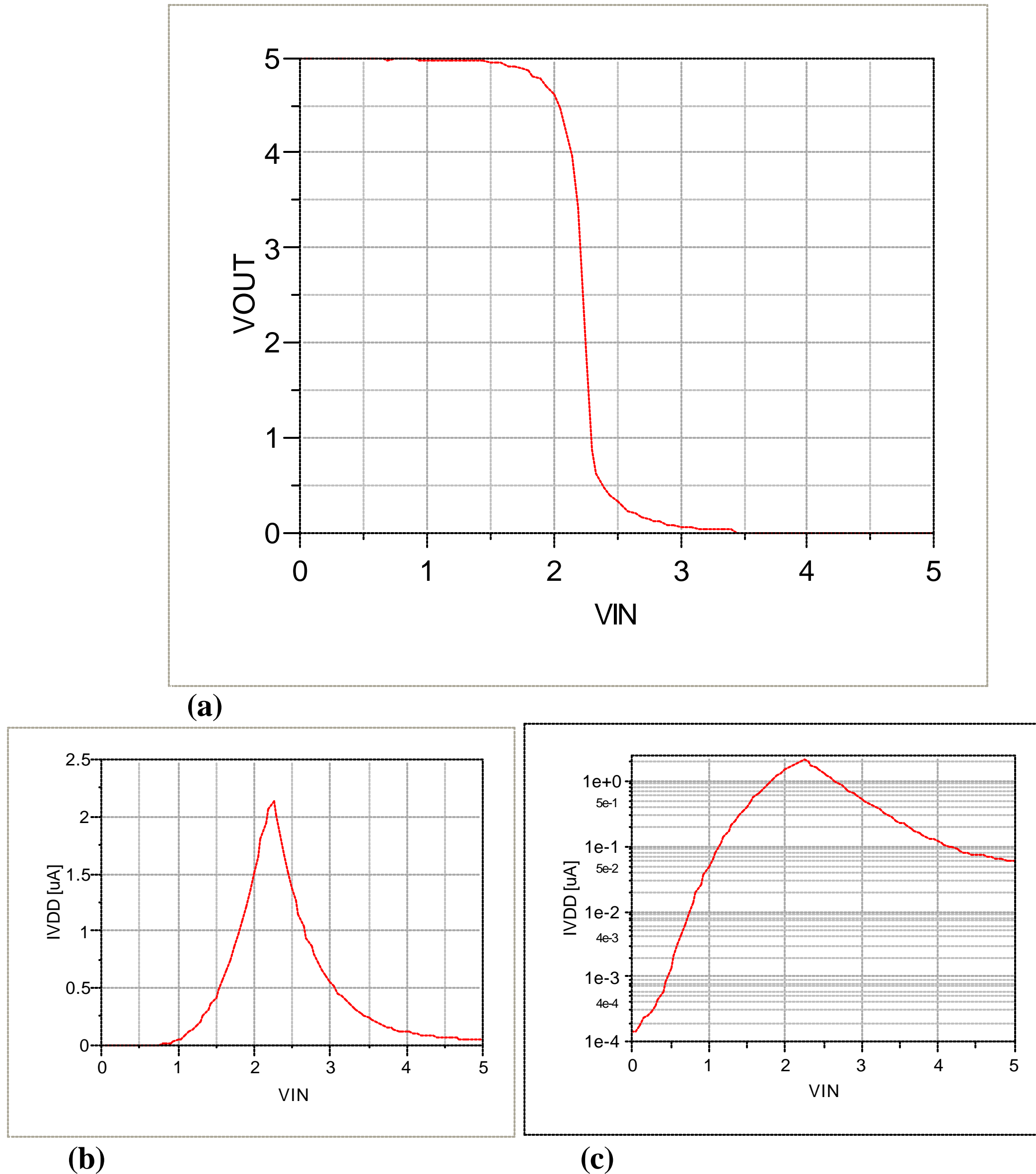


Figure 5.21: A CMOS voltage transfer characteristic (VTC) for common length transistors of 4µm, and widths of 18µm and 45 µm for the NFET and PFET respectively. The VTC is for X_{Si} ~300nm. The calculated linear mode mobility for the NFET was μ_n ~ 148cm^2/V-sec and μ_p ~ 65cm^2/V-sec for the PFET.

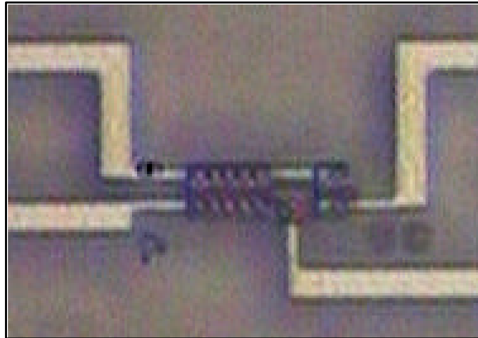


Figure 5.22: CMOS Inverter

Figure 5.21(a) shows the voltage-transfer characteristic (VTC) of an inverter fabricated using the LT-CMOS process. The Vin-Vout relationship has a textbook appearance; showing full-rail output and excellent gain (slope) at an inversion voltage of approximately $V_{DD}/2$. The VTC matches the characteristic of a nearly balanced inverter with symmetric threshold voltages at +1V and -1V for the NMOS and PMOS transistors, respectively; this is actually not the case. While the VTC appears almost ideal, a closer inspection of the short-circuit current indicates an issue with the output-low condition. The PMOS transistor should be in an off-state with a high on the input, however there is a fairly significant current flowing, as shown in fig. 5.21(c).

Another detail which is not obvious from the VTC is that the on-state threshold voltages of the transistors were approximately +/-6V; the entire VTC is actually within the subthreshold region of transistor operation. While this demonstration of CMOS was most interesting, it must be emphasized that the transistor operation was far from delivering an acceptable CMOS capability. Since the operation of the inverter depended on the influence of interface traps, which has a time dependence, the frequency response of the inverter was investigated.

5.6.1 CMOS INVERTER FREQUENCY RESPONSE

The AC characterization was not a main focus in this work, and thus a basic demonstration of switching ability was sufficient. A sinusoidal waveform was used as the input signal, and the input and output waveforms are shown in figures 5.23 and 5.24. Figure 5.23 displays a balanced inverter response to a 1.3kHz sinusoidal input; just past the halfway point on the input swing the output transitions to the opposite rail. Using increased input and supply voltages, Inverter behavior is still apparent at a 13kHz (shown in fig. 5.24) however the output waveform is significantly degraded. This degradation in the output is related to the current drive and output capacitive load (parasitics and oscilloscope probe), and may also be influenced by the time response of trap states involved with the device operation.

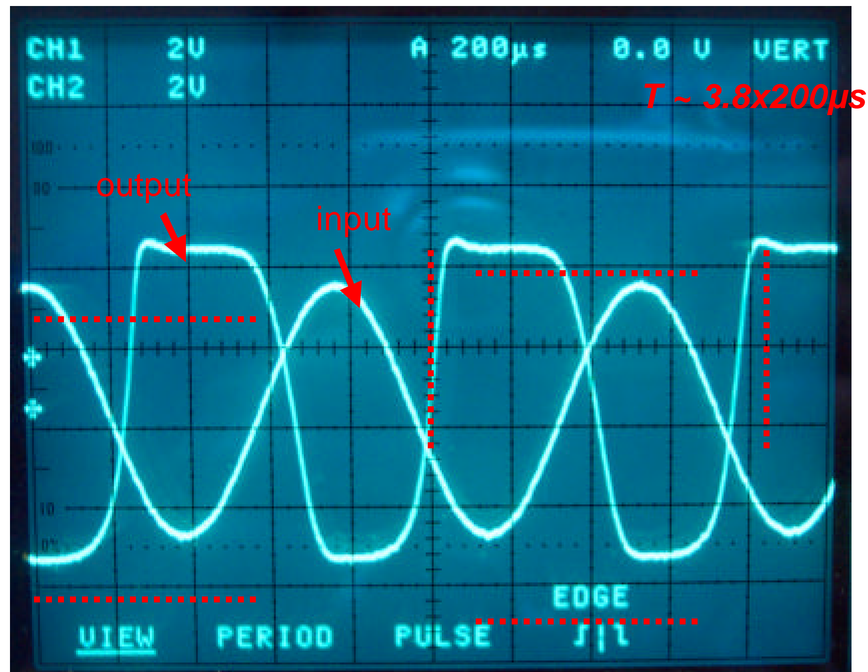


Figure 5.23: CMOS inverter frequency response (L=4µm Wp=45µm Wn=18µm). The input signal signal was a 6V p-p sinusoid, with a period of ~760µs, operating at a measured frequency of 1.3kHz. The circuit supply voltage was 8V (Vdd), and the output signal was measured at 7.8V peak to peak.

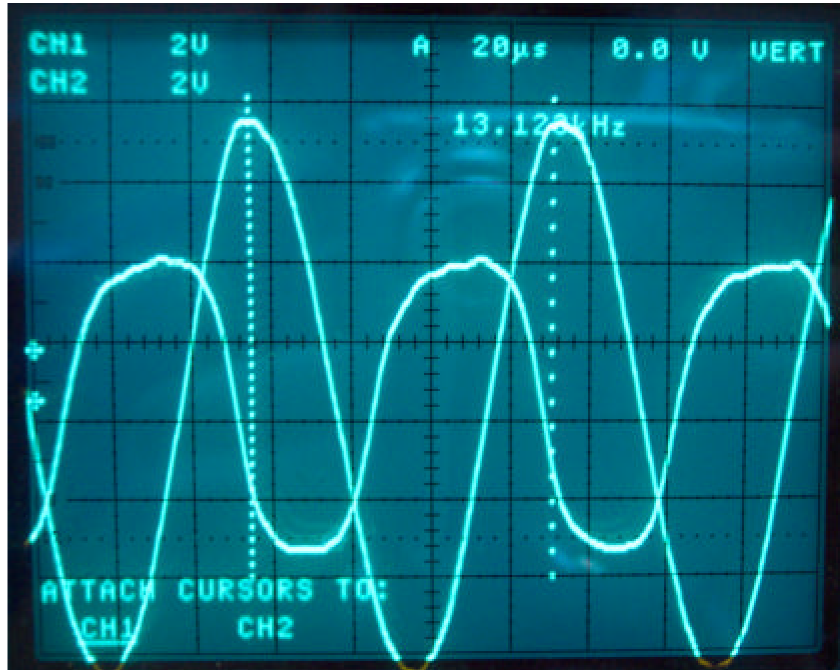


Figure 5.24: CMOS inverter characteristic at 13.1KHz. The input signal was a 14V peak to peak sinusoid. The circuit was operated with a 8V power supply and 7.4V peak to peak was measured at the output.

CHAPTER 6

SUMMARY OF RESEARCH

There were many challenges encountered in fabricating and understanding the behavior of NMOS and PMOS transistors on this substrate material still under development. A significant engineering effort has been invested in the successful realization of functional transistors. This has been the basis of this thesis, through which the understanding of the mechanisms of operation of these devices has begun. This chapter will summarize the various sections discussed, reinforcing the points of primary importance in this work.

6.1. PROCESS DEVELOPMENT

Thermal limitations of the Corning substrate required the development of non-standard unit process steps. The main technical challenge associated with fabricating transistors on glass substrates was the low-temperature (LT) requirement.

To simplify the process, mesa (or island) isolation, was chosen. The silicon profile was carefully engineered to avoid a sharp profile; to preserve the integrity of a conformal oxide deposition. A deposited gate dielectric was used, since thermal oxide cannot be grown within the thermal limitations of the substrate (and at atmospheric pressures). A self-aligned source/drain was desired, therefore a gate material was needed that could withstand dopant activation anneal temperatures. Molybdenum, was developed as the gate metal to fulfill this requirement. Perhaps the most important unit process developed for this SiOG was low temperature activation of dopants. Research was conducted to enhance the percentage of dopant activation at low temperatures by using pre-amorphization implants.

Procedural areas that needed to be addressed for the Corning substrates were glass contamination of standard CMOS processes, glass dimensional stability at process temperatures near the glass strain point, and wafer handling of glass substrates in silicon wafer tools. Figure 6.1 displays the process areas that were engineered to be compliant with LT SiOG CMOS. With the developed unit processes, a MOS device could be designed and implemented on the Corning substrate.

Figure 6.1: Illustration of the theoretical SiOG device.

6.2. SiOG TFT PROCESS INTEGRATION

A low-temperature process was designed to demonstrate that the Corning substrate could yield working CMOS devices. Overall processing of TFTs at low temperature has many similarities to traditional processing of CMOS transistors; there are, however, a few significant deviations as follows. Thermal oxide could not be grown at the required low temperature (T<600°C) thus a LPCVD LTO gate dielectric was implemented. Molybdenum gate material was a thermally stable substitute for in-situ doped polysilicon, which was not available at RIT and would have required an out-source service. Low-dose implants (i.e. well, channel-stop, threshold adjust) were avoided since their impact on carrier mobility and transistor performance was not certain.

The Silvaco licensed ATLAS simulation software package was used extensively to model device operation. Due to the uncertainty in backside interface charge levels on

the starting substrates, this capability allowed a device to be designed with a large tolerance, considering an unknown level of backside charge.

A test chip for the TFT process was designed to allow flexibility in process design, and to provide thorough characterization of the fabricated devices Figure 6.2 shows a 6x6 µm (LxW) device with a body contact. The active region (green) defines the silicon mesa isolated structure.

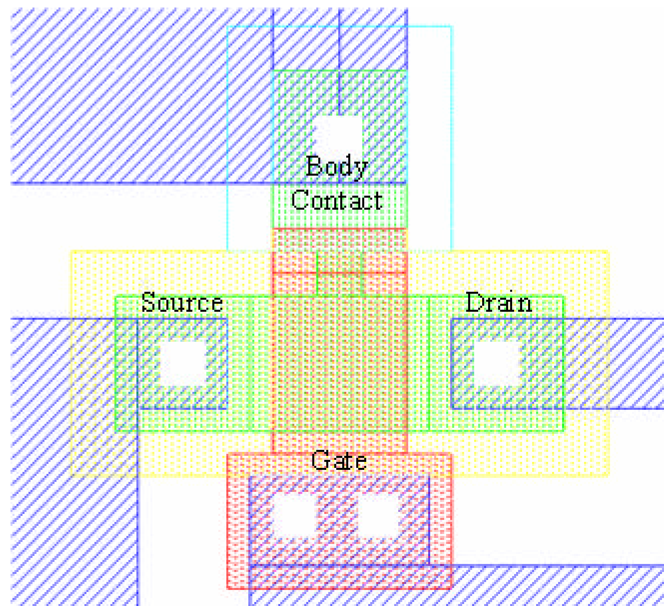


Figure 6.2: 6x6 µm device with a SOI style body contact. Note the body contact and gate polygons are arranged to maximize overlay tolerance.

6.3. TFT CHARACTERIZATION

There were a number of process issues surrounding the fabrication of the first lot (L1A), which was to be expected, as this was the first lot to experience the SiOG-LT-CMOS process. Among these were alignment overlay error that exceeded the design tolerance, and a low-quality LTO dielectric with relatively low breakdown field strength.

Nevertheless, the process yielded working NMOS and PMOS devices, with typical "family-of-curves" characteristics

The substrates in L1B had the same boron doping concentration as L1A, with both thin (150nm) and thick (300nm) silicon layers. Without the process issues that plagued L1A, L1B yielded devices with much improved physical appearance and operating characteristics. The oxide breakdown field strength was ~4.5MV/cm, attributed to improved processing procedures.

L1B produced enhancement mode NMOS and enhancement mode PMOS devices. Figure 6.3 shows an inverter voltage transfer characteristic operating with a 5 volt supply. Note the full rail high and low.

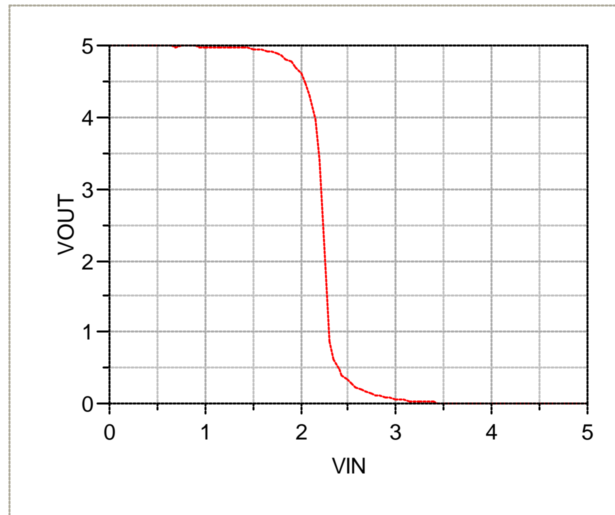


Figure 6.3: A CMOS voltage transfer characteristic (VTC) for common length transistors of 4μm, and widths of 18μm and 45 μm for the NFET and PFET respectively. The VTC is for X_{Si} ~300nm.

In additional to a DC inverter sweep ac characteristics were demonstrated on a SiOG circuit. Figure 6.4 displays a balanced inverter response to a sinusoidal input.

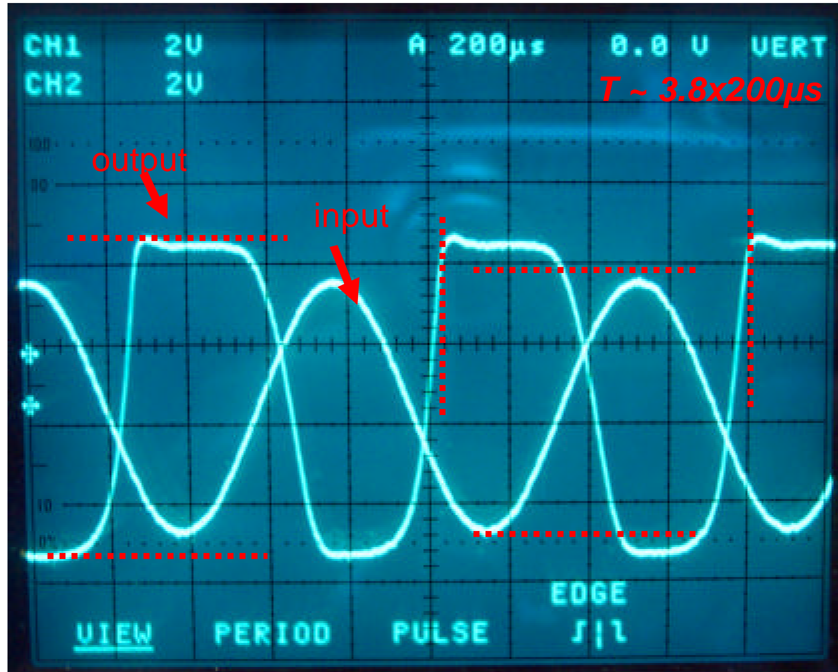


Figure 6.4: CMOS inverter frequency response (L=4µm Wp=45µm Wn=18µm). The input signal signal was a 6V p-p sinusoid, with a period of ~760µs, operating at a measured frequency of 1.3kHz. The circuit supply voltage was 8V (Vdd), and the output signal was measured at 7.8V peak to peak.

A comparison of NMOS and PMOS devices fabricated in lot 2A and lot 1B provided further insight on the details of device operation. Device simulation (Silvaco Atlas) was invaluable in demonstrating the effects of body doping and interface charge. The findings have also identified areas where improvements in the silicon-on-glass manufacturing process must be improved; information critical to Corning, Inc. While the interpretation of the electrical measurements is not entirely unambiguous, this work has provided a significant increase in the understanding of mechanisms involved with the device operation and electrical performance.

6.4. FEEDBACK FROM CORNING

Corning Inc. leads the industry in providing high quality glass to flat panel display manufacturers. It was RIT's privilege to work with Corning in evaluating the device quality of their SiOG substrate material. In 6 months of starting the project with Corning the team had produced two finished process runs, with a third run close behind. All three lots had functioning devices which provided feedback to Corning on their SiOG process and to RIT on low-temp CMOS processing. Corning has expressed their appreciation of RIT's efforts in written communication and also with continued funding for an additional year of investigation. An excerpt from one of Corning's Directors of Research is included below.

> Hi, Karl -
>
> Just a quick Friday pm note to say:
>
> "THANK YOU!!!!"
>
> Your team has done a great job getting this first set of TFT's done with a 2nd set right on their heels! We had a management review today and Dave "advertised" our satisfaction with your effort. The facility has provided the equipment availability and the Rob's obviously paid good attention to detail to put these devices together so well. The analytical work to understand the electron flow and material properties is really helping to guide our technical efforts. We have a very good plan with you moving forward.
>
> I haven't had that much experience with university collaborations. But I still think it is fair to label this effort as a model for "best in class." Having provided such insightful information within the first 6 months represents an excellent start to a hopefully long and fruitful interaction for both Corning and RIT.

Corning's primary interest was to evaluate the device quality of their substrate material, and identify the improvements required in order to present this new substrate material as an option to potential customers in the flat-panel display industry.

6.5. CONCLUDING REMARKS

The primary focus of this investigation was to solve the engineering challenges of dopant activation, deposited dielectric quality and interface charge associated with a low-temperature (LT) process. A process that is compatible with the thermal constraints of the glass has been designed and demonstrated through the fabrication of MOS transistors. The device characteristics demonstrated the on-state and off-state behavior of standard bulk-silicon devices, but also displayed unique features which required an extensive study to understand and explain the governing physics.

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APPENDIX

REV03 TFT PROCESS FLOW.xls

#	Step	Details	Measurement	Comments	Wafers
1	LTO Dep	Deposit 500A of LTO in 6" LPCVD (top) tube 2 runs back to back - first run verify dep rate Time ~4min Include monitor wafer during dep	Prometrix Spectramap thickness on M1	Same monitor wafer can be used for both depositions	Device M1 C1,C2
2	Moly Dep	CVC 601 Molybdenum Deposition Power: 300W Dep Pressure: ~6.9mT Argon Flow: 26.2 sccm Presputter ~ 500sec Dep Time:1600sec	P2 - glass side	Remember - to place the device wafers frontside up!!	Device
3	TEOS DEP	Deposit 2um TEOS oxide on backside to protect Mo *A6-2M TEOS LS*			Device
4	Active Litho	SVG - Coat trac GCA - Lithography SVG - Develop Job: EAGLE1 PASS: 3 Time: ~0.64s (Si wafer) Time: ~0.72s (glass wafer)		Additional hard bake (post develop on hot plate) for 1 min @ 125C	Device C1,C2
5	HF Dip	"Blue Tub" 560A/min (thermal ox etch rate) HF. Get etch rate from LTO monitor wafer (M1). Time = ~30sec	Verify All oxide removed from *un-active* areas		Device M1 C1,C2
6	Silicon Etch	LAM490 - Silicon Etch Gap - 1.24cm CF4 - 0 sccm O2 - 100 sccm Helium - 0 sccm SF6 - 150 sccm O2 - 0 sccm Time: 2:20			Device C1,C2
7	Resist Strip	PRS1000 - PRS2000 10min in each bath			Device C1,C2
8	HF Dip	"Blue Tub" 560A/min (thermal ox etch rate) HF. Get etch rate from LTO monitor wafer. Time = ~30sec	Verify All oxide removed Measure Silicon Step height 5 pts on P2 - Compare with thickness provided by Corning		Device C1,C2
9	Clean	Piranha Bath Use Fresh Piranha Chemistry Sulfuric Acid - 5000ml Hydrogen Peroxide - 100ml Temp - 120C Time - 10 min		Do this step a second before loading into LPVCD	Device C1,C2,C3,C4,C5
10	Gate Oxide Dep	Deposit 500A of LTO in 6" LPCVD (top) tube 2 runs back to back - first run verify dep rate Time ~4min Include monitor wafer during dep **-OR-** Deposit 500A of PECVD TEOS in P5000 A6 - KARL NLS ~5.1 sec dep time *Copy lift step from end to right before dep*	SCA C3,C4 Prometrix Spectramap thickness on M1, C3, C4		Device M1 *again* C1,C2,C3,C4,C5
11	Gate Metal Dep	CVC 601 Molybdenum Deposition Power: 300W Dep Pressure: ~6.9mT Argon Flow: 26.2 sccm Presputter ~ 500sec Dep Time:1600sec		Use the radiant heater during pumpdown	Device C1,C2,C3
12	Gate Litho	SVG - Coat trac GCA - Lithography SVG - Develop Job: EAGLE1 PASS: 3 Time: ~0.7s			Device C1,C2, **C3**
13	Gate Etch	Drytec Quad - Moly Etch Chamber #2 - Quartz carrier Power: 250W Pressure: 150mT SF6: 50sccm Time: 1:40	Verify Moly removed by measureing oxide thickness on C3	Run the ' clean' recipe on chamber 2 before processing. Also season chamber with moly recipe	Device C1,C2, C3
14	Resist Strip	PRS1000 - PRS2000 10min in each bath	P2 - C1 Moly etch depth	*Etch oxide off of M1* *for next step*	Device C1,C2, C3
15	Screen Ox	P5000 - 1000? TEOS Oxide Protective Moly Covering	Prometrix Spectramap thickness on C5 (gate+screen thickness)	**C6 - a p-type wafer** **C7 - a n-type wafer**	Device M1 C1,C2,C3,C5,**C6,** **C7**
16	N+ Litho	SVG - Coat trac GCA - Lithography SVG - Develop Job: EAGLE1 PASS: 3 Time: ~0.6s			Device C1,C2
17	N+ S/D Implant	Varian 350D Dose - 4E15 Energy - 110Kev Species - P31		C6 - a p-type wafer **No more than 30uA** **Beam Current**	Device C1,C2, **C6**
18	Resist Strip	Branson - O2 Ash Hard Ash recipe			Device C1,C2
19	P+ Litho	SVG - Coat trac GCA - Lithography SVG - Develop Job: EAGLE1 PASS: 3 Time: ~0.6s			Device C1,C2

APPENDIX

#	Step	Details	Measurement	Comments	Wafers
20	P+ S/D pre-amorphization Implant	Varian 350D Dose - 3E15 Energy - 60Kev Species - **F**		Flourine is ~ 304 on analyzer C7 - a n-type wafer **No more than 30uA** **Beam Current**	Device C1,C2, **C7**
21	P+ S/D Implant	Varian 350D Dose - 4E15 Energy - 40Kev Species - B11		C7 - a n-type wafer **No more than 30uA** **Beam Current**	Device C1,C2, **C7**
22	Resist Strip	Branson - O2 Ash Hard Ash recipe			Device C1,C2
23	Clean	Piranha Bath			Device C1,C2
24	Anneal	Bruce Tube - 07 Recipe 733 1 hour Anneal in N @600C	SCA C4 Etch Oxide off of C3,C6,C7 CV Test - C3 ResMap - C6,C7		Device C1,C2,C3,C4 C6, C7
25	P+ Buried Implant	Varian 350D Dose - 2E14 Energy - 110Kev Species - B11		***SKIP THIS STEP*** ***ON THIN WAFERS*** ***And ON 1 Thick*** ***Wafer!!!!!!***	Device C1,C2
26	Anneal	Bruce Tube - 07 Recipe 733 1 hour Anneal in N @600C	SCA C4	***Include only the device wafers that recived the Buried Implant***	Device C1,C2,C4
27	ILD0	P5000 - 4000? TEOS Oxide	Prometrix Spectramap thickness on C5 (gate+screen thickness+ILD0)		33
28	Contact Cut Litho	SVG - Coat trac GCA - Lithography SVG - Develop Job: EAGLE2 PASS: 3 Time: ~1.0s		Job 'Eagle2' should be modified to the correct die spacing. (No shrink - 12.7mm)	Device C1,C2
29	Contact Cut Etch	"Blue Tub" 560A/min HF *Get etch time from C5* Time: ~4:30	Verify **ALL** oxide removed from Contact Cuts		Device C1,C2,C5
30	Resist Strip	PRS1000 - PRS2000 10min in each bath			Device C1,C2
31	Metal Deposition	CVC601 - Aluminum Deposition 2000W 16 sccms Argon 5.0 mtorr dep pressure 20 min for ~7500?		**Dip in Blue Tub HF 2-3 times (1sec) directly before sputter pumpdown**	Device C1,C2,C4
32	Metal Litho	SVG - Coat trac GCA - Lithography SVG - Develop	Measure resist thickness on a C1	Additional hard bake (post develop on hot plate) for 1 min @ 125C	Device C1,C2,C4
33	Metal Etch	Wet Aluminum Etchant Use C4 as a monitor wafer Time: ~1:25			Device C1,C2,C4
34	Resist Strip	PRS1000 - PRS2000 10min in each bath	P2 - Metal thickness on C4	C4 can be used as a Aluminum metal capacitor	Device C1,C2,C4
35	Sinter	Bruce Tube - 07 Recipe 139 450C H2/N2 30min			Device C1,C2
36	TEST	Electrical Test			Device C1,C2