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Process design for charge-injection based imaging array fabrication

Michael Schippers

PROCESS DESIGN FOR CHARGE-INJECTION BASED IMAGING ARRAY FABRICATION

by

Michael S. Schippers

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Abstract:

Charge-injection devices (CID's) have been around almost as long as charge-coupled devices (CCD's), yet have generally been overlooked for solid state imaging applications due to their slower operating speeds. However, CID arrays offer advantages over CCD based arrays for certain applications where spectral response and/or X-Y addressing are required.

In order to fabricate CID based imaging arrays, a single level poly CMOS (p-well) process has been modified into a double level poly CMOS (p-well) process that will allow fabrication of both imaging structures and drive circuitry. These modifications are optimized for CID based structures, yet will also allow working CCD based arrays to be fabricated with this process.

Measurements obtained from processed wafers were compared to values obtained using SUPREM IV simulation software from Technology Modeling Associates Inc. and after analysis, further recommendations were made to improve the process.

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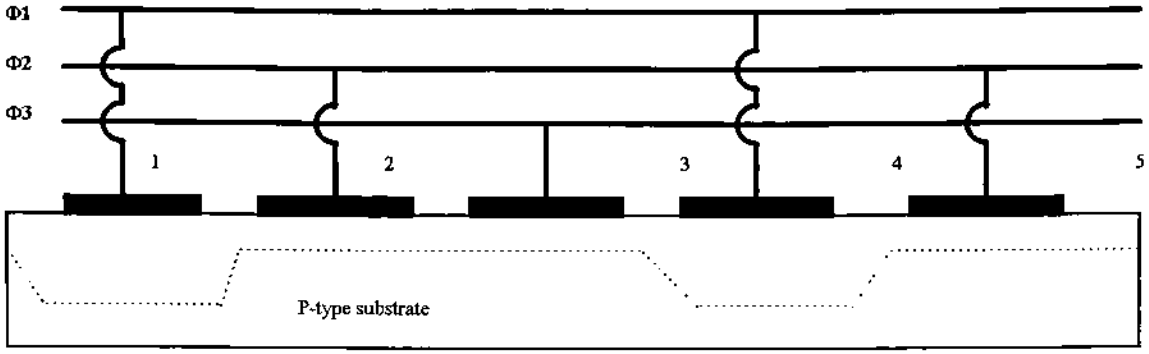
I. Introduction:

The field of solid state imaging has been overwhelmingly dominated by the use of Charge Coupled Devices (CCD's) since their invention in 1970. CCD's with individual pixels numbering as high as 66 million have emerged as the preferred device for almost all electronic imaging applications. However, structural and operational limitations are causing the CCD to be replaced by Charge Injection Devices (CID's) for certain applications that benefit from the CID's unique advantages.

To understand the advantages of the CID, one must first become familiar with the principles behind CCD operation. A CCD is a specific type of charge transfer device which, in its simplest form, can be thought of as a series of interconnected MOS capacitors. Photons which pass through the gate electrode generate electron-hole pairs, from which minority carriers are then collected and stored in potential wells at the surface of the semiconductor. The stored charge can be transferred along the surface by altering the potential (i.e.: voltage) applied to individual gate electrodes in a controlled fashion.



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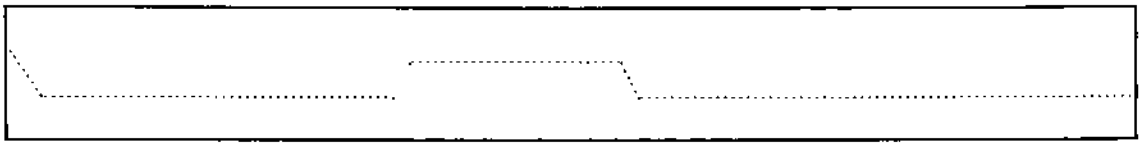

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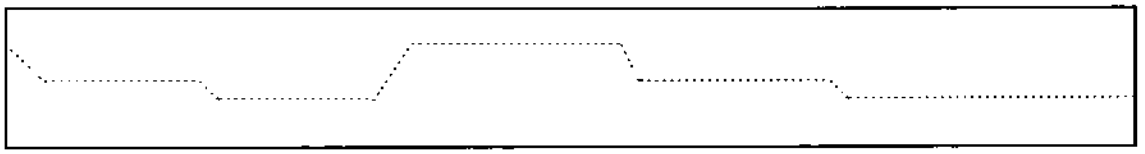

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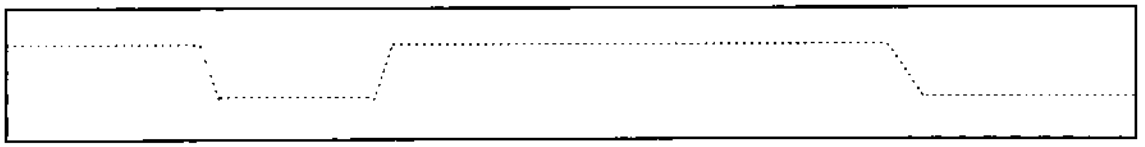


(d) time t = t4

fig. 1.1 Potential well diagram for a three-phase CCD

Since the charge resides at the "surface" (the Si / SiO_2 interface) of this device, it is referred to as a **surface channel** CCD (SCCD). This structure has several disadvantages, the most obvious being the interaction of the stored charge with the interface states. Charge moving along the device can be captured by the interface states, resulting in charge loss or lowered transfer efficiency. One solution to this problem was the invention of the ***bulk*** (i.e.: buried) ***channel CCD*** (BCCD), which moves charge away from the surface into a diffused / ion implanted channel where it is stored as majority carriers.

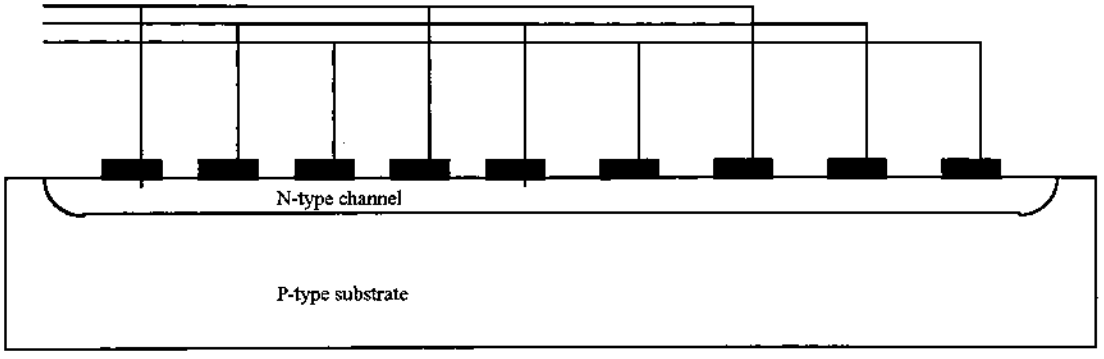


Fig. 1.2 bulk channel CCD [1]

Although charge can interact with bulk recombination / generation (R-G) centers in the channel (i.e.: impurities or dangling bonds within the crystal lattice), the degree of modern process control allows the R-G center density to be more easily controlled than the interface state density. This gives the BCCD a performance advantage over the SCCD. BCCD's collectively refer to two sub-categories of CCD's; **buried channel** CCD's and **peristaltic** CCD's. The term buried channel CCD is usually used in reference to BCCD's with a channel (usually N-type) depth of a micron or less, while peristaltic CCD refers to a BCCD with a channel depth of several microns (again usually N-type) grown by epitaxy.

When the charge is transferred between adjacent potential wells there is an unavoidable loss in net charge. this results because of either insufficient time for all the charge to flow between wells, charge captured by interface/recombination-generation states where the emission time is longer than the transfer time, or the presence of potential barriers between the wells. The overall effects on charge loss refer to the ***charge transfer efficiency*** (**CTE**), which can be thought of in terms of ***charge transfer inefficiency*** (**CTI**):

$$\mathbf{CTE} = (\mathrm{CHARGE}_{\text{before transfer}} - \mathrm{CHARGE}_{\text{after transfer}}) / \mathrm{CHARGE}_{\text{before transfer}} \quad (1.1)$$

$$\mathbf{CTI} = \mathrm{CHARGE}_{\text{before transfer}} / \mathrm{CHARGE}_{\text{after transfer}} \quad (1.2)$$

$$\mathbf{CTE = 1 - (CTI)} \quad (1.3)$$

(the actual expression for charge transfer efficiencies much more complex than this simplified relation, since it takes all effects into account). Acceptable charge transfer generally refers to an efficiency level of 99.99 %, and is directly dependent on such parameters as gate length, channel doping, clocking frequency, substrate bias, and applied gate potential (i.e.: clocking pulse amplitude). Some CCD's improve transfer efficiency by filling the entire channel with a large background charge (known as a ***fat zero***), which increases self-induced carrier drift and helps reduce the charge lost in transfer for small packets of charge. Since this method reduces low level sensitivity, charge transfer inefficiency must be kept as low as possible to prevent performance degradation. Even with high transfer efficiencies, it is evident that overall efficiency will decrease and signal distortion will increase as the number of **pixels** (individual light sensing areas) on the array increases.

Another problem effecting transfer efficiency (and signal distortion) is ***dark current***. Dark current refers to the additional current resulting from thermally generated minority carriers, and is inversely proportional to carrier lifetime. For quality substrates with long lifetimes on the order of 100 μseconds, dark current is essentially surface-state dominated and on the order of 30 nA/cm^2 (much lower in buried channel devices where it is caused by thermal generation in the bulk). While this would seem to only slightly effect low level sensitivity, it becomes a serious issue when the fact that impurities increase the level of dark current is considered. Charge packets transferred through a pixel with a high localized impurity level will be distorted by the increased level of dark current, in comparison to charge packets which are not. Thus, the entire row on the array which transfers charge packets through the affected pixel will have its signal distorted, or ***smeared***.

Another distortion problem which plagues CCD's is ***blooming***. Blooming occurs when the potential well of a pixel reaches its maximum storage capacity, and excess charge spills out and fills up adjacent pixels. This can easily be visualized by thinking of the effect which occurs when a video camera is pointed at a bright light. The intensity of the light is such that

so many minority carriers are generated, the image appears to "white out" in an effect similar to that which occurs in a snow storm. Bulk channel CCD's consisting of a diffused P-region on an N-type substrate (where the resulting p-n junction is reverse biased) exhibit reduced blooming effects, but the close proximity of adjacent pixels makes this problem hard to eliminate.

Last, there is the problem of ***spectral response***. CCD's require incident photons to pass through the gate electrode and gate oxide in order to generate electron-hole pairs in the substrate. Doped polysilicon is by far the most common gate material, yet even thinning to minimal 1500 Å thickness' (with a 500 Å gate oxide) results in poor response to wavelengths less than 500 nm:

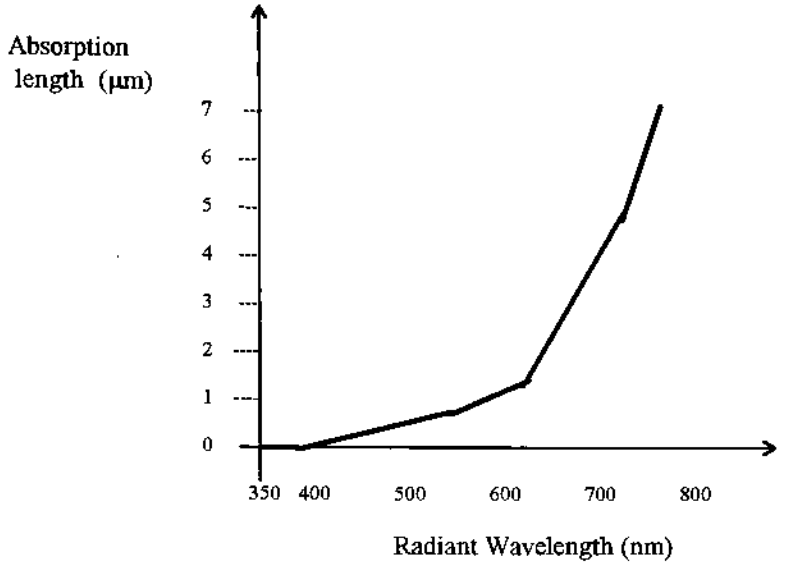


fig. 1.3 Wavelength vs. Absorption length

CID based imaging arrays are not affected by these problems to the same extent which CCD's are, mainly because of their unique pixel structure. When CCD's were first conceived by Bell laboratories, the smallest metal lines that could be patterned were ~10μm wide. Providing a means to access individual pixels directly would have reduced the amount of light sensing area on the chip to an unacceptably low percentage. The solution was to connect rows of pixels together and place the address and amplifier circuitry at the row and column ends, thus providing an acceptable percentage of the chip

was composed of light sensing structures. As a result CCD's lack X-Y addressability, a major limitation for applications involving image shift/rotation.

The CID's structure essentially requires it to function in an X-Y addressable mode. Individual pixel structures are composed of two intersecting MOS capacitors in an orthogonal layout:

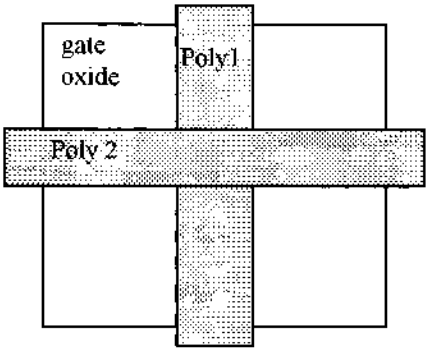


fig. 1.4 CID pixel structure [2]

A column of pixels will have one continuous polysilicon layer for the first capacitor electrode, which provides a common column electrode for all pixels in the vertical direction. The second polysilicon layer forming the other

electrode, will be common to all pixels in a horizontal row. Thus, individual pixels can be accessed by isolating a row for pixel readout at individual columns:

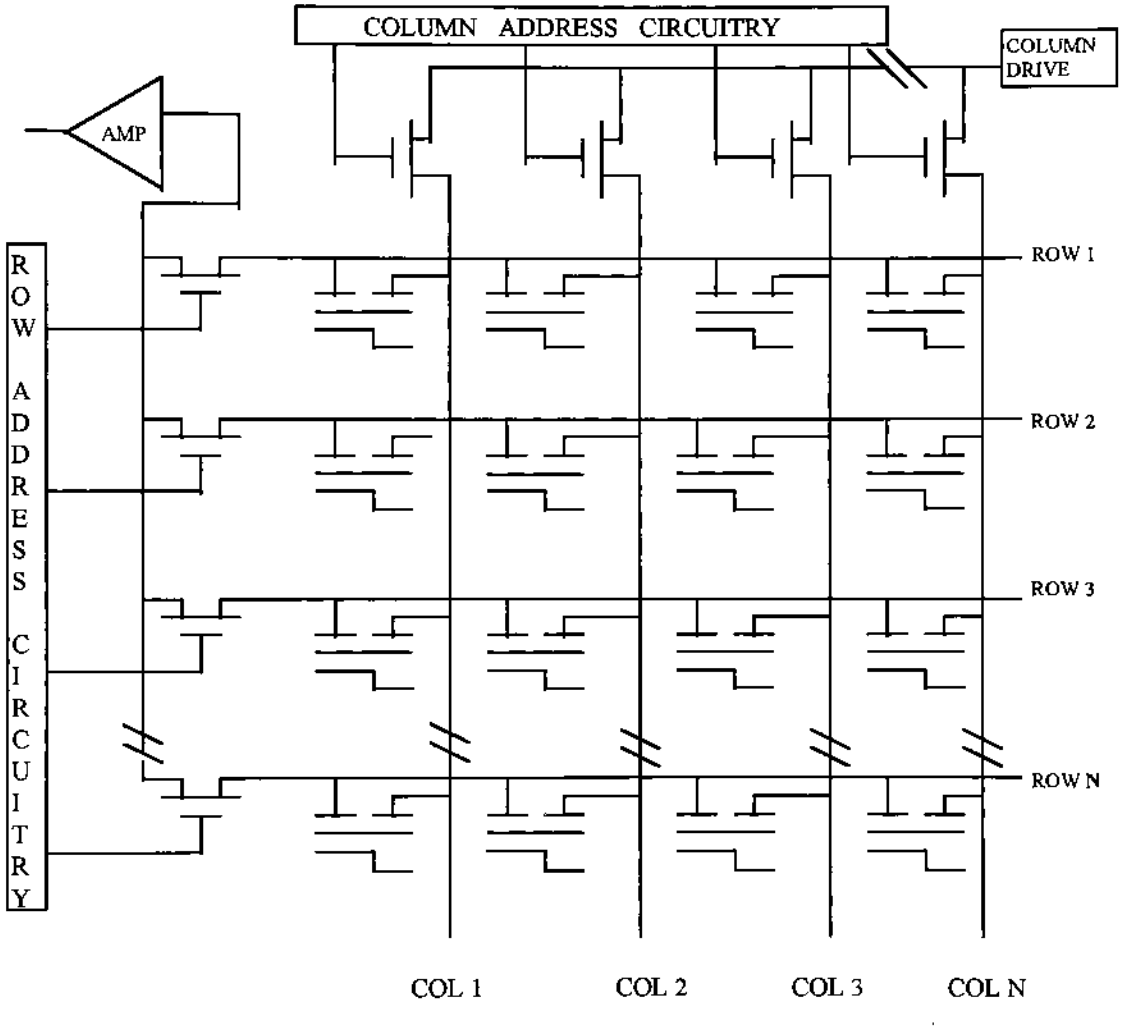


fig. 1.5 CID Imager Architecture [3]

With X-Y addressability being inherent to both the structure and readout technique, CID's do not require high ***charge transfer efficiencies*** and are not readily affected by signal distortion resulting from ***dark current***. Being able to address individual pixels allows for faulty pixels to be ignored without seriously impacting image quality. CID's with bad pixels can still provide excellent image quality, while each bad pixel in a CCD distorts the entire row in which it is located. In other words, CID's with defective pixels can be sold as working devices but CCD's must be totally defect free to function properly. This makes CID's much easier to fabricate than CCD's.

The CID's unique structure also provides excellent control against ***blooming***[4]. In general, CID's are P-channel devices created on low Resistivity N-type epitaxial Silicon. The N-type epi is grown on P-type substrates, the surface of which is P^+ type. This construction essentially forms a reverse biased p-n junction inside every pixel, which collects excess minority carriers and sweeps them into the P^+ layer. By providing such an easy path to the substrate, blooming effects are almost nonexistent in CID's.

Spectral response is also significantly improved by the CID's pixel structure. Only about half of the pixel area on a CID is covered by polysilicon, the rest is covered by the gate oxide. With just ~500 Å of SiO_2

covering half the pixel, wavelengths as small as 400nm will have a significantly improved chance to photogenerate electron-hole pairs in the substrate. Thus, CID's show excellent spectral response over the whole range of the visible spectrum, while CCD's typically lack good response for the "blue-green" through "violet" colors of visible light [5].

II. Theory:

2.1 Charge-injection Device Theory:

The charge-injection device structure (CID) is gaining acceptance for solid state imaging applications as a result of its unique advantages over imaging arrays based on charge-coupled devices (CCD's). The CID imaging technique utilizes injection and (or) intracell transfer to sense photogenerated charge at each individual pixel, which can then be addressed in an X - Y manner. This is in direct contrast to the CCD structure, which requires the photogenerated charge "packet" be transferred along adjacent pixels to a predesignated sensing site. The advantages result from the structure of the CID pixel which is based on the metal-oxide-semiconductor (MOS) capacitor, and consists of two intersecting capacitors that overlap to form a cross pattern (in fig. 2.1.1):

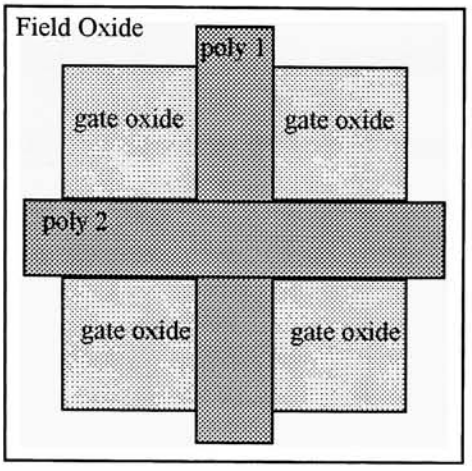


fig. 2.1.1 Basic CID layout

In this schematic the poly1 and poly2 lines represent the capacitor structures formed, respectively, by the first and second layers of deposited polysilicon during fabrication. These capacitor plates would each have the same gate oxide thickness underneath, and would be insulated from each other by an oxide formed on the surface of the first poly layer. Although the capacitor structure would only cover about half the pixel's surface area (defining where potential wells would form in the substrate to collect photogenerated charge),

carriers formed in the exposed regions of the substrate would also be collected, since they would diffuse from the bulk into the potential wells. While the CCD is also based on the MOS capacitor, its individual rows (or columns) consist of numerous interconnected and overlapping capacitor structures (fig. 2.1.2):

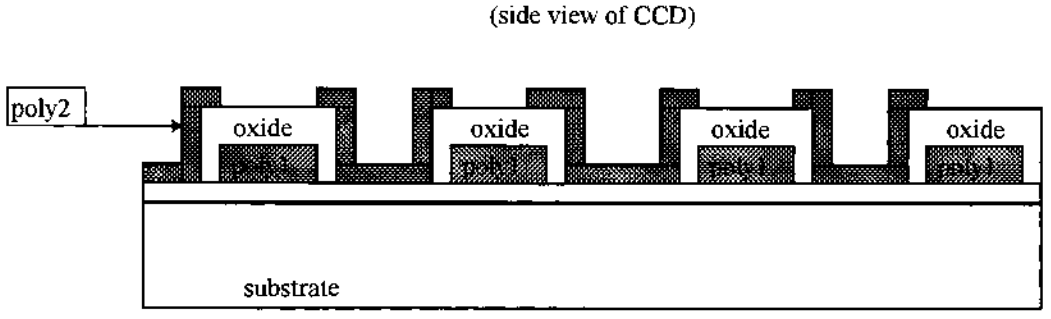


fig. 2.1.2 Basic CCD layout

This results in long series of pixels that must accurately transport individually sensed charge along with the photogenerated charge from preceding pixels, and virtually eliminates the possibility of X - Y addressing. While columns (rows) of CID pixels can be interconnected by one continuous capacitor

structure, they will remain X - Y addressable by isolating the other capacitor structure contained within the pixel. To better explain the unique advantages which the CID pixel structure has to offer requires a review of the structure and operation of the MOS capacitor.

The MOS capacitor refers to a system of metal and semiconductor layers separated by an oxide layer. The oxide layer can be replaced by any suitable insulator (also known as metal-insulator-semiconductor; MIS) but Silicon dioxide is by far the most common, as is evident in the general usage of the MOS capacitor acronym. The metal layer usually consists of either Aluminum, a degenerately doped polysilicon, or a silicide formed from polysilicon, either of which exhibits an energy band diagram similar to a metal. For simplicity, the Aluminum (AL)-Silicon dioxide (SiO_2)-p-type semiconductor (P-Si) composition will be used to explain the workings of the MOS system.

Starting with the energy band diagrams of all three materials prior to their contact, it is evident that all three materials posses different ***work functions*** (Φ):

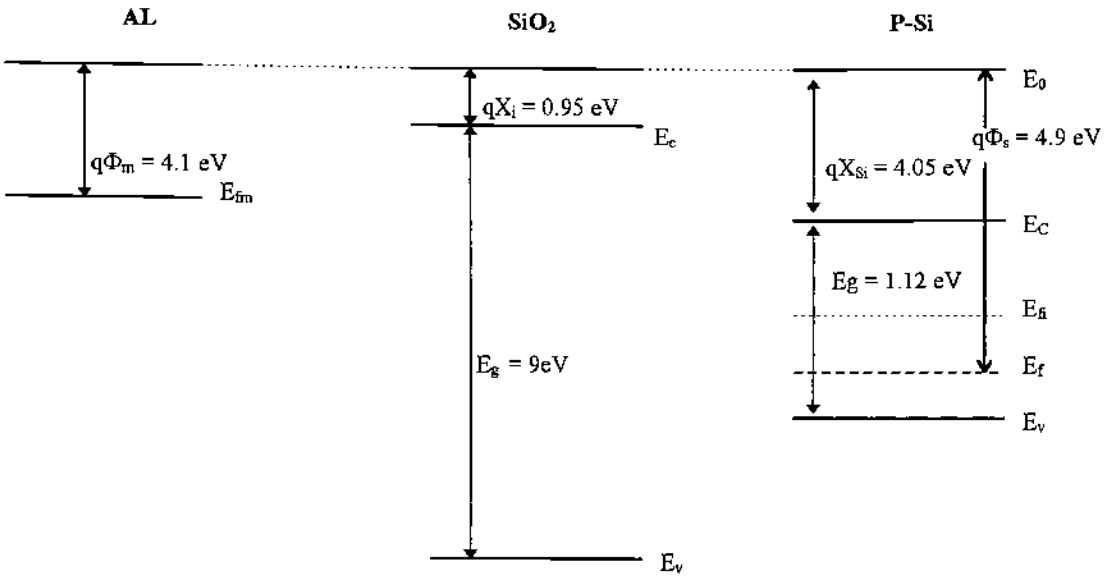


fig. 2.1.3 Metal, Oxide, and Semiconductor band diagrams

The ***work function*** being the energy required to move an electron from the Fermi level (E_F) to the Vacuum level (E_0) in a given material. Here E_0 refers to the ***Vacuum level*** which is a continuous function of position, and E_f refers to the ***Fermi level*** which can be thought of as the average energy for the valence electrons, and has an occupation probability of 1/2. In reality the ***Fermi level*** corresponds to the ***Fermi energy*** (defined as the energy in a

material below which all electron states are filled), but thinking of it in this manner reduces the complexity of the explanation. Before contact the ***Fermi level*** is different for all three materials, with respect to E_0. When the materials are placed in contact with each other and allowed to reach equilibrium (electrical contact is also made between the Al and P-type Silicon), the Energy band diagram is altered to the following configuration:

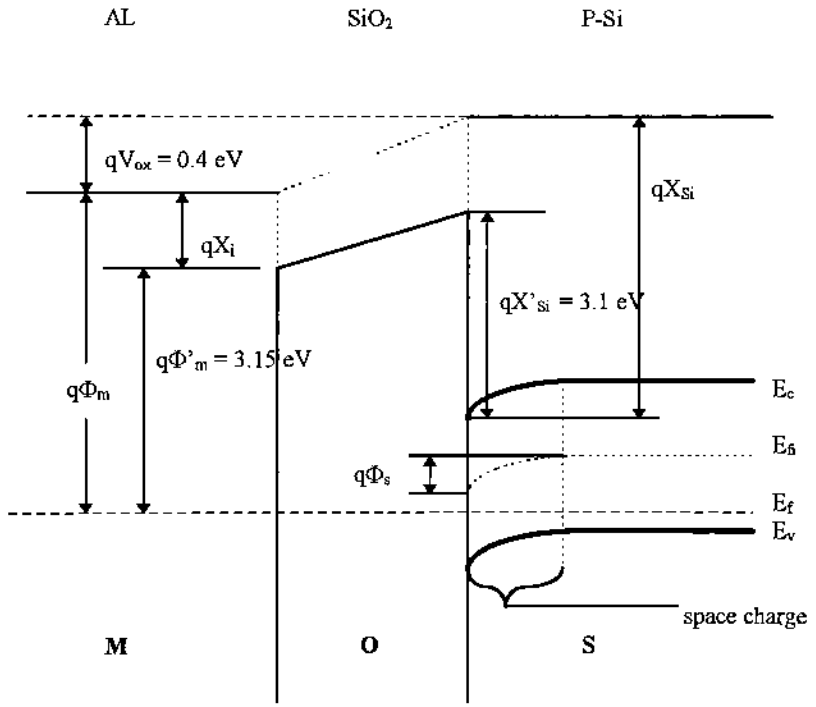


fig. 2.1.4 MOS band diagram

The electrons move from the material in which they posses a higher average energy (Aluminum) to a lower energy location (P-type Si). Since an electrical contact had also been made between the Aluminum and P-type Silicon, negative charge in the form of electrons transferred into the semiconductor because the work function for Al is 0.8 eV less than that of the semiconductor. This resulted in a thin layer of positive charge (equal in magnitude to the lost electrons) in the Aluminum at the Al-SiO_2 interface, and a corresponding accumulation of negative charge in the semiconductor at the SiO_2/P-type interface. It should be noted that the SiO_2 layer is assumed to be neutral in this ideal example; in reality it would contain a certain amount of positive charge. Since the Semiconductor is P-type, the negative charge results from the exposure of the ionized acceptor atoms as the majority carrier holes are repelled from the surface by the positive charge layer in the Aluminum. This energy difference corresponds to a drop in voltage of 0.4 eV, which divides itself across the SiO_2 and space charge regions. The energy bands for the two materials have correspondingly "bent" in response to this

voltage drop, with the exception of E_f which is continuous through all three materials (it must be constant throughout a system at equilibrium). The difference between E_F and E_i at the semiconductor surface is the ***surface potential*** : Φ_s. One result of this constant E_f with respect to the band bending, is that the surface of the P-type semiconductor now appears to be less P-type and more N-type. This effect is important because the surface of the semiconductor can be altered from its original type by the application of a suitable voltage to the Aluminum layer.

Applying a larger positive voltage to the Aluminum will cause more of the space charge layer to be exposed in order to balance the energy difference. The space charge layer can only be exposed to a certain thickness before inversion sets in, which is dependent on the doping level in the semiconductor material. This thickness, referred to as X_{dmax}, can be written in a form similar to that of a one-sided pn junction:

$$X_{dmax} = ((2\ \varepsilon_S\ \Phi_S)/(q\ N_a))^{1/2} \qquad (2.1.1)$$

where ε_S is the permittivity of the semiconductor and N_a is the doping level of the semiconductor. Larger positive potentials cannot be balanced by the maximum space charge thickness, and cause electrons (from the substrate and thermally generated in the space charge region) to accumulate at the semiconductor surface. When E_f at the surface is far above E_i, to the point where the surface potential is equal to $2(E_f - E_i)$ in the bulk (original spacing - no band bending), the electron concentration at the semiconductor surface will equal the hole concentration in the bulk of the semiconductor. The energy band diagram would now look like (fig. 2.1.5):

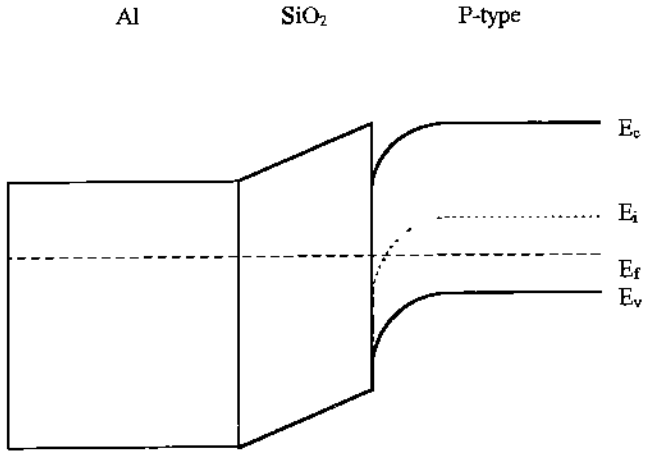


fig. 2.1.5 MOS band diagram at $\Phi_{SURFACE} = 2(E_F - E_i)$

This condition is known as the ***threshold inversion point*** and the applied voltage that creates it is called the ***threshold voltage***. Applying a negative voltage (with a magnitude less than 0.4 volts) will decrease the space charge width and decrease the degree of band bending. When the magnitude of the negative voltage is equal to 0.4 volts the system will have reached the condition of flat band, where no band bending or space charge layer exist:

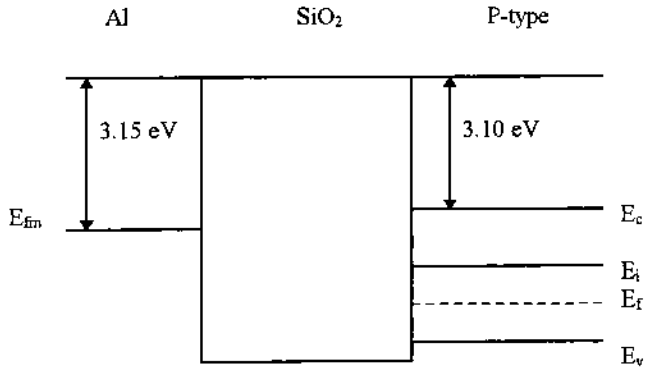


fig. 2.1.6 MOS band diagram at $V_{FLATBAND}$

Negative voltages greater in magnitude than 0.4 volts will allow holes to accumulate at the surface and cause the energy bands in the semiconductor to bend upwards (fig. 2.1.7):

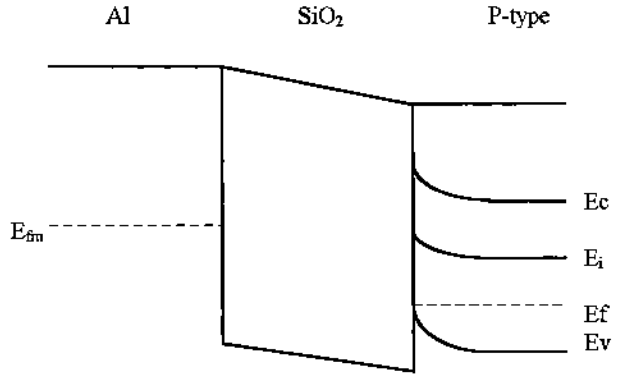


fig. 2.1.7 MOS band diagram for $V_{APP} < -0.4$

This basic knowledge of the behavior and operation of the MOS capacitor can now be applied to the CID pixel structure to provide a simplified understanding of its operation. As was previously stated, CID based arrays are normally fabricated on N^+ type epitaxial layers. The behavior will therefore be slightly different than the previously defined MOS capacitor; positive voltages will cause majority carriers (electron) to accumulate at the semiconductor surface, while negative voltages will expose the space charge region (depletion) and cause minority carrier (holes) inversion. In addition, the N^+ epitaxial region is positively biased to create a reverse biased p-n junction underneath each pixel. Placing a large negative potential (the epi layer is biased positive) on both electrodes would result in the formation of space charge regions (i.e.: potential wells) under both polysilicon electrodes:

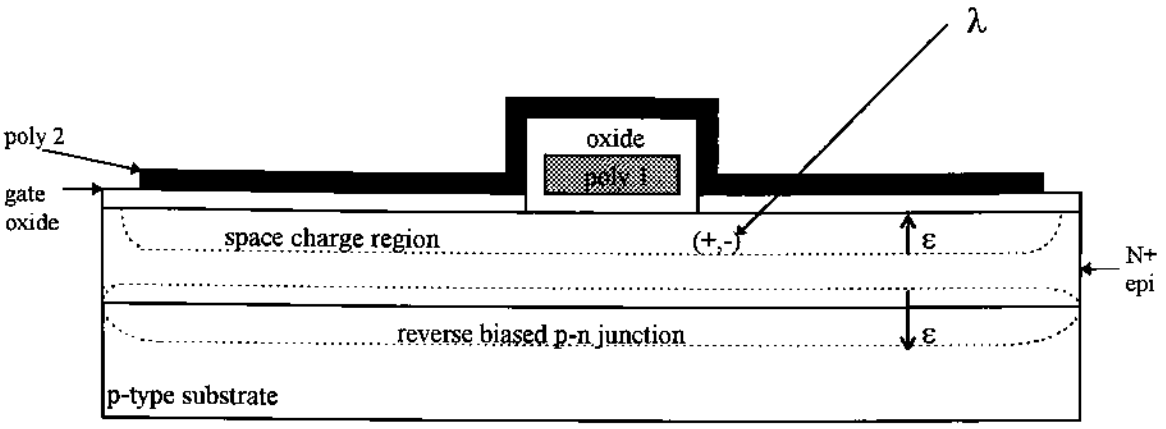


fig. 2.1.8 Horizontal view of CID

Photons, which pass either through the thin gate oxide into the bulk or through the polysilicon gate(s) into the space charge region, generate electron-hole pairs with the holes then being stored in the potential wells. The reverse biased p-n junction in each pixel serves to protect them from the effects of ***blooming***; the condition where a sufficient number of minority carriers generated in one pixel contaminate adjacent pixels. If more holes are generated in each pixel than the potential well can hold, the excess will escape only to diffuse into the p-n junction and swept into the substrate bulk.

Arrays with pre-amplifier structures connected to each row (poly 2 electrode) allow the column electrode (poly 1) to exist as a continuous structure over the column length, and will bias the column more negative than the rows to create a "deeper" potential well for charge storage. Examination of two readout techniques, ***non destructive readout*** and ***destructive readout***, provides an understanding of logic behind these concepts. Starting with both electrodes negatively biased (column bias larger than row bias) and sufficient charge in the potential wells, the device is observed to be in (a) accumulation (i.e.: inversion):

"sense pad"

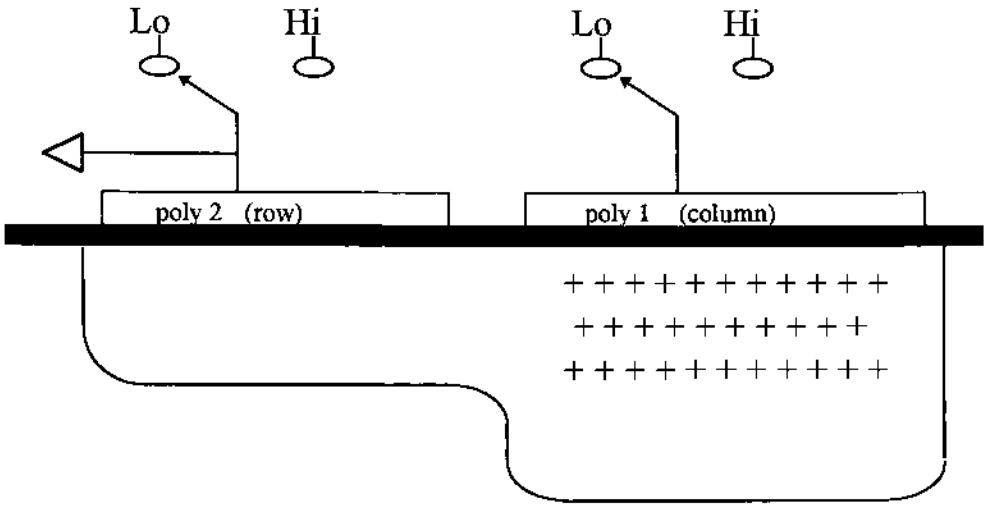


fig. 2.1.9 CID in accumulation mode

The more negatively biased column has a "deeper" potential well beneath it, where the collected charge then accumulates. Next, the sense pad is allowed to float unbiased while its potential is read; this is known as (b) "zero level" sense:

"sense pad"

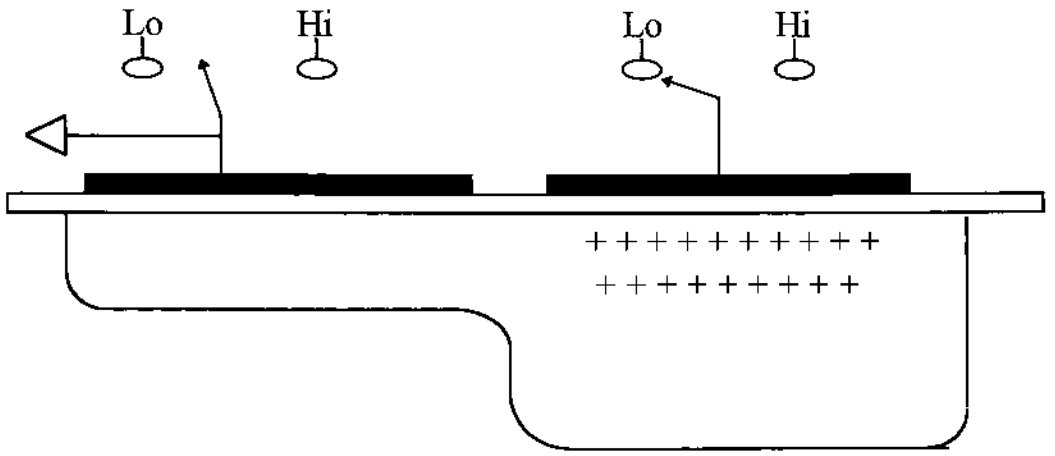


fig. 2.1.10 Zero level sense

After reading the "zero level" potential a positive bias is applied to the column electrode (high), which causes the potential well beneath it to collapse and injects the stored charge into the remaining well under the row (sense) electrode:

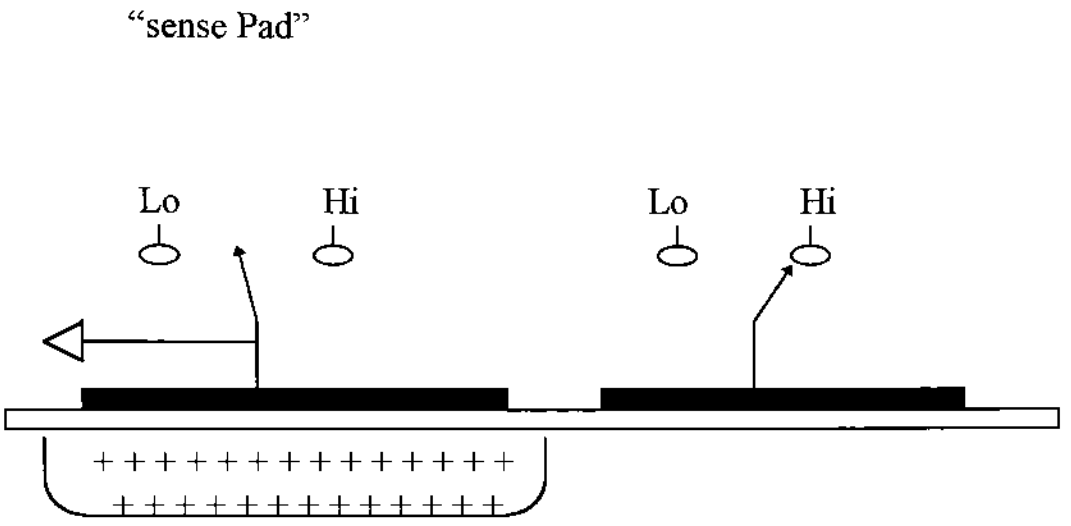


fig. 2.1.11 CID in signal sense

This is known as (c) "signal" sense. The appearance of charge under the row (sense) electrode causes a change in its potential, which corresponds to the amount of stored charge injected from the potential well under the column electrode (V = Q/c). By reading the shift in the voltage over the row electrode, the amount of photogenerated charge in the well can be inferred.

The combination of steps (a), (b), and (c) are known as ***non destructive readout*** (NDRO) since at this point the column electrode can be driven low to form a deeper potential well and start the cycle over. If ***destructive readout*** (DRO) is desired, a large positive potential must be applied to the row electrode as well. This step, referred to as (d) ***injection***, collapses the potential well and injects the stored charge into the substrate:

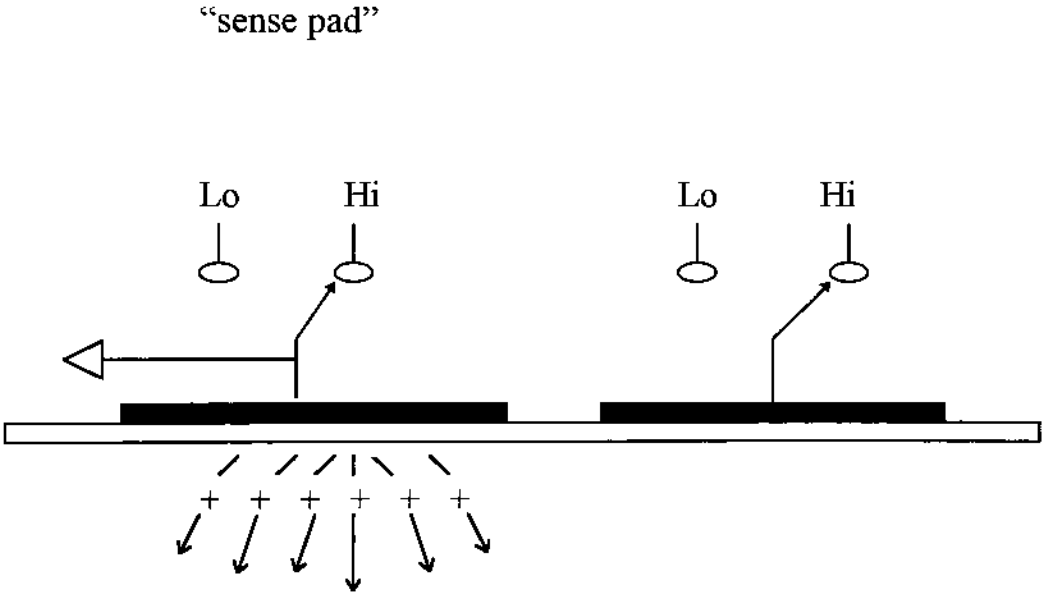


fig. 2.1.12 CID in injection mode

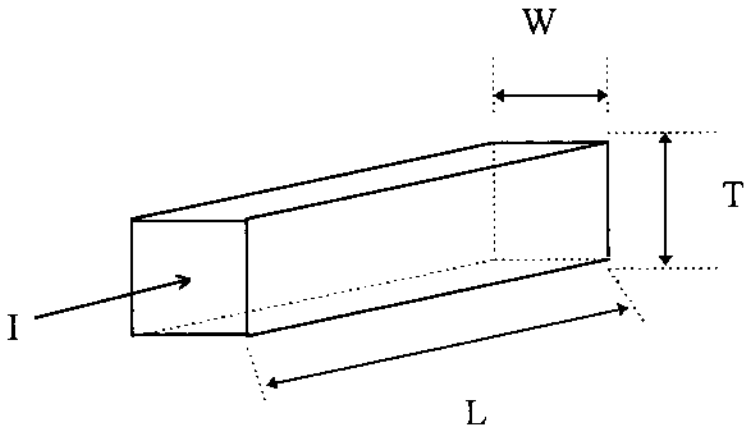
The injection pulse(s) must be of sufficient duration and magnitude in order to eliminate charge from the pixel as efficiently as possible. Although it is possible to use a variation of the injection step (d) as a method for reading stored charge (as much older designs have done), using NDRO with or without DRO appears to be the most useful way to exploit the advantages of a CID-based array.

2.2 Parameter Extraction Techniques:

Evaluation of the double level polysilicon P-well CMOS process consisted of the same techniques and structures used to evaluate the single level polysilicon P-well CMOS process, from which it was based. This included sheet resistance measurements using the Van Der Pauw resistor, contact resistance measurements using the Cross bridge Kelvin resistor, and the extraction of several characterization parameters from the (enhancement mode) MOS transistor structures. All measurements were made using the standard factory P-well CMOS test programs in conjunction with the HP-4145 Semiconductor Parameter Analyzer, the Rucker & Kohls 681A semiautomatic wafer prober, and the Keithly model 7001 switch system.

Fabricated Semiconductor layers that have been doped by ion implantation and/or diffusion, will posses non-uniform doping profiles. Resistivity is a function of doping concentration *and* the depth of the diffusion, which complicates device and circuit design. However, utilizing the parameter of *sheet resistance* can simplify the process, since it removes the need for understanding the specifics of the diffusion profile. Considering a

resistor with respect to all three dimensions can help to explain the concept of sheet resistance, along with its benefits. A uniformly doped block of material can be thought of as a resistor with a resistance value of ***R*** ohms:



$$R = \rho L / (T \cdot W) \qquad (2.2.1)$$

fig. 2.2.1 resistance as a function of three dimensions

Where ***R*** can be expressed in terms of the blocks dimensions with the addition of the materials *Resistivity*; **ρ**. Resistance is inversely proportional to the cross-sectional area of the resistor, but is proportional to the Resistivity.

The expression for resistance can be rewritten as:

$$\mathbf{R = (\rho / T) / (L / W) = R_{sh} (L / W)} \qquad (2.2.2)$$

Where $\mathbf{R_{sh}}$ is the *sheet resistance* of the material, a variable that is expressed in terms of ohms per square. Redefining the (L/W) ratio in eq. (2.3.2) as the number of "squares", specific value resistors can now be designed in materials of known sheet resistance by defining only a length and width.

To accurately measure the sheet resistance of a material requires using a ***Van Der Pauw*** resistor:

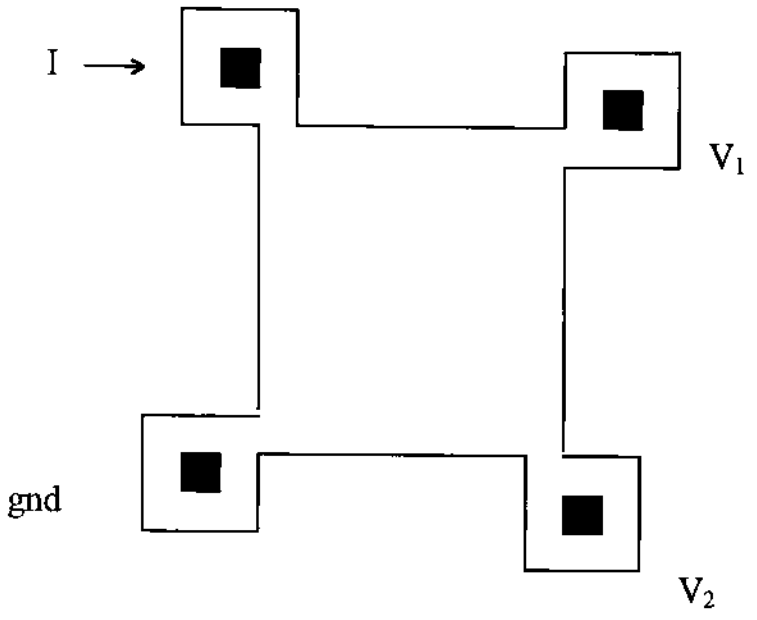


fig. 2.2.2 The Van Der Pauw resistor

By forcing a current (**I**) through the structure to ground (GND) and reading the voltage drop across it (V_1 - V_2), the sheet resistance can be calculated using:

$$\mathbf{R_{sh}} = ((\mathbf{V_1} - \mathbf{V_2}) / \mathbf{I}) \bullet (\Pi / \mathit{ln}\ 2) \qquad (2.2.3)$$

For the most accurate $\mathbf{R_{sh}}$, values should be extracted from a plot of current (**I**) vs. voltage (**V**) where the difference in voltage remains constant while the current linearly increases. Sheet resistance measurements were made in this manner for both diffusion (P-well, N+, and P+) and thin film (metal, N- poly, and N+ poly) Van Der Pauw structures.

Contact resistance ($\mathbf{R_{co}}$) is the physical parameter used to characterize the incremental resistance of the micron-scale metal-semiconductor contacts. Contact resistance is generally determined by the extraction of *the contact size independent parameter* ρ_c (expressed in units of mho/um^2) from electrical measurements performed on the **cross-bridge Kelvin resistor (CBKR)** structure:

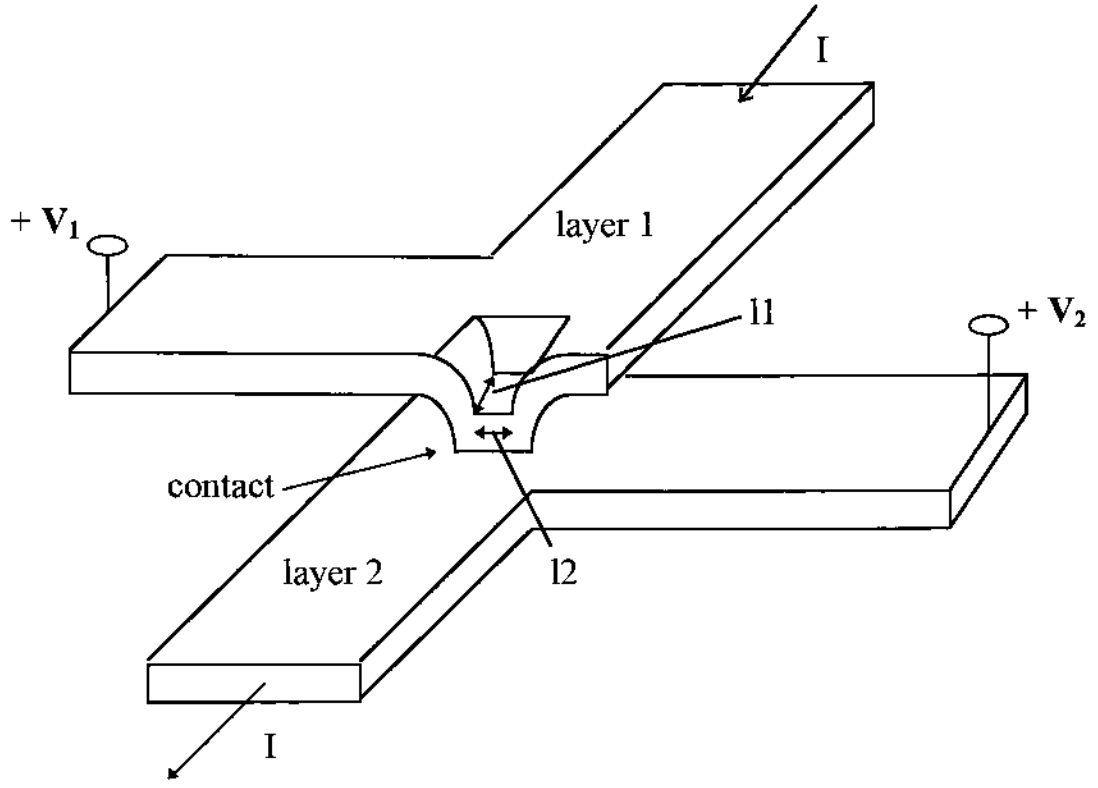


fig. 2.2.3 The cross-bridge Kelvin resistor

The CBKR structure is used to determine the contact resistance produced when current is passed between two layers. From this structure either the contact resistance associated with a specific sized contact opening $\mathbf{R_{co}}$ or the

contact size-independent parameter ρ_c can be calculated. This can be accomplished using either the graphical or direct method, with the direct being preferred at RIT. While the graphical method is the most accurate of the two, it requires at least ten sets of contacts that vary in length (l) along with at least two different sizes of *diffusion overlaps* (δ) for each length:

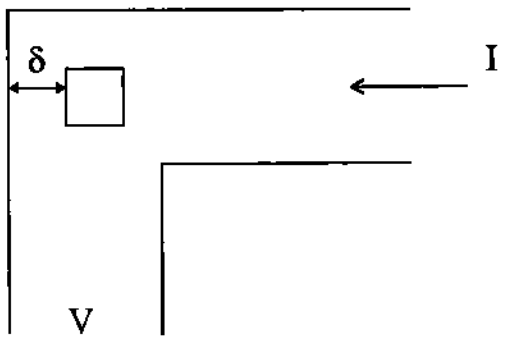


fig. 2.2.4 diffusion region overlap

The values of $\log_{10}$ ($\mathbf{R_{CBKR}/R_{sh}}$) must then be plotted versus $\log_{10}$ ($1/\delta$) on a set of universal CBKR curves (see appendix). The universal resistance curve

which gives the closest match will thus indicate the contact resistance. Although less accurate than the graphical method, the direct method is much faster since it allows for both R_{co} and ρ_c to be determined at each CBKR structure. In this method a current of known magnitude is forced through the CBKR structure, and the voltage is measured at V_1 and V_2. The measured difference in voltage is then used to calculate either the contact resistance for a specific sized opening R_{co} or the size-independent parameter ρ_c with a modified version of Ohm's law;

$$R_{co}\,(\Omega) = (V_1 - V_2) / I \qquad (2.2.4)$$

$$\rho_c\,(\Omega/um^2) = ((V_1 - V_2) / I) \cdot (1 / (l1 \bullet l2)) \qquad (2.2.5)$$

where (l1) and (l2) indicate the length and width of the contact opening. The measured structures were all designed with $\lambda = 4\mu m$ and consisted of $8\mu m$ x

8μm sized contacts for the Al-poly1 and Al-P^+ CBKR's, while the Al-N^+ CBKR possessed a 4μm x 4μm sized contact.

Evaluation of the MOS transistors required that several parameters be extracted from the NMOS and PMOS structures. NMOS transistors possessing a gate length (L_g) of 6μm and a channel width (W_c)of 32μm were used with PMOS transistors of gate length 16μm and 32μm channel width:

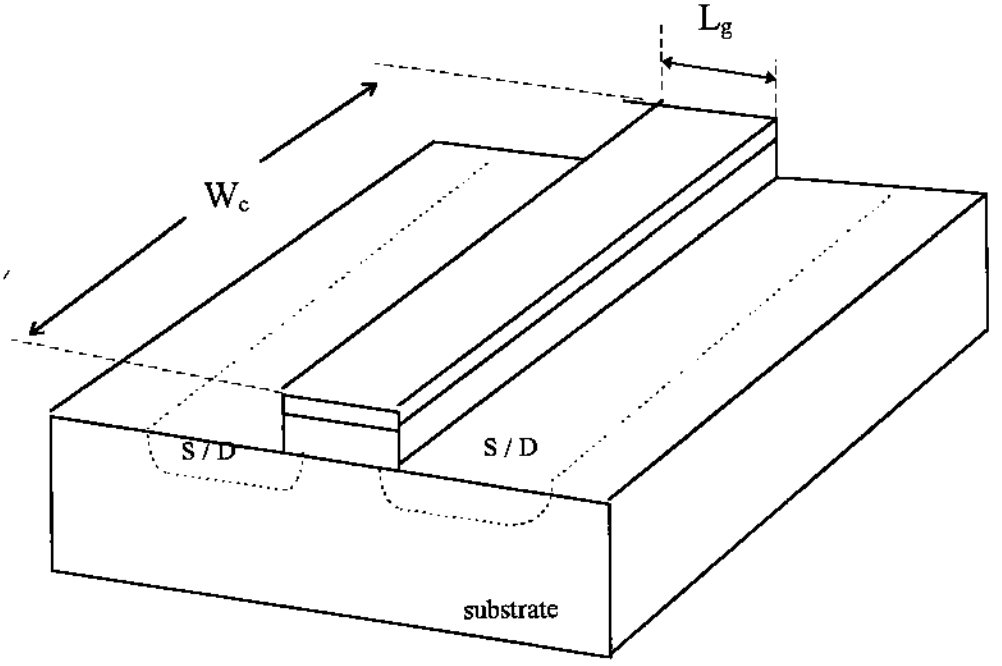


fig. 2.2.5 transistor gate length L_g and channel width W_c

to extract values for *threshold voltage* $\mathbf{V_T}$, the *channel length modulation parameter* $\boldsymbol{\lambda}$, *transconductance* (i.e.: gain) $\mathbf{G_m}$, the *minimum sub-threshold current* $\mathbf{I_{submin}}$, the *maximum sub-threshold current* $\mathbf{I_{submax}}$, the *sub-threshold slope* $\mathbf{ST_S}$, and evaluate the *body effect*.

The *threshold voltage* ($\mathbf{V_T}$) is the applied gate voltage that initiates conduction between the source and drain in the MOS transistor. Referring back to the energy band diagrams of section 2.1, it can also be thought of as the applied gate voltage required to invert the surface of the semiconductor beneath it. It is dependent on processing factors, and can be generally expressed as:

$$\mathbf{V_T = ((qN_a x_{dt}) - Q_{SS}')\bullet(t_{ox}/\varepsilon_{ox})) + \Phi_{ms} + 2\Phi_{fp}} \qquad (2.2.6)$$

where N_a is the substrate doping, x_{dt} is the maximum space charge thickness, Q_{ss}' is equivalent gate oxide charge, tox is the thickness of the gate oxide, ε_{ox} is product of the SiO_2 dielectric constant (3.9) and the permittivity of free space ($8.85e^{-12}$ F/m), Φ_{ms} is the metal-semiconductor work function difference, and $2\Phi_{fp}$ is the surface potential at threshold inversion. The threshold voltage is extracted from a MOS device by using a conductivity curve, which plots the gate voltage (V_g) versus the drain current (I_d) for drain voltages (V_d) less than $2\Phi_{fp}$. The absolute drain voltage is fixed at an acceptably low level (usually 0.05 to 0.1 volts) and the linear portion of the conductivity curve is extrapolated to $I_d = 0$ volts:

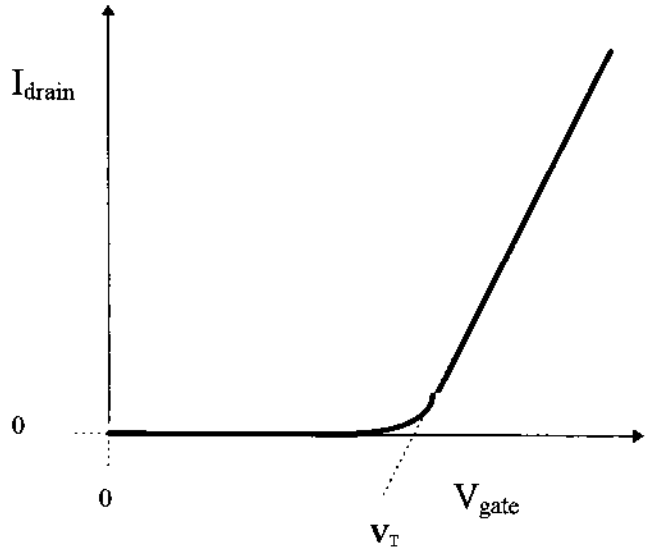


fig. 2.2.7 typical conductivity curve to extrapolate threshold voltage

This point, the intercept the X-axis, is defined as the *threshold voltage* $\mathbf{V_T}$ for the MOS transistor.

The *channel length modulation parameter* λ is equal to the slope of the $\mathbf{I_D}$-$\mathbf{V_D}$ conductivity curve in saturation, divided by the current at the onset of saturation. It can be thought of as an indication of the extent to which the

drain-to-source voltage impacts the *effective channel length*. Since the source-drain regions extend under the transistor gate, the actual channel length is somewhat less than the length of the gate. Add this to the fact that space charge regions between the source-drain and channel (formed from reverse biasing with respect to the substrate) also reduce the actual channel length, and the importance of *effective channel length* along with λ becomes obvious. The value of λ for a MOSFET can be determined from its $\mathbf{I_D}$-$\mathbf{V_D}$ conductivity curve (done at RIT for a specific gate voltage). The slope of the curve in saturation mode is divided by the current at the onset of saturation, a point corresponding to a drain voltage ($\mathbf{V_{Dsat}}$) equal to the difference of gate voltage ($\mathbf{V_G}$) minus the threshold voltage ($\mathbf{V_T}$):

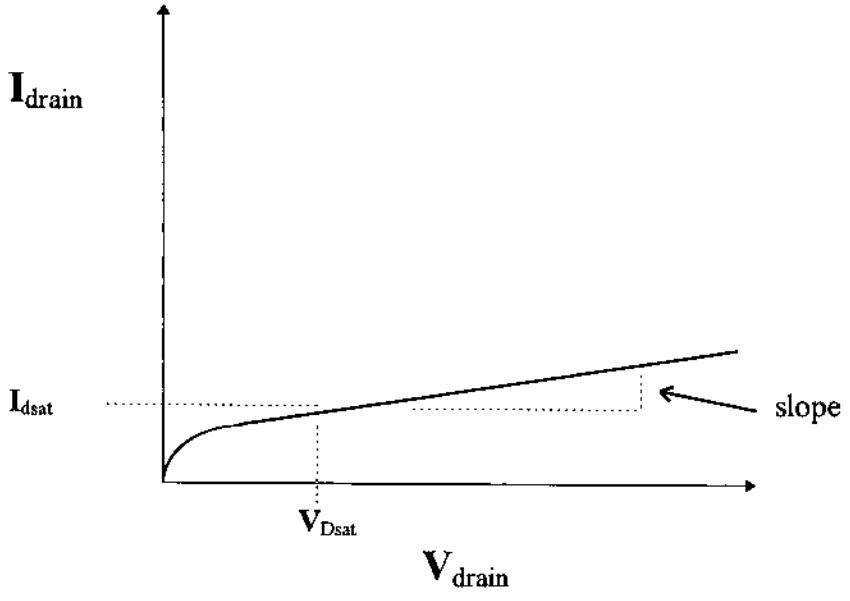


fig. 2.2.8 I_D-V_D conductivity curve for calculation of λ

As measured, λ will be in units of 1/volts.

The *transconductance* $\mathbf{G_m}$ of a MOSFET can be thought of as the transistor "gain", since it is defined as the change in drain current ($\mathbf{I_D}$) with respect to the corresponding change in gate voltage ($\mathbf{V_G}$). Transconductance is dependent on device geometry, threshold voltage, and carrier mobility. In the non-saturation region it is a linear function of $\mathbf{V_{DS}}$ but independent of $\mathbf{V_{GS}}$,

while in the saturation region it is a linear function of V_{GS} and independent of V_{DS}. In addition G_M can be plotted on an I_D-V_G conductivity curve, and measured at the peak value:

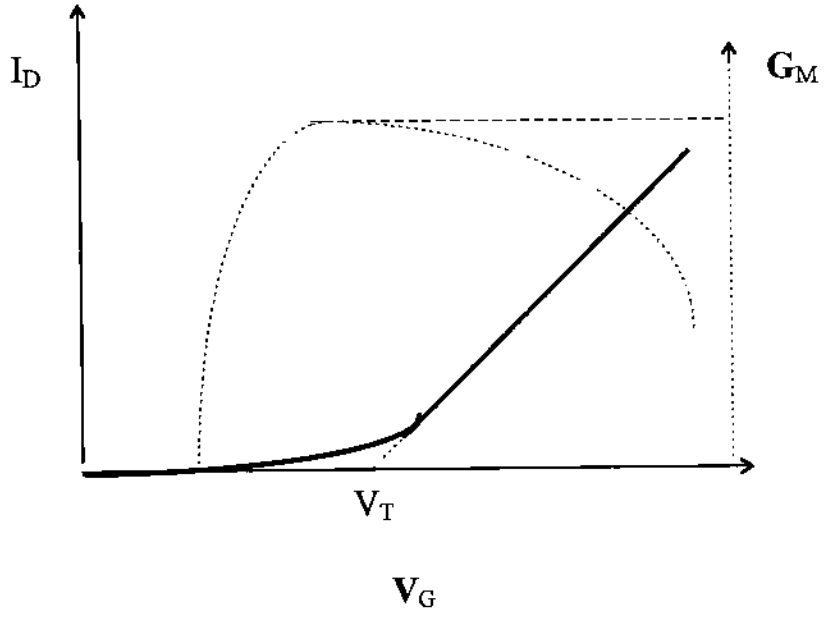


fig. 2.2.9 Plot of G_M on I_D-V_G conductivity curve

Finally, the parameters of *subthreshold slope* $\mathbf{ST_S}$, *minimum subthreshold current* $\mathbf{I_{Dsubmin}}$, and *maximum subthreshold current* $\mathbf{I_{Dsubmax}}$, are all used to describe the behavior of free charges in the channel for voltages less than $\mathbf{V_T}$. The basic model for the MOS transistor assumes no carriers exist in the channel until the threshold voltage is reached on the gate. Although a valid assumption for most conditions it fails at voltages approaching the threshold voltage, since the minority carrier density in the channel changes exponentially with respect to channel voltage. Thus, significant currents can exist at conditions between weak inversion and strong inversion (i.e.: $< \mathbf{V_T}$). Since a MOSFET is not considered to be "on" until the channel conducts a microamp of current ($1e^{-6}$ Amps), the *maximum subthreshold current* $\mathbf{I_{dsubmax}}$ should not exceed this value. The *minimum subthreshold current* $\mathbf{I_{dsubmin}}$ should also be significantly less than a microamp to result in an acceptable value of *subthreshold slope* $\mathbf{ST_S}$. *Subthreshold swing* **SS** is defined as the change in $\mathbf{V_G}$ that produces a decade increase in the subthreshold current:

$$\mathbf{SS} = \Delta \mathbf{V_G} / \Delta \mathbf{log}\ \mathbf{I_{Dsub}} \qquad (2.2.7)$$

A small value for the subthreshold swing is desirable, since it implies tight control of the channel current by the gate. The subthreshold swing conductivity curve is normally plotted with $\mathbf{I}_{Dsub}$ on a logarithmic Y-axis and $\mathbf{V}_G$ on a linear X-axis. Thus, a large *subthreshold slope* $\mathbf{ST}_S$ would indicate good control between the "on" and "off" states of the transistor, and a significant difference between $\mathbf{I}_{Dsubmin}$ and $\mathbf{I}_{Dsubmax}$ would imply a sharp transition between the "on" and "off" states.

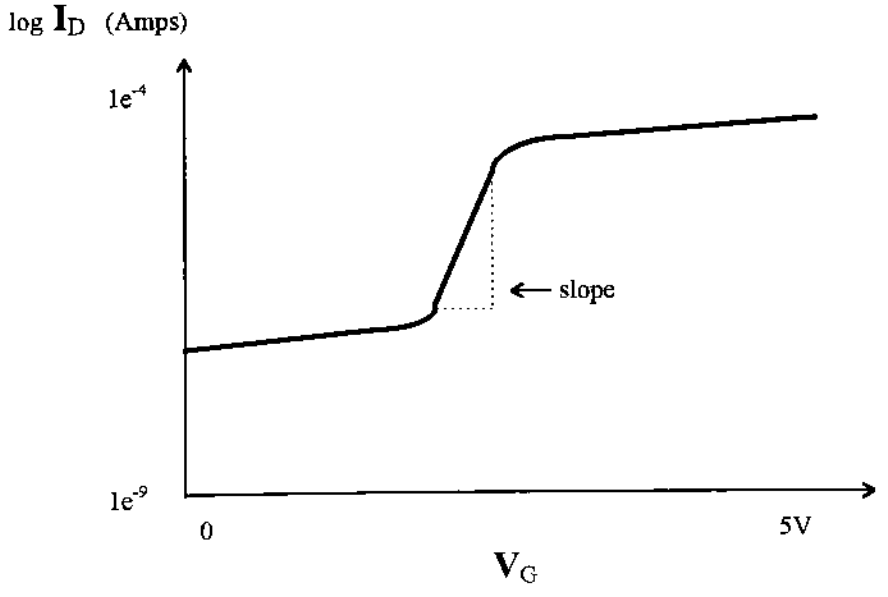


fig. 2.2.9 subthreshold conductance cure for NMOS

Subthreshold slope, the *minimum subthreshold current*, and the *maximum subthreshold current* are all measured from the same logarithmic conductivity plot (for a MOSFET) by sweeping the gate voltage in small steps with a slight bias applied to the drain. This is similar to the method of determining $\mathbf{V_T}$ except that the steps for $\mathbf{V_G}$ are smaller.

III. Procedure:

3.1 CMOS Process Description:

CMOS (Complementary **M**etal **O**xide **S**emiconductor) process technology evolved in the mid-1970's to reduce power dissipation problems, and has become the dominant process technology today [6]. The specifics of CMOS processing are beyond the scope of this thesis, so the explanation and background will be kept general.

As the era of very large scale integration (VLSI) emerged, the dominant process technology was NMOS (**N**-channel **M**etal **O**xide **S**emiconductor). This was due to it's speed advantage over PMOS, the high functional packing density which it allowed, and the inexpensive nature of fabrication costs [7]. However, it did possess a significant disadvantage with respect to power consumption. An NMOS logic circuit will draw a steady current whether a signal is propagating through it, or it is in standby mode. While the large current demand was not an issue for most applications, the

problem of power dissipation was. Conventional plastic packaging limited the maximum power dissipation of a circuit to approximately 1.5 watts [8], while more expensive ceramic packaging was required for higher power densities.

With the functional packing density of integrated circuits rapidly increasing (i.e.: Moore's law), a low power solution was required. The solution to this dilemma was CMOS technology, which involved the fabrication of both n-channel and p-channel transistors on the same chip. CMOS allowed for both a decrease in the power dissipation along with simplifying the construction of some logic gates. For example, a CMOS inverter consists of only an n-channel transistor and a p-channel transistor. Power will only be consumed when it switches logic states, and a high impedance path will exist between the voltage supply and ground when no signal propagates through it [9]. However, CMOS was not without it's drawbacks. Problems with latchup and transistor isolation limited its applications to those which required low power dissipation and/or very high noise margins, until effective solutions to these problems were found [10].

Although many different forms of CMOS technologies exist today (twin well, N-well, P-well, quad well, and BICMOS), the variation utilized

for this thesis is the P-well type. This form evolved out of early process limitations and involves the formation of a p-type region, in which the NMOS transistors are subsequently constructed. As a result of forming the NMOS transistors in such a lightly doped (i.e.: ~10^{16} dopant atoms per cm^3) region, the carrier mobility in the NMOS transistors is not significantly affected.

The basic P-well, double level poly, single level metal process developed requires 10 mask levels, the first of which is referred to as the **well** mask (level 1). After a 5000 Angstrom "alignment" oxide is grown on the surface of the wafers, the well mask is exposed onto a photoresist coating on the surface of the wafers to define the locations where the p-type regions will be formed on the substrate (fig. 3.1.1). The photoresist protects the oxide over the other regions from a subsequent etch in a buffered HF acid solution, which exposes the silicon surface of the wafer. P-type dopants are then ion-implanted into the exposed silicon with the resist (and oxide) acting as a mask.

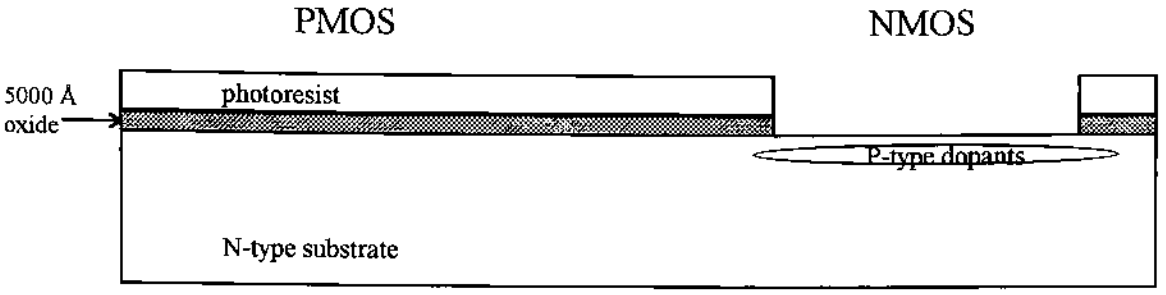


fig. 3.1.1 Mask level 1 after P-well implant

The resist is removed and the substrates are cleaned, then placed into an 1100^0 C furnace to drive-in the well. The initial part of the well drive is done in an Oxygen ambient which serves to oxidize the surface of the exposed well regions. After the well drive the oxide is etched off the surface of all wafers, leaving all well regions defined by a reduced step height in relation to the bulk silicon (fig. 3.1.2).

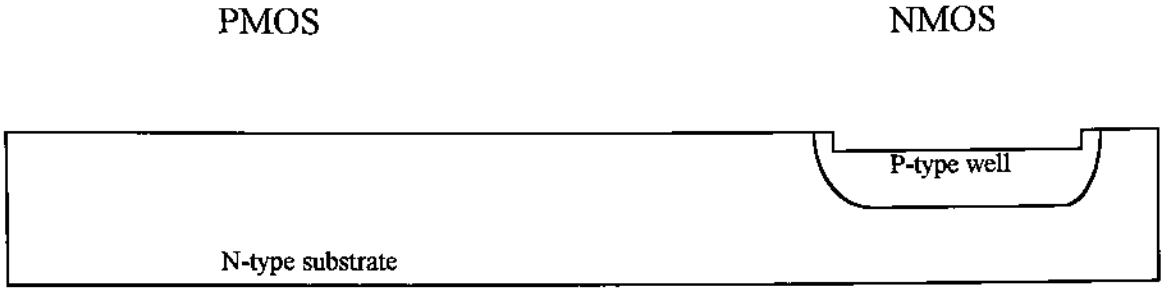


fig. 3.1.2 after well drive

Next, a thin (~ 500Å) pad oxide is grown on the wafers, followed by the deposition of a 1500Å Silicon Nitride layer. The next mask layer, the **active** (level 2), is exposed onto a photoresist layer to define the regions where both the n-channel and p-channel transistors are to be fabricated. This pattern is then transferred into the Silicon Nitride and pad oxide layers using a plasma etch step followed by a wet buffered oxide etch.

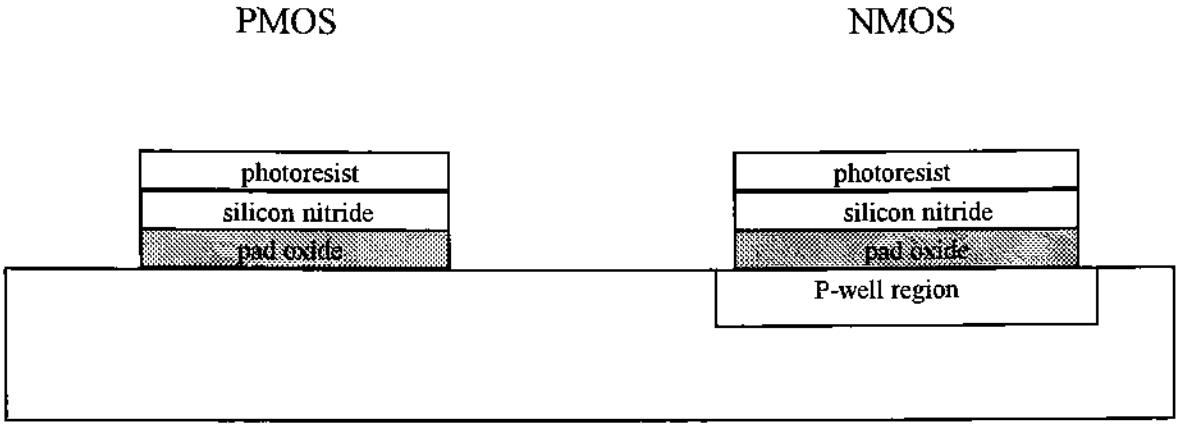


fig. 3.1.3 Mask level 2 after Nitride and oxide etch

The next mask, called the **channel stop** mask (level 3), defines in photoresist the region surrounding the well (and the edge of the active). P-type dopants are ion implanted there to increase their concentration and reduce the depletion effects of the field oxidation, which would otherwise lead to the formation of an N-type channel at the edges of the P-well.

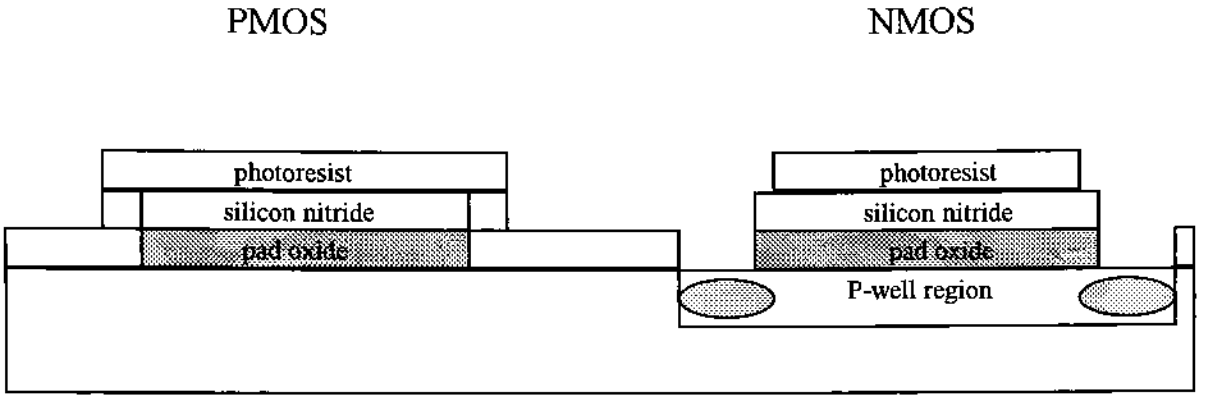


fig. 3.1.4 mask level 3 after channel stop implant

The photoresist is removed, the wafers are cleaned, and the field oxide is grown to isolate all active areas. Following oxidation, the Silicon Nitride and pad oxide layers are etched off, and a 1000 Angstrom "Kooi" oxide is grown (to decompose any residual nitride). Both threshold adjustment implants are then performed through this oxide. The threshold adjust implant for the p-channel transistors is performed as a blanket implant, while the one for the n-

channel transistors is a masked implant, defined in photoresist by re-exposing the **well** mask (level 4).

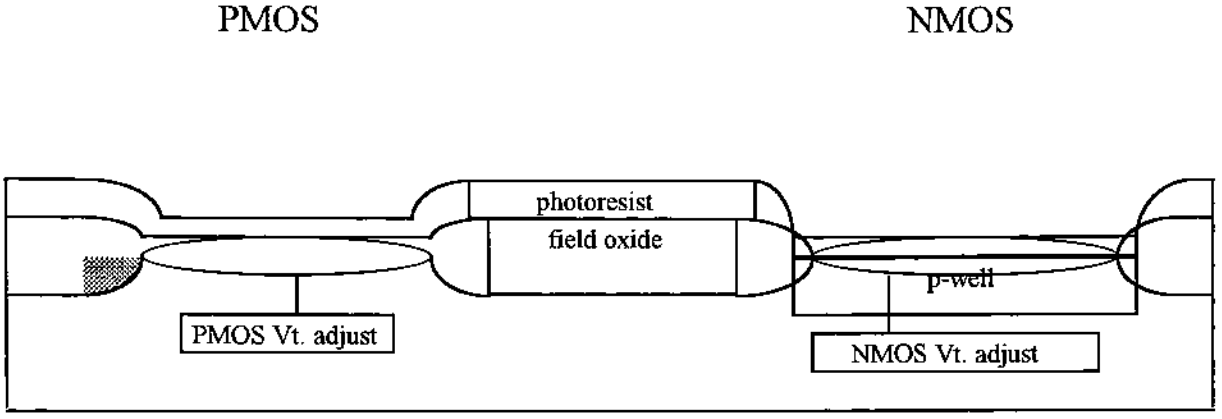


fig. 3.1.5 mask level 4 after NMOS VT implant

The photoresist is then removed, and the 1000 Angstrom "Kooi" oxide is etched off to expose bare Silicon over the active regions. The wafers are cleaned, and then the gate oxide is grown for the transistors. Polysilicon is then deposited over the wafers, and doped N^+-type using a spin on dopant.

The **poly1** mask (level 5) is then exposed in photoresist to define the gate region of the transistors, and subsequently etched into the polysilicon.

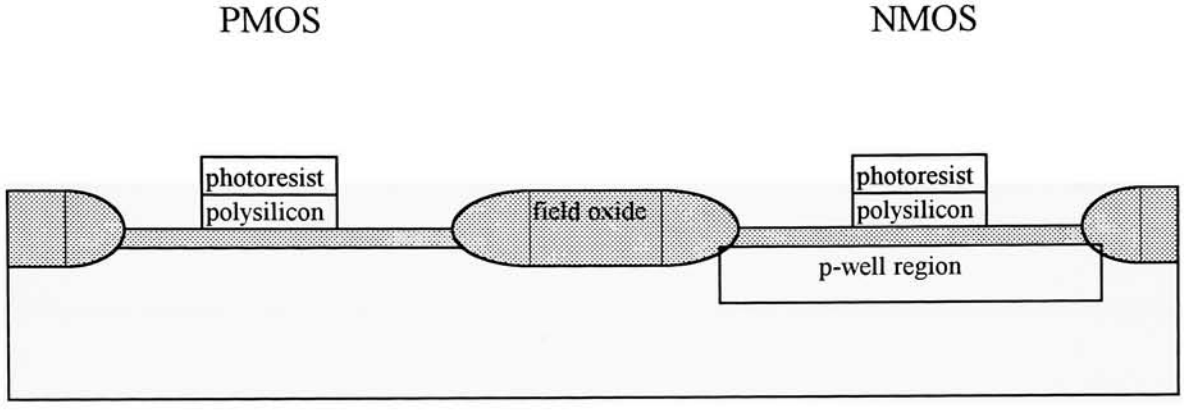


fig. 3.1.6 Mask level 5 after polysilicon etch

Up to this point no mention has been made with regard to the construction of a pixel (Imager) type of structure, which was the purpose of the thesis. This is because, with the exception of the gate dimensions, the pixel structure would look exactly like the PMOS transistor.

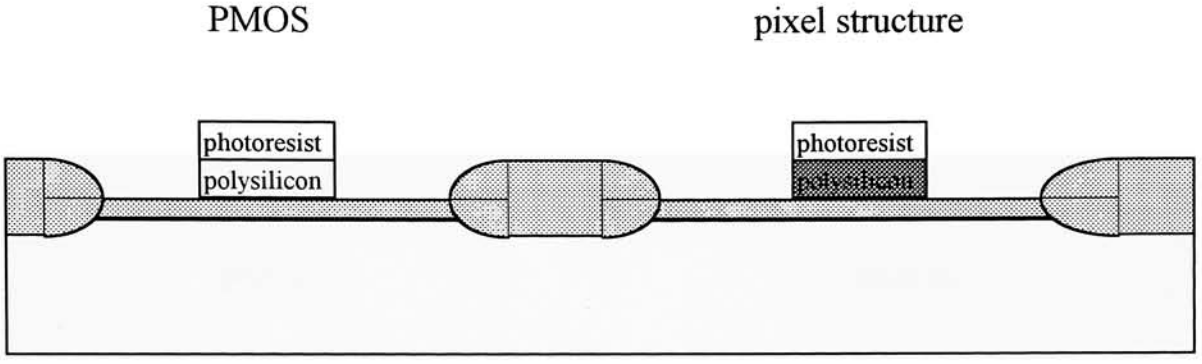


fig. 3.1.7 Pixel structure and PMOS transistor after polysilicon etch

The exposed gate oxide, which has been damaged during the patterning of the polysilicon gates, is etched off using a buffered HF acid solution. The wafers are cleaned, and then a second gate oxide is grown. This oxidation is needed to complete the pixel structure, but will also form an oxide on the first polysilicon layer that will insulate it from the second polysilicon layer. This second polysilicon layer is deposited, doped N^+-type with a spin on dopant,

and patterned using a photoresist layer exposed by the **poly2** mask (level 6). Since the second gate oxide and second polysilicon layer are only required to complete the pixel structure, the NMOS and PMOS transistors remain the same (as in the previous level), with the exception of an insulating oxide layer on the polysilicon gates.

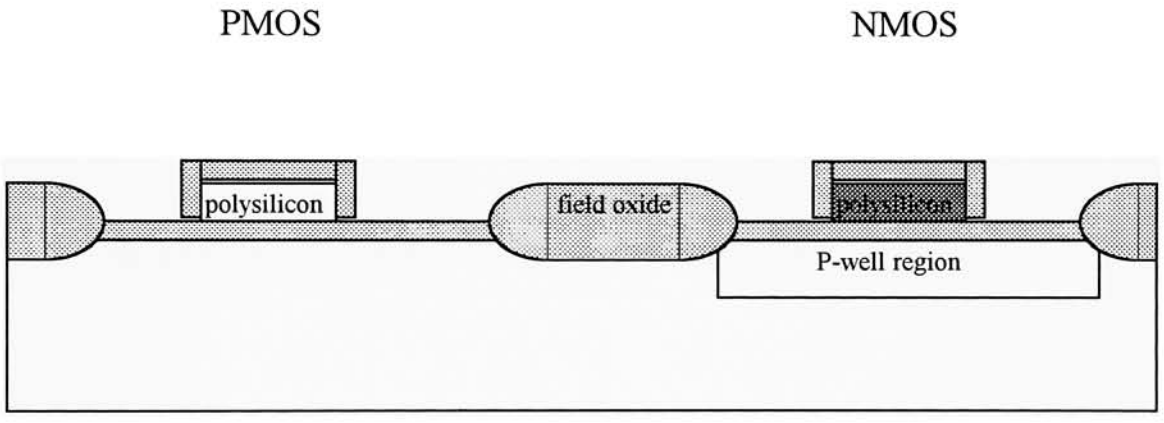


fig. 3.1.8 Transistors after polysilicon layer 2 etch

The pixel structure, however, will look remarkably different with respect to the PMOS transistor:

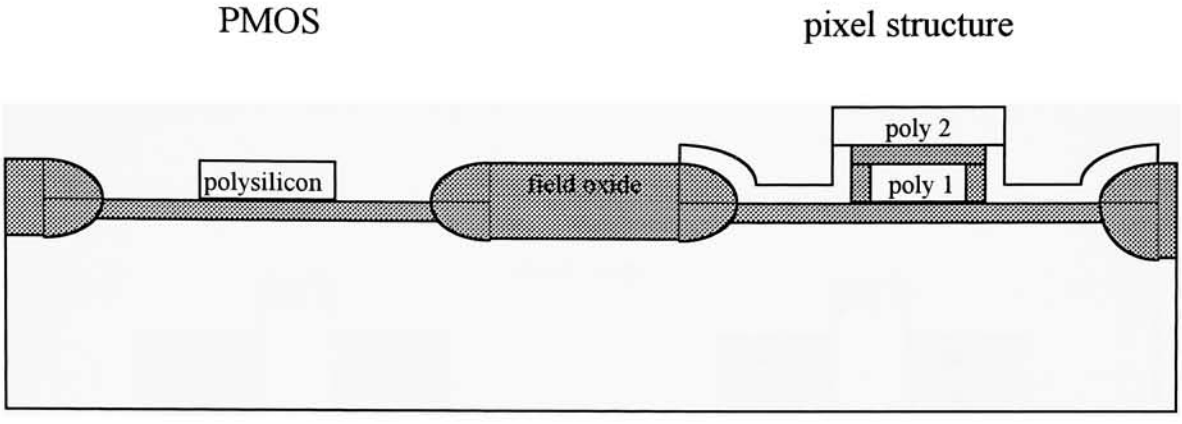


fig. 3.1.9 Pixel structure and PMOS transistor after second polysilicon etch

The pixel structure is now essentially complete, with the exception of the passivation layer (which is etched off its surface), and the metal layer(s) that contact both polysilicon layers. While difficult to comprehend when viewed as a cross-section, the completed pixel structure is easier to comprehend when viewed from the top:

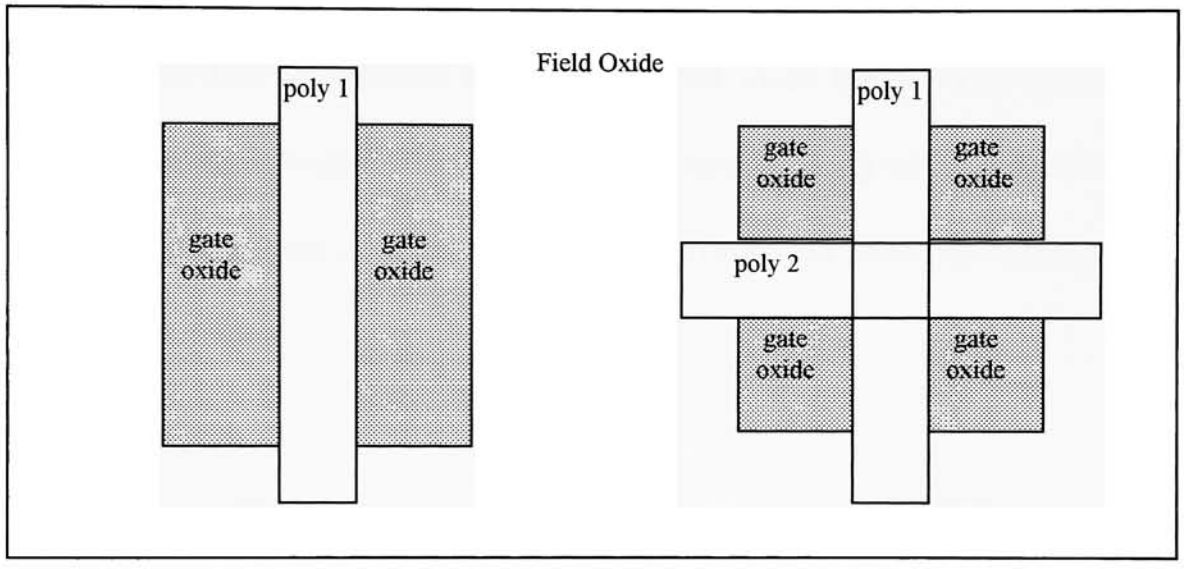


fig. 3.1.10 Top view of PMOS transistor and pixel structure

The pixel structure collects photogenerated minority carriers in potential wells formed under the polysilicon gates. Photons passing through the polysilicon gates and gate oxide will generate carriers that are stored in the potential wells, while carriers generated in the gate oxide regions will have to diffuse into the potential wells before they can be stored. With the pixel structure now essentially completed, the focus is shifted back to the transistors. A photoresist film is exposed using the **P+ s/d** mask (level 7) to define the source and drain regions on the PMOS transistors, along with contacts to the well regions. P-type dopants are then ion implanted to form the source/drains and well contacts.

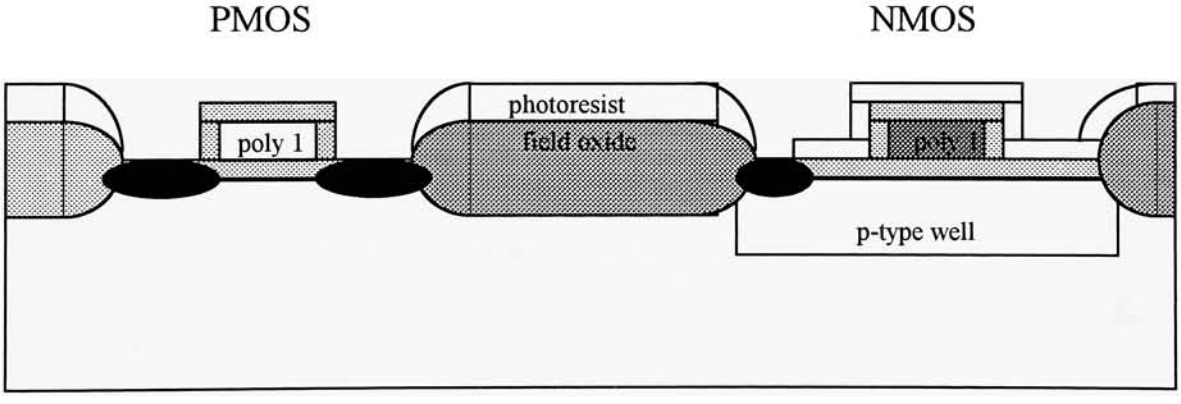


fig. 3.1.11 Mask level 7 after P+ S/D implant

The photoresist layer is removed, and a new photoresist coating is exposed using the **N+ s/d** mask (layer 8), to define the source and drain regions for the NMOS transistors and the substrate contacts. N-type dopants are then ion implanted to form these regions:

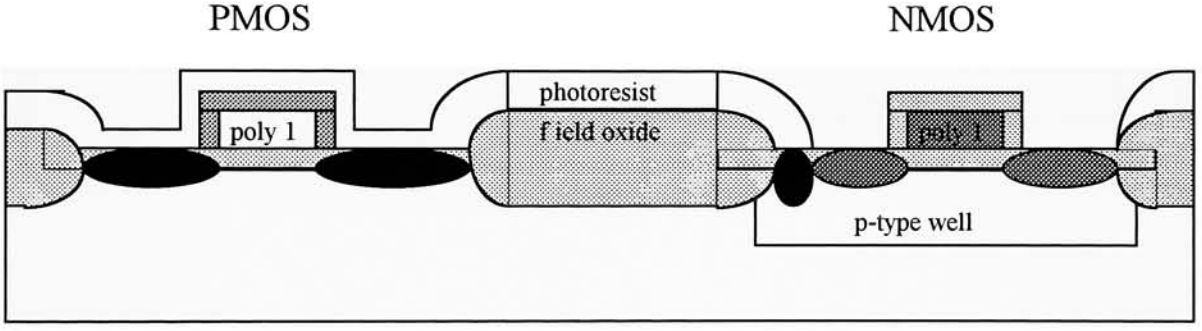


fig. 3.1.12 Mask level 8 after N+ S/D implant

The photoresist layer is then removed, and the wafers are cleaned before a 3000 Angstrom coating of LTO (Low Temperature Oxide) is deposited.

Following the deposition, the wafers are annealed to remove implant damage, activate the dopants, and densify the LTO film. A photoresist coating is then patterned using the **contact cut** mask (layer 9), and the exposed LTO film is etched in buffered HF acid to form contacts for the following metal layer.

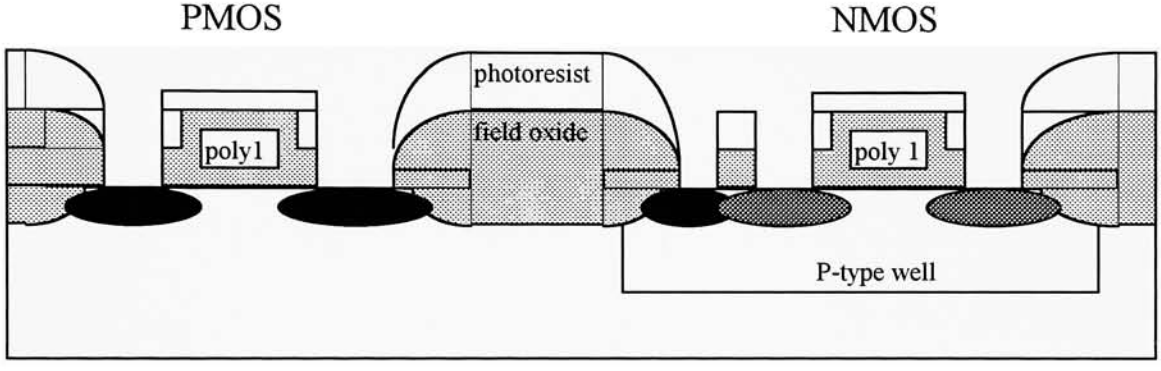


fig. 3.1.13 Mask level 9 after contact cut etch

Following the etch, the photoresist is removed and the wafers are cleaned before the Aluminum layer is deposited. The Aluminum is then patterned using a photoresist coating exposed with the **metal1** mask (layer 10), in conjunction with a phosphoric acid bath.

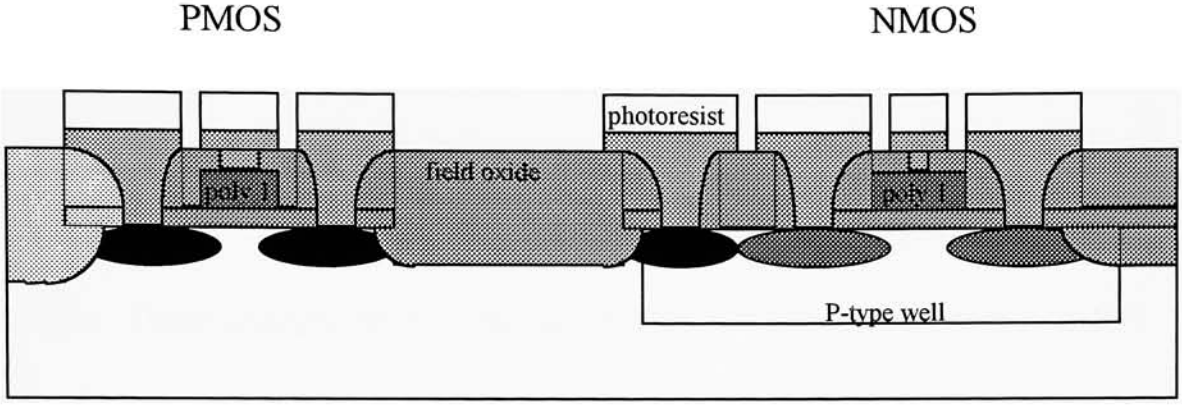


fig. 3.1.14 mask level 10 after Aluminum etch

Finally, the photoresist is completely removed and the wafers are sintered (at ~450 ^{0}C) to produce good ohmic contacts at the Aluminum / Silicon junctions.

3.2 CMOS Process Modifications:

Numerous changes were made to the original P-well (single level poly, single level metal) CMOS process to produce a double level poly (single level metal) P-well CMOS process capable of fabricating CID-based imaging arrays. These changes have potential benefits to other processes run at RIT, in addition to future applications such as CCD array fabrication and submicron CMOS. Before analyzing the test data gathered from the wafers, the potential benefits from the process alterations will be outlined.

First, all wafers should be coated with resist prior to having their backsides scribed. In the past the wafers bare device side had been placed on a cleanroom crew wipe to protect it during the scribe operation. While this was thought to be sufficient protection for the device side, an inspection step performed on a previous lot revealed scratches large enough to be seen under 10x magnification. Although this procedure adds an additional two steps to the process (spin coat, and resist ash), its effect on final yield should more than make up for this.

The pad oxide thickness should be reduced to ~500Å to minimize the "bird's beak" effect on the active area, without inducing crystalline defects in the substrate. Crystal defects (undesirable for all devices because they increase leakage currents) are especially bad for CID's, since they can drastically effect the injection operation. In the past, a pad oxide thickness of 1000Å was used in conjunction with a 1500Å Si_3N_4 layer for LOCOS isolation. The pad oxide was made intentionally thick to protect the substrate during Si_3N_4 etching in the Plasmatherm® RIE; a tool that lacked both selectivity and uniformity. With active area dimensions relatively large the "bird's beak" effect was not readily evident, yet it limited the process applications to feature sizes >2 μm. With the switch to a more selective Si_3N_4 etch recipe and the use of the GEC cell, the reduced pad oxide will still protect the substrate and allow device scaling into submicron dimensions (~0.9 - 0.8 μm). With the amount of Si_3N_4 consumed during the field oxide growth (~ 30Å) being so small, the original nitride thickness could easily be reduced to ~1200Å which would further reduce the chance of crystal defects.

After field oxidation, the SiO_2 layer formed on the Si_3N_4 film should be removed with a plasma etch (see process step #23 for specifics) instead of the

current buffered HF (BOE) solution. As with all wet chemical etches, the BOE is highly selective with respect to the nitride. Since the composition of the SiO_2 and Si_3N_4 films are not stoichiometric near their "interface" (more like an oxynitride film of varying composition), an overetch must be performed to remove all traces of SiO_2 which is not readily etched by the following nitride etch recipe (process step #23). The overetch significantly reduces the field oxide thickness and overexposes the substrate, while the wet etch and D.I. water rinse add to the processing time. By adopting the dry oxide etch, which is only ~ 700 $Å/_{min}$ and not as selective, less field oxide would be removed and throughput would increase (etch time per wafer only increases by approx. 30 sec.).

The NMOS V_T adjust mask should be eliminated from the process, and replaced with the P-well mask. Previous test chip designs used an NMOS V_T mask the approximate size of the active region, and significantly smaller than the P-well mask. By re-using the P-well mask for the NMOS V_T implant the number of written masks would be reduced by one. The NMOS transistor characteristics (i.e.: reduced leakage currents) ***may*** possibly improve, since the larger P-well mask would reduce the chance of overlay error masking part

of the active area from the threshold implant (areas masked from the implant would have a lower V_T, thus increasing the subthreshold current).

The use of two gate oxide growth recipes should be eliminated in favor of one (the second; step #43), which should also be used as the pad oxide recipe. Previous specifications called for 500Å first level gate oxides to be grown at 1100 ^{0}C (~ 8 minutes) while 500Å second level gate oxides were grown at 1000 ^{0}C (45-55 minutes). Closely matching the thickness' required tight tolerances on the first growth and proved very difficult. Adopting the second growth recipe for both steps would improve repeatability for gate oxidations and allow a closer thickness match between the two levels. This should help improve the V_T uniformity across the wafers and from lot to lot. Using this recipe for the pad oxide would provide an early indication of fluctuations in the process (requiring growth time alterations), since the pad oxide thickness is less critical than the gate oxide thickness.

Prior to the deposition of all LPCVD films (especially polysilicon and LTO), the reactor should be allowed additional time to stabilize at the desired temperature. Temperature fluctuations varying in magnitude from 10-20 ^{0}C were observed during the fabrication process. While not detrimental to the

operation of finished devices, the fluctuation will effect the properties (grain size and structure in polysilicon), uniformity, and deposition rate (LTO) of the deposited films. Allowing the reactor to stabilize at the desired temperature will significantly improve lot to lot uniformity, as well as repeatability.

The use of (Emulsitone) N-250 spin on dopant should be adopted for all N-type polysilicon doping, in accordance with the procedure outlined in process steps #35 and #36. The N-250 solution yielded sheet resistance's of ~20 Ω/cm when properly used. However coating nonuniformities and insufficient preface times cause sheet resistance deviations across the wafers, as well as residual organic contamination. By increasing the preface time to ~60 minutes (with the possible addition of increasing their spacing when placed in the oven using the quartz diffusion boats, or laying them flat in the oven without a boat) and adding a 10-15 minute APM bath after the spin on dopant removal, the resultant doped polysilicon films should have uniformly low sheet resistance's.

The polysilicon plasma etch recipe should be changed to 12.5 sccm O_2 + 37.5 sccm SF_6 at 20 watts and 300mtorr pressure, to improve polysilicon linewidth (i.e.: gate length) uniformity across the wafer as well as reducing

the loss of underlying gate oxide. The current polysilicon etch recipe is done at 400 mtorr and while somewhat selective over oxide, exhibits significant nonuniformities in etch rate across the wafer. The polysilicon on the wafers center die can clear in as little as 35 seconds while the edge die take up to 60 seconds to clear. As a result, the center die must be substantially overetched, often to the point that 2μm transistor gates disappear. The new recipe (from Dr. Lane's thin films lab) uses a higher Oxygen to Fluorine ratio with a lower power to improve the uniformity of reactants across the wafer surface, which results in an etch that is selective and of a uniform rate. As with all plasma etching, the etch rate should be verified before processing device wafers.

The LTO passivation film should be deposited before the source/drain anneal, instead of after it. By performing the source/drain anneal with the LTO film on the wafers, the loss of N+ dopants (phosphorous) to evaporation is minimized and the LTO film is "densified". As a result, the film exhibits an etchrate in buffered HF close to that of thermally grown SiO_2. This minimizes undercutting when etching contact cuts, allowing the formation of vias as small as 2μm.

"Dummy" wafers should proceed and follow device wafers during thermal steps, film depositions, and oxide growths. Non-uniformity's in temperature and flowrate during processing have been observed to cause significant deviations in film uniformity for small (5-15 wafer) lots. The most severely effected appear to be the ones at either end of the boats, possibly due to deviations from laminar flow at these regions. Placing clean "dummy" wafers on either end of the device wafers improves the flow characteristics over the entire lot, as well as reducing thickness deviations on the "end" device wafers. They would provide an easier method of measuring film thickness deviations across wafer lots and serve as convenient source of films to verify etchrates. Dummy wafers could be reused numerous times, then "retired" as lithography blanks.

A bottom anti-reflective coating (BARC) should be used on all metal level photolithography steps for patterning linewidths less than 4 μm. Because of the necessary latitude provided in the standard photolithography process (i.e.: overexposure), some linewidths must be biased if they are to be accurately reproduced in highly reflective underlying films. Biasing is an adequate technique for patterning 2μm lines in polysilicon, but is not effective

for small lines with films as highly reflective as Aluminum. Using a BARC coating (BARC films are just heavily dyed photoresists that bleach slowly upon exposure to light) between the Aluminum and photoresist layers minimizes the linewidth reduction effects from standing waves, and allows 2-3μm lines to be easily patterned. Adopting the same BARC coating characterized in all lithography labs would simplify its addition to the process, as well as providing data to monitor its process latitude.

3.3 Process Simulation:

Before proceeding with the actual processing of device wafers, transistor simulations were performed using the P-well CMOS, double level polysilicon, single level metal process parameters. These parameters were used in conjunction with SUPREM IV and MEDICI simulation software from Technology Modeling Associates, to 1) double check that the process modifications made working transistors with acceptable characteristics, and 2) compare the simulated results with the actual results and see if modifications need to be made to any of the models/parameters used by the software.

Analysis of the simulated results yielded acceptable values that corellated reasonably well with the actual results. The one major exception was the first gate oxide thickness, which was almost 100 Å too thin. However, no modifications were made to the process since this was attributed to residual TCA (Trichloroethylene) in the furnace, and could not be accounted for in the simulation. Overall, the results indicated that the major

process modifications would have the desired impact on device characteristics, and that no significant process alterations were necessary.

(Refer to Appendix C for SUPREM IV and MEDICI input files with output graphics)

IV. Results:

After the fabrication process was completed, the data from several process steps was collected and compared to calculated results for the same steps using SUPREM IV simulation software:

Process parameter	Target value	Measured	SUPREM IV
Alignment Oxide	5000 Å	~ 4950 Å	6141 Å
Well Oxide	3000 Å	~ 4100 Å	4492 Å
Pad Oxide	500 Å	~ 450 Å	378 Å
Nitride	1500 Å	~ 1300 Å	1500 Å
Field Oxide	10,000 Å	~ 10,700 Å	11,776 Å
Kooi Oxide	1000 Å	~ 850 Å	1083 Å
1st Gate Oxide	500 Å	~ 420 Å	374 Å
2nd Gate Oxide	500 Å	~ 415 Å	480 Å

The wafers were also tested in accordance with factory test procedures for P-well CMOS lots, and certain measured parameters were compared with simulated results from SUPREM IV and MEDICI software:

Test Parameter	Wafer # D3	D4	D6	D11
R_{SH}, *SHEET RESISTANCE* (Ω/sq.)				
N+ S/D	85.01	80.38	78.97	77.10
P+ S/D	84.57	86.523	90.06	78.15
P-well	1220	1170	1450	1161
N+ poly	19.01	17.81	16.34	17.12
N- poly	25.53	20.66	20.66	22.54
Metal	0.0468	0.0472	0.0473	0.0481
G_C, *CONTACT CONDUCTANCE* (mho/μm^2)				
Metal / Poly	$2.552e^{-3}$	$1.05e^{-3}$	$1.922e^{-3}$	$1.076e^{-6}$
Metal / N+	$760.4e^{-6}$	$8.941e^{-4}$	$864.5e^{-6}$	$507e^{-6}$
Metal / P+	$413.6e^{-6}$	$3.151e^{-3}$	$516.1e^{-6}$	$391e^{-6}$
TRANSISTOR MEASUREMENTS				
NMOS (poly 1):				
V_T (volts)	0.999	0.960	0.999	0.969
G_M (amps/volt)	$12.29e^{-6}$	$7.723e^{-6}$	$6.451e^{-6}$	$9.634e^{-6}$
Sub-V_T slope (decade/volt)	8.609	8.242	7.807	7.711
I_D sub-max (μamps)	11.273		5.286	7.225
I_D sub-min (p•amps)	54.96		56.04	43.36
λ (Lambda)	0.01818	0.01360	0.01272	0.01304
PMOS (poly 1):				
V_T (volts)	-0.513	-0.645	-0.555	-0.655
G_M (amps/volt)	$3.191e^{-6}$	$4.18e^{-6}$	$2.571e^{-6}$	$2.61e^{-6}$
Sub-V_T slope (decade/volt)	8.916	10.254	8.678	9.115
I_D sub-max (μ amps)	-5.022		-7.508	-4.654
I_D sub-min (n•amps)	-378.4		-2.731	-0.203
λ (Lambda)	0.04196	0.05916	0.03728	0.03443

	Wafer #			
Test Parameters	**D3**	**D4**	**D6**	**D11**
PMOS (poly 2):				
V_T (volts)	-0.340	-0.501	-0.410	-0.237
G_M (mamps/volt)	$672e^{-9}$	$750e^{-9}$	$1.565e^{-6}$	$1.213e^{-6}$
SubVT slope (decade/volt)	10.95	9.233	10.230	10.660
I_D **sub-max** (μamps)	-1.117		-4.199	-1.185
I_D **sub-min** (p•amps)	-30.08		-43.0	-47.0
λ (Lambda)	0.01099	0.01125	0.009893	0.01868

Test parameter	**Measured**	**MEDICI**
NMOS V_T	**0.999 V**	**0.9302 V**

V. Analysis and Discussion:

Analysis of the test data yielded surprising results, some of which indicated additional process modifications. Initial testing started with sheet resistance measurements on the Van Der Pauw structures. After all tests involving the P+ S/D structure failed (at different locations) for wafer #D11, it became evident that a contact problem existed. Sufficient current could not be forced through the resistor to read the voltage drop existing across it, indicating the possibility of an insufficient sinter step or the existence of a thin (>100Å) SiO_2 layer between the Aluminum film and the semiconductor regions. Since the contact cuts were significantly overetched and the final pre-metal HF dip was 50% longer than required (the HF dip lasted 90 seconds followed by a 30 second DI water rinse and a rinse in the spin rinser-dryer, where the wafers remained in dry Nitrogen until being placed in the CVC® sputter system), the contact problem was attributed to an insufficient sinter step. Closer examination of the Aluminum film revealed "specks" of an unknown material throughout, which was later determined to be Silicon. With the Silicon content of the Aluminum obviously greater than 1%, good Al/Si

ohmic contacts would not be formed unless the sinter temperature was raised above 450 ^{0}C. Lacking any indication of the actual Si content, rework was attempted on the Aluminum for five of the remaining six wafers (all wafers were originally coated with sputtered Al /1$^{\%}$Si at the same time, but only three were sintered at 450 ^{0}C to see if junction spiking occurred). Removal of the Silicon particles proved difficult while redoing the Aluminum films, and all five wafers were eventually scrapped. The one remaining wafer, #D4, was sintered at 500 ^{0}C for 60 minutes. While this reduced the contact resistance to a point where current could be passed through the test structures and the regular test programs would work, it caused a significant amount of Aluminum to diffuse into the semiconductor (which showed up as a series resistance on the NMOS transistor conductivity curves). Thus, while wafer #D4 could initially be tested as normal, wafers #D3, #D6, and #D11 required that the contact resistance was first broken down (by increasing maximum voltage on each structure's test program to 20 volts, and forcing current to break down the resistance). After this treatment the Van Der Pauw resistors for all three wafers still exhibited problems, and the test programs had to be changed to sweep voltage for accurate readings.

Overall, the sheet resistance measurements on the Van Der Pauw structures exhibited better uniformity across each wafer and between different wafers than was originally expected.

The P+ S/D sheet resistance was higher than expected, at ~ 85 Ω/sq. Although an acceptable value, it is most likely due to the use of BF_2 for the source/drain implant. The Varian® 400 ion implanter used during fabrication is a low current model that analyzes (separates) the specific ions before acceleration. Ions like BF_2 can disintegrate during acceleration causing a reduced dose of BF_2 to be implanted at the desired energy, along with B_{11}, BF, and F ions being implanted at significantly different energies. The end result is an unpredictable implant of varying composition, with a potentially negative impact on device performance. Since significant problems were experienced with the Boron source during the P+ S/D implant, this would appear to be a valid conclusion. To eliminate this problem from future lots, all P+ S/D implants should be performed using B_{11} ions.

The N+ S/D sheet resistance was significantly higher than expected, at ~ 80 Ω/sq. Previous factory lots exhibited sheet resistance's of ~ 30 Ω/sq., and had good ohmic contacts between the Aluminum and N+ regions. The

eventual appearance of a slight series resistance on Aluminum/ N+ contacts confirmed that the changes made to the N+ S/D implant (a 1e15 ions/cm^2 dose of P_{31} at 80 KeV) did not provide the required 1e19/cm^3 dopant level at the surface of the source/drain region, which is necessary for the formation of ohmic contacts between Aluminum and N+ Silicon. The problem is believed to be from the residual gate oxide over the source/drain region being significantly less than 500Å, which was used to model the implant profile. If the remaining oxide was thinner than expected, the peak of the implant would be deeper in the substrate and the surface concentration (after annealing) would be reduced by orders of magnitude. Without the necessary control over (or relevant thickness information about) the residual amount of gate oxide covering the source/drain region, the best solution would be to follow the steps in the N-well process and remove the oxide before the implant. By performing a 30 second buffered HF etch on the wafers after exposure of the N+ S/D mask, the residual oxide would be removed prior to ion implantation. The energy of the implant should then be reduced to ~33 KeV, which has been proven to form good Aluminum/ N+ Silicon ohmic contacts for a P_{31} dose of 1e15 ions/cm^2. By using a 1e15 ions/cm^2 implant dose instead of the

original 4e15 ions/cm^2 dose, the time needed to perform the N+ S/D implant is reduced by ~ 75%.

The P-well sheet resistance was approximately 1200 Ω/sq. Although a reasonable value, the significant fluctuations observed across individual wafers during testing may have caused error in this value. The majority of values were in the 1100-1200 Ω/sq. range, but several were as high as 3370 Ω/sq. While no indications exist as to the cause of this, the most likely one is thought to be an improperly set scan frequency on the ion implanter during the P-well implant.

The N+ poly and N- poly sheet resistance's were surprisingly low, at ~ 17.5 Ω/sq. and ~ 22 Ω/sq. respectively. These low values are unquestionably due to the effectiveness of the N-250 spin on dopant.

Finally, the metal sheet resistance was also surprisingly low, at ~ 0.0474 Ω/sq. Considering the high Silicon content of the film, this small a resistance was completely unexpected. To eliminate the Silicon contamination problem and ensure good contacts with future films, all Aluminum should be sputtered using the Perkin-Elmer® system.

Contact conductance $\mathbf{G_C}$ measurements were also lower than expected (in comparison to past factory lots), with the exception of the metal/ N+ value. $\mathbf{G_C}$ for the metal/poly structure was lower than expected at $1.65e^{-3}$ mho/μm^2, as was the metal/P+ structure at $1.118e^{-3}$ mho/μm^2. The metal/N+ structure tested at an acceptable, yet slightly high, $\mathbf{G_C}$ value of $7.565e^{-4}$, most likely due to the previously mentioned problem with N-type dopant concentration.

The measured transistor parameters were suprisingly uniform across individual wafers, as well as between them. When compared to past factory lots, the NMOS and PMOS transistors fabricated with the new process showed excellent operating characteristics.

The most unexpected results came from the NMOS transistors, which had threshold voltages closer to +1 volt than any previous lot. Aside from the previously mentioned series resistance, the average $\mathbf{V_T}$ for all four wafers was 0.982 volts, which is so close to the desired value that no further adjustments should be made. The transconductance $\mathbf{G_m}$ was low, at ~$9.02e^{-6}$ amps/volt, as was the channel length modulation parameter $\boldsymbol{\lambda}$, at ~0.01439/volts^2. This seemed to indicate good long channel characteristics for the 6μm/32μm

NMOS, which was supported by the $\mathbf{I_D}$-$\mathbf{V_D}$ conductivity curves. Subthreshold characteristics were acceptable with both $\mathbf{I_{Dsubmin}}$ and $\mathbf{I_{Dsubmax}}$ slightly lower than expected, although $\mathbf{I_{Dsubmax}}$ was potentially too low. However the subthreshold slope **SS** was ~ 8.1, indicating a good transition between "on" and "off".

The (first level poly) PMOS transistors were also better than expected, but lacked the uniformity displayed by the NMOS transistors. Threshold voltages varied significantly on wafers #D3 and #D6, with their average $\mathbf{V_T}$ being -0.534 volts. Wafers #D4 and #D11 displayed much better uniformity along with an average $\mathbf{V_T}$ of -0.65 volts, which appears to be the correct value. The PMOS VT is -0.35 volts off the desired value of -1 volt, which requires a threshold adjust implant of *Phosphorous* (dose = ~$1.006e^{12}$ ions/cm^2 at an energy of 80 KeV, through the Kooi oxide). This poses a problem, since threshold adjust implants at RIT have always used *Boron*. To perform this implant will require an additional mask level that defines only the PMOS active area. However, fabrication of an additional mask can be avoided by using a negative photoresist (or AZ 1524-E in image reversal) and exposing it with the P-well mask. This will mask all NMOS transistors from

the implant, and allow older mask levels to be used with this process. Transconductance G_M, at ~ $3.14e^{-6}$ amps/volt, and the channel length modulation parameter λ, at 0.0432 /volts^2, were also less than on previous factory lots. These low values imply good long channel behavior for the PMOS transistors, as should be expected for a device with 16 μm/ 32μm dimensions. Subthreshold characteristics were similar to the NMOS transistor, as $I_{Dsubmin}$ and $I_{Dsubmax}$ were both lower than expected. The subthreshold slope **SS** showed improved "on"/"off" characteristics with a value of 9.24.

Finally, several second level poly PMOS transistors were examined on wafer #D4. Unlike the first level poly transistors, their performance was not as good as was expected. The threshold voltage, as expected, had shifted slightly to -0.501 volts. The channel length modulation parameter λ, at 0.01125 /volts^2, had slightly declined but the transconductance G_M dropped almost an order of magnitude to ~$750e^{-9}$ amps/volt. While these devices should still exhibit good long channel behavior, the effect of these parameters on CID operation is not known. Subthreshold currents were also reduced by an order of magnitude, but the subthreshold slope was more than acceptable

at a value of 9.23. However, the greatest concern is the I_D-V_D conductivity curve. The maximum drain current is only 45.16 μamps (using the standard test program) which seems quite low, even when taking into account the smaller 10 μm /20μm device dimensions.

VI. Conclusions:

Numerous changes were made to the original P-well (single level poly, single level metal) CMOS process to produce a double level poly (single level metal) P-well CMOS process capable of fabricating CID-based imaging arrays. These changes have potential benefits to other processes run at RIT, in addition to future applications such as CCD array fabrication and submicron CMOS.

Transistors made from the first polysilicon level will be more than adequate for address circuitry, amplifier, and pixel applications, once the contact problem with the NMOS has been fixed and the PMOS Vt is adjusted. Second level polysilicon PMOS transistors seem acceptable, with the exception of the threshold voltage, but the low value for I_{Dsat} may have an effect on CID pixel performance. This may be the result of boron depletion in the channel (from the two gate oxidations), and should be investigated if fabricated arrays exhibit poor performance.

With the necessary modifications, the process should produce an operational CID (or CCD) array.

APPENDIX A

Description Of CMOS Process Operations

CMOS Processing:

The basic process is derived from a single level polysilicon P-well CMOS process. Modifications have been made to the original process that result in a double level polysilicon (P-well) CMOS process, which is capable of forming both the imaging structures and address circuitry. The resulting process was used to fabricate both the CIDTEC® testchip and the RIT P-well CMOS testchip on all ten device wafers, and is as follows:

Step #1: DE01: 4PT PROBE

One wafer from the lot was probed to measure the sheet resistance. At a voltage of 0.47 volts a current of 0.001 Amps was measured, indicating a sheet resistance of ~3.9 Ohm-cm, which was close to the 4.5 Ohm-cm sheet resistance listed on the container.

Step #2: ID01: SCRIBE

Prior to scribing the ID number on the back of each wafer, all wafers were spin coated with photoresist (Shipley 812 positive resist) using program 7,3,3 on the wafertrac® to protect the device side from scratches. After scribing, the photoresist coat was removed with a "piranha" bath (3 parts H_2SO_4 and 1 part H_2O_2).

Step #3: CL01: RCA CLEAN

Prior to the growth of the alignment oxide, the wafers were cleaned of contaminants in solutions of HCl/H_2O_2 (Hpm), 50:1 HF, and NH_4OH/H_2O_2 for 10 minutes/ 1 minute/ 10 minutes respectively. They were rinsed in D.I. water following each bath and dried in the spin rinser/dryer (SRD).

Step #4: OX04: WET OXIDE DIFFUSION

An 1100 ^{0}C wet oxidation to grow ~5000 Å of Oxide. This masks regions other than the P-well during the well drive, in addition to forming a step height between the substrate and P-well regions which serves to form the alignment mark.

Step #5: PH03: PHOTOLITH (WELL)

Using the wafertrac®, Shipley 812 positive photoresist is coated using program 7,3,3, exposed on the GCA® 6800 stepper to define the P-well region, and developed using MF 321 developer on program 7,2,2.

Step #6: ET06: OXIDE ETCH

Lithographically defined oxide is etched in a buffered HF solution to expose the silicon substrate.

Step #7: IM01: ION IMPLANT

A dose of 4e12 ions/cm^2 B11 at an energy of 50 KeV are implanted into the exposed silicon, to provide the p-type dopants for the well regions on the substrate.

Step #8: ET07: STRIP

The masking photoresist layer is exposed to a 300 watt Oxygen plasma which completely removes it.

Step #9: CL01: RCA CLEAN

The wafer are cleaned of contamination (prior to the well drive) using the same HPM/ HF /APM solutions as in step #3, for 10 minutes/ 1 minute/ 10 minutes respectively.

Step #10: OX06: DRY OXIDE DIFFUSION

The previously implanted B11 dopants are allowed to diffuse for 20 hours at 1125 ^{0}C to form the P-well. An initial 4 hour diffusion in Oxygen forms ~3000 Å of oxide over the well regions, while leaving the oxide masked regions essentially unchanged. The device wafers were accidentally exposed to 8.5 hours of Oxygen which required reducing the time in Nitrogen from 16 to 12 hours, in order to maintain the required well dopant profile.

Step #11: ET06: OXIDE ETCH

All oxide is etched off the wafers using buffered oxide etch. This leaves the P-well regions (and alignment marks) defined by their reduced step height in comparison to the bulk Silicon regions.

Step #12: OX05: DRY OXIDE DIFFUSION

A 500 Å pad oxide is grown in furnace #12 during a dry oxidation at 1100 ^{0}C to serve as a buffering layer between the substrate and the following Si_3N_4 layer. It is recommended that this growth be changed to the same specifications as the second gate oxide growth (~55min. O_2 at 1000 ^{0}C) to both increase the repeatability of this step, and serve as an indicator in case the gate oxidation needs to be adjusted for time.

Step #13: CV02: LPCVD NITRIDE

1500 Å of Si_3N_4 are deposited using low pressure chemical vapor deposition at 810 ^{0}C on all wafers. Since less than 300 Å will decompose during the later field oxidation, it is recommended that the deposited thickness be reduced to ~1200 Å to reduce both the stress on the substrate and the chance for crystal defect formation during field oxidation.

Step #14: PH03: PHOTOLITH (ACTIVE)

As in step #5, Shipley 812 positive photoresist is spin coated using program 7,3,3, exposed to define active areas, and developed using MF 321 developer with program 7,2,2.

Step #15: ET09: NITRIDE ETCH

In the GEC plasma cell, Si_3N_4 is etched using a 50 watt SF_6 plasma at 300 mtorr pressure (30 sccm SF_6 flowrate) for 60 seconds. It is recommended that the etchrate of the plasma is determined from test wafers prior to etching device wafers, in order to minimize overetching.

Step #16: ET07: STRIP

All photoresist is removed from the wafers using a 300 watt Oxygen plasma.

Step #17: PH03: PHOTOLITH (CHANNEL STOP)

Similar to step #5, Shipley 812 positive photoresist is spin coated using program 7,3,3 , exposed to define the region surrounding the P-well, and developed using MF 321 developer with program 7,2,2.

Step #18: IM01: ION IMPLANT

A dose of 8e13 ions/cm^2 B11 at an energy of 100KeV is implanted into the region surrounding the well to insure that the dopant level after oxidation is sufficient to prevent formation of an "inverted" region of minority carriers surrounding the P-well.

Step #19: ET07: STRIP

All photoresist is removed from the wafers in a 300 watt Oxygen plasma.

Step #20: ET06: OXIDE ETCH

Pad oxide exposed in regions where the Si_3N_4 was etched off, is removed prior to field oxidation using a buffered HF solution.

Step #21: CL01: RCA CLEAN

The wafers were cleaned of contaminants using the same previously mentioned HPM/ HF/ APM solutions for 10 minutes/ 1 minute/ 10 minutes respectively.

Step #22: OX04: WET OXIDE DIFFUSION

A field oxide of ~10,000 Å is grown in a wet Oxygen ambient at 1100 ^{0}C for 210 minutes to isolate the active regions from each other. The resulting field oxide is of a semi-recessed nature.

Step #23: ET07: NITRIDE ETCH

The Si_3N_4 that decomposed into SiO_2 during the oxidation is etched off in a buffered HF solution (30 seconds 10:1 BOE) prior to the plasma nitride strip (30 sccm SF_6 at 300 mtorr and 40 watts). It is recommended that this step be eliminated in favor of a plasma oxide etch that would reduce the field oxide thickness loss and increase throughput. A suitable recipe would be 30 sccm CHF_3 plus 1sccm O_2 in a ~40 watt, 30 mtorr plasma. This should result in a highly anisotropic etch of ~500 Å/minute, and would less than 1 minute per wafer to the overall plasma etch.

Step #24: ET06: OXIDE ETCH

Underlying pad oxide is removed from the active areas with a buffered HF solution. The etchrate of the HF solution should be measured just prior to etching, to determine the time that allows all pad oxide to be removed with a minimum thickness loss to the field oxide.

Step #25: CL01: RCA CLEAN

Contaminants are again removed from the wafers using the previously described solutions of HPM/ HF /APM for 10 minutes/ 1 minute/ 10 minutes respectively.

Step #26: OX04: WET OXIDE DIFFUSION

A 1000 Å wet ("Kooi") oxide is grown at 900 ^{0}C to decompose any Si_3N_4 which may have formed on the active regions during the field oxidation. The oxide will also allow proper placement of the peak concentrations for both threshold adjust implants in the substrate.

Step #27: IM01: ION IMPLANT

A dose of 1.0e11 ions/cm^2 B11 at an energy of 60KeV are implanted over all regions of the substrate for adjusting the threshold voltage of the pmos transistors to -1 volt.

Step #28: PH03: PHOTOLITH (NMOSVT)

As in previous steps, Shipley 812 positive photoresist is spin coated on all wafers using program 7,3,3, exposed to define the regions to receive the nmosvt implant, and developed using MF 321 developer with program 7,2,2 . It is recommended that the P-well level photomask is used instead of the nmosvt level, since it will expose all of the well area and reduce the number of mask levels to be fabricated.

Step #29: IM01: ION IMPLANT

A dose of 1.2e12 ions/cm^2 B11 at an energy of 60 KeV are implanted into the defined P-well regions to adjust the threshold voltage of the nmos transistor to +1 volt.

Step #30: ET07: STRIP

All photoresist is removed from the wafers by exposure to a 300 watt Oxygen plasma.

Step #31: ET06: OXIDE ETCH

The 1000 Å "Kooi" oxide grown in step #24 is etched off in a buffered HF solution. Again, the etchrate of the HF should be determined just prior to etching the device wafers to insure complete removal of the oxide and minimal loss of field oxide.

Step #32: CL01: RCA CLEAN

Contamination is cleaned from the wafers using the previously mentioned solutions of HPM/ HF /APM for 10 minutes/ 1 minute/ 10 minutes respectively.

Step #33: OX06: DRY OXIDE DIFFUSION

A 500 Å gate oxide is grown in furnace #12 during a dry oxidation at 1100 ^{0}C, for both the address circuitry transistors and the imager area structures. It is recommended that this step is changed to follow the second gate oxide recipe (new pad oxide recipe) of 55 minutes at 1000 ^{0}C to increase the repeatability of this oxide growth. In addition the TCA clean should be performed when the furnace stabilizes at 900 ^{0}C, since the effectiveness of the TCA increases with temperature.

Step #34: CV01: LPCVD POLYSILICON

Approximately 6000 Å of polysilicon are deposited on the wafers using low pressure chemical vapor deposition at 610 ^{0}C. It is recommended that extra time and care are taken during the setup of the LPCVD reactor to insure that a stable temperature gradient exists prior to deposition. This will help to reduce thickness variations across the wafer lot.

Step #35: DI04: N-TYPE DIFFUSION

N250 spin on dopant is spin coated on all wafers at 3000 rpm ~30 seconds, prebaked at 200 ^{0}C for 15 minutes, then diffused at 1000 ^{0}C for 15

minutes. Due to difficulties encountered with this technique, It is recommended that the N250 solution is spin coated before reaching room temperature in the following manner: spin coat several ml of N250 for ~5 seconds at 500 rpm (to initially coat wafer), immediately spun at ~2000 - 3000 rpm to achieve final coating thickness, prebaked at 200 ^{0}C for at least 1 hour, then diffused at 1000 ^{0}C for 15 minutes. Coating non-uniformity's and insufficient prebaking were believed to be the cause of sheet resistance fluctuations, and these additional steps should eliminate these problems. Assuming these steps do not eliminate the problem, an additional coating of N250 solution at the previously defined parameters is recommended following the prebake and prior to the 1000 ^{0}C diffusion.

Step #36: ET06: OXIDE (SOG) ETCH

All spin on dopant is etched off the deposited polysilicon using a buffered HF solution. It is recommended that a visual inspection follow this step, since an insufficient prebake may result in a residual "film" on the polysilicon surface that cannot be removed by the HF solution. Should a film be observed, a 10 - 15 minute immersion in an APM solution should remove

it. Sufficient prebake time should not produce a residual film after etching the spin on dopant.

Step #37: DE01: 4PT PROBE

Polysilicon sheet resistance is measured at 5 points on the wafer to insure adequate doping of the gate material.

Step #38: PH03: PHOTOLITH (POLY 1)

As in previous photolithography steps, Shipley 812 positive photoresist is spin coated using program 7,3,3, exposed to define the gate regions for the first polysilicon level, and developed using MF 321 developer with program 7,2,2 .

Step #39: ET08: POLYSILICON ETCH

Using the GEC plasma cell, the polysilicon was patterned in an SF_6\ O_2 plasma (42 sccm SF_6, 7.5 sccm O_2, 400 mtorr pressure, 40 watts power) for approximately 60 seconds per wafer. Visual endpoint detection was used for all wafers, due to the tendency of this plasma to etch faster in the center of

the wafer than at the edges. It is recommended that either this recipe is changed to use a lower processing pressure (i.e.: ~225 mtorr instead of 400 mtorr), or that the following recipe be used instead: 37.5 sccm SF_6, 12.5 sccm O_2, 300 mtorr pressure, at 20 watts power. While both recipes should yield more uniform results, the second should provide a better selectivity over the underlying gate oxide.

Step #40: ET07: STRIP

All photoresist is removed from the wafers by exposure to a 300 watt Oxygen plasma.

Step #41: ET07: OXIDE ETCH

All wafers are placed in a buffered oxide solution to remove gate oxide damaged from the polysilicon etch from areas where it will be re-grown. It is recommended that the etch rate of the bath be determined immediately prior to this step, to insure the wafers remain in the bath long enough to etch all the exposed gate oxide with a minimal loss to the field oxide.

Step #42: CL01: RCA CLEAN

Contamination is removed from all wafers by cleaning with the previously described solutions of HPM/ HF / APM for 10 minutes/ 1 minute/ 10 minutes respectively.

Step #43: OX06: DRY OXIDE DIFFUSION

A second 500 Å gate oxide is grown in furnace #12 on all areas of exposed single crystal silicon in a dry Oxygen ambient at 1000 ^{0}C for 55 minutes. In addition, an insulating layer of ~800 Å of oxide is grown on all exposed polysilicon, which will insulate it from the second polysilicon layer. It is recommended that this recipe be used ,as previously mentioned, for all gate oxide growths and the pad oxide growths to increase uniformity. As in the previous gate oxidation, the TCA should be used when the furnace reaches 900 ^{0}C to increase the effectiveness of the TCA.

Step #44: CV01: LPCVD POLSILICON

Approximately 6000 Å of polysilicon are deposited on the wafers using low pressure chemical vapor deposition at 610 ^{0}C. As with the previous

polysilicon deposition, it is recommended that additional time be allowed during the setup and stabilization of the LPCVD reactor.

Step #45: DI04: N-TYPE DIFFUSION

As in step #35, N250 spin on dopant is coated on all wafers at ~3000 rpm for 30 seconds, prebaked at 200 ^{0}C for 15 minutes, then diffused at 1000 ^{0}C for 15 minutes. Again, the same recommendations made in step #35 should also be applied to this step.

Step #46: ET06: OXIDE ETCH

The spin on dopant is removed from all wafers using a buffered HF solution. As in step #36, the wafers should be inspected for traces of residual organics and treated with an Apm solution as necessary.

Step #47: DE01: 4PT PROBE

Polysilicon sheet resistance is measured at 5 points on the wafer to insure adequate doping of the gate material.

Step #48: PH03: PHOTOLITH (POLY 2)

As with previous photolithography steps, Shipley 812 positive photoresist is spin coated on all wafers using program 7,3,3, exposed to define the second level polysilicon gate regions, and developed using MF 321 developer with program 7,2,2.

Step #49: ET08: POLYSILICON ETCH

Using the GEC plasma cell, the polysilicon gate regions were patterned using the previously mentioned SF_6/ O_2 plasma as in step #39 (42 sccm SF_6, 7.5 sccm O_2, 400 mtorr etch pressure, 40 watts power). It is recommended that the same changes mentioned in step #39 also be applied here to improve unifomity across the wafer.

Step #50: ET07: STRIP

All photoresist is removed from the wafers using a 300 watt Oxygen plasma.

Step #51: PH03: PHOTOLITH (P+ S/D)

As with previous photolithography steps, Shipley 812 positive photoresist is spin coated on all wafers using program 7,3,3, exposed to define the P+ source-drain regions, and developed using MF 321 developer with program 7,2,2.

Step #52: IM01: ION IMPLANT

A dose of 2e15 ions/cm^2 BF_2 at an energy of 150 KeV are implanted into the defined P+ active regions on each wafer to form the source and drain regions for the PMOS transistors.

Step #53: ET07: STRIP

All photoresist is removed from the wafers using a 300 watt Oxygen plasma.

Step #54: PH03: PHOTOLITH (N+ S/D)

As with previous photolithography steps, Shipley 812 positive photoresist is spin coated on all wafers using program 7,3,3, exposed to

define all N+ source/drain regions, and developed using MF 321 developer with program 7,2,2.

Step #55: IM01: ION IMPLANT

Due to a problem with the high voltage supply on the implanter, the required implant dose of 4e15 ions/cm^2 Phosphorous at an energy of 120 KeV could not be performed. Instead, an implant dose of 1e15 ions/cm^2 Phosphorous at an energy of 80 KeV was done into all the defined N+ active areas, to form the source and drain regions on the NMOS transistors.

Step #56: ET07: STRIP

All photoresist is removed from the wafers using a 300 watt Oxygen plasma.

Step #57: CL01: RCA CLEAN

The wafers were cleaned of contaminants using the previously described HPM/ HF/ APM solutions for 10 minutes/ 1 minute/ 10 minutes respectively.

Step #58: CV03: LPCVD LTO

Approximately 3000 Å of low temperature oxide are deposited on all wafers using low pressure chemical vapor deposition at 410 ^{0}C. It is recommended that, as in previous LPCVD steps, additional time is taken during the set-up of the LPCVD reactor to allow for stabilization of a proper temperature gradient. This should help minimize wafer to wafer thickness non-uniformities.

Step #59: OX08: ANNEAL

All wafers are diffused at 950 ^{0}C for 30 minutes (15 minutes Nitrogen, 15 minutes Oxygen) to anneal out crystal damage from the previous implants, and to activate all implanted dopants. In addition, the deposited LTO film will be "densified" by this step (it's etchrate in buffered HF solutions will be reduced to that of thermally grown oxide). This "densification" will reduce the minimum distance between vias, and allow smaller diameter vias to be placed closer together.

Step #60: PH03: PHOTOLITH (CONTACT CUTS)

As with previous photolithography steps, Shipley 812 positive photoresist is spin coated on all wafers using program 7,3,3, exposed to define the contact cut areas, and developed using MF 321 developer with program 7,2,2.

Step #61: ET06: OXIDE ETCH

The LTO and residual gate oxide films are etched from the exposed contact cut regions using a buffered HF solution. It recommended that the etchrate of the HF solution be determined immediately prior to etching the device wafers. Additionally, a test wafer (with a densified LTO film that equals or exceeds the film on the thickest device wafer) should be etched with all the device wafers to help determine endpoint. Once the test wafer "pulls dry" from the HF solution, an additional 1- 2 minute overetch should be added to allow complete removal of the oxide films. Visual inspection should follow the D.I. water rinse and dry.

Step #62: ET07: STRIP

All photoresist is removed from the wafers using a 300 watt Oxygen plasma.

Step #63: CL01: RCA CLEAN

Contamination is removed from the wafers using the previously mentioned HPM/ HF/ APM solutions for 10 minutes/ 1 minute/ 10 minutes respectively, except that an additional 1 minute HF dip follows the Apm bath to remove any oxide grown by the bath. This results in exposed silicon regions which should form good "ohmic" contacts with the following Aluminum film.

Step #64: ME01: ALUMINUM DEPOSIT

Approximately 7500 Å of Aluminum are deposited using the CVC® sputter system (base pressure ~5e-6 mtorr, 340 Volts, 10 Amps, for ~20 minutes (with a 7-10 minute pre-sputter)). Due to contact problems with the Aluminum films sputtered from this machine, it is recommended that the evaporation system be used until adequate films can be sputtered.

Step #65: PH03: PHOTOLITH (METAL)

As in previous photolithography steps, Shipley 812 positive photoresist is spin coated on all wafers using program 7,3,3, exposed to define the metal lines and pads, and developed using MF 321 with program 7,2,2. It is recommended that for features smaller than 4 microns, a bottom anti-reflective coating is used to minimize linewidth variations due to the reflective nature of the Aluminum.

Step #66: ET05: ALUMINUM ETCH

Aluminum exposed by the previous photostep is etched off the wafers in a bath of Aluminum etch (Phosphoric acid, Nitric acid, and Acetic acid) at 50 ^{0}C. It is recommended that, for optimum linewidth control, the bath temperature is reduced to 40 ^{0}C and all wafers are etched individually using visual endpoint detection. This should improve uniformity on dimensions at or below 4 microns. Visual inspection following rinsing and drying is also recommended.

Step #67: ET07: STRIP

All photoresist is removed from the wafers in a 300 watt Oxygen plasma. It is recommended that an additional 15 - 20 minutes be added to the plasma strip with a final visual inspection, to insure that the photoresist has been completely removed.

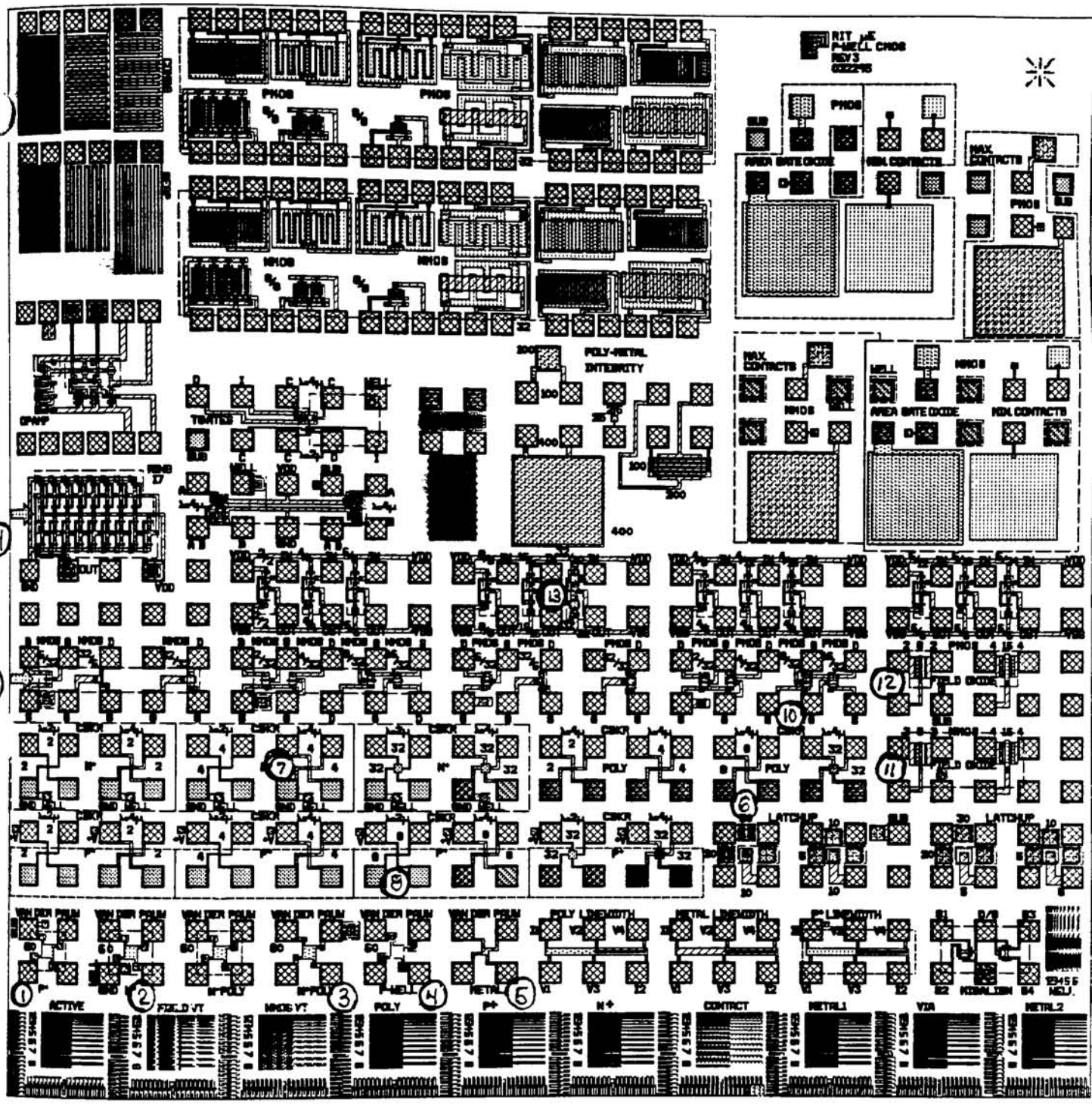
Step #68: SI01: SINTER

All wafers are sintered in forming gas (95% N_2, 5% H_2) at 425 ^{0}C to form ohmic contacts between the Aluminum and silicon regions. Additionally, dangling bonds contained in the gate oxide are passivated, thereby reducing the overall amount of trapped charge. It is recommended that sintering take place at 450 ^{0}C (due to temperature control problems with the furnace) to insure good ohmic contacts are formed.

Step #69: TE01: TEST

APPENDIX B

Test Chip And Device Chip Designs



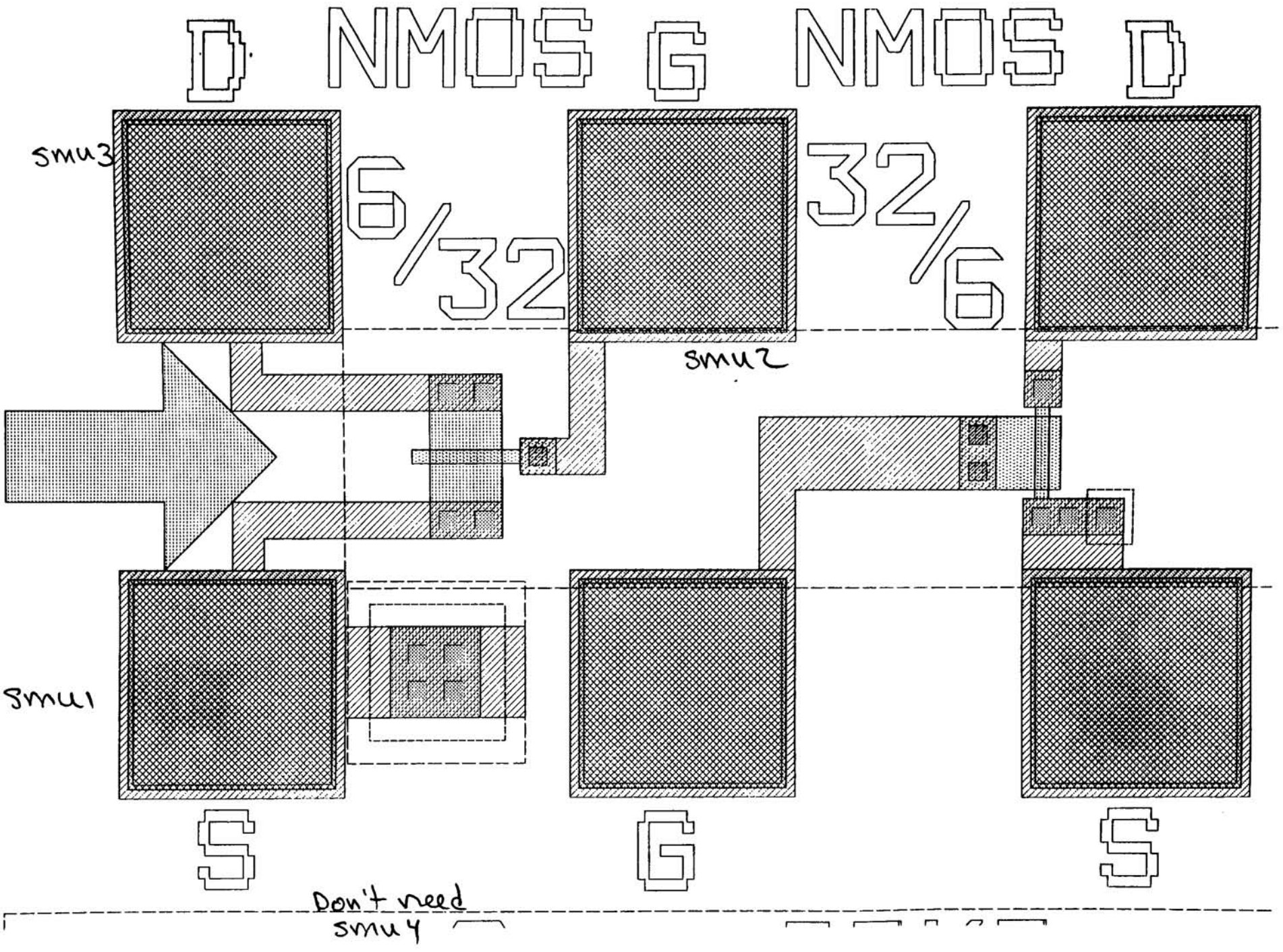
1 RHOS, P+DS
2 RHOS, N+DS
3 RHOS, POLY
4 RHOS, PWELL
5 RHOS, METAL

6 Gc metal-poly
7 Gc metal-n+
8 Gc metal-p+

9 NMOSFET
10 PMOSFET

11 NMOSFET FIELD OXIDE ON WELL
12 PMOSFET FIELD OXIDE ON SUB

13 Inverter
14 Ring Oscillator


D
NMOS
G
NMOS
D
smu3
6/32
32/6
smu2
smu1
S
G
S
Don't need
smu4

TEST NAME: **NFAM** NMOFET FAMILY OF CURVES IDS VS VDS AND VGS
L / W = 6 μm / 32 μm

EXTRACTION: LAMBDA is found from the slope of the VGS=3 curve in saturation divided by Idsat (units $1/V^2$)

CHANNEL DEFINITION

	NAME		SOURCE	
CHAN	**V**	**I**	**MODE**	**FCT**
SMU1	VS	IS	COM	CONST
SMU2	VG	IG	V	VAR1
SMU3	VD	ID	V	VAR2
SMU4	VB	IB	V	CONST
Vs 1		----------	V	
Vs 2		----------	V	
Vm 1		----------	----------	----------
Vm 2		----------	----------	----------
USER FCTN				
1				
2				

SOURCE SET UP

	VAR 1	VAR 2
NAME	VD	VG
SWEEP MODE	LINEAR	LINEAR
START	0	0
STOP	5 V	--------
STEP	0.1 V	0.5 V
NO. OF STEP	51	10
COMPLIANCE	100 mA	1 mA
CONSTANT		
VS COM	0	105 mA
VSUB V	0 V	100 mA

DISPLAY MODE: GRAPHICS

	X axis	Y1 axis	Y2 axis
NAME	VD	ID	
SCL	LINEAR	LINEAR	
MIN	0	0	
MAX	5 V	500 μA	

TEST NAME: **NIDVG** NMOSFET IDS VERSUS VGS WITH VD=0.1 VOLTS
L / W = 6 μm / 32 μm

EXTRACTION: The transconductance GM is measured at the peak value. The threshold voltage VT is the voltage VG where current starts to increase. Use the intersection of a straight line with the ID = 0 axis (or with a horizontal line at ID equal leakage current)

CHANNEL DEFINITION

	NAME		SOURCE	
CHAN	**V**	**I**	**MODE**	**FCT**
SMU1	VS	IS	COM	CONST
SMU2	VG	IG	V	VAR1
SMU3	VD	ID	V	VAR2
SMU4	VB	IB	V	CONST
Vs 1		----------	V	
Vs 2		----------	V	
Vm 1		----------	----------	----------
Vm 2		----------	----------	----------
USER FCTN				
1	GM	(/OHM) =	DELTA ID /	DELTA VG
2				

SOURCE SET UP

	VAR 1	VAR 2
NAME	VG	VB
SWEEP MODE	LINEAR	LINEAR
START	0	0.1
STOP	5 V	--------
STEP	0.1 V	-1
NO. OF STEP	51	0
COMPLIANCE	1 mA	50 mA
CONSTANT		
VS COM	0 V	105 mA

DISPLAY MODE: GRAPHICS

	X axis	Y1 axis	Y2 axis
NAME	VG	ID	GM
SCL	LINEAR	LINEAR	LINEAR
MIN	0 V	0 A	0
MAX	5 V	0.1 mA	50 μ mho

TEST NAME: **NSUBVT** NMOSFET SUB THRESHOLD CURRENT VS VGS (VDS=0.1)
L / W = 6 μm / 32 μm

EXTRACTION: The subthreshold slope in millivolts per decade is measured by drawing a straight line through the region where the current drecreases below VT. Minimum value of drain current Isub-min and the maximum value Isub-max is read off the curve at 0 and 5 volts

*** VERY IMPORTANT — MICROSCOPE LIGHT MUST BE OFF DURING THE MEASUREMENT.

CHANNEL DEFINITION

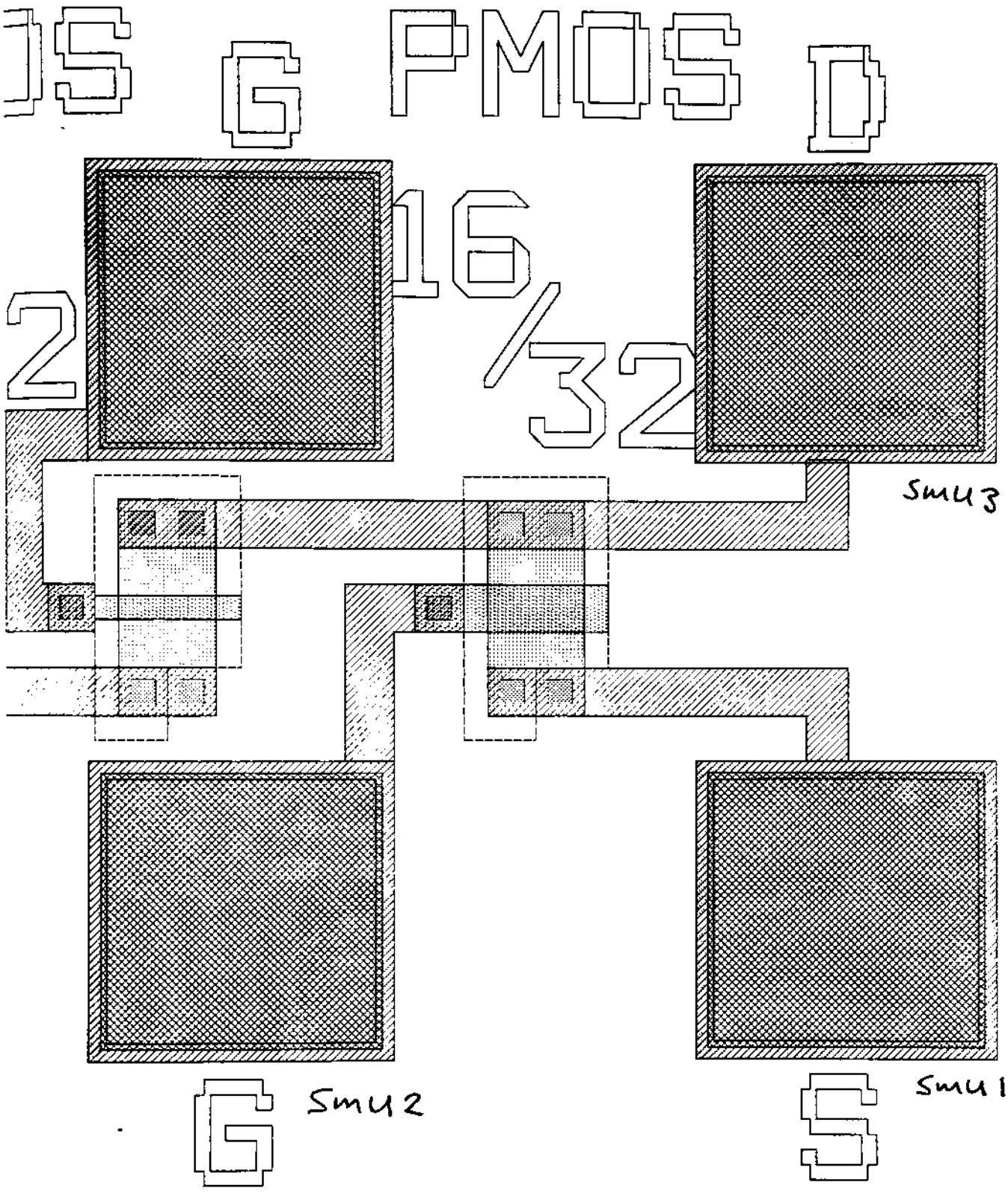
	NAME		SOURCE	
CHAN	**V**	**I**	**MODE**	**FCT**
SMU1	VS	IS	COM	CONST
SMU2	VG	IG	V	VAR1
SMU3	VD	ID	V	VAR2
SMU4	VB	IB	V	CONST
Vs 1		----------	V	
Vs 2		----------	V	
Vm 1		----------	----------	----------
Vm 2		----------	----------	----------
USER FCTN				
1				
2				

SOURCE SET UP

	VAR 1	VAR 2
NAME	VG	
SWEEP MODE	LINEAR	LINEAR
START	0	
STOP	5 V	----
STEP	0.05 V	
NO. OF STEP	101	
COMPLIANCE	1 mA	
CONSTANT		
VS COM	0	105 mA
VSUB V	0.100 V	100 mA
VB- COM	0	105 mA

DISPLAY MODE: GRAPHICS

	X axis	Y1 axis	Y2 axis
NAME	VG	ID	SUBVT
SCL	LINEAR	LOG	LINEAR
MIN	0	1 nA	0
MAX	5	1 mA	1


S
G
PMOS
D
2
16/32
SMU3
G
SMU2
S
SMU1
R
4

TEST NAME: **PFAM** PMOSFET FAMILY OF CURVES IDS VS VDS AND VGS
L / W = 16 μm / 32 μm

EXTRACTION: LAMBDA is found from the slope of the VGS= -3 curve in saturation divided by Idsat (units $1/V^2$)

CHANNEL DEFINITION

	NAME		SOURCE	
CHAN	**V**	**I**	**MODE**	**FCT**
SMU1	VS	IS	COM	CONST
SMU2	VG	IG	V	VAR2
SMU3	VD	ID	V	VAR1
SMU4	VB	IB	V	CONST
Vs 1		----------	V	
Vs 2		----------	V	
Vm 1		----------	----------	----------
Vm 2		----------	----------	----------
USER FCTN				
1				
2				

SOURCE SET UP

	VAR 1	VAR 2
NAME	VD	VG
SWEEP MODE	LINEAR	LINEAR
START	0	0
STOP	- 5 V	---------
STEP	- 0.1 V	- 0.5 V
NO. OF STEP	51	10
COMPLIANCE	100 mA	1 mA
CONSTANT		
VS COM	0	105 mA
VB V	0 V	100 mA

DISPLAY MODE: GRAPHICS

	X axis	Y1 axis	Y2 axis
NAME	VD	ID	
SCL	LINEAR	LINEAR	
MIN	0	0	
MAX	- 5 V	- 500 μA	

TEST NAME: **PIDVG** PMOSFET IDS VS VGS WITH VDS=0.1 VOLTS
L / W =1 6 μm / 32 μm

EXTRACTION: The transconductance GM is measured at the peak value. The threshold voltage VT is the voltage VG where current starts to increase. Use the intersection of a straight line with the ID = 0 axis (or with a horizontal line at ID equal leakage current)

CHANNEL DEFINITION

	NAME		SOURCE	
CHAN	**V**	**I**	**MODE**	**FCT**
SMU1	VS	IS	COM	CONST
SMU2	VG	IG	V	VAR1
SMU3	VD	ID	V	VAR2
SMU4	VB	IB	V	CONST
Vs 1		----------	V	
Vs 2		----------	V	
Vm 1		----------	----------	----------
Vm 2		----------	----------	----------
USER FCTN				
1	GM	(/OHM) =	DELTA ID /	DELTA VG
2				

SOURCE SET UP

	VAR 1	VAR 2
NAME	VG	VB
SWEEP MODE	LINEAR	LINEAR
START	0	0.1
STOP	- 5 V	--------
STEP	- 0.1 V	-1
NO. OF STEP	51	0
COMPLIANCE	1 mA	50 mA
CONSTANT		
VS COM	0 V	105 mA
VSUB V		

DISPLAY MODE: GRAPHICS

	X axis	Y1 axis	Y2 axis
NAME	VG	ID	GM
SCL	LINEAR	LINEAR	LINEAR
MIN	-5 V	0 A	0
MAX	0 V	- 1 mA	50 μ mho

TEST NAME: **PSUBVT** PMOSFET SUB THRESHOLD CURRENT VS VGS (VDS=0.1)
L / W = 16 µm / 32 µm

EXTRACTION: The subthreshold slope in millivolts per decade is measured by drawing a straight line through the region where the current drecreases below VT. Minimum value of drain current Isub-min and the maximum value Isub-max is read off the curve at 0 and - 5 volts

*** VERY IMPORTANT — MICROSOPE LIGHT MUST BE OFF DURING THE MEASUREMENT.

CHANNEL DEFINITION

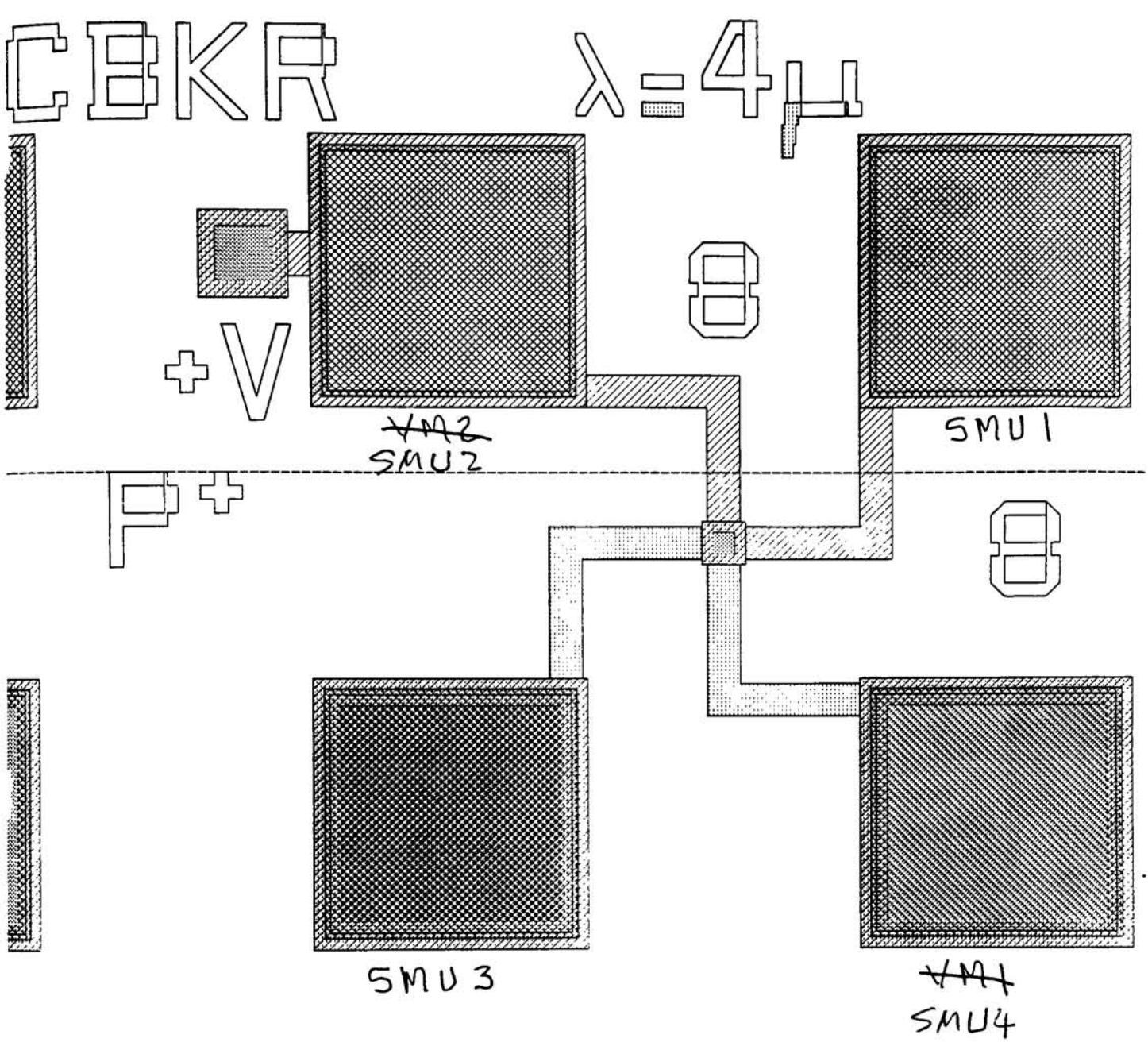
	NAME		SOURCE	
CHAN	**V**	**I**	**MODE**	**FCT**
SMU1	VS	IS	COM	CONST
SMU2	VG	IG	V	VAR1
SMU3	VD	ID	V	VAR2
SMU4	VB	IB	V	CONST
Vs 1		----------	V	
Vs 2		----------	V	
Vm 1		----------	----------	----------
Vm 2		----------	----------	----------
USER FCTN				
1				
2				

SOURCE SET UP

	VAR 1	**VAR 2**
NAME	VG	
SWEEP MODE	LINEAR	LINEAR
START	0	
STOP	-5 V	----
STEP	-0.05 V	
NO. OF STEP	101	
COMPLIANCE	1 mA	
CONSTANT		
VS COM	0	105 mA
VSUB V	-0.100 V	100 mA
VB. COM	0	105 mA

DISPLAY MODE: GRAPHICS

	X axis	**Y1 axis**	**Y2 axis**
NAME	VG	ID	SUBVT
SCL	LINEAR	LOG	LINEAR
MIN	0	-1 nA	0
MAX	-5	-1 mA	-1



W · VAN DER PAUW

TEST NAME: **OCBKR** METAL TO P+ CONTACT CONDUCTANCE / μm^2

EXTRACTION: Apply a current to two adjacent pads and measure the voltage across the other two pads. The contact resistance RC is (V/I). The designer needs a value that is a funtion of the contact area. The contact conductance per square micrometer, GC, can be multiplied by the contact area and inversed to give RC. So GC = (IF/V)/Area.

CHANNEL DEFINITION

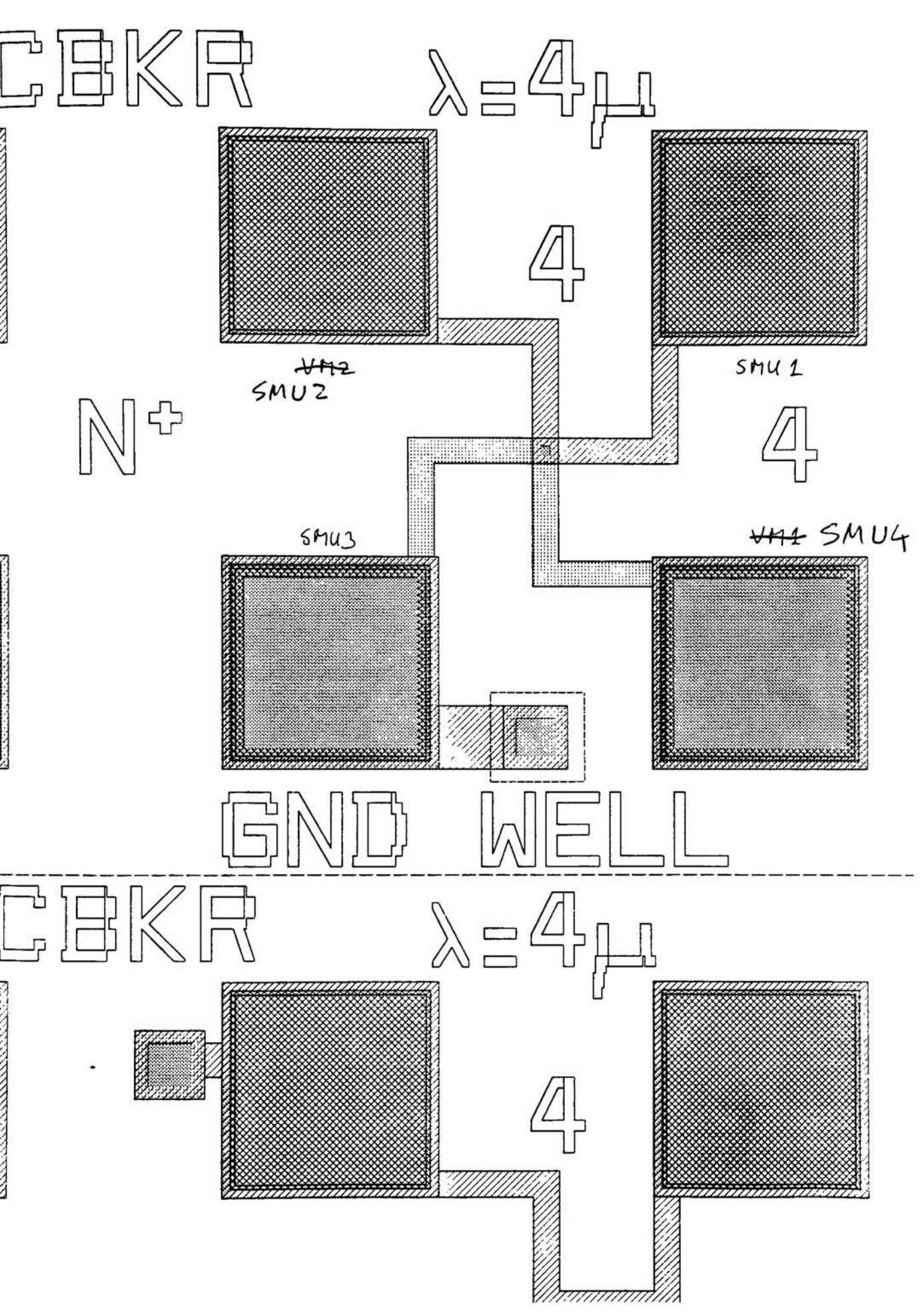
	NAME		SOURCE	
CHAN	**V**	**I**	**MODE**	**FCT**
SMU1	VF	IF	I	VAR1
SMU2	V_1	I_1	I	CONST
SMU3	V	I	COM	CONST
SMU4	V_2	I_2	I	CONST
Vs 1	~~VSUB~~	----------	V	~~CONST~~
Vs 2		----------	V	
Vm 1	~~V2~~	----------	----------	----------
Vm 2	~~V1~~	----------	----------	----------
USER FCTN				
1				
2	GC	(GC)=(IF / 64)	/ (V1-V2)	

SOURCE SET UP

	VAR 1	VAR 2
NAME SWEEP MODE	IF	
~~TEST NAME: W~~	LINEAR	
START	0	
~~CHANNEL~~ STOP	10.00 mA	
STEP	100.0uA	
NO. OF STEP	101	
~~SOURCE SET UP~~ COMPLIANCE	20.00V	
CONSTANT ~~DISPLAY MODE:~~		
VS COM	0	105 mA
~~VSUB~~ I_1 I	~~5.000 V~~ 0	0.1 V
I_2 I	0	0.1 V

DISPLAY MODE: GRAPHICS

	X axis	Y1 axis	Y2 axis
NAME	IF	VF	GC
SCL	LINEAR	LINEAR	LINEAR
MIN	0	0	0
MAX	10 mA	~~20~~ 2 V	~~0.2~~ 350E-6


CBKR
λ=4μ
4
~~VM2~~
SMU2
SMU 1
N+
4
SMU3
~~VM1~~ SMU4
GND WELL
CBKR
λ=4μ
4

TEST NAME: **NCBKR** METAL TO N+ CONTACT CONDUCTANCE/μm^2

EXTRACTION: Apply a current to two adjacent pads and measure the voltage across the other two pads. The contact resistance RC is (V/I). The designer needs a value that is a funtion of the contact area. The contact conductance per square micrometer, GC, can be multiplied by the contact area and inversed to give RC. So GC = (IF/V)/Area.

CHANNEL DEFINITION

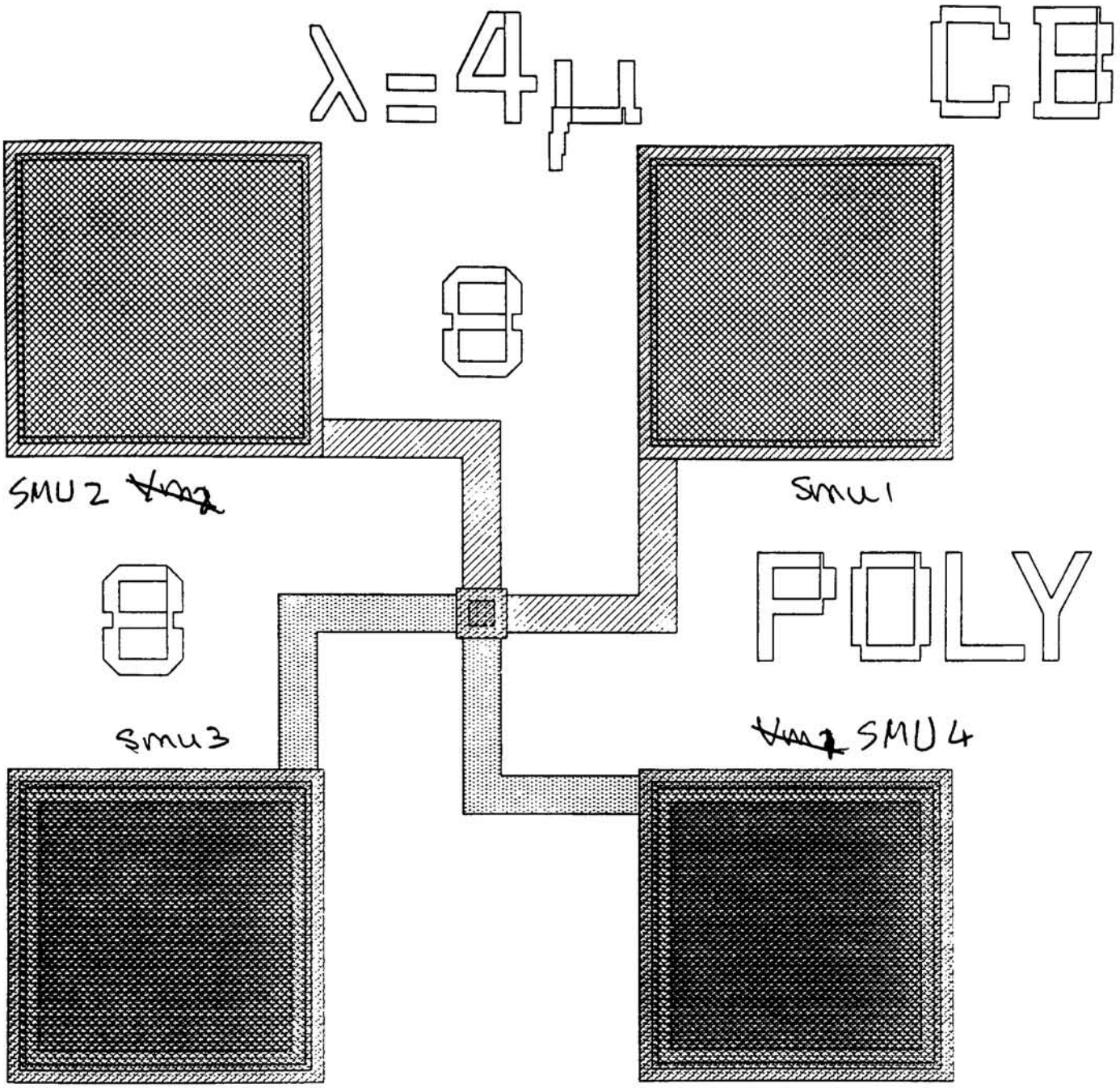
	NAME		SOURCE	
CHAN	**V**	**I**	**MODE**	**FCT**
SMU1	VF	IF	I	VAR1
SMU2	V_1	I_1	I	CONST
SMU3	V	I	COM	CONST
SMU4	V_2	I_2	I	CONST
Vs 1	~~VSUB~~	----------	V	~~CONST~~
Vs 2		----------	V	
Vm 1	~~V2~~	----------	----------	----------
Vm 2	~~V1~~	----------	----------	----------
USER FCTN				
1				
2	GC	(GC)=(IF / 16)	/ (VI-V2)	

SOURCE SET UP

	VAR 1	VAR 2
NAME	IF	
SWEEP MODE	LINEAR	
START	0	
STOP	10.00 mA	
STEP	100.0uA	
NO. OF STEP	101	
COMPLIANCE	20.00V	
CONSTANT		
~~VS~~ **COM**	0	103 mA
~~VSUB~~ I_1 ~~V~~ I	~~5.000 V~~ 0	0.1 V
I_2 I	0	0.1 V

DISPLAY MODE: GRAPHICS

	X axis	Y1 axis	Y2 axis
NAME	IF	VF	GC
SCL	LINEAR	LINEAR	LINEAR
MIN	0	0	0
MAX	10 mA	20 V	~~0.2~~ 10E-3


λ=4μ
CB
SMU 2
SMU 1
POLY
SMU 3
SMU 4

PCBKR

TEST NAME: ~~MCBKR~~ METAL TO POLY CONTACT CONDUCTANCE/μm^2

EXTRACTION: Apply a current to two adjacent pads and measure the voltage across the other two pads. The contact resistance RC is (V/I). The designer needs a value that is a funtion of the contact area. The contact conductance per square micrometer, GC, can be multiplied by the contact area and inversed to give RC. So GC = (IF/V)/Area.

CHANNEL DEFINITION

	NAME		SOURCE	
CHAN	**V**	**I**	**MODE**	**FCT**
SMU1	VF	IF	I	VAR1
SMU2	V_1	I_1	I	CONST
SMU3	V	I	COM	CONST
SMU4	V_2	I_2	I	CONST
Vs 1	~~VSUB~~	----------	V	~~CONST~~
Vs 2		----------	~~V~~	
Vm 1	~~V2~~	----------	----------	----------
Vm 2	~~V1~~	----------	----------	----------
USER FCTN				
1				
2	GC	(GC)=(IF / 64)	/ (V1-V2)	

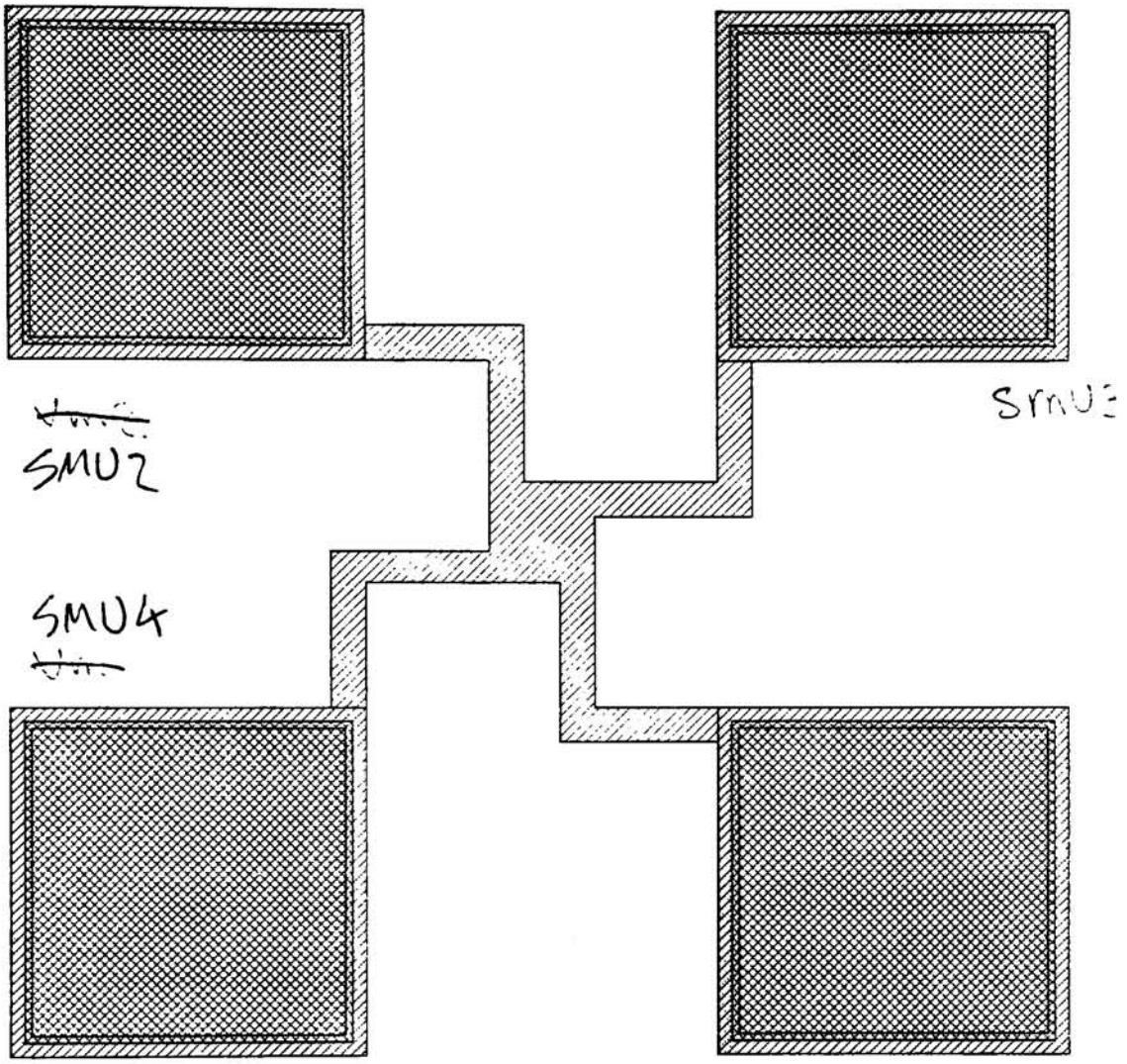
SOURCE SET UP

	VAR 1	VAR 2
NAME	IF	
SWEEP MODE	LINEAR	
START	0	
STOP	10.00 mA	
STEP	100.0uA	
NO. OF STEP	101	
COMPLIANCE	20.00V	
CONSTANT		
VS COM	0	105 mA
~~VSUB~~ I, ~~V~~ I	~~5.000 V~~ 0	0.1 V
. I_2 I	0	0.1 V

DISPLAY MODE: GRAPHICS

	X axis	Y1 axis	Y2 axis
NAME	IF	VF	GC
SCL	LINEAR	LINEAR	LINEAR
MIN	0	0	0
MAX	10 mA	20 V	~~5E-2~~ 5E-3

VAN DER PAUW



METAL

TEST NAME: **MPAW** METAL VAN DER PAUW

EXTRACTION: Apply a current to two adjacent pads and measure the voltage across the other two pads. The sheet resistance RS is (V/I)(Pi/ln2). The value of RS is measured in the flat region of the RS vs IF curve. The VF value will be small because metal is such a good conductor as a result the measurement will be noisy.

CHANNEL DEFINITION

	NAME		SOURCE	
CHAN	V	I	MODE	FCT
SMU1	VF	IF	I	VAR1
SMU2	~~V1~~	I1	I	CONST
SMU3	V	I	COM	CONST
SMU4	V2	I2	I	CONST
Vs 1	~~VSUB~~	----------	V	~~CONST~~
Vs 2		----------	V	
Vm 1	~~V2~~	----------	----------	----------
Vm 2	~~V1~~	----------	----------	----------
USER FCTN				
1				
2	RS	(RS)=(V1-V2)	*4.532 / IF	

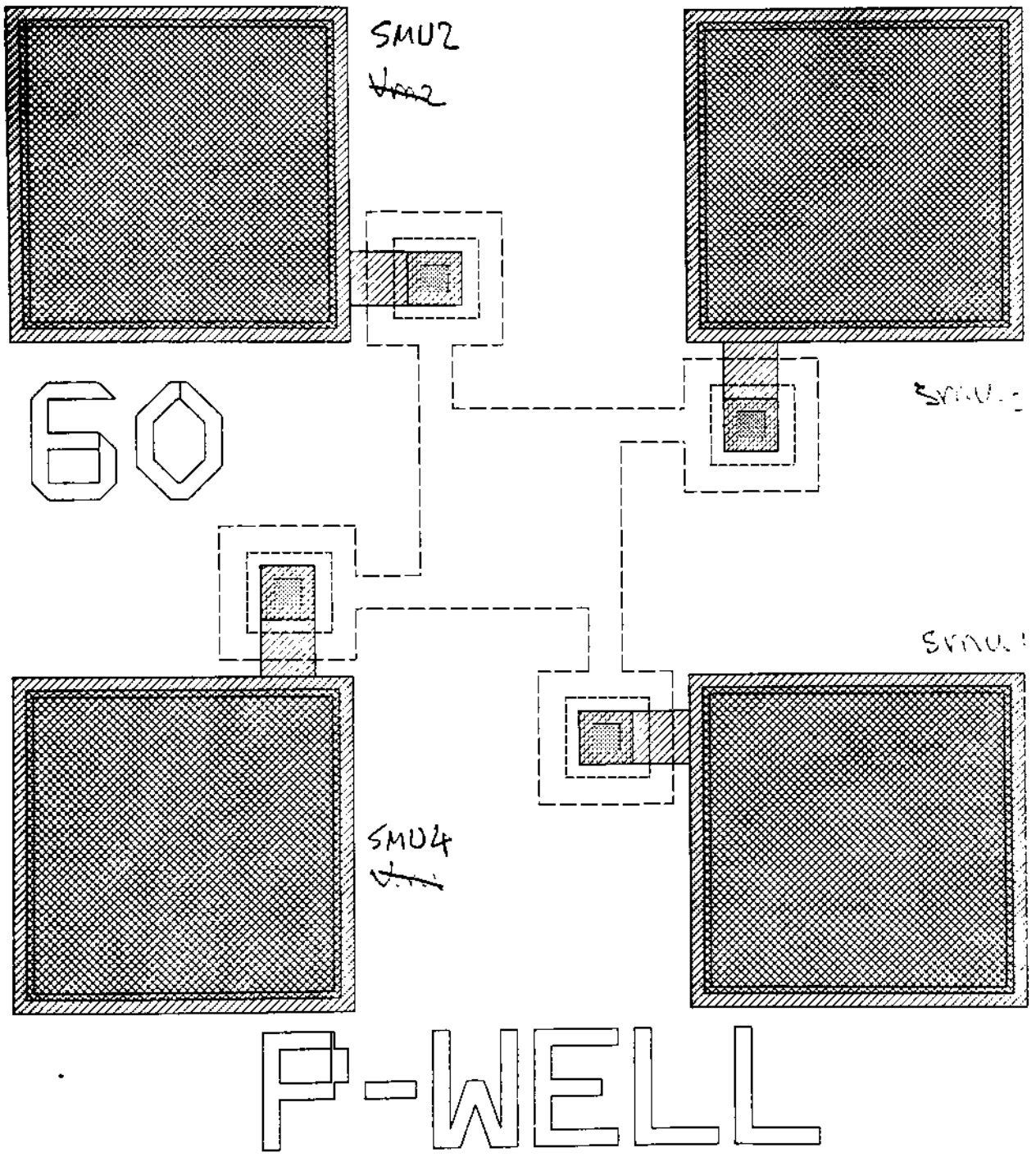
SOURCE SET UP

	VAR 1	VAR 2
NAME	IF	
SWEEP MODE	LINEAR	
START	0	
STOP	40.00 mA	
STEP	200.0uA	
NO. OF STEP	201	
COMPLIANCE	20.00V	
CONSTANT		
VS COM	0	105 mA
~~VSUB~~ I1 I	~~5.000 V~~ 0.A	10 V
I2 I	0 A	10 V

DISPLAY MODE: GRAPHICS

	X axis	Y1 axis	Y2 axis
NAME	IF	VF	RS
SCL	LINEAR	LINEAR	LINEAR
MIN	0	0	0
MAX	40.0 mA	0.2 V	0.5 ohms

VAN DER PAUW



TEST NAME: **WPAW** P-WELL VAN DER PAUW

EXTRACTION: Apply a current to two adjacent pads and measure the voltage across the other two pads. The sheet resistance RS is (V/I)(Pi/ln2). The value of RS is measured in the flat region of the RS vs IF curve. The VF value will be large for small If because the well resistance is high. Be sure VF is not in compliance. That is VF should be increasing not flat at data point.

CHANNEL DEFINITION

	NAME		SOURCE	
CHAN	V	I	MODE	FCT
SMU1	VF	IF	I	VAR1
SMU2	V_1	I_1	I	CONST
SMU3	V	I	COM	CONST
SMU4	V_2	I_2	I	CONST
Vs 1	~~VSUB~~	----------	V	~~CONST~~
Vs 2		----------	V	
Vm 1	~~V2~~	----------	----------	----------
Vm 2	~~V1~~	----------	----------	----------
USER FCTN				
1				
2	RS	(RS)=(V1-V2)	*4.532 / IF	

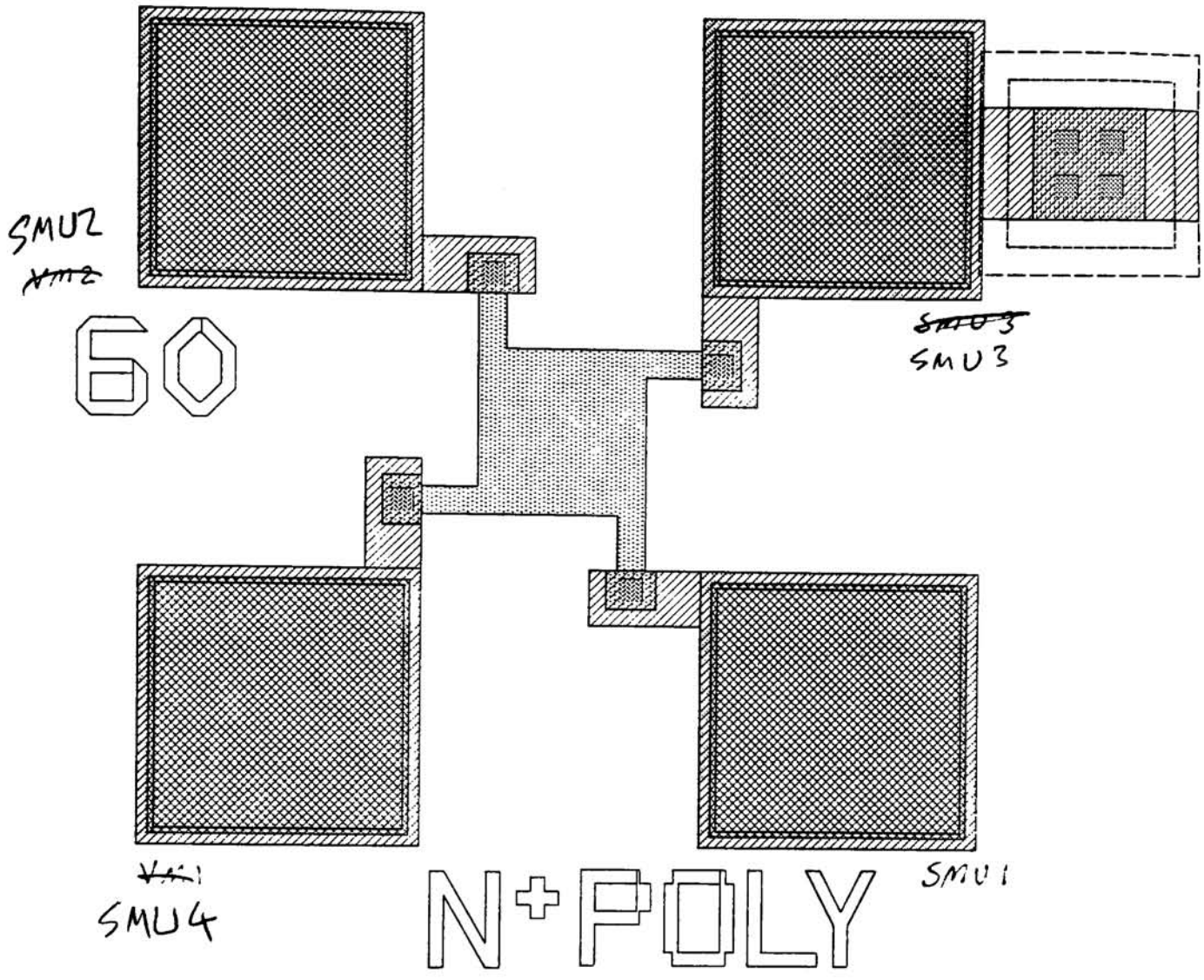
SOURCE SET UP

	VAR 1	VAR 2
NAME	IF	
SWEEP MODE	LINEAR	
START	0	
STOP	500 µA	
STEP	5 µA	
NO. OF STEP	101	
COMPLIANCE	20.00V	
CONSTANT		
VS\ COM	0	105 mA
~~VSUB~~ I_1 I_1	~~5.000 V~~ 0.A	10 V
I_2 I	0.A	10 V

DISPLAY MODE: GRAPHICS

	X axis	Y1 axis	Y2 axis
NAME	IF	VF	RS
SCL	LINEAR	LINEAR	LINEAR
MIN	0	0	0
MAX	500 µA	10.0 V	8000 ohms

VAN DER PAUW



NMOS VT

TEST NAME: **OPAW** N+ POLY SILICON VAN DER PAUW

EXTRACTION: Apply a current to two adjacent pads and measure the voltage across the other two pads. The sheet resistance RS is (V/I)(Pi/ln2). The value of RS is measured in the flat region of the RS vs IF curve. The VF value should be increasing at a constant slope.

CHANNEL DEFINITION

	NAME		SOURCE	
CHAN	V	I	MODE	FCT
SMU1	VF	IF	I	VAR1
SMU2	V_1	I_1	I	CONST
SMU3	V	~~ICOM~~	COM	CONST
SMU4	V_2	I_2	I	CONST
Vs 1	~~VSUB~~	----------	~~V~~	~~CONST~~
Vs 2		----------	~~V~~	
Vm 1	~~V2~~	----------	----------	----------
Vm 2	~~V1~~	----------	----------	----------
USER FCTN				
1				
2	RS	(RS)=(V1-V2)	*4.532 / IF	

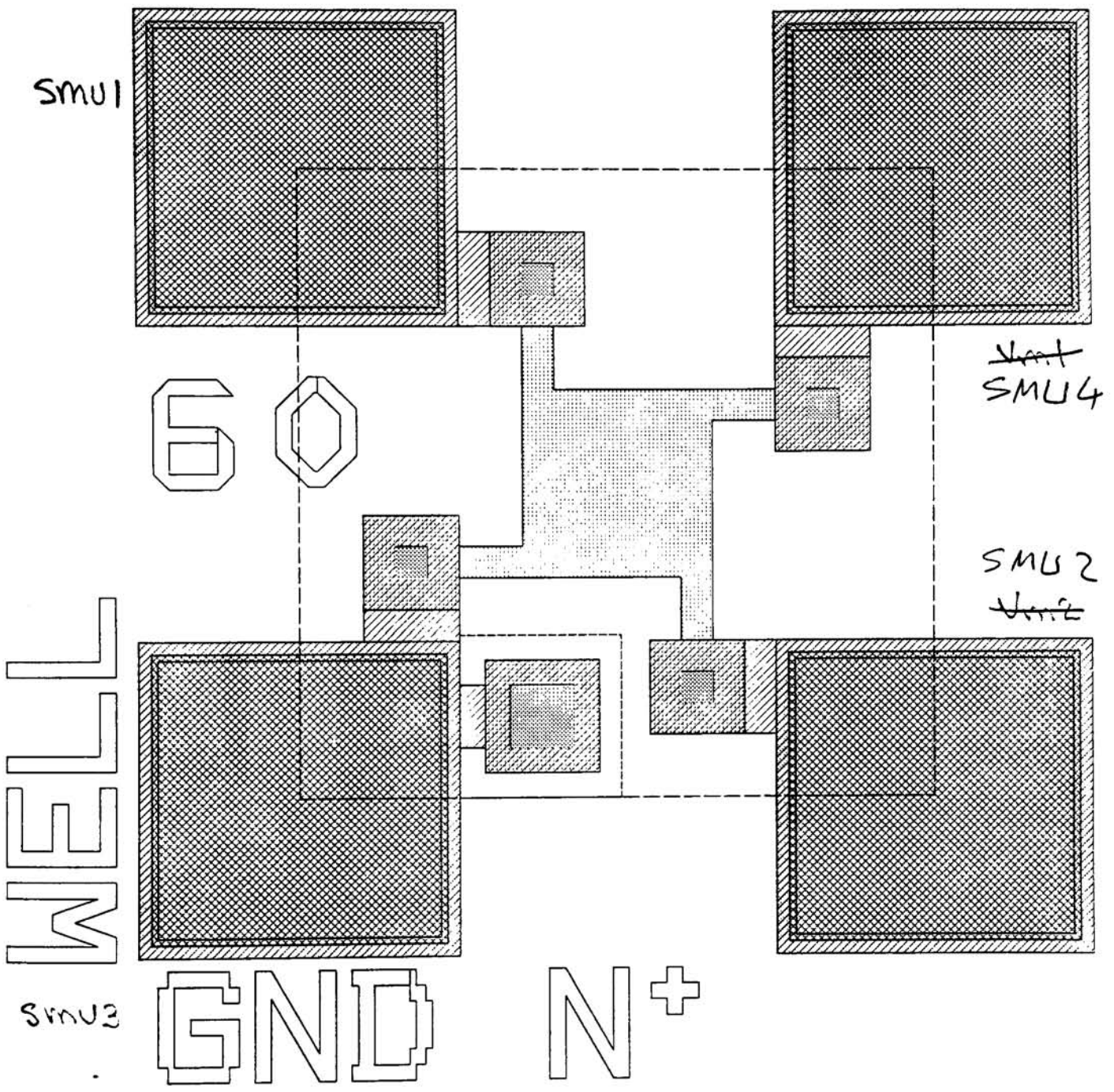
SOURCE SET UP

	VAR 1	VAR 2
NAME	IF	
SWEEP MODE	LINEAR	
START	0	
STOP	10.00 mA	
STEP	100.0uA	
NO. OF STEP	101	
COMPLIANCE	20.00V	
CONSTANT		
VS COM	0	1.05 mA
~~VSUB~~ I, X I	~~5.000 V~~ 0 A	10 V
I_2 I	0 A	10 V

DISPLAY MODE: GRAPHICS

	X axis	Y1 axis	Y2 axis
NAME	IF	VF	RS
SCL	LINEAR	LINEAR	LINEAR
MIN	0	0	0
MAX	10.0 mA	10.0 V	200 ohms

VAN DER PAUW



TEST NAME: **NPAW** N+ DRAIN/SOURCE VAN DER PAUW

EXTRACTION: Apply a current to two adjacent pads and measure the voltage across the other two pads. The sheet resistance RS is (V/I)(Pi/ln2). The value of RS is measured in the flat region of the RS vs IF curve. The VF value should be increasing at a constant slope.

CHANNEL DEFINITION

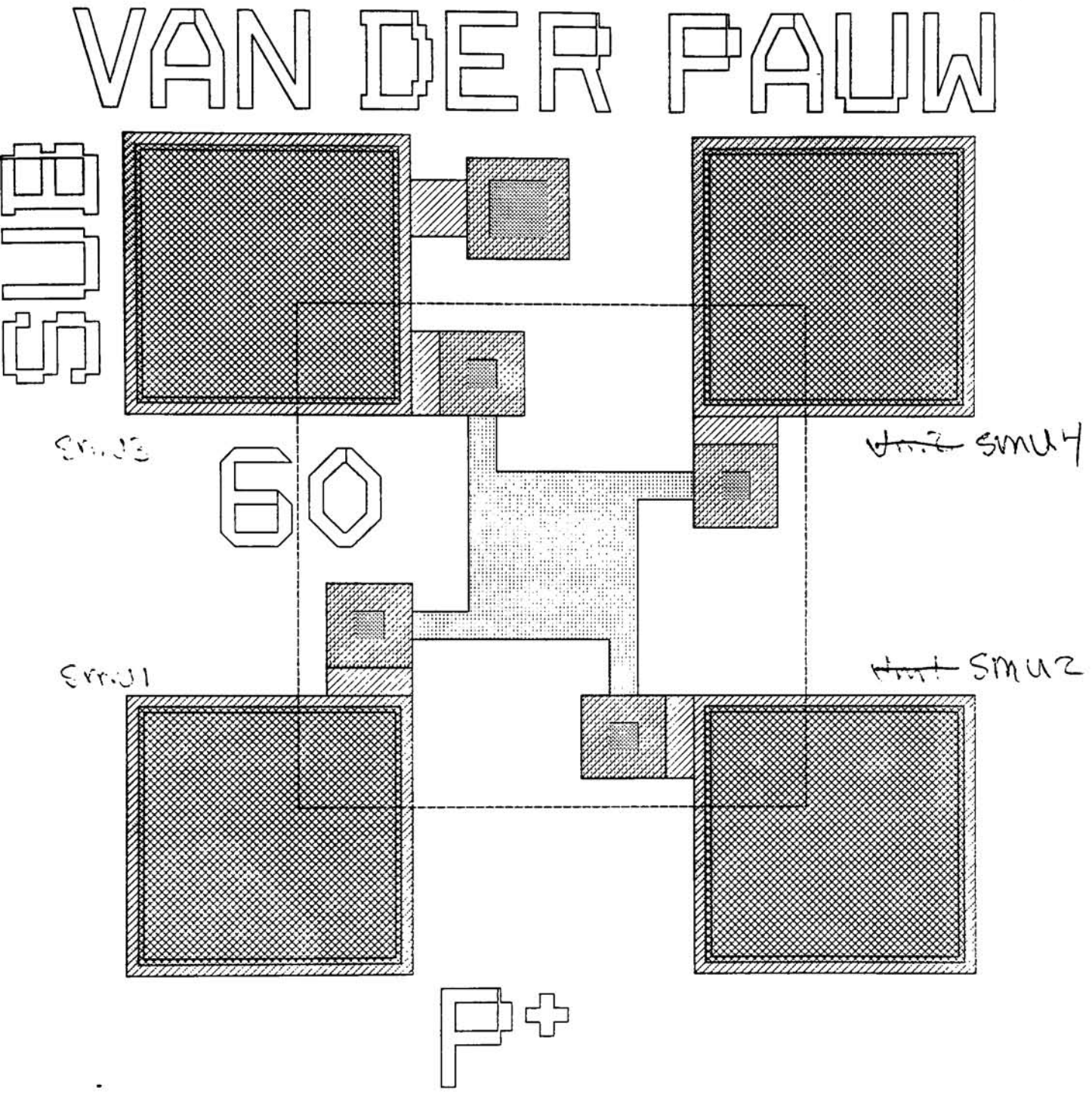
	NAME		SOURCE	
CHAN	V	I	MODE	FCT
SMU1	VF	IF	I	VAR1
SMU2	V_1	I_1	I	CONST
SMU3	V	I	COM	CONST
SMU4	~~V_2~~	I_2	I	CONST
Vs 1	~~VSUB~~	----------	~~V~~	~~CONST~~
Vs 2		----------	~~V~~	
Vm 1	~~V2~~	----------	----------	----------
Vm 2	~~V1~~	----------	----------	----------
USER FCTN				
1				
2	RS	(RS)=(V1-V2)	*4.532 / IF	

SOURCE SET UP

	VAR 1	VAR 2
NAME	IF	
SWEEP MODE	LINEAR	
START	0	
STOP	10.00 mA	
STEP	100.0uA	
NO. OF STEP	101	
COMPLIANCE	20.00V	
CONSTANT		
~~V~~ COM	0	105 mA
~~VSUB~~ I_1 V I COM	~~0/5.000 V~~	10 V
I_2 I	0. A	10 V

DISPLAY MODE: GRAPHICS

	X axis	Y1 axis	Y2 axis
NAME	IF	VF	RS
SCL	LINEAR	LINEAR	LINEAR
MIN	0	0	0
MAX	10.0 mA	2.0 V	200 ohms


VAN DER PAUW
SUB
60
SMU4
SMU2
P+

TEST NAME: **PPAW** P+ DRAIN/SOURCE VAN DER PAUW

EXTRACTION: Apply a current to two adjacent pads and measure the voltage across the other two pads. The sheet resistance RS is (V/I)(Pi/ln2). The value of RS is measured in the flat region of the RS vs IF curve. The VF value should be increasing at a constant slope.

CHANNEL DEFINITION

	NAME		SOURCE	
CHAN	**V**	**I**	**MODE**	**FCT**
SMU1	VF	IF	I	VAR1
SMU2	V1	I1	I	CONST
SMU3	V	I	COM	CONST
SMU4	V2	I2	I	CONST
Vs 1	~~VSUB~~	----------	~~V~~	~~CONST~~
Vs 2		----------	~~V~~	
Vm 1	~~V2~~	----------	----------	----------
Vm 2	~~V1~~	----------	----------	----------
USER FCTN				
1				
2	RS	(RS)=(V1-V2)	*4.532 / IF	

SOURCE SET UP

	VAR 1	VAR 2
NAME	IF	
SWEEP MODE	LINEAR	
START	0	
STOP	10.00 mA	
STEP	100.0uA	
NO. OF STEP	101	
COMPLIANCE	20.00V	
CONSTANT		
~~VS~~ I1 ~~COM~~ I	~~0~~ 0	~~105 mA~~ 10V
~~VSUB~~ V ~~V~~ COM	~~5.000~~ V 0	105mA
I2 I	0	10V

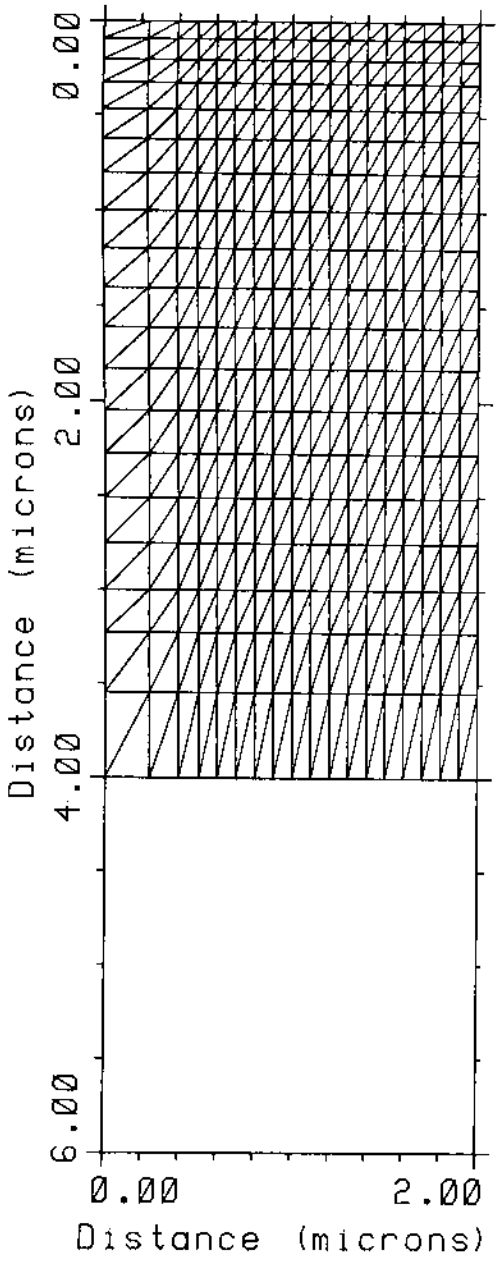
DISPLAY MODE: GRAPHICS

	X axis	Y1 axis	Y2 axis
NAME	IF	VF	RS
SCL	LINEAR	LINEAR	LINEAR
MIN	0	0	0
MAX	10.0mA	2.0 V	200 ohms

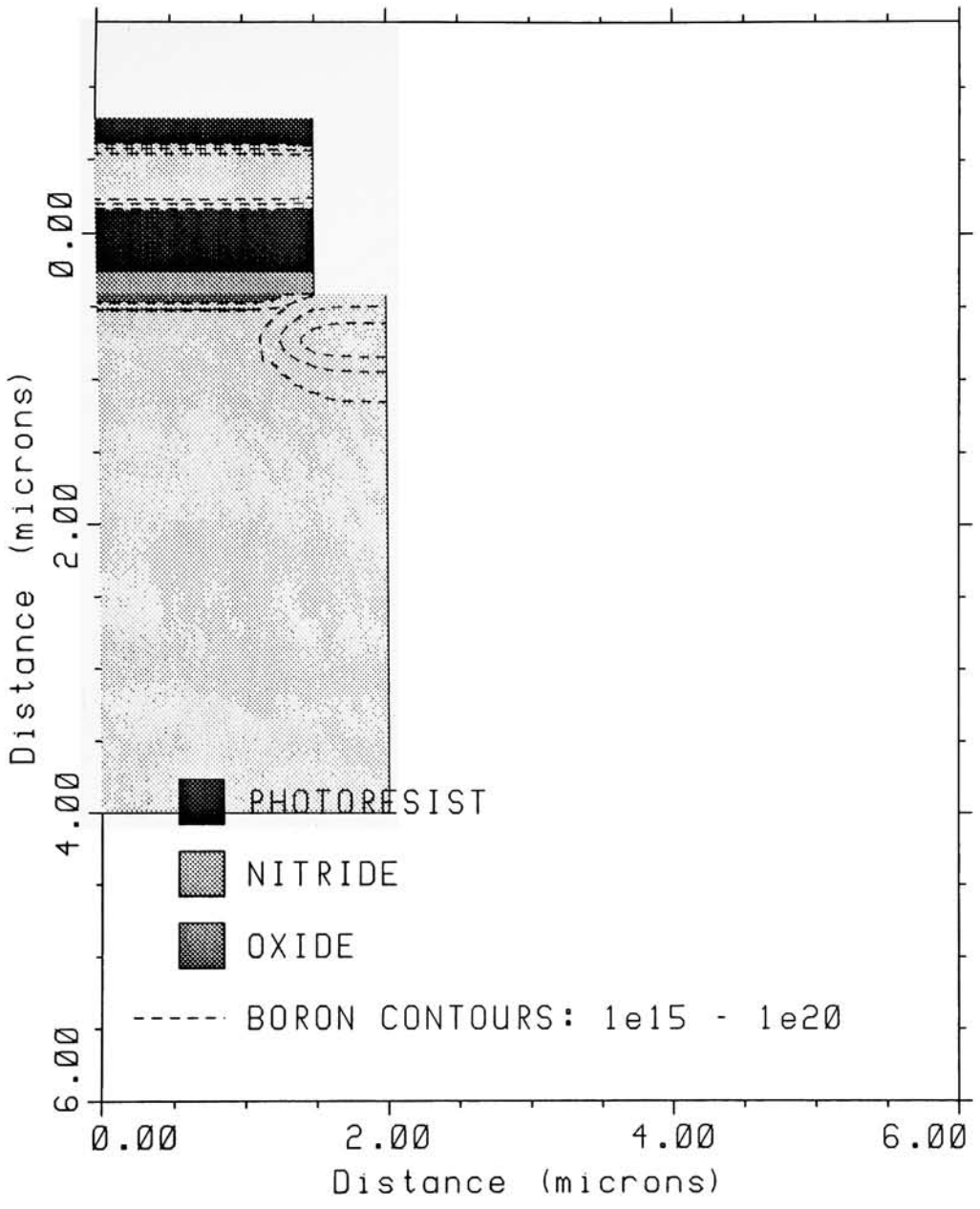
APPENDIX C

Process Simulation Files

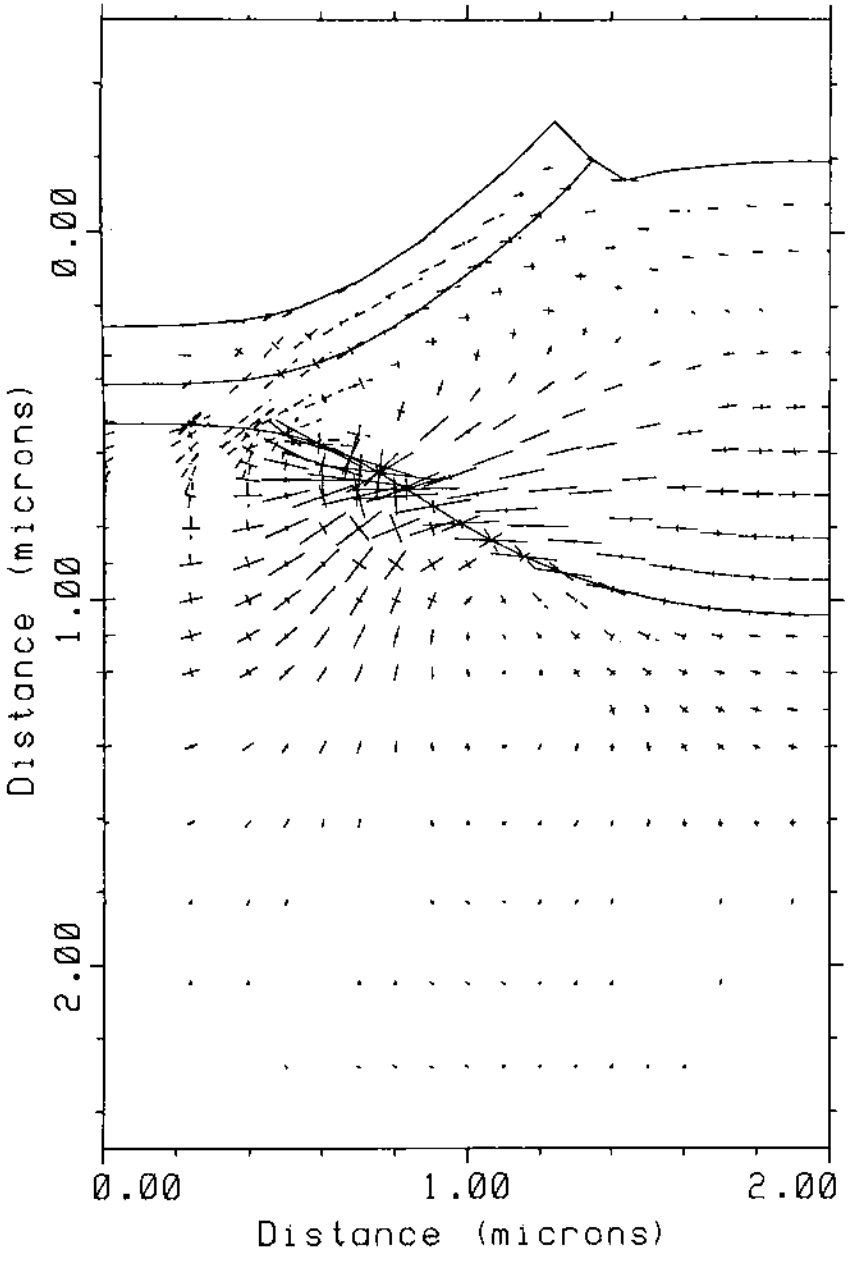
(CID) : INITIAL GRID FOR DEVICE

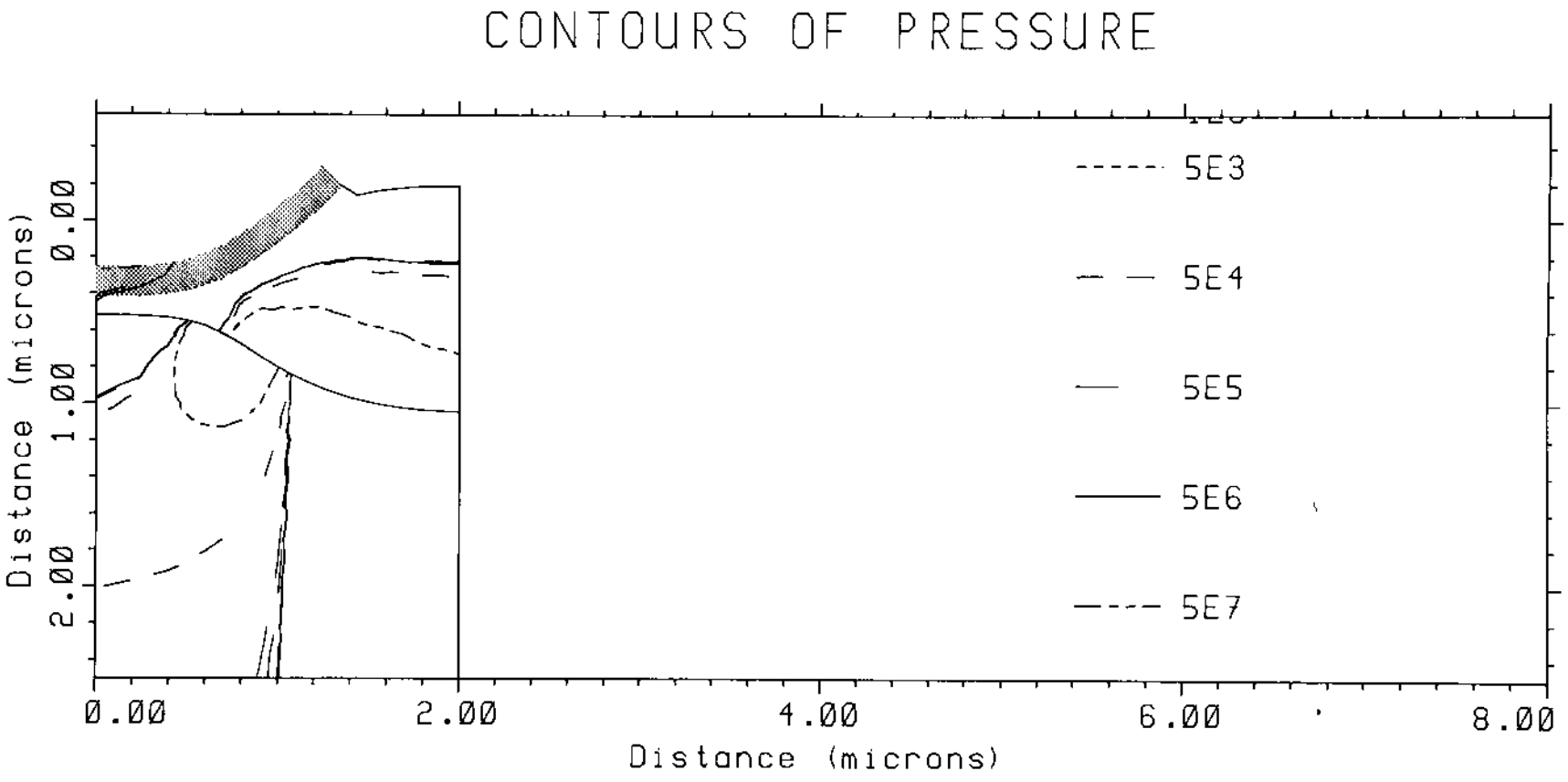


PMOS AFTER CHANNEL STOP IMPLANT

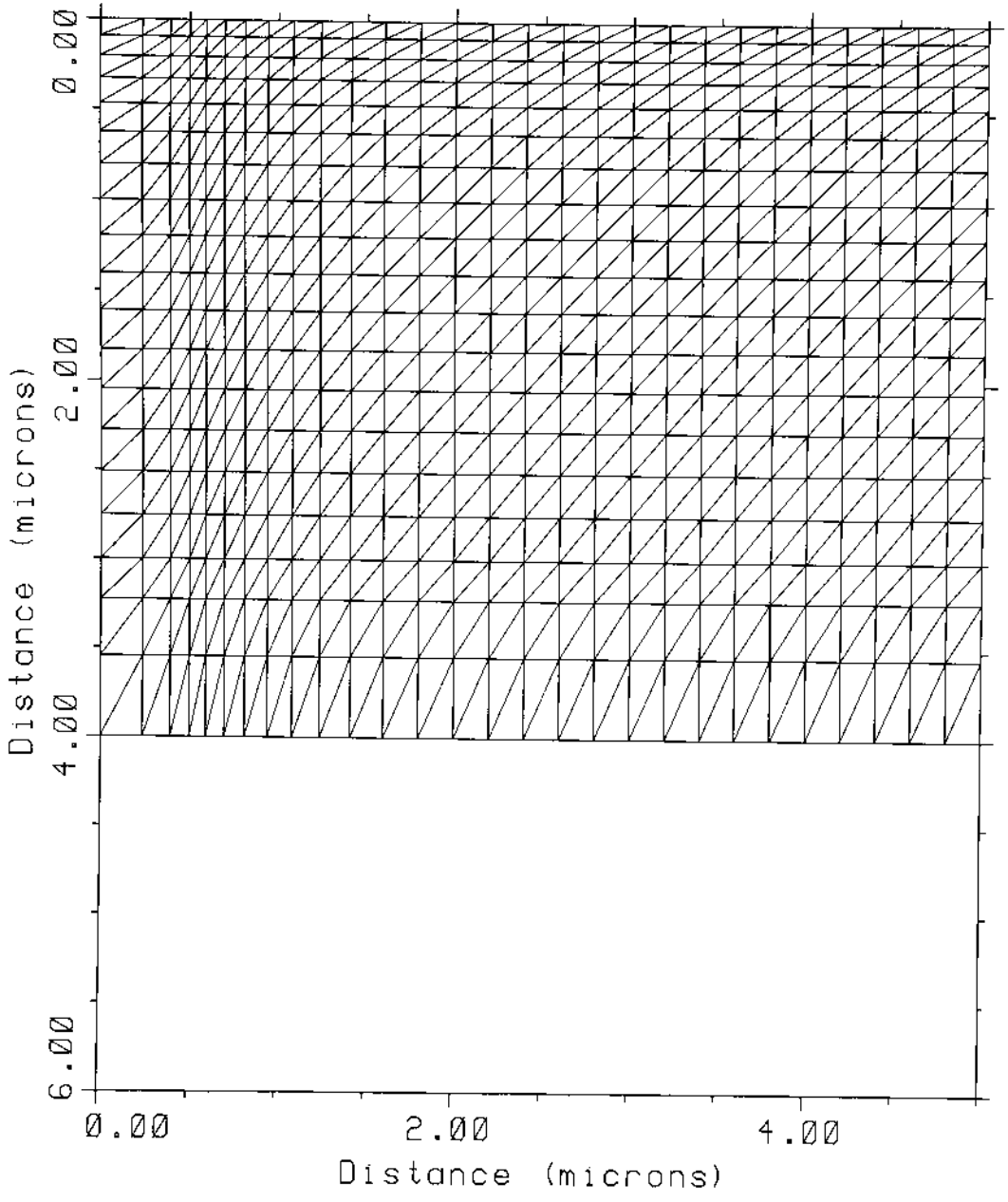


NDUCED STRESS IN SUBSTRATE AND OXIDE

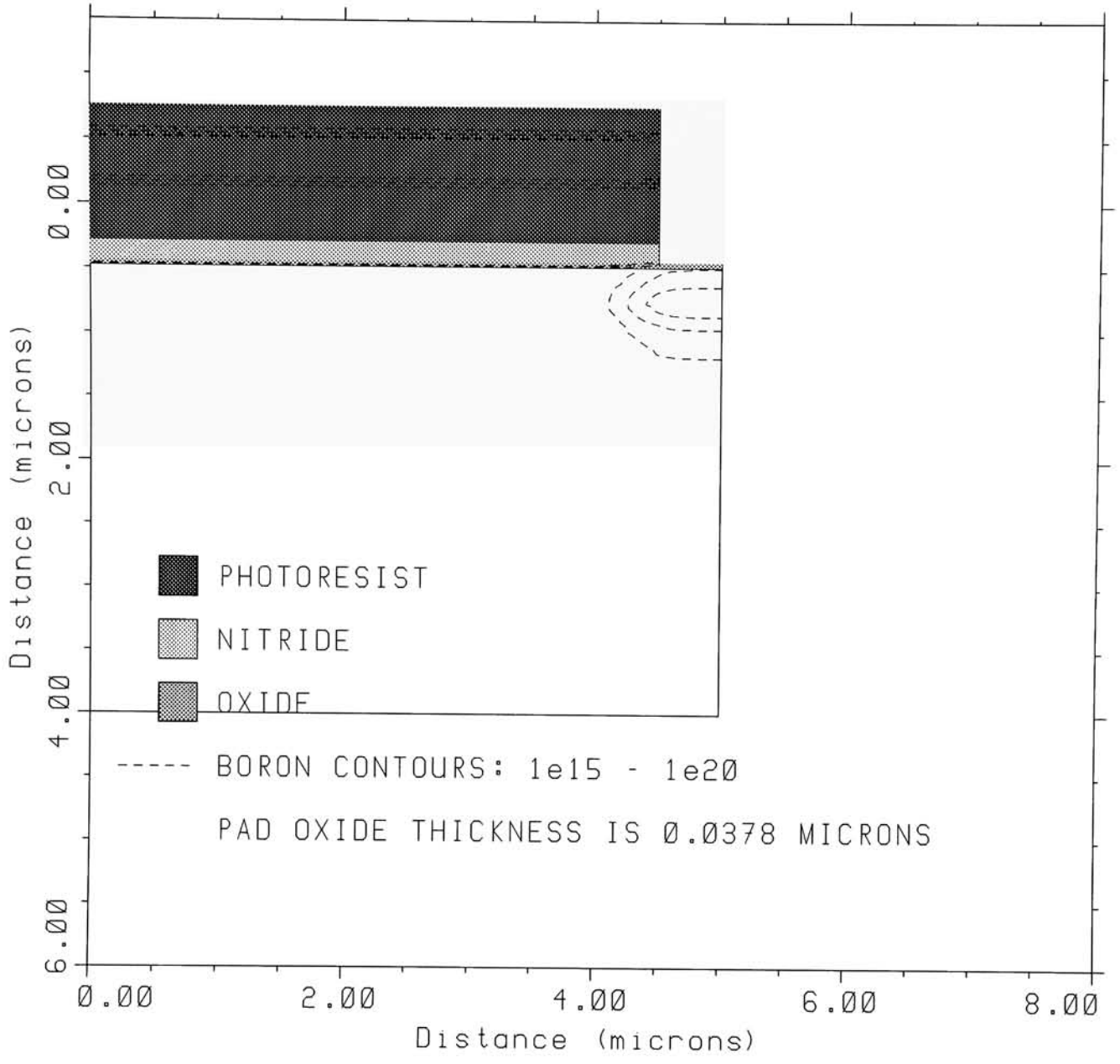



CONTOURS OF PRESSURE
5E3
5E4
5E5
5E6
5E7
Distance (microns)
0.00
1.00
2.00
0.00
2.00
4.00
6.00
8.00
Distance (microns)

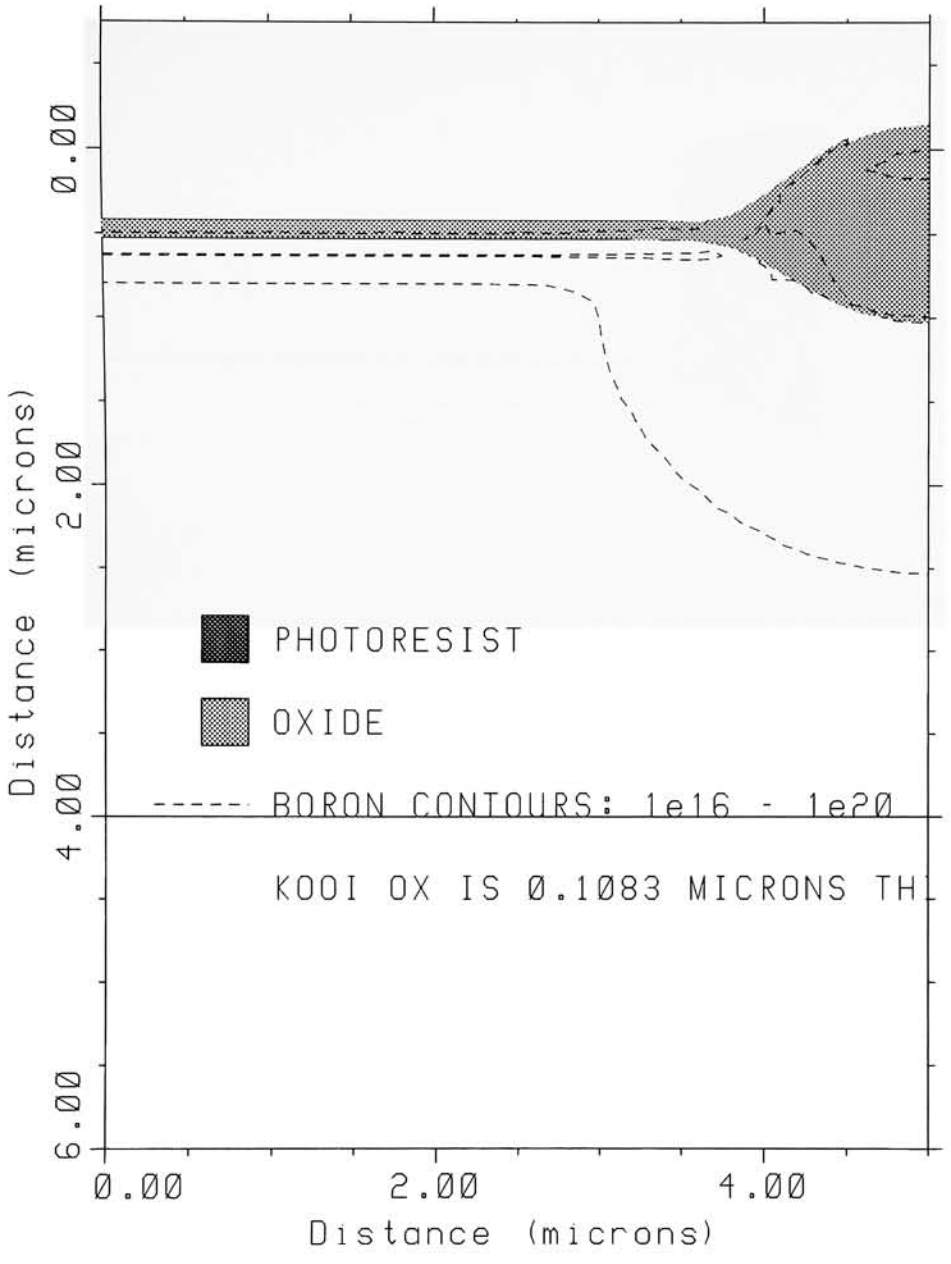
PWELL CMOS: INITIAL GRID FOR NMOS DEVICE



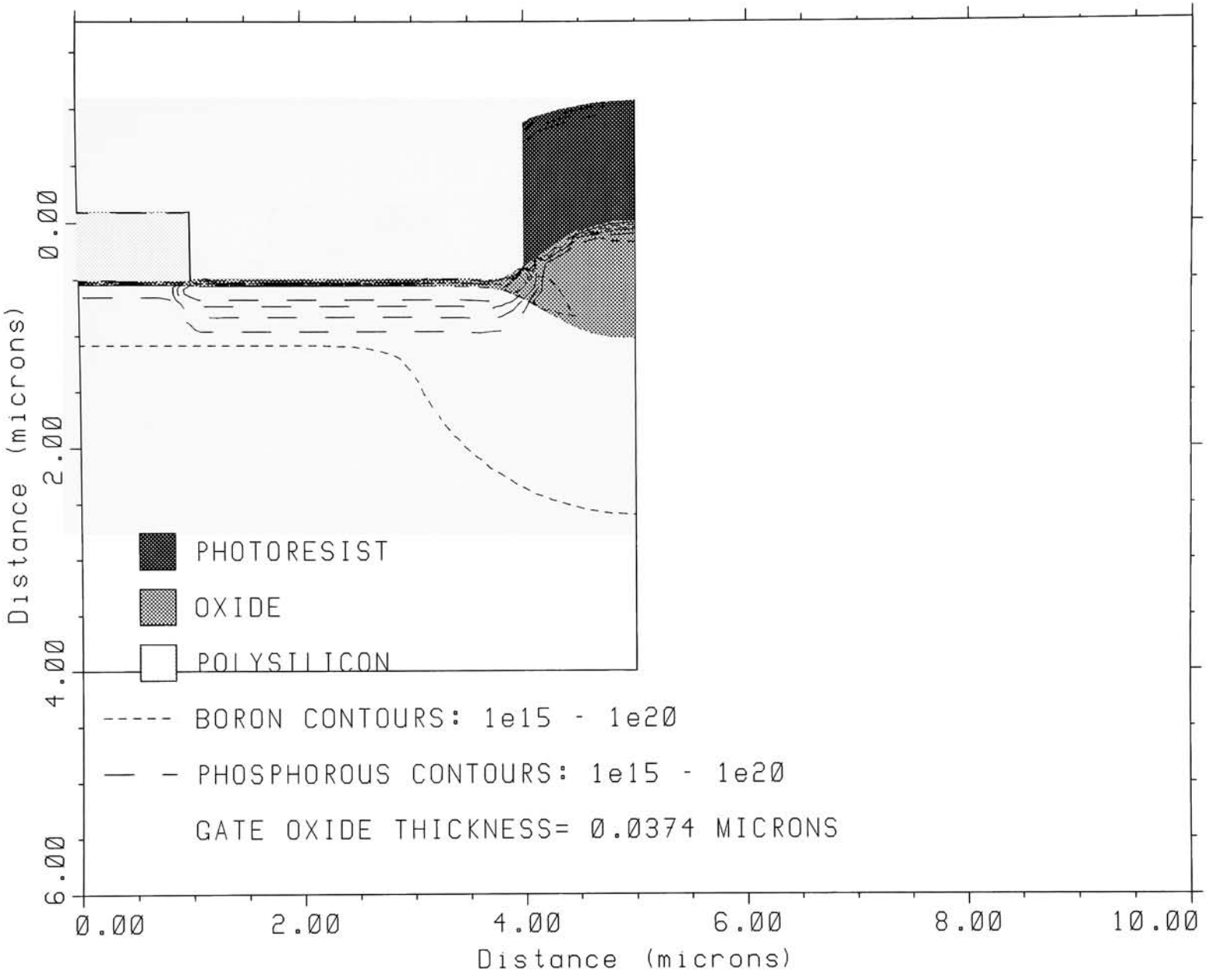
NMOS AFTER CHANNEL STOP IMPLANT



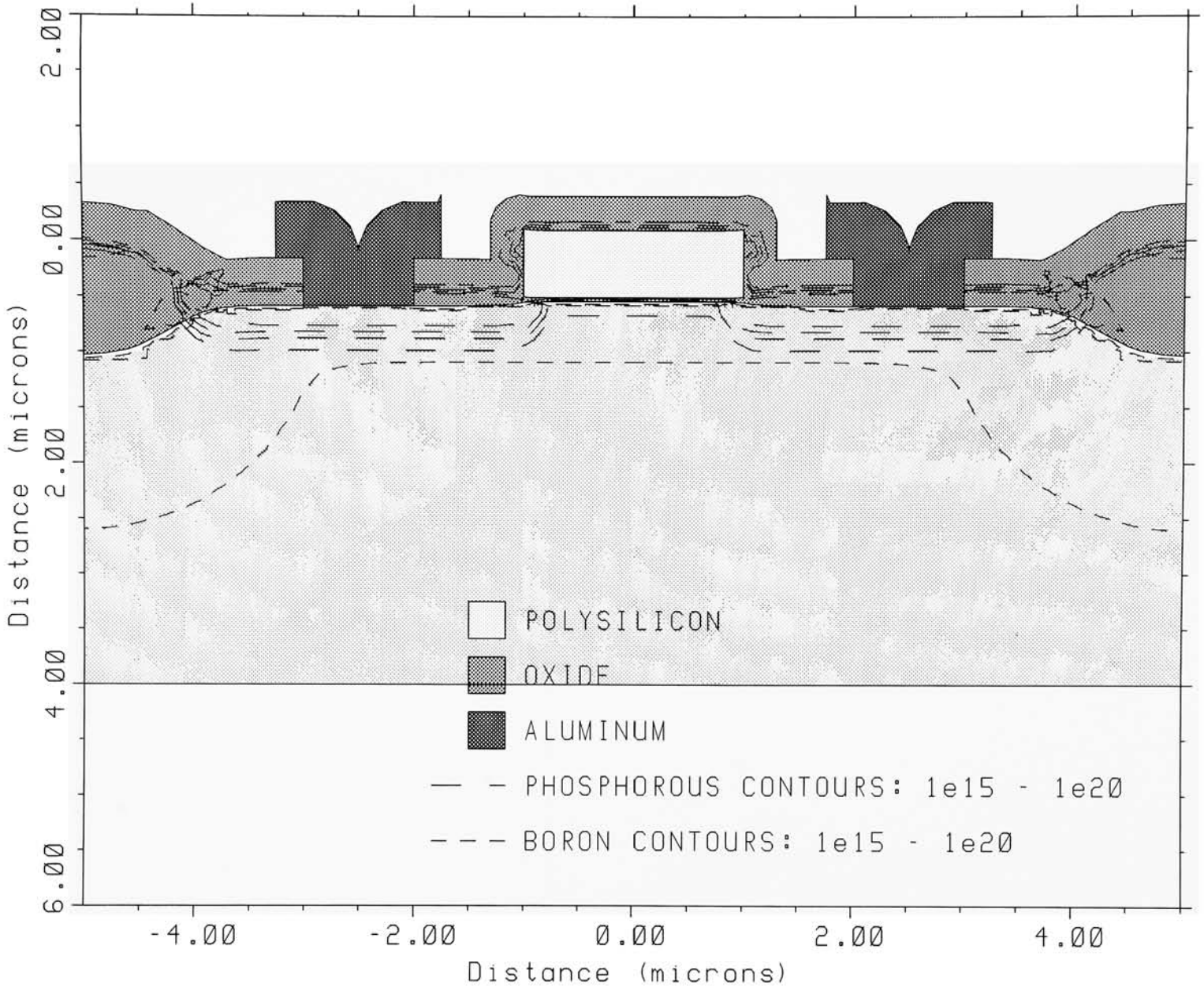
AFTER NMOS VT IMPLANT

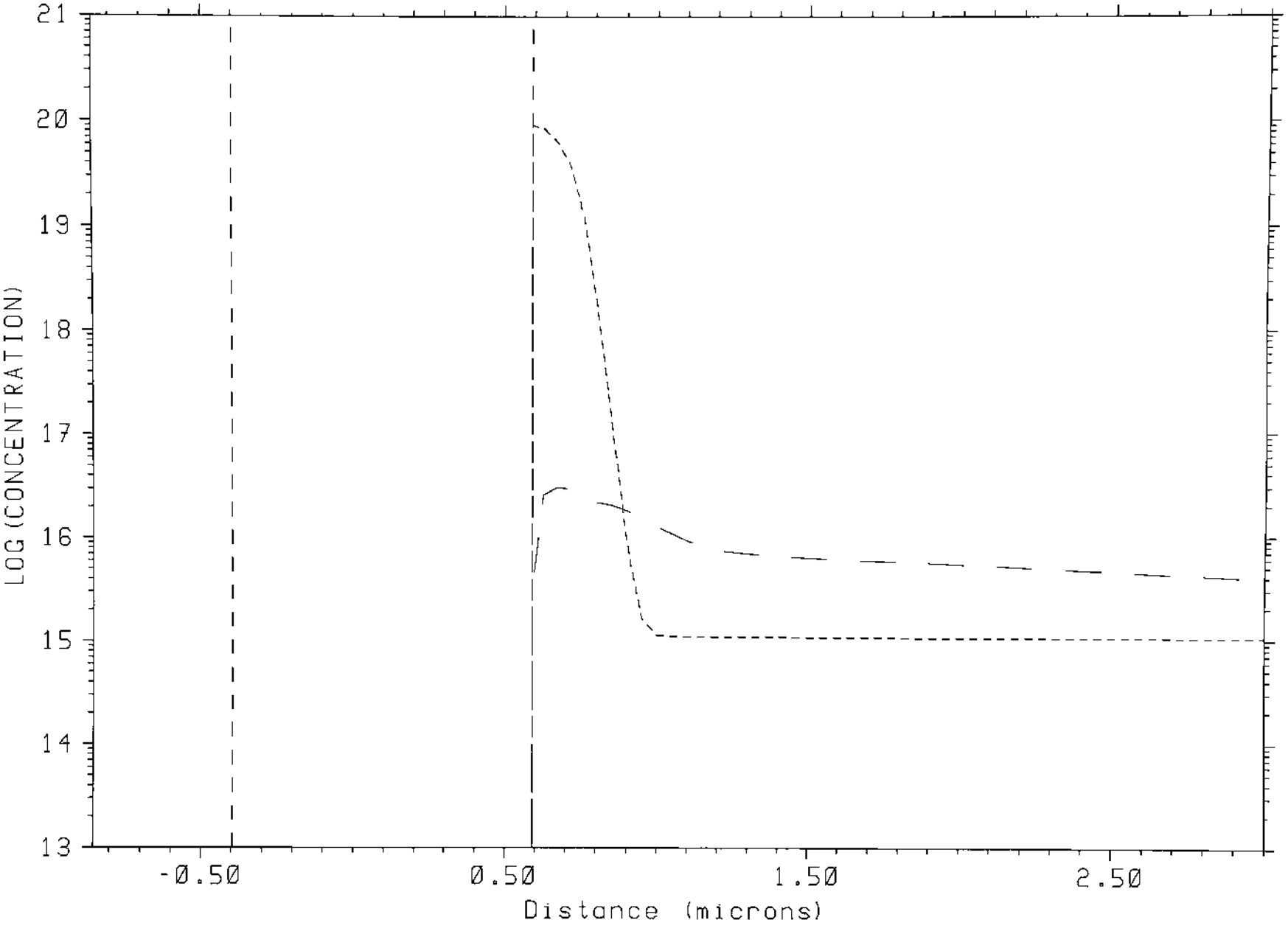


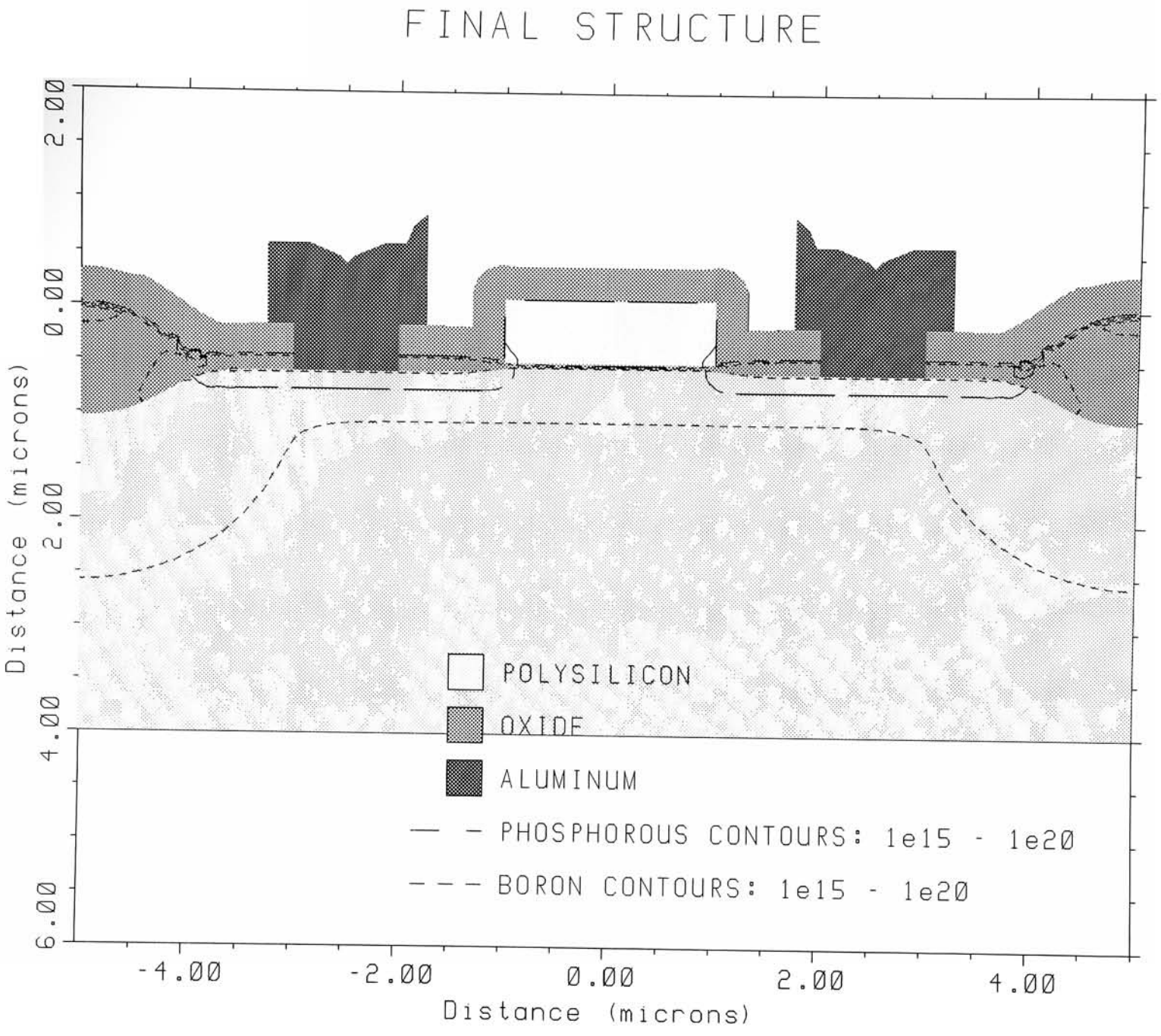
AFTER N+SOURCE/DRAIN IMPLANT

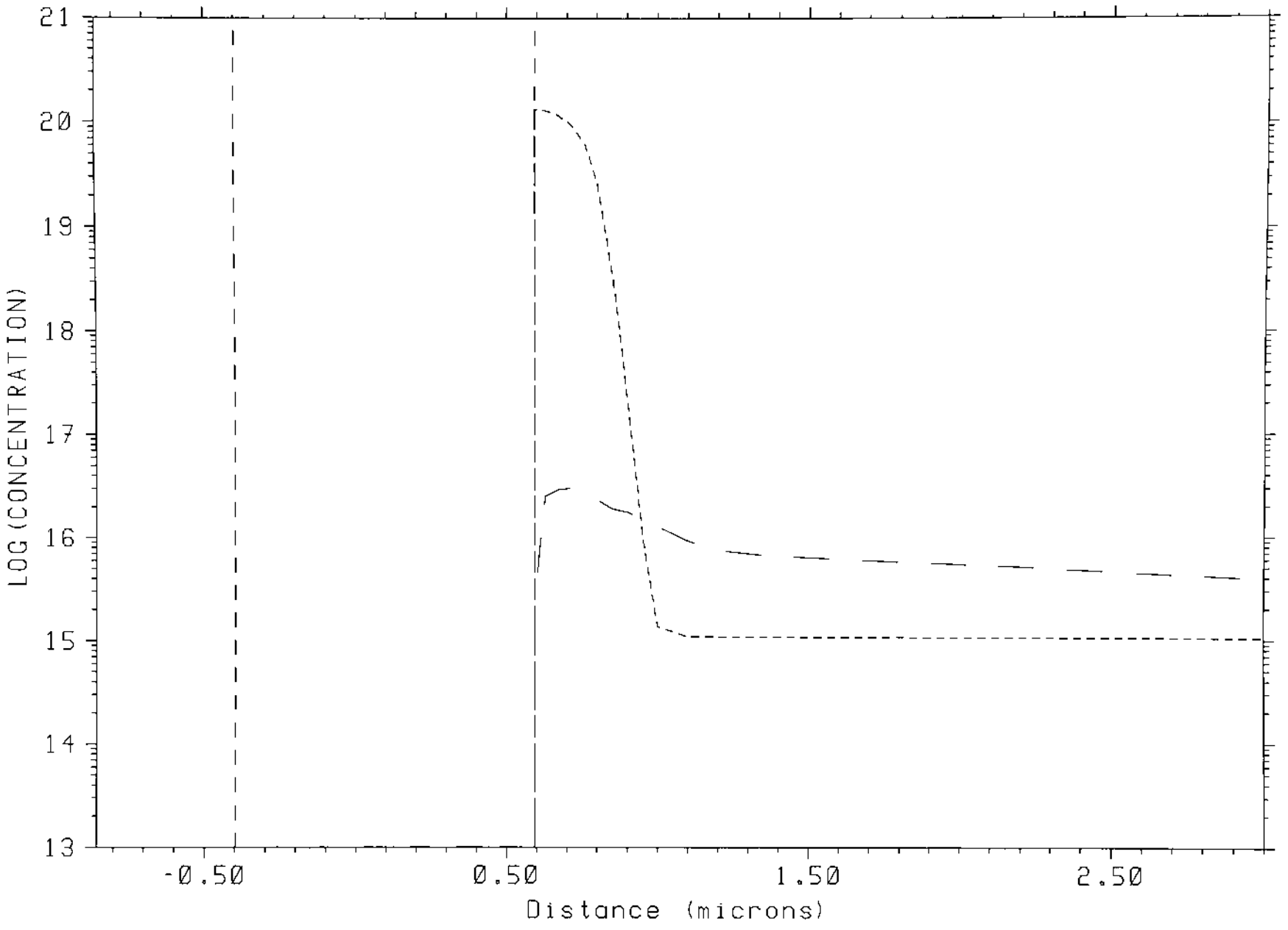


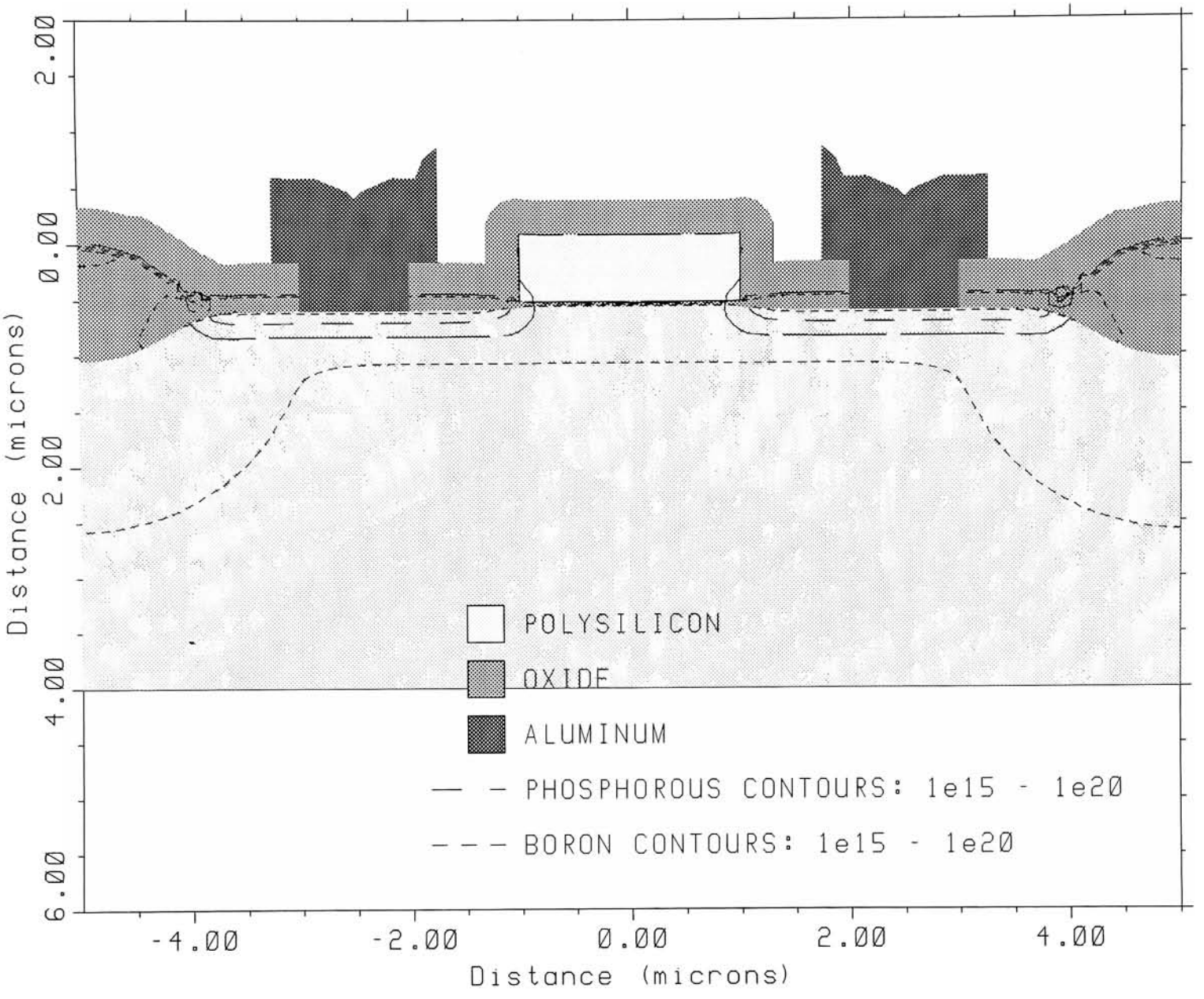
FINAL NMOS STRUCTURE



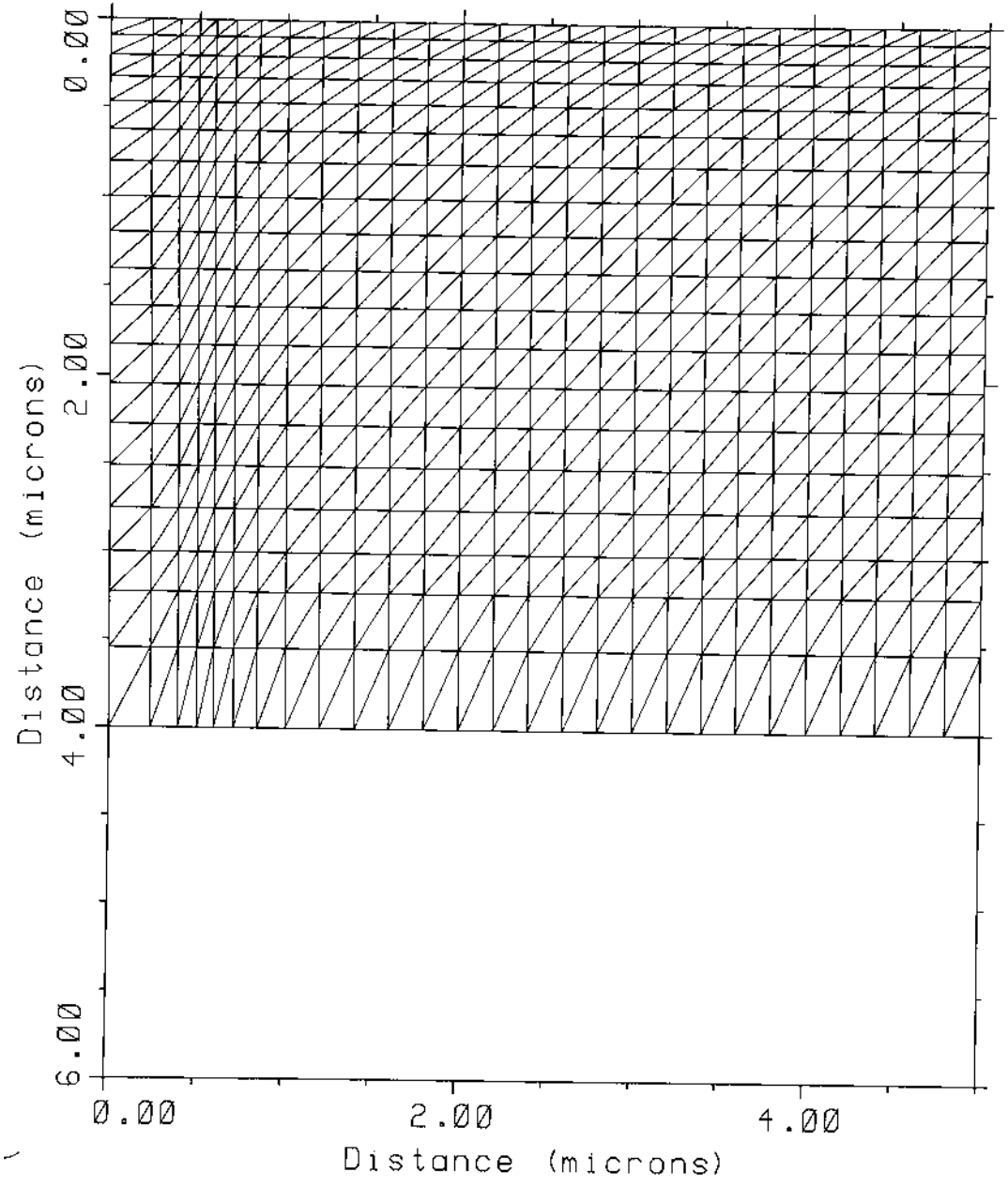

IMPLANT PROFILE 1e15
LOG (CONCENTRATION)
21
20
19
18
17
16
15
14
13
-0.50
0.50
1.50
2.50
Distance (microns)


FINAL STRUCTURE
2.00
0.00
2.00
4.00
6.00
Distance (microns)
POLYSILICON
OXIDE
ALUMINUM
PHOSPHOROUS CONTOURS: 1e15 - 1e20
BORON CONTOURS: 1e15 - 1e20
-4.00
-2.00
0.00
2.00
4.00
Distance (microns)

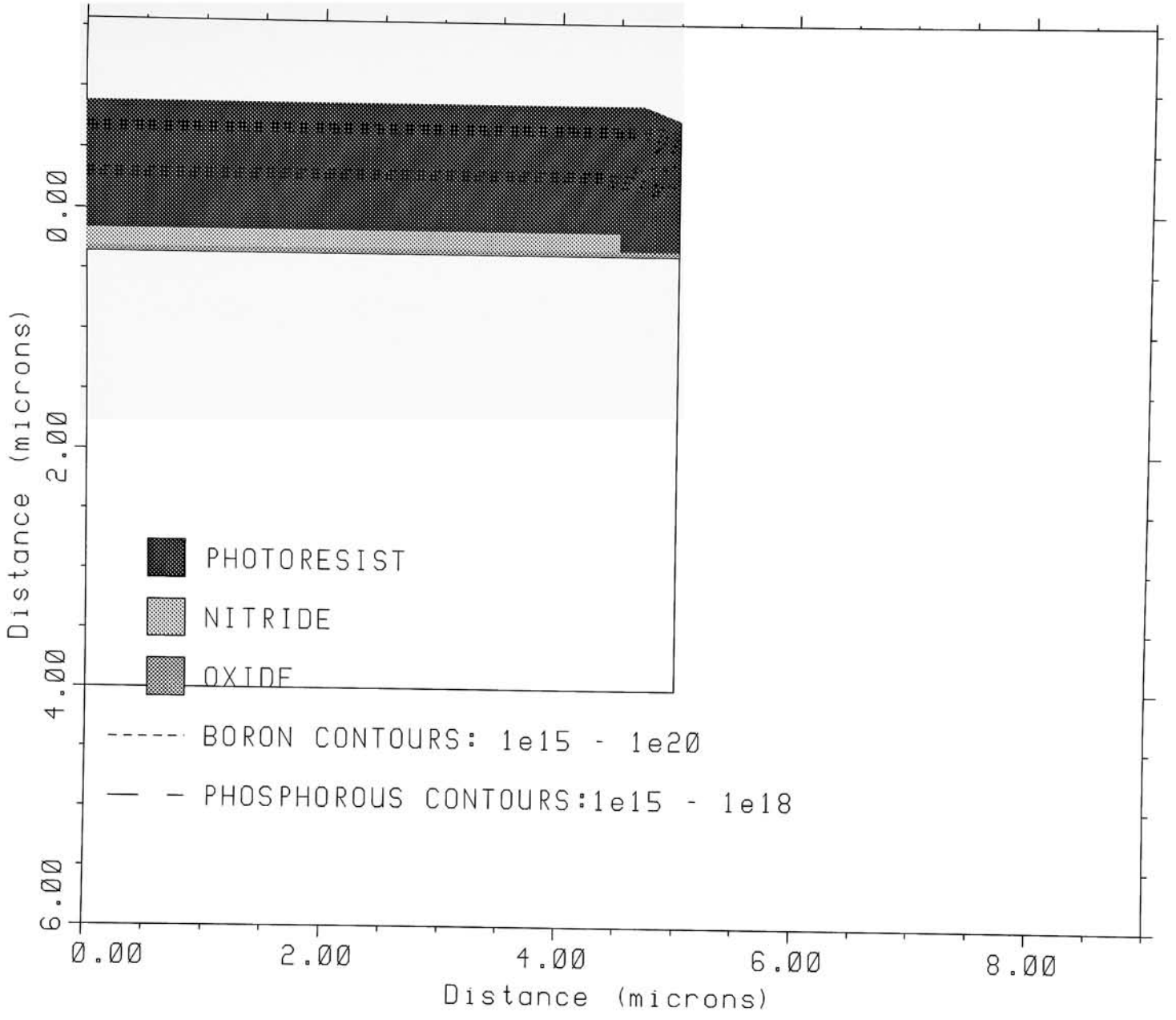

IMPLANT PROFILE 2e15
LOG(CONCENTRATION)
21
20
19
18
17
16
15
14
13
-0.50
0.50
1.50
2.50
Distance (microns)


FINAL STRUCTURE
2.00
0.00
2.00
4.00
6.00
Distance (microns)
POLYSILICON
OXIDE
ALUMINUM
PHOSPHOROUS CONTOURS: 1e15 - 1e20
BORON CONTOURS: 1e15 - 1e20
-4.00
-2.00
0.00
2.00
4.00
Distance (microns)

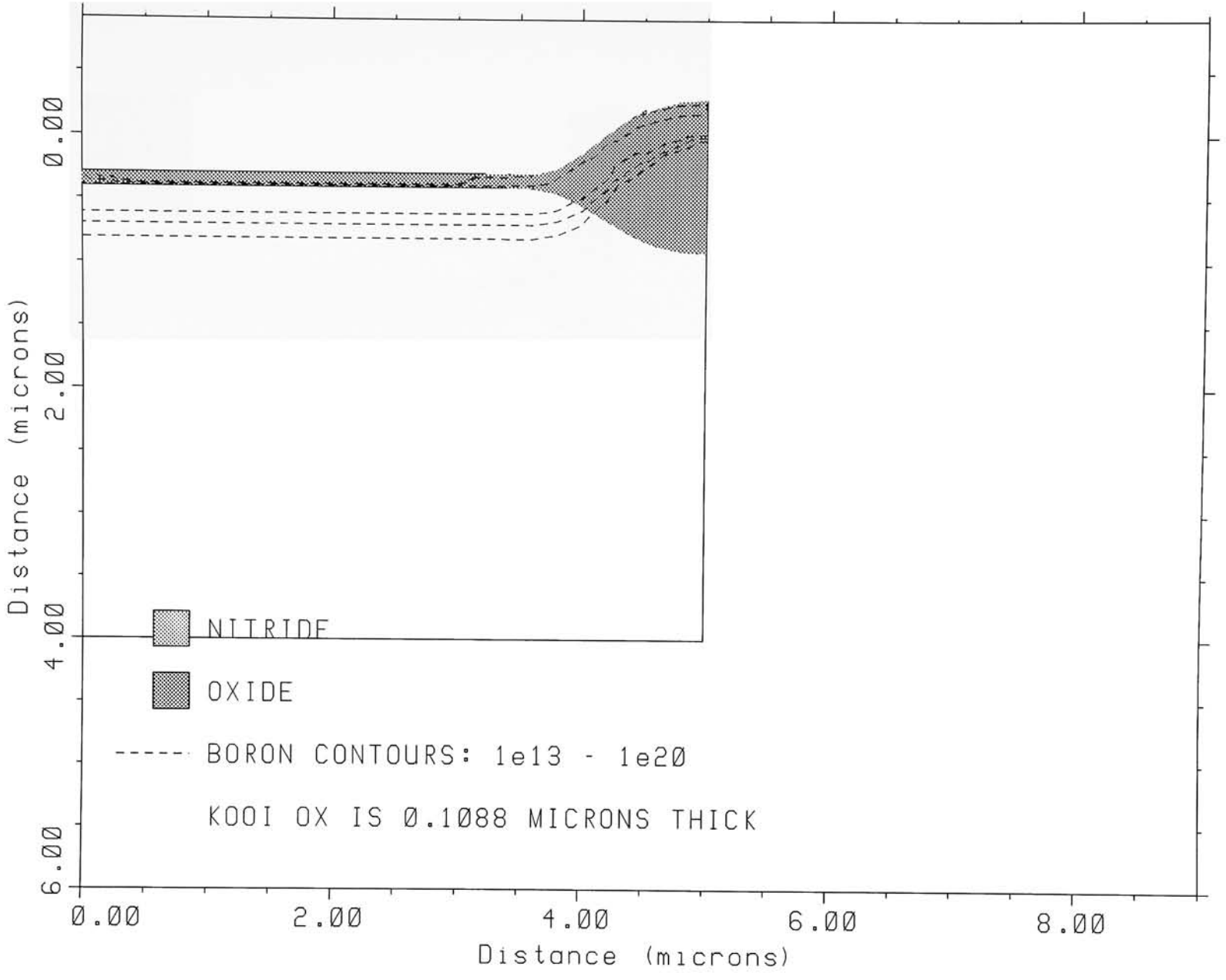
P-WELL CMOS: INITIAL GRID FOR PMOS DEVICE



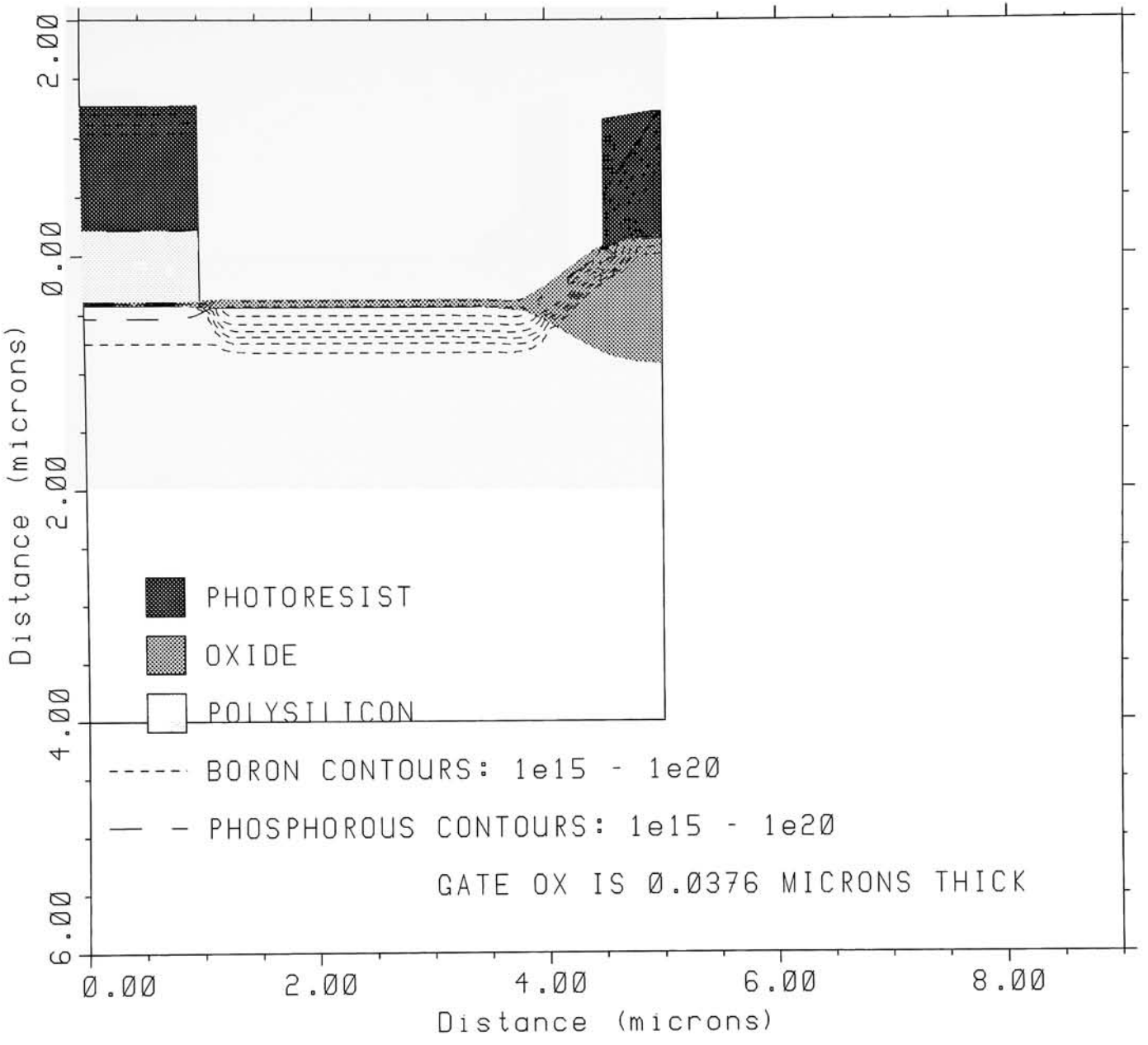
PMOS AFTER CHANNEL STOP IMPLANT

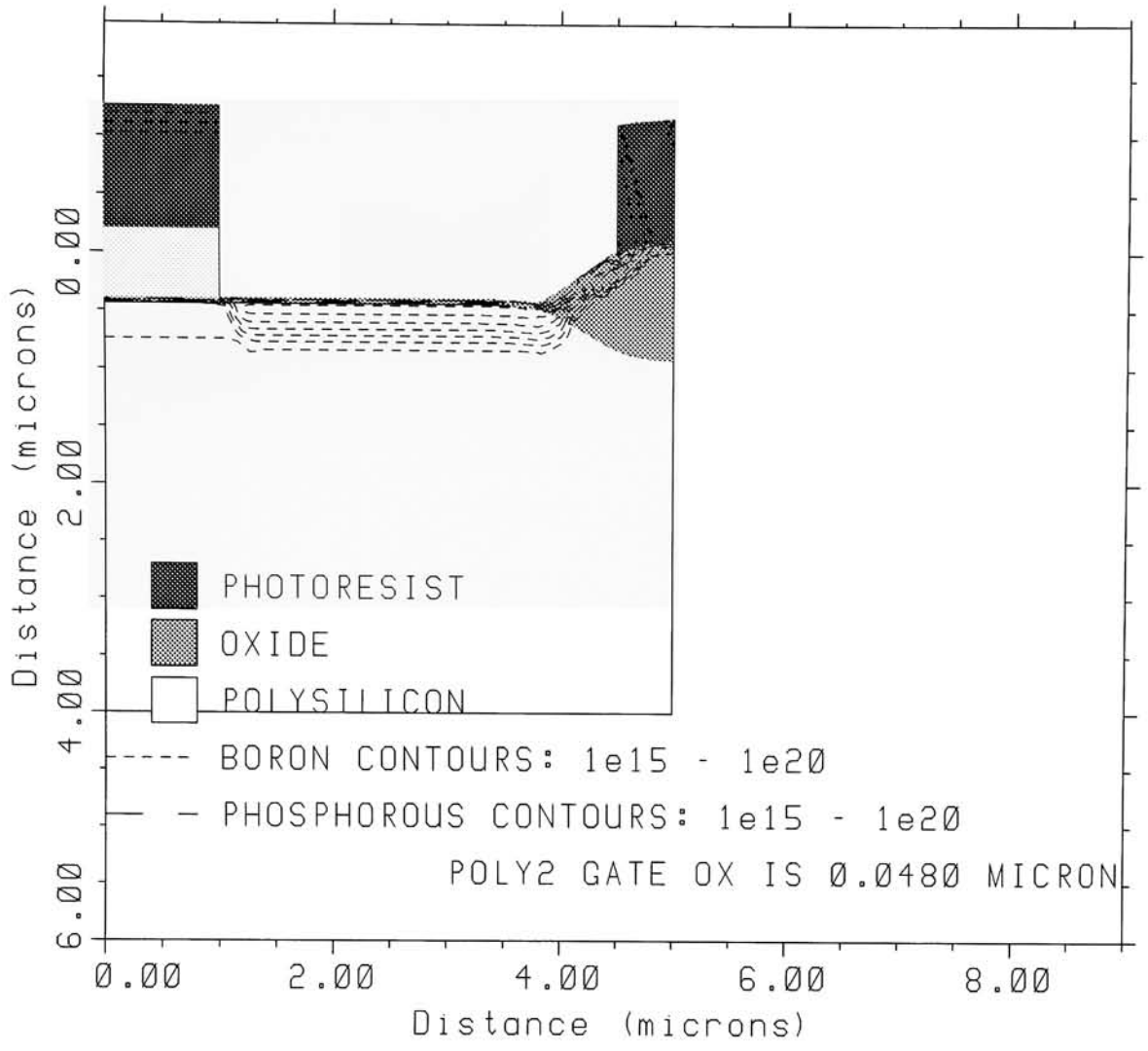


AFTER PMOS VT IMPLANT

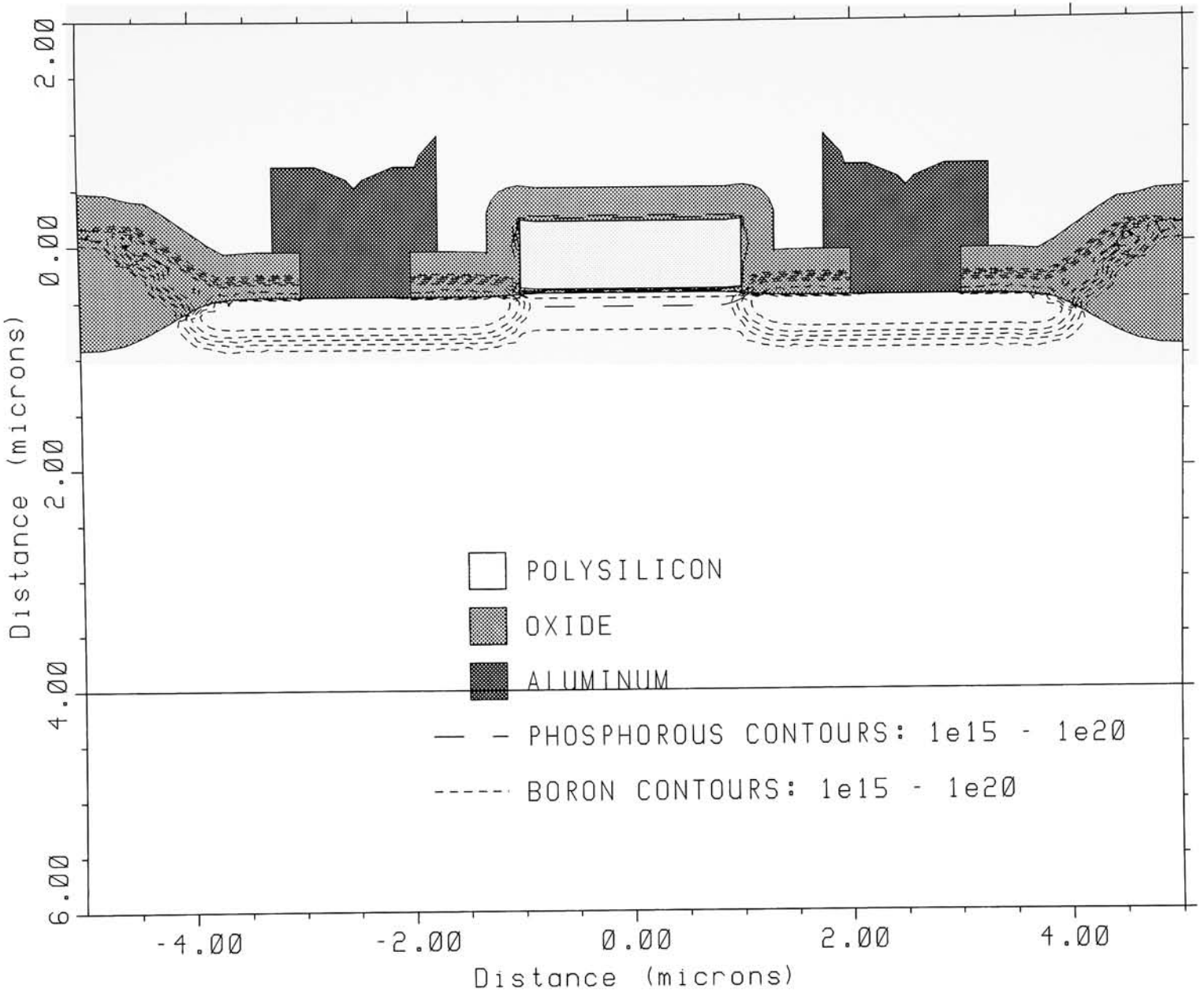


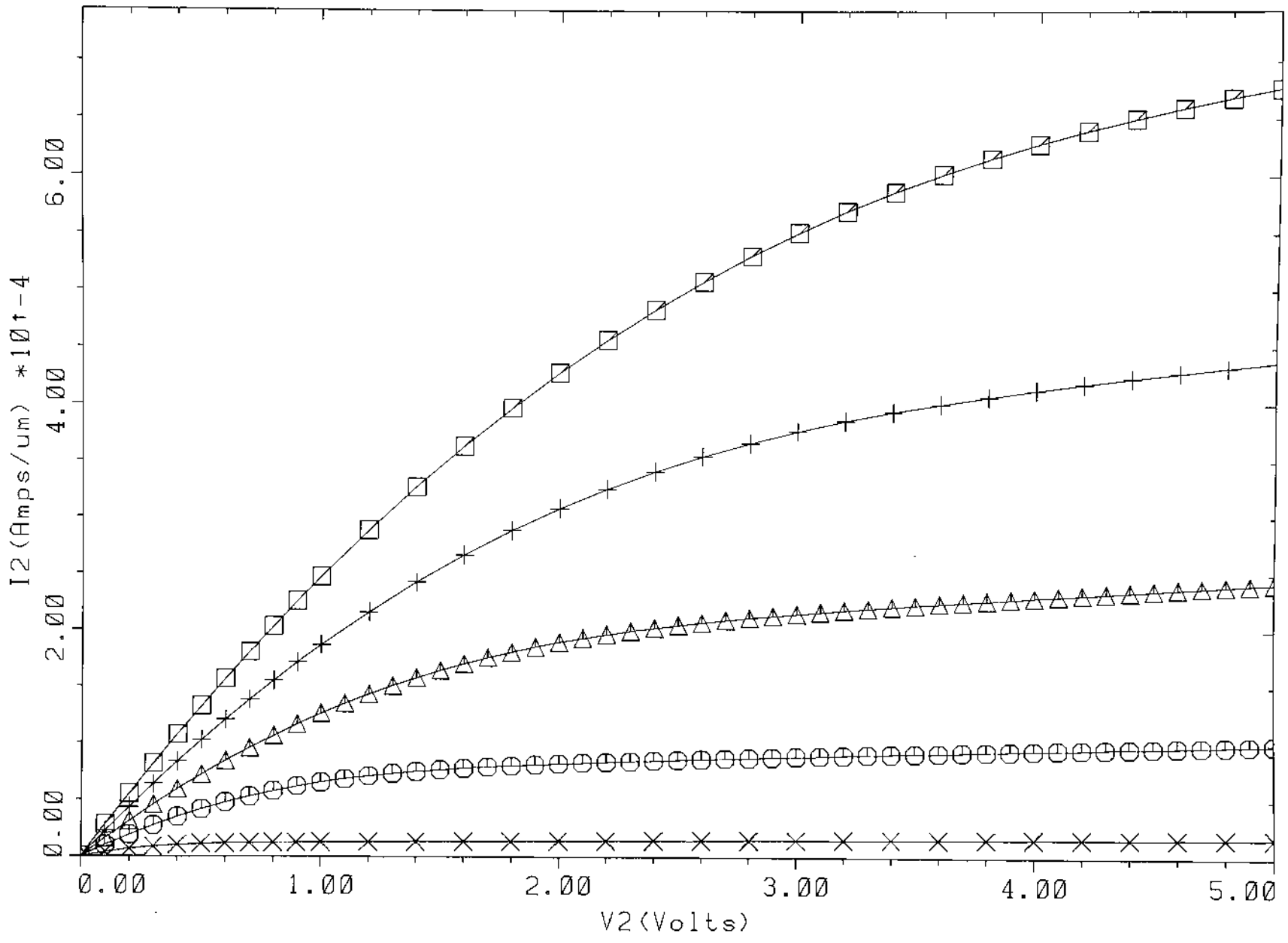
AFTER P+SOURCE/DRAIN IMPLANT

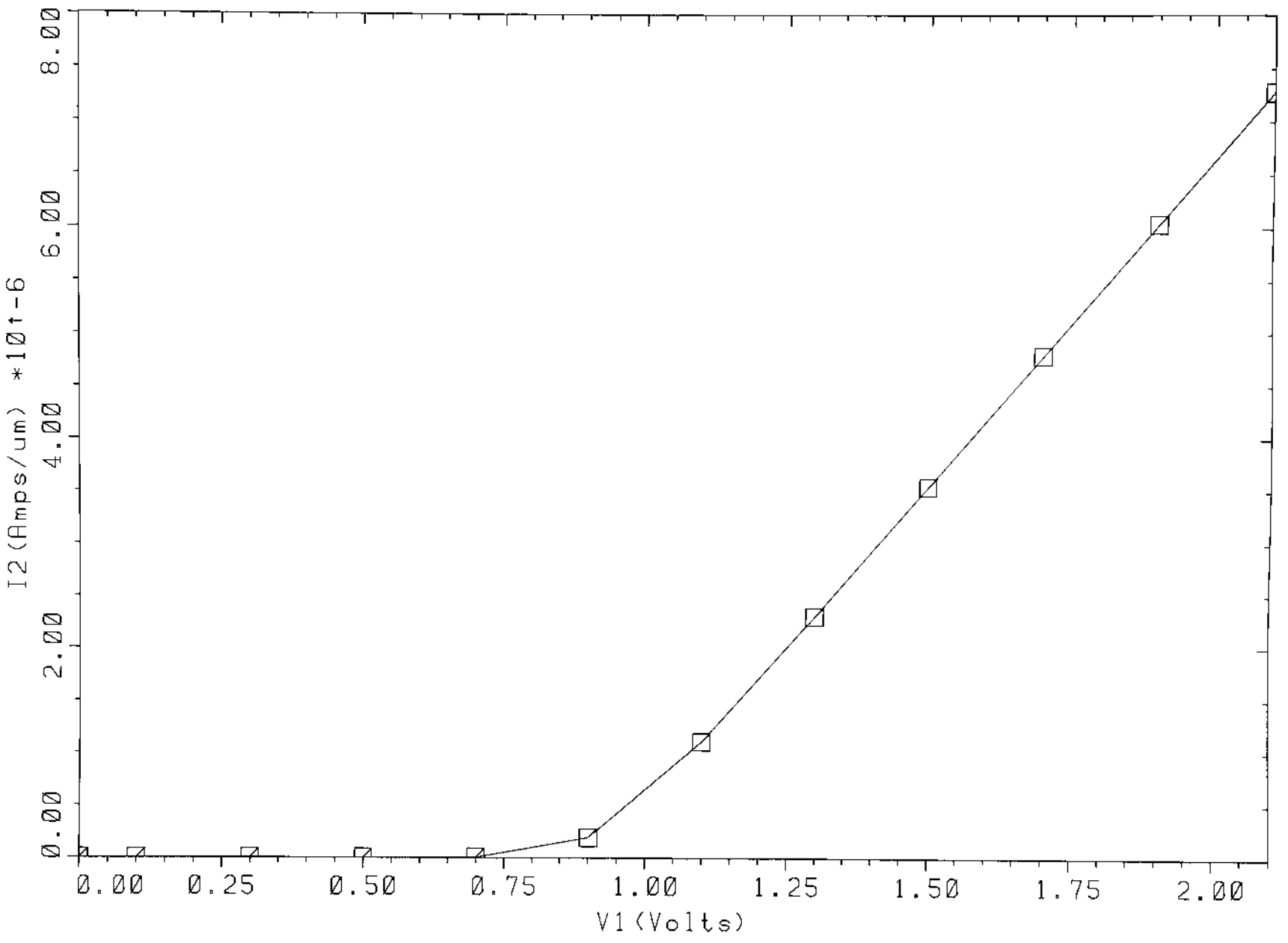


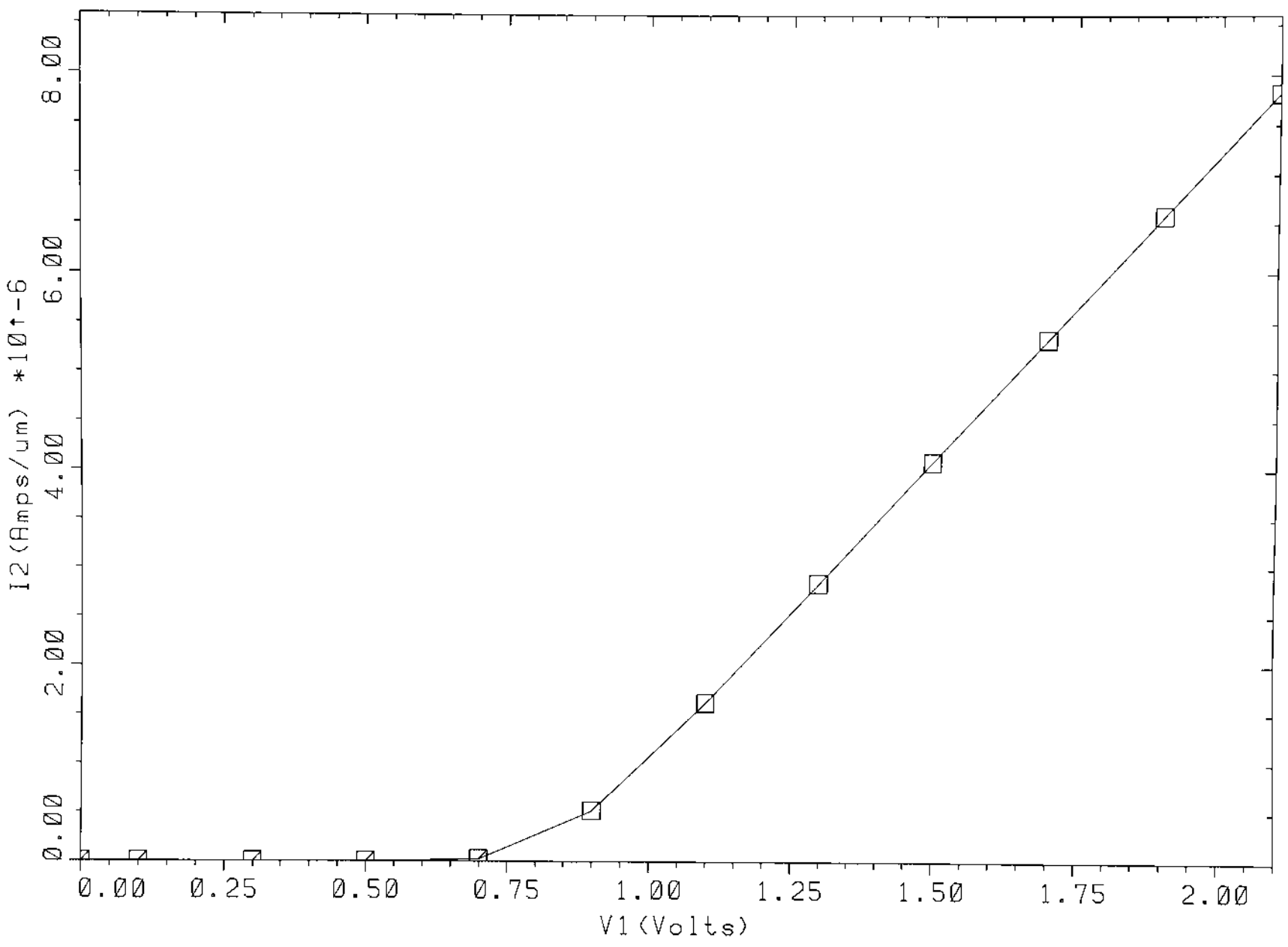

AFTER P+SOURCE/DRAIN IMPLANT
Distance (microns)
0.00
2.00
4.00
6.00
PHOTORESIST
OXIDE
POLYSILICON
BORON CONTOURS: 1e15 - 1e20
PHOSPHOROUS CONTOURS: 1e15 - 1e20
POLY2 GATE OX IS 0.0480 MICRON
0.00
2.00
4.00
6.00
8.00
Distance (microns)

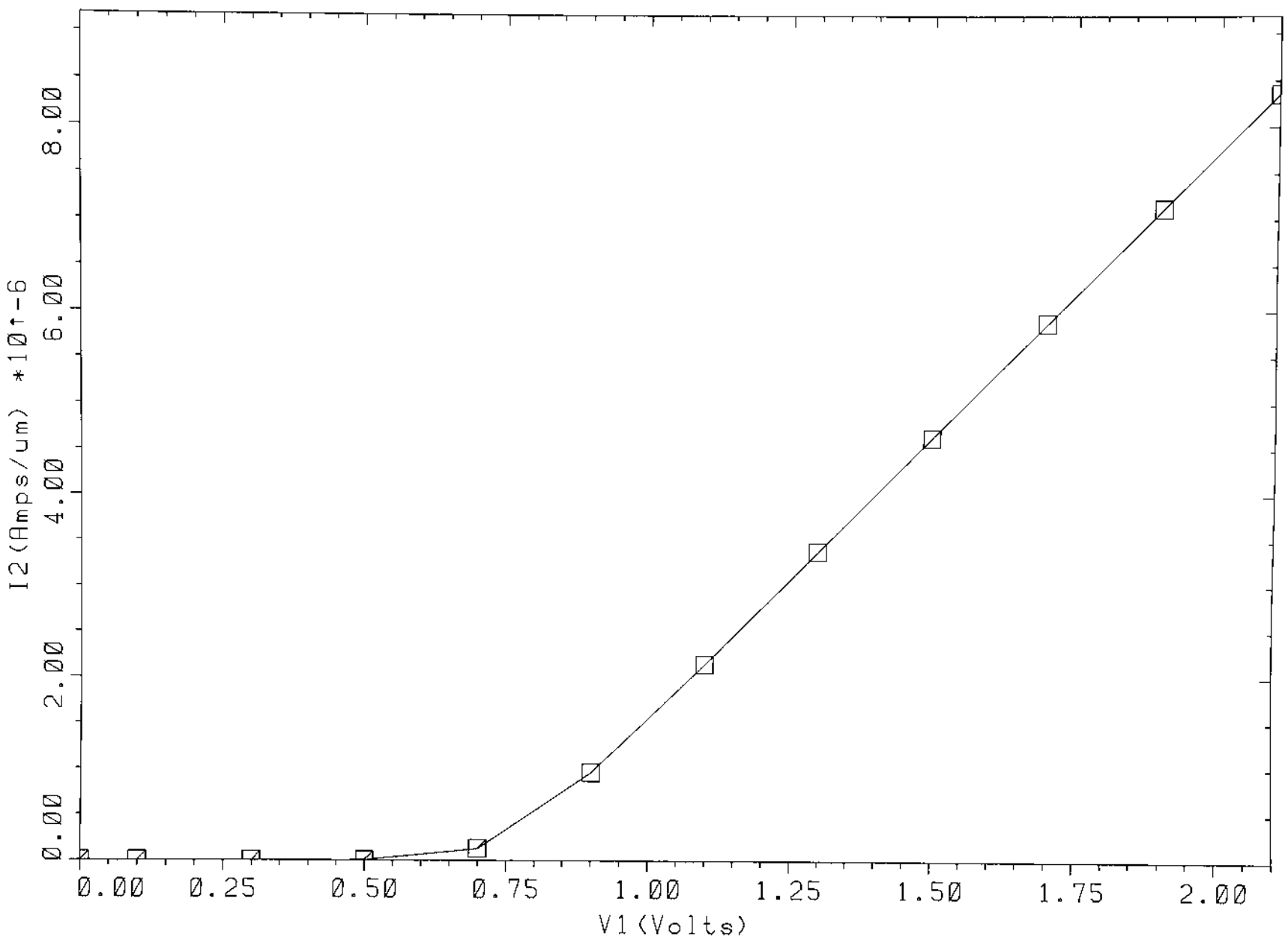
FINAL STRUCTURE

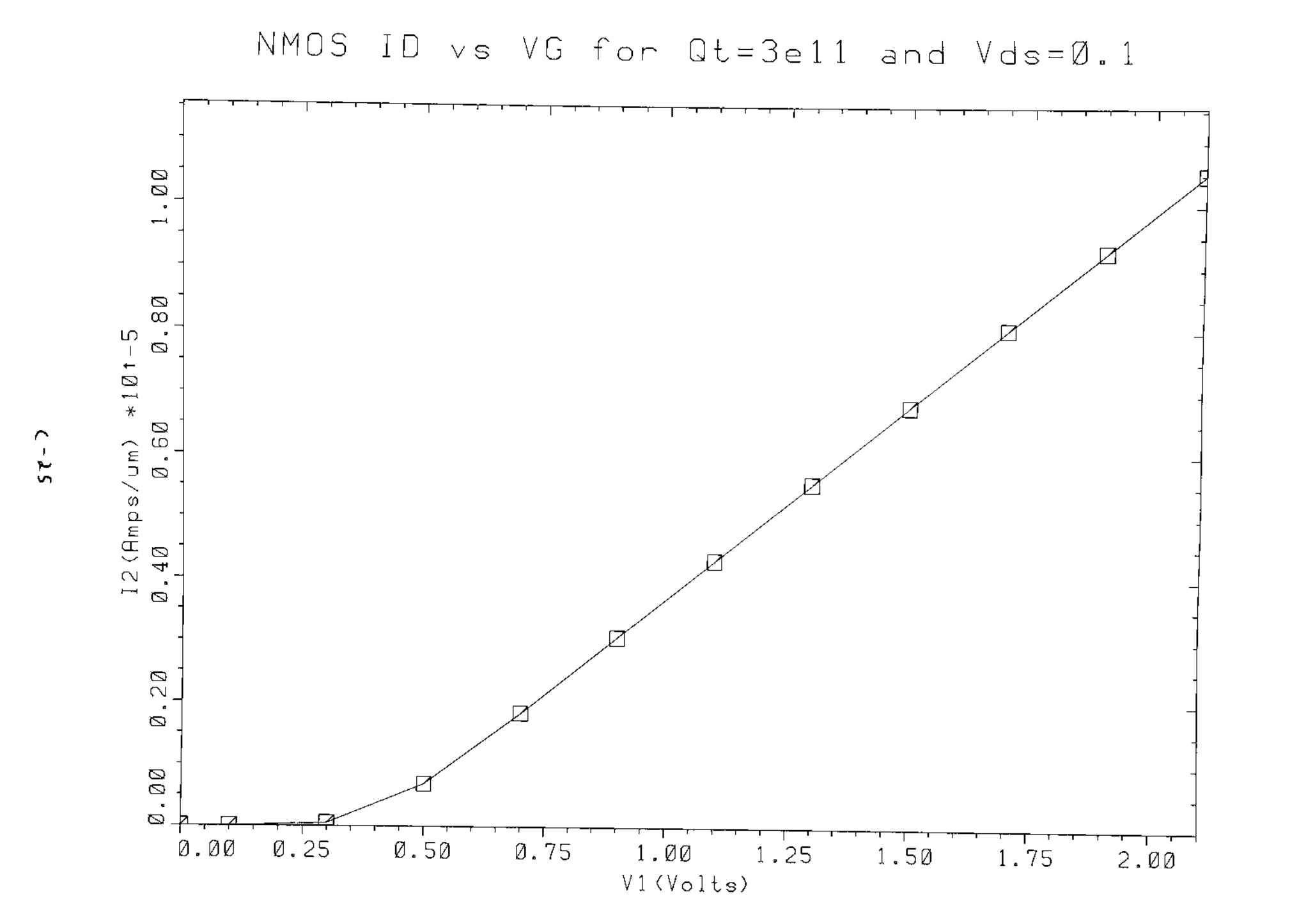


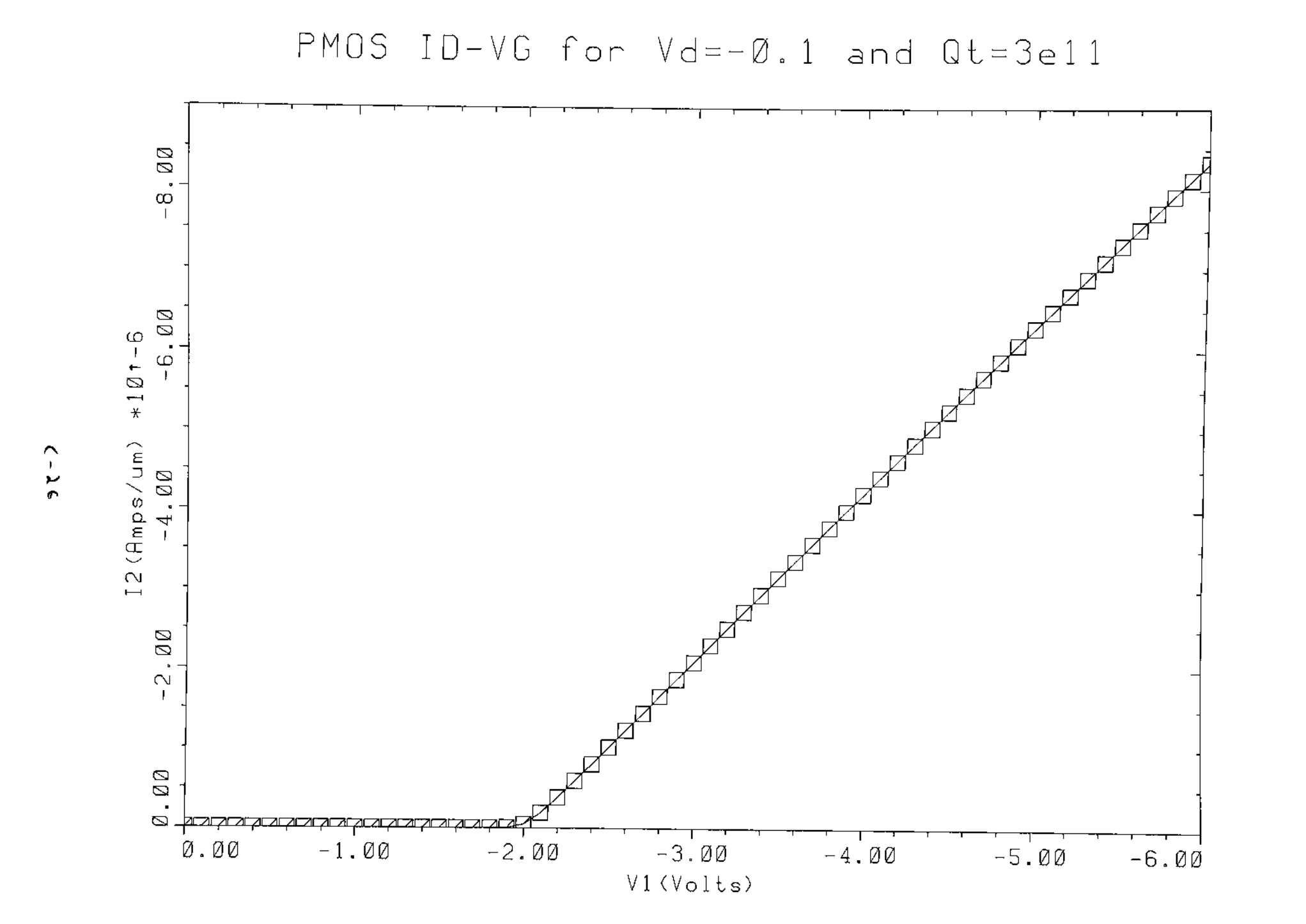

NMOS ID vs VD for Vg=1-5V & Vds=1 to 5V
I2(Amps/um) *10t-4
0.00
2.00
4.00
6.00
0.00
1.00
2.00
3.00
4.00
5.00
V2(Volts)


Gate Characteristics for Vds=0.1
I2(Amps/um) *10t-6
0.00
2.00
4.00
6.00
8.00
0.00
0.25
0.50
0.75
1.00
1.25
1.50
1.75
2.00
V1(Volts)


NMOS ID vs VG for Qt=5e10 and Vds=0.1
I2(Amps/um) *10↑-6
0.00
2.00
4.00
6.00
8.00
0.00
0.25
0.50
0.75
1.00
1.25
1.50
1.75
2.00
V1(Volts)


NMOS ID vs VG for Qt=1e11 and Vds=0.1
I2(Amps/um) *10↑-6
0.00
2.00
4.00
6.00
8.00
0.00
0.25
0.50
0.75
1.00
1.25
1.50
1.75
2.00
V1(Volts)


NMOS ID vs VG for Qt=3e11 and Vds=0.1
I2(Amps/um) *10t-5
0.00
0.20
0.40
0.60
0.80
1.00
0.00
0.25
0.50
0.75
1.00
1.25
1.50
1.75
2.00
V1(Volts)


PMOS ID-VG for Vd=-0.1 and Qt=3e11
I2(Amps/um) *10↑-6
0.00
-2.00
-4.00
-6.00
-8.00
0.00
-1.00
-2.00
-3.00
-4.00
-5.00
-6.00
V1(Volts)

```
$ Pwell CMOS process
$
$
$
$
$ Mask data file "nmos.tl1"
$
$
MASK       IN.FILE=nmos.tl1 PRINT
$
$ Set Display to X-Windows
OPTION DEVICE=X
$
$ Set up grid and initialize structure
$
$
LINE       X LOCATION=0 SPACING=0.5
LINE       X LOCATION=0.5 SPACING=0.1
LINE       X LOCATION=1.5 SPACING=.2
LINE       X LOCATION=5 SPACING=0.2
$
$ SET INITIAL Y GRID SPACING
$
LINE       Y LOCATION=0 SPACING=0.1
LINE       Y LOCATION=1 SPACING=0.2
LINE       Y LOCATION=3 SPACING=0.25
LINE       Y LOCATION=4 SPACING=1.0
$
$
#DEFINE gi 1.1
MESH       GRID.FAC=$gi
$
$ Start of Processing
$ Substrate wafer N-type,<100>, 5-15 Ohm-cm (10 Ohm-cm used
$
INITIALIZE RATIO=1.5 <100> ROT.SUB=0.0 PHOSPHOR=1e15
$
$
SELECT     TITLE="      PWELL CMOS: INITIAL GRID FOR NMOS DEVICES"
PLOT.2D    X.MIN=0 X.MAX=5 Y.MIN=-1 Y.MAX=4 SCALE "CLEAR X.SIZE=6, 25 -
 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 C.SIZE=0.4 L.BOUND=1 C.BOUND=1
 GRID L.GRID=1 C.GRID=1
$
$
$ STEP 1   TOOL SCRIBE
$
$ STEP 2   GRID OFF PROBE
$
$ STEP 3   CL01 RCA CLEAN
$
$ STEP 4   OX04 WET OXIDE
$
$       (START SOAK AT 1050 C)
$
DIFFUSION TIME=4 TEMPERAT=950 INERT
DIFFUSION TIME=5.5 TEMPERAT=950 T.FINAL=1050 INERT
DIFFUSION TIME=.5 TEMPERAT=1050 T.FINAL=1100 WET02
DIFFUSION TIME=46.5 TEMPERAT=1100 WET02
DIFFUSION TIME=10 TEMPERAT=1100 T.FINAL=1000 INERT
DIFFUSION TIME=4 TEMPERAT=1000 INERT
```

```
$
$
$ STEP 5   PW01 PHOTOLITH (WELL IMPLANT LEVEL 1)
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.05 SPACES=2
EXPOSE MASK=PWELL
DEVELOP
$
$ STEP 6   ET06 OXIDE ETCH
$
ETCH OXIDE TRAPEZOI
$
$ STEP 7   IM01 IMPLANT  PWELL
$
IMPLANT BORON DOSE=4e12 ENERGY=50 PEARSON RP.EFF
$
SAVEFILE  OUT.FILE=pwellimp SCALE=1.0
$
$ STEP 8   ET07 STRIP
$
ETCH PHOTORES ALL
$
$ STEP 9   CL01 RCA CLEAN
$
$ STEP 10  OX06 DRY OXIDE  (WELL DRIVE
$
$       (START SOAK AT 1125 C
$
DIFFUSION TIME=4 TEMPERAT=900 INERT
DIFFUSION TIME=10.75 TEMPERAT=900 T.FINAL=1125 INERT
DIFFUSION TIME=.5 TEMPERAT=1125 T.FINAL=1125 DRY02
DIFFUSION TIME=509.5 TEMPERAT=1125 DRY02
DIFFUSION TIME=900 TEMPERAT=1125 INERT
DIFFUSION TIME=17 TEMPERAT=1100 T.FINAL=1000 INERT
DIFFUSION TIME=4 TEMPERAT=1000 INERT
EXTRACT X=1.5  OXIDE  AREA.EXT  NAME=welldx
$
SAVEFILE  OUT.FILE=nmoswelldx SCALE=1.0
$
$ STEP 11  ET08 OXIDE ETCH (POST WELL DRIVE
$
ETCH  OXIDE  ALL
$
$
$ STEP 12 OX05 DRY OXIDE  PAD OXIDE
$
$       (START SOAK AT 1125
$
DIFFUSION TIME=4 TEMPERAT=900 INERT
DIFFUSION TIME=9.5 TEMPERAT=900 T.FINAL=1050 DRY02
DIFFUSION TIME=.5 TEMPERAT=1050 T.FINAL=1100 DRY02
DIFFUSION TIME=6 TEMPERAT=1100 DRY02
DIFFUSION TIME=10 TEMPERAT=1100 T.FINAL=1000 INERT
DIFFUSION TIME=4 TEMPERAT=1000 INERT
EXTRACT  X=2.0  OXIDE  AREA.EXT  NAME=padox
$
$
$ STEP 13 CV01 CVD NITRIDE
$
DEPOSITION NITRIDE THICKNES=.15 SPACES=2
```

```
DIFFUSION TIME=60 TEMPERAT=810 INERT
$
$
$ STEP 14  PH03 PHOTOLITH  (ACTIVE)
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.05 SPACES=2
EXPOSE     MASK=ACTIVE
DEVELOP
$
$
$ STEP 15  ET09 NITRIDE  (PRE-FIELD)
$
ETCH  NITRIDE  TRAPEZOI
$
$
$ STEP 16  ET07 STRIP
$
ETCH    PHOTORES  ALL
$
$
$ STEP 17  PH03 PHOTOLITH  (FIELD THRESHOLD VT)
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.05 SPACES=4
EXPOSE     MASK=CHANSTP
DEVELOP
$
$
$ STEP 18  IM11 IMPLANT  (P IMPLANT
$
IMPLANT    BORON DOSE=6e13 ENERGY=100 PEARSON RP.EFF
$
SELECT     Z=log10(BORON) TITLE="NMOS AFTER CHANNEL STOP IMPLANT"
PLOT.2D    X.MIN=0 X.MAX=5 Y.MAX=4 SCALE X.SIZE=4.25 Y.SIZE=0.25 X.OFFSET=1.0 -
 Y.OFFSET=2.0  T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR      COLOR=6 PHOTORES
COLOR      COLOR=3 NITRIDE
COLOR      COLOR=5 OXIDE
FOREACH    X(15 TO 20 STEP 1
CONTOUR    VALUE=15 LINE.TYP=2 COLOR=1
CONTOUR    VALUE=16 LINE.TYP=2 COLOR=1
CONTOUR    VALUE=17 LINE.TYP=2 COLOR=1
CONTOUR    VALUE=18 LINE.TYP=2 COLOR=1
CONTOUR    VALUE=19 LINE.TYP=2 COLOR=1
CONTOUR    VALUE=20 LINE.TYP=2 COLOR=1
END
LABEL      LABEL=PHOTORES1ST "CM X=1 Y=3 COLOR=1 LEFT SIZE=0.25 RECTANGL -
 C.RECTAN=6 W.RECTAN=.5 H.RECTAN=.5
LABEL      LABEL=NITRIDE "CM X=1 Y=3 $ COLOR=3 LEFT SIZE=0.25 RECTANGL -
 C.RECTAN=3 W.RECTAN=.5 H.RECTAN=.5
LABEL      LABEL=OXIDE "CM X=1 Y=4 COLOR=4 LEFT SIZE=0.25 RECTANGL C.RECTAN=5
 W.RECTAN=.5 H.RECTAN=.5
LABEL      LABEL="BORON CONTOURS: 1e15   1e16" "CM X=1 Y=4.5 COLOR=1 LEFT -
 SIZE=0.25 LINE.TYPE=2 C.LINE=7 LENGTH=1.0
LABEL      LABEL="PAD OXIDE THICKNESS IS @padox MICRONS" "CM X=1  Y=5 COLOR=1  LEFT
 SIZE=0.25
$
$
$ STEP 19  ET07  STRIP
$
ETCH    PHOTORES   ALL
```

```
$
$
$ STEP 20  ET06  OXIDE  ETCH
$
ETCH  OXIDE  TRAPEZOI
$
$
$ STEP 21  CL01 RCA CLEAN
$
$
$ STEP 22  OX04 WET OXIDE  (FIELD OXIDE
$
$       (START SOAK AT 1050 C)
$
$ METHOD        VISCOUS  GRID.OXI=4 INST=0.2
DIFFUSION TIME=4 TEMPERAT=900 DRY02
DIFFUSION TIME=9.5 TEMPERAT=900 T.FINAL=1050 DRY02
DIFFUSION TIME=.5 TEMPERAT=1050 T.FINAL=1100 WET02
DIFFUSION TIME=209 $ TEMPERAT=1100 WET02
DIFFUSION TIME=10 TEMPERAT=1100 T.FINAL=1000 INERT
DIFFUSION TIME=4 TEMPERAT=1000 INERT
EXTRACT  X=4.9  OXIDE  AREA.EXT  NAME=fieldox
$
SAVEFILE  OUT.FILE=nmosfox SCALE=1.0
$
$
$
$ STEP 23  ET05 NITRIDE (POST FIELD NITRIDE ETCH
$
ETCH    NITRIDE   ALL
$
$
$ STEP 24  ET06 OXIDE ETCH
$
ETCH    OXIDE  TRAPEZOI  THICKNES=1.06
$
$
$ STEP 25  CL01 RCA CLEAN
$
$
$ STEP 26  OX04 WET OXIDE   XXXX OXIDE
$
DIFFUSION TIME=4 TEMPERAT=900 INERT
DIFFUSION TIME=46 TEMPERAT=900 WET02
DIFFUSION TIME=4 TEMPERAT=900 INERT
EXTRACT  X=2.0  OXIDE  AREA.EXT  NAME=kdoiox
$
$ STEP 27  IM01 IMPLANT  (PMOS VT IMPLANT.
$
IMPLANT    BORON DOSE=1e11 ENERGY=60 PEARSON RP.EFF
$
$
$ STEP 28  PH03 PHOTOLITH  (NMOS VT IMPLANT
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.05 SPACES=2.0
EXPOSE     MASK=NMOSVT
DEVELOP
$
$
$ STEP 29  IM01 IMPLANT  (NMOS VT IMPLANT
```

```
$
IMPLANT   BORON  DOSE=1.2e12  ENERGY=60  PEARSON RP.EFF
$
$
SELECT    Z=log10(BORON, TITLE="AFTER NMOS VT IMPLANT"
PLOT.2D  X.MIN=0 X.MAX=5 Y.MAX=6 SCALE CLEAR T.SIZE=0.4 -
 L.BOUND=1 C.BOUND=1
COLOR     COLOR=6 PHOTORES
COLOR     COLOR=5 OXIDE
FOREACH   X(15 TO 20 STEP 1)
CONTOUR   VALUE=16 LINE.TYP=2 COLOR=1
CONTOUR   VALUE=17 LINE.TYP=2 COLOR=1
CONTOUR   VALUE=18 LINE.TYP=2 COLOR=1
CONTOUR   VALUE=19 LINE.TYP=2 COLOR=1
CONTOUR   VALUE=20 LINE.TYP=2 COLOR=1
END
LABEL     LABEL="PHOTORESIST "CM X=1 Y=3 COLOR=1 LEFT SIZE=0.25 RECTANGL C.RECTAN
 W.RECTAN=.5 H.RECTAN=.5
LABEL     LABEL="OXIDE "CM X=1 Y=3.5 COLOR=5 LEFT SIZE=0.25 RECTANGL C.RECTAN=5 -
 W.RECTAN=.5 H.RECTAN=.5
LABEL     LABEL="BORON CONTOURS: 1e16 - 1e20" "CM X=1 Y=4 COLOR=1 LEFT -
 SIZE=0.25 LINE.TYPE=2 C.LINE=1 LENGTH=1.0
LABEL     LABEL="XXOI OX IS @xoxiox MICRONS THICK" "CM X=1 Y=4.5 COLOR=1 LEFT
 SIZE=0.25
$
$ STEP 30   ET07 STRIP
$
ETCH     PHOTORES    ALL
$
$
$ STEP 31   ETCH OXIDE ETCH
$
ETCH       OXIDE    TRAPEZOI  THICKNES=0.125
$
$
$ STEP 32   CLN1 RCA CLEAN
$
$
$ STEP 33   OX16 DRY OXIDE  (GATE OXIDE
$
$       (START SOAK AT 1050 C)
$
DIFFUSION TIME=4 TEMPERAT=900 INERT
DIFFUSION TIME=3.5 TEMPERAT=900 T.FINAL=1050 DRYO2
DIFFUSION TIME=.5 TEMPERAT=1050 T.FINAL=1100 DRYO2
DIFFUSION TIME=8 TEMPERAT=1100 DRYO2
DIFFUSION TIME=10 TEMPERAT=1100 T.FINAL=1000 INERT
DIFFUSION TIME=4 TEMPERAT=1000 INERT
EXTRACT  X=2.0 OXIDE AREA.EXT NAME=gateox
$
$
$ STEP 34   CVD1 CVD POLY
$
DEPOSITION POLYSILI THICKNES=0.8 SPACES=2
$
DIFFUSION TIME=120 TEMPERAT=615 INERT
$
$
$ STEP 35   DIF4 N-TYPE DIFF  POLY DOPE
$
```

```
METHOD  INIT=0.2
DIFFUSION TIME=4 TEMPERAT=800 T.FINAL=900 INERT PHOSPHOR=7e21
DIFFUSION TIME=5 TEMPERAT=900 T.FINAL=1000 INERT PHOSPHOR=1e21
DIFFUSION TIME=15 TEMPERAT=1000 INERT PHOSPHOR=1e21
DIFFUSION TIME=4 TEMPERAT=1000 INERT PHOSPHOR=1e21
$
$
$ STEP 36   ET08 OXIDE ETCH
$
$ STEP 37   DE11 4PT PROBE
$
$ STEP 38   PH10 PHOTOLITH  (POLY
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.05 SPACES=2
EXPOSE    MASK=POLY1
DEVELOP
$
$
$ STEP 39   ET16  POLY ETCH
$
ETCH      POLYSILI TRAPEZOI THICKNES=0.65
$
SAVEFILE  OUT.FILE=nmospoly SCALE=1.0
$
$ STEP 40   ET17 STRIP
$
ETCH    PHOTORES   ALL
$
$
$ STEP 41 OXIDE DRY OXIDE DIFFUSION
$
DIFFUSION TIME=4 TEMPERAT=800 T.FINAL=850 INERT
DIFFUSION TIME=4.5 TEMPERAT=850 T.FINAL=900 DRYO2
DIFFUSION TIME=1.5 TEMPERAT=900 T.FINAL=1000 DRYO2
DIFFUSION TIME=60 TEMPERAT=1000 DRYO2
DIFFUSION TIME=10 TEMPERAT=1000 INERT
DIFFUSION TIME=4 TEMPERAT=1000 INERT
$
$
$ STEP 42   CVD1 CVD POLY2
$
$ DEPOSITION POLYSILI THICKNES=0.6 SPACES=2
$
DIFFUSION TIME=120 TEMPERAT=615  INERT
$
$
$ STEP 43   DIF4 N-TYPE DIFFUSION
$
DIFFUSION TIME=4 TEMPERAT=800 INERT
DIFFUSION TIME=5 TEMPERAT=800 T.FINAL=1000 INERT
DIFFUSION TIME=15 TEMPERAT=1000 INERT
DIFFUSION TIME=4 TEMPERAT=1000 INERT
$
$
$ STEP 44   OX06  OXIDE ETCH
$
$ STEP 45   DE11  4PT PROBE
$
$ STEP 46   PH10  PHOTOLITH  (POLY2
$
```

```
DEPOSITION PHOTORES POSITIVE THICKNES=1.05 SPACES=10
EXPOSE    MASK=POLY2
DEVELOP
$
$
$ STEP 47   ET06  POLY2 ETCH
$
$  ETCH   POLYSILI  TRAPEZOI  THICKNES=1
$
$
$ STEP 48   ET07  ETCH PHOTORESIST
$
ETCH   PHOTORES   ALL
$
SAVEFILE  OUT.FILE=nmosimp
$
$
$ STEP 49   PH12 PHTOLITH (P+ DRAIN/SIURCE
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.05
EXPOSE    MASK=P+S/D
DEVELOP
$
$
$ STEP 50   ET06  OXIDE ETCH
$
$ ETCH   OXIDE   TRAPEZOI  THICKNES=0.1
$
$
$ STEP 51   IM11 IMPLANT  (P- DRAIN/SIURCE
$
IMPLANT   BF2 DOSE=1e15 ENERGY=150 PEARSON RP.EFF TILT=7
$
$ STEP  52   ET07  STRIP RESIST
$
ETCH   PHOTORES   ALL
$
$  STEP  53 PH11  PROTOLITH  (N+ SOURCE/DRAIN
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.05 SPACES=2
EXPOSE   MASK=N+S/D
DEVELOP
$
$  STEP  54   IM11 IMPLANT  (N+ DRAIN/SOURCE
IMPLANT   PHOSPHOROUS  DOSE=1e15  ENERGY=60  PEARSON RP.EFF
$
$
SELECT   Z=log10 BORON  TITLE=" AFTER N+ SOURCE/DRAIN IMPLANT"
PLOT.2D  X.MIN=0 X.MAX=10 Y.MAX=6 SCALE CLEAR T.SIZE=0.4 L.BOUND=1
 C.BOUND=1
COLOR     COLOR=5  OXIDE
COLOR     COLOR=7  POLYSILICON
COLOR     COLOR=6  PHOTORESIST
FOREACH   X(15)
CONTOUR   VALUE=15 LINE.TYP=8 COLOR=7
END
FOREACH   X(16 TO 20 STEP 1)
CONTOUR   VALUE=X LINE.TYP=5 COLOR=7
END
SELECT    Z=log10(PHOSPHOR
```

```
FOREACH  X(15)
CONTOUR  VALUE=15 LINE.TYP=8 COLOR=1
END
FOREACH  X(16 TO 20 STEP 1)
CONTOUR  VALUE=X LINE.TYP=5 COLOR=1
END
LABEL    LABEL="PHOTORESIST "CM X=1 Y=3 COLOR=1 LEFT SIZE=0.25 RECTANGL -
 C.RECTAN=6 W.RECTAN=0.5 H.RECTAN=0.5
LABEL    LABEL="OXIDE "CM X=1 Y=3.5 COLOR=1 LEFT SIZE=0.25 RECTANGL -
 C.RECTAN=5 W.RECTAN=0.5 H.RECTAN=0.5
LABEL    LABEL="POLYSILICON "CM X=1 Y=4 COLOR=1 LEFT SIZE=0.25 RECTANGL -
 C.RECTAN=2 W.RECTAN=0.5 H.RECTAN=0.5
LABEL    LABEL="BORON CONTOURS: 1e15 - 1e20" "CM X=1 Y=4.5 COLOR=1
 LEFT SIZE=0.25 LINE.TYP=1 C.LINE=7 LENGTH=1.0
LABEL    LABEL="PHOSPHOROUS CONTURS: 1e15 - 1e20" "CM X=1 Y=5 COLOR=1 -
 LEFT SIZE=0.25 LINE TYP=5 C.LINE=1 LENGTH=1.0
LABEL    LABEL="GATE OXIDE THICKNESS= @gateox MICRONS" "CM X=1  Y=5 5 COLOR=1 -
 LEFT SIZE=0.25
$
SAVEFILE  OUT FILE=nmos50 SCALE=1.0
$
$ STEP 55   ET07 STRIP
$
ETCH    PHOTORES   ALL
$
$
$ STEP 56   CLN1 RCA CLEAN
$
$ STEP 57   CVD8  CVD LTO
$
DEPOSITION OXIDE THICKNES=0.3 SPACES=3
$
$ STEP 58   OX06  ANNEAL
$
DIFFUSION  TIME=15 TEMPERAT=550 INERT
DIFFUSION  TIME=15 TEMPERAT=550 T.FINAL=850 WET02
DIFFUSION  TIME=5 TEMPERAT=850 INERT
$
SAVEFILE  OUT FILE=nmosanneal SCALE=1.0
$
$
$ STEP 59   PH13  PHOTOLITH  (CONTACT CUTS
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.05 SPACES=2
EXPOSE    MASK=CONTCUT
DEVELOP
$
$
$ STEP 60   ET04  OXIDE ETCH
$
ETCH    OXIDE   TRAPEZOI
$
$
$ STEP 61   ET07  STRIP PHOTORESIST
$
ETCH    PHOTORES   ALL
$
$
$ STEP 62   CLN4 RCA CLEAN
$
```

```
$ STEP 63   MET1  AL DEPOSIT
$
DEPOSITION ALUMINUM THICKNES=0.5 SPACES=2
$
$
$ STEP 64  PH03  PHOTOLITH  (METAL)
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.05 SPACES=2
EXPOSE     MASK=METAL1
DEVELOP
$
$
$ STEP 65  ET05  ALUMINUM ETCH
$
ETCH     ALUMINUM  TRAPEZ01
$
$
$ STEP 66  ET07  STRIP PHOTORESIST
$
ETCH     PHOTORES   ALL
$
$
$ STEP 67  SI01  SINTER
$
DIFFUSION TIME=30 TEMPERATU=425 F.N2=3.55 F.H2=0.05
$
$
$ STEP 68   TE11  TEST
$
$
$
STRUCTURE REFLECT LEFT
SELECT     Z=log10(boron) TITLE="FINAL NMOS STRUCTURE"
PLOT.2D    Y.MIN=-1 Y.MAX=6 SCALE CLEAR T.SIZE=0.4 L.BOUND=1 +
 C.BOUND=2
COLOR      MIN.V=15 MAX.V=20 COLOR=7
COLOR      COLOR=2 POLYSILI
COLOR      COLOR=4 ALUMINUM
COLOR      COLOR=5 OXIDE
FOREACH    X(15)
CONTOUR    VALUE=15 LINE.TYP=3 COLOR=1
END
FOREACH    X(16 TO 20 STEP 1)
CONTOUR    VALUE=X LINE.TYP=5 COLOR=1
END
SELECT     Z=log10(PHOS)
FOREACH    X(15)
CONTOUR    VALUE=15 LINE.TYP=8 COLOR=1
END
FOREACH    X(16 TO 20 STEP 1)
CONTOUR    VALUE=X LINE.TYP=5 COLOR=1
END
LABEL      LABEL="POLYSILICON "CM X=-1 Y=3.5 COLOR=1 LEFT SIZE=0.25 RECTANGL +
 C.RECTAN=2 W.RECTAN=.5 H.RECTAN=.5
LABEL      LABEL="OXIDE "CM X=-1 Y=4 COLOR=1 LEFT SIZE=0.25 RECTANGL C.RECTAN=5
 W.RECTAN=.5 H.RECTAN=.5
LABEL      LABEL="ALUMINUM "CM X=-1 Y=4.5 COLOR=1 LEFT SIZE=0.25 RECTANGL +
 C.RECTAN=4 W.RECTAN=.5 H.RECTAN=.5
LABEL      LABEL="PHOSPHOROUS CONTOURS: 1e15 - 1e20" "CM X=-1 Y=5 COLOR=1 LEFT
 SIZE=0.25 LINE.TYP=5 C.LINE=1 LENGTH=1.0
```

```
LABEL      LABEL="BORON CONTOURS: 1e15 - 1e20" "CM X=-1 Y=5.5 COLOR=1 LEFT +
 SIZE=0.25 LINE.TYP=3 C.LINE=1 LENGTH=1.0
$
$
$
$
$
$
$ END OF PROCESSING
$
PLOT.2D    "AXES L.BOUND=1 C.BOUND=1 "CLEAR
SAVEFILE   OUT.FILE="TOS.GIF MET1C1 POLY.ELE ELEC.BOU
STOP
```

```
$ PWell CMOS process
$
$
$
$
$ Mask data file "locos.tif"
$
$
MASK      IN.FILE=locos.tif PRINT
$
$ Set Display to X-windows
OPTION DEVICE=X
$
$ Set up grid and initialize structure
$
$
LINE      X LOCATION=0 SPACING=0.5
LINE      X LOCATION=0.5 SPACING=0.1
LINE      X LOCATION=2 SPACING=0.1
$ LINE    X LOCATION=3 SPACING=0.2
$ LINE    X LOCATION=4 SPACING=2
$ LINE      X LOCATION=6 SPACING=2
$ LINE      X LOCATION=8 SPACING=0.2
$ LINE    X LOCATION=9 SPACING=0.1
$ LINE    X LOCATION=10 SPACING=0.2
$ LINE      X LOCATION=11 SPACING=1.0
$ LINE    X LOCATION=12 SPACING=1.0
$
$
$ Set initial Y Grid Spacing
$
LINE      Y LOCATION=0 SPACING=0.1
LINE      Y LOCATION=1 SPACING=0.2
LINE      Y LOCATION=3 SPACING=0.25
LINE      Y LOCATION=4 SPACING=1.0
$
$ Eliminate X columns in X grid
$
$
$ Eliminate initial y columns in y grid
$
$ ELIMINATE ROWS X.MIN=-1 X.MAX=12 Y.MIN=-0.5 Y.MAX=4
$ ELIMINATE ROWS X.MIN=-1 X.MAX=12 Y.MIN=4 Y.MAX=6
$ ELIMINATE ROWS X.MIN=-1 X.MAX=12 Y.MIN=6 Y.MAX=8
$
$
$DEFINE gs 1.0
MESH      GRID.FAC=gs
$
$ Start of Processing
$ Substrate wafer N-type,<100>, 5-15 Ohm-cm (10 Ohm-cm used
$
INITIALIZE RATIO=0.5 <100> ROT.SUB=0.0 PHOSPHOR=1e15
$
$
SELECT    TITLE="P-WELL CMOS (CCD ) INITIAL GRID FOR DEVICES"
PLOT.2D   X.MIN=-1 X.MAX=2 Y.MIN=-1 Y.MAX=6 SCALE "CLEAR X.SIZE=11.25 -
 Y.SIZE=0.25 X.OFFSET=1.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1 -
 GRID L.GRID=1 C.GRID=1
$
```

```
$
$ STEP 1   INIT SCRIBE
$
$ STEP 2   DEC1 4PT PROBE
$
$ STEP 3   CLO1 RCA CLEAN
$
$ STEP 4   OX04 WET OXIDE
$
$       (START SOAK AT 1090 C)
$
DIFFUSION TIME=4 TEMPERAT=900 INERT
DIFFUSION TIME=9.5 TEMPERAT=900 T.FINAL=1050 INERT
DIFFUSION TIME=.5 TEMPERAT=1050 T.FINAL=1100 WET02
DIFFUSION TIME=48.5 TEMPERAT=1100 WET02
DIFFUSION TIME=10 TEMPERAT=1100 T.FINAL=1000 INERT
DIFFUSION TIME=4 TEMPERAT=1000 INERT
$
$
$ STEP 5   PHO2 PHTOLITH (WELL IMPLANT LEVEL 1
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.05 SPACES=2
EXPOSE MASK=PWELL
DEVELOP
$
$ STEP 6   ET16 OXIDE ETCH
$
ETCH OXIDE TRAPEZOI
$
$ STEP 7   IM01 IMPLANT (PWELL
$
IMPLANT BORON DOSE=4e12 ENERGY=80 PEARSON RP.EFF
$
$ STEP 8   ET07 STRIP
$
ETCH PHOTORES ALL
$
$ STEP 9   CLO1 RCA CLEAN
$
$ STEP 10  OX06 DRY OXIDE  (WELL DRIVE
$
$       (START SOAK AT 1125 C)
$
DIFFUSION TIME=4 TEMPERAT=900 INERT
DIFFUSION TIME=30.75 TEMPERAT=900 T.FINAL=1125 INERT
DIFFUSION TIME=.5 TEMPERAT=1125 T.FINAL=1125 DRY02
DIFFUSION TIME=509.5 TEMPERAT=1125 DRY02
DIFFUSION TIME=720 TEMPERAT=1125 INERT
DIFFUSION TIME=10 TEMPERAT=1100 T.FINAL=1000 INERT
DIFFUSION TIME=4 TEMPERAT=1000 INERT
$
$
$ STEP 11  ET08 OXIDE ETCH (POST WELL DRIVE
$
ETCH  OXIDE  ALL
$
$
$ STEP 12 OX05 DRY OXIDE (PAD OXIDE
$
$       (START SOAK AT 1050
```

```
$
DIFFUSION TIME=4 TEMPERAT=900 INERT
DIFFUSION TIME=9.5 TEMPERAT=900 T.FINAL=1050 DRY02
DIFFUSION TIME=.5 TEMPERAT=1050 T.FINAL=1100 DRY02
DIFFUSION TIME=8 TEMPERAT=1100 DRY02
DIFFUSION TIME=10 TEMPERAT=1100 T.FINAL=1000 INERT
DIFFUSION TIME=4 TEMPERAT=1000 INERT
$
$
$ STEP 13 CVD2 CVD NITRIDE
$
DEPOSITION NITRIDE THICKNES=.15 SPACES=2
DIFFUSION TIME=60 TEMPERAT=810 INERT
$
$
$ STEP 14  PHO3 PHOTOLITH  (ACTIVE)
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.05 SPACES=2
EXPOSE    MASK=ACTIVE
DEVELOP
$
$
$ STEP 15  ET05 NITRIDE  (PRE-FIELD
$
ETCH  NITRIDE  TRAPEZOI
$
$
$ STEP 16  ET07 STRIP
$
ETCH   PHOTORES  ALL
$
$
$ STEP 17  PHO3 PHOTOLITH  (FIELD THRESHOLD VT
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.05 SPACES=4
EXPOSE    MASK=CHANSTP
DEVELOP
$
$
$ STEP 18  IM02 IMPLANT   P IMPLANT
$
IMPLANT   BORON DOSE=6e13 ENERGY=100 PEARSON RP.EFF
$
SELECT    Z=1.0*LOG10("BORON  TITLE="PMOS AFTER CHANNEL STOP IMPLANT"
PLOT.2D   X.MIN=-1 X.MAX=6 Y.MAX=4 SCALE X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 -
 Y.OFFSET=1.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR     COLOR=6 PHOTORES
COLOR     COLOR=3 NITRIDE
COLOR     COLOR=5 OXIDE
COLOR MIN.V=15 MAX.V=20 COLOR=7
FOREACH   X=15 TO 20 STEP 1)
CONTOUR   VALUE=15 LINE.TYP=2 COLOR=1
CONTOUR   VALUE=16 LINE.TYP=2 COLOR=1
CONTOUR   VALUE=17 LINE TYP=2 COLOR=1
CONTOUR   VALUE=18 LINE.TYP=2 COLOR=1
CONTOUR   VALUE=19 LINE TYP=2 COLOR=1
CONTOUR   VALUE=20 LINE.TYP=2 COLOR=1
END
LABEL     LABEL="PHOTORESIST "CM X=1 Y=4 COLOR=1 LEFT SIZE=0.25 RECTANGL
 C.RECTAN=6 W.RECTAN= 5 H.RECTAN=.5
```

```
LABEL     LABEL="NITRIDE "CM X=1 Y=4.5 COLOR=3 LEFT SIZE=0.25 RECTANGL -
 C.RECTAN=3 W.RECTAN=.5 H.RECTAN=.5
LABEL     LABEL="OXIDE "CM X=1 Y=5 COLOR=5 LEFT SIZE=0.25 RECTANGL C.RECTAN=5 -
 W.RECTAN=.5 H.RECTAN=.5
LABEL     LABEL="BORON CONTOURS: 1e15 - 1e20" "CM X=1 Y=5.5 COLOR=1 LEFT -
 SIZE=0.25 LINE.TYPE=2 C.LINE=7 LENGTH=1.0
$
$
$ STEP 19  ET07 STRIP
$
ETCH    PHOTORES   ALL
$
$
$ STEP 20  ET04 OXIDE ETCH
$
ETCH  OXIDE  TRAPEZOI
$
$
$ STEP 21  CLO1 RCA CLEAN
$
$
$ STEP 22  OX04 WET OXIDE  (FIELD OXIDE
$
$       (START SOAK AT 1050 C)
$
METHOD  VISCOUS  GRID.OX1=4 IN1=0.2
DIFFUSION TIME=4 TEMPERAT=900 DRY02
DIFFUSION TIME=5.5 TEMPERAT=900 T.FINAL=1050 DRY02
DIFFUSION TIME=.5 TEMPERAT=1050 T.FINAL=1100 WET02
DIFFUSION TIME=209.5 TEMPERAT=1100 WET02
DIFFUSION TIME=10 TEMPERAT=1100 T.FINAL=1000 INERT
DIFFUSION TIME=4 TEMPERAT=1000 INERT
$
$
$   CALCULATE THE STRESS IN THE SILICON SUBSTRATE
$
METHOD  *SKIP.SOL
DIFFUSION TIME=25.6  TEMP=1100  WET02
SAVEFILE        OUT.FILE=locosstress.imp
$
SELECT  TITLE="LOCOS INDUCED STRESS IN SUBSTRATE AND OXIDE"
PLOT.2D  SCALE  STRESS  VLEN=0.35  X.MIN=0  X.MAX=2 Y.MAX=2.5 -
C.COMPRE=4  C.TENSIO=2  L.TENSIO=2
$
$
SELECT  TITLE="CONTOURS OF PRESSURE"
PLOT.2D  SCALE  X.MIN=-1  X.MAX=6  Y.MAX=3
COLOR    NITRIDE   COLOR=3
SELECT   Z=-1.0 *(SXX+SYY)
CONTOUR  VALUE=1e8 LINE=1 COLOR=11
CONTOUR  VALUE=5e8 LINE=2 COLOR=11
CONTOUR  VALUE=1e9 LINE=3 COLOR=12
CONTOUR  VALUE=5e9 LINE=4 COLOR=13
CONTOUR  VALUE=1e5 LINE=5 COLOR=14
CONTOUR  VALUE=5e5 LINE=6 COLOR=15
CONTOUR  VALUE=1e6 LINE=7 COLOR=16
CONTOUR  VALUE=1e7 LINE=8 COLOR=18
CONTOUR  VALUE=5e7 LINE=10 COLOR=19
SELECT   Z=Y
PRINT.1D  SILICON /OXIDE
```

```
$
LABEL X=6    Y=-0.55 LABEL="1E3"  LINE.TYP=1 C.LINE=10 LENGTH=1.0
LABEL X=6    Y=-0.25 LABEL="5E3"  LINE.TYP=2 C.LINE=11 LENGTH=1.0
LABEL X=6    Y=0.35  LABEL="5E4"  LINE.TYP=4 C.LINE=13 LENGTH=1.0
LABEL X=6    Y=0.95  LABEL="5E5"  LINE.TYP=6 C.LINE=15 LENGTH=1.0
LABEL X=6    Y=1.55  LABEL="5E6"  LINE.TYP=8 C.LINE=17 LENGTH=1.0
LABEL X=6    Y=2.15  LABEL="5E7"  LINE.TYP=10 C.LINE=19 LENGTH=1.0
LABEL X=6    Y=2.65  LABEL="1.4E8"  LINE.TYP=7 C.LINE=4 LENGTH=1.0
LABEL X=6    Y=3.25  LABEL="2.0E8"  LINE.TYP=10 C.LINE=4 LENGTH=1.0
$
SELECT       Z=Y
PRINT.1D     SILICON /OXIDE
$
$
$ END OF PROCESSING
$
SAVEFILE  OUT.FILE=locos50
STOP
```

NMOS

```
TL1  0001
/ These will be user-generated comments.
/
%% ---------------- LORENZO ----------------
%% Mask layout file for 1-dimensional data
%% -----------------------------------------
1.000000E-03
   0  5000
10
PWELL          0
ACTIVE         1
     0     4500
CHANSTP        2
     0     4500
NMOSVT         3
POLY1          4
     0     1000
POLY2          5
P-S/D          6
     0     5000
N-S/D          7
  4000     5000
CONTCUT        8
     0     2000
  3000     5000
METAL1         9
  1750     3250
```

PMOS

```
TL1  0001
/ These will be user-generated comments.
/
%% ---------------- LORENZO ----------------
%% Mask layout file for 1-dimensional data
%% -----------------------------------------
1.000000E-03
   0  5000
10
PWELL          1
     0     5000
ACTIVE         4
     0     4500
CHANSTP        2
     0     5000
NMOSVT         1
     0     5000
POLY1          4
     0     1000
POLY2          5
P-S/D          6
     0     5000
  4500     5000
N-S/D          7
     0     5000
CONTCUT        8
     0     2000
  3000     5000
METAL1         9
  1750     3250
```

PMOS Poly2

```
TL1  0001
/ These will be user-generated comments.
/
%% ---------------- LORENZO ----------------
%% Mask layout file for 1-dimensional data
%% -----------------------------------------
1.000000E-03
   0  5000
10
PWELL          1
     0     5000
ACTIVE         4
     0     4500
CHANSTP        2
     0     5000
NMOSVT         1
     0     5000
POLY1          4
POLY2          5
     0     1000
P-S/D          6
     0     5000
  4500     5000
N-S/D          7
     0     5000
CONTCUT        8
     0     2000
  3000     5000
METAL1         9
  1750     3250
```

LOCOS

```
TL1  0001
/ These will be user-generated comments.
/
%% ---------------- LORENZO ----------------
%% Mask layout file for 1-dimensional data
%% -----------------------------------------
1.000000E-03
   0  2000
3
PWELL          0
ACTIVE         1
     0     1500
CHANSTP        2
     0     1500
```

```
$
$  T-SUPREM4/MEDICI INTERFACE FOR NMOS
$
$
$
$ MESH  IN.FILE=nmos.str  TSUPREM4  ELEC.BOT  Y.MAX=2.5
$
$ INTERFACE S.N=0.0 S.P=0.0 QF=3e11 N.ACCEPT=0.0 P.ACCEPT=0.0 N.DONOR=0.0 P.DONO
$
$ SYMB  CARRIERS=0
$ METHOD  ICCG  DAMPED
$ SOLVE  V1=0
$ SYMB  CARRIERS=1  NEWTON  ELECTRON
$ LOG  IVFILE=nmos1V0
$ SOLVE  V2=0  ELEC=2  VSTEP=0.25  NSTEP=10
$
$
$ SYMB  CARRIERS=0
$ METHOD  ICCG  DAMPED
$ SOLVE  V1=1
$ SYMB  CARRIERS=1  NEWTON  ELECTRON
$ LOG  IVFILE=nmos1V1
$ SOLVE  V2=0  ELEC=2  VSTEP=0.1  NSTEP=10
$ SOLVE  V2=1  ELEC=2  VSTEP=0.2  NSTEP=10
$
$
$ SYMB CARRIERS=0
$ METHOD  ICCG  DAMPED
$ SOLVE  V1=2
$ SYMB  CARRIERS=1  NEWTON  ELECTRON
$ LOG  IVFILE=nmos1V2
$ SOLVE  V2=0  ELEC=2 VSTEP=0.1  NSTEP=10
$
$
$ SYMB  CARRIERS=0
$ METHOD  ICCG  DAMPED
$ SOLVE  V1=3
$ SYMB  CARRIERS=1  NEWTON  ELECTRON
$ LOG  IVFILE=nmos1V3
$ SOLVE  V2=0  ELEC=2  VSTEP=0.1  NSTEP=10
$
$
$ SYMB  CARRIERS=0
$ METHOD  ICCG  DAMPED
$ SOLVE  V1=4
$ SYMB  CARRIERS=1  NEWTON  ELECTRON
$ LOG  IVFILE=nmos1V4
$ SOLVE  V2=0  ELEC=2  VSTEP=0.1  NSTEP=10
$
$
$ SYMB  CARRIERS=0
$ METHOD  ICCG  DAMPED
$ SOLVE  V1=5
$ SYMB  CARRIERS=1  NEWTON  ELECTRON
$ LOG IVFILE=nmos1V5
$ SOLVE  V2=1  ELEC=2  VSTEP=0.1  NSTEP=10
$ PLOT Ide vs Vds
$
PLOT.2D   X.AXIS=V2 Y.AXIS=I2 IN FILE=nmos1V5 LEFT=0 C RIGHT=5 BOTTOM=0 T
 X.OFFSET=0.0 Y.OFFSET=0 T TITLE="NMOS II vs V2 for Vg=0.5V & Vds=1 to 5V"



 T.SIZE=0.4 X.SIZE=0.25 Y.SIZE=0.25 SYMBOL=1 C.SIZE=0.25 LINE.TYP=1 COLOR=1
$
$
PLOT.1D   X.AXIS=V1 Y.AXIS=I2 IN FILE=nmos1V2 T.SIZE=0.4 X.SIZE=0.25 -
 Y.SIZE=0.25 UNCHANGE ^CLEAR SYMBOL=2 C.SIZE=0.25 LINE.TYP=1 COLOR=1
$
$
PLOT.1D   X.AXIS=V1 Y.AXIS=I2 IN FILE=nmos1V3 T.SIZE=0.4 X.SIZE=0.25 -
 Y.SIZE=0.25 UNCHANGE ^CLEAR SYMBOL=3 C.SIZE=0.25 LINE.TYP=1 COLOR=1
$
$
PLOT.1D   X.AXIS=V1 Y.AXIS=I2 IN FILE=nmos1V4 T.SIZE=0.4 X.SIZE=0.25 -
 Y.SIZE=0.25 UNCHANGE ^CLEAR SYMBOL=4 C.SIZE=0.25 LINE.TYP=1 COLOR=1
$
$
PLOT.1D   X.AXIS=V1 Y.AXIS=I2 IN FILE=nmos1V5 T.SIZE=0.4 X.SIZE=0.25 -
 Y.SIZE=0.25 UNCHANGE ^CLEAR SYMBOL=5 C.SIZE=0.25 LINE.TYP=1 COLOR=1
$
STOP
```

```
$
$  T-SUPREM4/MEDICI INTERFACE FOR NMOS
$
$
$
MESH  IN.FILE=nmos.str  TSUPREM4  ELEC.BOT  Y.MAX=2.5
$
INTERFACE S.N=0.0 S.P=0.0 QF=3e11 N.ACCEPT=0.0 P.ACCEPT=0.0 N.DONOR=0.0 +
 P.DONOR=0.0
$
SYMB  NEWTON  CARRIERS=1  ELECTRONS
$
LOG   IVFILE=nmoslogg
$
$ Vds=0.1 then ramp gate to 5V
$
SOLVE  V2=.1
$SOLVE  V1=.1  ELEC=1  VSTEP=.2  NSTEP=10
$
$
EXTRACT   MOS.PARA DRAIN=2 GATE=1 IN FILE=nmoslogg
$
$ PLOT Ids vs Vgs
$
PLOT.1D  Y.AXIS=DI  X.AXIS=V1  IN.FILE=nmoslogg  points  color=1
+ TITLE="NMOS Id vs Vg for Qf=3e11 and Vds=0.1"
$
$$$$
```

```
$
$  T-SUPREM4/MEDICI INTERFACE FOR NMOS
$
$
$
$ MESH  IN.FILE=pmos.str  TSUPREM4  ELEC.BOT  Y.MAX=2.5
$
$ INTERFACE S.N=0.0 S.P=0.0 QF=3e11 N.ACCEPT=0.0 P.ACCEPT=0.0 N.DONOR=0.0 P.DONO
$
$
$ SYMB  CARRIERS=0
$ METHOD  ICCG  DAMPED
$ SOLVE  V2=-1
$ SYMB  CARRIERS=1  NEWTON  hole
$ LOG  IVFILE=pmoslv1
$ SOLVE  V2=2  ELEC=2  VSTEP=-0.1  NSTEP=11
$ SOLVE  V2=-1  ELEC=2  VSTEP=0.2  NSTEP=21
$
$
PLOT.1D   X.AXIS=V2 Y.AXIS=I2 IN.FILE=pmoslv1 LEFT=-5 RIGHT=0 BOTTOM=0.0 +
 X.OFFSET=1.0 Y.OFFSET=2.0 TITLE="PMOS ID vs V2 for Vg=-1V and Vds=-1 to 5V" +
 Y.SIZE=0.6 X.SIZE=0.25 Y.SIZE=0.25 SYMBOL=1 X.SIZE=0.25 LINE.TYP=1 COLOR=1
$
$
$$$$
```

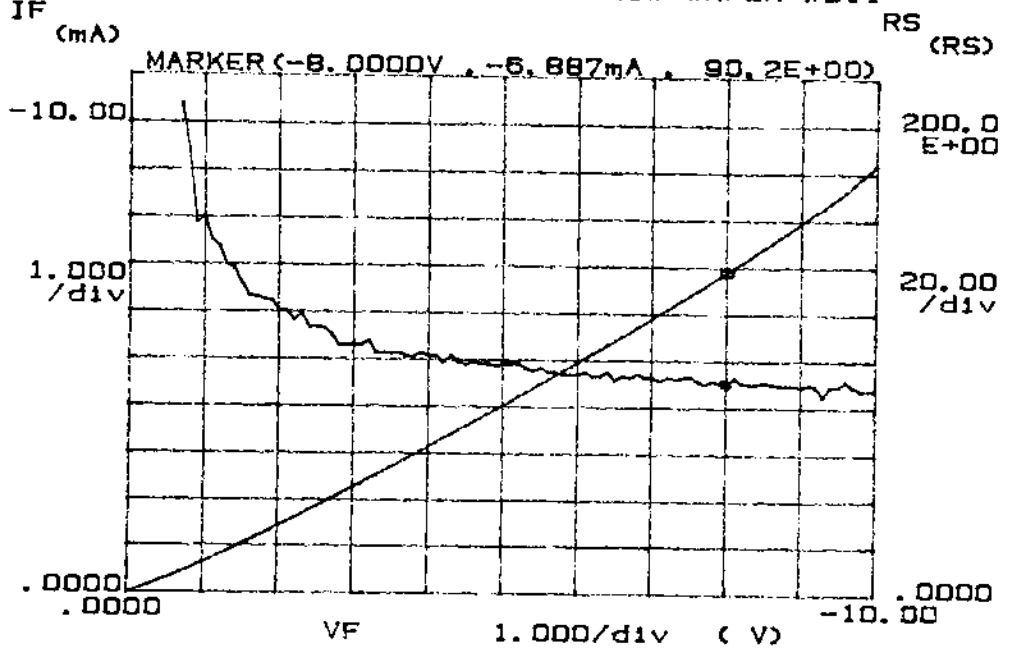
```
$
$  T-SUPREM4/MEDICI INTERFACE FOR PMOS
$
$
$
MESH       TSUPREM4 ELEC.BOT Y.TOLER=0 Y.MAX=2.5 IN.FILE=pmos2.str RECTANGU
$
$
INTERFACE S.N=0.0 S.P=0.0 QF=3e11 N.ACCEPT=0.0 P.ACCEPT=0.0 N.DONOR=0.0 +
 P.DONOR=0.0
$
CONTACT   NUMBER=1 N.POLYSI
$
$
SYMBOLIC  GUMMEL  CARRIERS=2
$
SOLVE     V1=0 V2=-1
$
SYMBOLIC  GUMMEL  CARRIERS=1  HOLES  PRINT
$
LOG       IVFILE=pmos2log
$
$ Vds=-1 then ramp gate to -5V
$
SOLVE     V1=0 V2=-1 ELECTRODE 1  VSTEP=-0.1 NSTEPS=60
$
$
EXTRACT   MOS.PARA DRAIN=2 GATE=1 IN FILE=pmos2log
$
$ PLOT Ids vs Vgs
$
PLOT.1D   X.AXIS=V1 Y.AXIS=I2 IN.FILE=pmos2log LEFT=0 RIGHT=-6 BOTTOM=0.0 +
 X.OFFSET=1.0 Y.OFFSET=4 TITLE="PMOS ID-VG for Vds=-1 and Qf=3e11" Y.SIZE=4 +
 X.SIZE=1.25 Y.SIZE=1.25 POINTS C.SIZE=0.25 LINE TYP=1 COLOR=1
$
$$$$
```

APPENDIX D

Parameter Measurements

****** GRAPHICS PLOT ******

P+ VANDERPAUW WAFER #D11



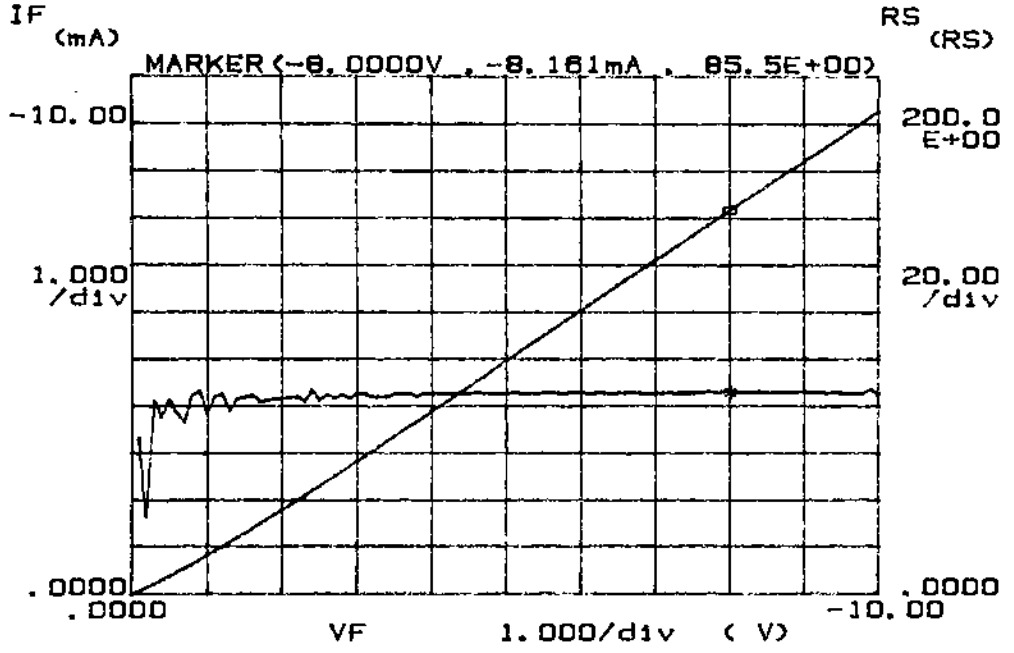
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -10.000V
Step - .1000V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V1-V2)*4.532/IF

****** GRAPHICS PLOT ******

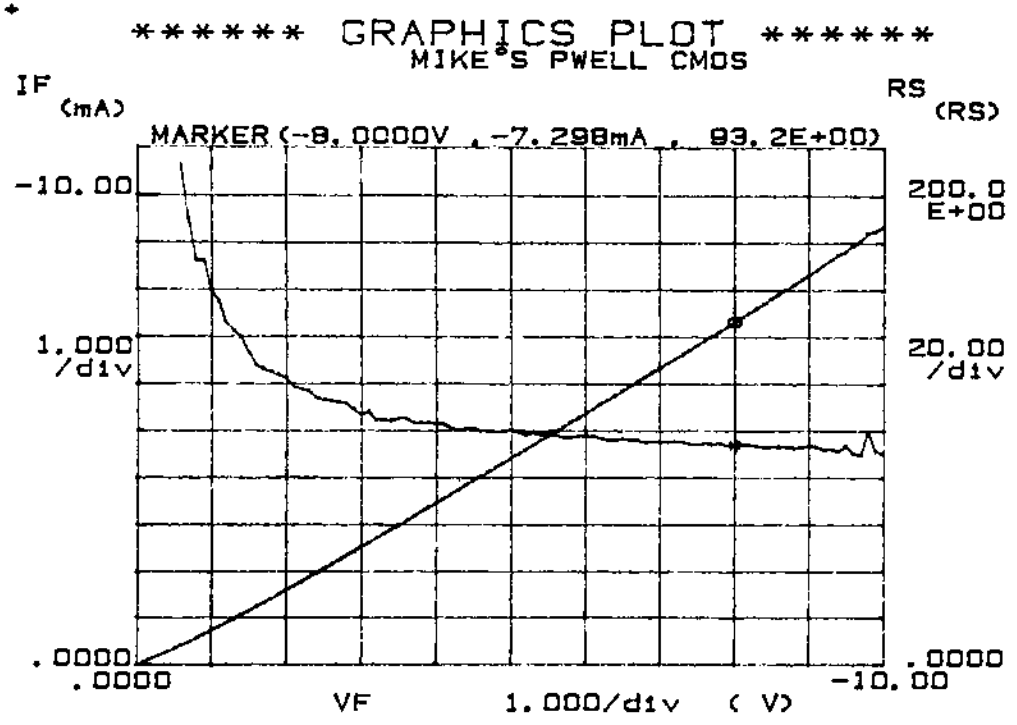
MIKE'S PWELL CMOS



Variables:
VF -Ch1
Linear sweep
Start .0000V
Stop -10.000V
Step -.1000V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V1-V2)*4.582/IF



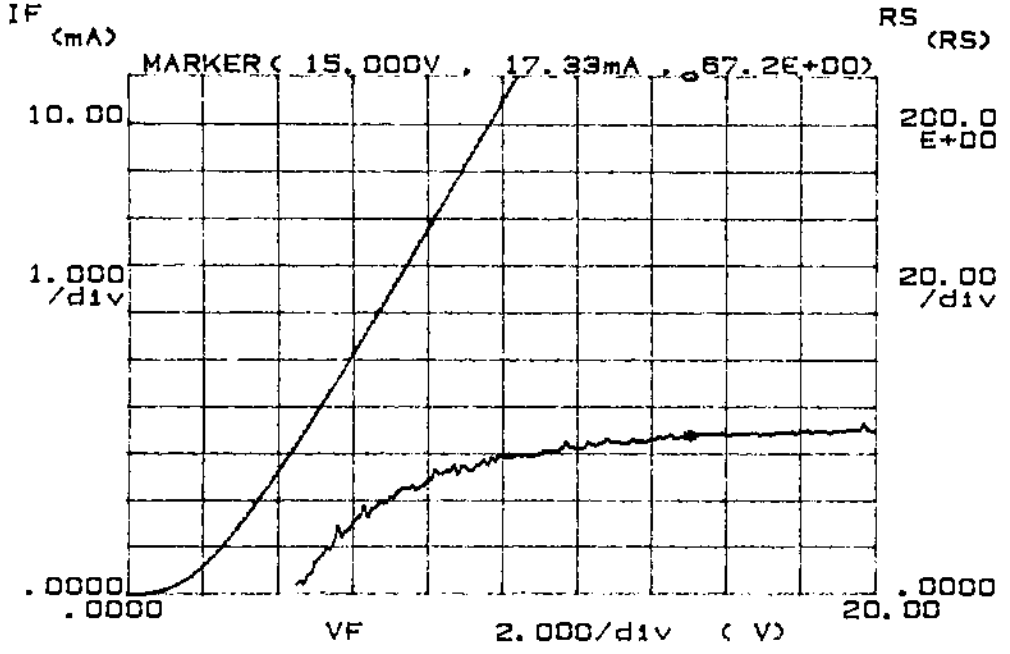
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -10.000V
Step -.1000V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V1-V2)*4.532/IF

****** GRAPHICS PLOT ******

N+ VANDERPAUW WAFER#11



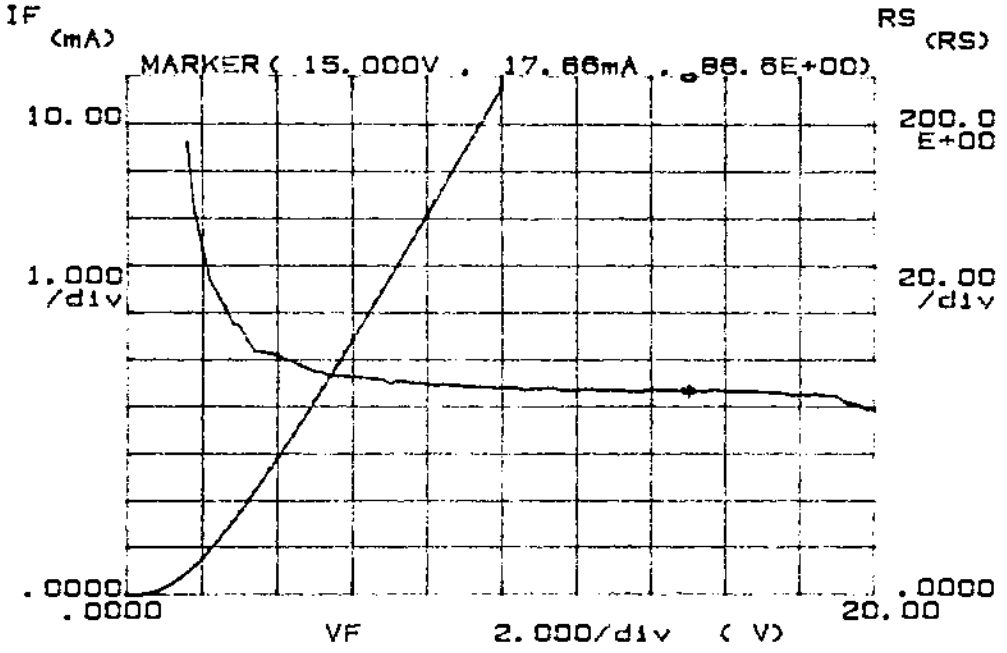
Variables:
VF -Ch1
Linear sweep
Start .0000V
Stop 20.000V
Step .1000V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

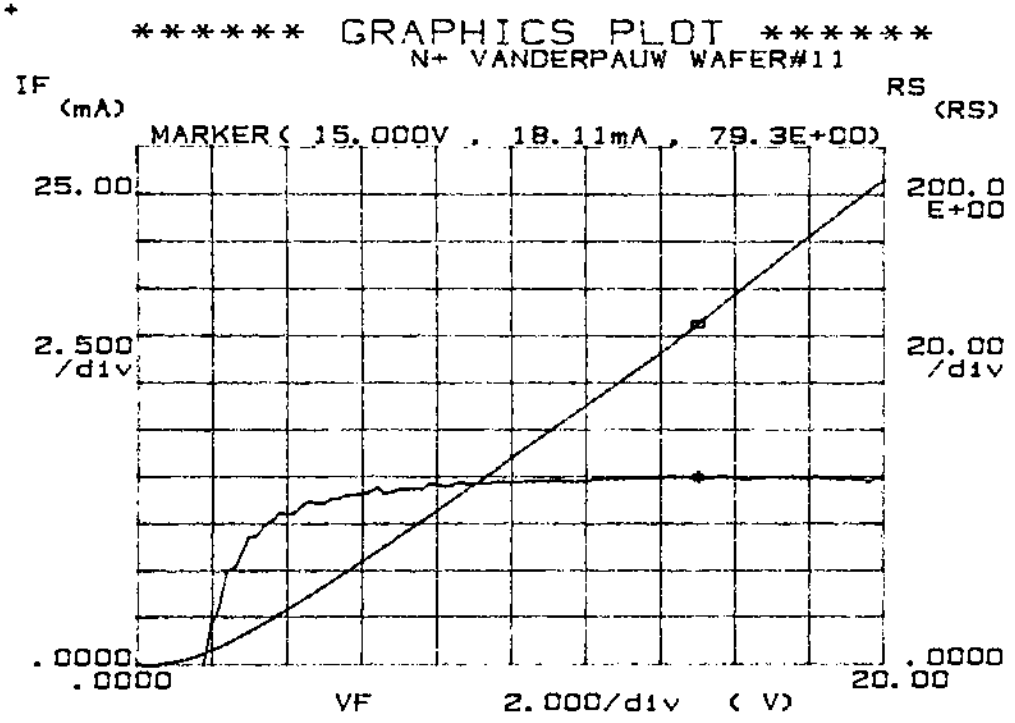
N+ VANDERPAUW WAFER#11



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 20.000V
Step .2000V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF



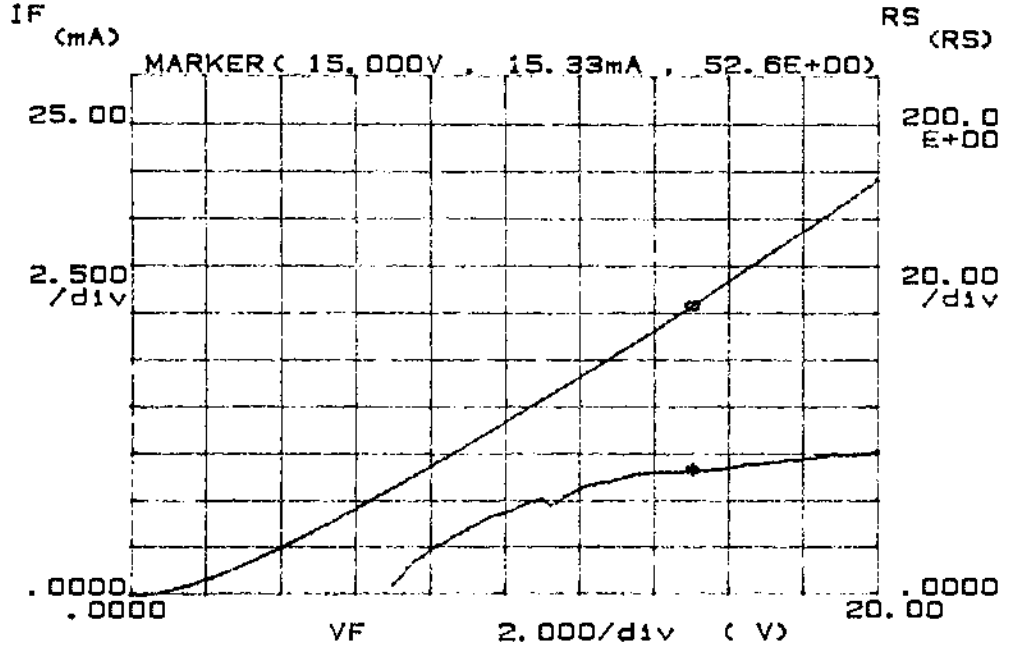
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 20.000V
Step .2000V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.932/IF

****** GRAPHICS PLOT ******

N+ VANDERPAUW WAFER#11



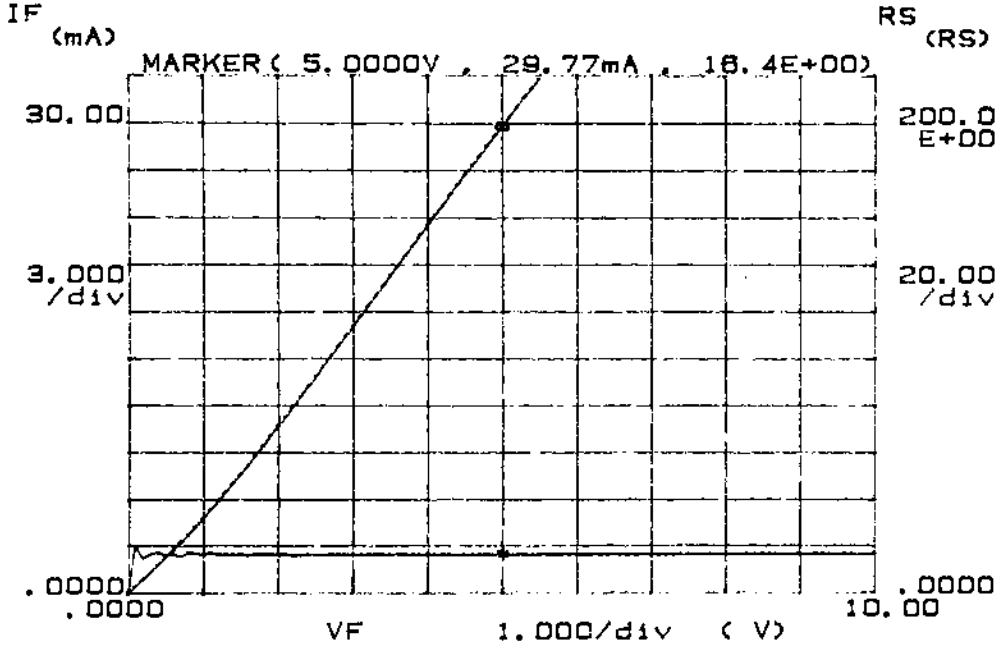
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 20.000V
Step .2000V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

N+ POLY VANDERPAUW WAF#11



Variables:

VF	-Ch1	
Linear sweep		
Start		.0000V
Stop		10.000V
Step		.1000V

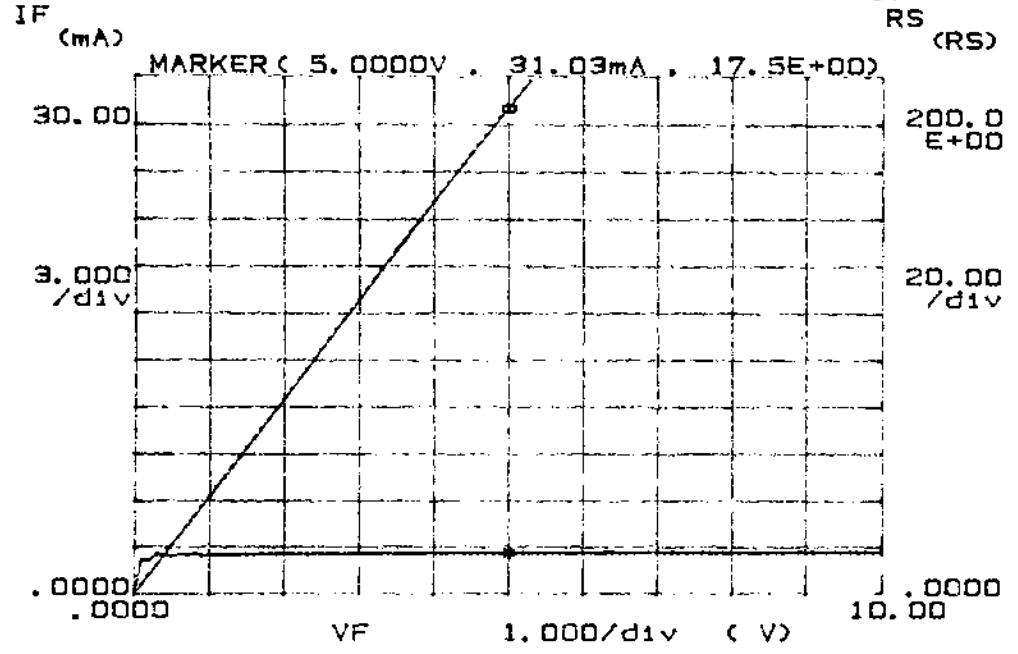
Constants:

I1	-Ch2	.000 A
V	-Ch3	.0000V
I2	-Ch4	.000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

N+ POLY VANDERPAUW WAF#11



Variables:

VF	-Ch1	
Linear sweep		
Start		.0000V
Stop		10.000V
Step		.1000V

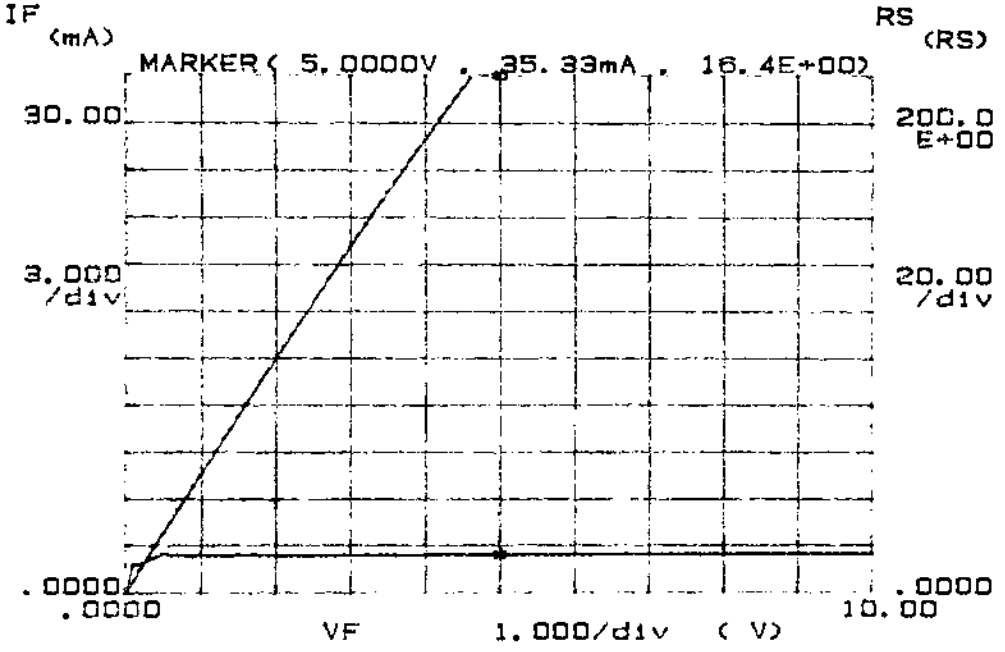
Constants:

I1	-Ch2	.000 A
V	-Ch3	.0000V
I2	-Ch4	.000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

N+ POLY VANDERPAUW WAF#11



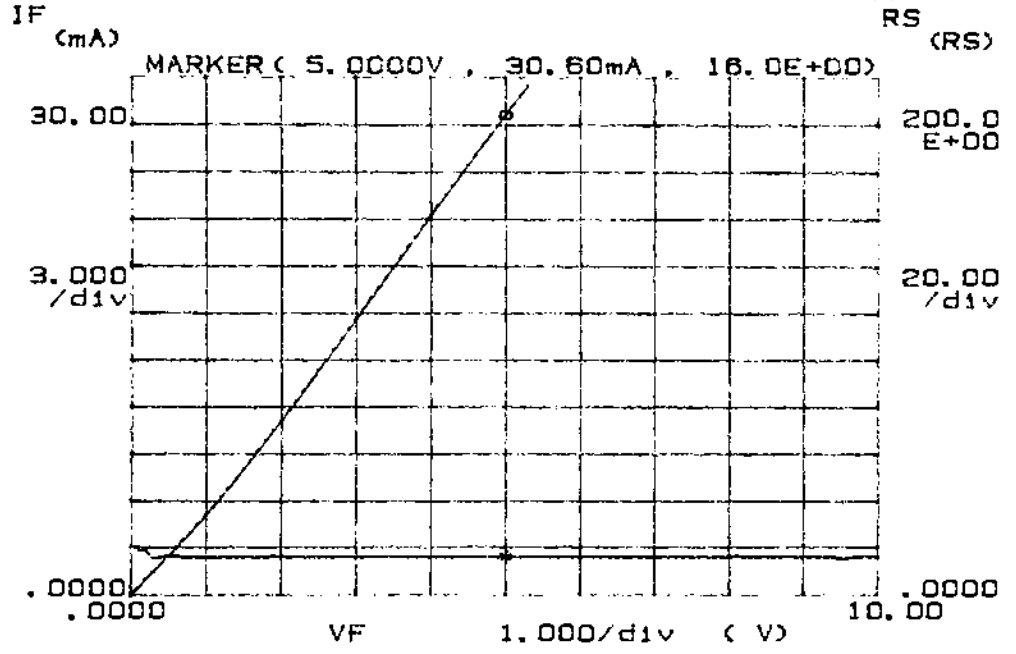
Variables:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

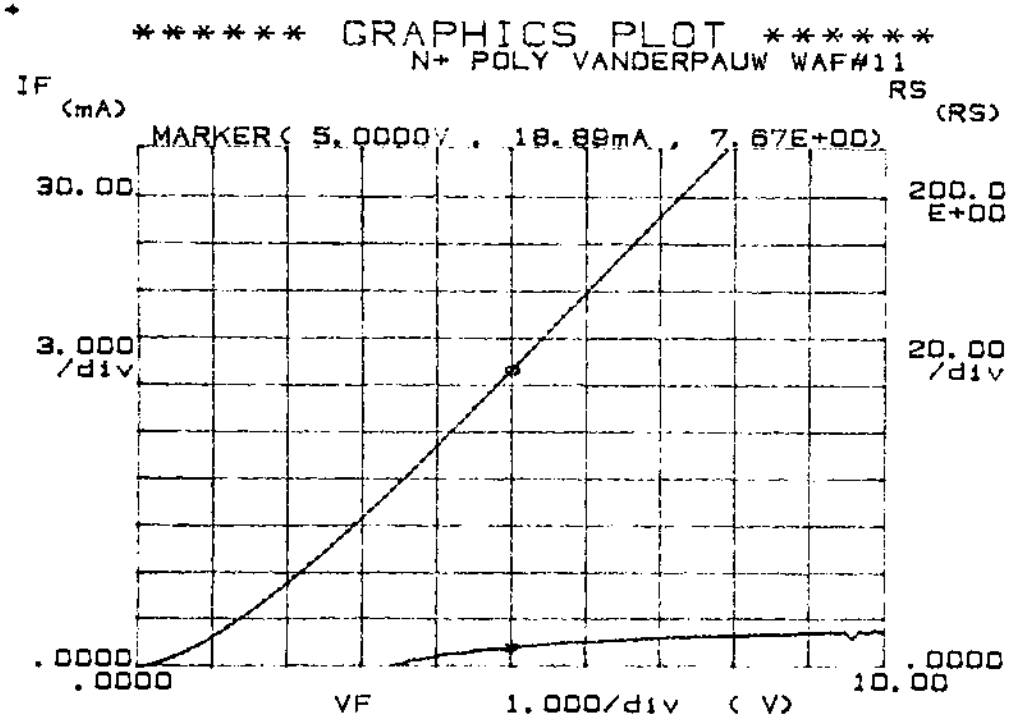
N+ POLY VANDERPAUW WAF#11



Variable1:
VF --Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constante:
I1 --Ch2 .000 A
V --Ch3 .0000V
I2 --Ch4 .000 A

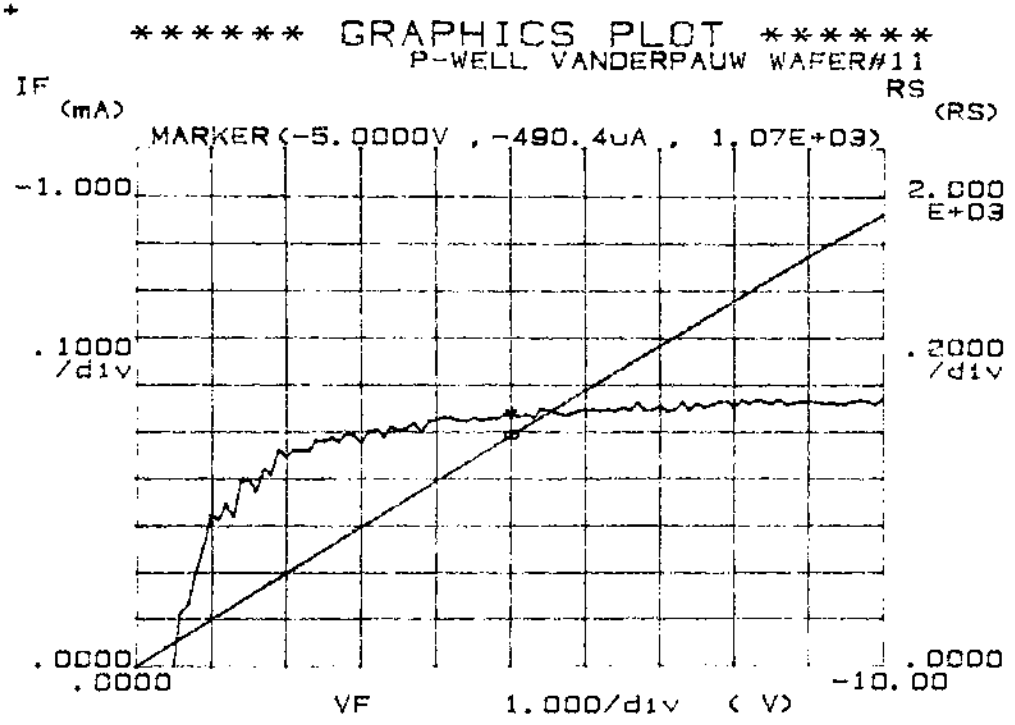
RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF



Variable1:
VF ~Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
I1 ~Ch2 .000 A
V ~Ch3 .0000V
I2 ~Ch4 .000 A

RC (RC) = (V2-V1)/IF
RB (RB) = (V2-V1)*4.532/IF



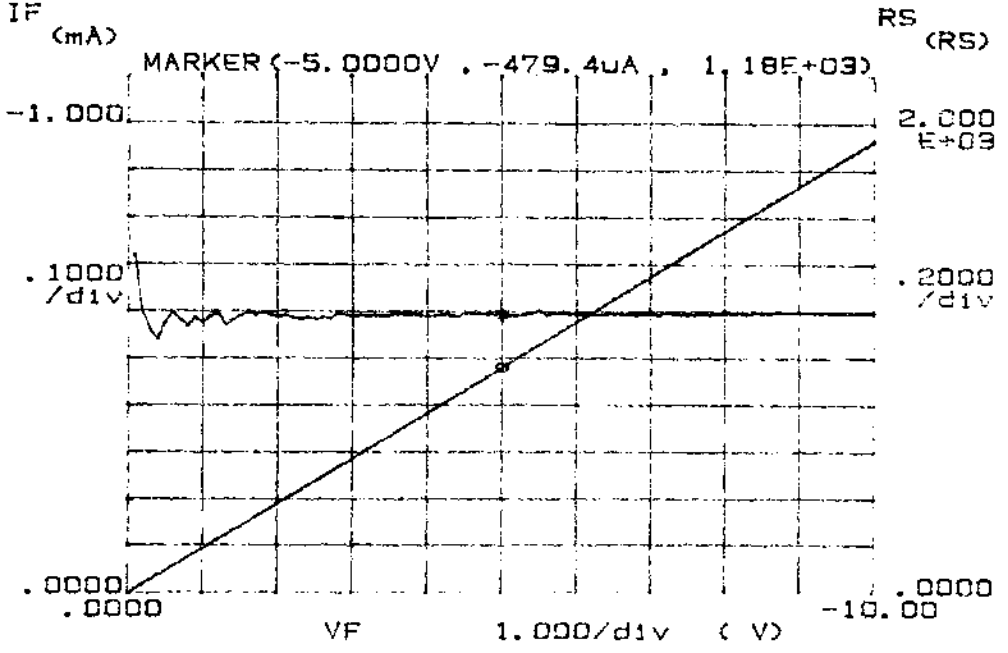
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -10.000V
Step -.1000V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

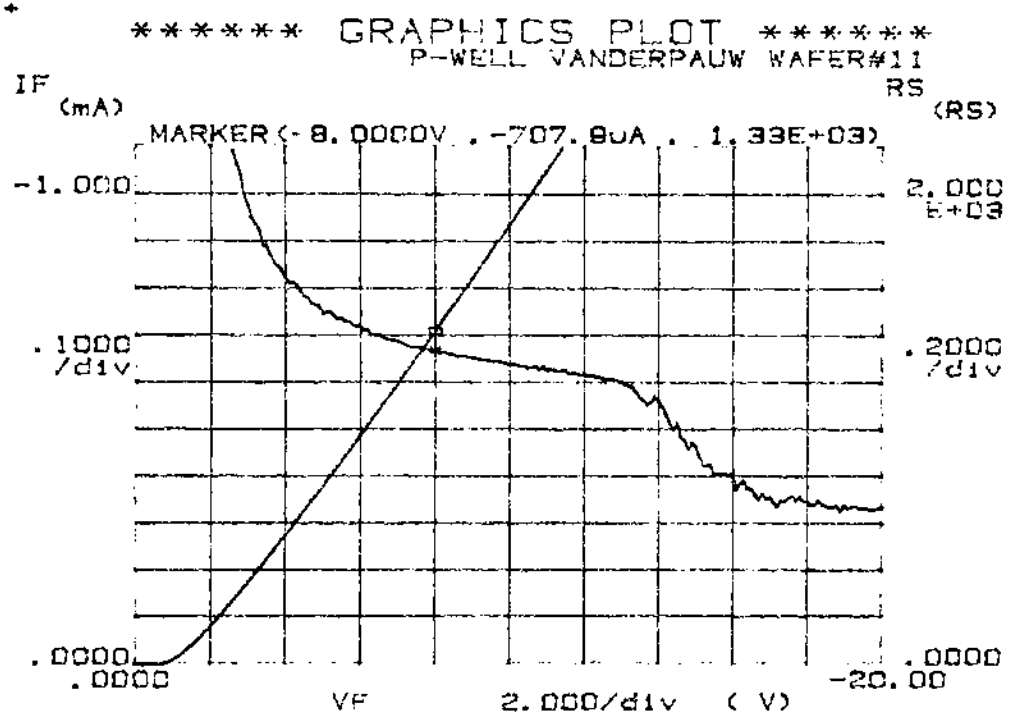
P-WELL VANDERPAUW WAFER#11



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -10.000V
Step -.1000V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.592/IF



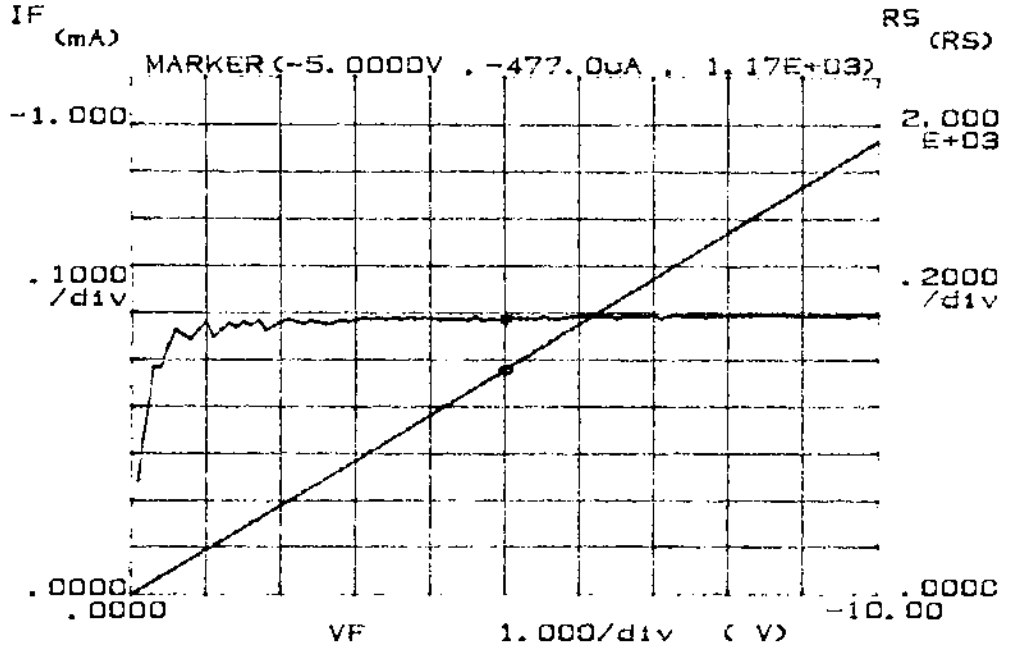
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -20.000V
Step -.1000V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

P-WELL VANDERPAUW WAFER#11



Variables:

VF	-Ch1	
Linear sweep		
Start		.0000V
Stop		-10.000V
Step		- .1000V

Constants:

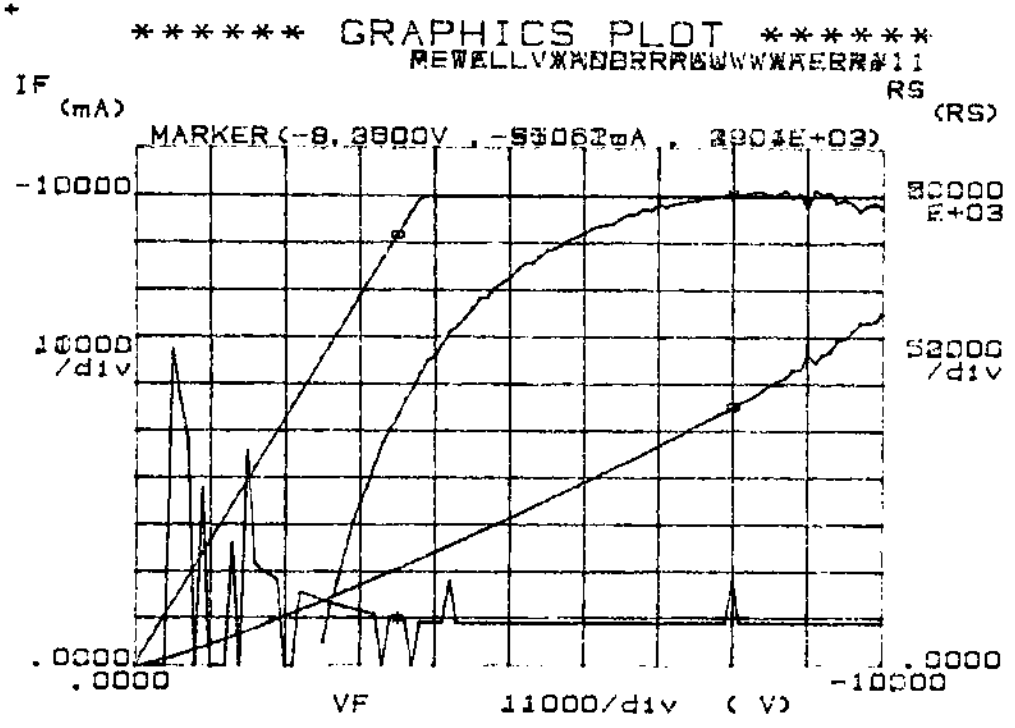
I1	-Ch2	.000 A
V	-Ch3	.0000V
I2	-Ch4	.000 A

RC (RC) = (V2-V1)/IF

RS (RS) = (V2-V1)*4.532/IF

Metal Vanderpaw

81-D



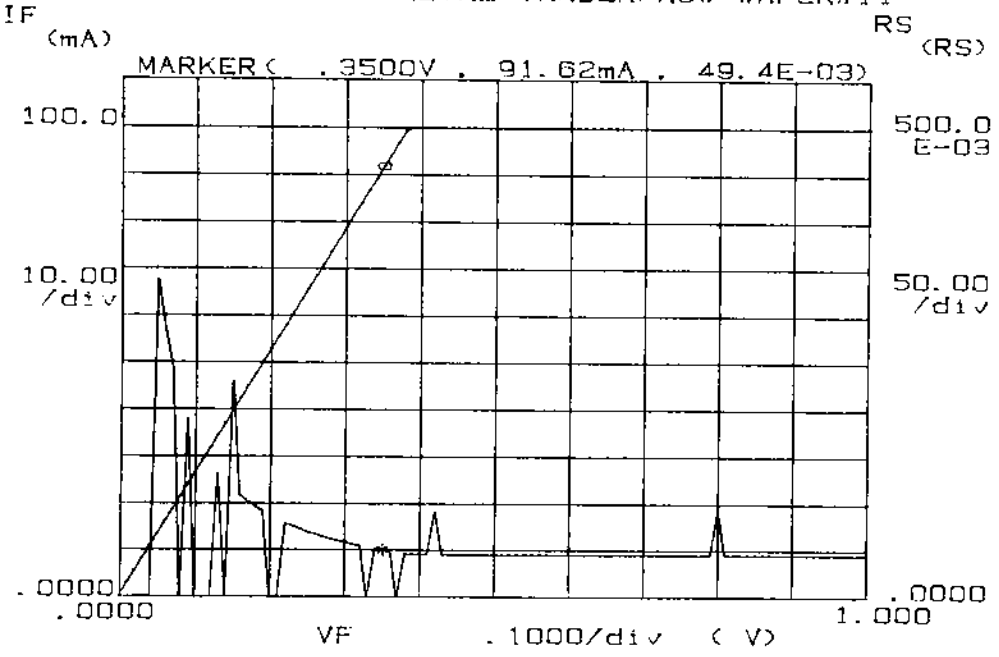
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -100000V
Step - .8800V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

METAL VANDERPAUW WAFER#11



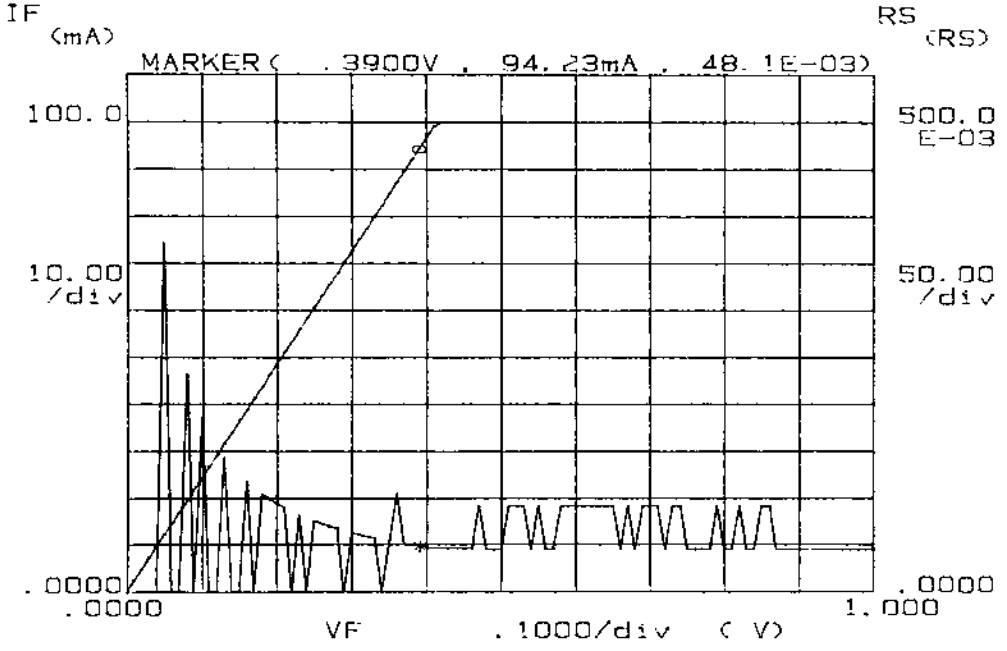
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 1.0000V
Step .0100V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

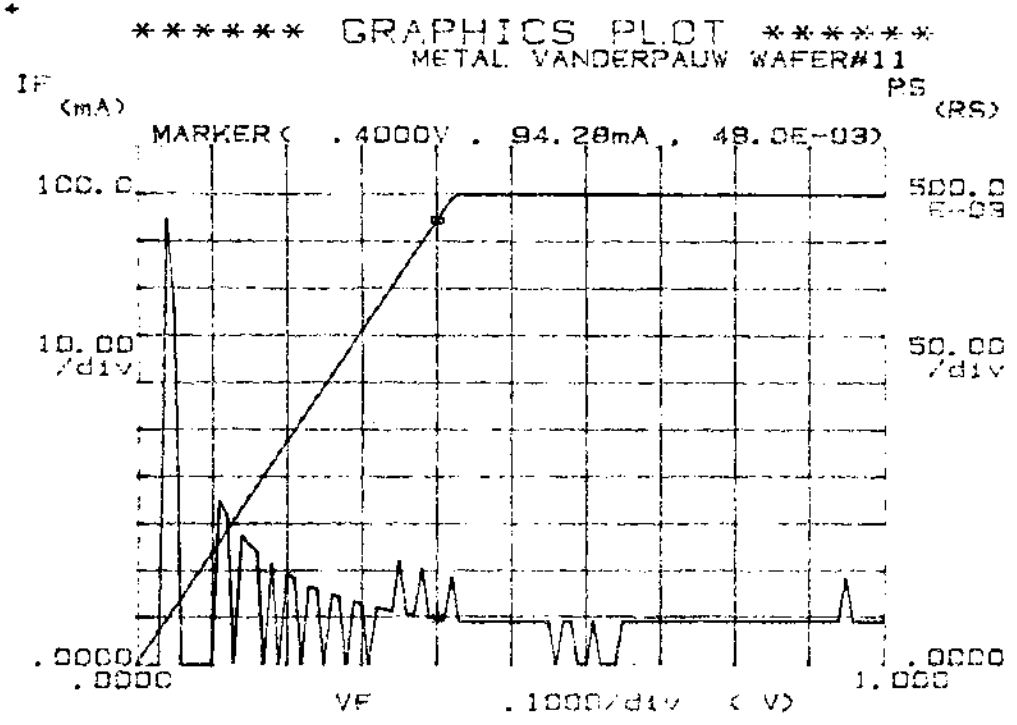
METAL VANDERPAUW WAFER#11



Variable:
VF -Ch1
Linear sweep
Start .0000V
Stop 1.0000V
Step .0100V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF



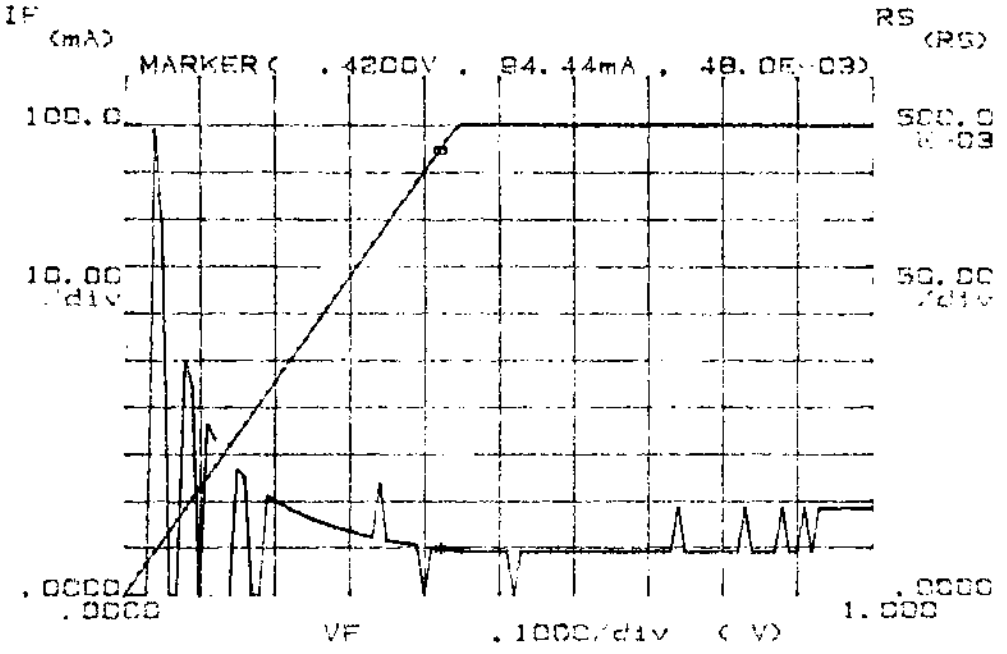
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step 1.0000V
Stop .0100V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

METAL VANDERPAUW WAFER#11

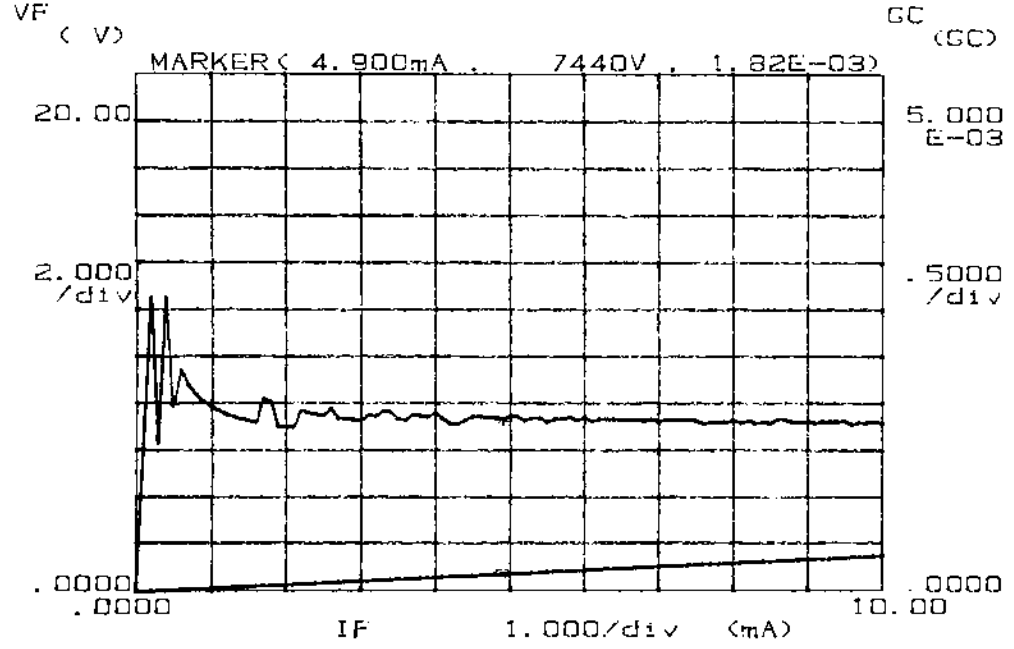


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 1.0000V
Step .0100V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******



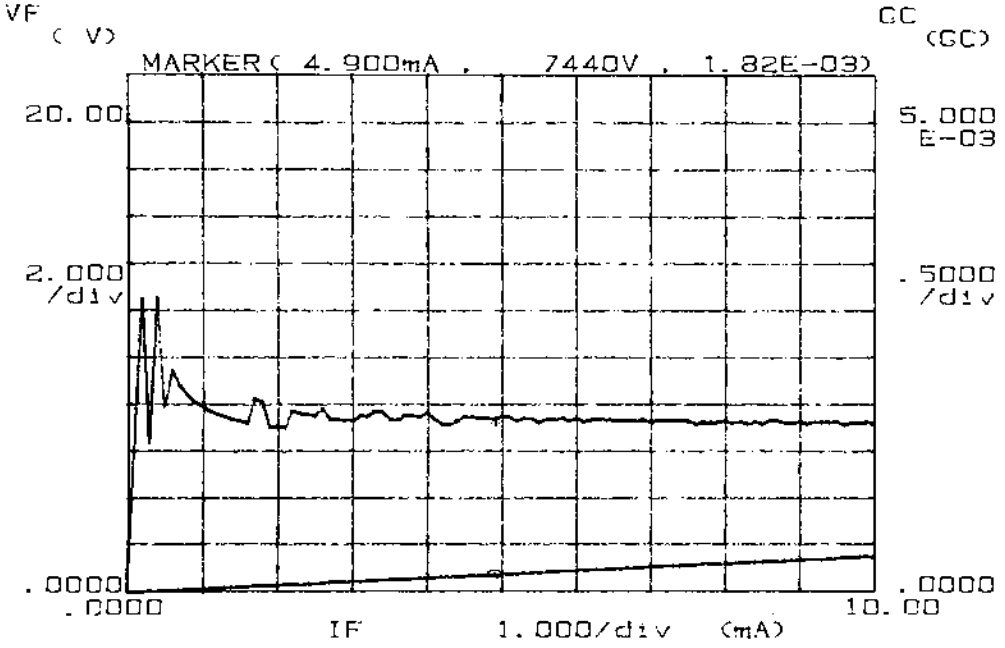
Variable1:
IF -Ch1
Linear sweep
Start .000 A
Stop 10.00mA
Step 100.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

GC (GC) = IF/84/(V1-V2)
RB (RB) = (V1-V2)*4.532/IF

****** GRAPHICS PLOT ******

METAL-POLY CBKR W#11



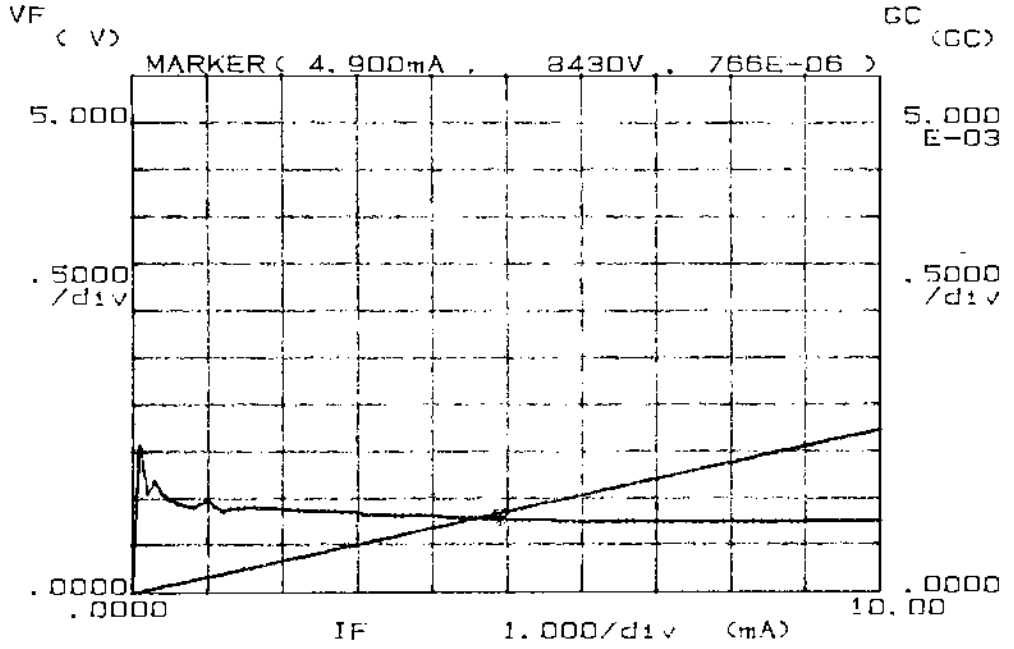
Variable1:
IF -Ch1
Linear sweep
Start .000 A
Stop 10.00mA
Step 100.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

CC (GC) = IF/84/(V1-V2)
RS (RS) = (V1-V2)*4.532/IF

****** GRAPHICS PLOT ******

METAL-POLY CBKR W#11



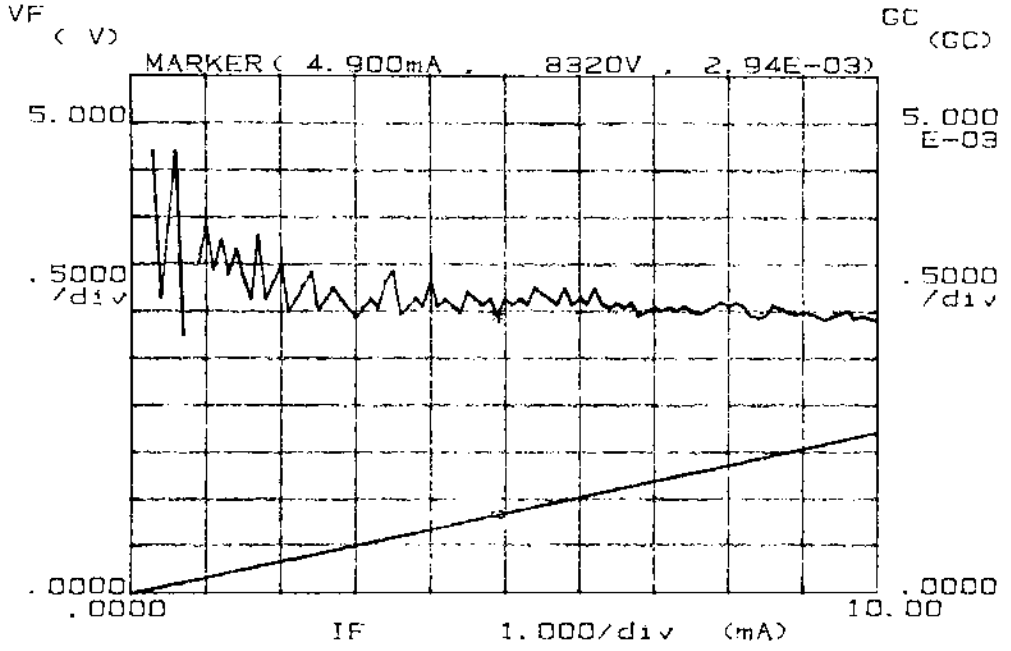
Variable1:
IF --Ch1
Linear sweep
Start .000 A
Stop 10.00mA
Step 100.0uA

Constants:
I1 --Ch2 .000 A
V --Ch3 .0000V
I2 --Ch4 .000 A

GC (GC) = IF/84/(V1-V2)
RS (RS) = (V1-V2)*4.592/IF

****** GRAPHICS PLOT ******

METAL-POLY CBKR W#11



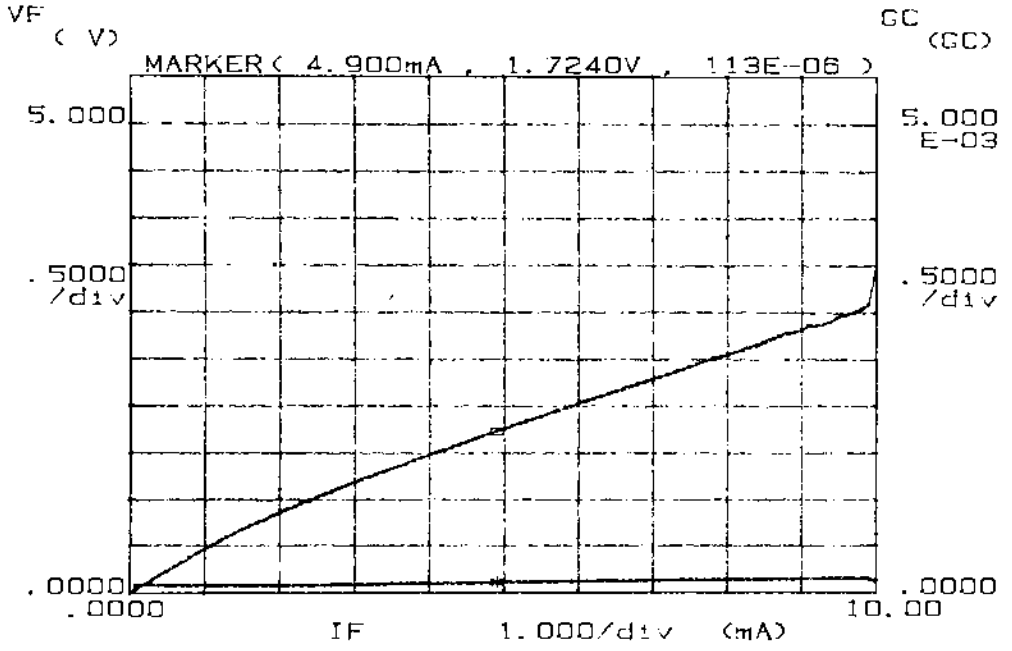
Variable:
IF -Ch1
Linear sweep
Start .000 A
Stop 10.00mA
Step 100.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

GC (GC) = IF/64/(V1-V2)
RS (RS) = (V1-V2)*4.532/IF

****** GRAPHICS PLOT ******

METAL-POLY CBKR W#11



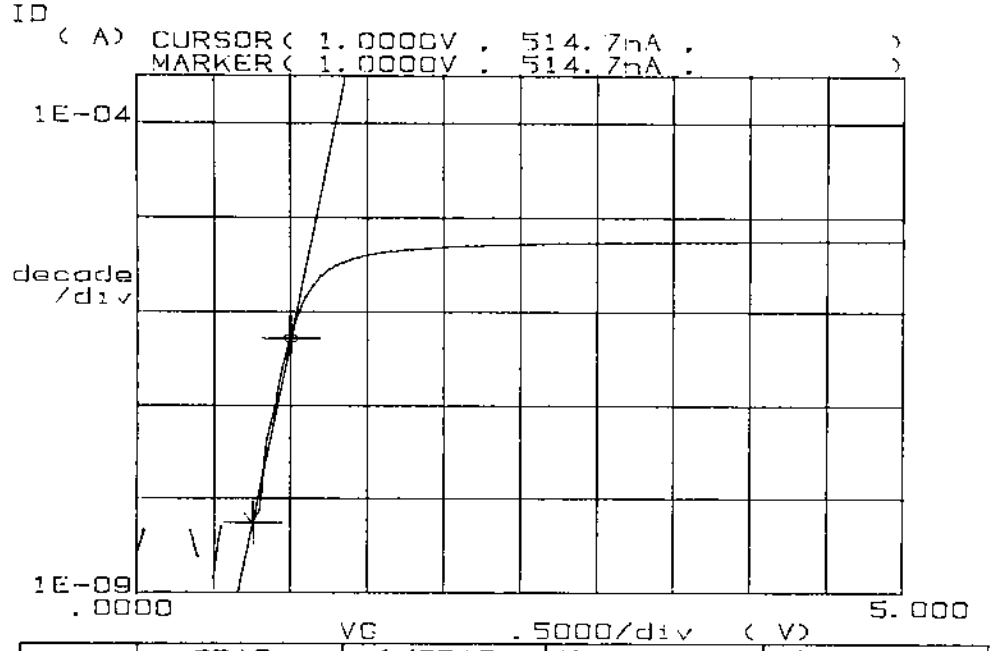
Variable1:
IF -Ch1
Linear sweep
Start .000 A
Step 10.00mA
Step 100.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

GC (GC) = IF/64/(V1-V2)
RS (RS) = (V1-V2)*4.532/IF

****** GRAPHICS PLOT ******

NMOS 6/32 SUBVT #D4



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	7.85E+00	127E-03	1.80E+00	7.04E-15
LINE2				

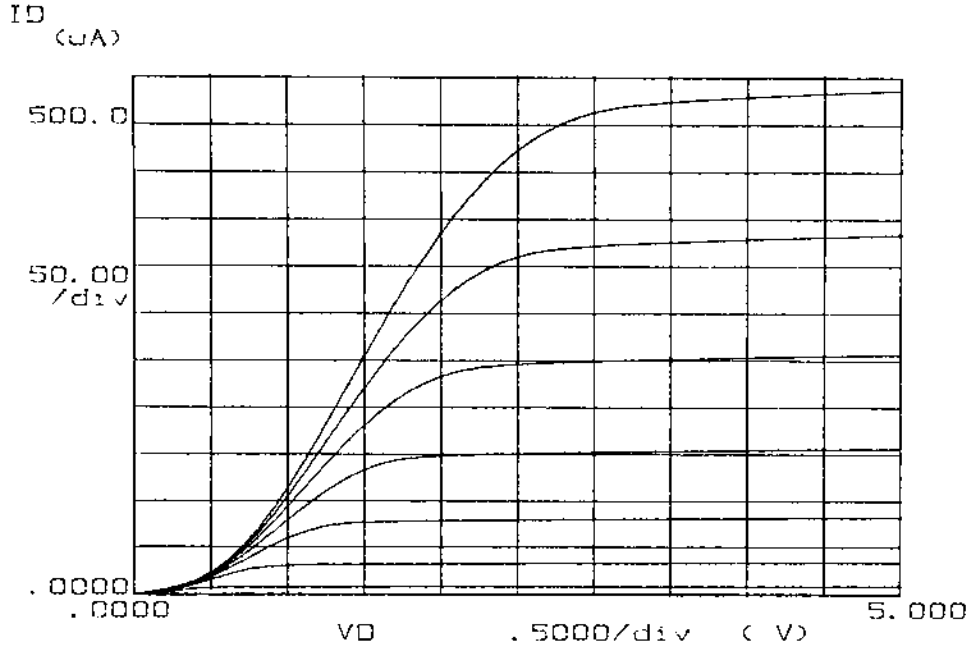
Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Variable2:
VD -Ch3
Start .1000V
Stop .1000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

NMOS 6/32 IDVD #D4



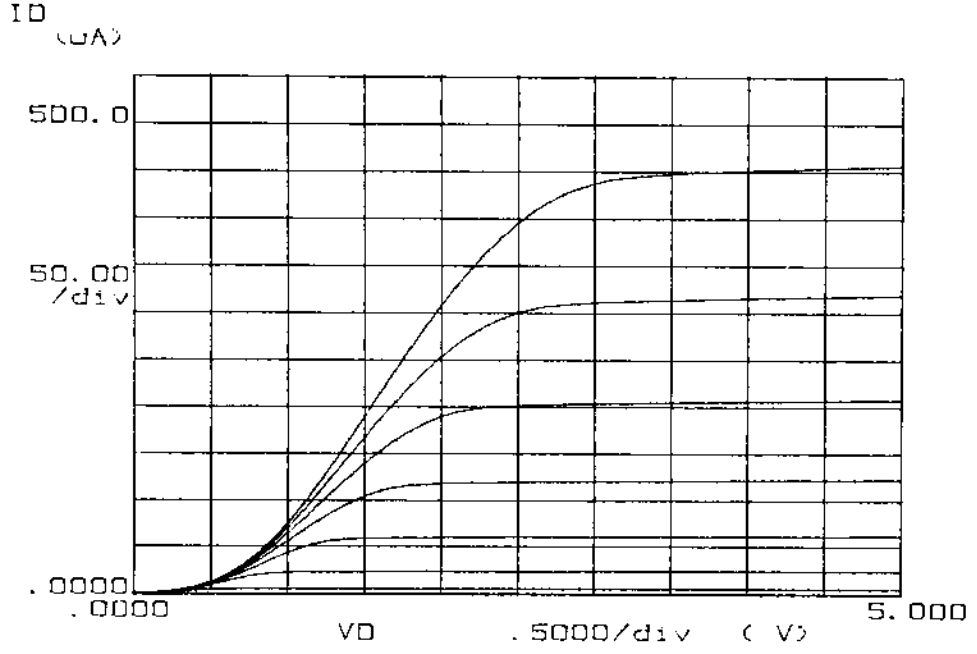
Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

Variable2:
VG -Ch2
Start .0000V
Stop 4.5000V
Step .5000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

NMOS 6/32 IDVD #04



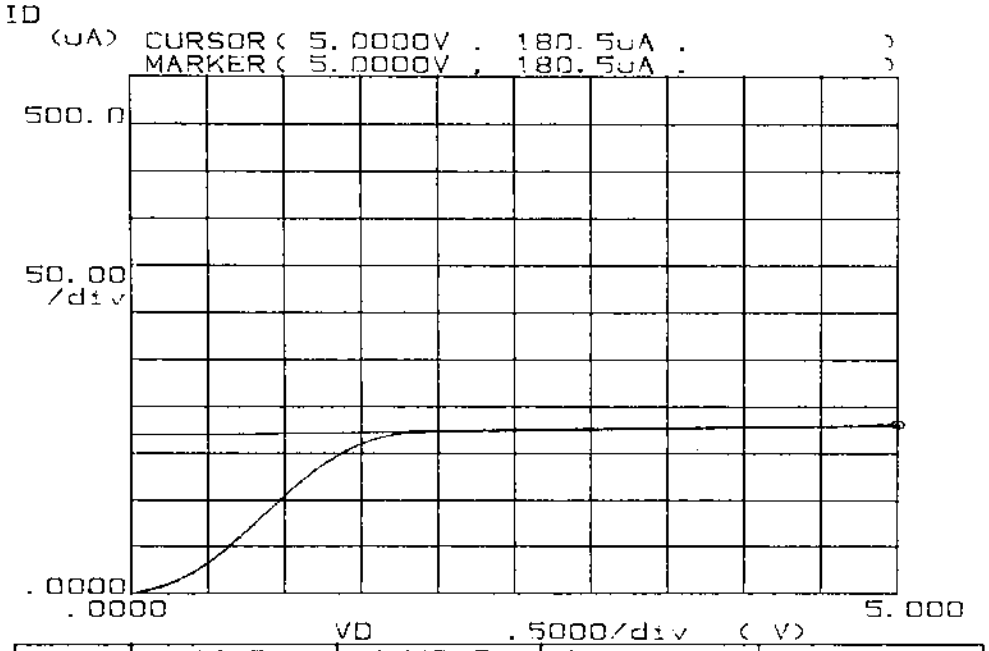
Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

Variable2:
VG -Ch2
Start .0000V
Stop 4.5000V
Step .5000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

NMOS 6/32 IDVD #04



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	2.25E-06	445E+03	-75.8E+00	169E-06
LINE2				

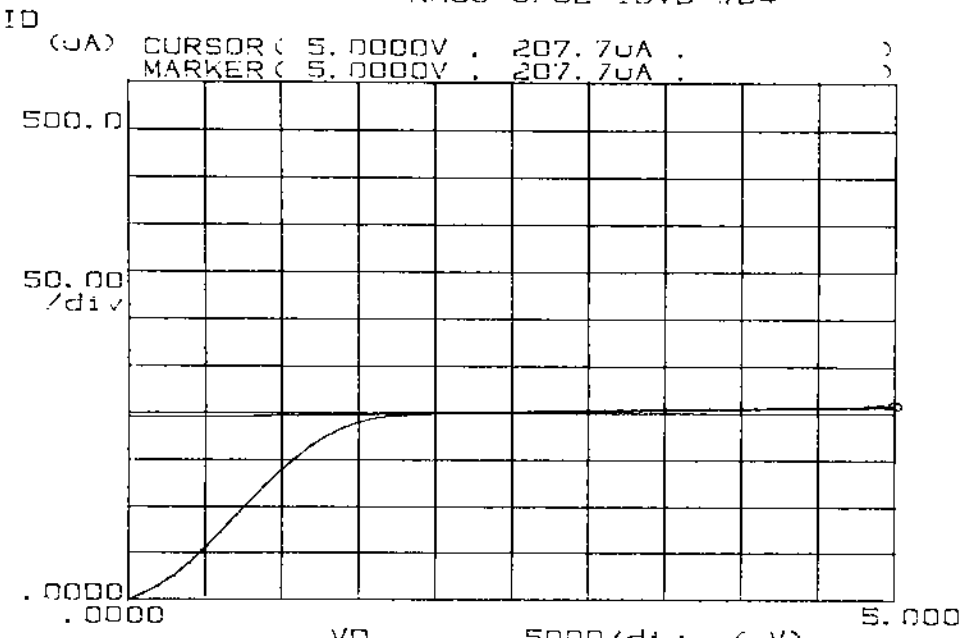
Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

Variable2:
VG -Ch2
Start 3.0000V
Stop 3.0000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

NMOS 6/32 IDVD #04



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	2.57E-06	389E+03	-75.9E+00	195E-06
LINE2				

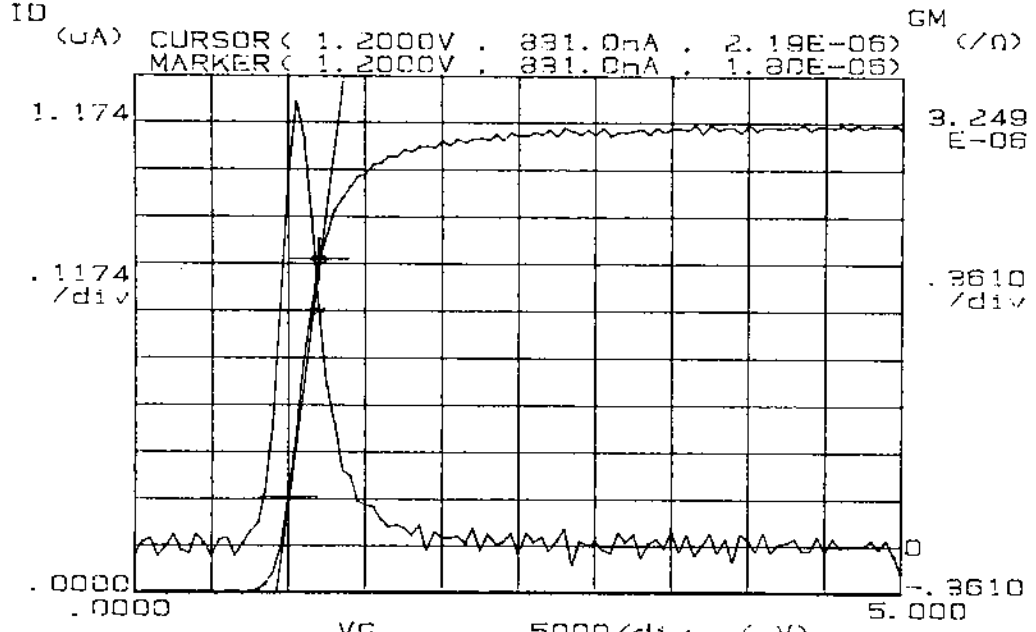
Variable1:
VD --Ch3
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

Variable2:
VG --Ch2
Start 3.0000V
Stop 3.0000V
Step .0000V

Constants:
VS --Ch1 .0000V
VB --Ch4 .0000V

****** GRAPHICS PLOT ******

NMOS 6/32 IDVG #D4



Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Variable2:
VD -Ch3
Start .1000V
Stop .1000V
Step -1.0000V

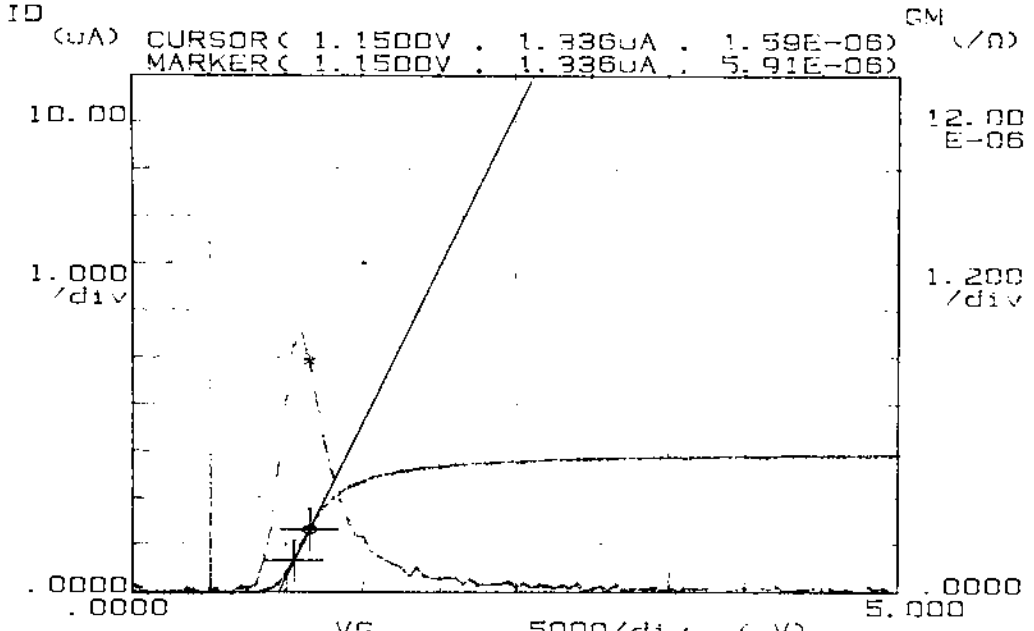
Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	2.96E-06	337E+03	920E-03	-2.73E-06
LINE2				

GM (/Ω) = AID/AVG
IDS (A) = FID

****** GRAPHICS PLOT ******

NMOS 6/32 IDVG #D4



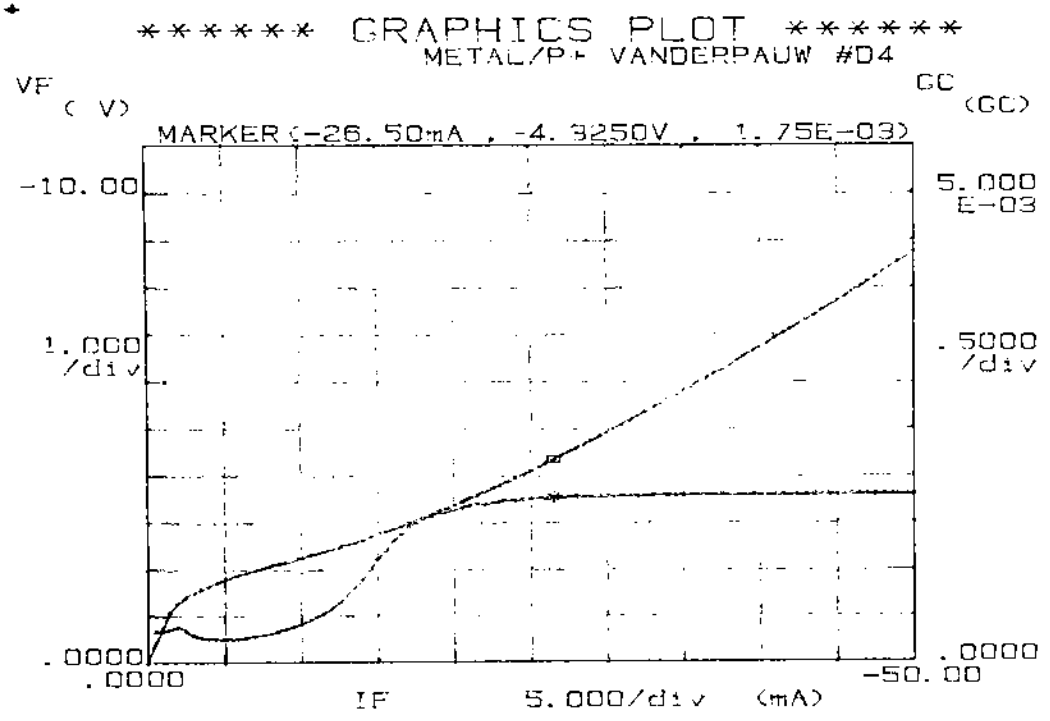
	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	6.58E-06	152E+03	947E-03	-6.23E-06
LINE2				

GM (/Ω) = AID/AVG
IDS (A) = AID

Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Variable2:
VD -Ch3
Start .1000V
Stop .1000V
Step -1.0000V

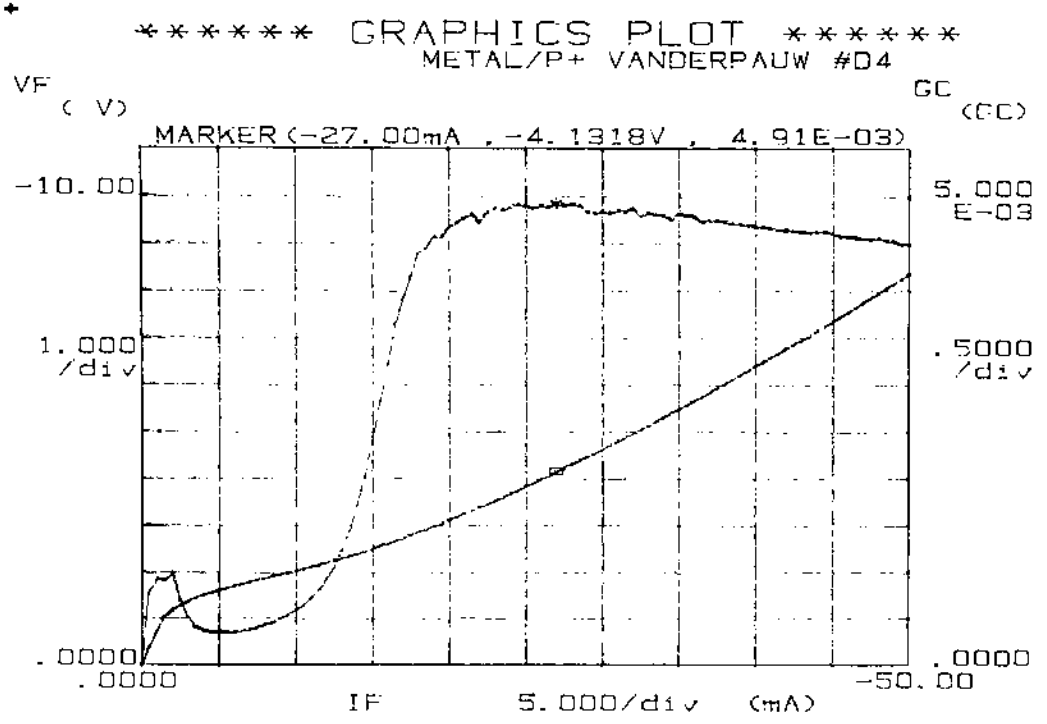
Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V



Variables:
IF -Ch1
Linear sweep
Start .000 A
Stop -50.00mA
Step -500.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

CC (GC) = IF/64./(V1-V2)
RS (RS) = (V1-V2)*4.532/IF



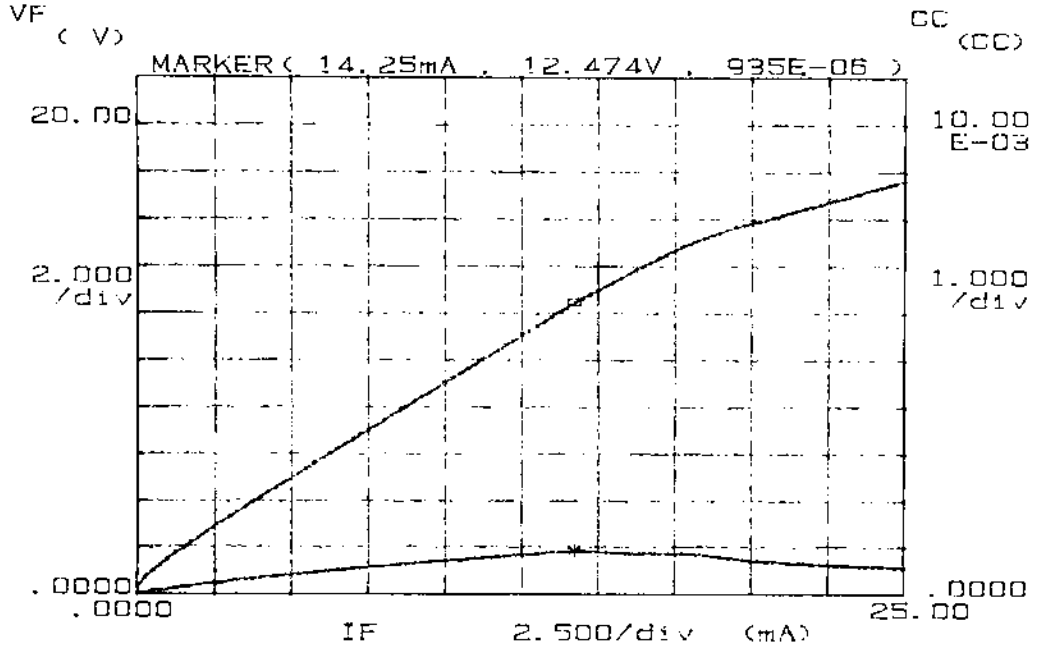
Variables:
IF -Ch1
Linear sweep
Start .000 A
Stop -50.00mA
Step -500.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .000CV
I2 -Ch4 .000 A

GC (GC) = IF/54/(V1-V2)
RS (RS) = (V1-V2)*4.532/IF

****** GRAPHICS PLOT ******

METAL/N+ CBKR #D4



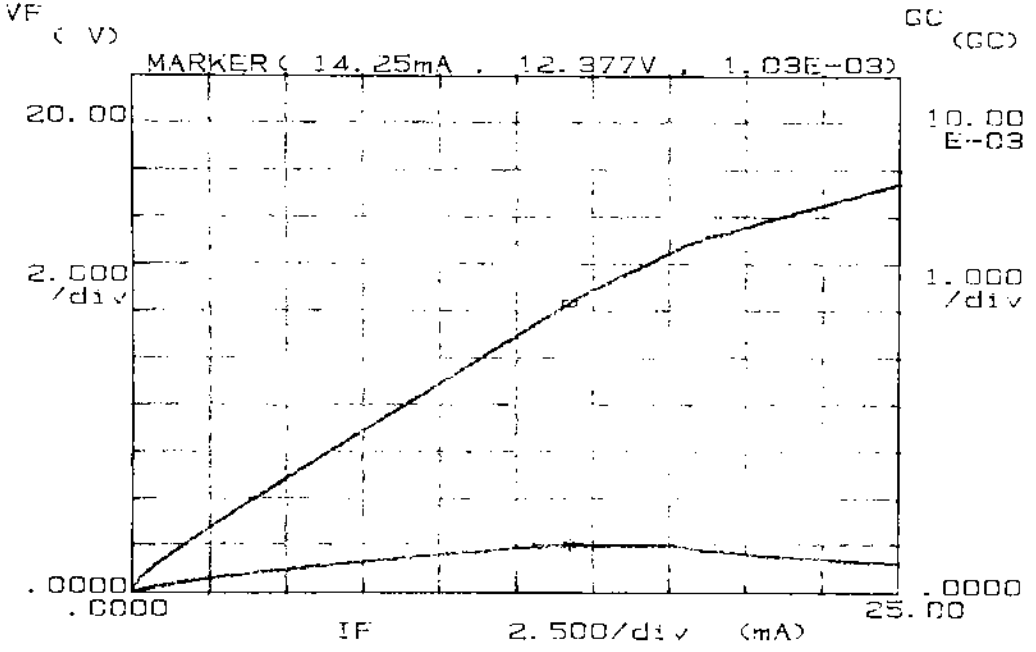
Variable1:
IF -Ch1
Linear sweep
Start .000 A
Stop 25.00mA
Step 250.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

GC (GC) = (IF/10)/(V1-V2)
RS (RS) = (V1-V2)*4.532/IF

****** GRAPHICS PLOT ******

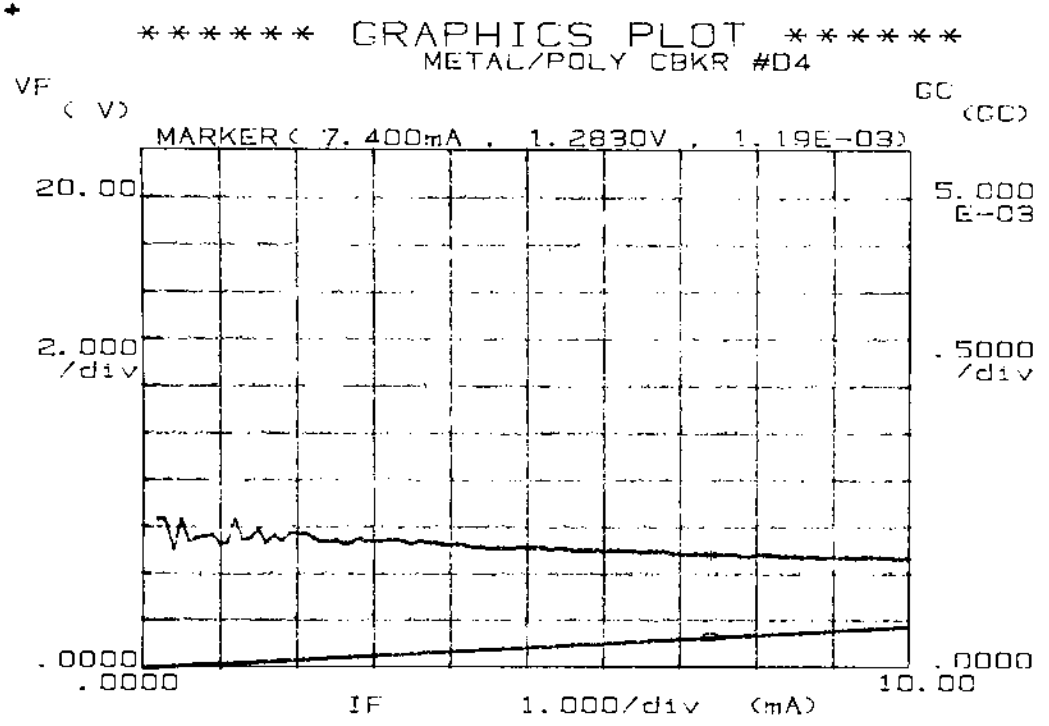
METAL/N+ CBKR #D4



Variable1:
IF -Ch1
Linear sweep
Start .000 A
Step 25.00mA
Stop 250.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

GC (GC) = (IF/1E)/(V1-V2)
RS (RS) = (V1-V2)*4.592/IF



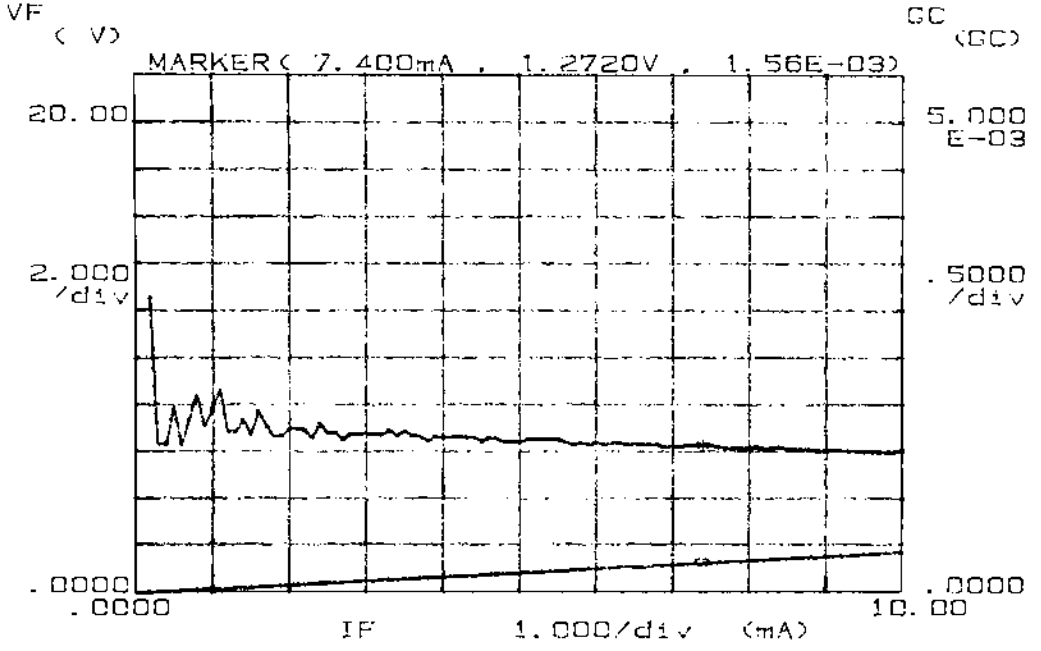
Variable1:
IF -Ch1
Linear sweep
Start .000 A
Stop 10.00mA
Step 100.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

GC (GC) = IF/84/(V1-V2)
RC (RC) = (V1-V2)/(IF*84)

****** GRAPHICS PLOT ******

METAL/POLY CBKR #D4



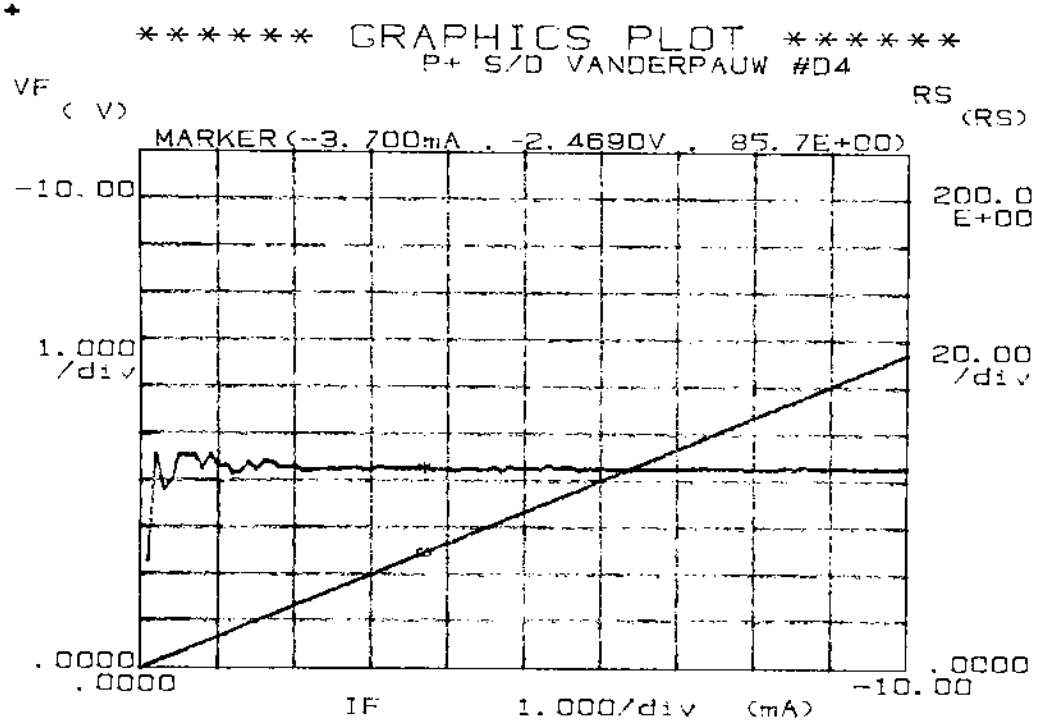
Variables:

IF	-Ch1	
Linear sweep		
Start		.000 A
Stop		10.00mA
Step		100.0uA

Constants:

I1	-Ch2	.000 A
V	-Ch3	.0000V
I2	-Ch4	.000 A

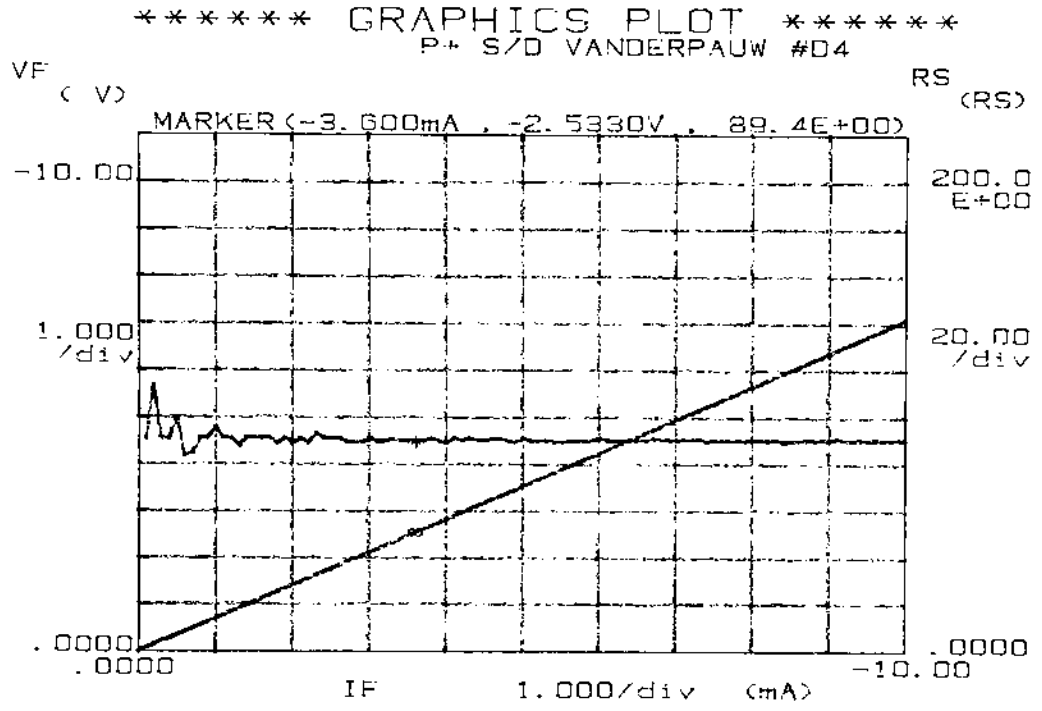
GC (GC) = IF/84/(V1-V2)
RS (RS) = (V1-V2)*4.532/IF



Variables:
IF -Ch1
Linear sweep
Start .000 A
Stop -10.00mA
Step -100.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

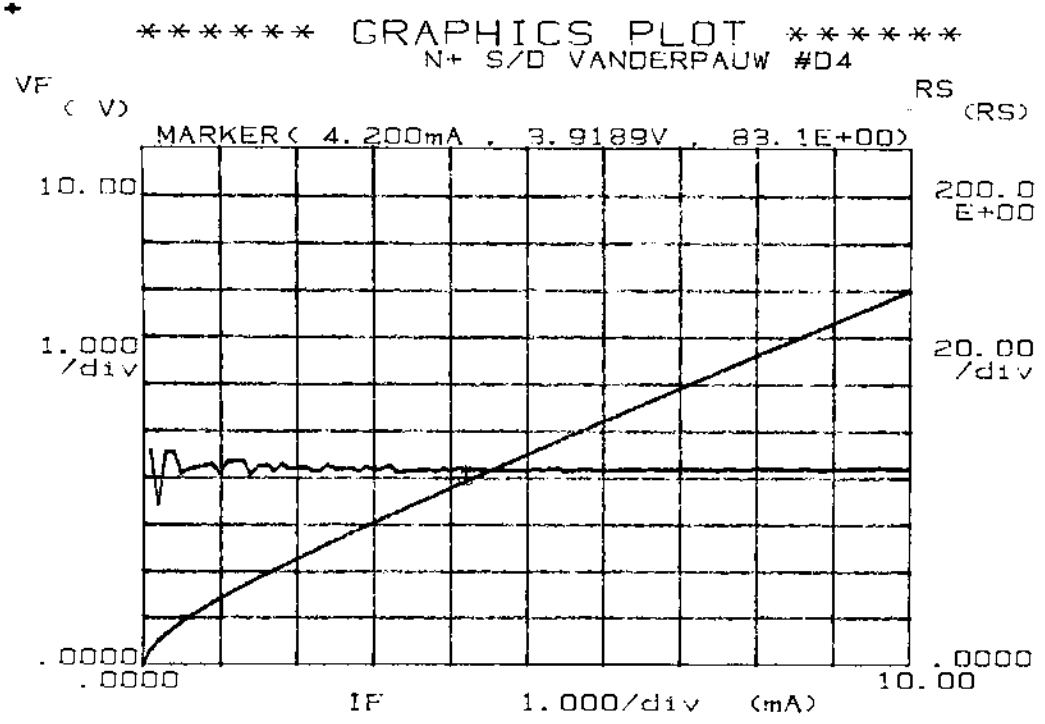
RC (RC) = (V2-V1)/IF
RS (RS) = (V1-V2)*4.532/IF



Variable1:
IF -Ch1
Linear sweep
Start .000 A
Step -10.00mA
Step -100.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V1-V2)*4.532/IF



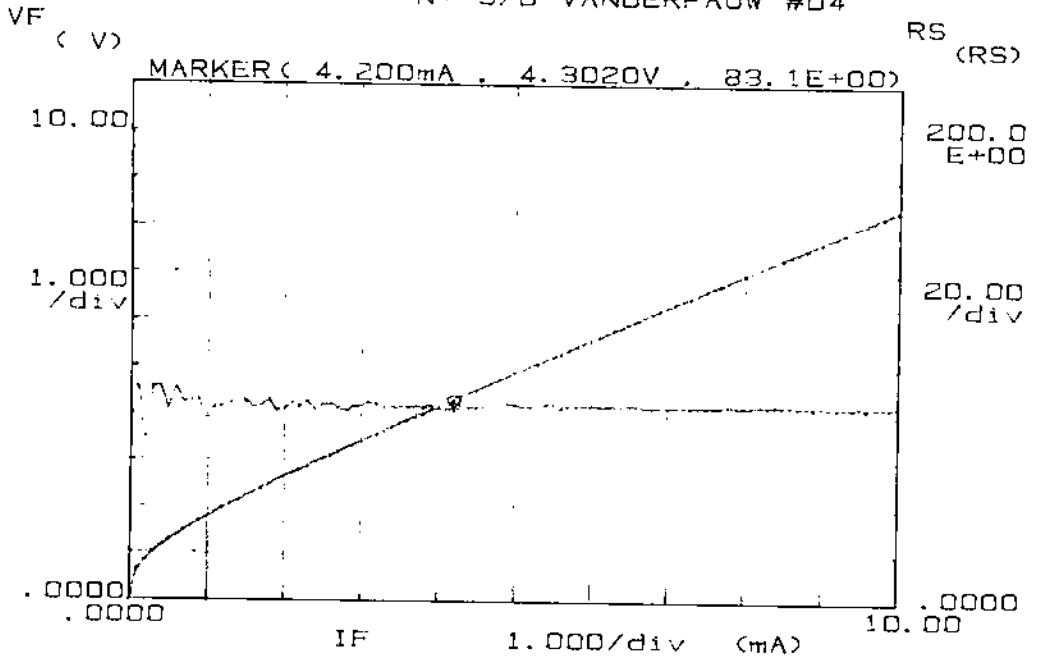
Variables:
IF ->Ch1
Linear sweep
Start .000 A
Stop 10.00mA
Step 100.0uA

Constantes
I1 ->Ch2 .000 A
V ->Ch3 .0000V
I2 ->Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

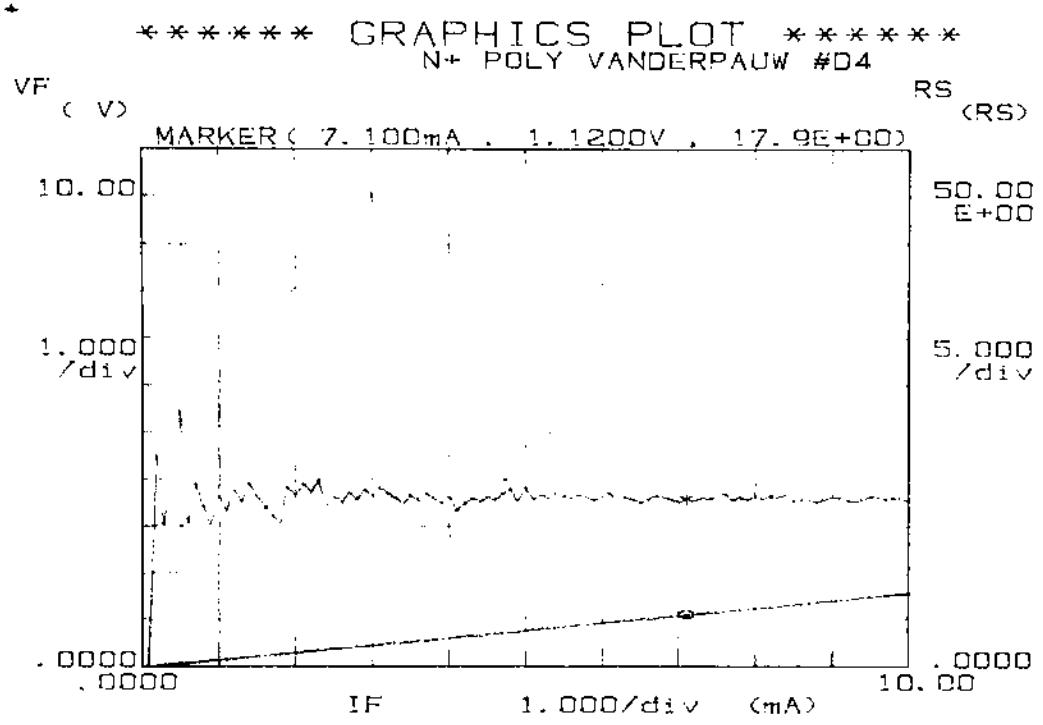
N+ S/D VANDERPAUW #04



Variable1:
IF -Ch1
Linear sweep
Start .000 A
Step 10.00mA
Stop 100.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

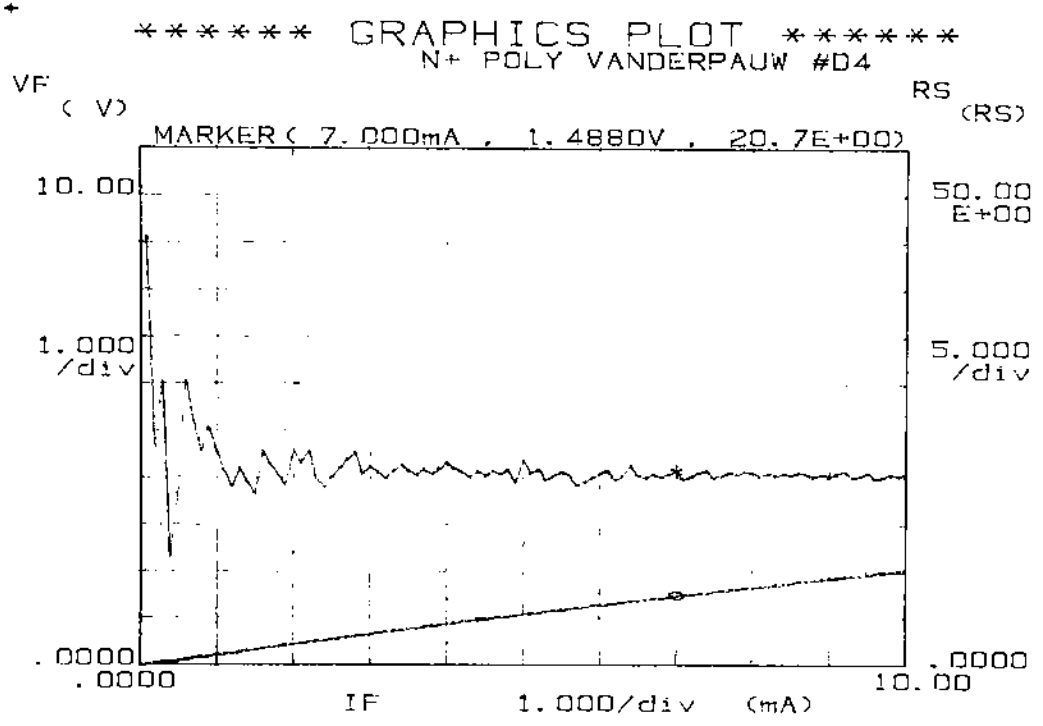
RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF



Variable1:
IF -Ch1
Linear sweep
Start .000 A
Step 10.00mA
Step 100.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/I



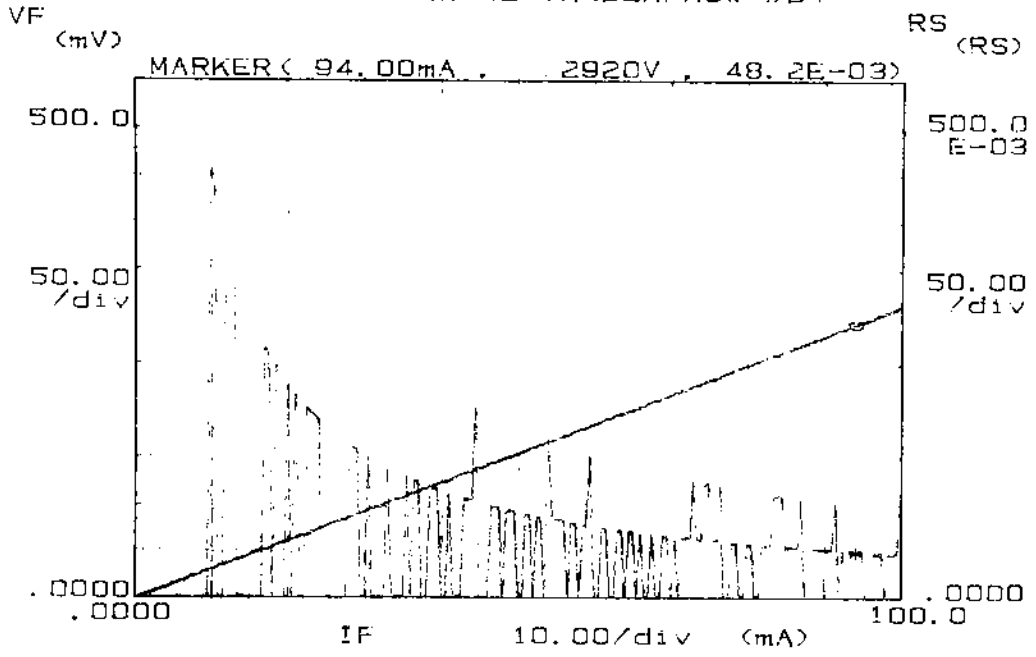
Variables:
IF -Ch1
Linear sweep
Start .000 A
Step 10.00mA
Stop 100.0mA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

METAL VANDERPAUW #D4



Variables:

IF	--Ch1	
Linear sweep		
Start		.000 A
Stop		100.0mA
Step		500.0uA

Constants:

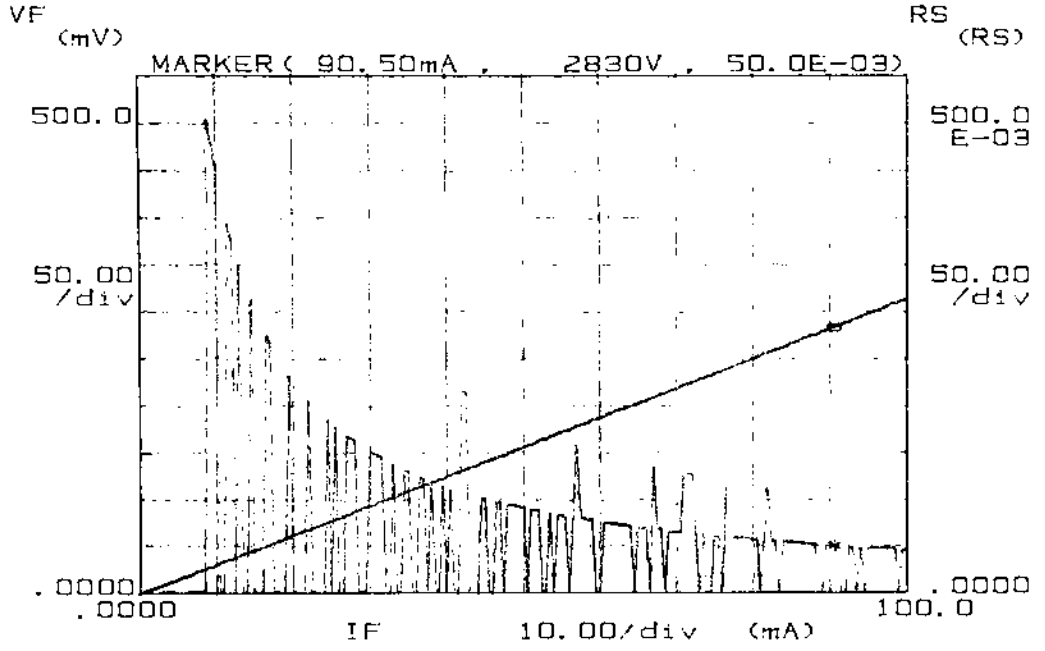
I1	--Ch2	.000 A
V	--Ch3	.0000V
I2	--Ch4	.000 A

RC (RC) = (V2-V1)/IF

RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

METAL VANDERPAUW #04



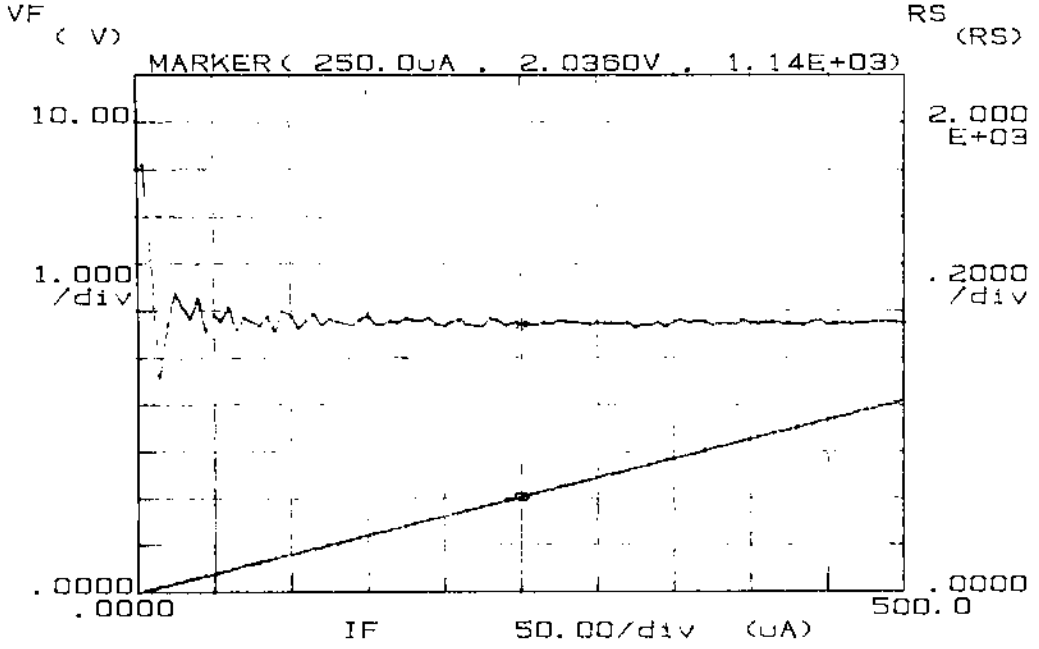
Variables:
IF -Ch1
Linear sweep
Start .000 A
Stop 100.0mA
Step 500.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

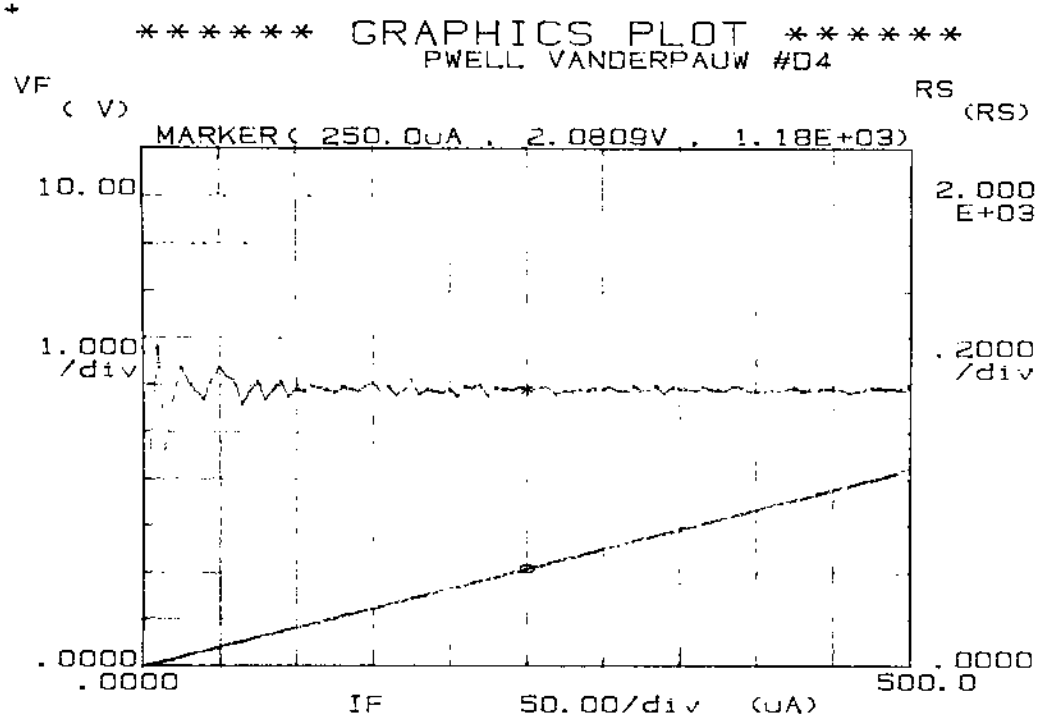
PWELL VANDERPAUW #04



Variable1:
IF -Ch1
Linear sweep
Start .000 A
Stop 500.0uA
Step 5.000uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

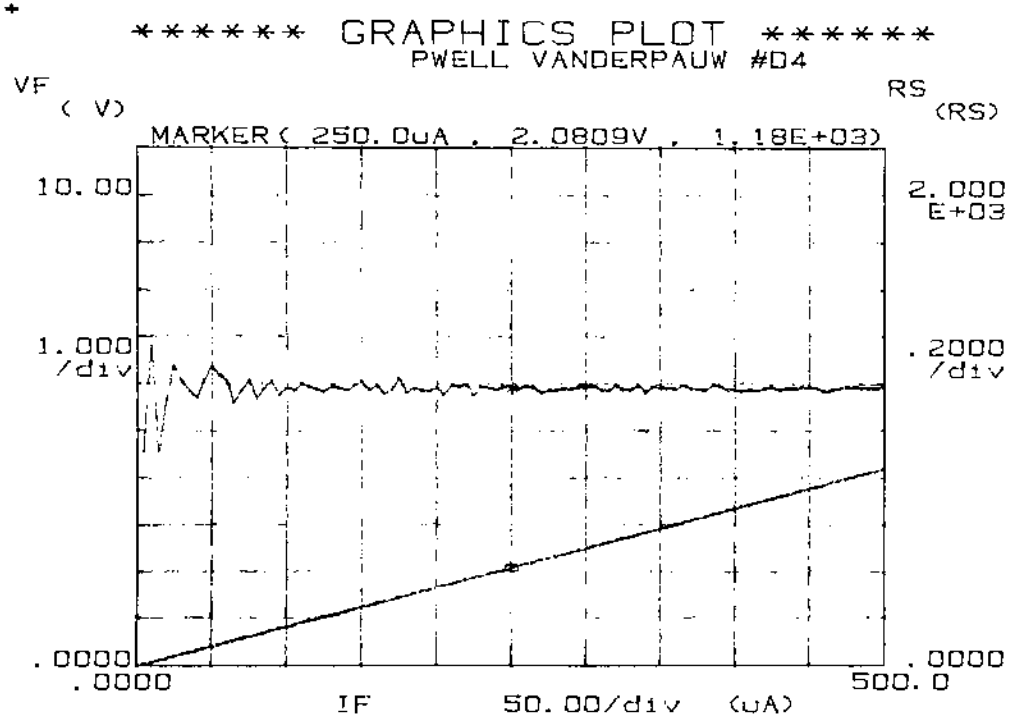
RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF



Variable1:
IF -Ch1
Linear sweep
Start .000 A
Step 500.0uA
Step 3.000uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF



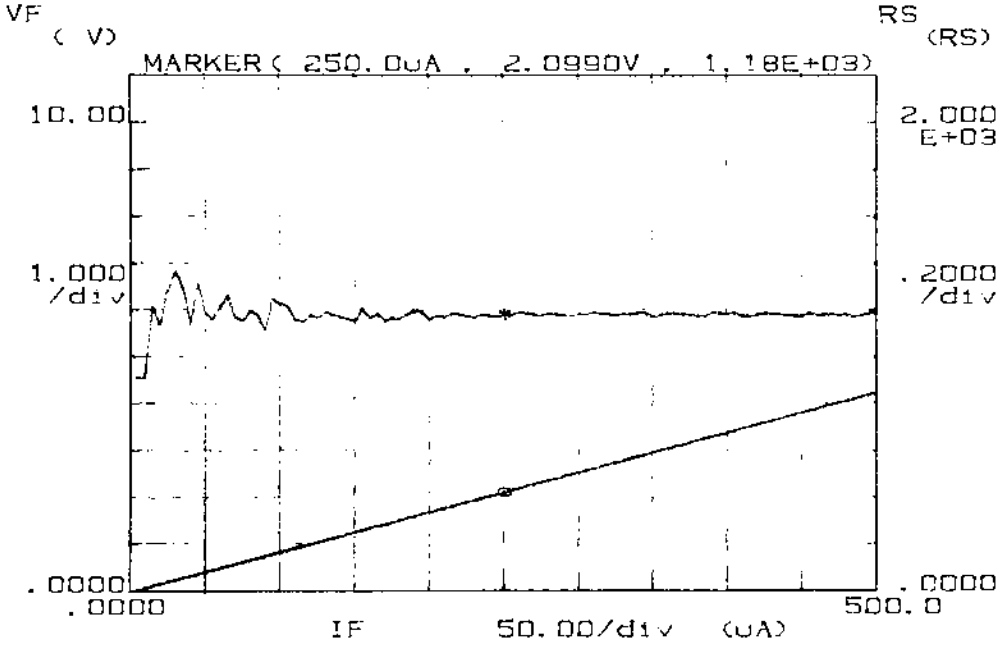
Variable1:
IF -Ch1
Linear sweep
Start .000 A
Stop 500.0uA
Step 5.000uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

P-WELL VANDERPAUW #D4

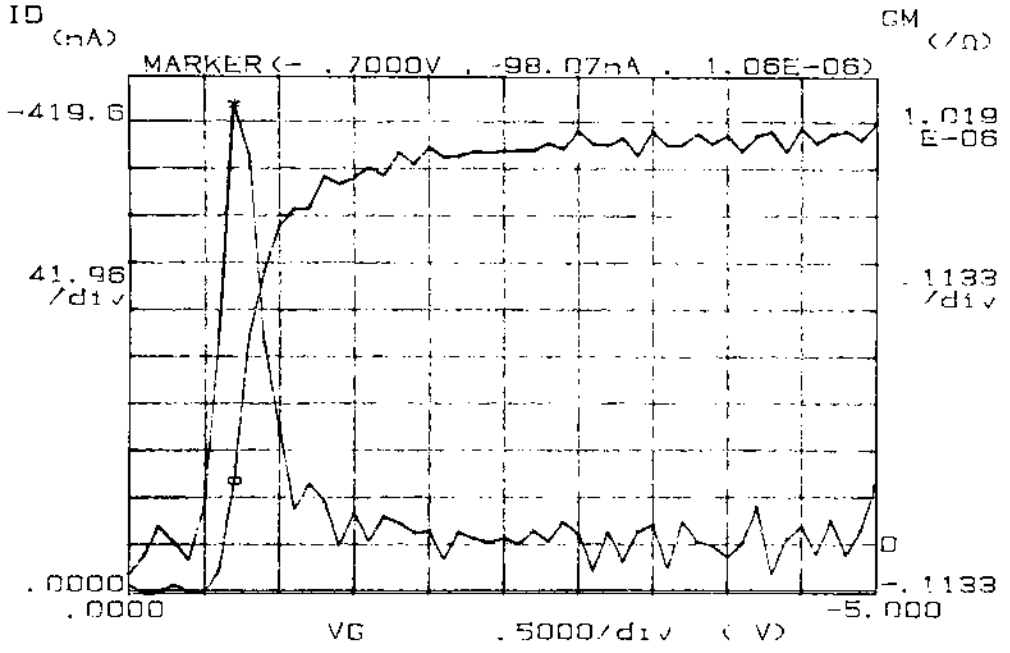


Variables:
IF -Ch1
Linear sweep
Start .000 A
Stop 500.0uA
Step 5.000uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******



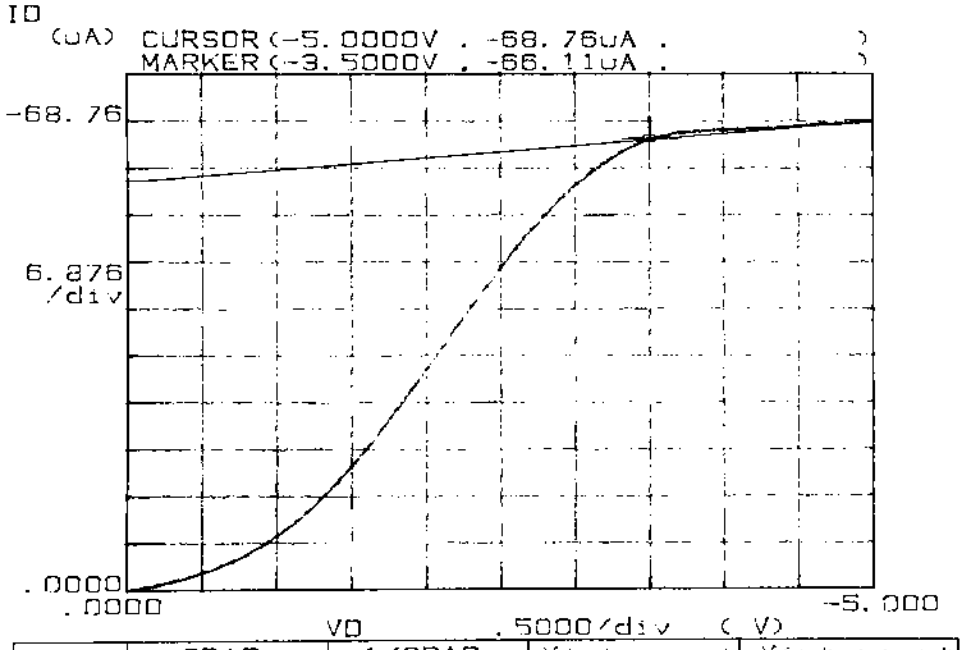
Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop -5.0000V
Step - .1000V

Variable2:
VD -Ch3
Start - .1000V
Step - .1000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

GM (/Ω) = ΔID/ΔVG
IDS (A) = ID

****** GRAPHICS PLOT ******



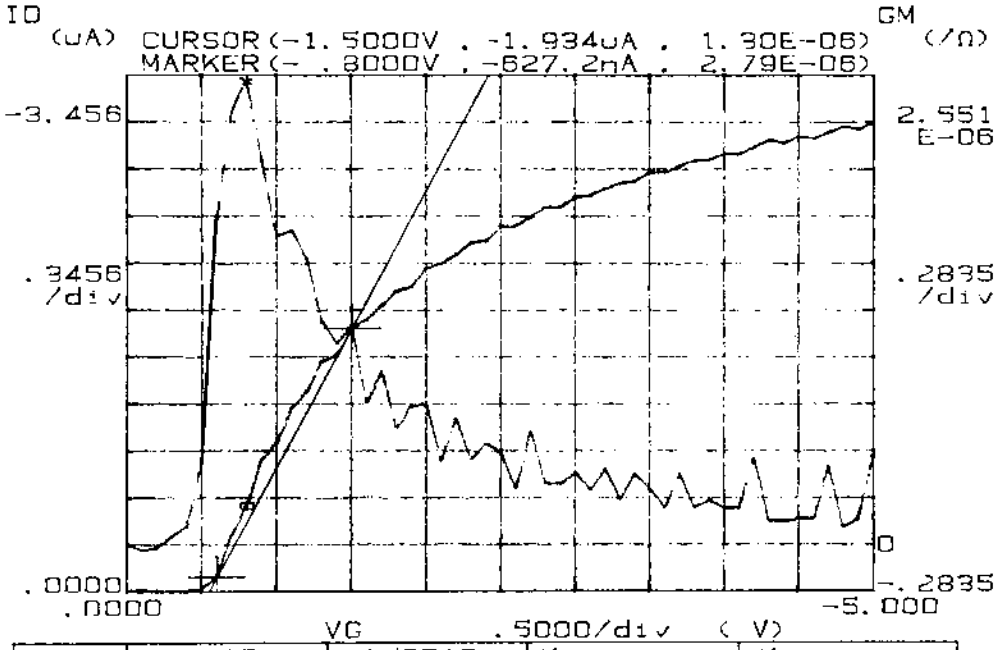
	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	1.77E-06	566E+03	33.9E+00	-59.9E-06
LINE2				

Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step -.1000V

Variable2:
VG -Ch2
Start -3.0000V
Stop -3.0000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	2.03E-06	492E+03	-549E-03	1.12E-06
LINE2				

GM (/Ω) = ΔID/ΔVG
IDS (ΓA) = ΓID

Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop -5.0000V
Step -.1000V

Variable2:
VD -Ch3
Start -.1000V
Stop -.1000V
Step .0000V

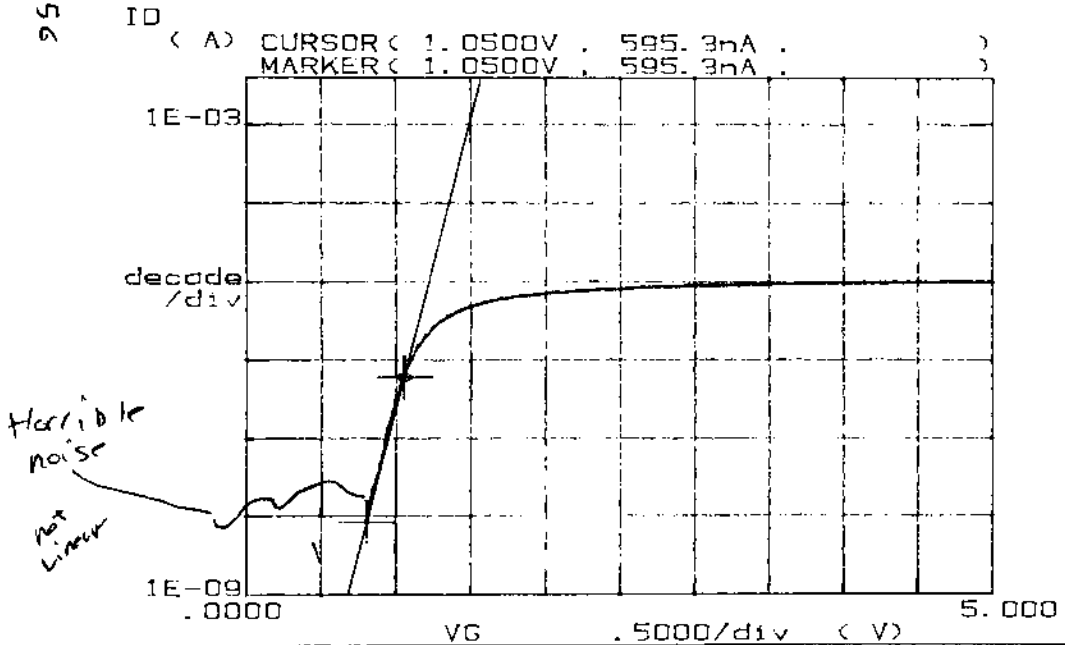
Constants:
VB -Ch1 .0000V
VB -Ch4 .0000V

wafer #151
pos #5
NMOS SubVT
C/32

P-56

****** GRAPHICS PLOT ******

NMOS SUBVT ~~D5 C792 #050721~~



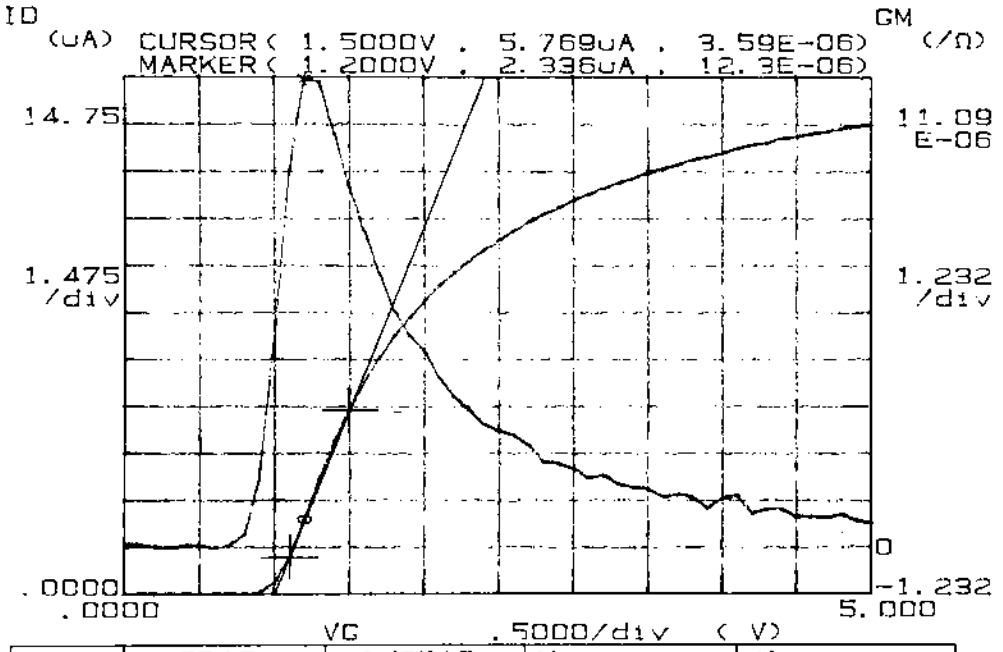
Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Constants:
VS -Ch1 .0000V
VD -Ch3 .1000V
VB -Ch4 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	7.41E+00	135E-03	1.89E+00	9.87E-15
LINE2				

****** GRAPHICS PLOT ******

NMOS 6/32 [redacted]



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	11.6E-06	86.5E+03	1.00E+00	-11.6E-06
LINE2				

GM (/Ω) = AID/AVG
IDS (A) = ∫ID

Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

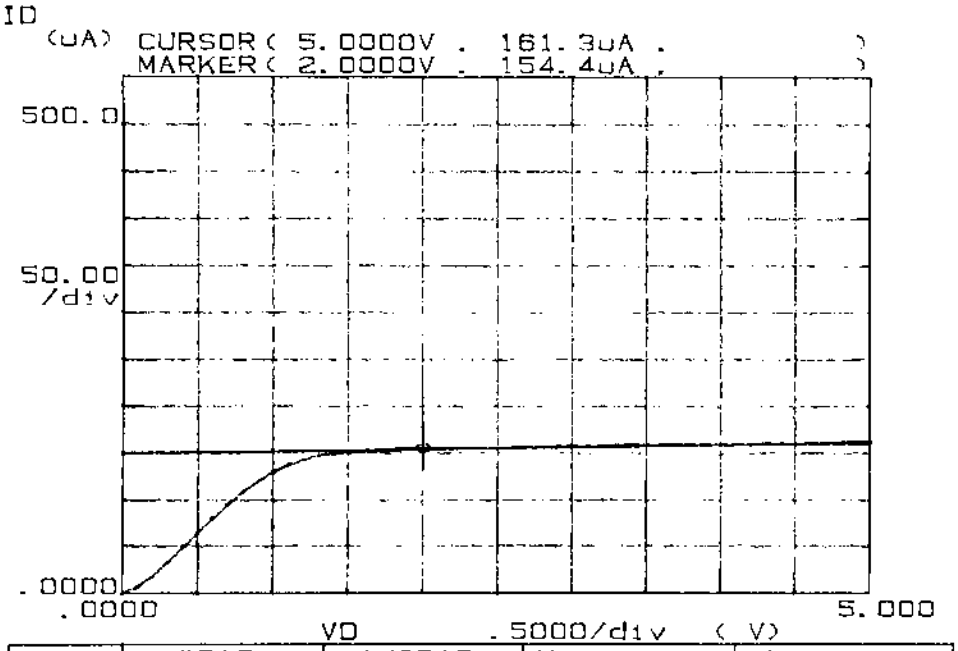
Variable2:
VD -Ch3
Start .1000V
Stop .1000V
Step -1.0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

wafer #D11

****** GRAPHICS PLOT ******

NMOS 16/32 [redacted]



Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

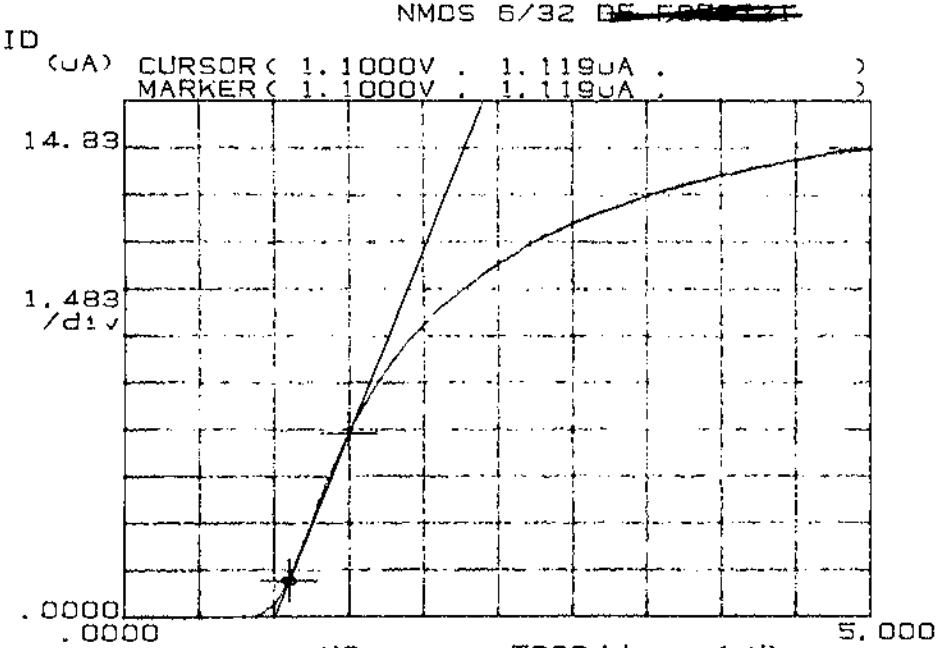
Variable2:
VG -Ch2
Start 3.0000V
Stop 3.0000V
Step .0000V

Constants:
VB -Ch1 .0000V
VB -Ch4 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	2.33E-06	429E+03	-64.2E+00	150E-06
LINE2				

wafer D11
pos #1

****** GRAPHICS PLOT ******
NMOS 6/32 [redacted]



Variable1:
VG ~Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

Variable2:
VD ~Ch3
Start .1000V
Stop .1000V
Step -1.0000V

Constants:
VS ~Ch1 .0000V
VB ~Ch4 .0000V

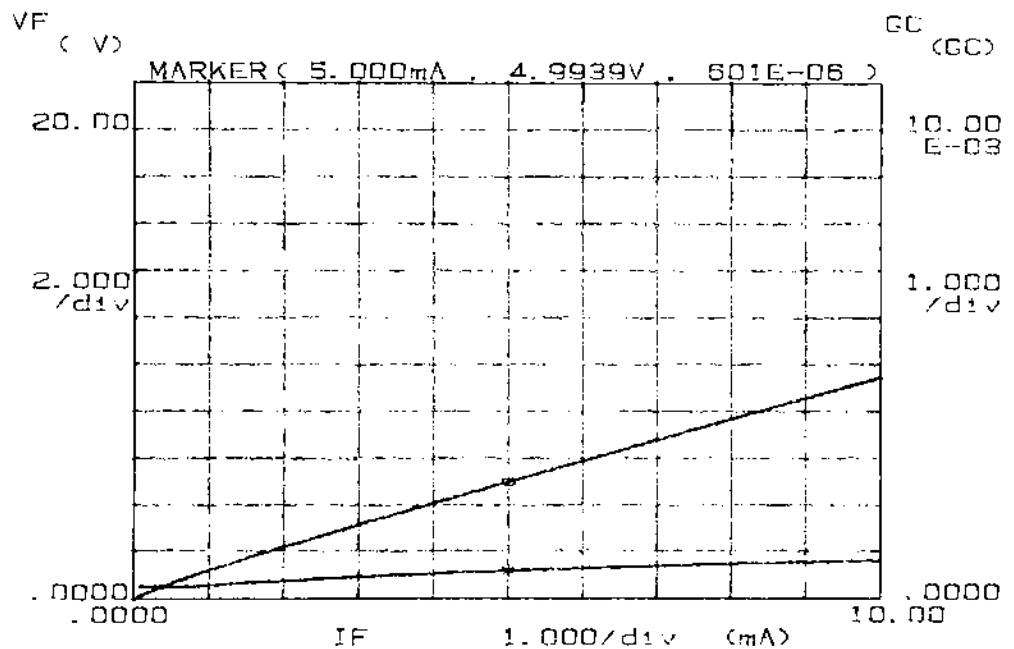
	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	11.7E-06	85.7E+03	1.00E+00	-11.7E-06
LINE2				

GM (/Ω) = AID/AVG
IDS (A) = FID

Pos 2
NCDIFF

Fig 6

****** GRAPHICS PLOT ******



Variables:
IF -Ch1
Linear sweep
Start .000 A
Stop 10.00mA
Step 100.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

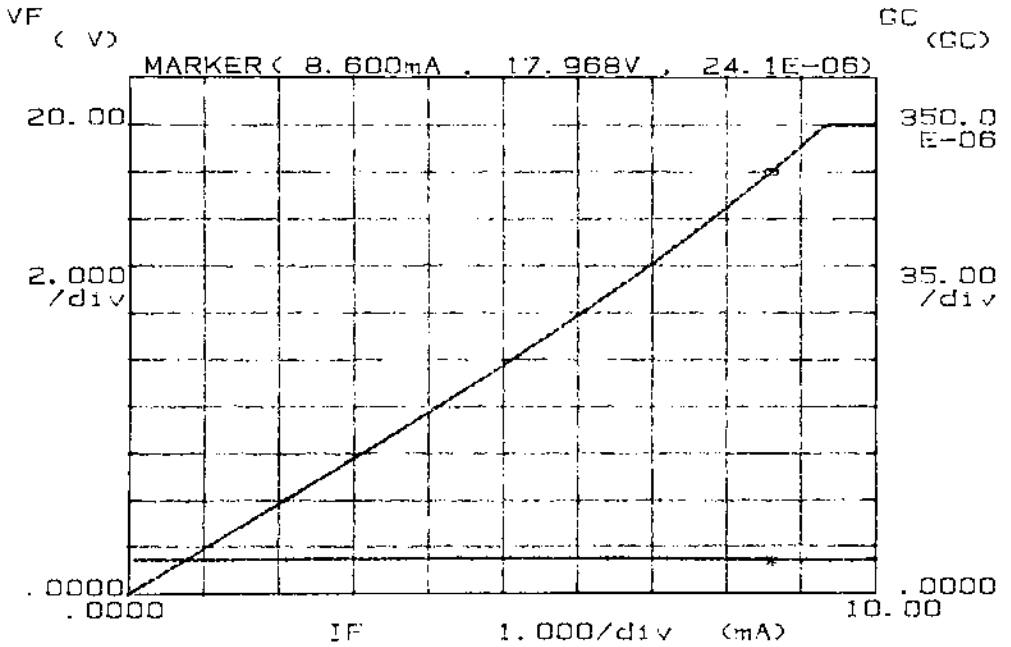
GC (GC) = IF/10/(V1-V2)
RS (RS) = (V1-V2)*4.932/IF

P'CB/FR

Pos #1

P61

****** GRAPHICS PLOT ******

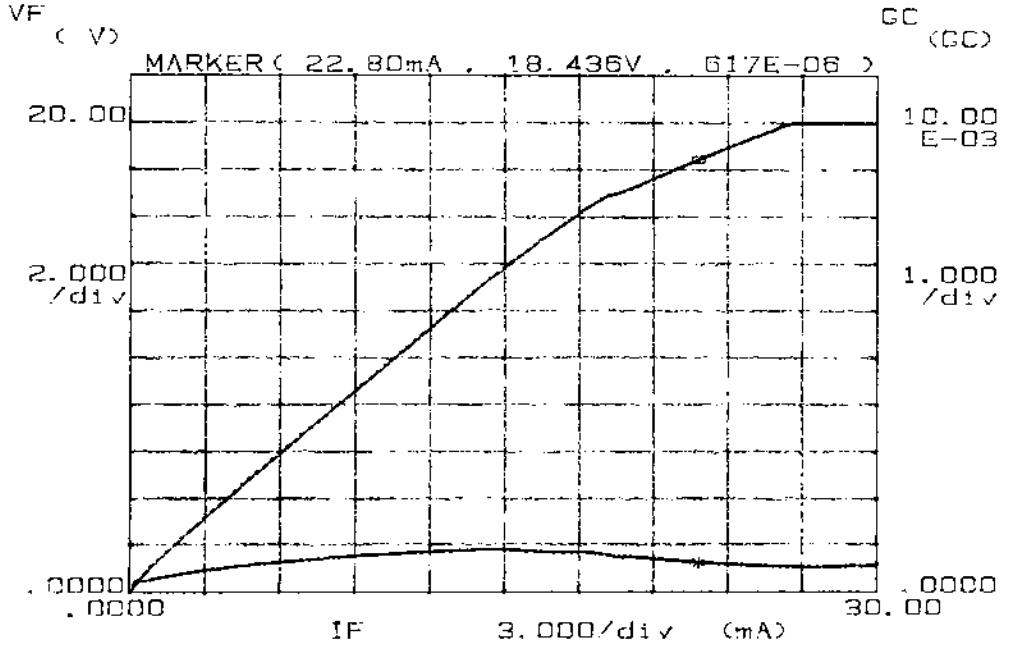


Variable1:
IF -Ch1
Linear sweep
Start .000 A
Stop 10.00mA
Step 100.0uA

Constants:
I1 -Ch2 .000 A
V --Ch3 .0000V
I2 -Ch4 .000 A

GC (GC) = IF/64/(V1-V2)
RS (RS) = (V1-V2)*4.532/IF

****** GRAPHICS PLOT ******

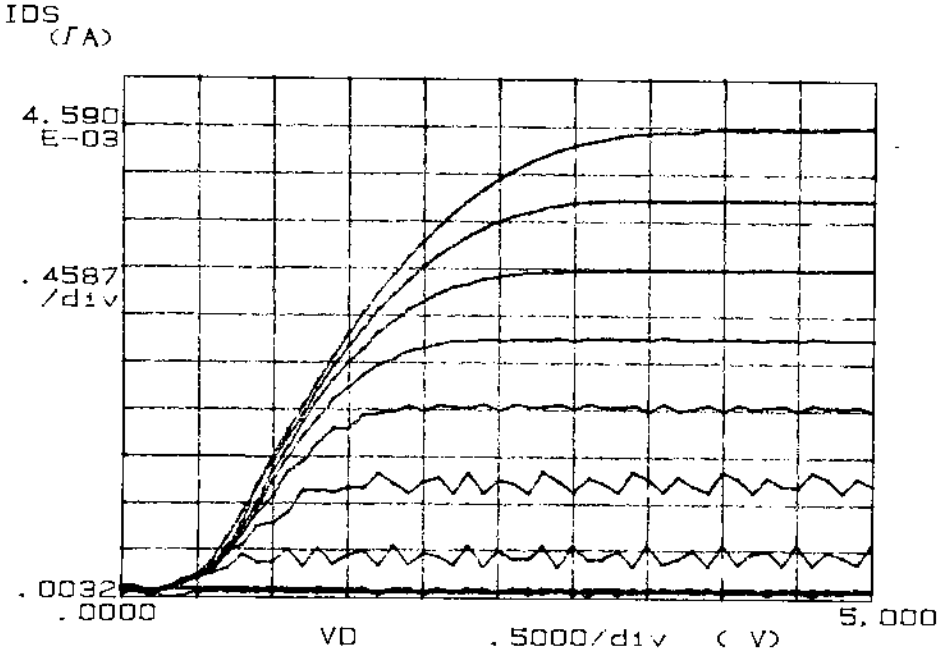


Variables:
IF -Ch1
Linear sweep
Start .000 A
Step 30.00mA
Step 300.0uA

Constantes:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

GC (GC) = IF/18/(V1-V2)
RS (RS) = (V1-V2)*4.532/IF

****** GRAPHICS PLOT ******

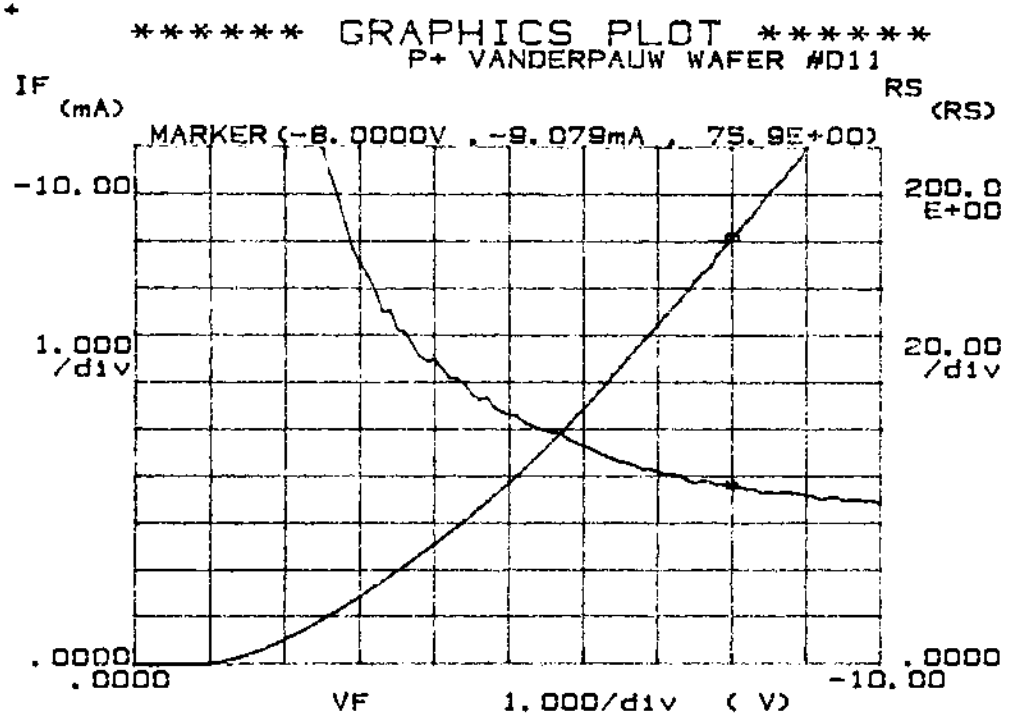


Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

Variable2:
VG -Ch2
Start .0000V
Stop 4.5000V
Step .5000V

Constants:
VS -Ch1 .0000V

GM (/Ω) = AID/AVG
IDS (/A) = /ID



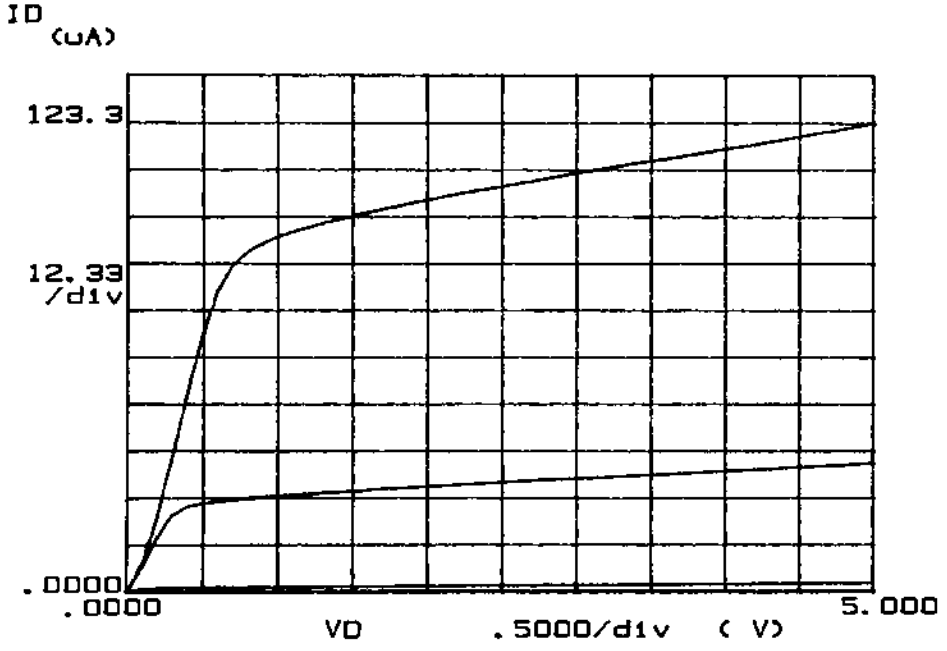
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -10.000V
Step - .1000V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V1-V2)*4.532/IF

****** GRAPHICS PLOT ******

NMOS 2/32 IDVD #D11



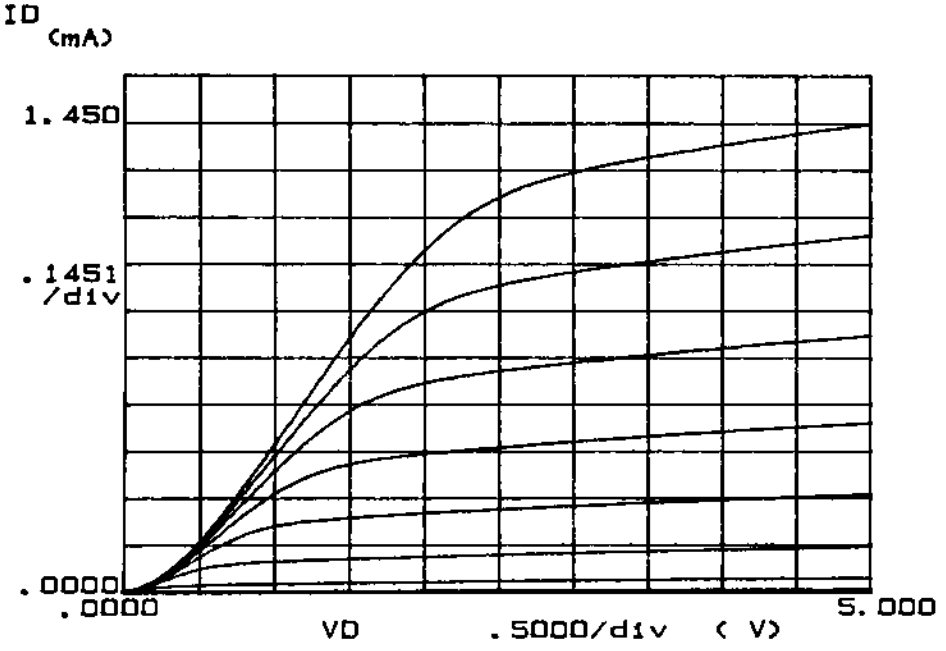
Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

Variable2:
VG -Ch2
Start .0000V
Stop 2.0000V
Step .5000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

NMOS 2/32 IDVD #D11



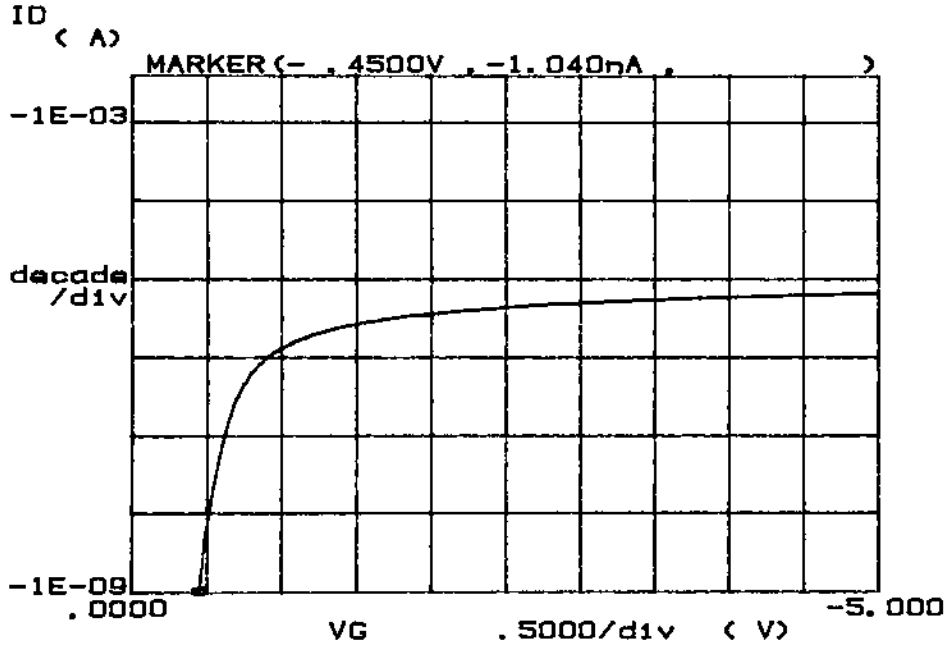
Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

Variable2:
VG -Ch2
Start .0000V
Stop 4.5000V
Step .5000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

PMOS 16/32 SUBVT #D6



Variable1:
VG -Ch2
Linear sweep
Start .0000V
Step -5.0000V
Step -.0500V

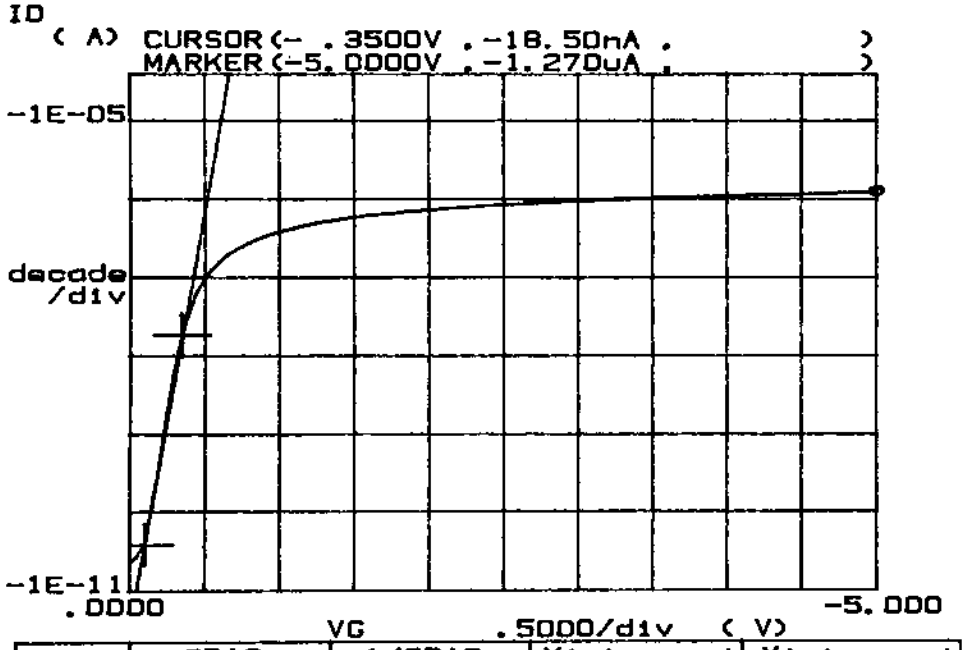
Variable2:
VD -Ch3
Start -.1000V
Step -.1000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

SUBVT (mV) = ΔVG/(LOG((ΔID+2)+ID)-LOG(ID))

****** GRAPHICS PLOT ******

PDLY2 PMOS 16/32 SUBVT #03



Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop -5.0000V
Step - .0500V

Variable2:
VD -Ch2
Start - .1000V
Step - .1000V
Step .0000V

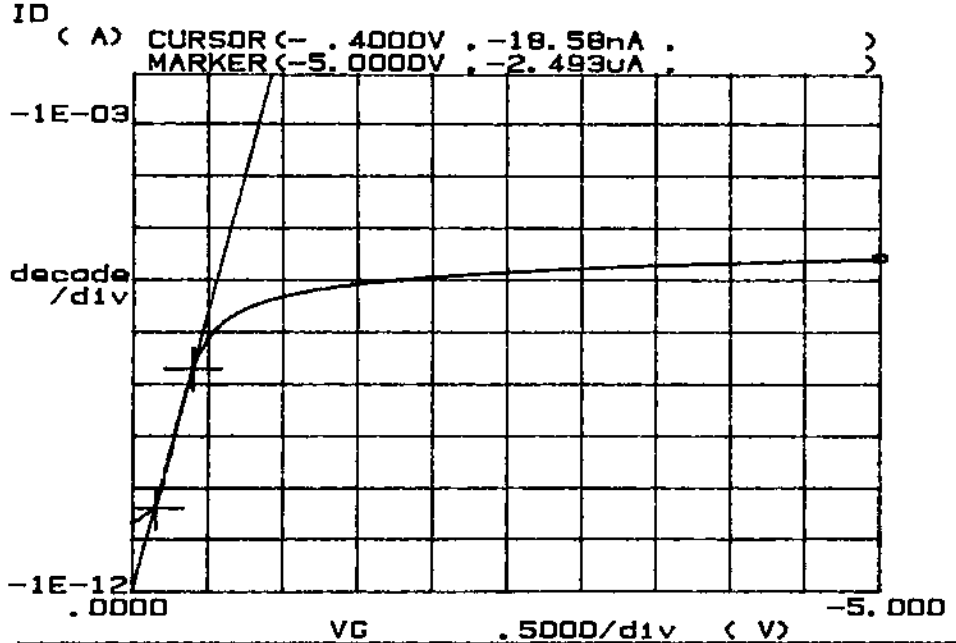
Constants:
VB -Ch1 .0000V
VB -Ch4 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-10.7E+00	-93.4E-03	-1.07E+00	-3.32E-12
LINE2				

SUBVT (mV) = ΔVG/(LOG((ΔID+2)+ID)-LOG(ID))

****** GRAPHICS PLOT ******

POLY2 PMOS 16/32 #03



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-10.7E+00	-93.7E-03	-1.12E+00	-1.00E-12
LINE2				

SUBVT (mV) = AVG/(LOG((AID*2)+ID)-LOG(ID))

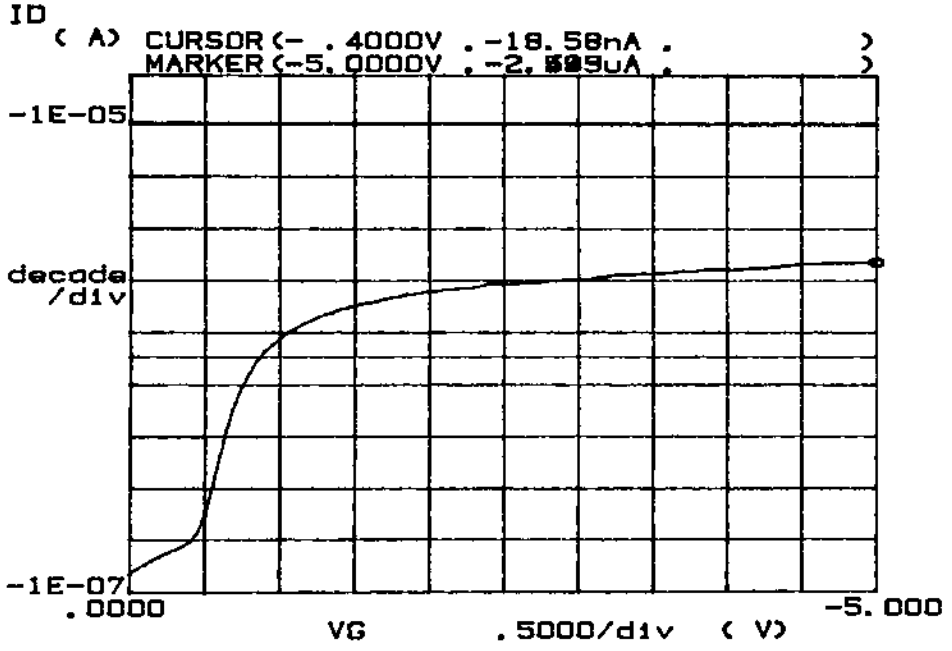
Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop -5.0000V
Step - .0500V

Variable2:
VD -Ch3
Start - .1000V
Stop - .1000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

PMOS 16/32 SUBVT #D3



Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop -5.0000V
Step - .0500V

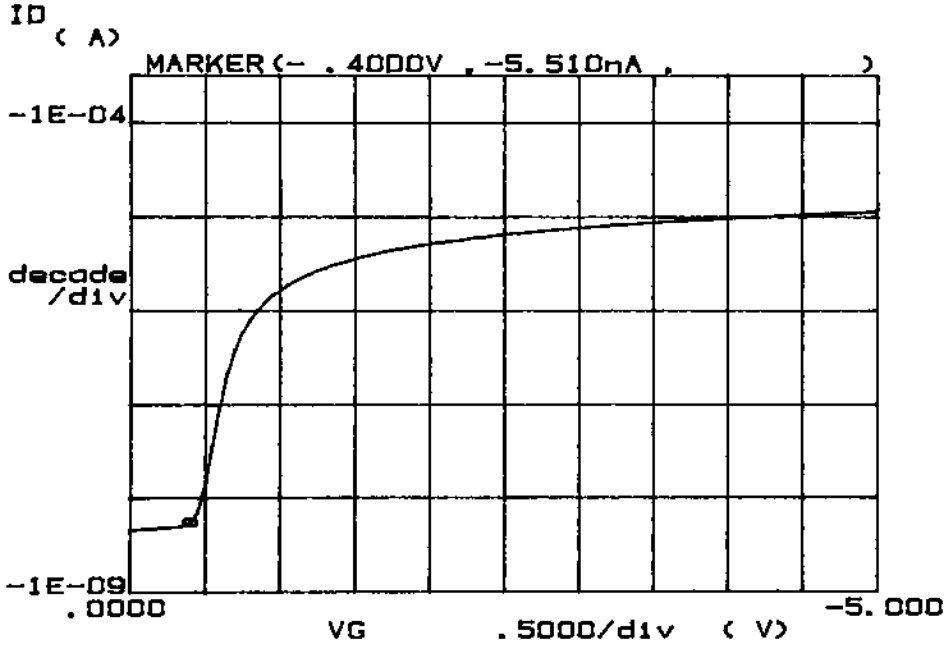
Variable2:
VD -Ch3
Start - .1000V
Stop - .1000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

SUBVT (mV) = ΔVG/(LOG((ΔID÷2)÷ID)-LOG(ID))

****** GRAPHICS PLOT ******

PMOS 16/32 SUBVT #D3



Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop -5.0000V
Step - .0500V

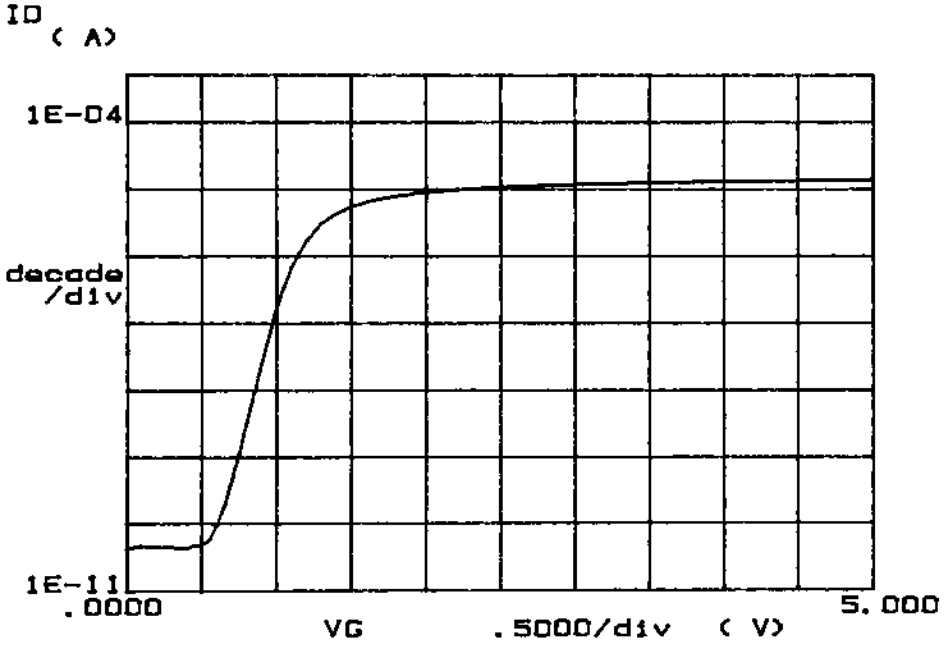
Variable2:
VD -Ch3
Start - .1000V
Stop - .1000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

SUBVT (mV) = AVG/(LOG((ΔID*2)÷ID)-LOG(ID))

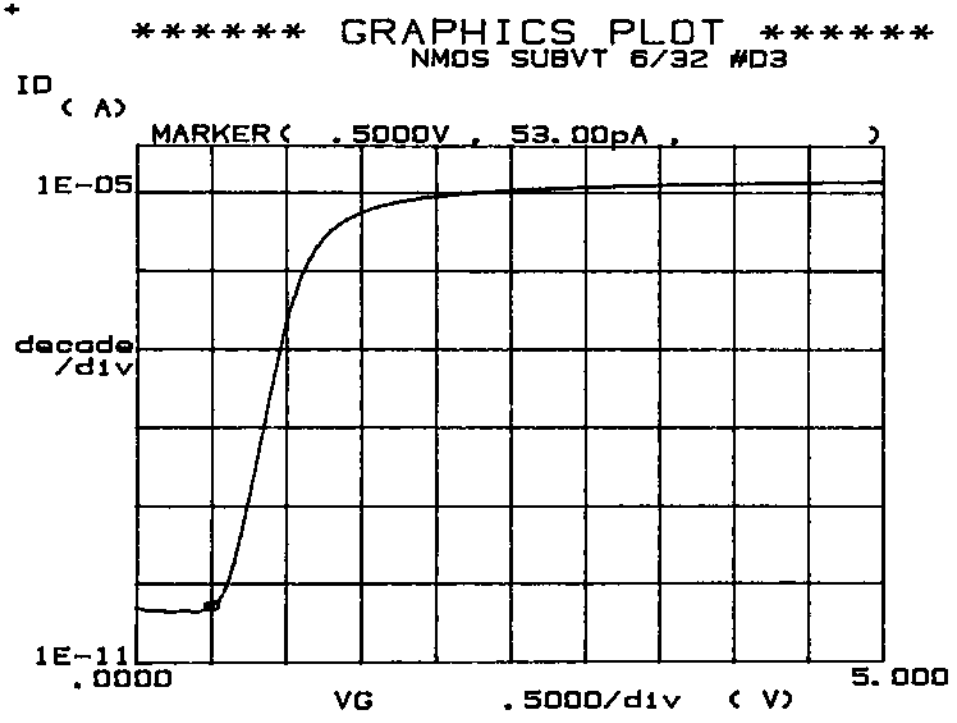
****** GRAPHICS PLOT ******

NMOS SUBVT 6/32 #03



Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Constants:
VS -Ch1 .0000V
VD -Ch3 .1000V
VB -Ch4 .0000V

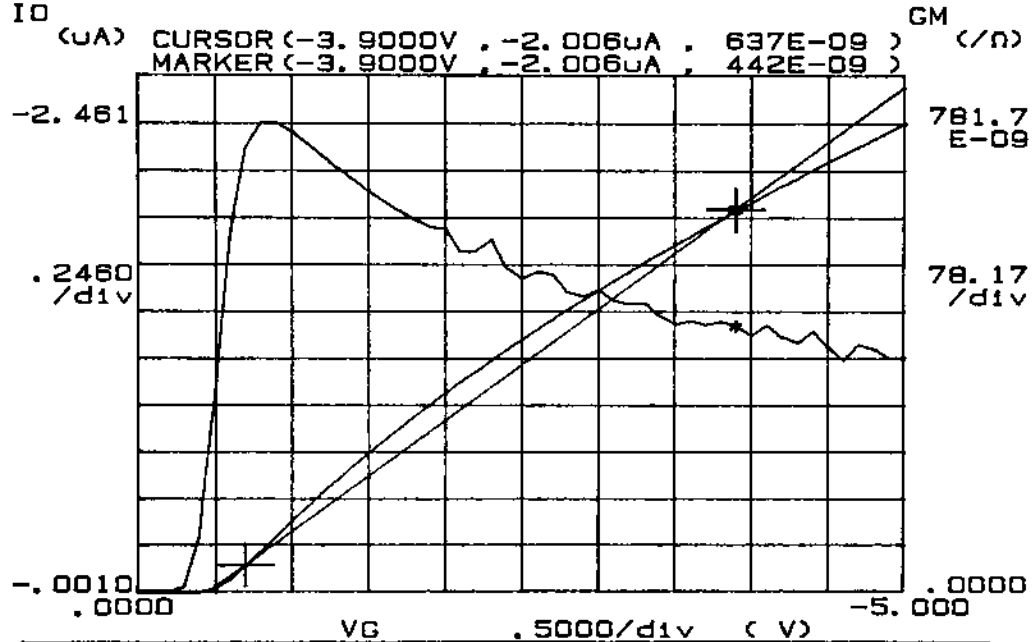


Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Constants:
VS -Ch1 .0000V
VD -Ch3 .1000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

POLY2 PMOS 10/20 #04



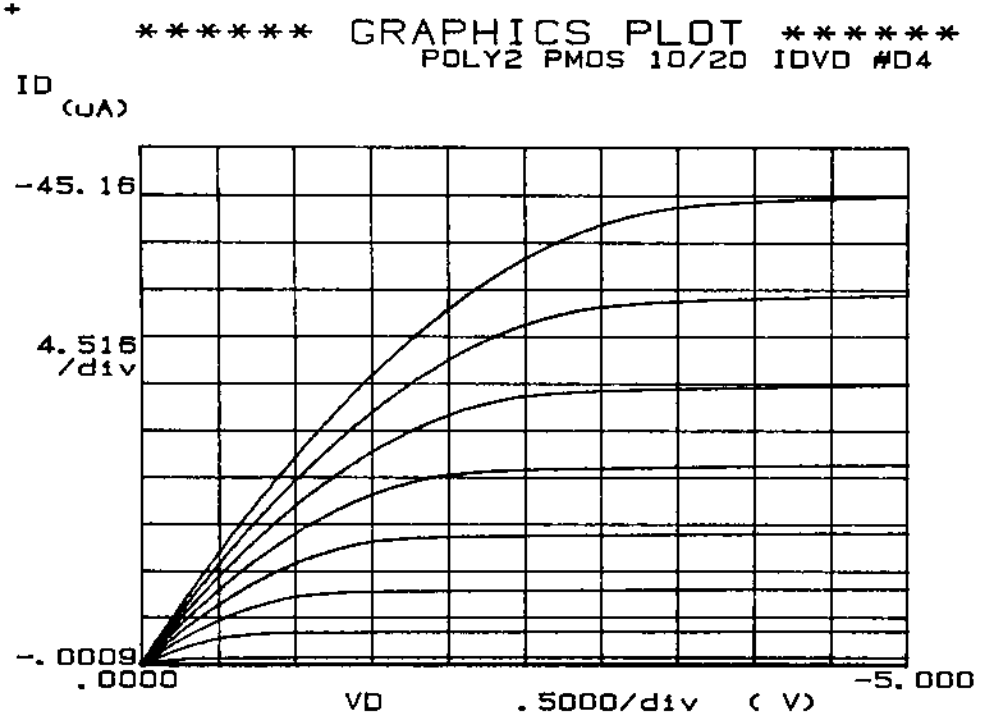
	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	583E-09	1.71E+06	-461E-03	269E-09
LINE2				

GM (/Ω) = ΔID/ΔVG
IDS (ΓA) = ΓID

Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop -5.0000V
Step -.1000V

Variable2:
VD -Ch3
Start -.1000V
Stop -.1000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V



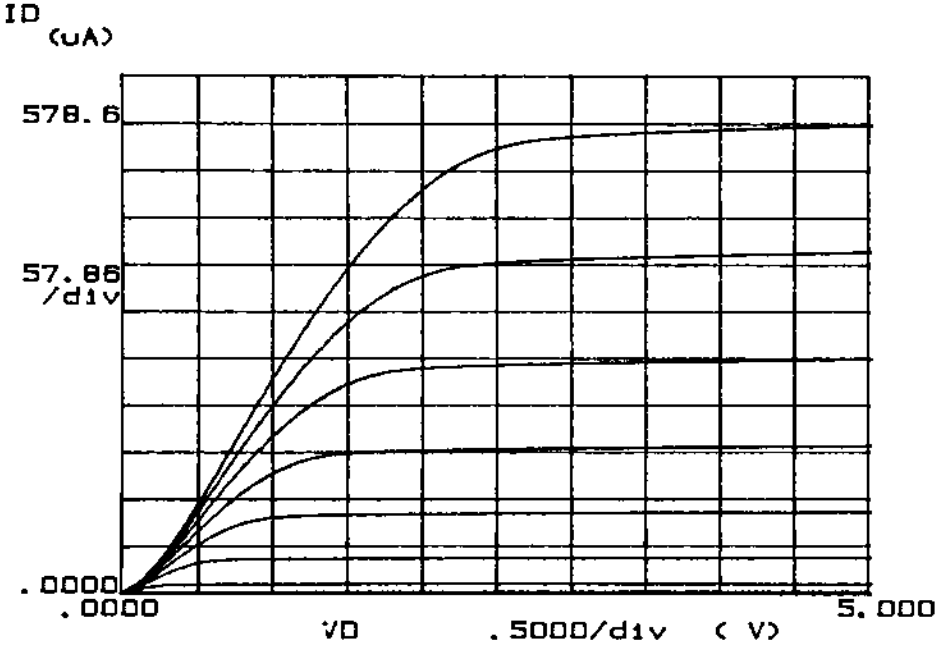
Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step - .1000V

Variable2:
VG -Ch2
Start .0000V
Stop -4.5000V
Step - .5000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

NMOS 16/32 IDVD #D11



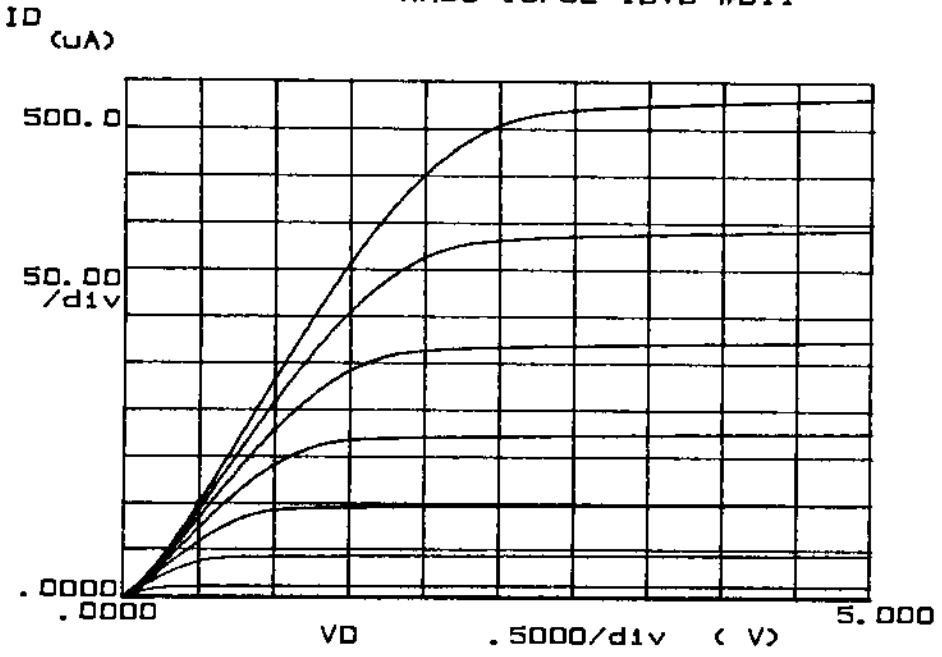
Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

Variable2:
VG -Ch2
Start .0000V
Stop 4.5000V
Step .5000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

NMOS 16/32 IDVD #D11



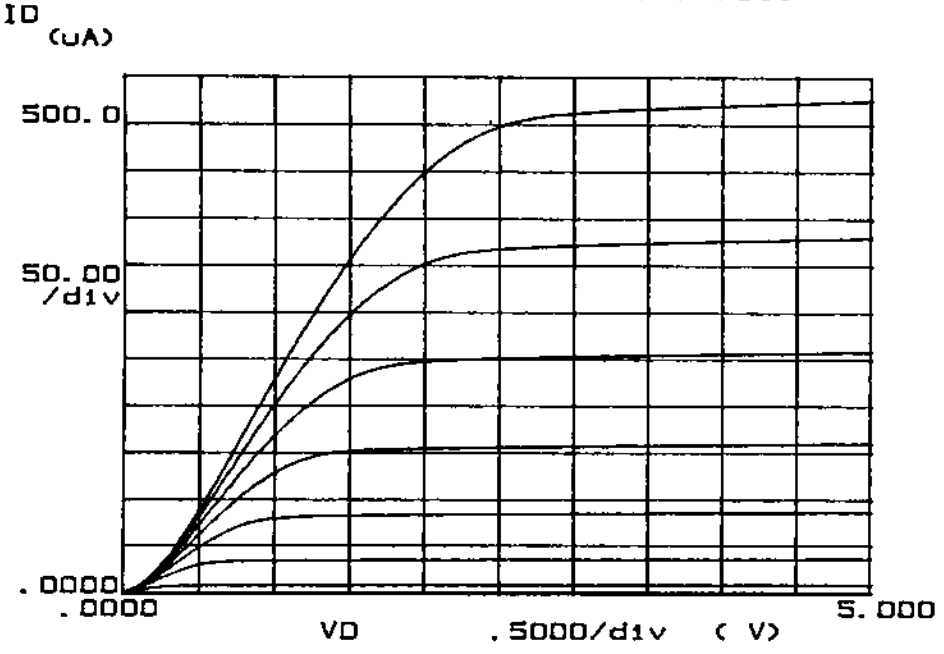
Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

Variable2:
VG -Ch2
Start .0000V
Stop 4.5000V
Step .5000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

NMOS 16/32 IDVD #D11



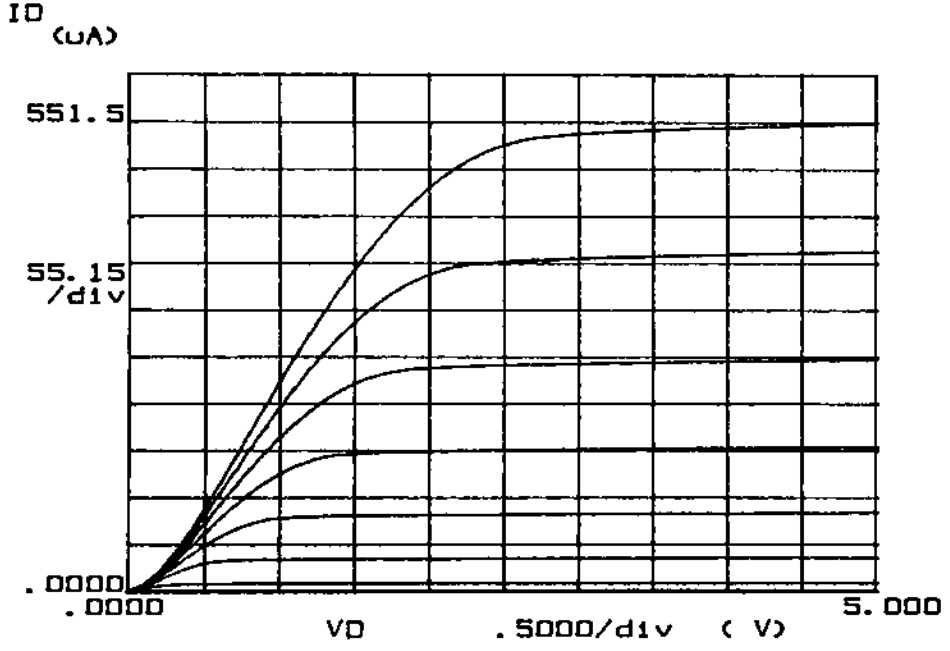
Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

Variable2:
VG -Ch2
Start .0000V
Stop 4.5000V
Step .5000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

NMOS 16/32 IDVD #D11



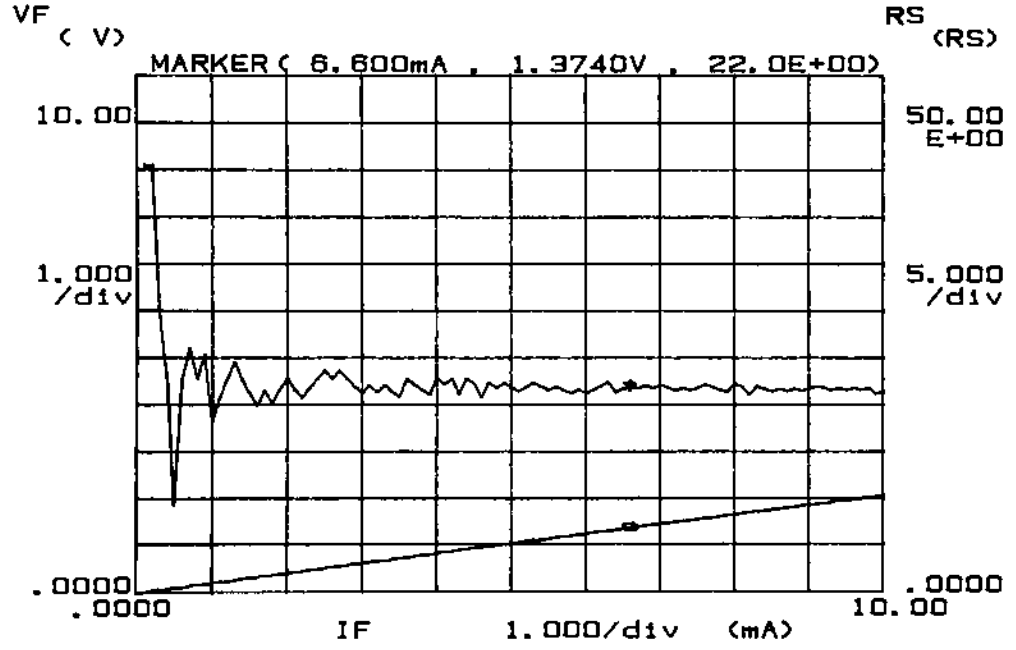
Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

Variable2:
VG -Ch2
Start .0000V
Stop 4.5000V
Step .5000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

N- POLY VANDERPAUW #D4



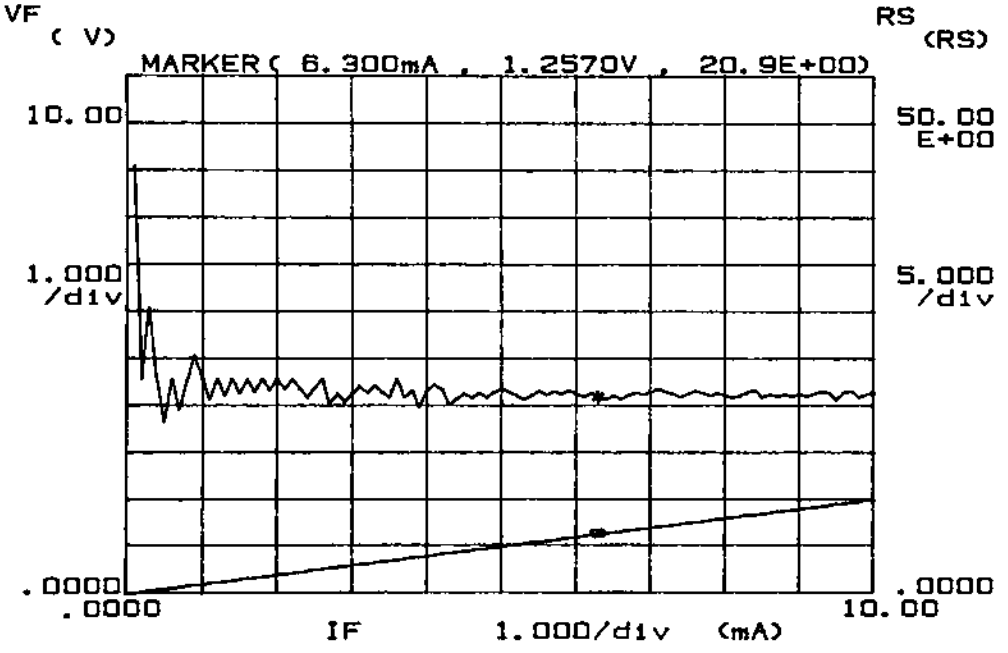
Variable1:
IF -Ch1
Linear sweep
Start .000 A
Stop 10.00mA
Step 100.0uA

Constants:
I1 -Ch2 .000 A
V -Ch2 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

N- POLY VANDERPAUW #D4



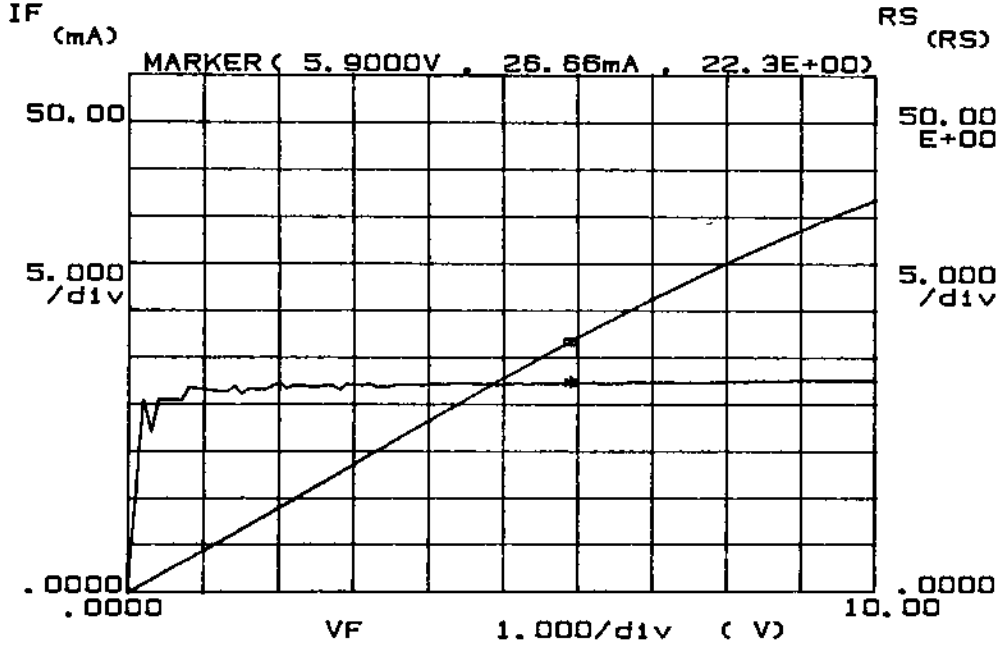
Variable1:
IF -Ch1
Linear sweep
Start .000 A
Stop 10.00mA
Step 100.0uA

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

N- VANDERPAUW #03



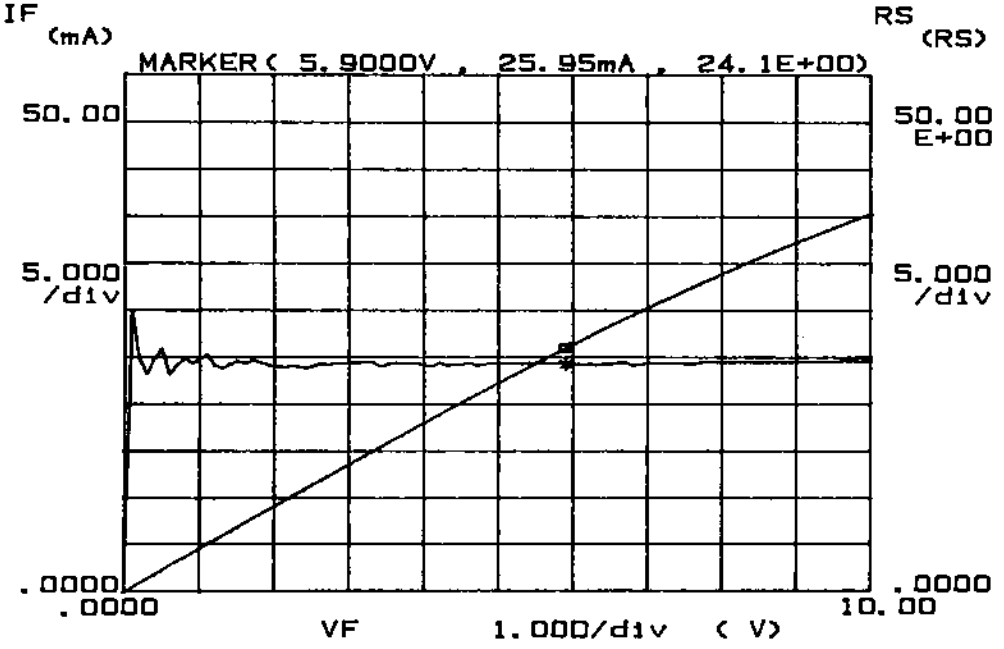
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step 10.000V
Step .1000V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

N- VANDERPAUW #D3



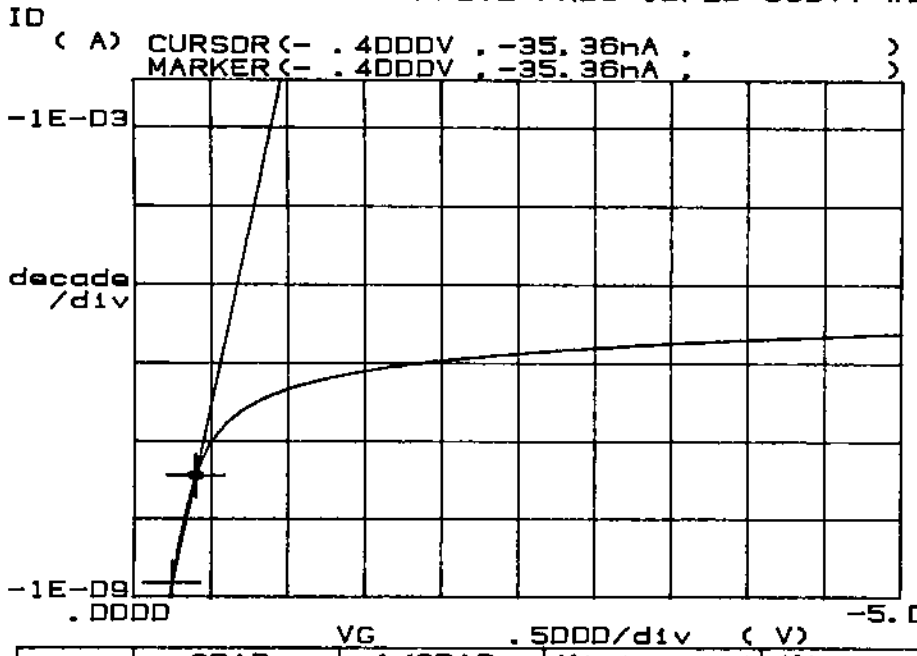
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step 10.000V
Step .1000V

Constants:
I1 -Ch2 .000 A
V -Ch3 .0000V
I2 -Ch4 .000 A

RC (RC) = (V2-V1)/IF
RS (RS) = (V2-V1)*4.532/IF

****** GRAPHICS PLOT ******

PDLY2 PMOS 1D/2D SUBVT #D4



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-9.11E+00	-11DE-03	-1.22E+00	-8.03E-12
LINE2				

SUBVT (mV) = ΔVG/(LOG((ΔID+2)+ID)-LOG(ID))

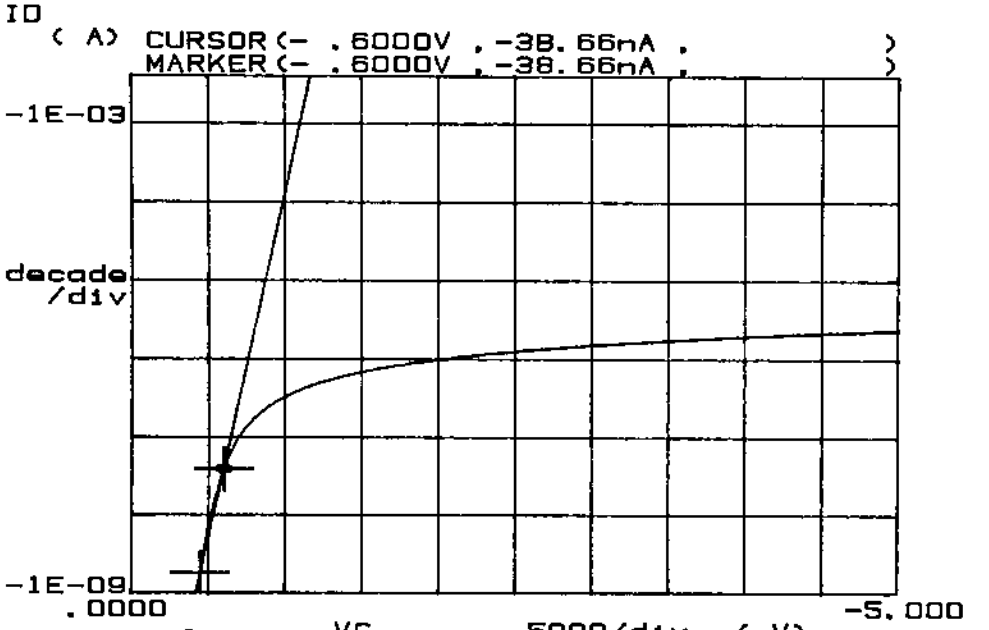
Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop -5.0000V
Step -.0500V

Variable2:
VD -Ch3
Start -.1000V
Stop -.1000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

POLY2 PMOS 10/20 SUBVT #D4



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-8.83E+00	-113E-03	-1.44E+00	-196E-15
LINE2				

SUBVT (mV) = AVG/(LOG((ΔID=2)+ID)-LOG(ID))

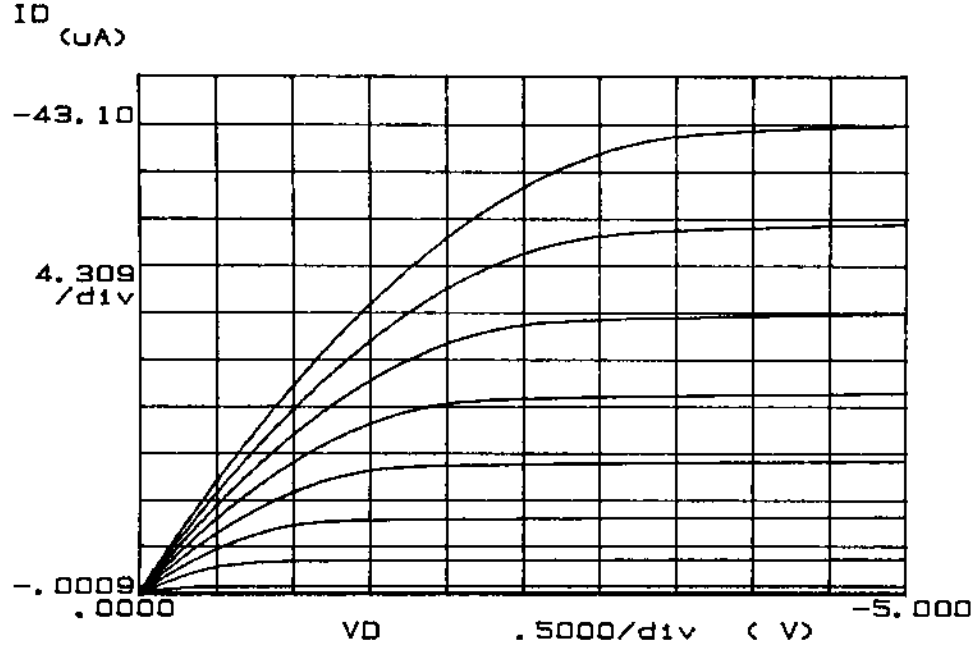
Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop -5.0000V
Step - .0500V

Variable2:
VD -Ch3
Start - .1000V
Stop - .1000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

POLY2 PMOS 10/20 IDVD #D4



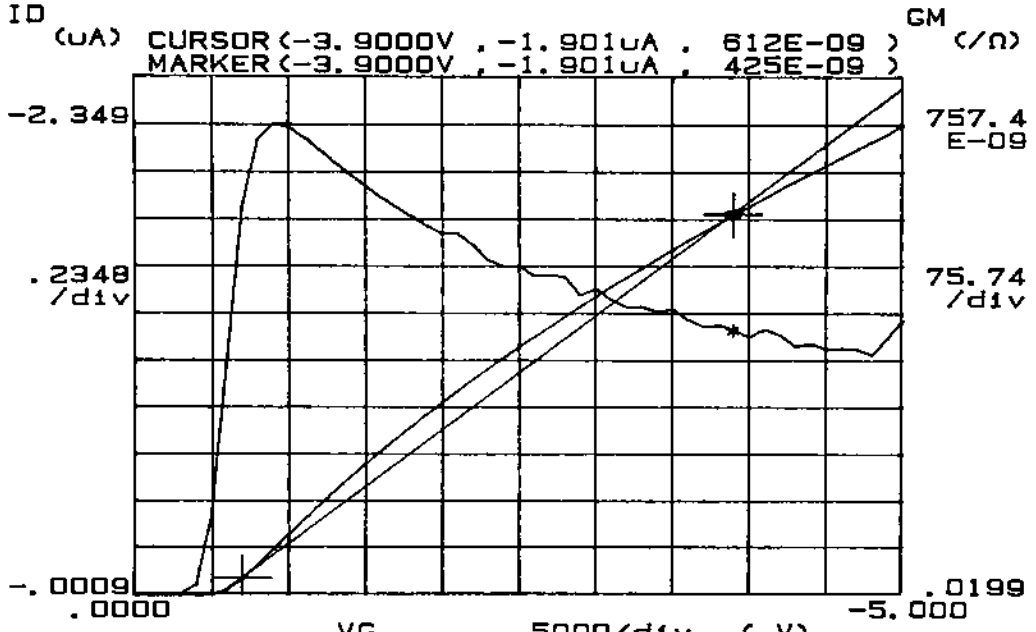
Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step - .1000V

Variable2:
VG -Ch2
Start .0000V
Stop -4.5000V
Step - .5000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

POLY2 PMOS 10/20 #D4



Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop -5.0000V
Step -.1000V

Variable2:
VD -Ch3
Start -.1000V
Stop -.1000V
Step .0000V

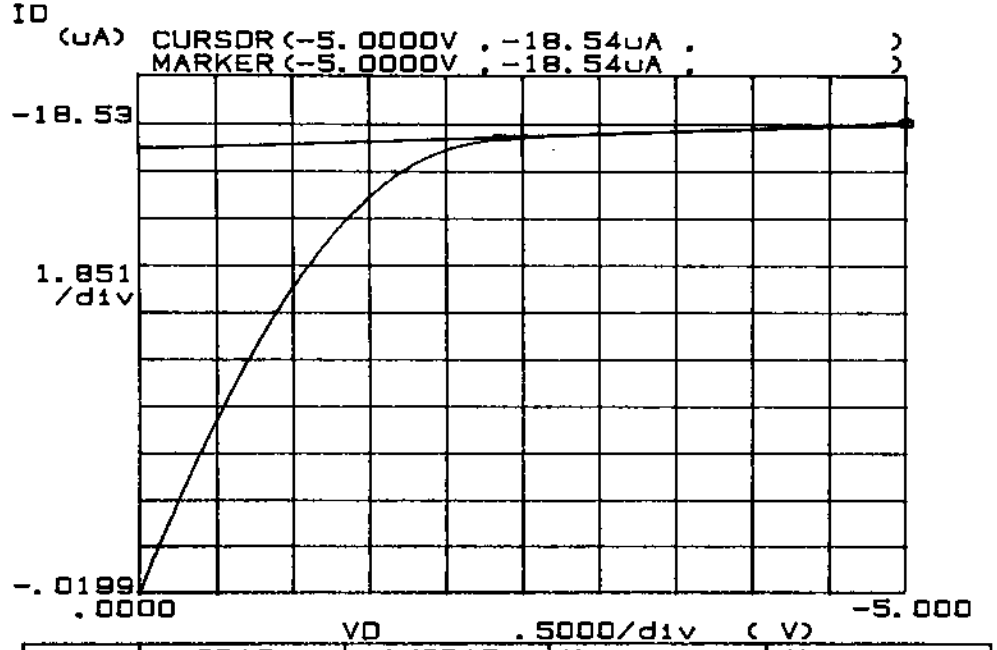
Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	569E-09	1.76E+06	-558E-03	317E-09
LINE2				

GM (/Ω) = ΔID/ΔVG
IDS (/A) = ∫ID

****** GRAPHICS PLOT ******

POLY2 PMOS 10/20 IDVD #D4



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	202E-09	4.94E+06	86.6E+00	-17.5E-06
LINE2				

Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step -.1000V

Variable2:
VG -Ch2
Start -3.0000V
Stop -3.0000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

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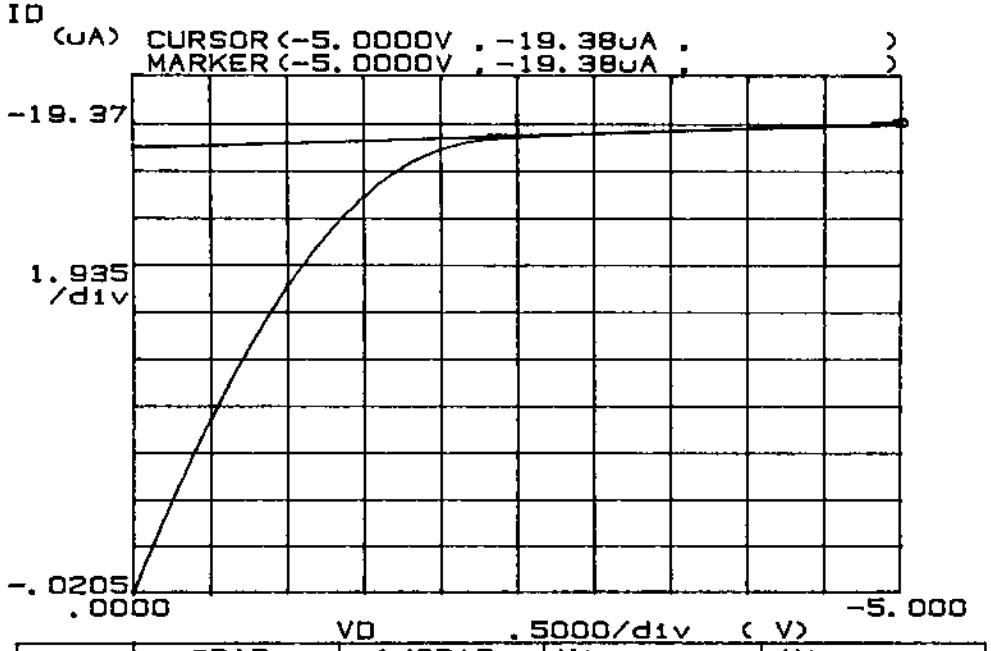
****** GRAPHICS PLOT ******

POLY2 PMOS 10/20 #D4



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	204E-09	4.90E+06	89.9E+00	-18.4E-06
LINE2				

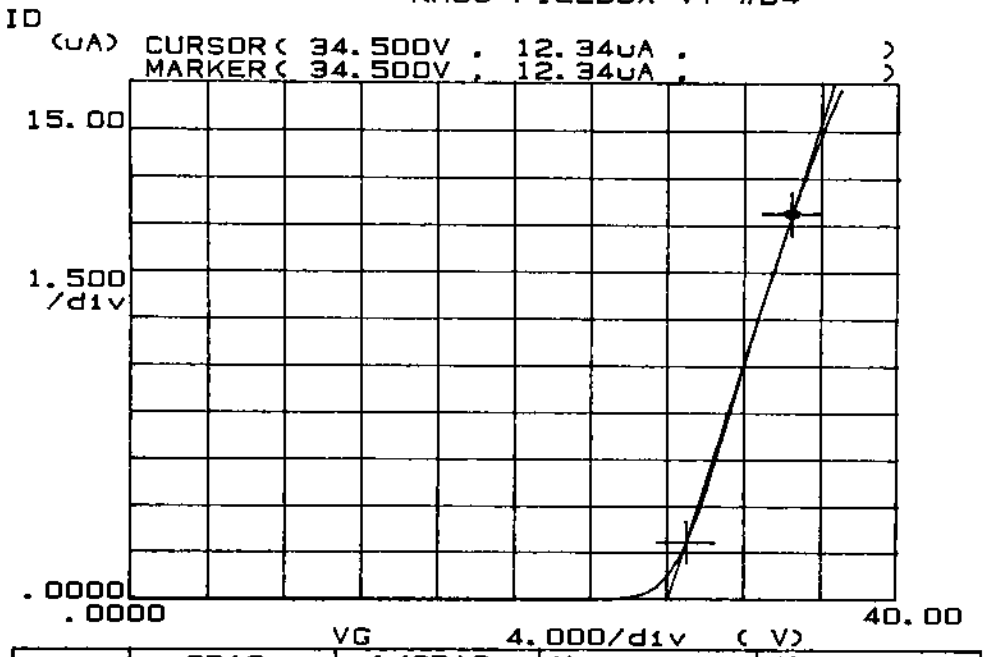
Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step - .1000V

Variable2:
VG -Ch2
Start -3.0000V
Stop -3.0000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

NMOS FIELDOX VT #D4



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	1.91E-06	523E+03	28.0E+00	-53.6E-06
LINE2				

GM (/Ω) = ΔID/ΔVG
IDS (fA) = fID

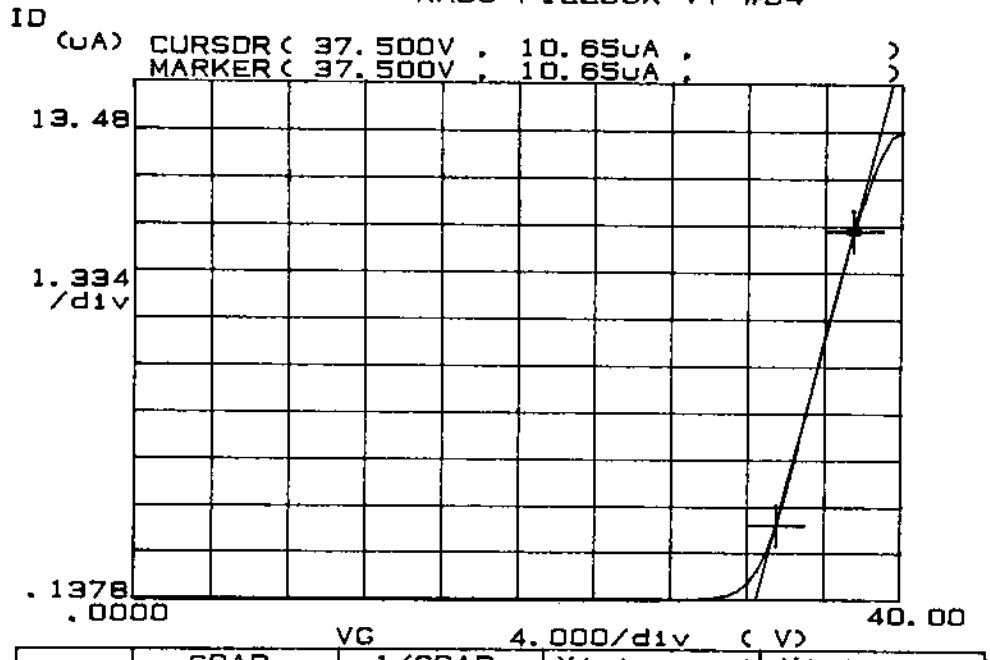
Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 40.000V
Step .5000V

Variable2:
VD -Ch3
Start .1000V
Stop .1000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

NMOS FIELDOX VT #D4



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	2.10E-06	477E+03	32.4E+00	-67.9E-06
LINE2				

GM (/n) = ΔID/ΔVG
IDS (√A) = √ID

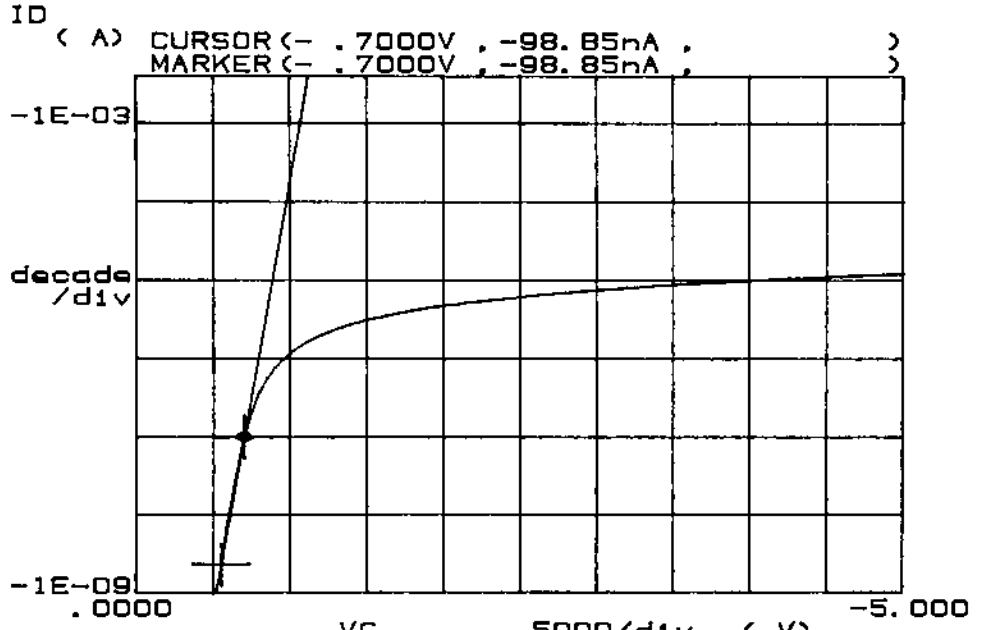
Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 40.000V
Step .5000V

Variable2:
VD -Ch3
Start .1000V
Stop .1000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

PMOS 16/32 SUBVT #D3



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-10.9E+00	-91.9E-03	-1.34E+00	-2.38E-15
LINE2				

SUBVT (mV) = ΔVG/(LOG((ΔID*2)+ID)-LOG(ID))

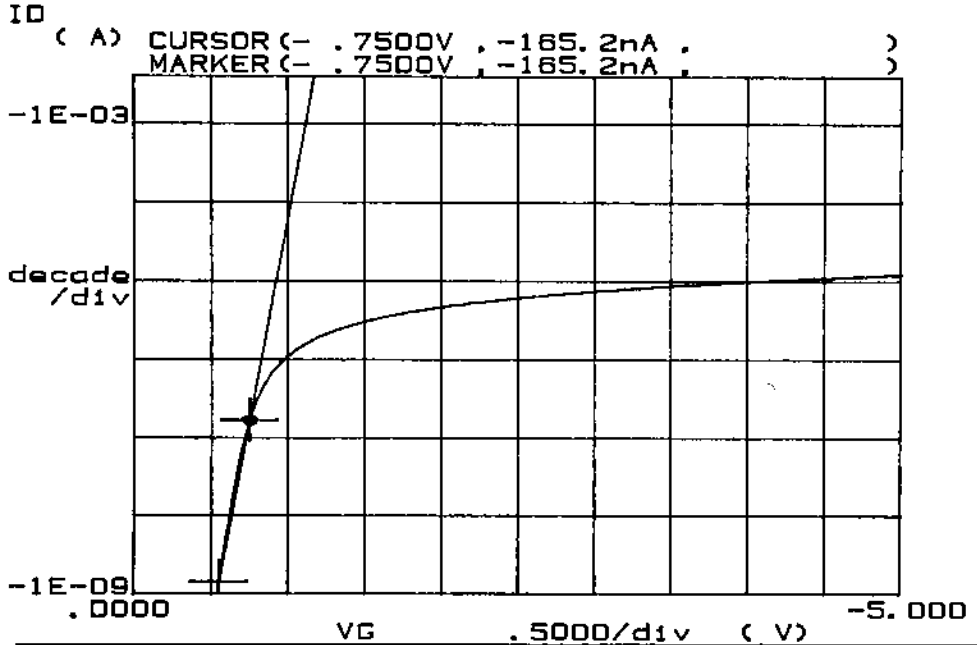
Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop -5.0000V
Step -.0500V

Variable2:
VD -Ch3
Start -.1000V
Stop -.1000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

PMOS 16/32 SUBVT #03



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-10.3E+00	-96.8E-03	-1.41E+00	-2.97E-15
LINE2				

SUBVT (mV) = ΔVG/(LOG((ΔID*2)+ID)-LOG(ID))

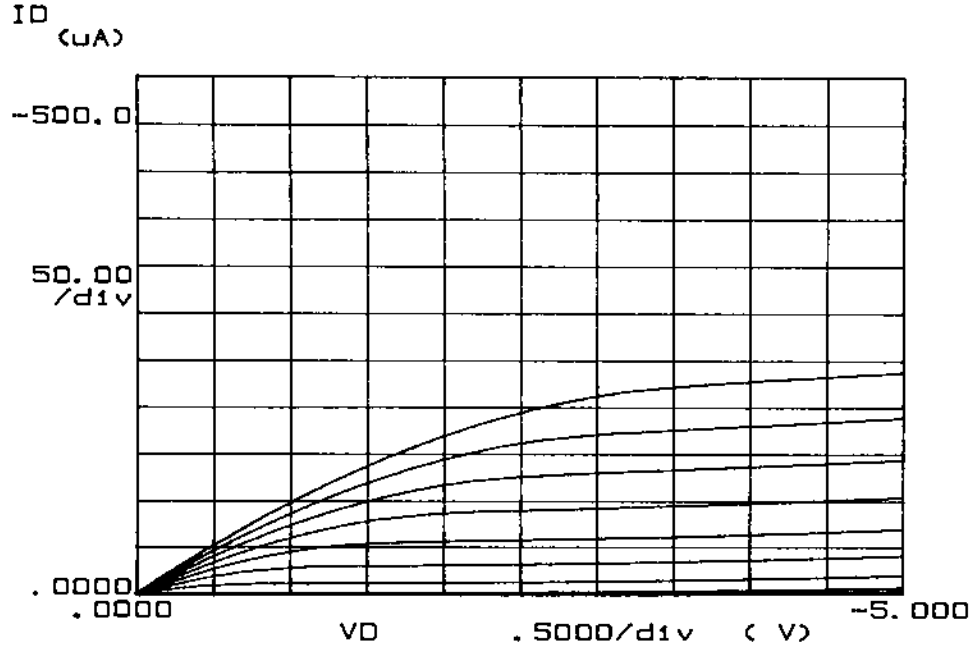
Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop -5.0000V
Step -.0500V

Variable2:
VD -Ch3
Start -.1000V
Stop -.1000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

PMOS 16/32 IDVD #D4



Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step -.1000V

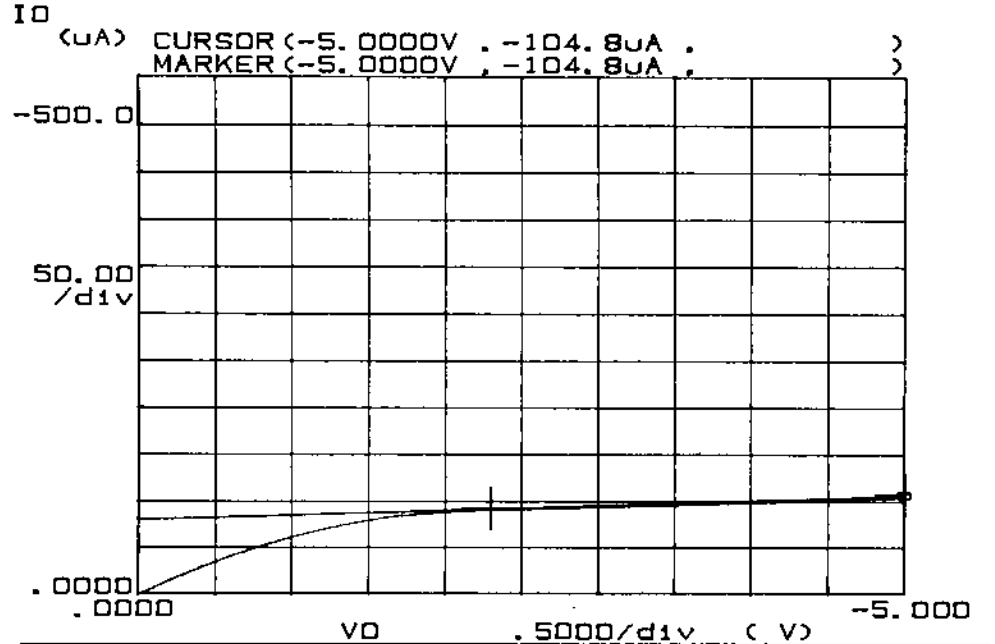
Variable2:
VG -Ch2
Start .0000V
Stop -4.5000V
Step -.5000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

P-45

****** GRAPHICS PLOT ******

PMOS 16/32 IOVO #04



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	5.05E-06	198E+03	15.8E+00	-79.5E-06
LINE2				

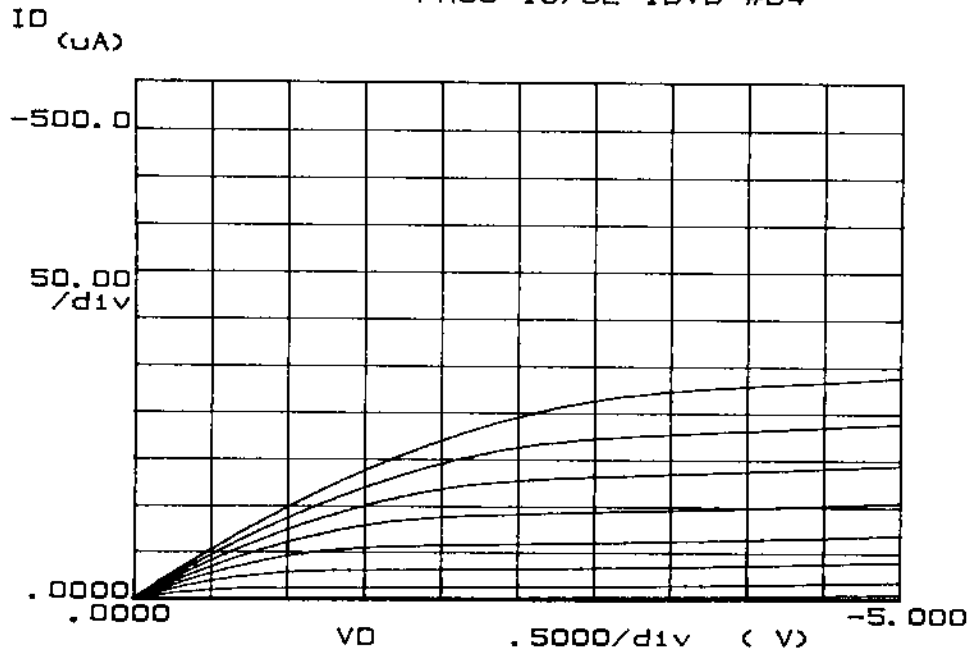
Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step -.1000V

Variable2:
VG -Ch2
Start -3.0000V
Stop -3.0000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

PMOS 16/32 IDVD #D4



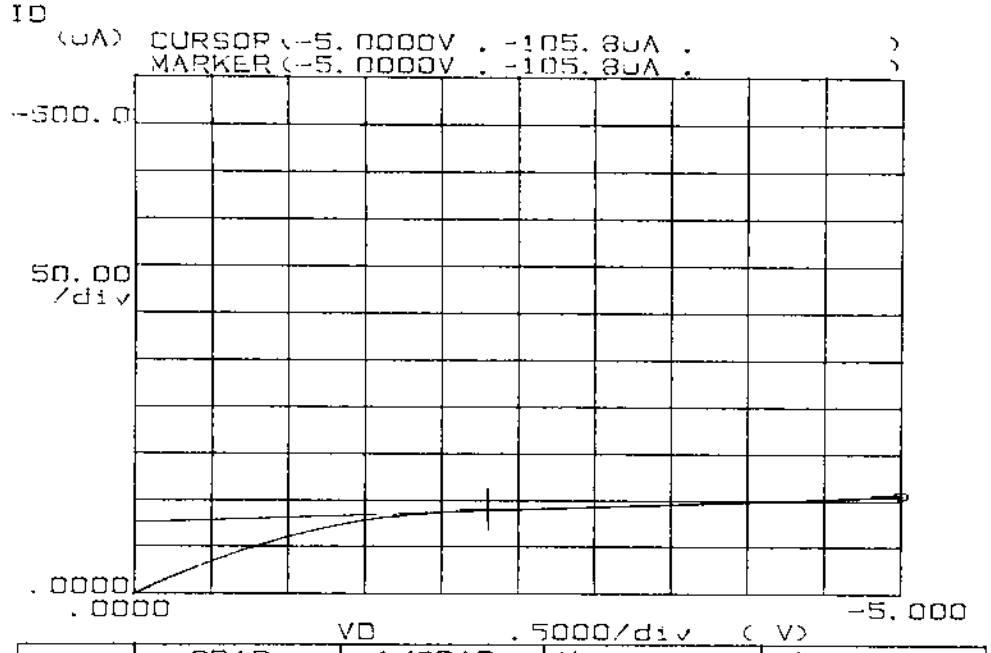
Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step - .1000V

Variable2:
VG -Ch2
Start .0000V
Stop -4.5000V
Step - .5000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

PMOS 16/32 IDVD #D4



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	5.80E-06	172E+03	13.2E+00	-76.8E-06
LINE2				

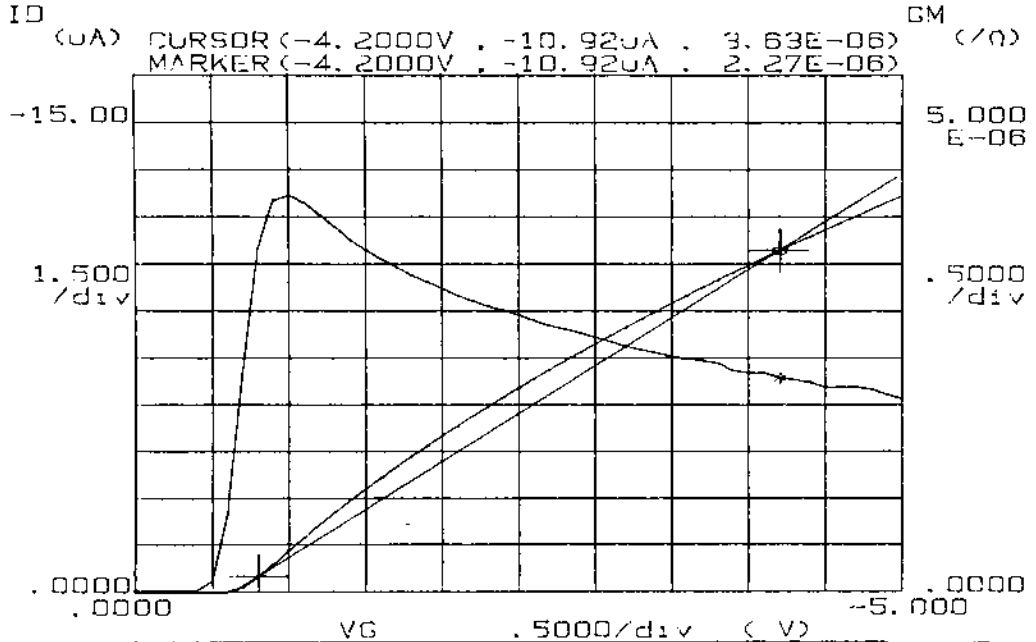
Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step -.1000V

Variable2:
VS -Ch2
Start -3.0000V
Stop -3.0000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

****** GRAPHICS PLOT ******

PMOS 16/32 IDVG #D4



Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop -5.0000V
Step -.1000V

Variable2:
VD -Ch3
Start -.1000V
Stop -.1000V
Step .0000V

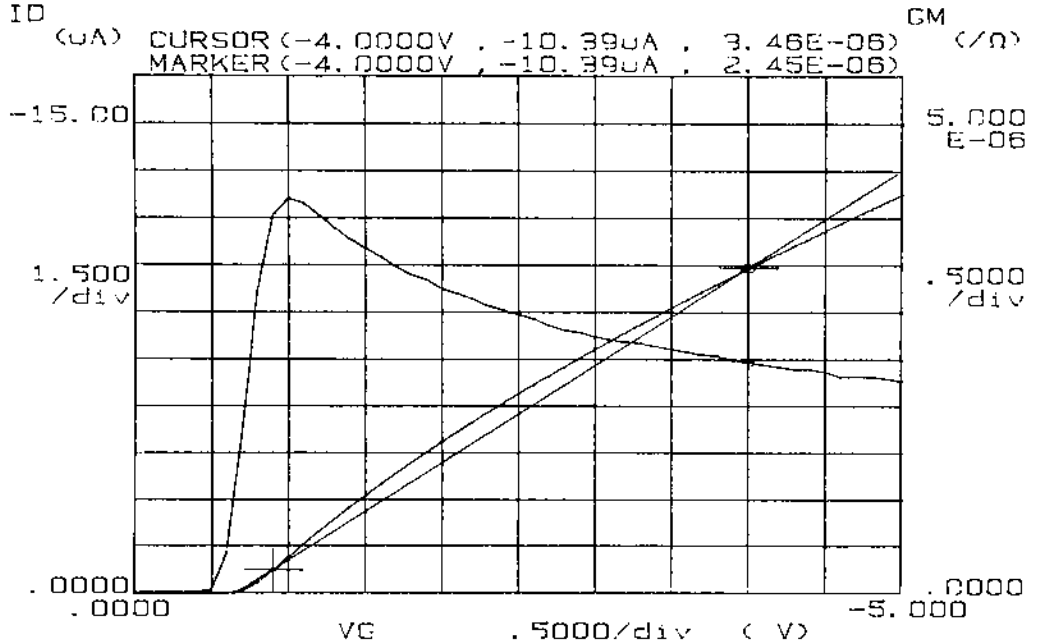
Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	3.07E-06	326E+03	-639E-03	1.96E-06
LINE2				

GM (/Ω) = ΔID/ΔVG
IDS (A) = FID

****** GRAPHICS PLOT ******

PMOS 16/32 IDVG #D4



Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop -5.0000V
Step -.1000V

Variable2:
VD -Ch3
Start -.1000V
Stop -.1000V
Step .0000V

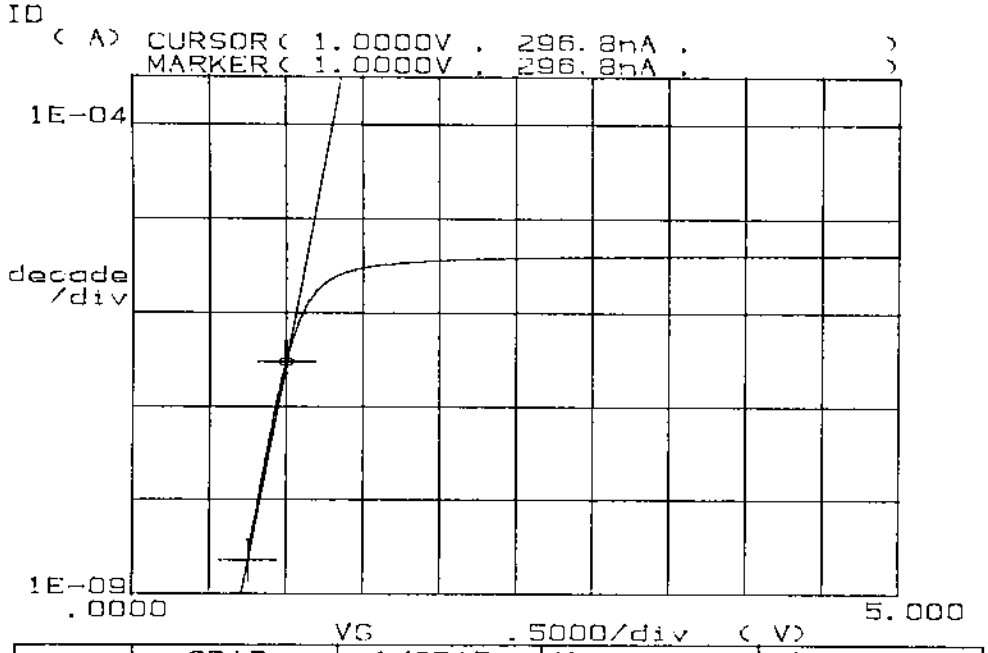
Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	3.11E-06	321E+03	-664E-03	2.07E-06
LINE2				

GM (/Ω) = AID/AVG
IDS (A) = AID

****** GRAPHICS PLOT ******

NMOS 6/32 SUBVT #04



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	8.44E+00	118E-03	1.77E+00	1.07E-15
LINE2				

Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Variable2:
VD -Ch3
Start .1000V
Stop .1000V
Step .0000V

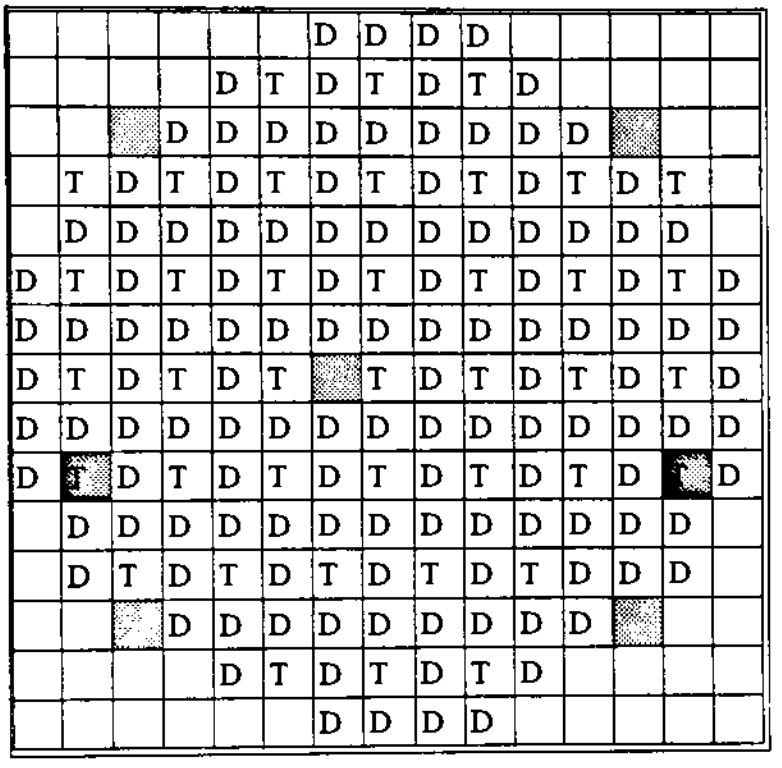
Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

APPENDIX E

Wafer Map

P-WELL CMOS TEST CHIP, DEVICE CHIP AND TEST SITE LAYOUT:

FOR ANALOG AND CID PRODUCTS:



<----------76.2 mm ---------->

ALIGNMENT DIE: LEFT ROW 10, COL 2
RIGHT ROW 1, COL 14

ALIGNMENT KEY OFFSET: (on wafer, in mm, with respect to center of the die)

X = 2.25050
Y = - 2.24800

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4,5 D.D. Buss, M.F. Tompsett, et all, *IEEE Transactions on Electron Devices,*vol ED-23 no. 2, February 1976, pg 177-182.

6-10 S. Wolf, Silicon Processing for the VLSI era,Volume 2: Process Integration, Lattice Press, California, 1990. pg368-373

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13. B. Backer, Z. Ninkov, M. Corba, *SPIE Proceedings*, vol. ,1996