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Developing Germanium on Nothing (GON) Nanowire Arrays

By

Paul M. Thomas

A Thesis Submitted

in Partial Fulfillment of the

Requirements for the Degree of

Master of Science

in

Microelectronic Engineering

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ROCHESTER INSTITUTE OF TECHNOLOGY

ROCHESTER, NEW YORK

SEPTEMBER, 2010

Developing Germanium on Nothing (GON) Nanowire Arrays

By

Paul M.Thomas

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Paul M. Thomas September 29, 2010

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Abstract

Advanced crystal growth techniques enable novel devices and circuit designs to further scale and integrate heterogeneous structures for CMOS, MEMS/NEMS, and optoelectronic applications. In particular, nanowires (NW) are among the promising structures derived from these developments. Research has demonstrated the utility of NWs as a channel material for gate-all-around transistors, high sensitivity biological/chemical sensors, photodetectors, as well as a whole spectrum of LEDs and lasers. However, NW based devices are not without their fabrication challenges. Relatively simple structures for CMOS or MEMS/NEMS processes are difficult to reproduce when many NW based devices rely on a dropcast process. This thesis demonstrates a method for producing Germanium on Nothing (GON) NW arrays on a Si substrate that forgoes dropcasting and, instead, creates NWs via selective material removal methods commonly utilized by industry.

GON NW arrays are formed through the sequential use of E-beam lithography, selective wet chemical etching, and reactive ion etching. Global oxide thinning in BOE leaves a thin masking layer that protects the underlying Si, preventing etching in a TMAH solution. GON regions are defined by E-beam lithography and are subject to a RIE which creates release points in the remaining SiO_2. Unmasked Si is then etched by a TMAH solution, undercutting the Ge lines, leaving an array of suspended Ge wires. NW dimensions are reached by thinning the Ge wire diameter with a H_2O_2 solution. NWs with ~50 nm diameters and ~ 200 nm lengths, as well as 10 μm by 10 μm membranes of Ge/SiO_2, have been demonstrated in this thesis.

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Chapter 1

Introduction and Motivation

1.1 Introduction

Advanced crystal growth techniques enable novel devices and circuit designs to further scale and integrate heterogeneous structures for CMOS, MEMS/NEMS, and optoelectronic applications. Nanowires (NW) are among the promising structures derived from these developments, in particular. Other work has shown the utility of Ge NWs as gate-all-around transistors, high sensitivity biological/chemical sensors, as well as LEDs. However, NW based devices are not without their fabrication challenges. Relatively simple structures for CMOS or MEMS/NEMS are difficult to reproduce when many NW based devices rely on a dropcast process. This thesis demonstrates a method for producing Germanium on Nothing (GON) NW arrays that forgoes dropcasting and, instead, creates NWs via selective material removal methods commonly utilized by industry.

NW production is limited to a handful of techniques, of which few can form prealigned structures. The majority NWs are formed with aid of a metal catalyst from which wire growth propagates. Vapor-Solid-Liquid (VLS) growth is one of the most common methods through which NWs are meticulously grown on a substrate and collected for dropcast processing. NWs are also commonly grown from catalysts in solution. Device fabrication utlizing these NWs involves dropcasting over a substrate and wire alignment using an electric field. While this alignment process results in NWs over the contacts, the exact orientation and placement of these wires is not a repeatable process. Additional processing steps to secure the wires to the source and drain contact

regions are performed and the NW is then ready for additional modifications to make devices. The aforementioned processes tend to produce random crystal orientations in the NWs as well as random placement on the substrate/contact surface [3-6]. Additional techniques include the use of microcrucibles for rapid melt growth (RMG) formed wires and reactive ion etching (RIE) of a film stack of Si/Si_xGe_{1-x} and wet etching to produce Si NWs on a substrate [1]. However, few have investigated selective wet chemical etchants for creating Ge NW systems from film stacks of Si and Ge.

NWs may be part of the future for the CMOS industry as the quasi-1 dimensional nature of these structures lend themselves to gate-all-around devices which, similar to double gate and fin structures, have significantly greater electrostatic control of the channel resulting in better short channel effect resistance than planar FETs at the technology node [7, 8]. However, to the author's knowledge, few of the previously developed fabrication techniques produce channel regions compatible with the demands of the IC industry. Materials used for growth of NWs, poor control of growth direction, and difficult integration have all plagued the utilization of NW devices for today's applications [3-6]. In this study the authors present a method by which arrays of Germanium-on-Nothing (GON) NWs may be fabricated by methods commonly used in CMOS production.

Researchers have been investigating Ge NWs for use in a variety of MEMS/NEMS applications ranging from high frequency oscillators to extremely sensitive sensors [9]. Because NWs have high surface area to volume ratios any additional material will fundamentally alter the electrical characteristics, biological and chemical sensors benefit from this increased sensitivity to a target chemical species [10].

Other MEMS could take advantage of the ferromagnetic properties of Mn doped Ge NWs [11]. Additionally, due to minute scale of NEMS these systems will generally consume less power and have lower heat capacity than MEMS [9].

In addition to logic devices and NEMS, Ge NWs may be particularly useful for optoelectronic applications. Ge NWs, under tensile strain or near degenerate n-type doping conditions, have been shown to emit light due to the secondary conduction valley that is a direct bandgap. Recent studies have shown that n-doped or tensile strained bulk Ge can emit light at wavelengths of roughly 1550 nm [12]. Ge NW arrays may present a method for tuned light emission through adjustments in the strain on the suspended NWs. Other studies on nanoscale Si and Ge have shown interesting bandgap charactersistics due to the quantum confinement seen in NWs, as such Ge may also provide a path for monolithically integrating visible wavelength lasers, LEDs, and photodetectors on a Si substrate [13, 14].

The GON NW approach demonstrated here may present a method by which NW devices could be fabricated in designated locations and by methods under common use in industry. GON relies on epitaxial growth of semiconductor material in dielectric trenches on a Si substrate [15]. A series of wet and dry etches as well as electron beam lithography (EBL) is used to define where the GON NWs will be located [16-18]. GON NWs with dimensions as small as 50 nm diameter and 250 nm lengths have been fabricated on a Si substrate.

1.2 Literature review

Since the discovery of Carbon Nanotubes in the 1990's, researchers have been investigated the use of one dimensional devices [19, 20]. Among these novel structures

are Si and Ge nanowires. While the concept of these structures may be easy to visualize, the production of them is nontrivial [3-6]. Complicated techniques involving specific catalysts combined with particular substrates or solutions, liquid phase epitaxy, and material stacks combined with selective etching [1-6]. However, these processes do not provide simple solutions for integration into circuits and often rely on dropcasting solutions containing nanowires over a series of contacts and other difficult to control mechanisms.

1.2.1 Vapor-Liquid-Solid growth

Many NW systems are formed via Chemical Vapor Deposition (CVD) growth techniques, commonly referred to as a "Vapor-Liquid-Solid" growth. During VLS, a catalyst is deposited on a wafer surface, the catalyst is typically Au, and the formation gasses flow into the heated chamber where they contact the catalyst and form a eutectic alloy. As additional material is reacted, a wire of size determined by the catalyst radius is formed. However, these wires have a tendency to grow in random orientations, and even branch off of each other, creating coral-like clusters of NWs as seen in Figure 1.1 [10]. While progress has been made in the growth control of these nanowires, even with the best growing surface there are often enough random growths to have undesired effects and controlled placement of the catalyst is still problematic [4]. As with many reactions, the crystal orientation matters and will have definitive effects on the orientation and direction of growth of the nanowires [21].

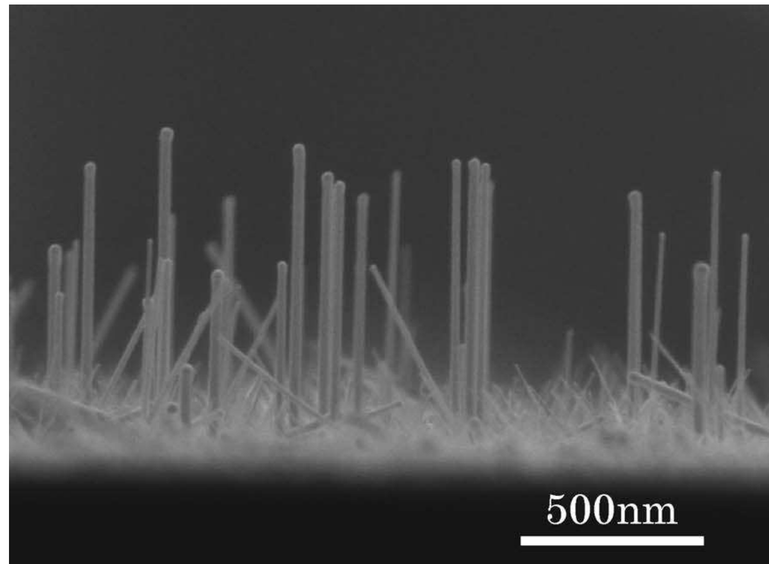


Figure 1.1. SEM micrograph of Ge NWs grown via CVD on a (111) p doped Si substrate [10].

1.2.2 Solution Growth

Growing nanowires in solution is similar to the CVD approach in that a catalyst is utilized. However, in this case, a supersaturated stock solution provides the growth material and a colloidal metal powder acts as the catalyst where particle size defines the size of the grown wires. While this process eliminates the need to delaminate nanowires from the substrate, it suffers from the same wire placement issue associated with drop casting as shown in Figure 1.2 [7].

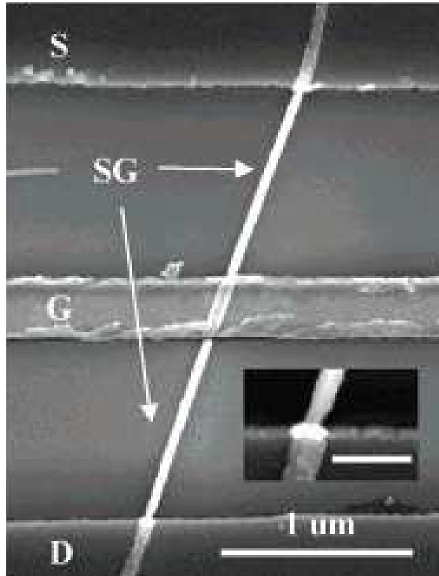


Figure 1.2. NWs generated in solution drop cast on contacts on the substrate [7]

1.2.3 Rapid Melt Growth Process

Rapid melt growth (RMG) is a form of liquid phase epitaxy (LPE). During RMG, a polycrystalline deposit is made into a prefabricated trench with a contact to a specifically oriented seed crystal wafer [2]. This material is then capped with a thermally stable compound and the entire wafer is rapidly heated to the point where the polycrystalline material will melt. This method requires that the growth material melt at a lower temperature than the seed region. As the material cools a growth front originates from the seed layer and progresses through the melt until a single crystalline layer of the same orientation as the seed layer forms. Cross sections of RMG process are shown in Figure 1.3, this process forms relatively defect free crystals in the microcrucible. Small NWs may be produced with this method, though care would need to be taken to minimize defect formation during the cooling phase of the wire formation.

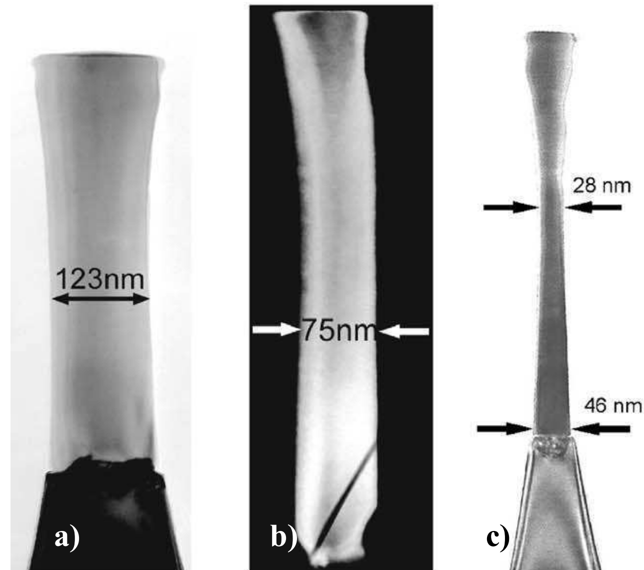


Figure 1.3. (a) Ge column with 123 nm width. (b) Dark field view of 75 nm diameter Ge column, showing defect. (c) Ge column with NW dimensions [2].

1.2.4 Epitaxial film stack Process

Nanowires grown by this process originate from alternating layers of epitaxially grown material. After the epilayers have been formed, an etch mask is defined by photoresist or hardmask. RIE removes material exposed to the plasma gases, leaving a column of desired material. Then the material in the epistack column is selectively etched, and suspended NWs are formed by the remaining material as seen in Figure 1.4 [1].

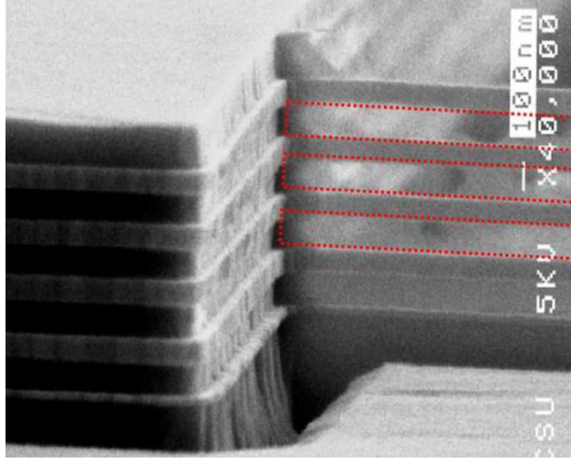


Figure 1.4. Si_xGe_{1-x} NWs formed by RIE and TMAH wet etch [1].

1.3 Nanowire applications

NWs are increasingly the subject of research for the upcoming generation of many interesting applications and devices. Researchers have demonstrated the utility of nanowires for a variety of devices ranging from transistors to NEMS.

1.3.1 Gate-all-around transistors

NWs formed by the GON process may provide a path for relatively easy gate-all-around (GAA) transistor integration. GAA transistors may be possible by this process because the suspended regions allow for conformal coating of the channel region. GON may produce GAA transistors similar to the works of Cohen *et al.,* Fang *et al.* and Dupré *et al.* related to Si NWs [22-24]. A GAA transistor provides greater electrostatic control of the channel when compared to planar and dual gate FETs [25]. Smaller technology nodes require more advanced control of the channel due to effects related to the diminishing gate lengths. Without proper controls the benefits of scaling are lost to short channel effects that significantly diminish the utility of transistors. GON may provide a path around this by creating suspended wires for use in GAA transistors.

1.3.2 Semiconductor lasers and LEDs

NWs may be particularly suited to making small light emitting diodes (LED) and lasers. Semiconductor LEDs and lasers require a medium which provides optical gain and acts as a waveguide. The largest NWs may easily provide both, and in a range of wavelengths tunable by NW diameter. Light emitted from NW systems is mostly likely to propagate out from the ends due to the confinement,

1.3.3 Photodetectors

Dense arrays of NWs may act as a source of future photodetectors. NWs and nanodots (ND) only allow a few specific states due to quantum effects. Such effects may be advantageous for detecting specific wavelengths or polarizations of light. These NWs would conduct current when exposed to specific wavelengths, with large responses near the absorption edges of the wire.

1.3.4 Sensors

Sensors built from NWs may be especially sensitive and allow for fine tuning of applications. Photosensors were covered previously, but strain, thermal, chemical, and motions could all be measured by NW based devices. Most devices would rely on the change in resistance due to strain of the wire with respect to the stimulus, as it would be the easiest change to monitor. However, chemical sensors would like measure a change in resistance due to the added material clinging to the wire. Many sensing applications stand to improve in sensitivity with the incorporation of NWs into the circuitry.

Chapter 2

Theory

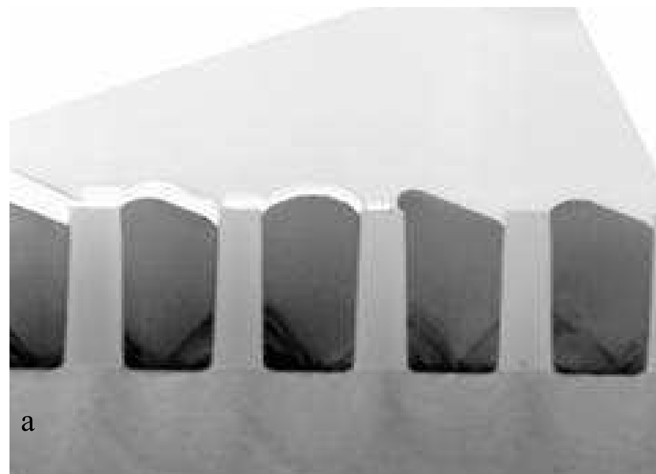
2.1 Introduction

Fabricating Ge NWs via subtractive processes is in line with the methods used to make the integrated circuits of today. However there are unique challenges for Ge systems which will be addressed in the following sections.

2.2 Aspect Ratio Trapping

The primary principle of Aspect Ratio Trapping (ART) is that a lattice mismatched semiconductor (such as Germanium) can be grown on Silicon, and have a reduction in dislocation defect density proportional to the aspect ratio of the trench in which the semiconductor was epitaxially grown. ART was developed to address the issues associated with lattice mismatched epitaxial growth on Silicon, which requires thick graded junctions for any reasonable crystal quality. However, ART was designed to create a virtual substrate of the grown semiconductor without the need for thick transition regions that would be required otherwise.

ART started as attempts to grow lattice mismatched semiconductors in small openings in a thermal oxide on a Si substrate [26]. Park *et al.* demonstrated that the crystal growth plane in a MOVCD would be such that once the semiconductor reached the critical thickness that the defects would propagate out to and terminate at the oxide walls of the trench. Under NSF grants ECCS-0725760 and ECCS-0832653, Amberwave systems provided ART substrates for the purpose of forming Ge devices or devices on virtual Ge/GaAs substrates as presented by Rommel *et al.* [27].



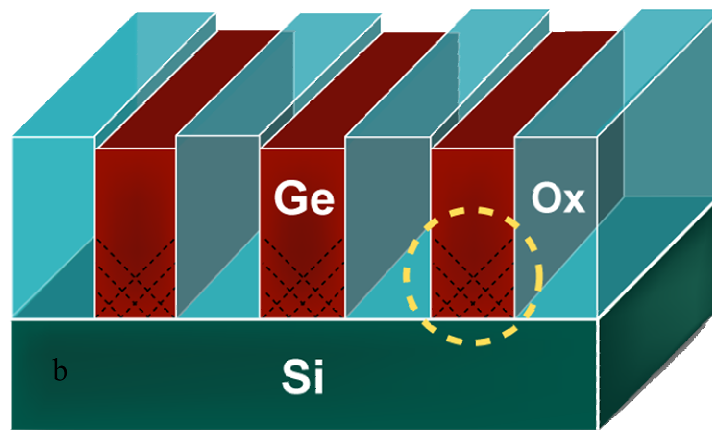
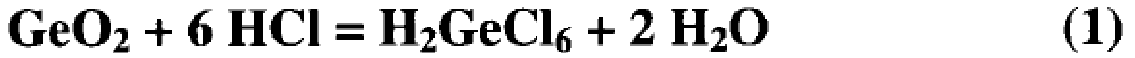


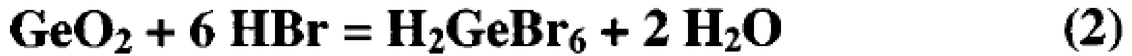
Figure 2.1. (a) Columns of ART Ge developed by Amberwave systems [15]. (b) This study utilized the material in the trenches and not the virtual substrate to fabricate nanowires in a subtractive, top-down process.

2.3 Hydrofluoric acid oxide etch

It has long been known that HF will etch glass (SiO_2), and as such this chemical has been used for many years in the IC industry to etch the SiO_2 formed during processing [28]. HF acid etches GeO_2 and SiO_2 by the reactions seen in Figure 2.2. HF does not etch Si at any appreciable rate without an additional oxidizer to form SiO_2, such HNO_3 [29]. Due to the similar lattice and bond structure of Ge relative to Si, the material is also resistant to etching in a HF solution as shown in Figure 2.2. However, like SiO_2,

GeO_2 is also etched rapidly by HF and, as such, this may be useful for device fabrication in the future. The concentration of HF in solution affects the etch rate of oxide has to be taken into consideration as some SiO_2 is needed as a mask material during the Si etch.





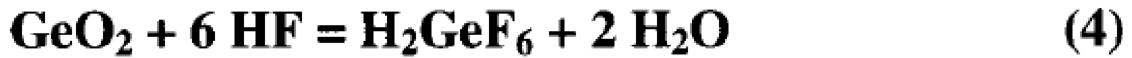


Figure 2.2. The chemical reactions of halogen acids with Ge and Si oxides [30].

2.4 E-beam Lithography

Where optical lithography utilizes photons to initiate the chemical reaction in photoresist to define positive and negative features, E-beam lithography utilizes electrons to provide the energy for the chemical reaction that will leave features behind. As a research tool, e-beam lithography allows a researcher to create patterns much smaller than could be produced by contact lithography and also allows for alignment so that devices more complicated than simple diodes can be realized. Patterns produced with an E-beam are limited by the dwell time of the beam, width of the beam, and the acceleration bias of the electrons [31]. The LEO EVO50 SEM equipped with a Nabity Pattern Generation System (NPGS) at RIT has produced test structures as small as 35 nm across in PMMA 9550 4A. Pieces are mounted on a planten and loaded into the LEO SEM. When writing with E-beam, the focus of the beam is absolutely vital to the production of good patterns and, as such, characteristics such as beam wobble,

stigmation, gun tilt all will be adjusted to get the maximum possible current and focus. While photons can be focused utilizing lenses, electrons must be electrostatically and magnetically focused in the beam column into the writing spot size as seen in Figure 2.3 [32].

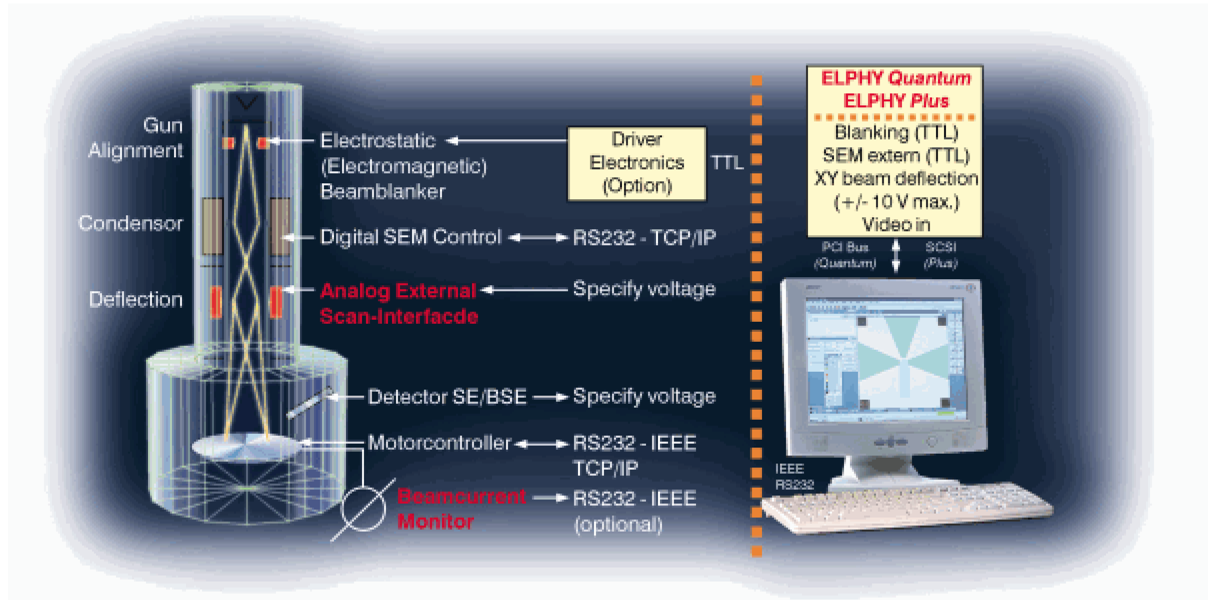


Figure 2.3. An example of how the electrons are guided down a beam column and detected [32].

After the beam is satisfactorily focused, the sample needs an additional focus step to ensure that the plane of the write is in focus. The pattern file is then loaded with the specified die to die spacing, line to line spacing, and exposure dose and then the operator hits go, and the system starts to write. E-beam systems write small, dense features though poorly implemented die design may overexpose and merge patterns. Once exposed to electrons the PMMA polymer reacts and becomes soluble in MIBK and IPA as seen in Figure 2.4. Depending on the beam current, the write time for the system can be limited by the stage movement time.

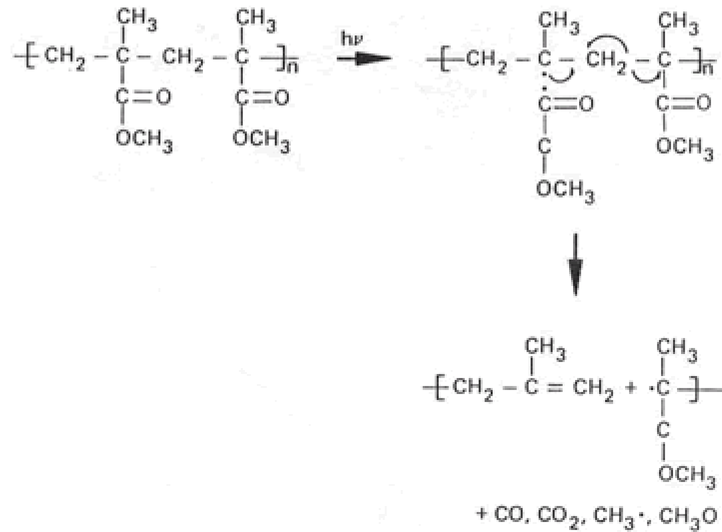


Figure 2.4. PMMA, when exposed to electrons, cleaves the polymer into solvent soluable compounds and gasses [33].

2.5 Reactive ion etching

Reactive Ion Etching (RIE) combines the chemical component of wet etching with the physical component of sputtering, to provide a system that often has great material selectivity and reasonable anisotropy. In a RIE system, plasma is created to produce radical ions that will often preferentially etch certain materials. The plasma is created by accelerating electrons towards a cathode, when these electrons collide with gasses in the chamber they can impart some of their energy to create excited molecules or, with enough energy transfer, break molecular bonds altogether. These free radicals and ions are now drawn toward the sample surface where they may react to form gaseous compounds or may sputter the exposed area. A cartoon of the plasma process combined with the dry etching process can be seen in Figure 2.5 [34].

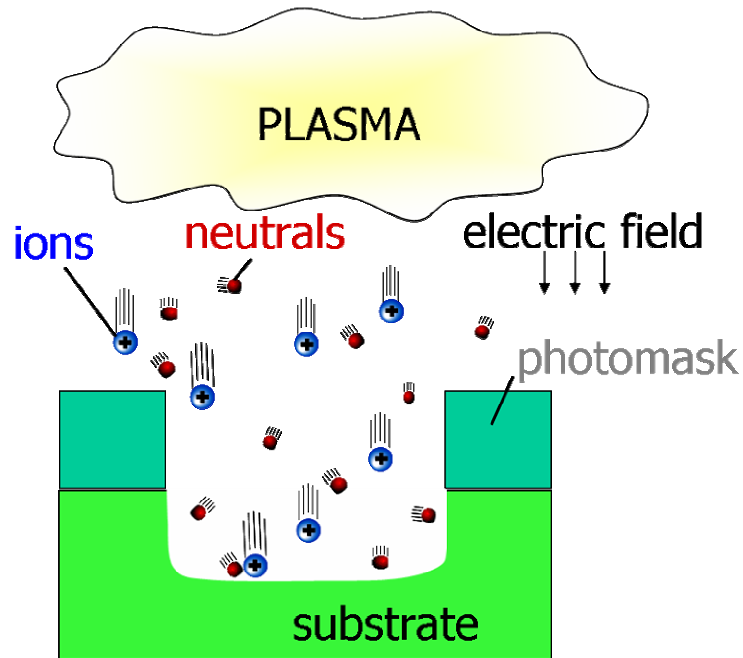


Figure 2.5. A cartoon depicting the process of physical and chemical etching that occurs during a RIE process. Ions react with the substrate surface while the neutral atoms provide additional bombardment to loosen and dislodge material [34].

Anisotropic etching capabilities of RIE allow for large aspect ratio trench fabrication as seen in Figure 2.6 [35]. The ART trenches used in this study were formed using such a technique, which was selective to SiO_2. Gases such as CF_4 plasma etch by releasing the highly reactive F atoms from their C-F bonds. Because Si-F and Ge-F bond formation is energetically favorable, the F forms bonds with those materials. This reaction results in a gas of Si-F or Ge-F which is then pumped out of the chamber while new reaction gases are continuously supplied.

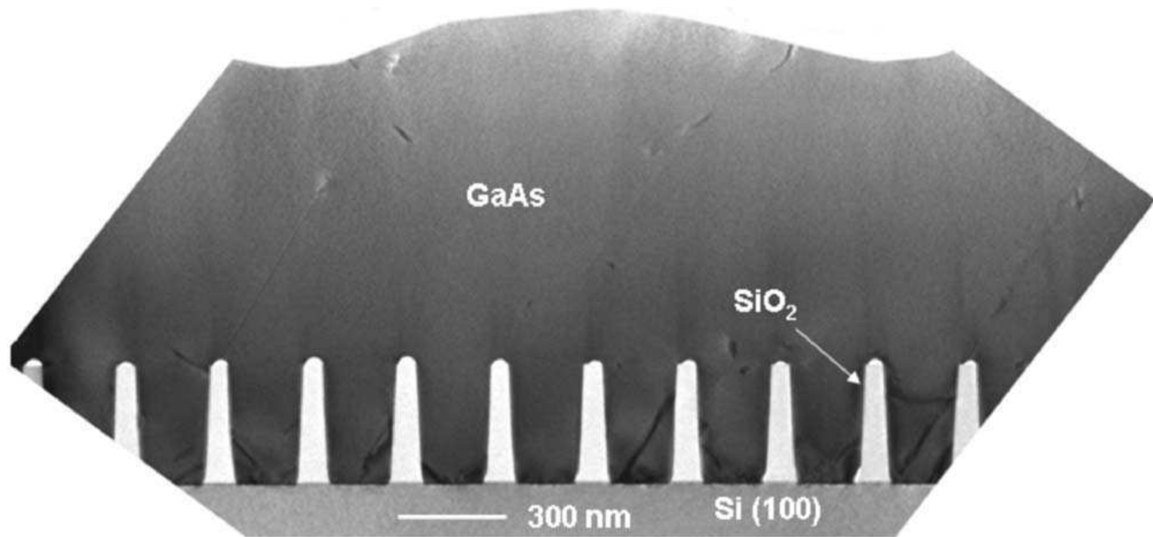


Figure 2.6. A SEM micrograph depicting the ART process for GaAs virtual substrates. The anisotropy of the RIE during trench formation is clearly demonstrated by the abrupt and flat trench floors [35].

2.6 Crystallographic wet chemical etching

Wet chemical etches often show a directional dependence and high selectivity between materials, this is witnessed in many crystal systems such as InAs, GaAs, InGaAs, InP, etc where lattice matched crystals where one semiconductor is completely inert to the solution while the other vigorously dissolves [36]. Si and Ge, too, show dependencies on etch rate based on crystal direction, and this material selectivity is used as a tool for strained sources and drains for the present technology nodes.

For Si, hot KOH chemical baths have been used for the production of MEMS for years due, in large part, to the highly selective etch of the (100) plane [1]. TMAH, like KOH, etches Si rapidly on the (100) plane, and very slowly along the (111) plane, resulting in the characteristic inverted pyramid shape seen in Figure 2.7. The TMAH reaction with Si is more energetically favorable for breaking the single Si bond holding an atom on a (100) plane instead of three bonds holding an atom on a (111) plane, this

characteristic leads to the preferential etch along the (111) facet and the telltale inverted pyramid etch pit.

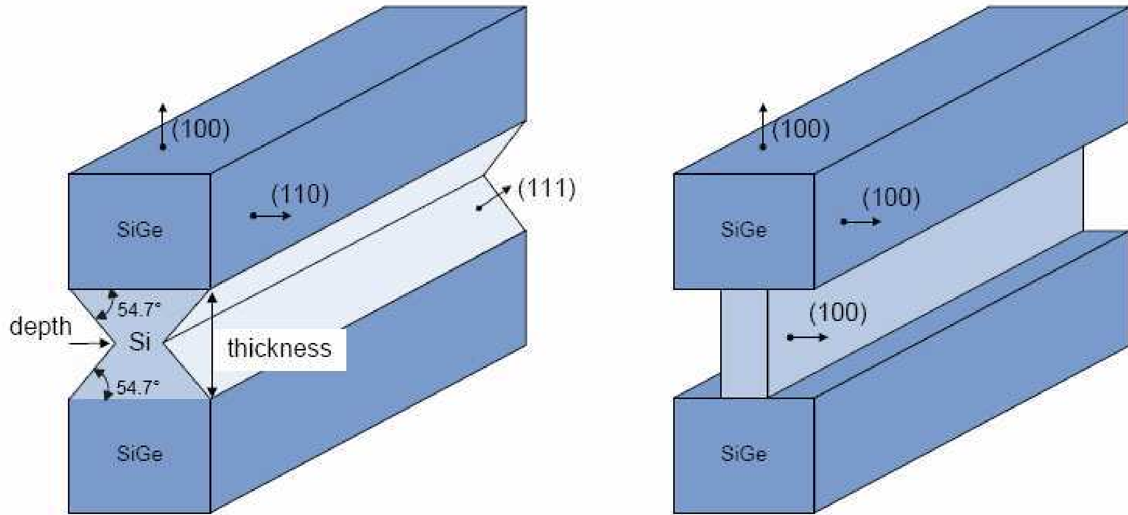


Figure 2.7. A cartoon of how TMAH preferentially etches along the (100) crystal plane, resulting in either a flat or angled etch profile depending on the orientation of substrate [1].

H_2O_2 either on its own, or in combination with several other chemicals, will etch Ge along the (111) plane in a fashion similar to that of TMAH etching of Si as depicted in Figure 2.8 [17]. The reaction is as rapid as it is because the H_2O_2, oxidizes the exterior layers of Ge in the lattice, and then these outer layers are soluble in the H_2O/ H_2O_2 solution. In principle a narrow diameter wire could be achieved by removing any side and bottom support material and then performing the H_2O_2 etch. Depending on the concentration of the H_2O_2 the etch rate will be more or less rapid.

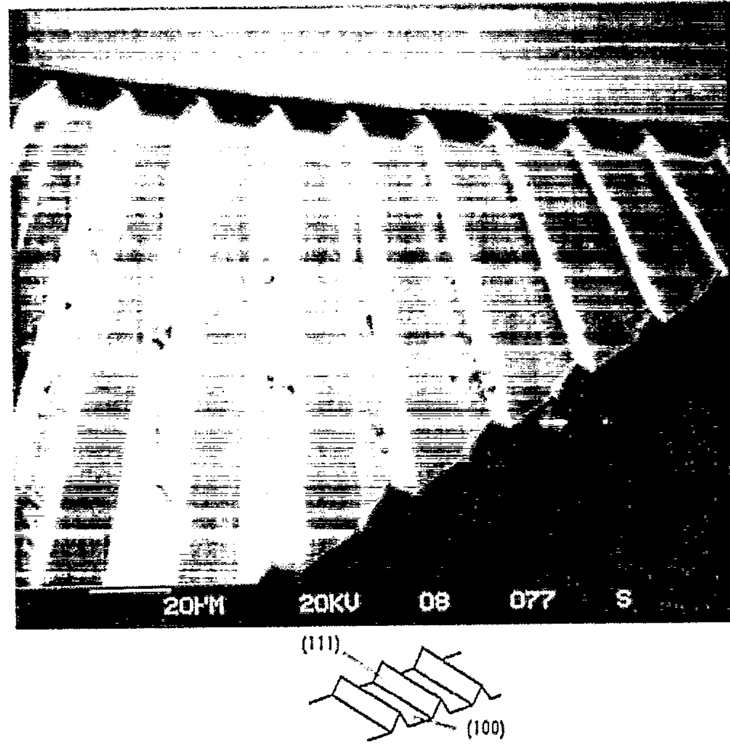


Figure 2.8. A micrograph displaying the crystallographic etching of Ge by H_2O_2 containing solutions [17].

Chapter 3

Experimental and Results

3.1 Introduction

The aforementioned processes have demonstrated the ability to create reasonably large quantities of NWs, Ge or otherwise. However, these methods have, essentially, failed a very important task, integration. Grow and dropcast processes may produce and place NWs with a limited degree of repeatability, but they lack the ability to be integrated on the starting substrate. The author proposes an alternate method, GON, for fabricating arrays of NWs on a substrate. Preliminary experiments for this process and the planned methods to create submicron NWs will be discussed in the following sections.

3.2 Preliminary experiment and results

ART wafers are an ideal test platform due to the dense Ge and SiO_2 features on each sub-die and provide excellent proof of concept tests for dry and wet chemical etch selectivity. Si etch rates in TMAH slow dramatically with increasing Ge content, thus it is surmised that Ge will not etch in a TMAH solution [7,17]. Figure 3.1 a-c demonstrates that HF, TMAH, and H_2O_2 etch only the target material at any appreciable rate, SiO_2, Si, and Ge, respectively. Ten minutes of 10:1 BOE completely removed the oxide trench walls from the sample seen in Figure 3.1-a is proof that HF only attacks the surface oxides of the Si and Ge. In Figure 3.1-b, exposed Si is subject to 30 seconds of hot TMAH providing evidence that the crystallographic etch profile of the (111) plane. Ge is seen to be unscathed by the solution. The final image in Figure 3.1-c shows how the H_2O_2 etch only etches the Ge surface and in an orientation specific manner. A follow up

experiment of 90 seconds in TMAH at 70 ºC, was sufficient to delaminate Ge lines from the Si surface as shown in Figure 3.2.

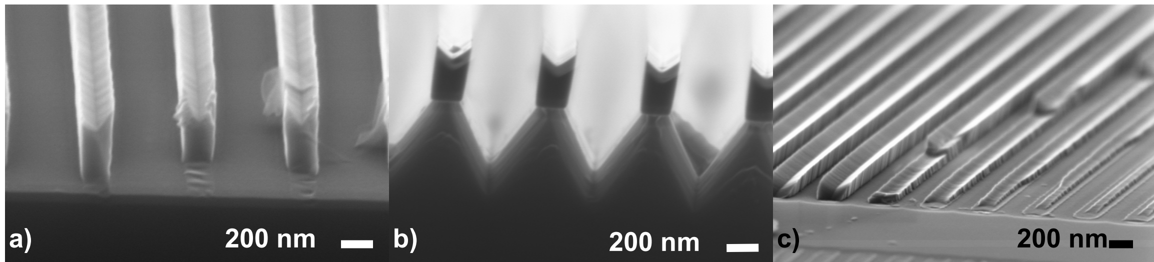


Figure 3.1. (a) 10 minutes of BOE removed all SiO_2, but Si and Ge remain intact. (b) 30 seconds in TMAH at 70 ºC have etched Si between Ge columns to the (111) plane. (c) H_2O_2 etches Ge only, leaving some residual SiGe from alloying during Ge growth.

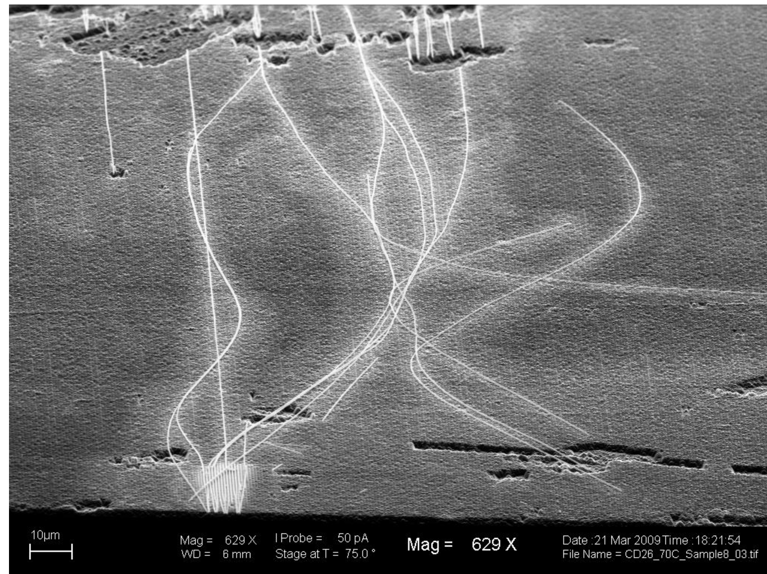


Figure 3.2. 90 seconds of hot TMAH etching will delaminate unsupported Ge wires. Therefore, some oxide must remain to act as an etch mask so as to anchor the Ge to the substrate.

Figure 3.3 a-h shows a cartoon of the process flow for achieving suspended Ge NWs. Combining these etches with contact lithography and 1813 resist as an etch mask demonstrates the proof of concept structure as displayed in Figure 3.4 a and b. Despite the success of the initial test pattern, undercut due to wet etching poses a potential

problem for suspended lengths below 3 μm. Suspension lengths longer than 4 μm also suffer from bowing, which is hypothesized to be due to electrostatic forces due to the attraction between wires and the substrate. Gravity on such a small object is going to be negligible, and would be insufficient to cause the lattice to stretch significantly.

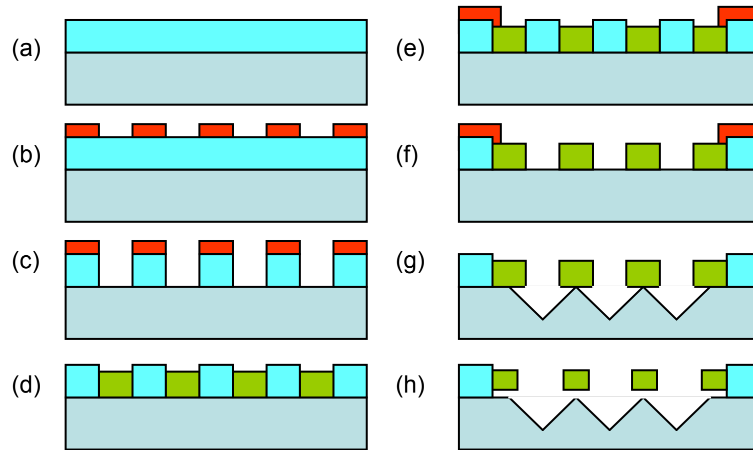


Figure 3.3. GON fabrication process flow. (a) Wet thermal oxide grown to sufficient height for dislocation defect reduction, roughly 2.5 times as tall as the trench is wide [15, 37]. (b) Pattern Ge growth locations. (c) RIE of oxide for high aspect ratio trenches. (d) Epitaxial Ge growth in oxide trenches. (e) Pattern GON NW array locations. (f) BOE removal of excess oxide. (g) TMAH etch of Si for initial Ge release. (h) H_2O_2 etch for final GON NW diameter.

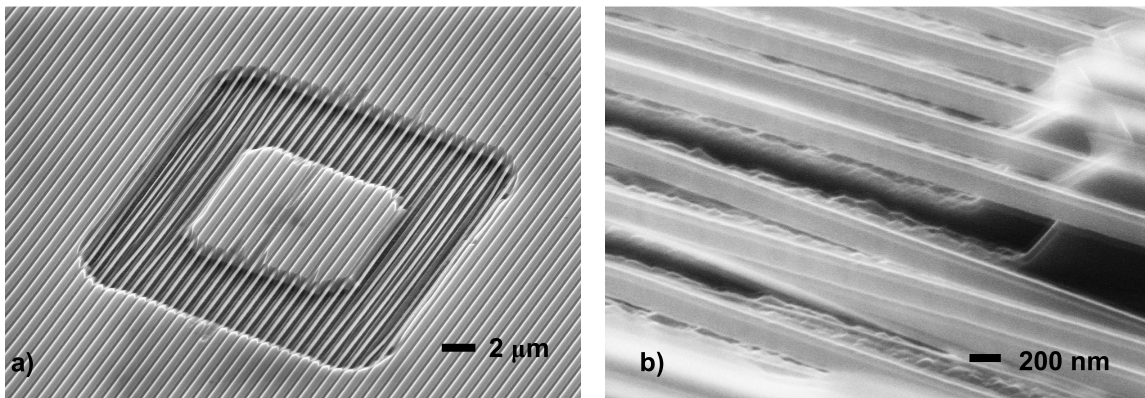


Figure 3.4 (a) SEM micrograph of 4 μm GON NW array fabricated via selective wet chemical etching and contact lithography. (b) Tilted view of GON NW array, portraying a suspension height of roughly 300 nm above the Si substrate and bending of the longest wires.

3.3 E-beam lithography defined suspension experiment 1

Following the success of the preliminary experiments, assumptions were made as to the performance of the E-beam resist processing and the ease of processing. The PMMA/LOR 5A film stack was formed following the steps in Table 3.1, with detailed steps in Appendix A. However, several problems associated with the processing steps developed. Undercutting of the resist for mesa formation appeared as a critical issue as shown in Figures 3.5 and 3.6.

Table 3.1. Preliminary E-beam processing for GON NW processing

Process Flow	
1)	Clean sample surface with Isopropyl Alcohol.
2)	Coat and spin with LOR 5A and PMMA 955 A4.
3)	Drive off solvents for 10 minutes at 180 ºC on a hot plate.
4)	E-beam write
5)	Develop
6)	HF etch the oxide for 5 minutes to expose the Si below.
7)	Peroxide etch to thin Ge for 3 minutes.
8)	TMAH etch the exposed Si for 3 minutes to eliminate resist and create GON wires.

As shown in Figure 3.5, there was an undercut during the HF and CD-26 processing of the sample that lead to the failure to attain the desired suspension length of 10 μm. HF and TMAH appear to travel deeper than anticipated under the PMMA/LOR 5A system and lead to a near contact between the two pad regions. Undercut is most apparent in the direction of the ART lines, which hints that the undercut problems are due to chemistry creeping down the channels and facilitating undercuts greater than are typical for homogenous surfaces. Following a H_2O_2 dip for 60 s, the edges of the pattern are apparent in Figure 3.6. Also apparent from Figure 3.6 are the striations as each step cut further below the resist stack, leading to a final under cut of almost 10 μm. Lateral

undercuts, such as those shown in the images, are unacceptable for suspension formation, as the final result could be almost three times the designed suspension length.

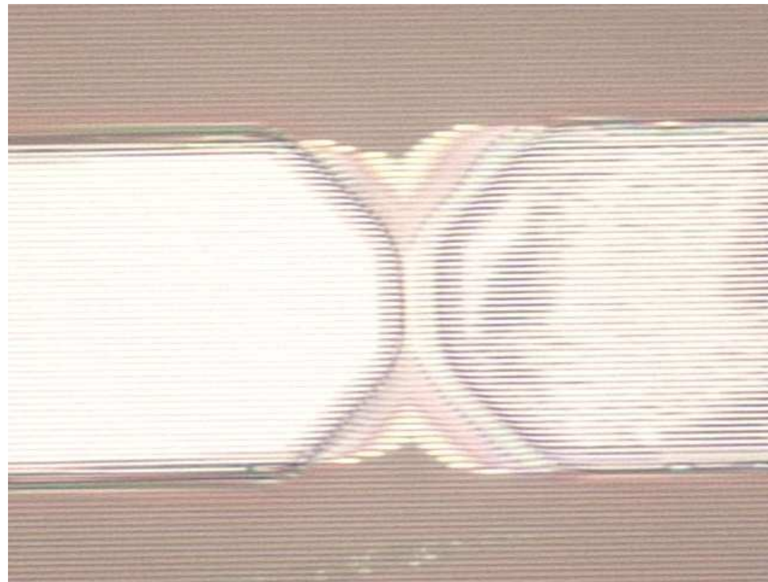


Figure 3.5. Post TMAH etch, the undercut of both the HF and TMAH is quite apparent. The PMMA is practically suspended which, while practical for MEMS, is unacceptable for use as an etch mask or lift off processing.

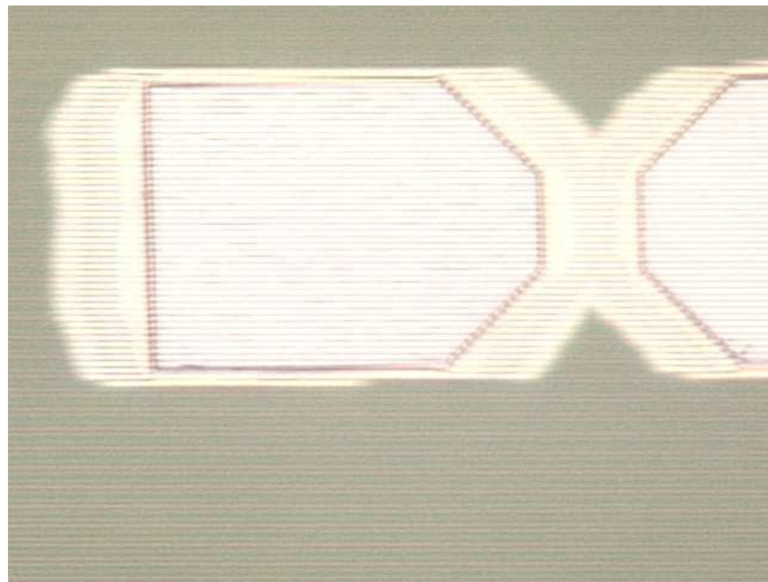


Figure 3.6. Following the peroxide etch, the undercut for each of the processing steps is quite apparent. The photoresist failed to protect the masked regions as had been anticipated.

Due to the poor masking of the ART substrate by the PMMA/LOR stack an additional attempt to avoid preprocessing of the sample was attempted utilizing a BOE bath with surfactant of a 16:3:3 composition. With a premise being that the alternative solution would not have as drastic an undercut and may leave the mask intact. Resulting in Figure 3.7 this was not, at all, the case for the HF with surfactant. Alternative steps actually stripped the resist stack from the surface within 180 s of process time, leaving the folded and/or delaminated film on the sample surface once dried. Clearly, utilizing the HF bath with surfactant should be avoided for PMMA/LOR 5A systems if reasonably good results are desired.

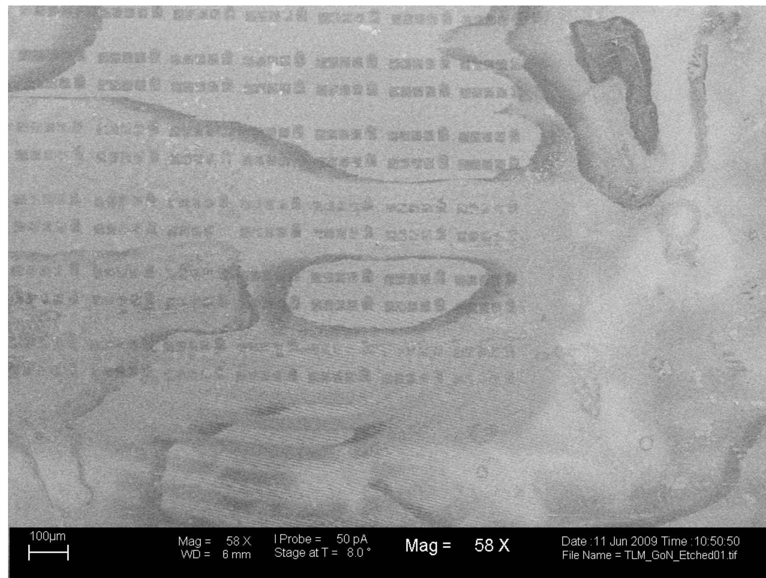


Figure 3.7. HF with surfactant has a negative impact on the film stack, as some portions fold back or form bubbles over the ART surface.

3.4 E-beam lithography defined suspension experiment 2

3.4.1 Positive and negative E-beam resists under RIE conditions

Due to the problems that arose from wet etching and E-beam lithography, an approach utilizing a dry etch in the DryTek Quad or TRION would be necessary to achieve the desired result of narrow suspension lengths. Conditions similar to those

commonly used for student labs were initially chosen, based on the ability of the etch recipes to remove SiO_2 and Si while leaving the masking resist stack largely intact. Etch process 1 from the DryTek is defined in Table 3.2 below. CHF_3 gas utilized in this etch is widely known to be more benign with respect to photoresist etching, while the Ar provides some additional physical bombardment to help create higher aspect ratio holes in the resist openings. 75 W of power and 70 mTorr of pressure were chosen to ensure reduced etch rates of the photoresist while maintaining reasonable etch rates for the SiO_2.

Table 3.2. Drytek etch process 1 was the first attempt to combine E-beam lithography with a RIE.

Parameter	CF_4 (sccm)	CHF_3 (sccm)	O_2 (sccm)	Ar (sccm)	Power (W)	Pressure (mTorr)	Time (s)
Condition	0	65	0	25	75	70	300

3.4.2 Results from positive and negative E-beam resists under RIE conditions

Ideally, the etch profile is even across an entire opening and both Ge and SiO_2 etch at the same rate under the process conditions, or the Ge would even not etch at all. However, etch process 1 appears to remove additional material near the sidewalls of the resist mask. A deeper etch near the wall, likely due to longer dwell times for the etching gases near the corners because the wide spaces have lower confinement of the gas near the edges of the pattern as seen in Figure 3.8. An etch rate in the range of 10 to 15 Å per second was observed utilizing a Si dummy piece.

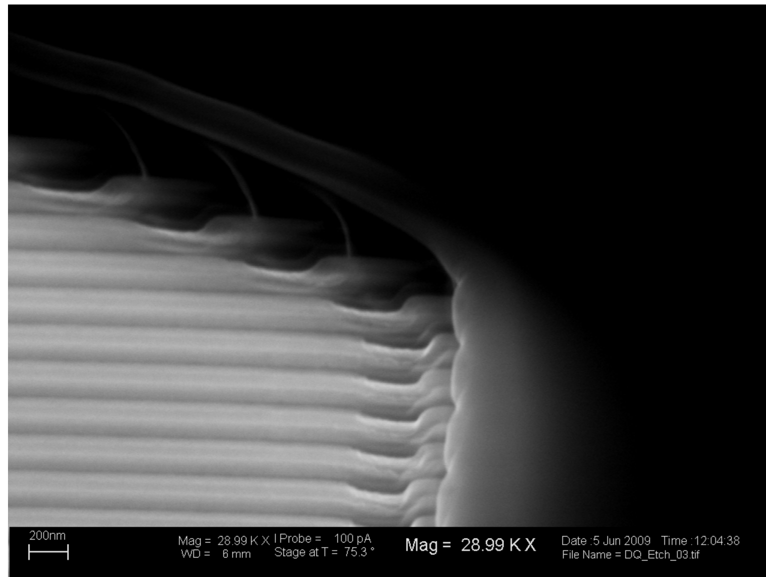


Figure 3.8. RIE etching in the Drytek Quad using CHF_3 etched Ge at a greater rate than SiO_2. In addition, the greater material removal rates at the edges can also be seen.

A negative resist, nLOF, is briefly investigated in this experiment, however the results and processing requirements were not sufficient to warrant further study. nLOF proved to develop more evenly along the entirety of the exposed region as seen in Figure 3.9. Unfortunately, this negative resist also requires significantly larger doses (only the largest dose at 900 nC/cm^2 resolved) and, thus, is not be ideal for the other experiments in this study.

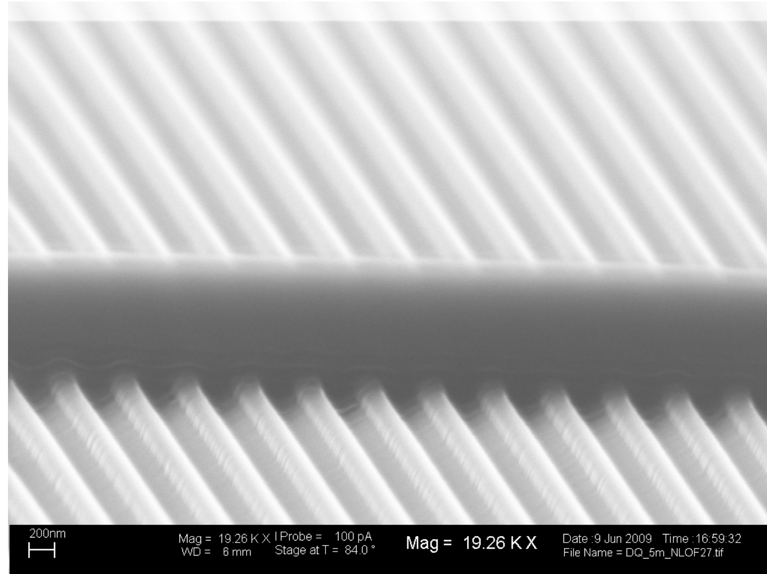


Figure 3.9. An etch profile following etch condition 1 for nLOF. Unlike the PMMA/LOR5A sample, a greater etch rate along the mask defined edges was not observed.

3.5 E-beam lithography defined suspension experiment 3

3.5.1 Samples 0609A and 0609B, an experiment with film stack and etch time

Samples 0609A and 0609B are obtained from wafer E03644.5 which produced the previous samples. Piece 0609A has the same PMMA/LOR5A film stack used in previous experiments utilizing EBL. Though, 0609B is coated with PMMA only. Both samples are surface cleaned with IPA and dried prior to coating. Following EBL and develop, a 300 s chamber seasoning is added to the etch procedure, though the conditions qre, otherwise, equivalent to etch process 1. The 180 nm 3:1 SiO_2 to Ge ART die are used, as this sub die is the easiest to undercut Ge lines since more Si is after SiO_2 removal.

3.5.2 Results from samples 0609A and 0609B

Previous experiments etched in the Drytek Quad RIE system. However, some issues and inconveniences drove the study to the TRION etcher which had just been

brought online. Because the Drytek Quad has longer load lock pump down times, and samples have, repeatedly, blown off the carrier wafer due to chamber pressure differences, moving to a different system may alleviate these problems. However, the Drytek does have more gases available and wider range of power and pressure settings for the chamber during etch, but such decisions must sometimes be made to make progress. Further RIE processing will move to the TRION system, which doesn't blow sample pieces off of the carrier wafer and will allow faster processing due to the significantly shorter load lock pump down period. Samples 0609A and 0609B were written and developed (120 s MIBK:IPA 1:3, 90 s CD26:H_2O 1:1). TRION etch process 2 and then cleaved into additional pieces for further processing and observation in the SEM. Table 3.3 lists the etch conditions which had to vary from the initial work on the Drytek due to differences between the controllers on both pieces of equipment.

Table 3.3. Etch process 2 differed from etch process 1 due to equipment differences.

Sample	CF_4 (sccm)	CHF_3 (sccm)	O_2 (sccm)	Ar (sccm)	Power (W)	Pressure (mTorr)	Time (s)
0609A	0	65	0	25	75	85	300
0609B-1	0	65	0	25	75	85	600
0609B-2	0	65	0	25	75	85	1200

Sample 0609A-1 was first observed and regions with a lower dose produced suspended PMMA bridges following the RIE as seen in Figure 3.10. Figure 3.11 displays the typical etch result for the higher dosed PMMA/LOR5A regions.

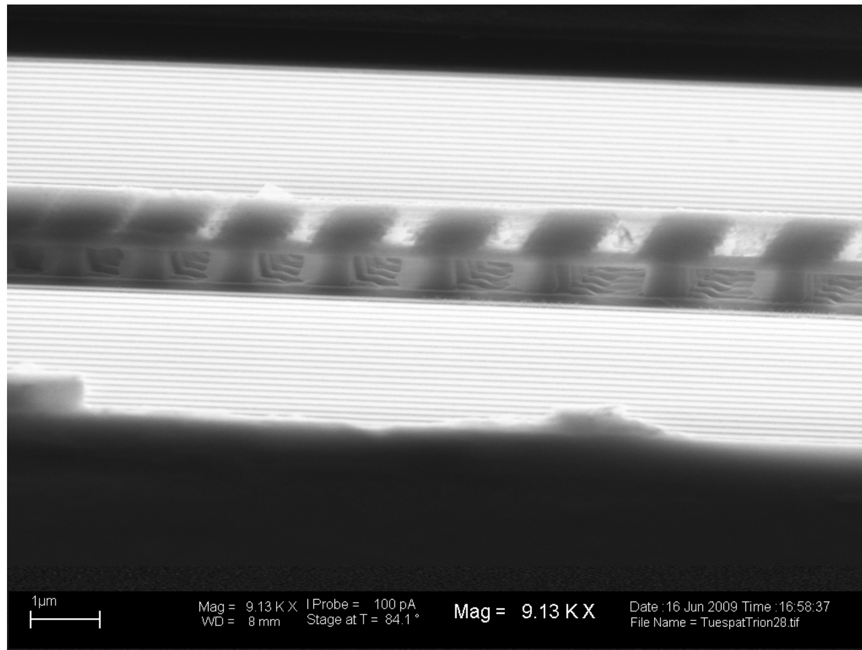


Figure 3.10. Following etching in the TRION for 5 minutes in CHF_3, the low doses near the edge lead to undeveloped PMMA and the interesting "film" structure. The edge RIE effects can be seen between the support columns of LOR5A indicating that etch gases dwelled longer in those regions.

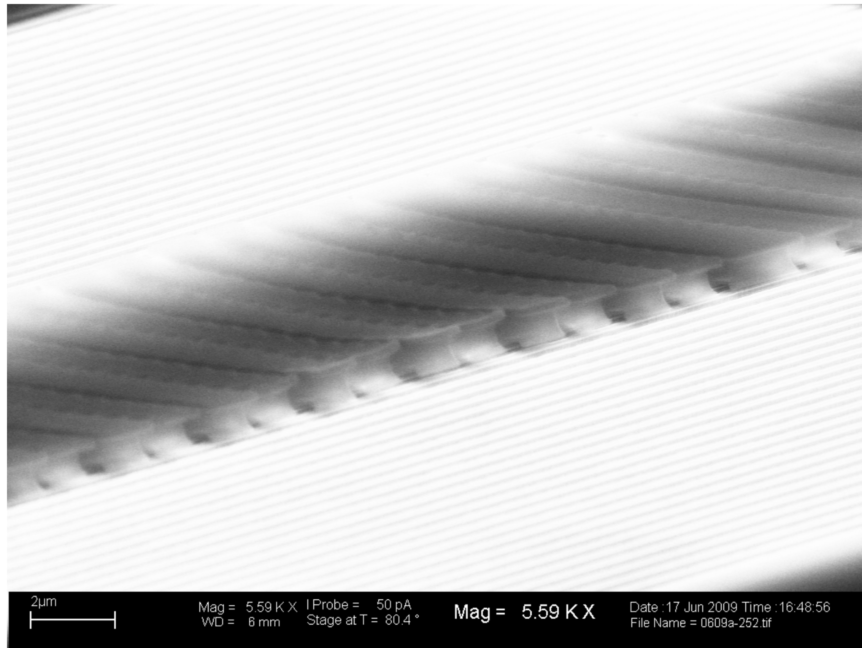


Figure 3.11. Following etching in the TRION for 5 minutes in CHF_3, the oxide and Ge in the exposed areas are largely removed, though to a lesser extent than was evident in the Drytek.

The PMMA only sample, 0609B, did have openings over the oxide, but there appeared to be a change in the dose that was actually received as small holes were attained instead of the wide openings that were expected. Figure 3.12 shows the openings made in the PMMA. The variance in dose may be related to a change in the beam current as many of the fine details for EBL with this system were unknown at the time of the experiment. Effects from variables such as the beam wobble and centering the beam power had not been fully pursued at this period of EBL development and, as such, the beam current would sometimes drop as much as 30% from the initial measured current. Sample 0609B-1 etched for 10 minutes to test the resilience of the PMMA resist.

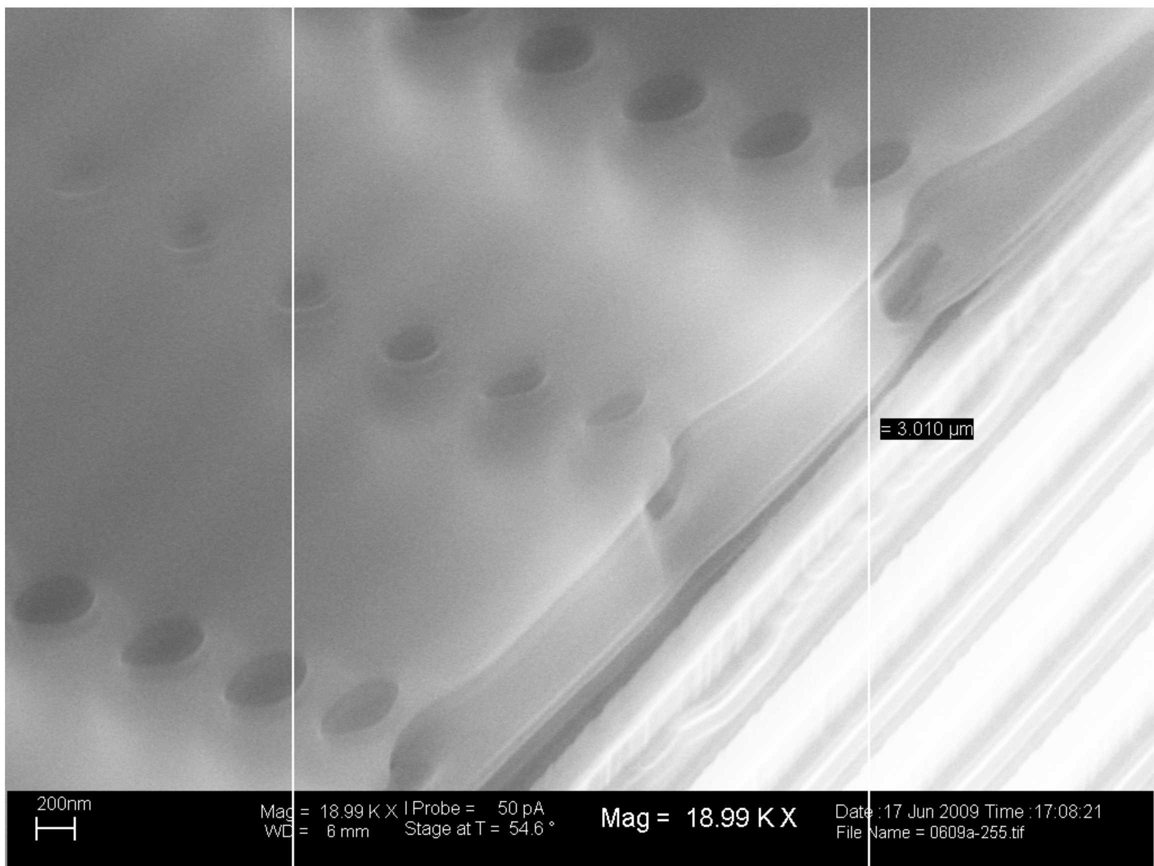


Figure 3.12. Following etching in the TRION for 10 minutes in CHF_3, the oxide and Ge in the exposed areas are largely removed, though to a lesser extent than was evident in the Drytek.

Resist loss is approximately 300 Å for 10 minutes of TRION etch, sample 0609B-2 was etched for an additional 20 minutes under the same conditions to determine the resilience of the resist stack to RIE. The expected result was significant photoresist loss coupled with deep etch pits in the Ge/SiO_2 exposed regions. However, as seen in Figure 3.13, the etch process produced "grass," or redeposited some form of polymer on the sample surface, seemingly after all the photoresist had been etched away.

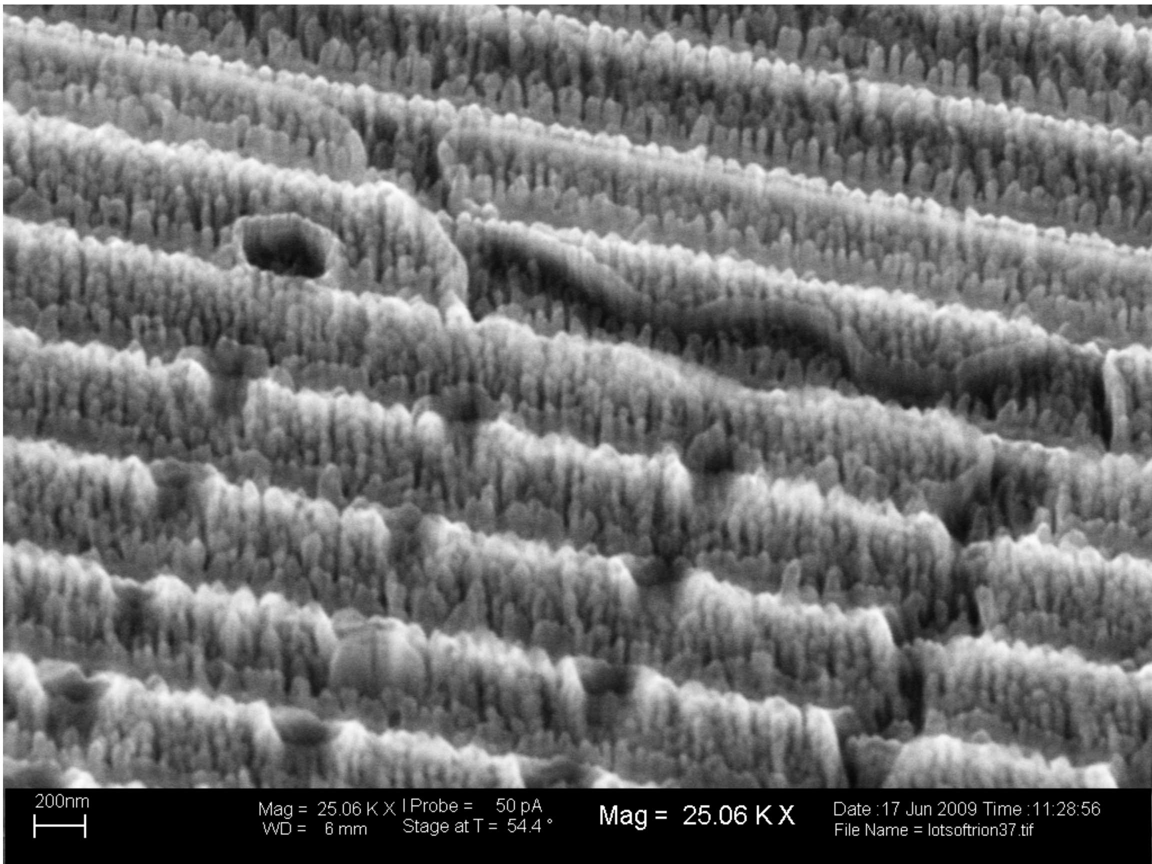


Figure 3.13. Following etching in the TRION for 20 minutes in CHF_3, the oxide and Ge in the exposed areas are largely removed, though a large amount of "grass" from redeposited polymers have also been formed creating an interesting, but useless, surface.

Following initial observation of sample 0609A-1, 0609A-2 was processed in accordance with previous suspension work and analyzed with optical microscopy to determine if the procedure had been successful in suspending the largest features.

0609A-2 was first placed into the 10:1 BOE bath, to remove SiO_2 in the unmasked regions, for 300 s. Sample 0609A-2 then etched in a CD-26 etch bath at 70ºC for 60 s to undercut the Ge lines. Followed by imersion in room temperature H_2O_2 for 60 s reduces the wire diameter to 120 nm from 180 nm. The sample was then subject to a second heated CD-26 etch, where the PMMA lifted off. Viewing the sample in the SEM in Figure 3.14, and it appeared that the SiO_2 had not been fully removed as there was no apparent etching of the unmasked regions.

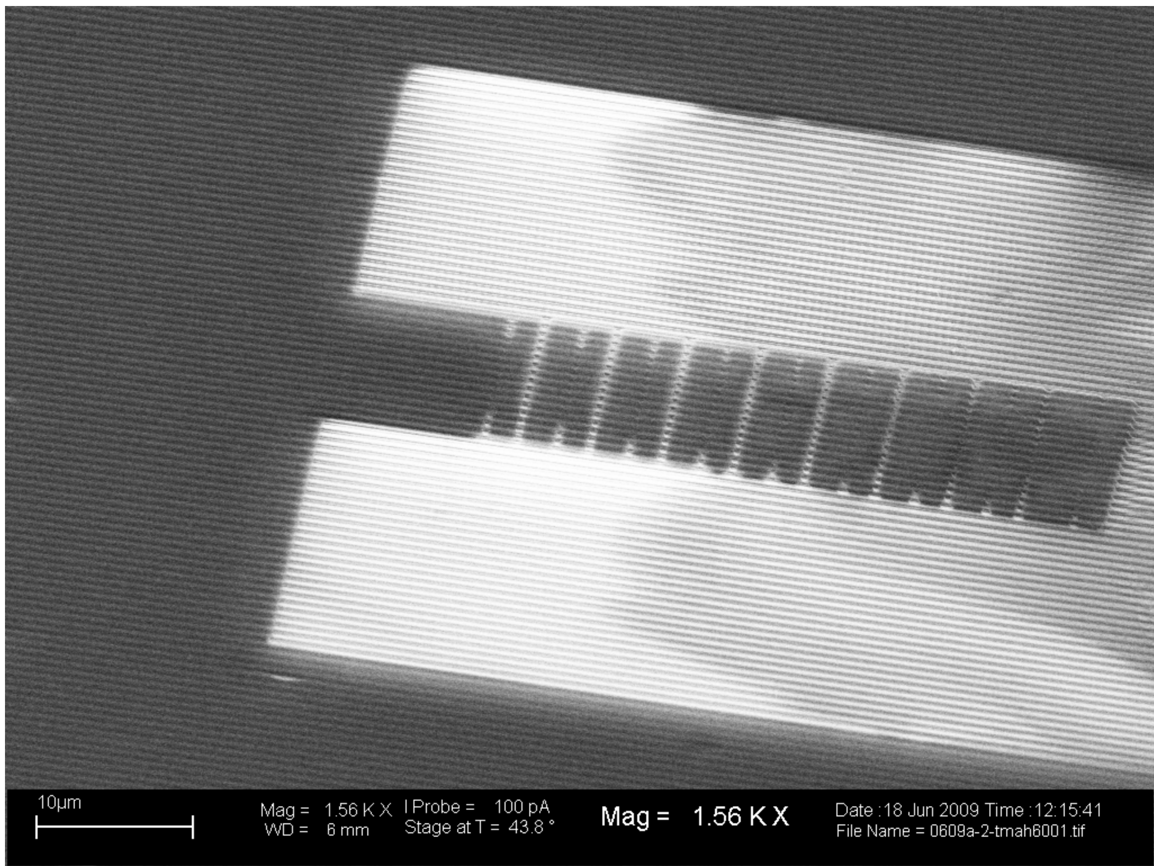


Figure 3.14. Following etching 300 s of oxide SiO_2, 240 s of TMAH etching, and 120 s of H_2O_2 etching, the Ge lines did not appear to be suspended as anticipated.

Because the oxide had not been removed as thought, the sample was again placed in HF for 30 s followed by an additional 60 s of H_2O_2 etching. 0609A-2 was then subject

to an additional 60 s of HF etching because there appeared to be no change in the sample optically. HF etching followed by an additional 180 s of heated TMAH etching, produced some Si etch patterns between the features. An additional 60 s of HF etching, there still seemed to be some SiO_2 remaining as shown in Figure 3.15, and a final 300 s of HF etching was performed to remove all the remaining SiO_2.

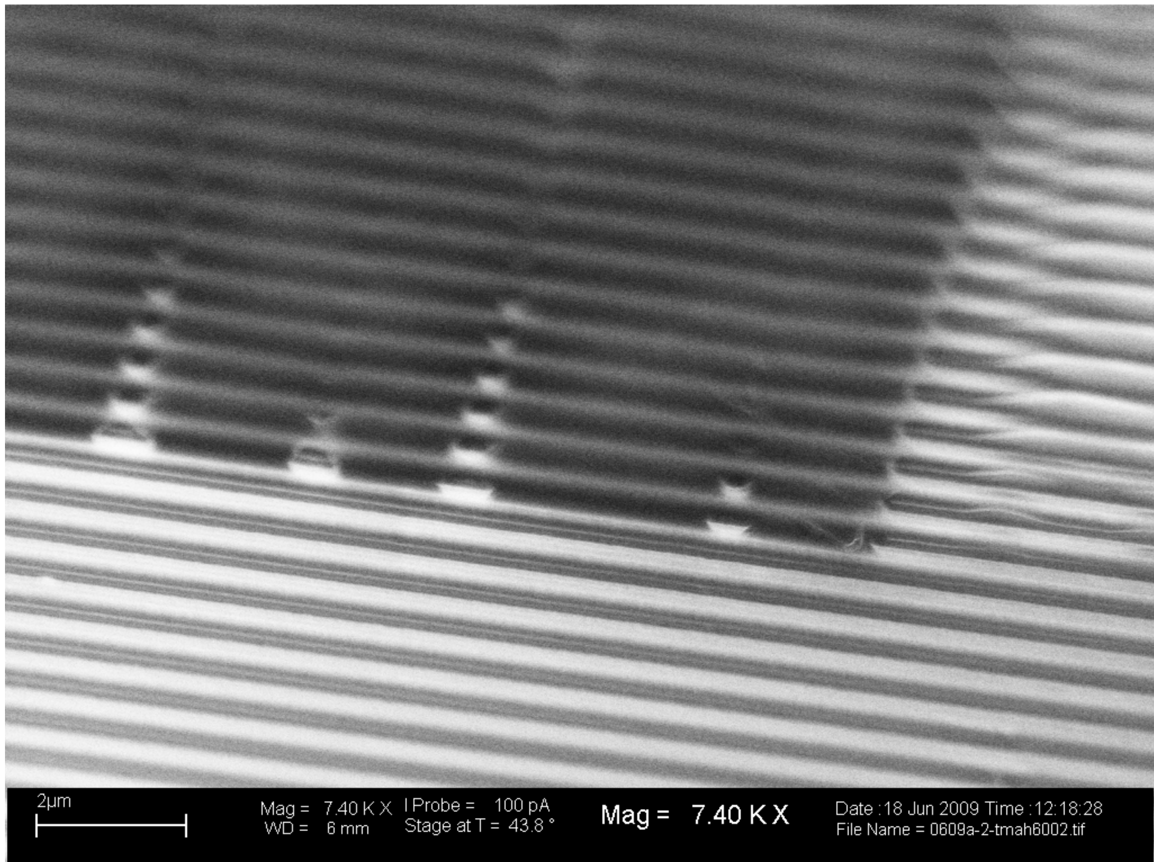


Figure 3.15. 120 s of HF etching combined with 180 additional seconds of TMAH etching seemed to produce suspended wires, though not in the organized manner as had been sought.

The end result of the entire etch process can be seen in Figure 3.16 a and b. Narrow Ge suspensions over an air gap were attained; however the process flow for these suspensions was not, at all, optimal. Ge wires as narrow as 50 nm in diameter and 200 nm in length were observed on 0609A-2, as were additional longer length suspensions up

to 1 μm in the regions defined for suspension. The regions surrounding the suspension regions had deep etch pits and wires contacting the floor of those pits. Because the SiO_2 had not been completely removed by HF, H_2O_2 opened up small holes to the Si substrate below. These holes undercut the Ge lines and allowed TMAH etching of the underlying Si. The second H_2O_2 etch was able to attack all sides of the suspended Ge creating the narrow bridge Ge in Figure 3.16 b. A summary of the process steps for 0609A-2 is listed in Table 3.4. This process provided the desired result of narrow, suspended Ge lines, but not in particularly useful manner.

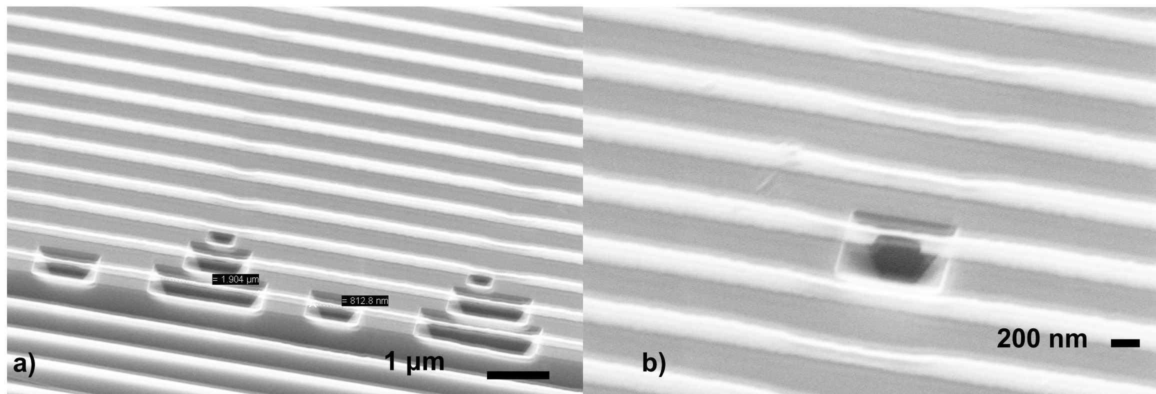


Figure 3.16 a. Pattern transfer of lines and spaces from combinations of dry and wet etching with EBL must be optimized. b. EBL combined with dry etching created a 200 nm long by 50 nm diameter NW demonstrating significantly smaller features than those by contact lithography and wet etching alone.

Table 3.4. Process steps for 0609A-2.

Step	Process	Time (s)	Step	Process	Time (s)	Step	Process	Time(s)
1	MIBK	120	6	Si etch	120	11	SiO_2 etch	60
2	CD26/DI	90	7	SEM	--	12	Si etch	180
3	SiO_2 etch	300	8	SiO_2 etch	30	13	SiO_2 etch	60
4	Si etch	120	9	Ge etch	60	14	SEM	--
5	Ge etch	60	10	SiO_2 etch	60	15	SiO_2 etch	300

3.6 Experiment 4, partial oxide removal versus complete oxide removal

3.6.1 Sample 0709A and 0709B experiment plan

Significant undercutting of the photo resist by HF must be assessed. An experiment utilizing samples 0709A and 0709B from substrate E03644.5 will determine if removing the SiO_2 and relying on PMMA to form a mask or if partially removing the oxide and following with a dry etch after develop could provide successful GON results. 0709A is to be stripped of oxide with a 480 s etch where sample 0709B is to have a 300 s etch to leave a thin SiO_2 layer that will quickly etch unmasked regions during a dry etch. Because the LOR5A is soluble in hot TMAH, only a PMMA layer was spun onto the sample surfaces.

3.6.2 Sample 0709A and 0709B results

Processing for sample 0709A proceeded according to the plan, 480 s of HF exposure was to remove all the oxide between ART lines. Both samples 0709A and 0709B had ~2500 Å of PMMA spun onto the surface. 120 s of TMAH at 70 ºC was used to etch the unmasked Si on the substrate surface. The sample yielded some suspended regions that were larger than had been defined in the write and develop as seen in Figure 3.17. The original oxide thickness for sample 0709B was measured on a nanospec and found to be roughly 4100 Å. Sample 0709B was then etched for 5 minutes in the BOE acid bath and remeasured on the nanospec, the oxide thickness was found to range between 180 and 280 Å. 0709B had etch process 4, summarized in Table 3.5, to thin the oxide following a global oxide wet etch.

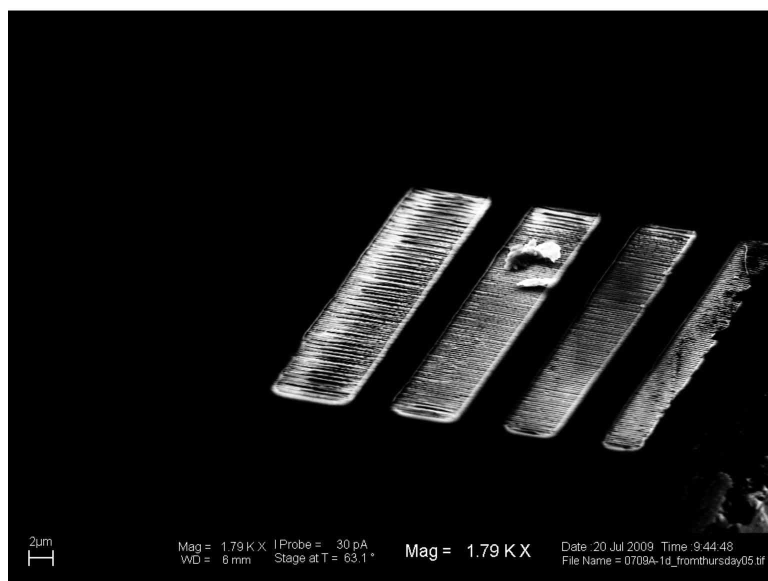


Figure 3.17 Pattern transfer occurred, but because the oxide had been removed globally, a significant amount of Ge had demlaminated in other regions.

Table 3.5. Etch process 4 included an ash to remove some of the photo resist covering the sample.

Step	CF_4 (sccm)	CHF_3 (sccm)	O_2 (sccm)	Ar (sccm)	Power (W)	Pressure (mTorr)	Time (s)
1	40	0	0	0	175	150	45
2	0	0	60	0	150	150	10

Processing sample 0709B removed more Ge than anticipated and produced few suspended wires. SiO_2 etching was insufficient and Ge etching was more vigorous than in earlier experiments, possibly due to a fresh bottle of H_2O_2. In Figure 3.18 the crystallographic etching appears to have begun in some regions, but has terminated prior to releasing the Ge, and more oxide appears to be present than had been expected. The sample was cleaved across a defined opening, mounted, and imaged in the SEM. The micrograph in Figure 3.19 presents evidence that all the oxide had not been removed by the combination of RIE and HF etching, and hints that the oxide does not etch down into the trenches in the planar pattern that was expected.

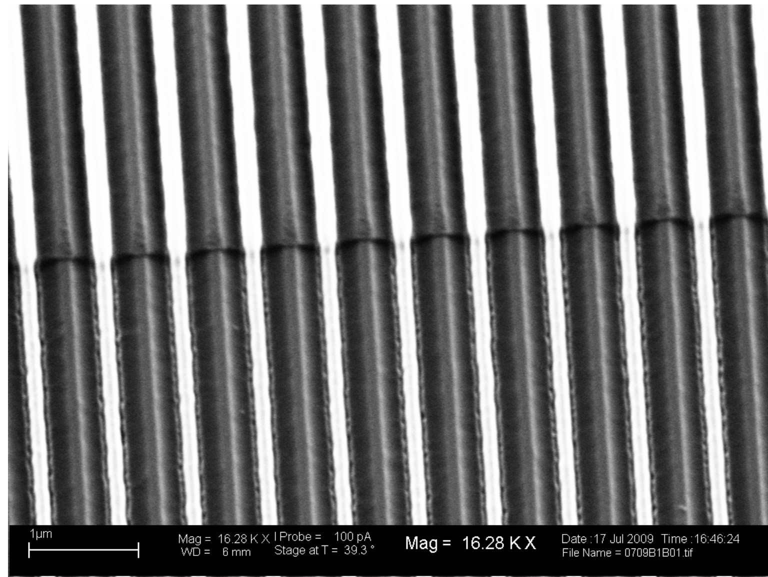


Figure 3.18. RIE and peroxide have etched Ge more than expected, and TMAH etching was unable to release Ge lines due to SiO_2 masking.

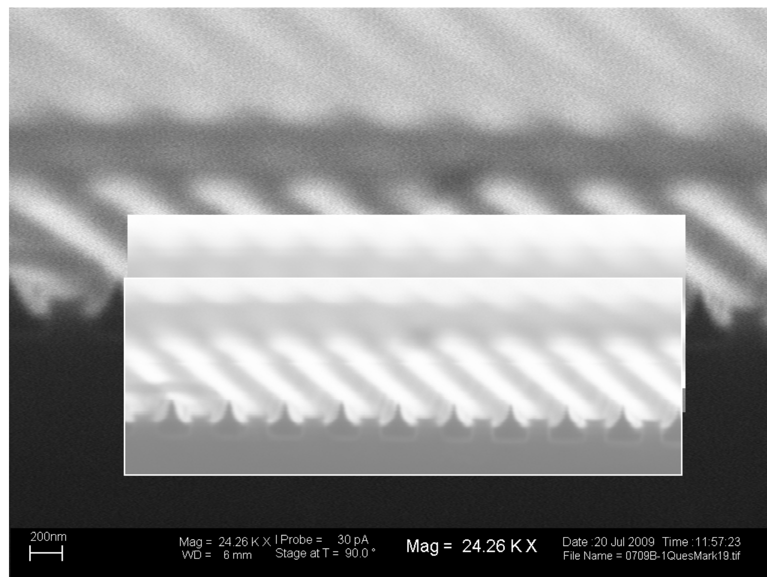


Figure 3.19. 0709B at a 90º tilt, the SiO_2 etched in a “Hershey Kiss” pattern. Almost a mirror of sidewall spacer formation, this indicates the sample may not be coplanar as thought.

3.7 Experiment 5, Determination of etch pattern of oxide.

3.7.1 Sample experiment plan

The failure of previous samples to suspend properly seems to relate to an incomplete removal of the oxide mask between Ge lines with only 300 s of HF etching and the inability of PMMA to completely mask the sample when all of the oxide has been removed. Because of this problem, samples 0709C through 0709G were taken from substrate E03644.5 to determine the amount of HF etching required to leave a thin masking oxide that could be removed via a RIE. The etch matrix with varying etch times is listed in Table 3.6. Following the HF etch bath the samples were to be exposed to heated TMAH for 60 s to determine if enough of the masking oxide had been removed between lines to allow Si etching to proceed.

Table 3.6. Etching times in HF for samples 0709C through 0709G

Sample	HF Etch Time (seconds)
0709C	0
0709D	360
0709E	480
0709F	600
0709G	420

3.7.2 SiO_2 etching results

Samples were etched according to plan, with the exception of 0709D which was accidentally etched for 480 s in HF because of an error in operating the timer on the wet bench. Sample 0709E was etched for 480 s in HF and 60 s in heated TMAH, enough of the masking SiO_2 was removed around the line edges, but not between sub-die, to allow for some Si etching to occur as seen in Figure 3.20. 60 s of HF etching removed sufficient oxide to allow significant Si etching between Ge lines.

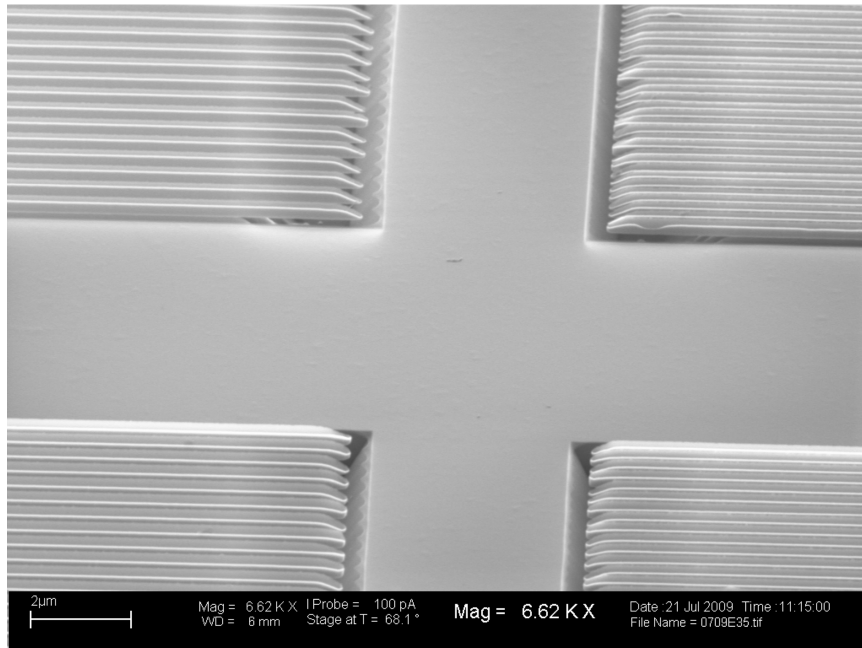


Figure 3.20. The 8 minutes of HF etching of sample 0709E opened tiny windows for the TMAH to attack the Si around the perimeter of the wires. This etch profile provides some evidence for a nonplanar etch of the SiO_2 and reaffirms that high selectivity of TMAH for Si over oxide and Ge.

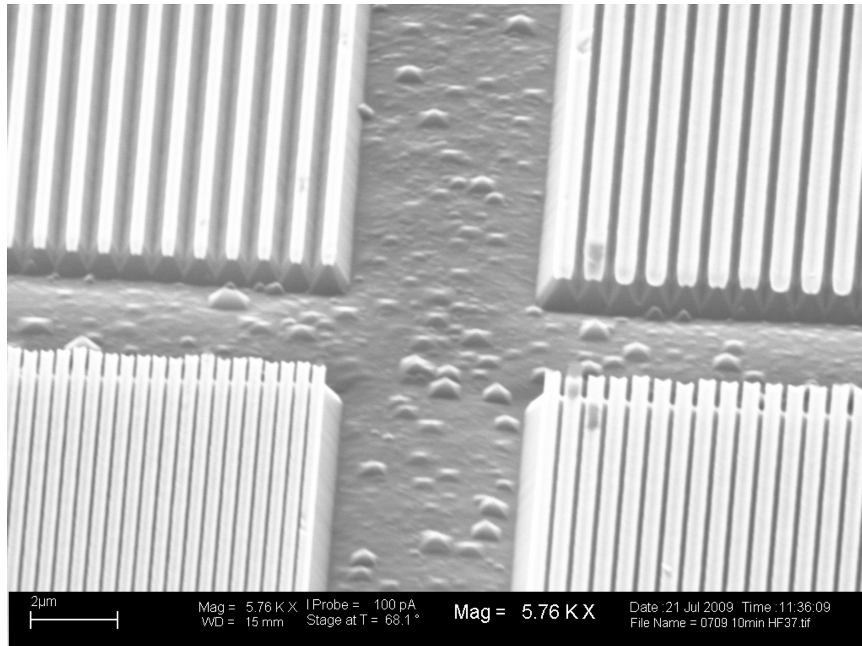


Figure 3.21. 10 minutes of HF etching of 0709F completely removes the protective SiO2 from the streets between sub-die and between Ge lines as evidenced by the crystallographic etch pattern.

Provided the knowledge that 480 s seemed to be just enough etch time, samples 0709D and 0709G, 480 s and 420 s of etching respectfully, were cleaved into two pieces for an additional etching study comparing wet etching and dry etching results. The plan laid out in Table 3.7, has enough wet etch time to remove the remaining SiO_2 and a, supposedly, conservative dry etch time. Wet etching appeared to undercut more than anticipated, as the suspension lengths were longer than designed. The Ge lines for both the RIE and wet etch of 0709D delaminated during the 120 s Si etch step, and the effects can be seen in Figure 3.22.

Table 3.7. Etch type and times for samples 0709D through 0709G

Sample	Etch Type	Etch Time (seconds)
0709D-1	HF	120
0709D-2	CF_4 RIE	120
0709G-1	HF	180
0709G-2	CF_4 RIE	120

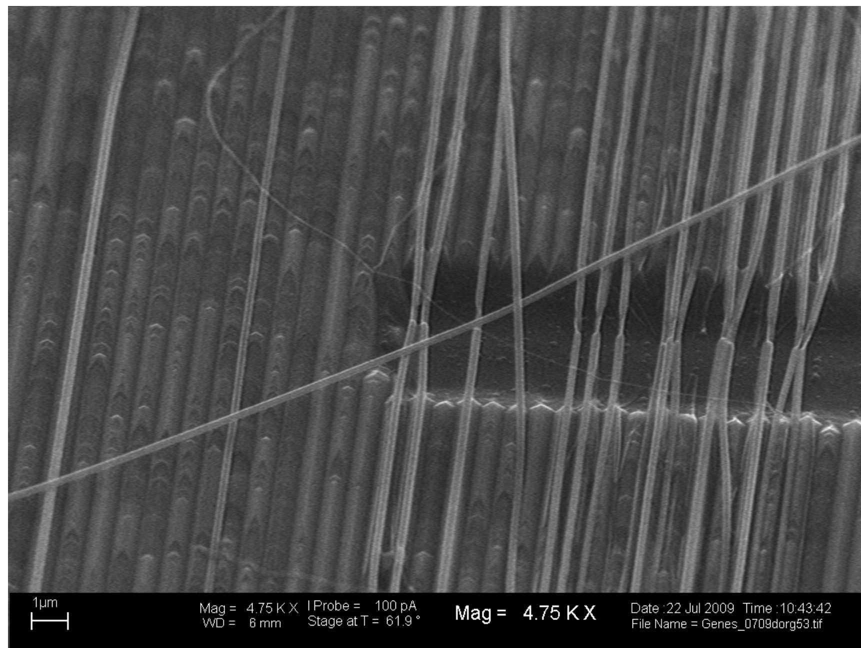


Figure 3.22. An example of the effects of the processing steps on sample 0709D, this micrograph is the RIE sample, because of the central thinned regions on the Ge lines.

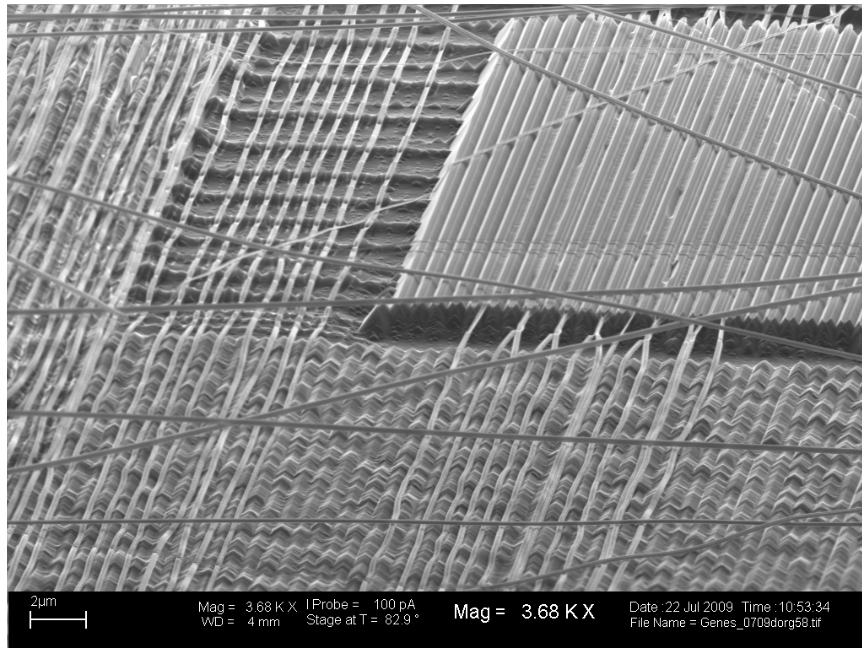


Figure 3.23. Sample 0709D-1 following the wet etch in HF and then TMAH, the SiO_2 was too thin in many locations leading to collapsed Ge lines on the Si substrate surface.

Samples undergoing wet etch did see similar undercutting as had been seen with previous samples. Despite being from different samples, Figures 3.24 and 3.25 show similar effects of undercutting for 0709D and 0709G. SiO_2 etching under the photoresist indicates that the HF is progressing rapidly between the Ge lines. Regions in direct contact with the etch pit show the undercutting of the HF during the oxide etch, such a pattern indicates that the HF is somehow accessing the substrate surface despite the presence of the PMMA. The manner in which the undercutting is occurring indicates that either the HF attacks PMMA at higher rates than reported or that there exists some mechanism by which HF is drawn under the photoresist. An additional study comparing the progression of the etch profile of SiO_2 will be performed to study how the it etches between the Ge lines.

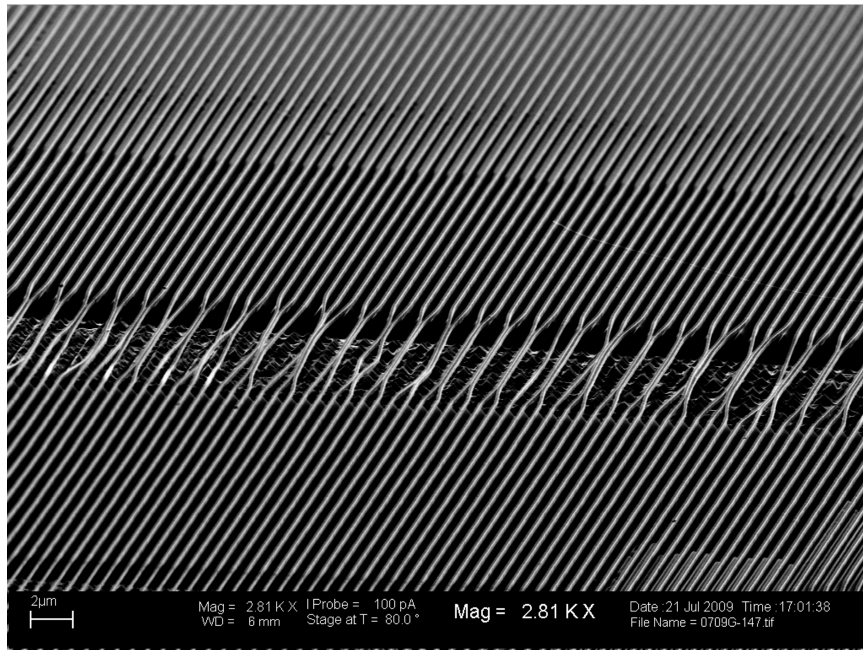


Figure 3.24. Sample 0709G following the wet etching steps, the creeping of HF under the masking material is apparent due to the tapered pattern of the oxide leading to the pit in the Si which was exposed to HF the longest and thus was able to etch in TMAH.

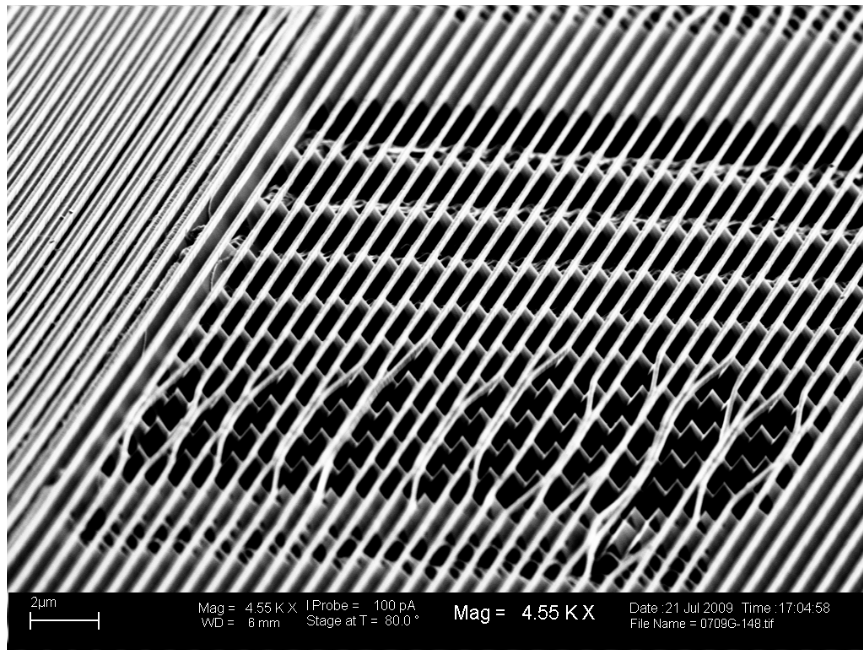


Figure 3.25. Sample 0709G following the dry etch and TMAH etch step, the SiO_2 interface with the exposed regions is much more abrupt, indicating that removing some SiO_2 and then utilizing a dry etch in the exposed regions could be an effective means for suspending Ge wires.

3.8 Experiment 6, suspension attempt.

3.8.1 Sample experiment plan

Many of the problems associated with the success, or failure, of Ge line suspension revolve around the oxide wet etch in HF. Perhaps, utilizing only RIE through EBL defined windows will yield suspended lines. A 450 s global wet etch will be performed to thin the SiO_2 and EBL will follow once the sample has been coated in PMMA. Once a pattern has been defined, the sample will be subject to 150 s of either CF_4 RIE or HF wet chemical etching to further remove the oxide masking the Si below. With the Si exposed, the samples will then be etched in alternating baths of heated TMAH and H_2O_2, twice for one minute per etch for a total of two minutes in each etch bath and four minutes overall. A summary of the steps for this experiment are listed in Table 3.8.

Table 3.8. Processing Steps for 0709H and 0709I

Step	Process	Time (s)	Step	Process	Time (s)	Step	Process	Time (s)
1	SiO_2 etch	450	6	Bake	120	11	Si etch	60
2	Coat	--	7	HF/CF_4 etch	150	12	Ge etch	60
3	Ebeam	--	8	Si etch	60	13	SEM	--
4	MIBK	120	9	Ge etch	60	14		
5	CD26/DI	120	10	Bake	120	15		

3.8.2 Sample experiment results

Samples 0709H and 0709I were globally wet etched for 450 seconds. Sample 0709I was taken for SEM examination prior to coating to inspect for any glaring discontinuities or completely etched regions. No peculiarities were apparent, and 0709H and 0709I were coated and processed. Sample 0709I went under a second wet etch for 150 s, whereas 0709H underwent 150 s of CF_4 RIE. Both samples were then placed in heated TMAH for 180 s to etch Si for Ge suspension. The RIE proceeded to etch Ge,

SiO_2, and the then Si that was exposed during etching as seen in Figure 3.26. All the Ge that was intended for suspension was removed during this step. Clearly, 150 s of exposure to RIE is too long. 0709I did not fair any better than 0709H. The second SiO_2 etch appeared to remove too much SiO_2 and all the Ge lines delaminated as seen in Figure 3.27. Short suspensions seem to not be possible by wet etching alone, because too much of the masking SiO_2 is removed resulting in delaminated Ge lines. However, 150 s of CF_4 RIE results in the complete removal of the Ge. Thus, combining HF and a short, 60 s to 120 s, CF_4 etch step will likely result in the desired product.

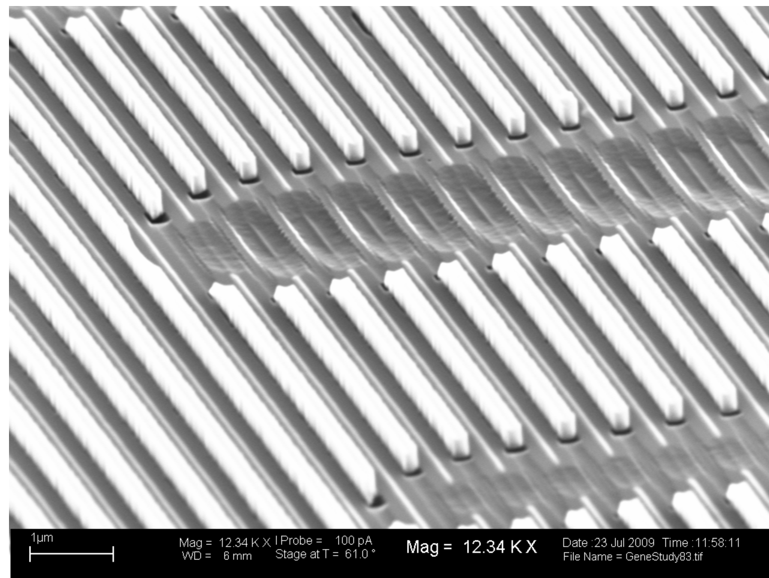


Figure 3.26. CF_4 RIE, clearly, is effective at removing all three materials. 150 s of dry etching is sufficient to remove all the exposed Ge; therefore a shorter RIE must be used if suspended Ge lines are to be produced.

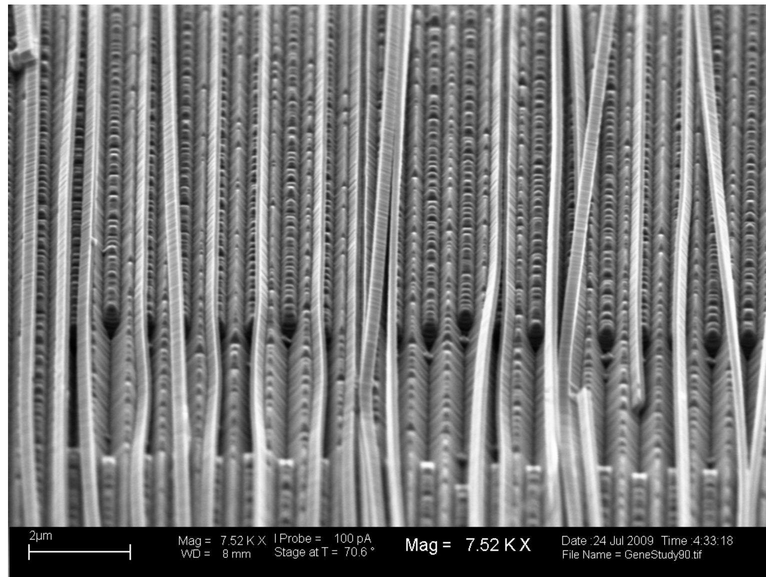


Figure 3.27. Sample 0709I received only wet etching, resulting in delaminated Ge lines. Wet etching seems to be incapable of producing suspensions lengths under 2 μm, regardless of the size of the lithographically defined etch windows.

3.9 PMMA Undercut and HF etching study

3.9.1 Sample experiment plan

The previous experiments have shown that an understanding of how the PMMA is undercut will be vital to attaining narrow suspension lengths for the Ge lines. A control sample, as well as several other samples will be etched to time increments as performed in the previous experiment. Because 480 s seems to be on the cusp of what is required to attain Si etching in the trenches, a 450 s minute etch will be the upper limit on etch time. This will leave a thin SiO_2 for RIE punchthrough. The samples will be cleaved and observed in the SEM. Table 3.9 summarizes the etch steps that are to take place in this study.

Table 3.9. Global SiO_2 etch times

Sample	Etch Time (seconds)
0709J	330
0709K	0
0709L	450
0709M	240

3.9.2 Results of etching study

The results of the etch study can be seen in Figures 3.28 through 3.31. The SiO_2 etch proceeds in the peculiar slope due to the dishing of Ge caused by a CMP process performed on the substrates before receipt.

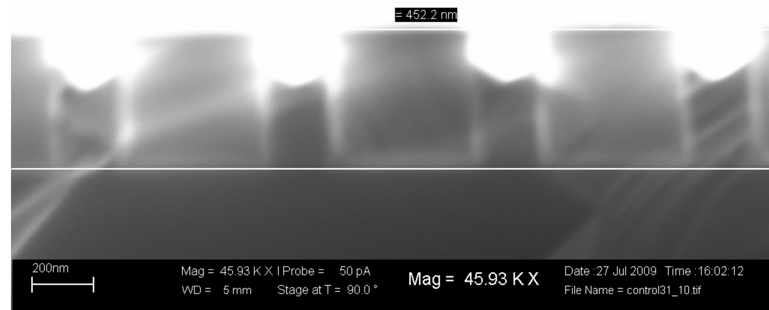


Figure 3.28. There was dishing of the Ge from samples originating from wafer EO3644.5 due to CMP, the anticipated result had been coplanar Ge and SiO_2. A coplanar nature had been assumed by previous experiments, which largely produced unimpressive results.

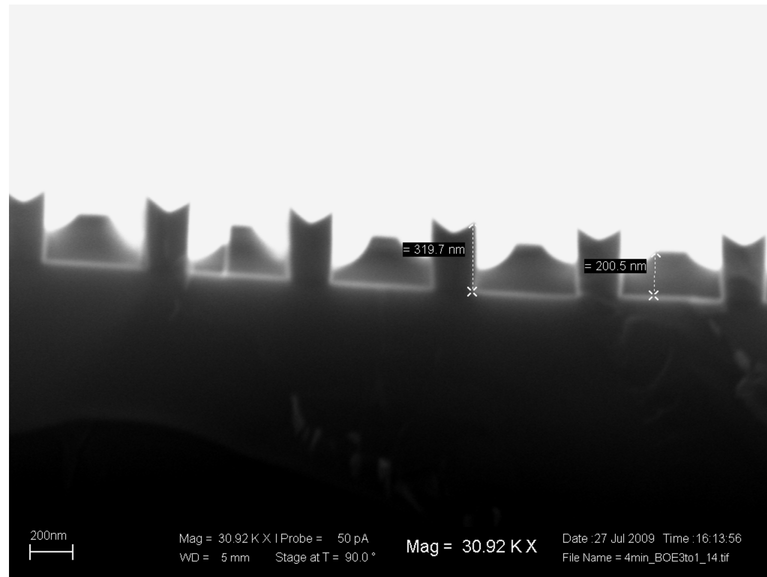


Figure 3.29. Sample 0709M after 240 s of HF etching is shown above. The isotropic etching of SiO_2 in HF results in the "Hershey kiss" like structures. HF encroachment under the photoresist mask would certainly occur with these structures, resulting in larger than anticipated etch depths.

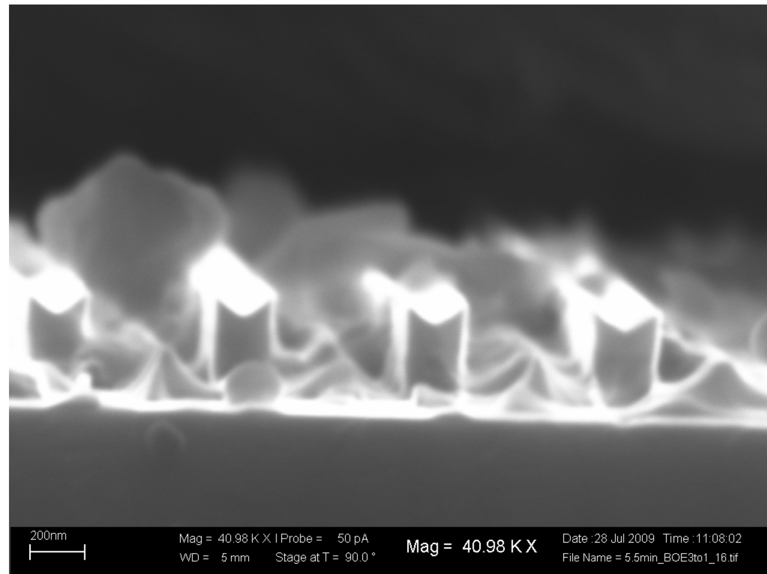


Figure 3.30. Sample 0709J following 330 s of global HF wet etching. Much thinner layers of SiO_2 remain after this etch interval.

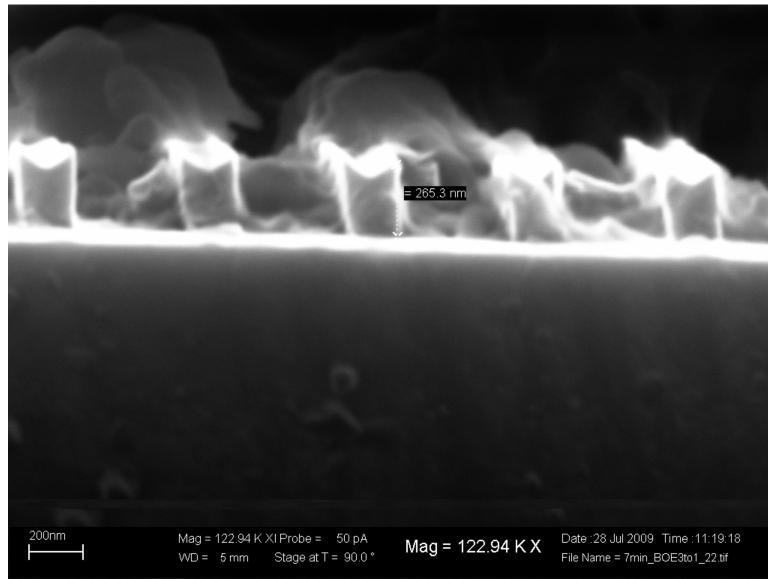


Figure 3.31. Sample 0709L following 450 s, the majority of the oxide has been etched from between the Ge columns. Such gaps would allow wet chemistry to freely etch seemingly masked regions on a sample.

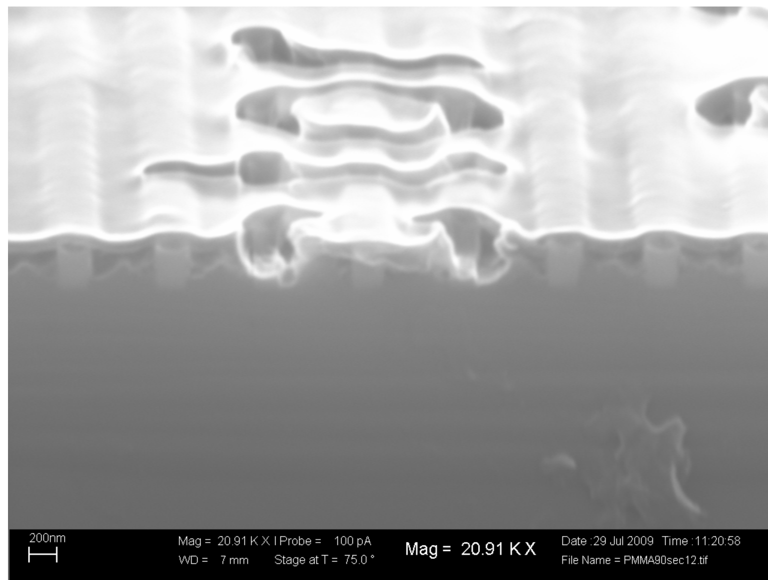


Figure 3.32. Sample 0709P received a global wet etch for 330 s and was then coated with PMMA. There is clear bridging of the PMMA between Ge pillars, which created channels that allowed wet chemistry to etch away material under the photoresist mask.

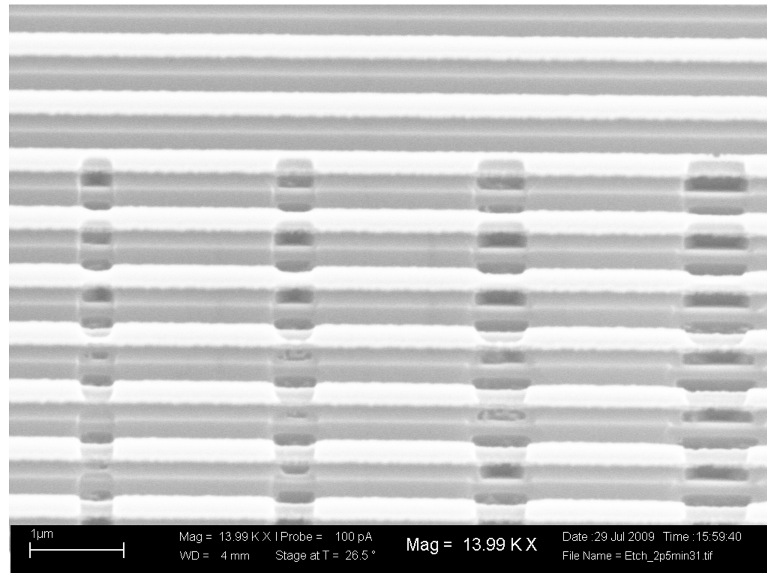


Figure 3.33. A closer view of 0709P which had seen 90 s of CF_4 etching combined with 600 s of hot TMAH etching. Narrow suspensions of both Ge and SiO_2 can be attained with the GON technique.

3.10 Germanium on Nothing

3.10.1 GON process plan

Upon the near successful completion of the desired suspension lengths the processing window seems to have been hammered out. Samples are to undergo a HF pre-etch of 360 s and 30 s to remove sufficient SiO_2 to allow the RIE punch through. Following etch, the sample is to be coated with PMMA and written per the EBL process that had been developed. Once openings are developed in MIBK, the sample will be ready for the subsequent RIE in CF_4 plasma. Utilizing the TRION etch tool, sample 0709K will be etched for 90 s at 175 W of power and 150 mTorr pressure to etch release holes for the TMAH Si etchant solution. Following RIE, sample 0709K will be subject to 180 s of heated TMAH etch solution at 70 ºC. Following processing, the sample will be examined optically and by SEM to confirm wire suspension.

3.10.2 GON process results

Germanium on Nothing nanowires were realized in this experiment. Tables 3.10 and 3.11 describe the processing steps and RIE conditions utilized to produce GON. Suspensions as long as 100 μm in length are observed in Figure 3.34. The structures in Figure 3.34 display the potential for this process, as a CMOS compatible MEMS process to heterogeneously integrate non-silicon materials on a Si platform. However, further refinement is required if this process is to be integrated into production processes as complete etch control of the Ge and Si components has yet to be attained.

Table 3.10. Processing Steps for Successful GON NW Fabrication

Step	Process	Time (s)	Step	Process	Time (s)	Step	Process	Time (s)
1	SiO_2 etch	450	6	Bake	120	11	Si etch	600
2	Coat	--	7	HF/CF_4 etch	150	12	Ge etch	60
3	Ebeam	--	8	Si etch	60	13	SEM	--
4	MIBK	120	9	Ge etch	60	14		
5	CD26/DI	120	10	Bake	120	15		

Table 3.11. Dry Etch Conditions Utilized for GON Process.

Piece	CF_4 (sccm)	CHF_3 (sccm)	O_2 (sccm)	Ar (sccm)	Power (W)	Pressure (mTorr)	Time (s)
0709K-1A	40	0	0	0	175	150	90
0709K-1B	40	0	0	0	175	150	165
0709K-1C	40	0	0	0	175	150	125
0709K-1D	40	0	0	0	175	150	105
All	0	0	20	0	150	150	120

Figure 3.34. Sample 0709K-1A following processing. Long Ge suspensions are clearly evident, indicating the potential for this method to be integrated into MEMS.

Suspended SiO_2 was attained in addition to the Ge lines. This result was unexpected, as it was anticipated that the RIE would obliterate any of the remaining SiO_2 that was exposed. However, this SiO_2 appears to provide additional support to the suspended Ge structure as seen in Figures 3.35 through 3.37. The suspended SiO_2 lines in Figure 3.35 seem to show some Van der Waal's attraction to the nearby Ge lines, an investigation into the stress on such SiO_2 and the effects on the Ge and SiO_2 properties may provide some interesting results. Figure 3.36 exemplifies how the GON process could be utilized to produce large arrays of suspended Ge lines for GAA type transistor applications.

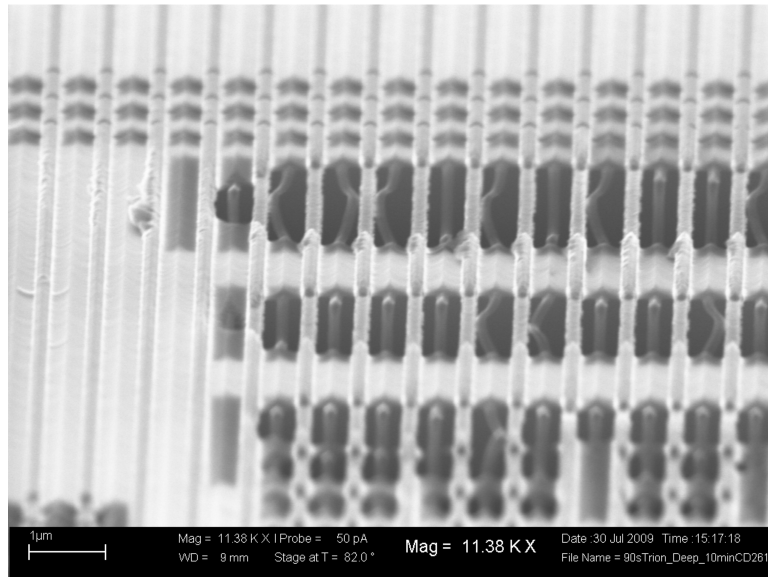


Figure 3.35. An additional image of the sample post processing. The Ge lines are suspended with minimal bending. The SiO_2 may impart some structural support by acting as a brace between each of the suspended lines.

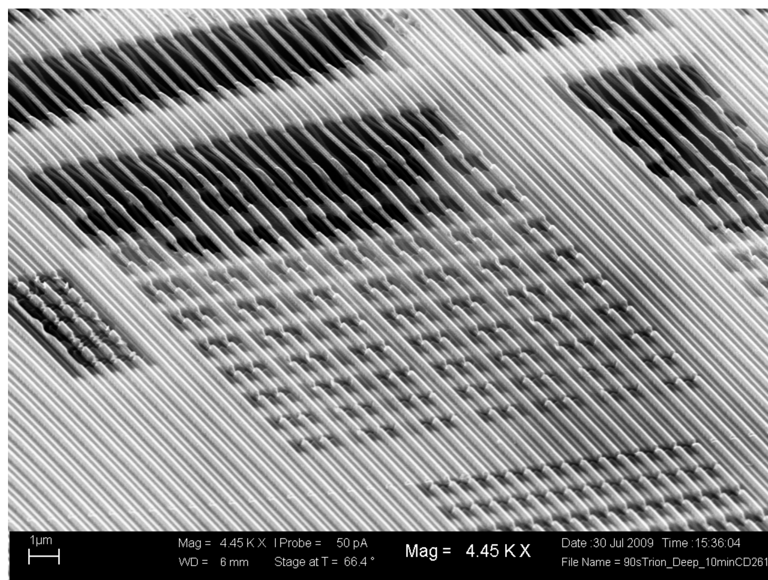


Figure 3.36. The sample at a lower magnification, the regions where Ge was exposed during the RIE display a local thinning.

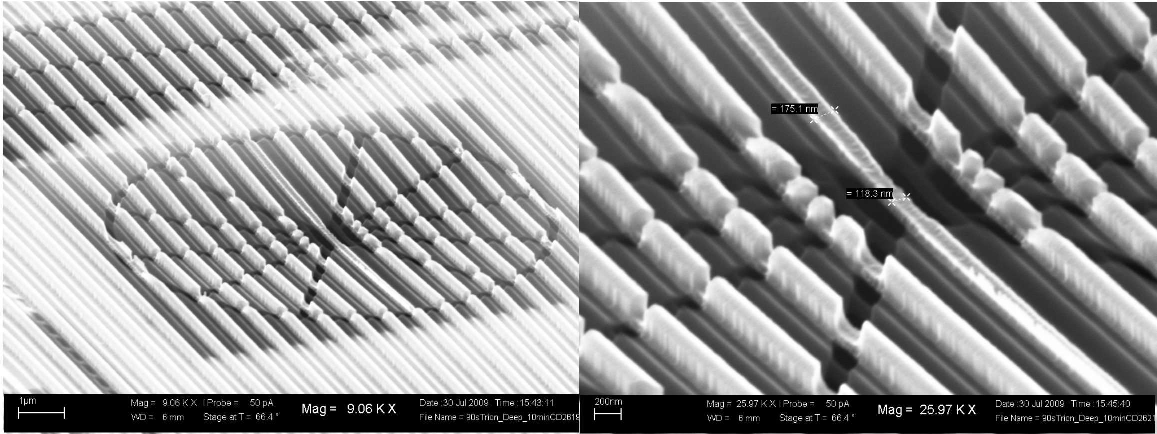


Figure 3.37. (a) A suspended membrane consisting of Ge lines with oxide spacers. This type of structure could have potential in micropump and accelerometer applications for MEMS [38-40]. (b) The thinned oxide appears to provide additional mechanical support to the membrane by simultaneously preventing wire tangling and providing additional connectivity to the supported portions of the membrane.

Sample 0709K-1B was processed under longer etch conditions that also integrated an H_2O_2 etch for further Ge width reduction. Unfortunately the longer etch processes utilized on samples 0709K-1B though 0709K-1D did not produce the desire results. The dramatic effects of the longer etches are displayed in Figures 3.38 and 3.39. The membranes that had been supported by Ge and oxide collapsed when exposed to 165 s of RIE and 60 s of H_2O_2. Such a process would have to be avoided for any designs utilizing such suspended structures. For the shorter suspension lengths, it can be seen that the combination of RIE and H_2O_2 for these etch conditions are too strenuous on the Ge, resulting in the annihilation of nearly all the exposed Ge. This process is not ideal for Ge suspensions, but may work for other semiconductors. Additional samples 0709K-1C and 0709K-1D were processed at 125 s and 105 s of RIE etching, respectively. Only sample 0709K-1D provided successful suspension, as 125 s of RIE was also deemed too long of an etch process.

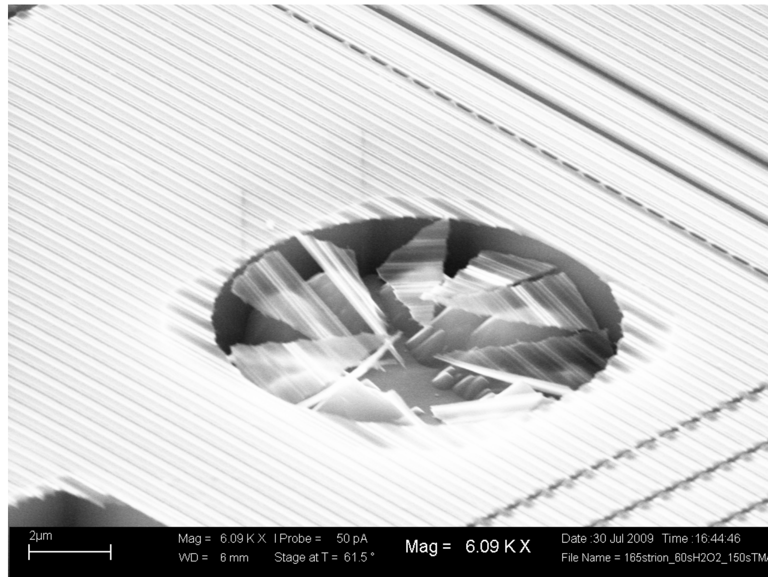


Figure 3.38. Etching away a portion of the Ge depletes the strength of the composite membrane, resulting in collapsed "tin roof" pieces in the etch pit. This technique should likely be avoided for MEMS applications that are to see repeated use.

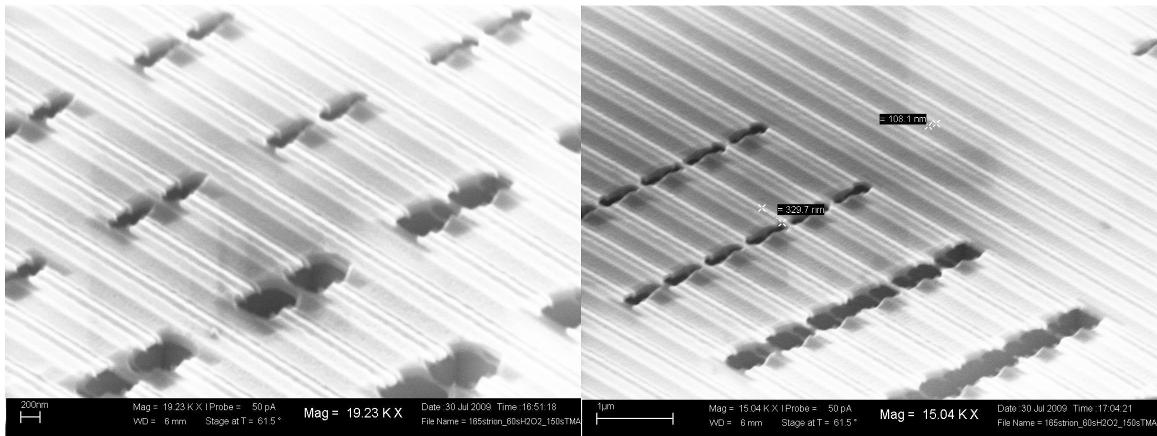


Figure 3.39. (a) Sample 0709K-1B, when exposed to RIE and peroxide etch conditions for extended periods, the Ge suspensions are completely removed. (b) Only Ge structures that were partially concealed by photoresist survived the combined RIE and wet etch.

GON NW structures have been successfully demonstrated through samples 0709K-1A and 0709K-1D. Maintaining RIE etch periods under two minutes seems to be pertinent to the survival of the suspended Ge lines. Dilute H_2O_2 etches might be combined with the short RIE to produce a clean (111) surface for the suspended Ge lines. The NWs and membranes demonstrated by this process may have applications ranging from transistors to NEMS and optoelectronic devices.

Chapter 4

Discussion and Future Direction

4.1 GON Discussion

Successful demonstration of narrow Ge suspensions has been achieved. After many experiments, the necessary process conditions and nuances to make submicron GON structures on an ART wafer were attained. Moving from the simple contact lithography process to EBL provided an opportunity to learn about the differences and difficulties of achieving suspended submicron structures. Significant variation from the initial lift-off scheme was necessary to achieve GON. EBL, RIE, and stepped etching were all vital to the successful manufacture of submicron GON structures. Further refinement of the techniques developed in this thesis may allow for the integration of heterogeneous material beyond Ge on a Si platform.

Migrating from contact lithography to EBL was more complicated than originally anticipated. Factors such as etch times and undercut proved to be more elusive to illuminate than a simple lithography system change hinted. Undercutting of ART lines during wet etch also proved to be a significant hurdle to attaining submicron suspensions. The SiO_2 removal etch tended to severely undercut the PMMA mask, later, it was discovered that this tendency was due to a nonplanar surface which allowed for wet chemistry to travel under the photoresist. As such, assumptions about the surface conditions can not be made when attempting to suspend Ge lines. Thus, critical etch times and surface characteristics must be taken into consideration or the Ge suspensions will delaminate or be significantly longer than desired.

GON is far from being a final process and, as such, there are a variety of paths for improvement in this process. RIE and EBL could use further refinement to reach the limits imposed by the lithography step. Specifically, RIE material selectivity could greatly benefit the GON process. A plasma chemistry that resisted the etching of Ge while simultaneously removing Si and oxide is highly desirable. Some research has been performed with respect to Ge selectivity, but has otherwise seen very little use or publicly announced application. It has been demonstrated that the inclusion of N_2 in the RIE plasma mixture significantly reduces the etch rate of Ge containing compounds in an alternating Si/SiGe/Ge epilayer film stack as seen in Figure 4.1 [41]. This investigation should be applied to an ART sample to determine if the same principles apply. Such an etch could lead to significant suspension length reduction without removing the Ge line material. The necessary gasses for this experiment are presently available in the SMFL, only MFC's and appropriate tubing are required to plumb for the N_2 gas.

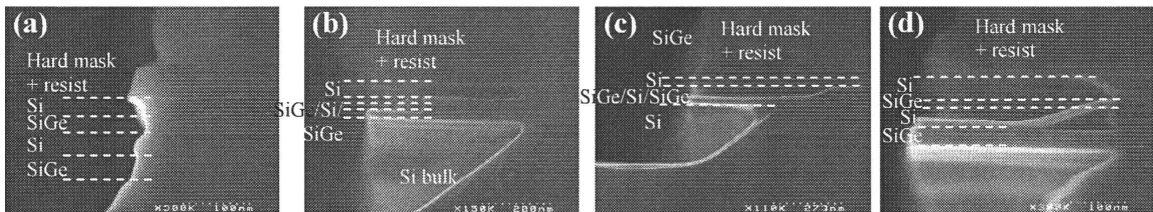


Figure 4.1. SEM micrographs displaying the progression of etch selectivity as a function of N_2 flow. (a) 0 SCCM of N_2 (b) 50 SCCM of N_2 (c) 100 SCCM of N_2 (d) 200 SCCM of N_2 [41].

The planarity of the substrate surface played a significant role in the development of the techniques utilized in GON. Changing the heights of the materials relative to each other could open some interesting conditions for processing. A sample with Ge taller or planar with oxide would need a different wet and dry etch process flow. In these cases, the oxide might not form the central ridge that appeared in reduced oxide thickness

samples where the oxide that was taller than the Ge. Such a difference would effect the required oxide removal time as well as the length of RIE processes. This experiment should be simple to perform with planar samples, a step etch experiment would be useful for showing the progression of the wet etch of oxide in planar ART wafers. Ideally, the oxide thickness should be reduced to between 20 nm and 50 nm to allow for release holes similar to those formed in this thesis. However, a RIE that was selective to Si and SiO_2 would diminish the problems associated with nonplanar samples.

Whilst structures as narrow as 48 nm and as short as 250 nm have been produced by this process, more diminutive structures might be possible. Presently, the EBL step for the GON technique utilizes relatively large beam currents, on the order of 1 nA, to increase the device throughput. It is well known that lower beam currents or higher acceleration biases may increase the resolution of patterns produced by EBL [31]. Utilizing a lower beam current with a more selective RIE may allow for the development narrower GON wires that reach the limits of the LEO writing capability. Such suspensions may reach 50 nm lengths if combined with appropriately reduced ART line spacing which limits the required Si etching.

The GON technique, while far from finished, shows a great deal of promise for integrating submicron length channels of Ge on a Si substrate. The various etch selectivities of the processes utilized in this technique all for suspended or fin structures that could be used for future devices. Additionally the membranes and wires formed may also see use in a variety of MEMS type applications. GON, or techniques like it, may prove beneficial in the further scaling of devices.

4.2 Future Work and Applications

GON may provide a path to integration for a variety of different structures and materials on a Si substrate. While the focus of this work was to demonstrate that NWs could be produced via this selective etch process, other possibilities beyond NW integration may exist. A variety of optical devices from LED's and lasers to waveguides may benefit from ART based GON structures that are similar in structure to modern devices [42-44]. Tunneling and standard transistor devices could also benefit from a GON architecture where wire strain could improve performance [8]. Finally, MEMS systems could apply GON for integrating Ge based devices on a Si platform.

Ge is an optically interesting material in that it has a direct band gap that is very near the indirect band gap in addition to having one of the largest indices of refraction [45]. This characteristic allows for doping and strain to encourage electrons in a Ge sample to transition via the direct gap [46-48]. Properly doped and strained GON lines could act as a gain medium for a laser or LED [49-52]. Furthermore, the design of the ART lines could be utilized as a high order grating that could allow light to escape along the perpendicular axis for coupling into other devices and detectors. Because of the large index of refraction, a waveguide based on Ge could be much smaller than Si or SiO_2 for on chip or chip to chip communication [53]. With GON, it is conceivable that all three components for an optical integrated circuit could be produced from one material system on a Si platform. Such an accomplishment could provide a boon to the telecom and integrated circuit industries by reducing the cost of expensive optical switches and by increasing the available bandwidth for component communication within modern computer systems.

GON structures could show potential for TFET, lateral Esaki diodes, and future FETs. The engineered strain of a suspended structure could enable Ge as a candidate for PMOSFETs, the high hole mobility could allow for faster device operation at lower currents because of the narrow bandgap of Ge (when compared to Si) [54]. This strain could be utilized to minimize the, otherwise large, leakage currents from Ge based FETs [54-56]. Additionally the suspended structure allows for full or near full channel control with the GAA and fin gates structures, allowing greater gate control over the channel region. GAA and fin based devices could also be integrated into TFET designs, where the greater channel control allows for modulation of the electron tunneling probability. Application of a gate voltage would change the effective carrier concentration in the channel thereby modulating the effective width of the tunneling region. When tunneling current probabilities are high, the device would operate by allowing a large number of electrons to tunnel between conduction and valence bands. Aside from the FET and TFET opportunities, GON could provide a path to realizing lateral Esaki diodes. The vast majority of tunnel junction work, from Esaki diodes through Resonant Interband Tunnel Diodes (RITD) has largely been focused on current traveling through the device plane. A lateral Esaki would be trickier to build and test, but may provide insight as there is much less interaction with the substrate. A lateral Esaki may prove to be useful for the development of TFET designs because one of the two regions could be gated with a GAA type structure, and the effects of varied gate voltage measured. Such data could then be applied to the various device models available to help predict the tunneling characteristics and output current that could be expected for a specific device.

MEMS applications could greatly benefit from GON and similar techniques. Integrating Ge based devices on Si for MEMS could greatly improve photodetectors and other devices on Si [57]. Ge NWs are frequently used in biological and chemical detector chips, but the process by which these devices are created could hardly be considered uniform [58]. GON enables highly order arrays of Ge based NWs to be fabricated on a Si platform [59]. However, the methods utilized by GON could easily apply to other material systems such as GaAs or potentially GaN or wide gap semiconductors. These NWs could then be integrated onto the Si platform, and into whichever MEMS/NEMS application was desired. GON could also allow for single crystal membrane films for potentially better accelerometers and other force based MEMS. The single crystal films might allow for better piezoelectric coefficients for better device gain, or potentially power scavenging applications. The ability to utilize materials other than Si for the functional device can really open the field for diverse MEMS and NEMS applications.

Techniques such as GON will enable an ever evolving landscape of device applications. From the relatively mundane, but advanced, logic transistors to complex MEMS and MOEMS, the ability to utilize non-silicon based devices will enable diverse applications with specific material needs; imagine multi-junction solar cells powering microsensory arrays all integrated onto a single chip. While the GON process is not yet fully developed, there is great potential for the use of this approach in a variety of emerging devices.

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Glossary

BOE	-	Buffered Oxide Etch
CMOS	-	Complimentary Metal Oxide Semiconductor
CMP	-	Chemical Mechanical Polishing
CVD	-	Chemical Vapor Deposition
EBL	-	Electron beam lithography
FET	-	Field Effect Transistor
GAA	-	Gate All Around
GON	-	Germanium on Nothing
IPA	-	Isopropyl Alcohol
LED	-	Light Emitting Diode
LOR5A	-	Lift Off Resist 5A
MEMS	-	Micro electro-mechanical systems
MFC	-	Mass Flow Controller
MOCVE	-	Metal Organic Chemical Vapor Epitaxy
MOEMS	-	Micro optoelectro-mechanical systems
NPGS	-	Nabity Pattern Generation System
NW	-	Nanowire
PMMA	-	Poly methylmethacrylate
RIE	-	Reactive ion etching
RITD	-	Resosant Interband Tunnel Diode
SEM	-	Scanning electron microscope
SFML	-	Semiconductor and Microsystems Fabrication Laboratory

SON	-	Silicon on Nothing
TFET	-	Tunneling Field Effect Transistor
TMAH	-	Tetramethylammonium Hydroxide
VLS	-	Vapor Liquid Solid