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Phosphorus Implants for Off-State Improvement of SOI CMOS Fabricated at Low Temperature

By

Siddhartha Singh

A Thesis Submitted

in Partial Fulfillment

of the Requirements for the Degree of

Master of Science

in

Microelectronic Engineering

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DEPARTMENT OF MICROELECTRONIC ENGINEERING

COLLEGE OF ENGINEERING

ROCHESTER INSTITUTE OF TECHNOLOGY

ROCHESTER, NEW YORK

FEBRUARY, 2009

Phosphorus Implants for Off-State Improvement of SOI CMOS Fabricated at Low Temperature

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Siddhartha Singh

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Siddhartha Singh February 24th, 2009

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ABSTRACT

A study on the influence of phosphorus implanted source/drain features on the off-state performance of transistors fabricated in thin-film crystalline silicon at low temperature is presented. Complementary Metal Oxide Semiconductor (CMOS) thin film transistors (TFTs) were fabricated on silicon-on-insulator (SOI) substrates; both NFET and PFET devices in the same p-type layer. Lightly Doped Drain (LDD) features were implemented on NFETs, and a surface-halo source barrier (N-barrier) was implemented on PFETs, using a common implant step. A new mask set was designed with fine resolution of gate offset to investigate small changes in placement of the LDD/ N-barrier structures. The focus of this investigation was the off-state characteristics of the devices; the implanted features were designed to help suppress the effects of Gate Induced Drain Leakage (GIDL) and Drain Induced Barrier Lowering (DIBL). Along with the mask design offsets, a number of process variations resulted in TFTs with different degrees of gate overlap and device symmetry. Electrical device characteristics are presented in the study, with comparisons to devices simulated using Silvaco ® Atlas™.

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CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

The Microelectronic Engineering Department at RIT has been working with Corning Incorporated on the development of a crystalline Silicon On Glass (SiOG) material that has a temperature limit of 600 ºC. The established low temperature baseline CMOS TFT process (Team Eagle CMOS) at RIT has limited off-state performance. It does not provide graded junctions formed by diffusion during high temperature anneals; hence the electric field near the drain junction is high. In addition, there can be end-of-range damage remaining after the source/drain anneal. Poor junction integrity can lead to pronounced off-state leakage currents due to carrier tunneling and/or reduced barrier effects. This study involved implementation of structural enhancements such as a Lightly Doped Drain (LDD) for NFET TFTs, and an enhanced source barrier for PFET TFTs fabricated in the same P-type crystalline silicon thin-film layer. The LDD structure was proposed to eliminate/suppress the leakage currents such as Gate-Induced Drain Leakage (GIDL) current, by lowering the concentration of the field near the drain junction and hence improve the off-state characteristics of the NFET TFT. The

symmetric and asymmetric surface halo implants at the PFET source and drain ends formed an N-barrier and was proposed to suppress DIBL characteristic in accumulation mode PFET TFTs. The TFTs were built on SIMOX SOI substrates; NFET LDD and PFET N-barrier were realized through a common implant step. The mask set was designed to realize totally overlapped, non-overlapped and partially overlapped LDD/N-barrier structures.

1.2 CONSTRAINTS AND CHALLENGES

In order to avoid complex process integration schemes, double-level gate layers and non-self-aligned implant strategies have been considered with a dummy gate arrayed to account for sources of overlay error. The primary objective of this work is to investigate the proposed enhancement features on SOI devices as a benchmark; providing insight for improvement of the off-state characteristic of TFTs on SiOG substrate. The SIMOX SOI substrates used provided the highest quality crystalline silicon; thus avoiding any confounding with imperfections in the semiconductor material. The project also focused on the various constraints placed by the process on lithography, as the technology must eventually be transferred to the display industry with a very low mask count. Further, in this context a single P-type starting layer was considered to keep the process flow simple. In order to improve off-state characteristic one would expect to make ultra thin body TFTs; however, manufacturing technology constraints preclude the fabrication of ultrathin-body SiOG substrates. To enhance the on-state characteristic (increase in drive current) the gate oxide scaling was precluded because of the challenges

in the TFT display industry to deposit high-quality thin gate-oxide at present. There are various other process integration details that will be needed to be resolved as this study does not focus on self-aligned devices.

1.3 SUMMARY AND OUTLINE OF THESIS

There were various challenges encountered in designing the mask, process and while fabricating the devices. A significant engineering effort was invested in order to realize functional transistors for different strategies. This thesis is presented over the six remaining chapters. Chapter 2 provides the review of existing literature related to GIDL and DIBL. Chapter 3 provides details on simulation and effect of structural enhancement on device performance. Chapter 4 presents information on process development for various fabrication design strategies. Chapter 5 presents the device characteristics of fabricated devices along with the details of various structural enhancements and their effect on device performance. Chapter 6 presents a summary of the work, and reiterates the conclusion made following the investigations described throughout the process development and device characterization.

CHAPTER 2

HISTORIC REVIEW

2.1 INTRODUCTION

The future of CMOS scaling and reliability [1] has outlined goals to increase transistor current in order to increase the speed in charging/discharging parasitic capacitances and to reduce transistor sizes for subsequent increase in density. It also outlines constraints such as acceptable leakage current in off-state operation mode and acceptable reliability lifetime/failure rate. With the growing demand for battery-operated low-power circuit applications, off-state leakage currents have been a dominant concern in the semiconductor industry. As transistors are scaled down, it is increasingly complex to control the off-state leakage current. Suppression of off-state leakage current in a CMOS TFT technology by employing LDD for NFET and a surface halo implant to form an N-barrier for PFET will be extensively covered in subsequent sections.

2.2 GATE-INDUCED DRAIN LEAKAGE (GIDL)

Of various off-state leakage currents [1, 2], GIDL and its suppression techniques will be explored in detail in this portion of the work. In a thin gate oxide MOSFET band-to-band tunneling in the gate-drain overlapped region gives rise to the GIDL phenomenon. It is important to understand the cause of GIDL and understand the implicit constraints that it implies on the acceptable supply voltage and/or oxide thickness for future technology. GIDL occurs in the gate-drain overlapped region of MOS transistor. For ease of presentation the GIDL in NFET transistor is explained in this section. When a NFET transistor is in accumulation mode, the silicon surface layer under the gate has almost the same potential as the P-type substrate. The accumulated holes produced at the silicon surface makes it of heavier effective doping in comparison to the substrate. As the gate potential is made more negative or the drain potential is made more positive, a depletion region is formed in the N-type drain. Figure 3.1(a) [2] shows depletion layer narrowing at the silicon surface due to p+ accumulated holes. This narrowing of depletion region on silicon surface layer increases the field near the surface region. The drain region under the gate will be depleted with increase in negative bias voltage, and beyond a certain level of increase in negative bias the drain region can even be inverted as shown in Figure 3.1(b) [2]. The inverted field causes field crowding at this region. The presence of high electric field between drain and gate in this region corresponds to bending of energy bands. If the band bending is more than the band gap (E_g) across a narrow depletion region then this condition is conducive to band-to-band tunneling in this region. As an electron tunnels through to the conduction band a hole is created simultaneously due to an electron-hole-pair generation mechanism. The valence electron is transported to

the drain and the hole goes to the substrate as it has lower potential for minority carrier, thus creating path for GIDL phenomenon [2]. The band diagram as a function of y-depth in the gate-drain overlap region for band bending V_{bend} larger than E_g is shown in Figure 3.2 [3] for a NFET device. The valance electron tunnels through the energy barrier to the conduction band, and creates a hole simultaneously.

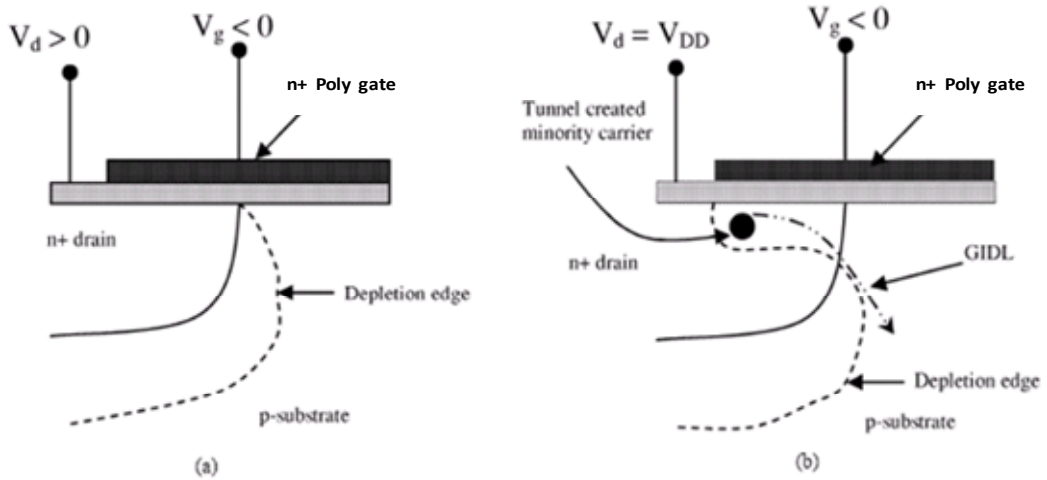


Figure 2.1: Depletion region near the gate drain overlap region of the NFET (a) with low negative gate bias (b) with high negative gate bias such that drain region is inverted [2].

The basic concept, mechanism and limitations of GIDL in both Bulk and SOI substrates are further explored in this study. GIDL is sensitive to electric field which, in turn, depends on several parameters like oxide thickness, gate geometry, terminal bias, drain doping profile, and defect distribution at the interface and in oxide [8]. Various experimental results have been reported showing GIDL's dependence on factors such as gate oxide thickness [11], channel type [4] and the length of channel [8]. Various structures such as LDD, Total Overlap Spacers (TOPS), and Gate Drain Overlapped LDD (GOLD) are also explored in subsequent sections with implication of each for GIDL.

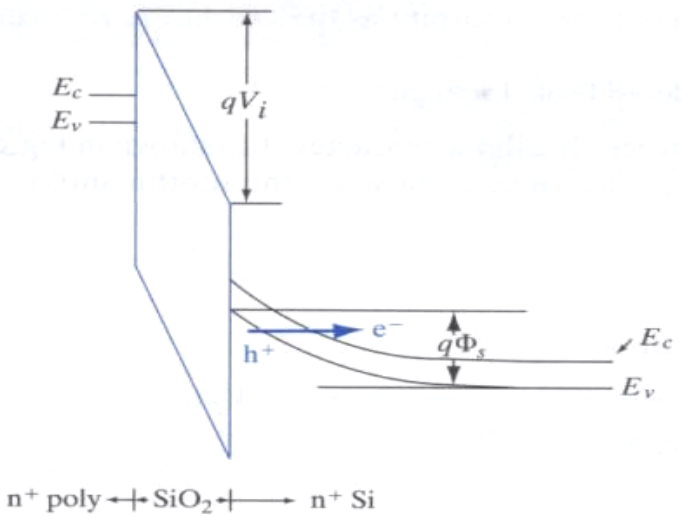


Figure 2.2: The band diagram exhibiting the band-to-band tunneling process in the gate-drain overlapped region of NFET [3].

2.2.1 LEAKAGE MECHANISM

Various models and mechanisms have been proposed to model GIDL current. An initial report [4] stated that the field oxide strength was too low in the gate-drain overlap region to cause Fowler-Nordheim tunneling and the field oxide thickness was too thick for direct tunneling, so GIDL was primarily attributed to band-to-band tunneling. However, report [5] suggests that at higher fields gate-to-drain leakage occurs through a combination of various effects which include band-to-band tunneling and Fowler-Nordheim tunneling of electrons from the gate to the drain, and injection of GIDL-generated holes into the gate. Band-to-band tunneling happens when there is high electric field at the silicon surface which causes band bending to be higher than the energy band gap of silicon (E_g). The electric field at the silicon surface depends on the potential difference between gate voltage (V_d) and drain voltage (V_g), and also on the doping concentration of diffused area. Band-to-band tunneling can be modeled with an

assumption of direct band gap and a uniform electric field [4, 5]. The vertical electric field and leakage current can be found from Figure 2.3 [5].

In Figure 2.3, the 3 T_{ox} originated from the permittivity values of silicon and oxide. The T_{ox} value in this expression is the oxide thickness over the gate-drain overlap region. For Figure 2.3 (1-D model) the band-to-band tunneling is assumed to occur at a minimum band bending of 1.2 eV. When tunneling occurs, the electron enters the drain and holes are generated simultaneously; these holes leave the substrate, creating leakage current. In the 1-D model of [4, 5] the lateral doping profile has been neglected; further, a fixed band bending value has been used for simplicity. A quasi 2-D model has also been considered in [5]. The quasi 2-D model in [5] considers an indirect band-to-band tunneling and dependence of lateral electric field on the total electric field. The dependence of GIDL on the drain doping profile was further explained in [5].

1-D Model:

$$J_t = \frac{A_D}{B_D}\mathrm{E}_{VERT}\exp\left(\frac{-B_D}{\mathrm{E}_{VERT}}\right)$$

Where $\mathrm{E}_{VERT} = \dfrac{V_{DG} - 1.2}{3T_{OX}}$

Direct Tunneling assumes:

$$A_D = \frac{q^2 m_r \pi E_g \Phi_S}{h^3}$$

$$B_D = \frac{\pi m_r^{1/2} E_g^{3/2}}{2\sqrt{2}qh} = 21.3 \text{ MV/cm}$$

Figure 2.3: A 1-D model for GIDL current and vertical electric field in gate-drain overlapped region [5].

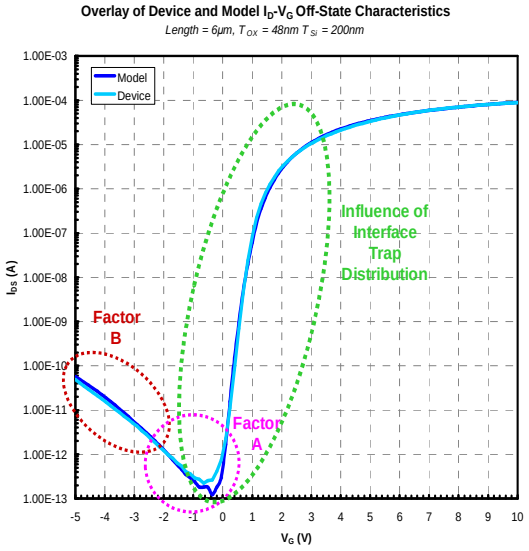


Figure 2.4: Overlay of simulated and measured characteristic of an NFET TFT showing GIDL currents [6].

An overlay of a device and modeled I_d - V_g off-state transfer characteristic for an NFET TFT is shown in Figure 2.4 [6]. This plot follows the concept covered in Figure 2.1 and 2.2 -*i.e.*, as the gate voltage over-drives the off-state (negative) leakage current goes up. The device parameters were as indicated: length = 6 µm, T_{ox} = 48 nm and T_{Si} = 200 nm, V_{DD} = 5 V. The device was fabricated using the standard Team Eagle CMOS process at RIT. In order to model band-to-band tunneling, adjustments in tunneling carrier generation factors (A, B, shown in Figure 2.4) using tunneling equation (1) were employed [7].

$$G_{BBT} = A\mathrm{E}^{\gamma} e^{\left(-\frac{B}{\mathrm{E}}\right)} \tag{1}$$

where γ=2.

In regard to GIDL current, better device performance was characterized for PFET than NFET devices in [12]. Two specific mechanisms were reported for this improved device performance in PFET in [4] which are as follows: (a) Boron doping concentration is more graded than Arsenic doping concentration near the junction which contributes to variation of electric field at the silicon surface, and (b) the local field at which the valence band electron enters the barrier is significantly lower than the surface field, thus making tunneling more difficult.

It was reported in [8] that the GIDL current is independent of channel length. It can be further concluded from Figure 2.5 that the GIDL current is strongly dependent on V_{DD} and not on channel length.

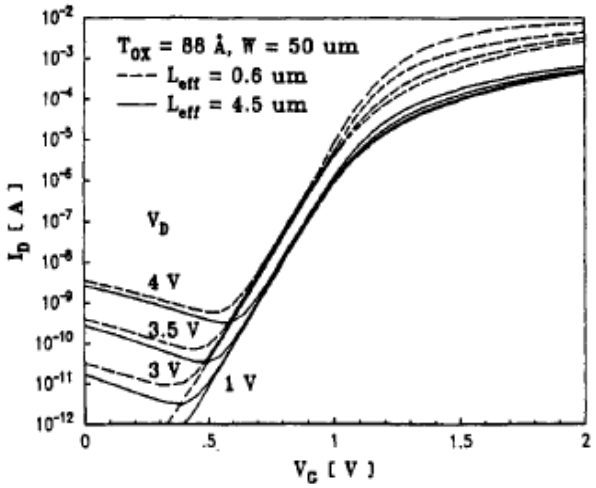


Figure 2.5: Subthreshold plot of 88 Å gate oxide of NFET with L_{eff} = 0.6 µm and 4.5 µm. Higher V_D value exhibits higher drain leakage current [8].

2.2.2 LEAKAGE REDUCTION TECHNIQUES

Effective measures are needed to reduce the leakage power. As reported in [2], due to substantial increase in leakage current, the static power consumption is expected to exceed the switching component of the power consumption. Leakage current is sensitive to the following parameters: oxide thickness, drain concentration, lateral doped draining gradient and applied drain-to-gate voltage [5]. As described initially, in the gate-to-drain overlap region the gate workfunction and high drain concentration enhance field strength. This large field, in turn, depletes the heavily doped drain surface, giving rise to transport-limited thermal generation.

The LDD structure enables the device designer to meet the constraint of hot-carrier reliability, breakdown voltage and GIDL [1]. The blanket large-angle tilt implant used to form NLDD and P-Halo simultaneously in [9] reported very superior device performance along with process simplification by elimination of one NLDD

masking step and one halo implant step. Various Lightly Doped Drain structures such as Gate-Drain Overlapped LDD (GOLD) [10], Total-Overlap Poly Spacer [5], along with traditional LDD structures with oxide side wall spacer have been reported to have better performance over a regular Source/ Drain (SD) device. Figures 2.6 (a), 2.6 (b) and 2.7 show TOPS, LDD structure with oxide sidewall spacer [5] and GOLD [8] structures, respectively. The influence of halo implant and the LDD structure was reported in [9].

(a) (b)

Figure 2.6: The drain structure schematic for (a) TOPS and (b) LDD with oxide side wall spacer [5].

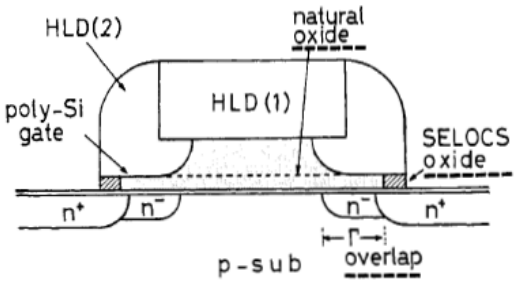


Figure 2.7: The drain structure schematic for a GOLD structure [10].

The LDD structures were employed to eliminate/suppress GIDL. Reduction of GIDL was possible by using LDD structure as it lowered the concentration of the field near the drain junction. The performance of various structures was reported in [5]. Figure 2.8 [5] represents the off-state characteristics for Source Drain (SD), TOPS and LDD with oxide side wall spacer devices at V_D = 5 V and t_{ox} = 8.5 nm for W = 50 µm and L = 10 µm device. The LDD device with oxide side wall spacer exhibited least GIDL

current of all the reported devices. For devices where an abrupt n+ junction was overlapped by gate (SD, TOPS), there existed a built-in lateral field which should be added vectorially with the vertical field. This addition of built-in field caused an increase in GIDL current and lowered V_{max}. The GOLD structure was reported to reduce the n- resistance due to the overlapped gate [10]. The GOLD structure was also stated to have improved channel currents and higher transconductance due to reduced L_{eff}. It was recommended to keep the spacer length longer than the lateral diffusion length of the dopant to minimize GIDL and maximize V_{max}.

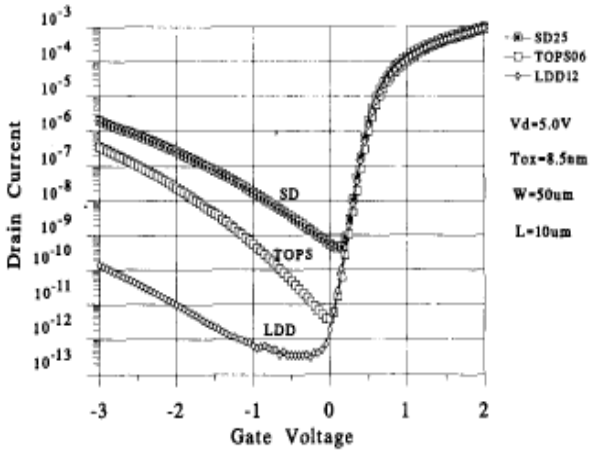


Figure 2.8: Subthreshold characteristics for the SD, TOPS and LDD devices with oxide side wall spacer [5].

2.2.3 GIDL DEPENDENCE ON BODY THICKNESS IN SILION ON INSULATOR (SOI)

The benefit of using a thin-body transistor such as Single-Gate Ultra-Thin-Body (SG-UTB) transistor was investigated during the study in [13]. Dependence of GIDL

current on body thickness was demonstrated on SG-UTB. I_d-V_g characteristics for PFET and NFET SG-UTB FETS are shown in Figure 2.9 (a) and 2.9 (b), respectively.

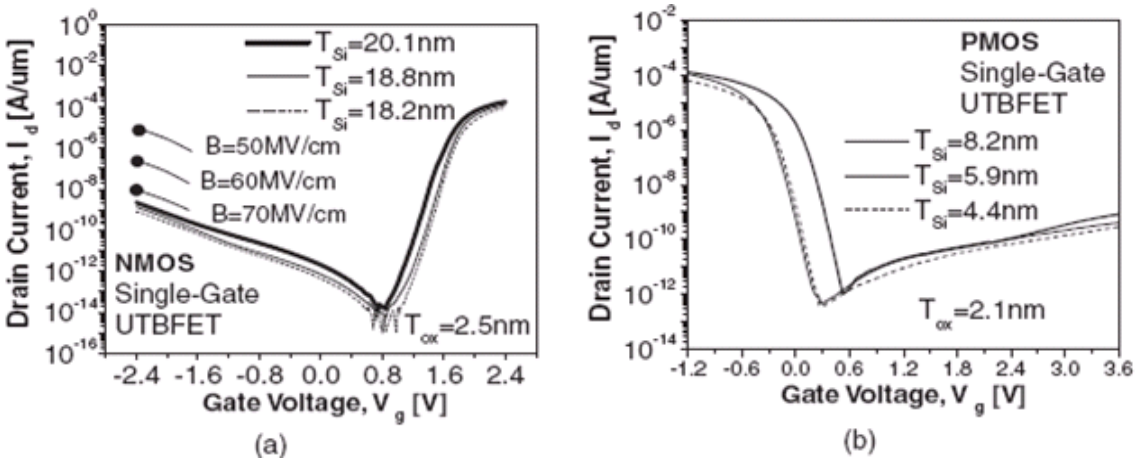


Figure 2.9: Extracted I-V characteristic for SG_UTBFET devices (a) NFET and (b) PFET [13].

From Figure 2.9 it can be seen that as the body thickness is decreased, the GIDL current is reduced for both p-channel and n-channel devices. It was also reported in [14] that the SOI MOSFETs provide additional device and circuit design flexibility due to unique short channel effects they exhibit. The GIDL reduction in [13] was attributed to reduced E_{VERT} value in Figure 2.3 which was reported to be more significant for thinner body thickness. Another effect was stated that the tunneling effective electron mass will increase the parameter B in Figure 2.3. The reason for this was reported to be due to the occurrence of sub-band splitting when the body thickness is thinned, so that the population of electrons in the 2-fold valleys increases as the body thickness decreases, which in turn will cause the effective mass value to increase as the body thickness reduces.

2.3 DRAIN-INDUCED BARRIER LOWERING (DIBL)

This portion of the study will cover the mechanism behind DIBL, the design parameters that affect DIBL, its impact on device performance, and the two different kinds of DIBL *i.e.*, surface and bulk. As FETs are scaled to smaller channel lengths, short channel effects (SCEs) like hot carrier effects (HCE), DIBL and punchthrough are realized. In long channel devices, source and drain are well separated from each other. The potential barrier between source and drain of a long channel device regulates a channel current, which is independent from drain voltage. However when channel length is reduced, the depletion region of drain penetrates into source region, leading to a lowered potential barrier between source and drain regions [15]. The degree of penetration is dependent on parameters like substrate doping, gate-oxide thickness, channel length, channel width, temperature, junction depth, and substrate bias. DIBL causes an undesired current flow, which cannot be controlled precisely, in the bulk; at the surface; or both at the surface and in the bulk simultaneously, even in subthreshold region of operation [15].

2.3.1 DIBL MECHANISM

DIBL is among the most crucial SCE and is defined as in equation (2) [16]. According to (2), for a given change in drain potential of a FET, a change in the threshold voltage of FET “(turn-on voltage)” results, provided everything else remains constant. This was first presented in [17] where a relationship was developed that described threshold voltage as a function of drain bias.

$$\lambda_{DIBL} = -\frac{\partial V_T}{\partial V_{DS}} \qquad (2)$$

According to charge-sharing theory [18], the depletion region from the drain encroaches on the channel, making the effective area that the gate controls and is able to turn "on" or "off" smaller under the influence of DIBL. Figure 2.10 [19] shows the concept of DIBL by surface potential along the channel for a long channel device and a short channel device as calculated by a two dimensional model [19]. For a long channel device, the potential barrier is constant almost along the entire channel and the electron injection is controlled by the height of the barrier and, indirectly by the gate voltage [15]. The electric field along the entire channel can be considered as one dimensional (vertical field from gate to bulk) except when very close to source and drain edges so that a one-dimensional Poisson's equation is applicable to solve for this barrier height. However for the short channel in Figure 2.10, surface potential is not constant over the channel and the two dimensional solution to the Poisson equation must be used to account for the influence of the drain bias. It was further reported in [15] that the potential barrier is further decreased by increasing V_{DS}. DIBL can be a result of increased V_{DS}, reduced channel length, or combination of both simultaneously. In Figure 2.10 $\Delta\phi_S$ is change in barrier height caused by applied potential on the drain. ϕ_B is source barrier potential for short channel device and ϕ_{BL} is source barrier potential for the long channel device.

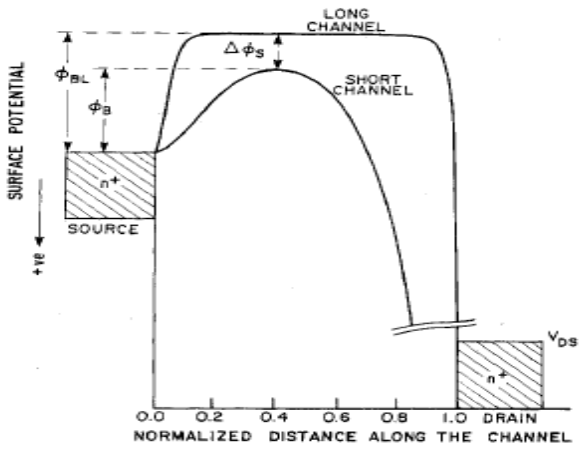


Figure 2.10: Surface potential vs. normalized distance along the channel with V_{GS}=V_{SB}=0 [19].

The main consequence of DIBL in a short channel device is the reduction of threshold voltage due to applied drain bias. This shift in V_T can be calculated by either performing two dimensional numerical analysis [20], developing a two dimensional analytical solution based on the charge sharing approach [21], or simplifying Poisson's equation in the depletion region. For analytical expressions of DIBL, geometrical forms for source and drain depletion regions and how they fit together with the gate induced depletion regions were assumed. This method uses the effect of drain-to-substrate, or source-to-substrate biases to determine the depletion widths and, in turn, the effect on DIBL and therefore current. In [18] the Source/Drain depletion regions were divided into trapezoids, each being controlled by a different potential. This was regarded as good for quick calculations, but this method is limited to specific device design, and does not accurately represent the potential near the depletion edge, and thus does not provide an accurate estimate of the barrier height near the source. The alternative method used to

describe the phenomenon of DIBL is by solving two-dimensional Poisson equation (3) in the depletion region under the gate [22].

$$\nabla^2 \psi(x, y) = \frac{q N_a}{\varepsilon_{si}} \qquad (3)$$

where q is the charge of an electron, ε_{si} is the permitivity of silicon, and N_a is the substrate doping. A very crude way of looking into the origin of DIBL is presented in [15] by using the 2-D dipole structure. In [28] this depiction was further extended to 3D for investigating the width dependence of DIBL.

The injection of charges from source to drain can either be at the surface, in the bulk or both at the surface and in the bulk [15]. In order to distinguish between two cases, DIBL has been classified as “surface DIBL” and “bulk DIBL”. Bulk DIBL is usually referred to as “punchthrough” [23]. Even though both occur due to the increase in V_{DS}, they are noticeable in different regions of the device transfer characteristics. A simulated test of DIBL is shown in Figure 2.11 [15] using low gate biases, where the drain is swept and current is measured. Two distinct regions on the V_G=0.5 V trace have been marked. The area where point *A* lies is in the surface DIBL-dominated region and the area were point *B* lies is where bulk DIBL dominates. It was reported in [19] that, even though in DIBL the threshold voltage is somewhat shifted, the slope will not change significantly when V_{DS} is varied, whereas in punchthrough, the slope will change, indicating that the level of gate control over current is changed.

Punchthrough current flows below the surface region whereas surface DIBL current, usually referred to as just DIBL, flows through surface. When drain potential is increased, it increases the depletion region associated with that reverse biased junction, and eventually the space charge region of source and drain junctions merge if junction breakdown does not occur first. This causes a current to flow in the bulk in such a way that gate has little control over it. However, in case of DIBL, current will flow through the transistor near the silicon/oxide interface due to decrease in potential barrier between source and drain.

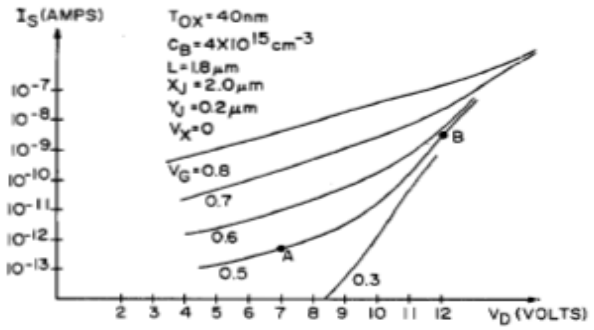


Figure 2.11: Simulated FET low-level current/voltage characteristics [15].

2.3.2 LIMITATION ON MOSFET SCALING

DIBL sets a fundamental limitation in advanced MOSFET scaling [15]. Along with scaling, the SCE should be suppressed to an acceptable level for operation in the subthreshold region. DIBL depends on various device parameters. DIBL decreases with scaling of the gate-oxide due to higher gate control over the channel depletion region. As gate-oxide thickness is increased, the gate electrode is further separated from the channel, causing an increase in the penetration of field lines from drain to source, and lesser

vertical electric field from gate. This corresponds to a reduced gate control over the channel and a decrease in the peak of potential barrier [15]. It is stated in [19] that the DIBL effect and subthreshold current decrease with an increase in substrate doping. The increased doping level in substrate reduces spread of depletion layers for source and drain regions. However, excessive increase in substrate doping degrades carrier mobility-hence drive current-and it further enhances the HCE. As channel length is reduced, the slope of barrier height and V_T with respect to V_{DS} increases due to enhanced field penetration from drain to source region [19]. In other words, DIBL increases with scaling of the channel length of device. DIBL further increases with increase in junction depth of the device [19].

DIBL implies a significant restriction on the scaling of supply voltage. An increase in magnitude of substrate voltage results in an increase in height of the barrier from source to channel. This, in turn, causes lower subthreshold current to flow through the channel. An increase in magnitude of substrate voltage increases the depletion regions associated with source and drain junctions. An increase in slopes of barrier height and V_T reduction is observed as the substrate bias is increased [19]. It is reported in [24] that smaller width devices show suppression in DIBL over larger width devices for STI processes. However, devices fabricated with a LOCOS process exhibit more punch through for narrower device [28].

2.3.3 REDUCTION OF DIBL CHARACTERISTIC

For submicron devices the presence of SCE results in excessive amount of leakage currents flowing through undesired current paths. Leakage currents can be reduced by drain and well engineering, as they play a significant role in altering electric field distribution in the substrate by changing energy bandgap, interface charge, and source/drain diffusion profiles [15]. Increasing substrate doping reduces the DIBL effect due to decrease in depletion width of the junctions [19]. This can be implemented in two ways: either by performing a localized implant which increases the doping concentration around source/drain junctions, or by engineering well doping concentration to give high amount of dopant around junctions and less dopant at the surface to form a "Retrograde Well" [25]. The other alternative to suppress DIBL is by performing anti-punchthrough implants which are concentrated around source and drain edges. Figure 2.12 and 2.13 shows variations of the localized implant approach. The blanket anti-punchthrough implant is done by combination of well and channel implants. The pocket implant is done at large tilt angles after the formation of gates so that the ions do not pass through the channel. This gives better control over threshold voltage and more tolerance to higher dose implantation since it is localized around only the source and drain edges [27].

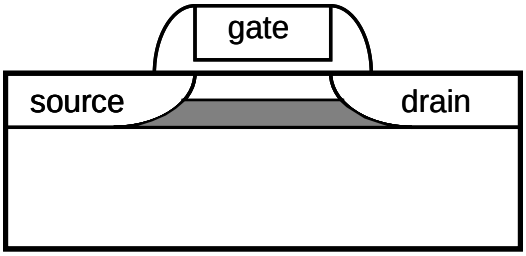


Figure 2.12: Blanket anti-punchthrough implant, after [27].

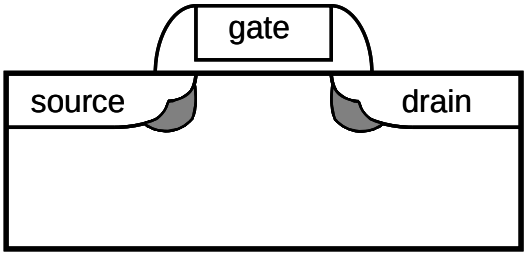


Figure 2.13: Pocket anti-punchthrough Implant, after [27].

In [15] design trade-offs between hot carrier effects (HCE) and DIBL have been stated. Hot carrier effects are usually reduced by introducing low-doped regions next to heavily doped junctions to allow gradual increase in electric field along the channel. These low doped regions help to reduce HCE, but they cause DIBL to increase due to the enhanced penetration of the depletion regions. The LDD structure is used in devices mainly to spread the drain electrical field in order to overcome the impact ionization-induced hot electron effects [26] and to suppress GIDL currents [5]. The shallower the junction depth of an LDD structure, the more suppression of DIBL effect is seen in the transistor [27].

Halo implant technology for PFET was reported to have improved short channel performance after careful tradeoffs that were made between L_{min} and other electrical parameters of the device [29]. The halo implants caused the channel edges to be more heavily doped, which made the junction depletion width smaller and the distance between source and drain regions larger [2]. This effect leads to lower drain-induced barrier lowering (DIBL); however, higher doping near the channel edges caused larger band-to-band-tunneling which increased GIDL current. High p-channel current drive and acceptable p-channel short channel hardness were reported in [9] with fewer process complications for optimized halo implant.

2.3.4 DIBL IN SOI

The DIBL and threshold roll-off characteristics of the SOI FETs are very promising candidates for sub-100 nm ULSI applications, due to their marked advantages for low power and high performance applications. Partially depleted SOI transistors are more mature, but the fully depleted SOI FETs have more potential for reaching the ultimate stages of downscaling [30]. However, there is a problem due to fringing fields which act as an additional DIBL and V_T roll-off component. This fringing field arises due to the penetration of field from drain and source underneath the channel, through the buried oxide (BOX) and substrate. The physics-based quantitative evaluation of this phenomenon remains a problem [30]. Scaling of film thickness with channel length and by biasing the back gate (substrate) can contribute in controlling threshold voltage reduction by charge sharing, drain-induced barrier lowering in weak inversion and channel–length modulation [14]. In Figure 2.14 [32] the DIBL effect of the double-gate SOI device increases quadratically with the body thickness. Various gate structures have been suggested in the literature to suppress DIBL effectively.

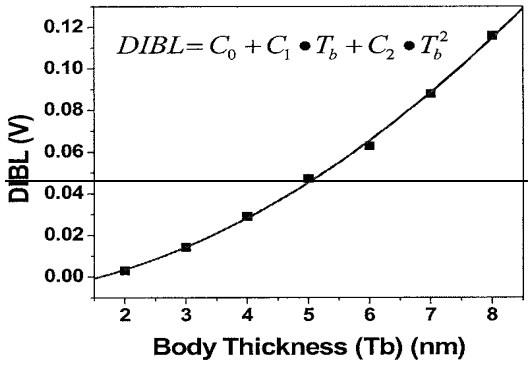


Figure 2.14: DIBL effect of the double-gate SOI device increases quadratically with the body thickness [32].

2.4 SUMMARY

The mechanism of GIDL and DIBL was studied in this section along with the design parameters that affect them and the strategies that suppress/eliminate them. It was noted that GIDL was independent of channel length, and was significantly dependent on oxide thickness as it was higher for thinner oxide. GIDL was also observed to be lower for PFET device than for NFET device. GIDL current in thin body transistor was found to be much lower than the typical bulk body-Si MOSFETs. GIDL current was also observed to decrease with decreasing body thickness as transverse electric field was reduced and tunneling effective mass in the drain region increased. The LDD device with oxide sidewall spacer was observed to have lower GIDL current than the TOPS or conventional SD devices. The drain doping profile and spacer length was also observed to play a significant role in controlling GIDL current, as they vary the electric field at the silicon surface. The design parameters must be carefully chosen to avoid band-to-band tunneling as GIDL imposes an additional restriction on future MOS scaling. Scaling of gate oxide thickness and supply voltage was observed to be restricted by GIDL current.

The DIBL parameter was observed to increase dramatically with a decrease in channel length. DIBL can cause source injection at the surface and in the bulk. Design parameters such as channel length, bulk doping, gate oxide thickness and source/drain junction depths will determine the exact location of the source injection and the bias conditions needed to obtain DIBL. These parameters must be chosen carefully to avoid punch-through and hot-carrier effects. For a double gate device, the DIBL effects seem to increase quadratically with silicon body thickness in SOI. Blanket and pocket anti-

punchthrough implants have been suggested to reduce/suppress DIBL apart from retrograde well engineering.

While the discussion on GIDL in Section 2.2 is relevant to the NFET TFTs in this study, the DIBL effect on the PFET TFTs is somewhat different. DIBL is much more pronounced since the PFETs in this study are accumulation-mode and are fabricated in a p-type thin-film silicon layer. An appropriate gate work function ensures a fully-depleted off-state, and the device turns on as the gate voltage allows holes to return to the p-type body, followed by hole accumulation as the gate bias (magnitude) increases. In a silicon-on-glass application the problem is further enhanced due to lack of a substrate bias; however, this investigation is focused on results from SOI SIMOX substrates.

CHAPTER 3

DEVICE MODELING

3.1 INTRODUCTION

Device simulation plays a key role in any investigation. It not only provides a path for process fabrication steps, but also helps in saving resources. By using appropriate models and parameters, one can estimate the influence of alterations in the process flow on over-all device performance. This simulation can be further used to compare against fabricated devices. The implications of incorporating LDD for NFET and N-barrier for PFET have been investigated in this part of the study. Silvaco Atlas device simulation software has been used to model the device characteristics. Specific models related to each FET type were invoked at necessary steps in the simulation code and will be covered briefly. Certain parameters were chosen to match the transfer characteristics of fabricated TFTs. Careful trade-offs were considered in order to enhance the off-state performance, without compromising on-state current significantly. The LDD/surface halo dose and length were optimized accordingly.

3.2 MODELING OF GIDL CHARACTERISTIC IN NFET DEVICES

The GIDL characteristic of NFETs has been modeled in a close approximation with SiOG and SIMOX SOI fabricated devices [7]. The Shockley-Read-Hall (SRH) trap-based recombination and concentration-dependent (CONMOB) low-field mobility default models were used along with field-dependent mobility (FLDMOB) altered (B.Electrons =2 and B.Holes=1) values. The SRH model uses fixed minority carrier lifetime which along with CONMOB that uses simple power law temperature dependence eases convergence for simulation. The FLDMOB was used to account for any type of velocity saturation and was preferred over other models to avoid usage of very fine grid while accounting for transverse field dependence in planar devices. Band-to-band tunneling (BBT.STD) was modeled using equation (1) of Section 2.2.1, with adjusted carrier generation factors ($A=8.5\text{x}10^{16}$, $B=7.5\text{x}10^{6}$ and $\gamma=2$). The BBT.STD accounted for direct transitions in the presence of high field. Default band gap narrowing (BGN) models were used to account for decrease/increase in band gap due to concentration in the heavily doped regions. Fermi-Dirac statistics along with Newton methods for numerical solutions were used. Device parameters in simulation were as indicated: L_{eff} = 1 µm and 4 µm, T_{OX} = 500 nm, T_{Si}= 200 nm and L_{LDD} = 0.1 µm. Doping levels of $1\text{x}10^{15}\,\text{cm}^{-3}$, $1\text{x}10^{17}\,\text{cm}^{-3}$ and $1\text{x}10^{20}\,\text{cm}^{-3}$ are used, respectively, for p-silicon layer, N-type LDD and n+ source/drain regions. The gate work function for Molybdenum of 4.53 V was used.

The saturation sweep for NFET with L_{LDD} = 0.1 µm and no gate overlap (LDD self aligned to main-gate) at V_{DS} = 5 V in Figure 3.1 is observed to be a promising solution for suppression of GIDL currents in NFET for the above-mentioned device

parameters. The simulated characteristic in Figure 3.1 qualitatively resembles the measured characteristic in Figure 2.8 [5]. The LDD with overlap of gate has been assumed analogous to TOPS of [5]. Figure 3.1 further shows that the GIDL current is independent of the channel length. The trade-off using LDD in NFETs can be seen in Figure 3.1, as a decrease in transistor current is observed. A further detail of the off-state is shown in Figure 3.2 for NFET simulation.

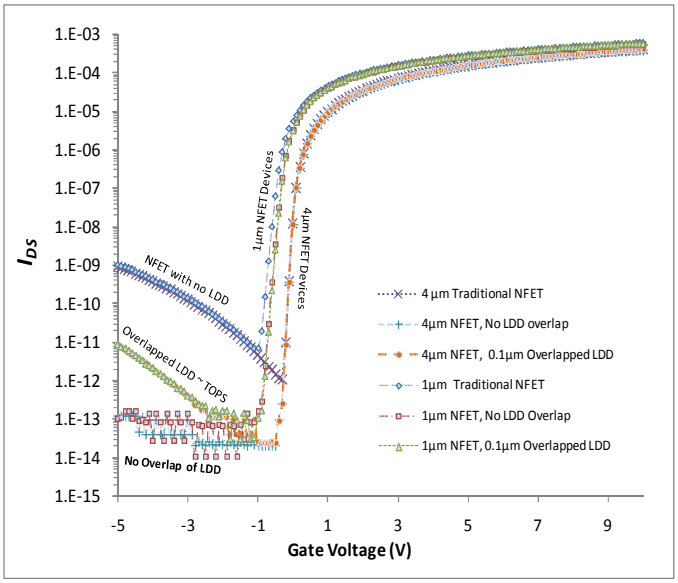


Figure 3.1: Saturation Sweep for NFET with implication of GIDL on enhancement structures; LDD and TOPS.

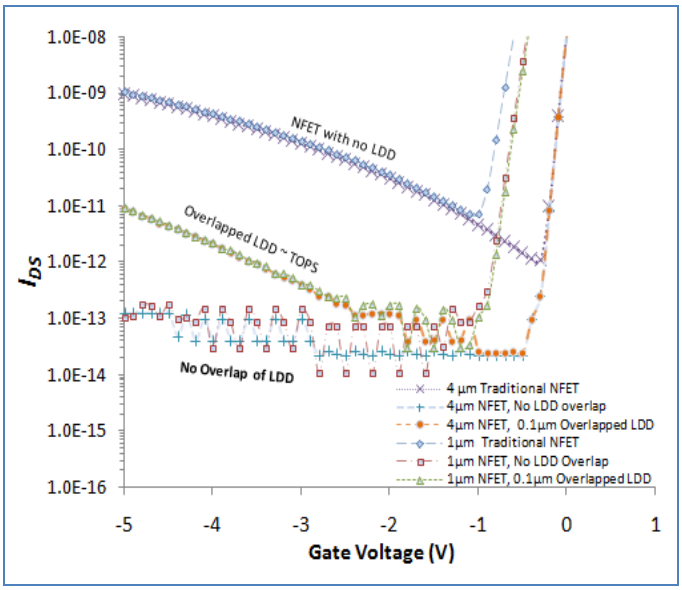


Figure 3.2: Saturation sweep for NFETs showing GIDL in the off-state.

3.3 MODELING OF DIBL CHARACTERISTIC IN PFET DEVICES

Asymmetric surface halo implants to form an N-barrier at the source end of the TFT PFETs were modeled in the engineering effort to suppress DIBL without compromising other on-state (e.g. current drive) or off-state (e.g. GIDL) characteristics. To model DIBL [7] default Shockley-Read-Hall (SRH) trap-based and Auger recombination models were used as well as the Shirahata (SHI) model to extend the Klassen's concentration-dependent lifetime model with transverse electric field dependence. Default band gap narrowing (BGN) models were used to account for decrease/increase in band gap due to concentration, and default field-dependent mobility (FLDMOB) models were used. Fermi-Dirac statistics along with Newton and Gummel methods for numerical solutions were used. The device parameters in simulation were as indicated: L_{eff} = 1 µm and 4 µm, T_{OX} = 500 nm, T_{Si} = 200 nm and L_{Halo} = 0.1 µm and

0.2 µm. Doping levels of $1x10^{15}$ cm^{-3}, $1x10^{17}$ cm^{-3} and $1x10^{20}$ cm^{-3} are used, for the p-type silicon layer, N-type surface halo, and p+ Source/Drain regions, respectively. The gate work function for Molybdenum of 4.53 V was used. In the PFET simulation presented in this portion of the study, asymmetric surface halo implants were totally overlapped by the gate electrode to ensure a complete gate-supported channel, with minimal trade-off in on-state current drive.

The potential distribution along the channel of TFT PFETs at different channel lengths (L_{eff} = 1 µm and 4 µm) has been studied under low drain bias and high drain bias conditions. The channel-length dependence of barrier lowering is demonstrated under low-field conditions in Figure 3.3, and under high-field conditions in Figure 3.4.

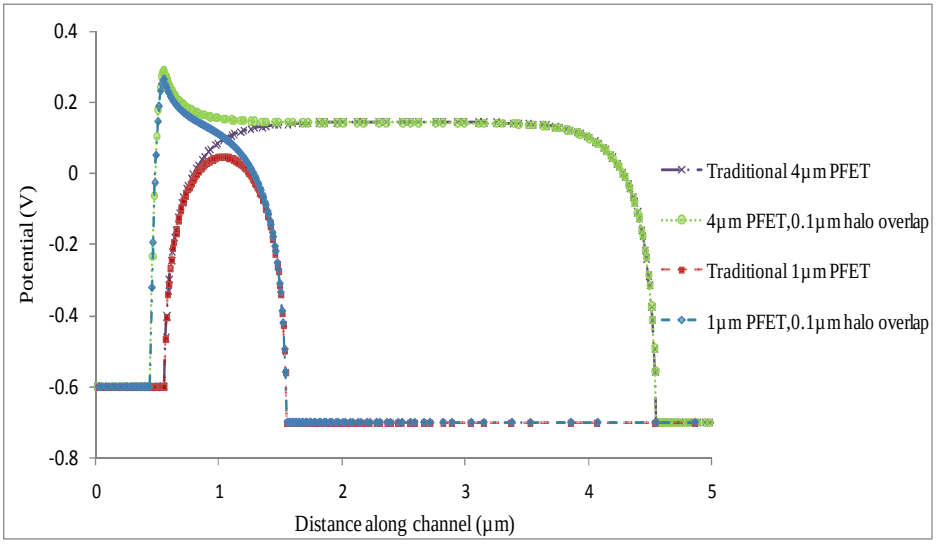


Figure 3.3: Channel potential across PFETs(L_{eff} = 1 µm and 4 µm) for V_{DS} = -0.1 V and V_{GS} = 0 V. A lower potential barrier is seen for 1 µm PFET (traditional variety) indicating dependence of barrier height on channel length under low-field conditions.

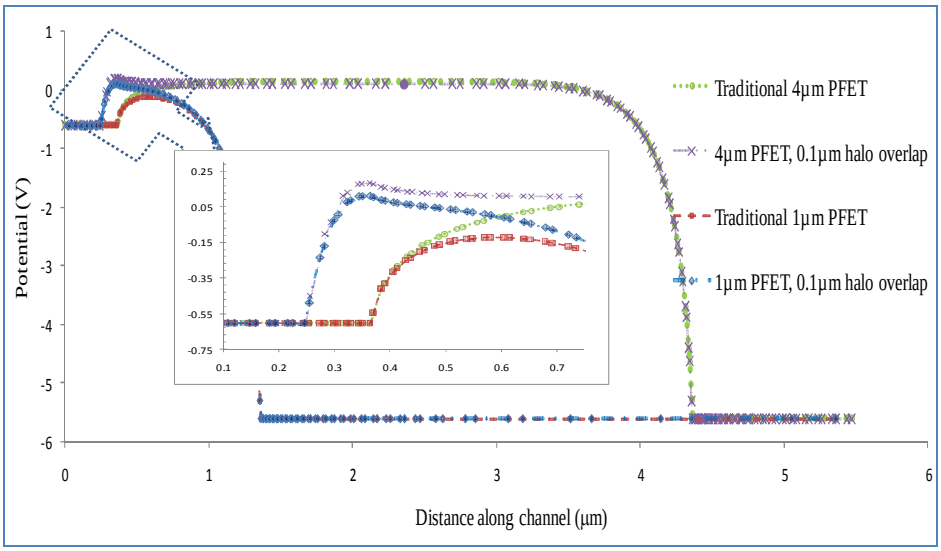


Figure 3.4: Channel potential across PFETs for V_{DS} = -5 V and V_{GS} = 0 V, (L_{eff} = 1 µm and 4 µm). The DIBL observed under saturation conditions is unacceptably high for the 1 µm non-enhanced PFET.

Figure 3.3 shows a significant reduction in the hole barrier height on the L = 1 µm non-enhanced PFET compared to the L = 4 µm device, even at a minimal drain bias. The accumulation mode PFET is highly susceptible to short-channel behavior compared to a traditional enhancement-mode device. The barrier lowering at low drain bias conditions would result in significant V_T *roll-off,* and unacceptably pronounced DIBL under high drain bias conditions as shown in Figure 3.4. The enhanced PFET does not exhibit this behavior at low drain bias, and is also quite resistant to barrier lowering in saturation conditions as shown in Figure 3.4.

The transfer characteristics were simulated for both traditional and barrier-enhanced PFETs, with results shown in Figure 3.5 (linear scale) and Figure 3.6 (log scale).

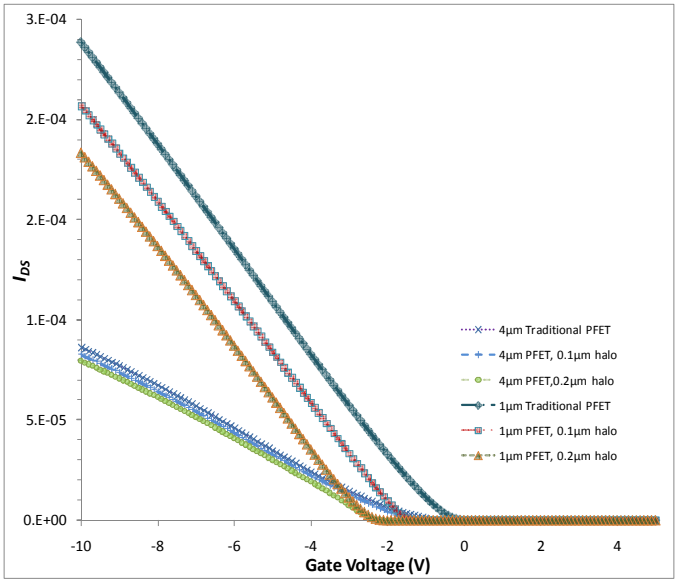


Figure 3.5: Linear-scale transfer characteristics for PFET devices with and without an enhanced source barrier (surface halo) at high drain bias (V_{DS} = -5 V) and L_{eff} at 4 µm and 1 µm.

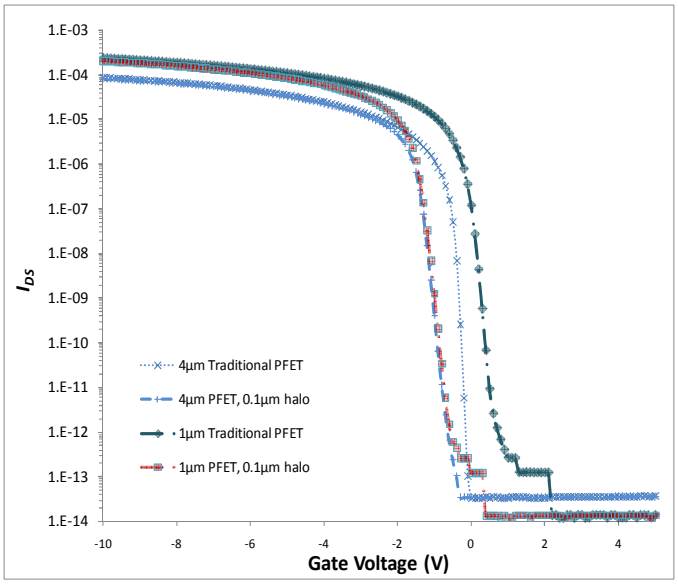


Figure 3.6: Log-scale transfer characteristics for PFET devices with and without an enhanced source barrier (surface halo) at high drain bias (V_{DS} = -5 V) and L_{eff} at 4 µm and 1 µm.

Figure 3.5 shows the transfer characteristics for PFET devices on a linear scale. The drain is at a constant bias of -5 V, which causes the device to transition from the linear regime (low gate bias) into saturation (high gate bias). Results are shown from simulated devices at channel lengths of 1 µm and 4 µm without enhancement, and with enhanced source barriers of 0.1 µm and 0.2 µm wide. The enhanced barriers increase the threshold voltage of the devices (as would be expected), however Figure 3.5 shows only a minor decrease in current drive consistent with the V_T shift.

Figure 3.6 shows a comparison of the off-state behavior, where an enhanced barrier of 0.1 µm width shows marked suppression of DIBL while still maintaining an acceptable threshold voltage. With no source barrier enhancement, DIBL results in a significant lowering of the threshold voltage, causing the 1 µm device to appear to turn on with V_{GS} slightly positive. With the enhanced barrier, the 1 µm and 4 µm devices have negligible differences in V_T, with almost perfect overlay in the subthreshold regime. It should be noted that the subthreshold swing (SS, mV gate voltage / decade current) does increase with the enhanced source barrier. This is due to the additional depletion capacitance associated with the source end of the device with the formation of this n-type region. While there is a slight compromise in this particular parameter, the suppression of DIBL with a minimal compromise in on-state current drive makes the tradeoff easily justified.

3.4 CONCLUDING REMARKS

In the preceding section the implications of incorporating LDD for NFET and N-barrier for PFET was investigated. Silvaco Atlas device simulation software was used to model the device characteristics. Careful trade-offs were considered in order to enhance the off-state performance, without compromising on-state current significantly. The LDD/surface halo dose and length were optimized accordingly to determine the initial values for process design parameters, and to explore the influence of parameters that could not be adjusted.

For both the LDD-NFET and source barrier enhanced PFET, an n-type region of 0.1 µm width (or length in the context of the transistor channel) appears to improve the targeted off-state behavior with minimal compromise in the on-state performance. The question remains whether or not the results from ideal device structures in simulation can be realized in fabricated devices. The NFET is not that sensitive to variations in the modified region, however the PFET structure is extremely sensitive and variation can significantly degrade the device performance. The ability to fabricate device structures within the tolerances needed for this investigation would not appear to not be feasible without extremely tight process control on lithography overlay and process biases.

Considering that such control is not practical for the process technology used, a testchip layout and process integration schemes were developed that allowed for process bias and overlay variation while still providing device structures with precise feature offsets. This was done by setting up arrays for each device structure under investigation that had design offsets of critical features in small increments that provided the required

precision. In addition, several integration schemes were used which resulted in different types of LDD / surface halo structures. Details of the testchip design and process integration are discussed in chapter 4.

CHAPTER 4

PROCESS INTEGRATION

4.1 INTRODUCTION

In order to study different types of LDD/N-barrier implant and their implications for device performance, five process flows and mask structure designs were incorporated in this study. All the strategies were based on double-level gate layers; a dummy gate and main gate were used at different levels in the process flow to accomplish the desired structures. Fine resolution alignment verniers of size one micron with 0.1 micron shift and two micron spacing was used to quantify overlay errors between the two gate structures. The dummy gates were arrayed with an incremental shift of (+/-) 0.1 micron to account for expected overlay error associated with the GCA g-line stepper at the RIT SMFL. The dummy gate overlapped or under-lapped the main gate by either 0.1 micron or 0.2 microns, realizing various types of LDD and N-barrier implanted structures. In order to emulate the TFT fabrication in the display industry, a gate oxide thickness of 500 Å was used for this study. This gate oxide thickness seemed to be in accordance with both the constraint implied by the GIDL on gate oxide thickness [11] as well as in the inability of the display industry at present to deposit the high-quality thin gate-oxide for

TFT fabrications. The following sections will describe the various process options and associated device structures, limiting the discussion to details which show the process-device connection.

4.2 TEST CHIP LAYOUT

A new eight lithographic level mask set was designed to incorporate the device enhancements (LDD/N-barrier) on the established CMOS TFT process (see Figure 4.1). The mask set featured four varieties of NFETs and PFETs with various channel length and constant width. The mask was designed by coding in the SILVACO L-Edit software to realize perfectly stepped offset structures. The critical features were arrayed to account for overlay issues with GCA G-line stepper at RIT SMFL and to realize optimally aligned structures. Over-lapped and under-lapped dummy-gate have been shown in Figure 4.2. Figure 4.2 (a) is representative of the Source/Drain last and self aligned to main-gate strategy. Figure 4.2 (b) is representative of both LDD/N-Barrier last and self aligned to main-gate and gate-last strategy. For the asymmetric TFT PFETs the dummy-gate extends over the drain side to block the N-barrier implant. A representative alignment/misalignment of the double-level gate has been shown in Figure 4.3 for a 2X24 micron (LXW) device structure. Figure 4.3 (b) symbolizes a perfectly aligned main-gate and dummy gate, whereas Figure 4.3 (a) and 4.3 (c) shows the misalignment of +1 micron and -1 micron in horizontal direction respectively. The mask also features CBKR and Van der Pauw test structures (see Figure 4.4) to quantify contact and sheet resistance apart from P-N junctions and MOS capacitors.

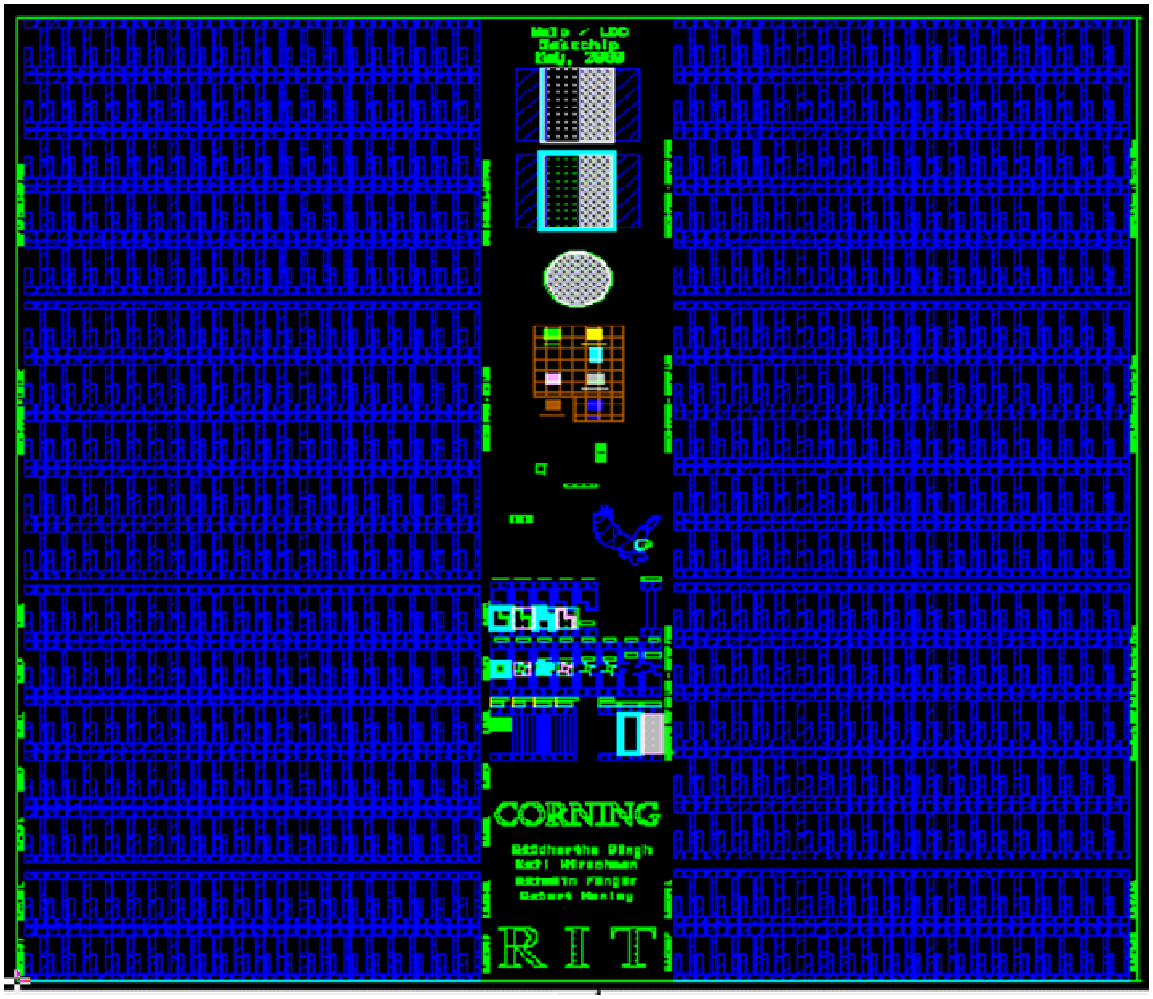
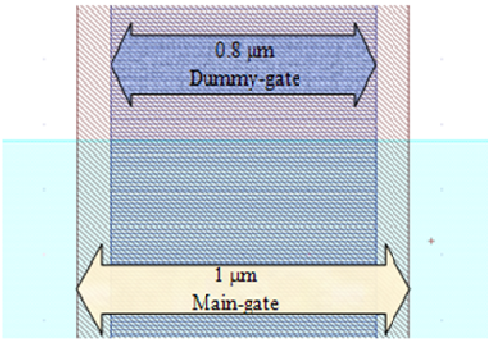
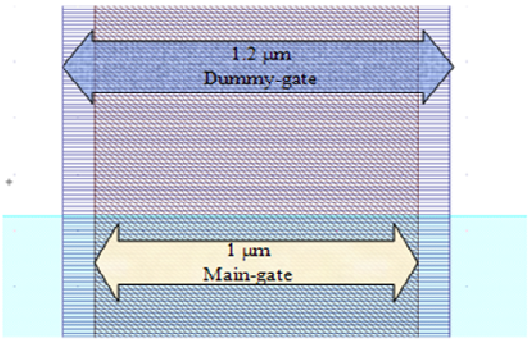


Figure 4.1: New eight lithographic levels Test chip lay out.

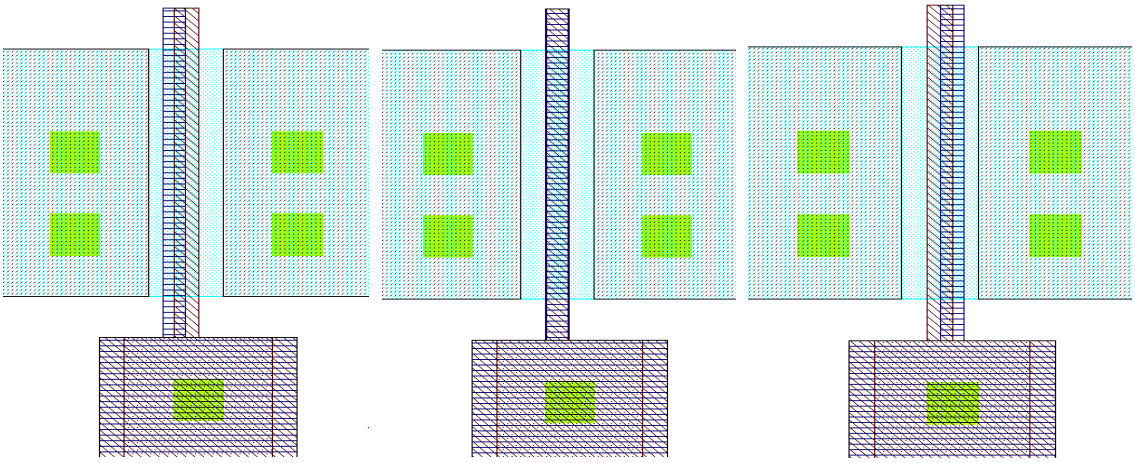


(a)



(b)

Figure 4.2: (a) An overlapped LDD structure as source/drain last and self-aligned to main gate and (b) Showing LDD/N-Barrier last and self-aligned to main gate and gate-last strategy



(a) (b) (c)

Figure 4.3: Overlay of the double level of the two-layered gate structure for 2X24 micron (LXW) device structures. (a) Dummy gate is off by -1 µm from main gate in horizontal direction, (b) Dummy gate and main gate are perfectly aligned to each other(c) Dummy gate is off by +1 µm from main-gate in horizontal direction.

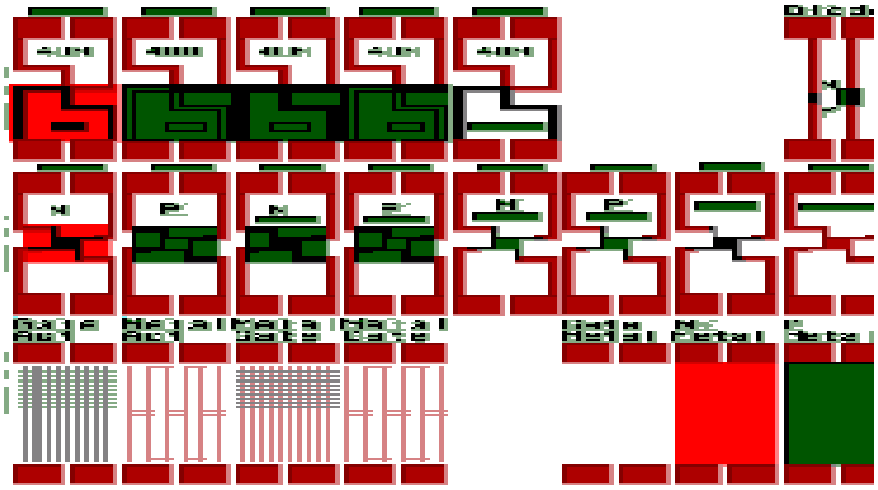


Figure 4.4: CBKR and Van der Pauw test structures to quantify contact and sheet resistance

4.3 PROCESS DESIGN AND FABRICATION FLOW

4.3.1 SYMMETRIC LDD/ N-BARRIER FIRST, SOURCE/DRAIN LAST AND SELF-ALIGNED TO MAIN GATE STRATEGY

In this strategy the LDD for NFET and N-barrier for PFET were aligned to a dummy-gate. Both the LDD as well as N-barriers were realized through common blanket implant step. The source and drain in this strategy were self-aligned to the main-gate structure. The LDD/N-barriers are totally overlapped by the final gate structure as seen in Figure 4.5.1. The key process design steps are displayed in the subsequent sequential processing steps.

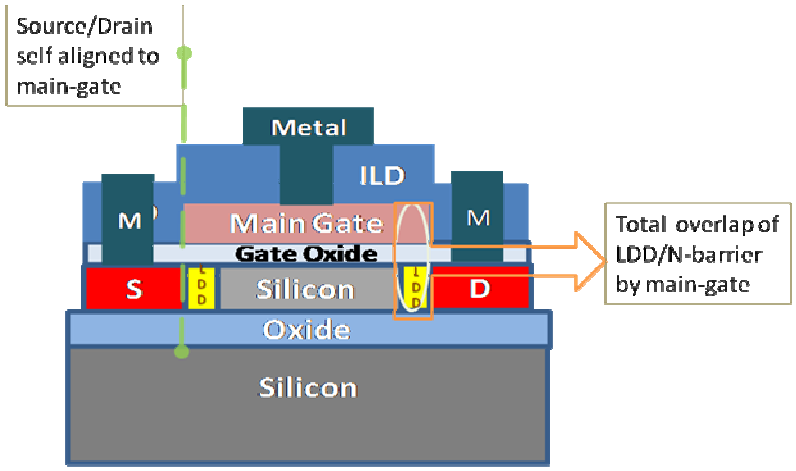
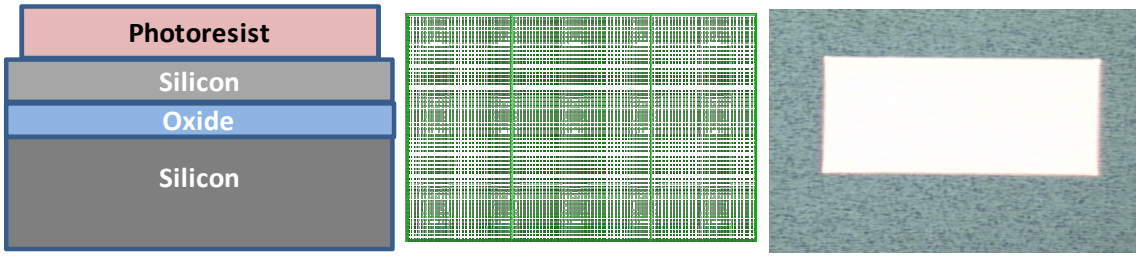


Figure 4.5.1: Symmetric LDD/N-barrier implanted first, source/drain implanted last and self-aligned to main gate

The starting SOI wafer had <100> crystal orientation and P-type (Boron) dopant with the resistivity in the range of 10-200 ohm-cm. The specified thickness of the wafer was ~ 500-550 µm, with the device layer thickness of 190 +/- 5 nm and buried oxide layer of 375 +/- 5 nm. A LPCVD LTO of 1000 Å screen oxide layer (SiO_2) was

deposited to serve two purposes: to avoid channeling during P+ backside implant and to protect silicon surface during initial processing. The P+ backside implant was followed by anneal at 1000 ºC for 30 minutes in Bruce furnace in N_2 ambient for backside dopant activation. The backside implant was performed in order to provide adequate back side body contact with the chuck while testing. The protective screen oxide was removed using a wet HF dip (10:1 :: H_2O:HF), for a length of ~ 1 minute.

The active litho was performed using the new mask set with device enhancements (see Figure 4.5.2). The standard Team Eagle baseline CMOS resist coat and develop recipes were used on 4" SVG wafer track. Necessary modifications in GCA g-line stepper jobs were made for the new mask set. Plasma of SF_6 and O_2 was used to etch silicon, and to define the rounded edge mesa structure. This graded mesa structure forms a conformal deposition of gate dielectric, thus avoiding any gate leakage due to thin region of gate dielectric. The photoresist was removed in a heated solvent strip bath.

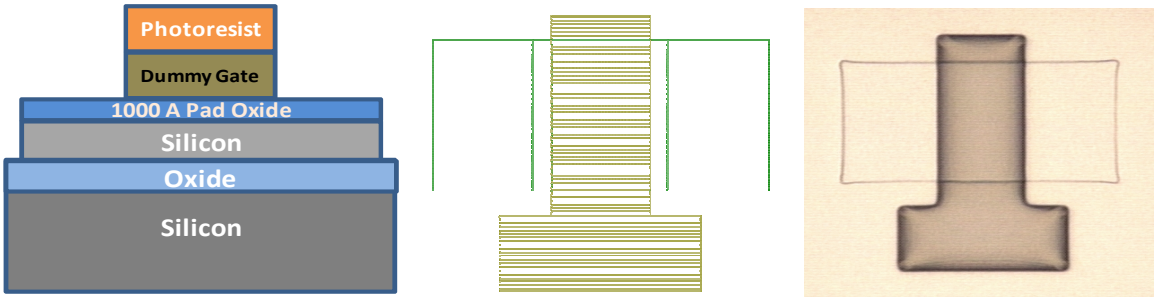


(a) (b) (c)

Figure 4.5.2: Active litho step for MESA etch definition, (a) cut-down (b) mask layout (c) device image.

A dummy screen oxide of 1100 Å was deposited in LPCVD system following the clean. Next 4900 Å of Molybdenum was sputtered using physical vapor deposition system. Dummy gate lithography was done, incorporating structures that would underlap

the main gate (see Figure 4.5.3). A reactive ion etching tool was used to etch the Molybdenum. Plasma chemistries used to etch were CF_4 and Oxygen. The photoresist was removed in a heated solvent strip bath. The gate etch defined the dummy gate, to which low dose blanket Phosphorus implants were aligned (see Figure 4.5.4). This implant served as LDD for NFET and N-barrier for PFETs.



(a) (b) (c)

Figure : 4.5.3: Dummy Gate Litho pattern (a)cut-down (b)mask image (c)device image.

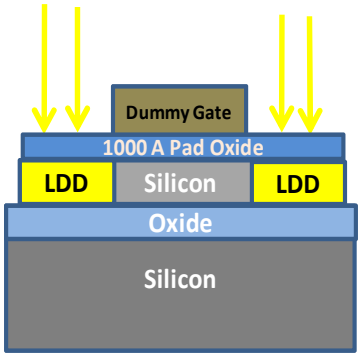
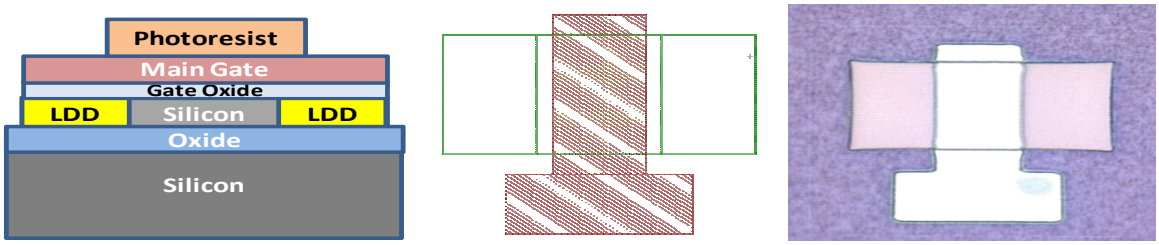


Figure 4.5.4: Low dose blanket Phosphorus implants aligned to dummy gate to serve as LDD for NFET and N-barrier for PFETs.

Following the LDD implant, 2500 Å of additional TEOS oxide was deposited in LPCVD system to preserve the alignment marks for a later reference, so as to determine the underlap of LDD with main gate. The alignment saver lithography was done to protect the additional oxide and alignment marks during subsequent oxide etch, and

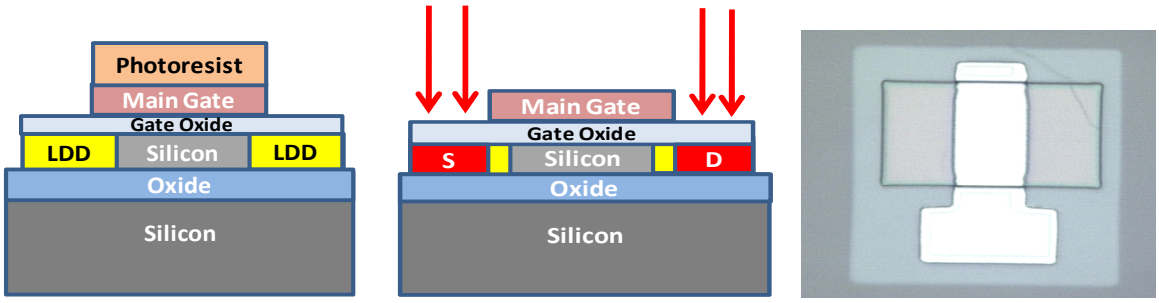
Molybdenum etch. The protective screen oxide was removed using a wet HF dip (10:1 :: H_2O:HF), for a length of ~ 3 minute. Next the Molybdenum was etched in Transene Type A aluminum etch (phosphoric, nitric and acetic acid) at 50 ºC. The remaining dummy gate oxide was removed using wet HF dip (10:1 :: H_2O:HF), for a length of ~ 3 minute. The photoresist from alignment saver litho was removed in heated solvent bath. Next piranha clean was done and the LTO gate oxide of ~500 Å was deposited in LPCVD system for the gate oxide. Following gate oxide deposition, 5000 Å of Molybdenum was again sputtered using the physical vapor deposition system for the main gate. Next the main-gate lithography (see Figure 4.5.6) was done and Molybdenum was etched in RIE tool with plasma chemistries comprised of CF_4 and Oxygen. The gate region defined the S/D regions implants which were self-aligned to the main gate.



(a) (b) (c)

Figure 4.5.6: Main gate lithography (a) Cut-down, (b) mask image (c) device image

The photoresist was removed in heated solvent strip bath following the gate etch (see Figure 4.5.7.(a)). Another PECVD based TEOS oxide layer was deposited to protect the Molybdenum gates during subsequent anneal step and to serve as implant screen for the source and drain implants (see Figure 4.5.7(b)).



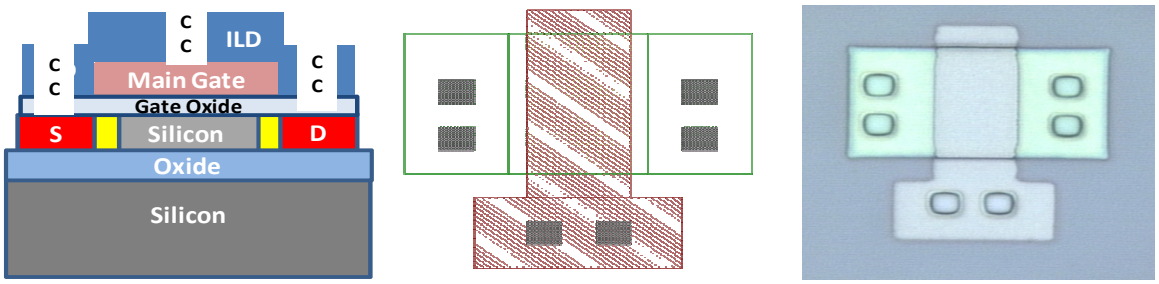
(a) (b) (c)

Figure 4.5.7: Source/drain implants self aligned to main gate (a) Cut down, (b) Cut down image depicting source/drain implants, (c) device image

Next the N+ source and drain lithography defined the NFET device. A single Phosphorus (P_{31}) implant was used to form the N+ source/drain. Branson Asher was used to remove resist in Oxygen-based plasma. The P+ source and drain lithography defined the PFET device. Fluorine was used to pre-amorphize the P+ Source/Drain region followed by p-type dopant Boron (B_{11}) implant. Fluorine amorphizes the crystalline structure of Silicon. The amorphous structure helps to permit higher level of dopant activation, as during annealing, the silicon layer re-crystallizes, incorporating dopant ions into the lattice. After implant, photoresist was removed in Branson Asher and wafers were cleaned in a heated piranha bath. Following clean, additional 4000 Å of PECVD TEOS oxide was deposited to isolate the devices from metal. The wafers were annealed in a horizontal furnace at 600 ºC for two hours in an inert ambient.

Contact cut lithography was done to open up the window in resist for the contact cut etch. The contact cut etch was done in 10:1 buffered oxide etch (10:1 :: H_2O:HF) with surfactants for approximately 10 minutes. Next photoresist was removed in heated solvent strip bath (see Figure 4.5.8). In order to ensure that all oxide had been removed in

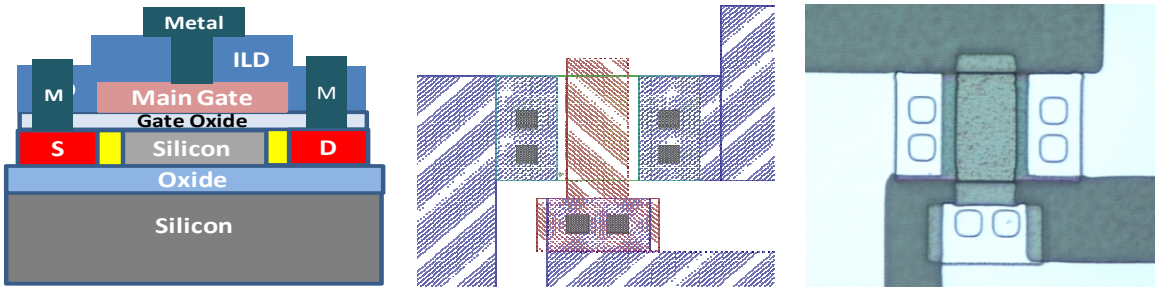
the contact regions, an additional dip in buffered oxide etch was done immediately before metal deposition.



(a) (b) (c)

Figure 4.5.8: Device structure after stripping resist from Contact cut lithography (a)cut down, (b) mask image, (c) device image

Next 7500 Å of Aluminum was sputtered onto the wafers using physical vapor deposition system. Aluminum is the main interconnects layer as well as the primary metal for the bond pads. Metal gate lithography was done and aluminum was then etched in Transene type A aluminum etch (phosphoric, nitric and acetic acid). Photoresist was stripped using heated solvent bath (see Figure 4.5.9). The substrate was sintered in Forming gas (H_2/N_2) at 425ºC for 30 minutes.



(a) (b) (c)

Figure: 4.5.9: Device structure after stripping resist from metal gate lithography (a) cut down image (b) mask image (c) device image

The following sections will describe the other process options and associated device structures, limiting the discussion to details which show process-device connection.

4.3.2 ASYMMETRIC N-BARRIER FIRST, SOURCE/DRAIN LAST AND SELF ALIGNED TO MAIN GATE STRATEGY

This strategy incorporates a dummy gate that extends over the drain region, in order to realize an asymmetric device with an N-barrier on the source side of the PFET. A surface halo implant is desired on the source side to form an N-barrier that would shut off the channel in the off-state to decrease the DIBL effect on the accumulation mode PFET. Symmetric barrier implants on both the source and drain would potentially enhance GIDL current in the off-state of the transistor [2]; hence asymmetric transistors are used to isolate the suppression of DIBL. The N-barrier is self-aligned to the dummy gate. The source/drain is self-aligned to the main gate in this strategy. The N-barrier is totally overlapped by the main gate as seen in Figure 4.6.1.

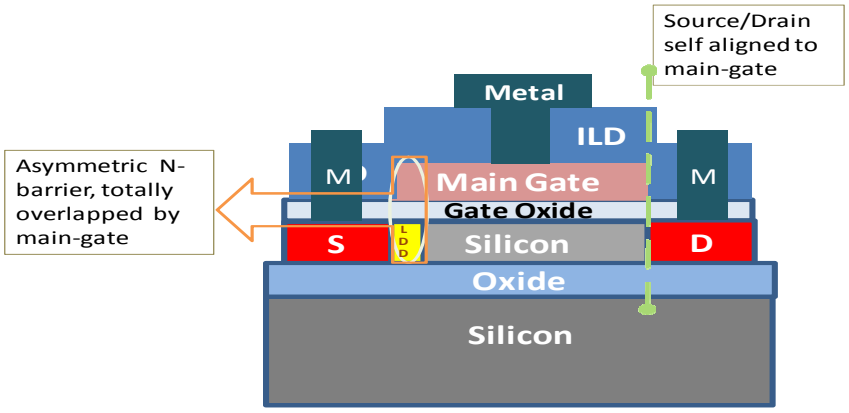
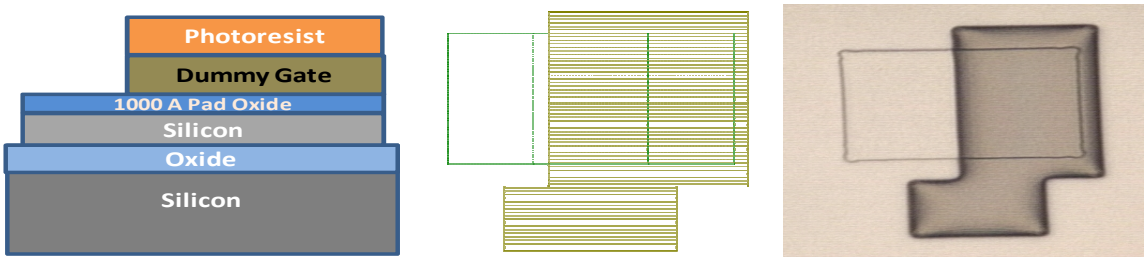


Figure 4.6.1: Asymmetric N-barrier implanted first, source/drain implanted last and self-aligned to main gate

The dummy gate lithography pattern extended over the drain region and etches in RIE tool as mentioned in Section 4.6.1 yielded the asymmetric dummy gate (see Figure 4.6.2). Following the gate etch resist was stripped in heated solvent bath and a low dose blanket Phosphorus implant was performed (see Figure 4.6.3). This low dose Phosphorus

implant was expected to form a surface halo that would shut off the channel in off-mode of the accumulation mode PFET, hence eliminating DIBL effects.



(a) (b) (c)

Figure 4.6.2: Dummy gate lithography, yielding asymmetric gates (a) cut down, (b) mask image, (c) device image

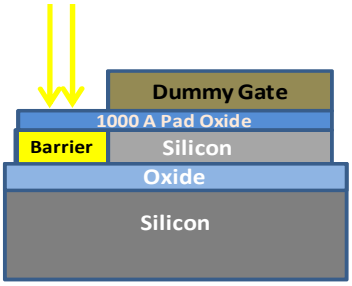


Figure 4.6.3: A blanket low dose Phosphorus implant expected to form a surface halo on the source side

The preceeding steps were similar to as mentioned in Sections 4.3.1 to yield the final structure of Figure 4.6.1.

4.4 SYMMETRIC SOURCE/DRAIN FIRST, LDD/N-BARRIER LAST AND SELF-ALIGNED TO MAIN GATE STRATEGY

In this method the source and drain are self-aligned to a dummy gate and the LDD/N-barrier implant is self-aligned to the main gate such that the main gate does not

overlap it. The LDD/N-barrier implant is self-aligned to the main gate as seen in Figure 4.7.1, and realized through a blanket implant via a common implant step.

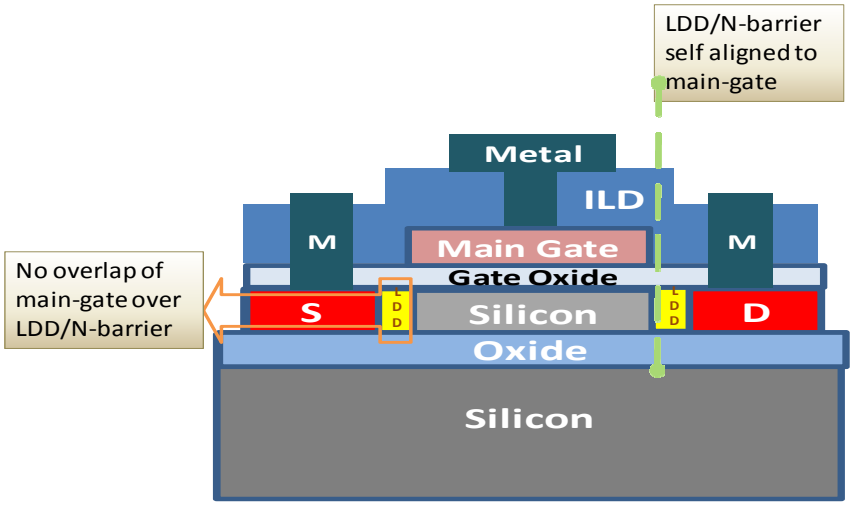


Figure: 4.7.1 Source/Drain implanted first, LDD/N-barrier implanted last, and self-aligned to main gate

In this strategy after the RIE etch of dummy gate Molybdenum the source/drain implants were performed (see Figure 4.7.2). Following it the process steps mentioned in Section 4.6.1 yielded main gate structure to which the LDD implant were aligned (see Figure 4.7.3).

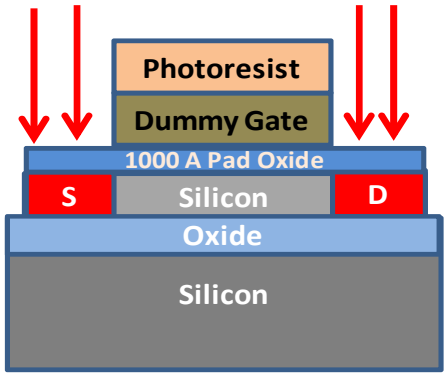


Figure: 4.7.2: Source/ drain implants aligned to dummy gate

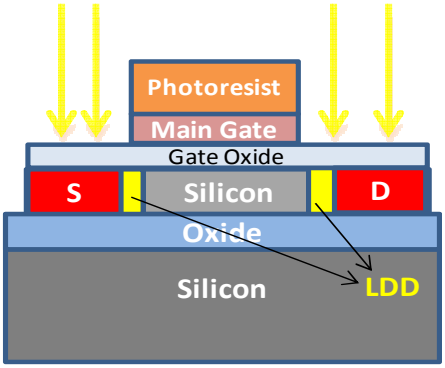


Figure: 4.7.3: LDD implants aligned to main gate

The subsequent steps were similar to Section 4.3.1, that yielded final structure of Figure 4.7.1, where the main-gate does not overlap the LDD implants.

4.5.1 SYMMETRIC NON-SELF-ALIGNED NFET WITH GATE LAST AND DUMMY GATE UNDER-CUT STRATEGY

The advantage of this strategy was to realize device structures with precise control on LDD placement relative to the source/drain regions. In this study, this strategy was used only for NFET devices (see Figure 4.8.1) for several reasons. For both NFET and PFET devices to be realized using this strategy, NFET and PFET dummy gate patterning would have to be done separately, with the PFET gate mask being a combination of the PFET gates and other design layers to protect the NFET active (mesa) regions from the p+ implant. In addition, this strategy does not accommodate the asymmetric PFET design which is of particular interest.

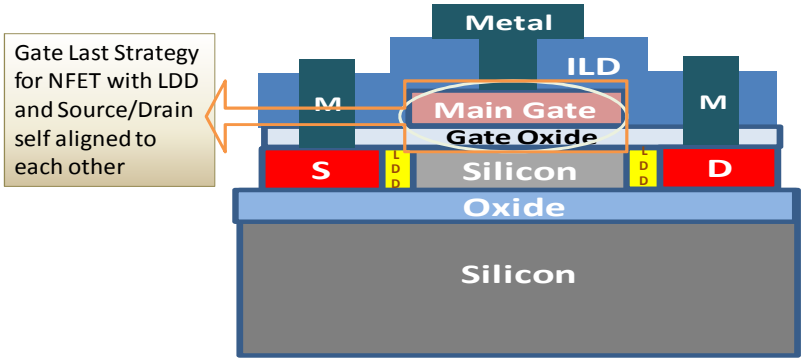


Figure 4.8.1: Symmetric non-self aligned NFET with gate last and dummy gate under-cut strategy

The source/drain and LDD are self-aligned to a dummy gate, and thus to each other. The photoresist was not stripped off after depositing, patterning and etching the

Molybdenum for the dummy gate formation. The source drain implants were self-aligned to the dummy gate pattern (see Figure 4.8.2). This preserved photoresist mask enabled the dummy-gate undercut in Transene type A aluminum etch (phosphoric, nitric and acetic acid) after the source/drain implant (see Figure 4.8.3). After the dummy gate under-cut the photoresist was stripped and LDD implants were done, which was self-aligned to the "shortened" dummy gate and, in turn, to the source/drain regions (see Figure 4.8.4). The main-gate had a range of overlap dimensions due to the gate alignment offset array.

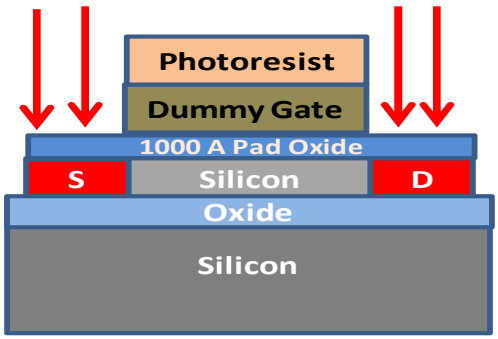


Figure 4.8.2: Source/Drain implant. Aligned to dummy gate.

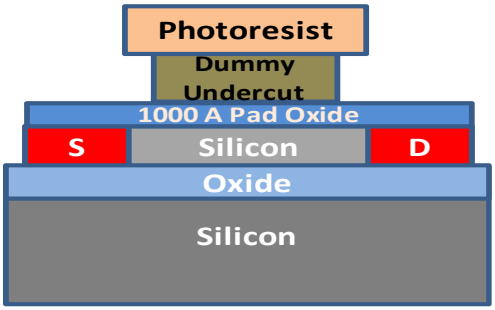


Figure 4.8.3: Dummy gate under cut in Transene type A aluminum etch.

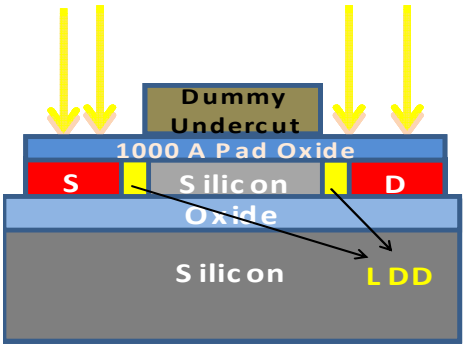


Figure : 4.8.4: LDD implants self-aligned to the "shortened" dummy gate and, in turn, to the source/drain regions

The subsequent steps were similar to as mentioned in Section 4.3.1 and yielded the final structure of Figure 4.8.1.

4.5.2 SYMMETRIC NON-SELF-ALIGNED PFET WITH GATE LAST AND NO BARRIER IMPLANT STRATEGY

This strategy was used to realize PFETs only on a wafer, without any surface halo implant to form an N-barrier. The region of P-body between the accumulated channel and the P+ source/drain was expected to act as a "P-LDD". The source/drain implants were self-aligned to a dummy gate. The mask design includes main gates that will either overlap (no P-LDD) or under-lap (P-body LDD) the source/drain regions. The main gate with an under-lap is shown in Figure 4.9.1. The process flow for this strategy was similar to that mentioned in Section 4.3.1 with an exception to surface halo implant to yield the final device structure of Figure 4.9.1.

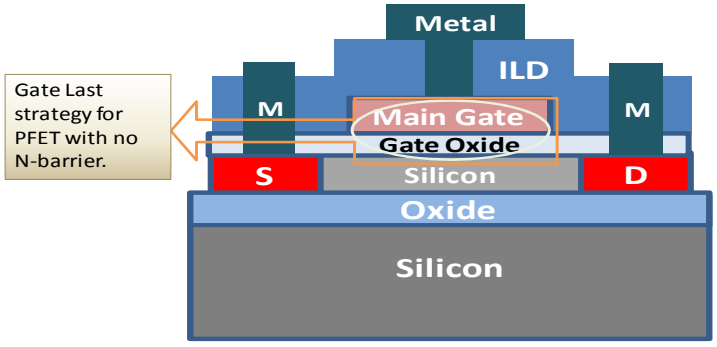


Figure 4.9.1: Gate last strategy for PFET with no N-barrier implants on source/drain. This strategy had overlap as well as under-lap of main gate over source/drain region.

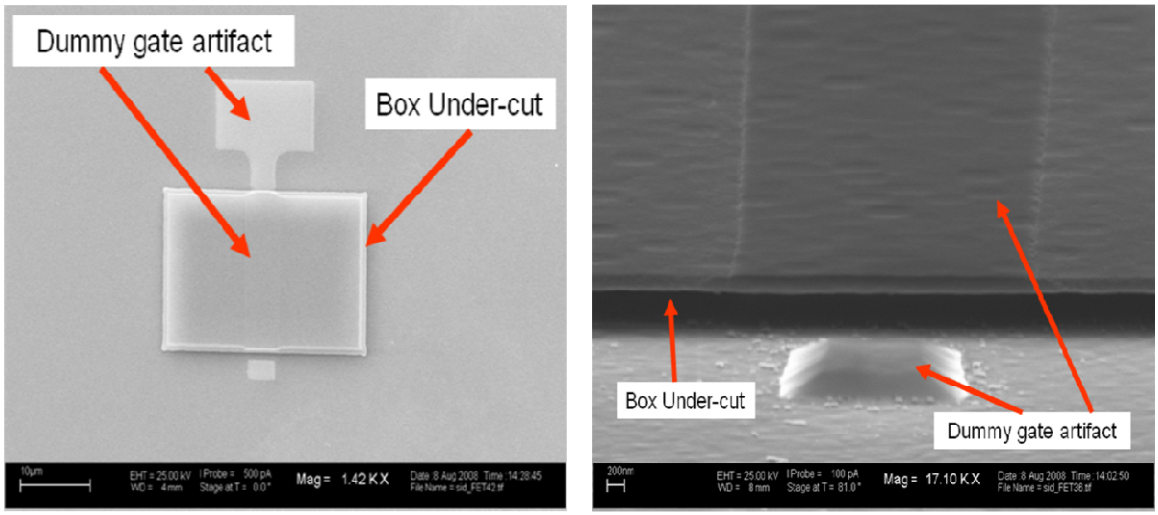
The main gate was designed to either provide S/D overlap, when considering a center-aligned broad gate, or S/D underlap (gap formation), when considering a center-aligned

narrow gate. This strategy was designed to have “native” LDD structures formed by the lightly doped background p-type silicon regions, resulting in either single-sided (offset broad gate) or double-sided (narrow gate) LDD PFETs.

4.6 PROCESS DEVIATIONS AND POTENTIAL COMPROMISE ON DEVICE PERFORMANCE

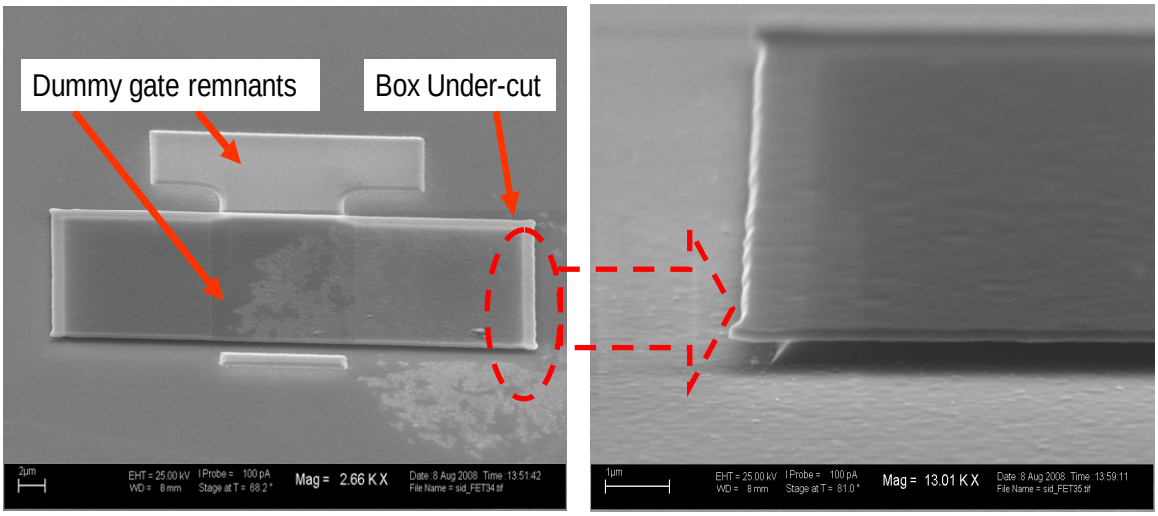
After the high dose S/D implant the molybdenum of dummy gate had left an artifact on the active area (see Figures 4.10 - 4.13), which through an optical microscope appeared exactly like residual molybdenum. In order to etch away this artifact from the active area, various wet chemistry processes were tried (some with HF) which resulted in significant undercut in buried oxide (BOX) layer of SOI (see Figures 4.10 and 4.11) in most of the treatment combinations.

Following AFM measurements, it was hypothesized that the material that appeared like residual sacrificial gate metal (molybdenum) in optical micrographs (see Figure 4.11 - 4.13) was actually a portion of the bottom part of the 400 nm buried oxide (BOX) layer. This material was formed where the gate metal was present – presumably due to some difference in thermal conditions. It is proposed that the silicon and oxygen distribution in the 400 nm SIMOX BOX layer must be supporting the formation of a non-stoichiometric SiO_x material. This material appears to be much more resistant to HF than SiO_2, and thus remains atop the field silicon regions even though the BOX has been removed outside of the mesa regions.



(a) (b)

Figure 4.10: SEM image exhibiting an artifact after dummy gate etch for 2X24 device that replicates in the portion where the dummy gate existed (a) device view, (b) a zoomed in view showing significant Box undercut.



(a) (b)

Figure 4.11: SEM image exhibiting an artifact after dummy gate etch for 12X24 device that replicates in the portion where the dummy gate existed (a) device view with significant surface roughness, (b) a zoomed in view showing significant Box undercut.

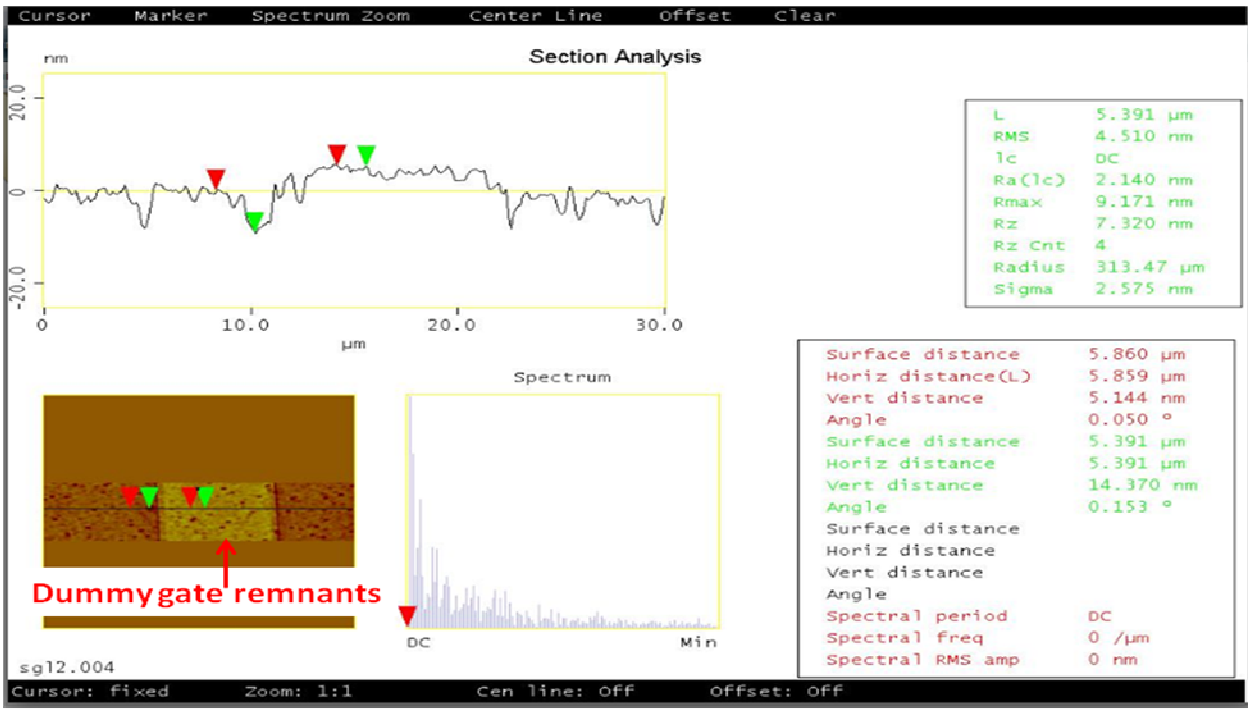


Figure 4.12: The AFM micrograph showing artifact where dummy gate existed before etch when the tip was swept over the active area.

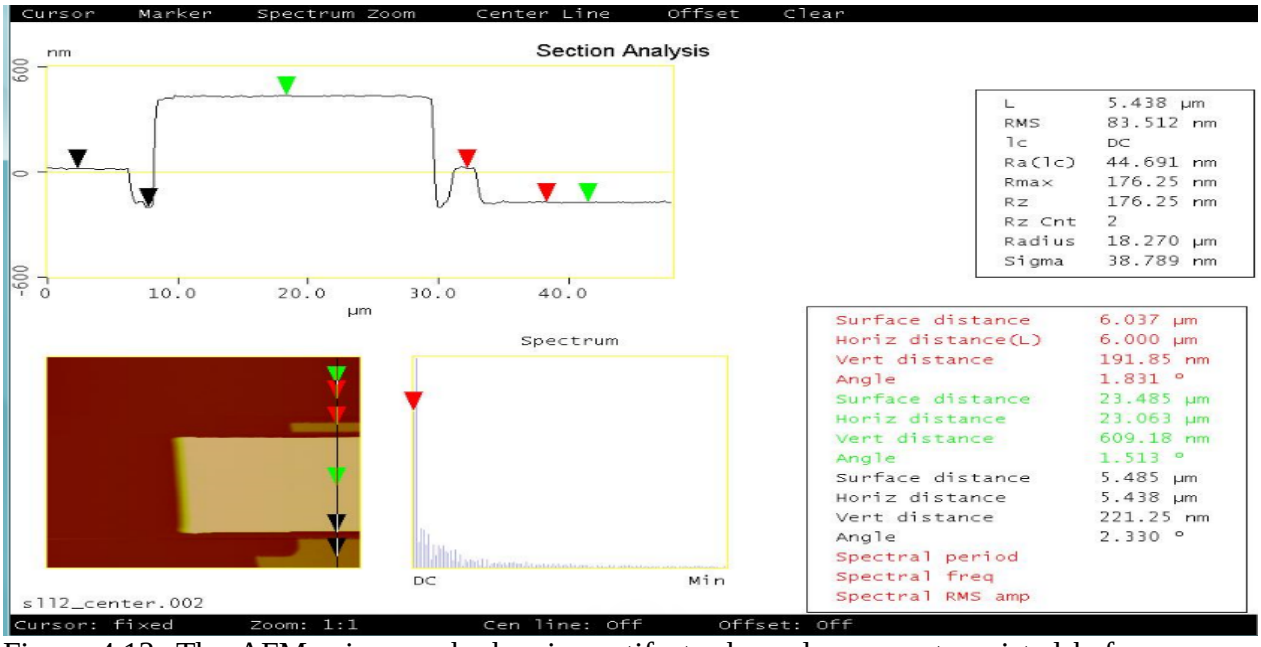


Figure 4.13: The AFM micrograph showing artifact where dummy gate existed before etch when the tip was swept across the MESA.

4.7 CONCLUDING REMARKS

The preceding section discussed five process flows to yields four varieties of NFET and PFETs along with the new eight-level mask set that was designed for the study. The process flow details were shown. The process options and associated device structures were discussed to show process-device connection. All the strategies were based on double-level gate layers; a dummy gate and main gate were used at different levels in the process flow to accomplish the desired structures. The dummy gates were arrayed with an incremental shift of (+/-) 0.1 micron to account for expected overlay error associated with the GCA g-line stepper at the RIT SMFL. The dummy gate overlapped or under-lapped the main gate by either 0.1 micron or 0.2 microns, realizing various types of LDD and N-barrier implanted structures.

Because of the process deviations described which could potentially compromise the quality of the silicon device regions; there was a significant concern about the ability to achieve working devices with characteristics that would isolate the influence of the factors under investigation. This section is referenced in Chapter 5 in certain cases where device performance results and comparisons are not easily explained.

CHAPTER 5

DEVICE TESTING AND CHARACTERIZATION

5.1 INTRODUCTION

The analysis of electrical characteristic of fabricated NFETs and PFETs will be presented in this section. The testing of the fabricated transistors on SOI substrates was done at RIT, with test devices in the gate alignment offset array identified from the alignment information preserved (alignment saver strategy, Chapter 4). An initial die map survey was done across the entire wafer and based on this initial sampling a single die was chosen to test all 21 transistors across the alignment offset array to determine the influence of a variety of overlapped or underlapped device features created in the described CMOS process flow (Chapter 4).

Device performance of the control devices is presented first to establish the comparison benchmark. This is followed by the investigation on the various LDD NFET structures implemented for GIDL suppression. Finally the investigation on the various PFET structures implemented for both DIBL and GIDL suppression is presented.

5.2 SIOG & SOI CMOS TRANSFER CHARACTERISTICS

The I_D-V_G transfer characteristics of low temperature TFT CMOS fabricated on SiOG and SIMOX SOI wafer is shown in Figure 5.1 [6]. The NFET is a traditional inversion mode device and the PFET is an accumulation mode device. The overdriven gate leads to GIDL in the off-state of the devices. Table 5.1 highlights the key device parameters extracted, including threshold voltage, effective channel mobility and subthreshold swing.

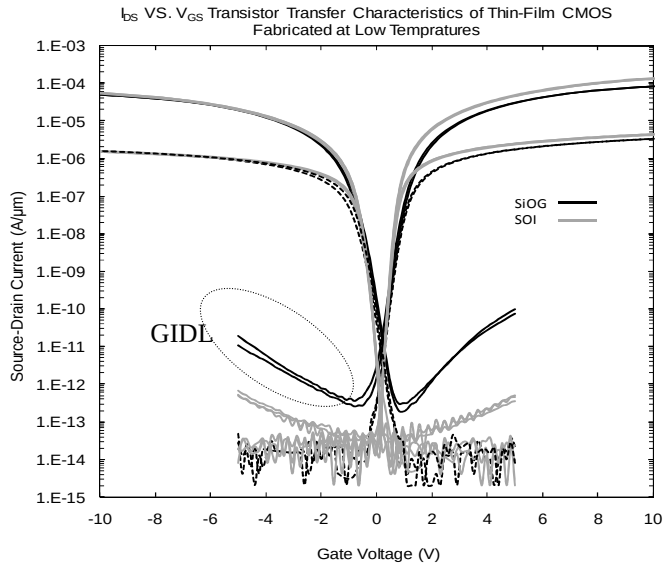


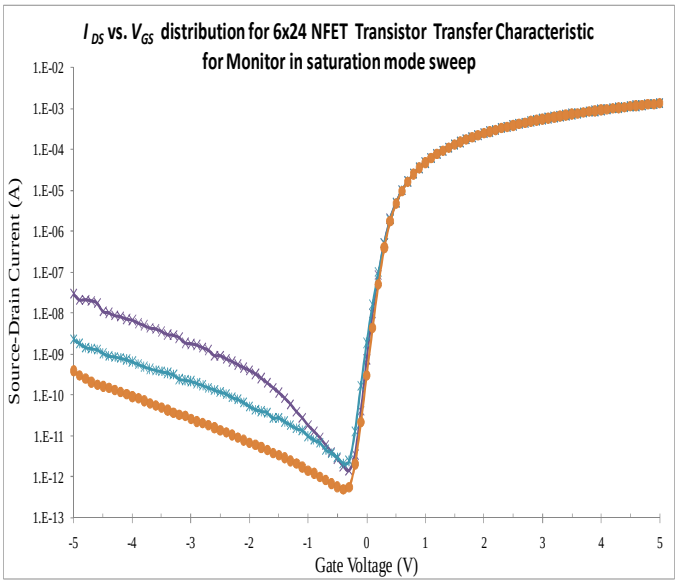
Figure 5.1: Comparison of I_D-V_G transfer characteristics of CMOS built on SiOG and SOI substrates. V_{DS} was set to a magnitude of 0.1 V for the linear regime characteristics and 5 V for the saturation regime. The NFET is a traditional inversion mode device and the PFET is an accumulation mode device [6].

Table 5.1: Extracted Device Characteristics [6]

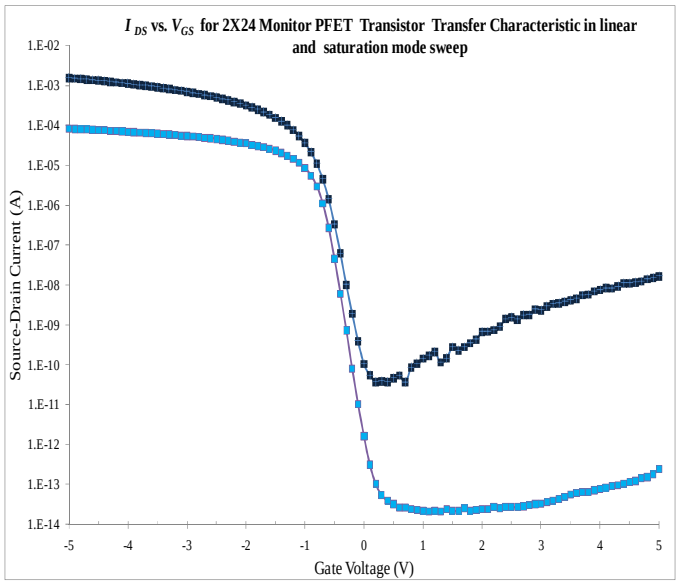
	Substrate	V_T (V)	μ_{FET} (cm^2/Vs)	Subthreshold Swing (mV/dec)
NFET	SiOG	0.95	410	160
	SOI	0.74	618	99
PFET	SiOG	-0.6	220	220
	SOI	-0.7	260	103

5.3 NON-ADJUSTED SOI DEVICE CHARACTERIZATION

The SOI monitor wafer devices were processed with no implanted adjustments for off-state performance enhancement, and served as controls for comparison while demonstrating the quality of the fabrication process. Transfer characteristics at low and high drain bias are shown in Figure 5.2. The monitor NFETs demonstrated GIDL during the saturation-mode sweep, with some variation on the level of current observed. The monitor PFETs also demonstrated GIDL, as well as DIBL at channel length of 2 µm. The characteristics shown in Figure 5.2 will be referenced for comparisons against devices that were fabricated with the designed enhancements to suppress GIDL and DIBL effects.



(a)



(b)

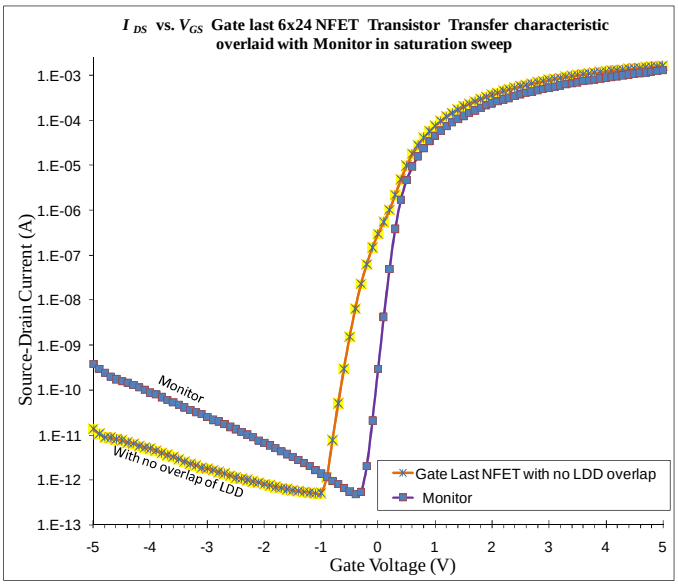
Figure 5.2: SOI Monitor wafer I_D-V_G transfer characteristics for (a) inversion-mode NFET and (b) accumulation-mode PFET. V_{DS} was set to a magnitude of 5 V for the NFET, with plot (a) showing a distribution of GIDL behavior. The PFET characteristics at low and high drain bias (-0.1 V and -5 V, respectively) demonstrate DIBL at a channel length of 2 µm.

5.4 CHARACTERIZING THE NFET LDD INFLUENCE ON GIDL

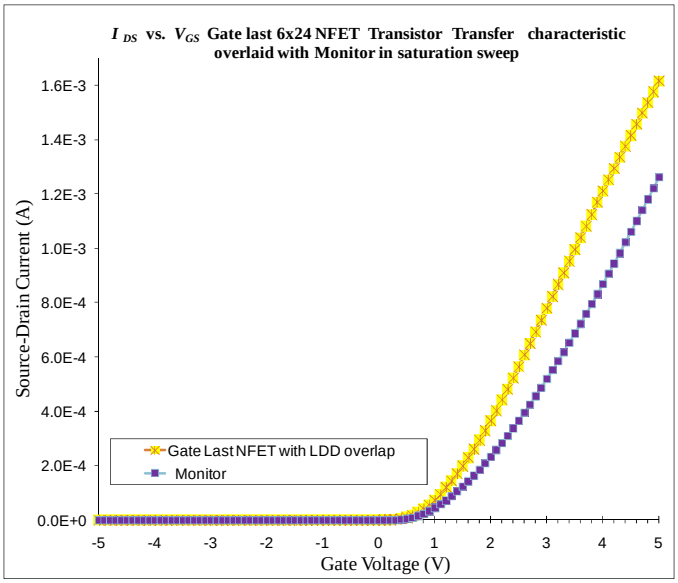
There were four varieties of NFET devices designed, three of which yielded devices for characterization. Variations on the NFET designs included the fabrication order of the LDD structures, source/drain (S/D) regions, and the gate electrode. This section will show representative data collected for the different varieties, and provide a discussion on the interpretation of electrical test results along with comparisons to the control devices.

5.4.1. *NON-SELF-ALIGNED NFET: (DUMMY-GATE UNDERCUT, NARROW MAIN-GATE LAST)*

The gate-last strategy with dummy-gate undercut strategy of Section 4.5.1 demonstrated improvement in GIDL current behavior as seen in Figure 5.3. In this strategy the S/D implants were aligned to the sacrificial dummy gate, and then a dummy gate undercut etch was done; LDD implants were aligned to this narrowed dummy gate and thus to the S/D implants. The main gate in the nominally aligned structure ideally has minimal (ideally zero) overlap of the LDD structures, however this depends specifically on the undercut etch results. The characteristic overlay shows significant improvement in GIDL current, as well as an increase in current drive in comparison to the best performing monitor NFET. While LDD structures typically reduce on-state current drive due to added series resistance, in this process strategy the LDD structures reduce the effective channel length instead. Note that there is a kink in the subthreshold characteristic that was consistently observed on this device treatment, perhaps due to interface traps that may be a result of the processing issues discussed in Section 4.6.



(a)

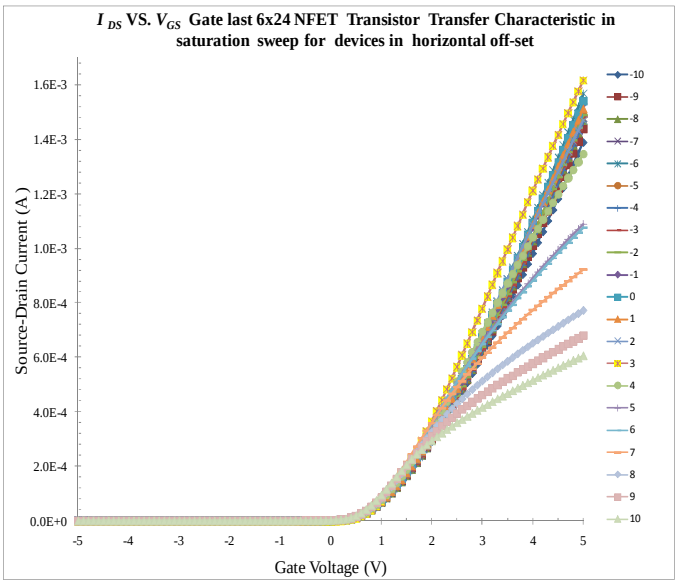


(b)

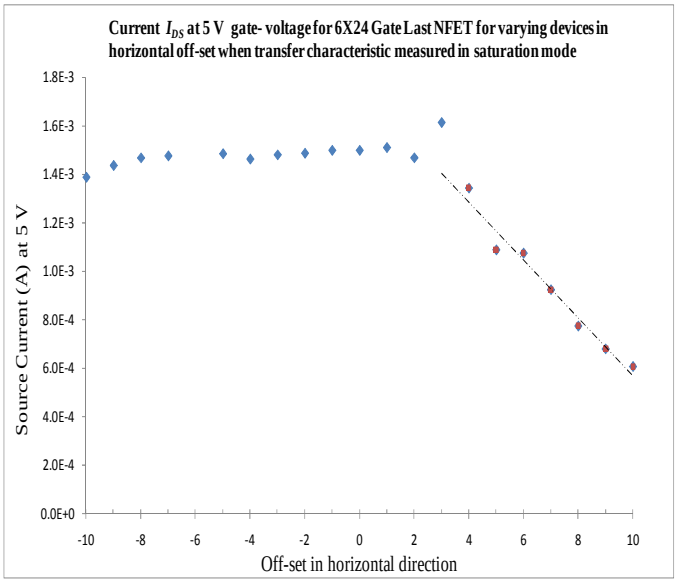
Figure 5.3: I_D-V_G transfer characteristics for non-self-aligned NFET with *(dummy-gate undercut, narrow main-gate last)* overlaid with monitor in saturation sweep (a) log scale (b) linear scale. V_{DS} was set to a magnitude of 5 V for the NFET, with plot (a) showing a significant improvement in GIDL behavior over monitor.

The forward drive current was observed to be strongly dependent on the LDD implant length, which was in turn dependent on the dummy gate offset (see Figure 5.4).

The forward drive current was observed to decrease systematically from the device with +0.3 µm designed offset to the device with +1.0 µm designed offset. The device with +0.3 µm designed offset seems to have the optimal LDD implant overlap; it exhibits the highest forward drive current as well as significant improvement in the GIDL characteristic. As the designed offset shifts more positive (towards the source end), there is a decrease in non-overlapped LDD length at the drain end, and an associated increase in series resistance (see Figure 5.5). While this may improve GIDL, the device provides less current drive until the shift no longer supports an inversion layer. As the designed offset shifts more negative (toward the drain end), the current drive appears relatively constant due to the total series resistance associated with the source and drain LDD regions remaining approximately the same (decreasing at drain end, increasing at source end). However, Figure 5.6 shows the increasing trend in GIDL as the designed offset shifts from +0.3 to -1.0 µm which can be attributed to the increase in drain-end LDD gate overlap; consistent with the discussions in Chapters 2 and 3, and the findings in references [2, 5]. Results support the argument that a greater degree of overlap of the gate over LDD leads to field crowding in the LDD portion of the channel and thus promotes band-to-band tunneling, making GIDL more prominent.



(a)



(b)

Figure 5.4: Saturation-mode transfer characteristics for various designed offsets in linear scale (a), with the value of current drive measured at V_G = 5 V plotted versus the designed offset (b).

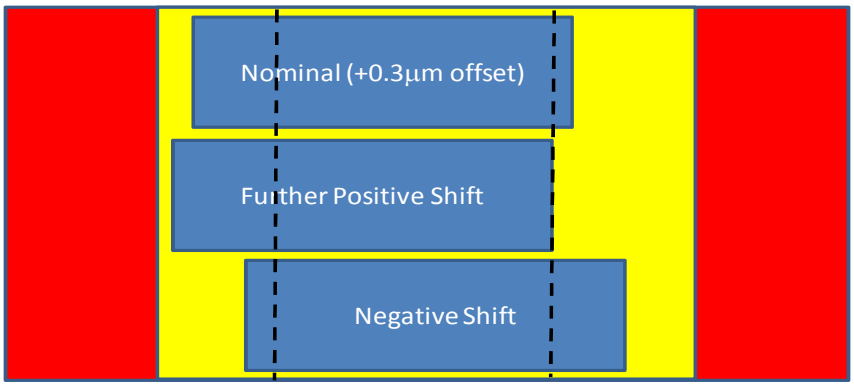
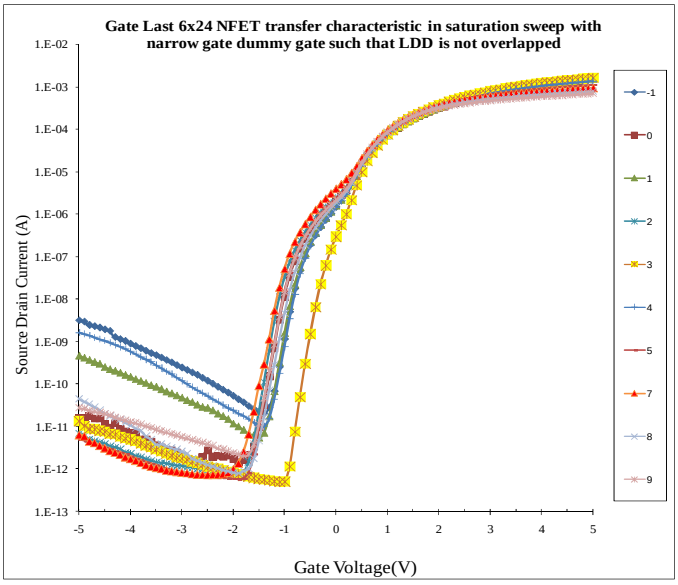
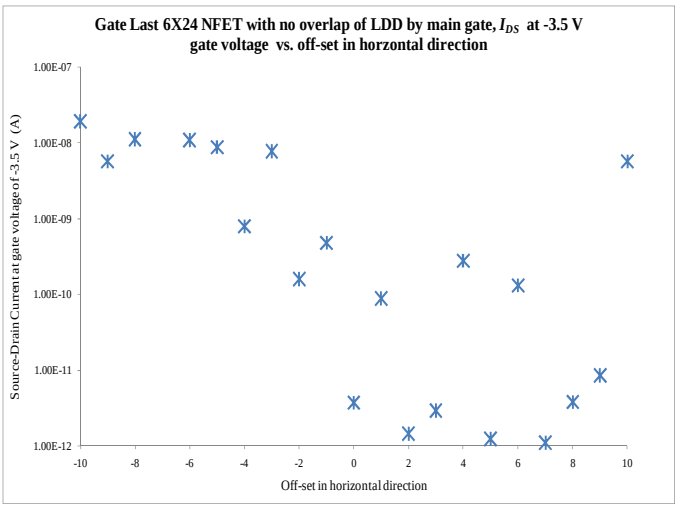


Figure 5.5: Replication of various main gate positions for non-self-aligned NFET with ***(dummy-gate undercut, narrow main-gate*** *last)* strategy depending on the gate offset shift.



(a)



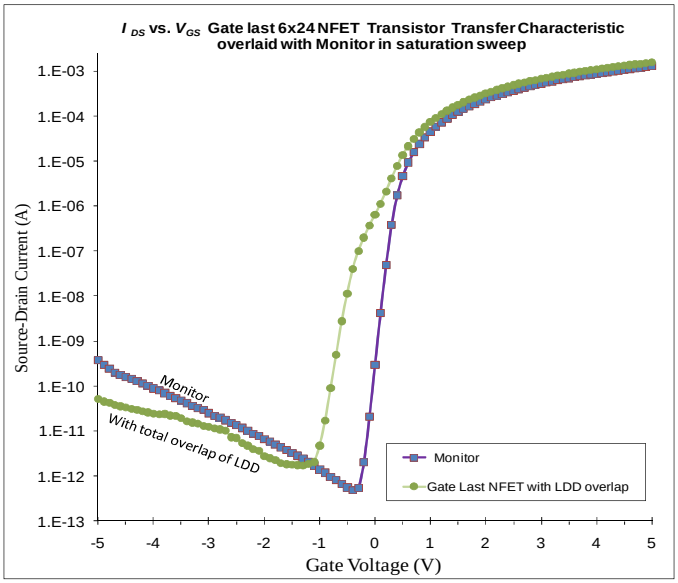
(b)

Figure 5.6: Saturation-mode transfer characteristics for various designed offsets (a), with the value of GIDL current measured at V_G = -3.5 V plotted versus the designed offset (b). Note the consistency in the subthreshold region distortion (kink), attributed to interface traps.

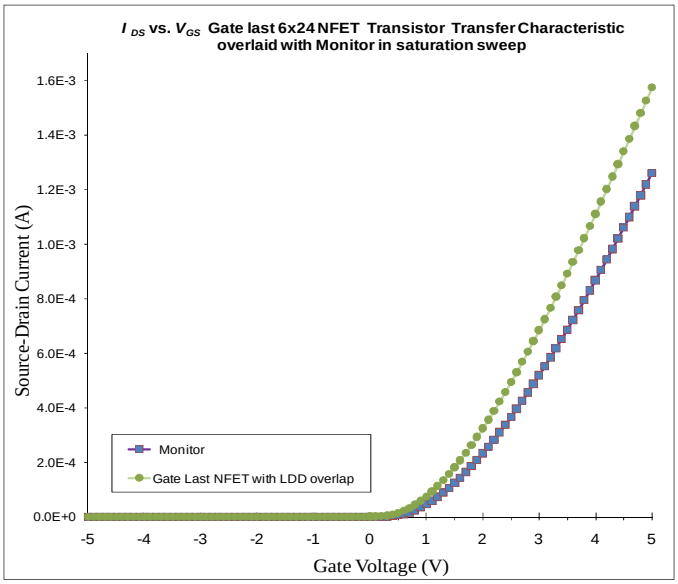
5.4.2 *NON-SELF-ALIGNED NFET (DUMMY GATE UNDERCUT, BROAD MAIN GATE LAST)*

The gate last with dummy gate undercut and broad main gate was designed such that the LDD implants were totally overlapped by the main gate. Due to the LDD the depletion region broadens and hence band-to-band tunneling in this region is suppressed compared to the NFET monitor. This results in a modest reduction in GIDL, as well as an increase in drive current due to an effective decrease in channel length (see Figure 5.7). However this improvement in GIDL is not as significant as that demonstrated by the narrow gate version for reasons described in the previous section. Figure 5.8(a) shows the saturation-mode transfer characteristics over the designed overlay offsets; note that certain devices with relatively high leakage exhibited little dependence on gate bias. Figure 5.8(b) shows the GIDL current level at V_G = -4 V, with a trend line fit based on

the observed systematic increase in GIDL associated with the designed offset decreasing from +1.0 to +0.6 µm (gate increasing LDD overlap).

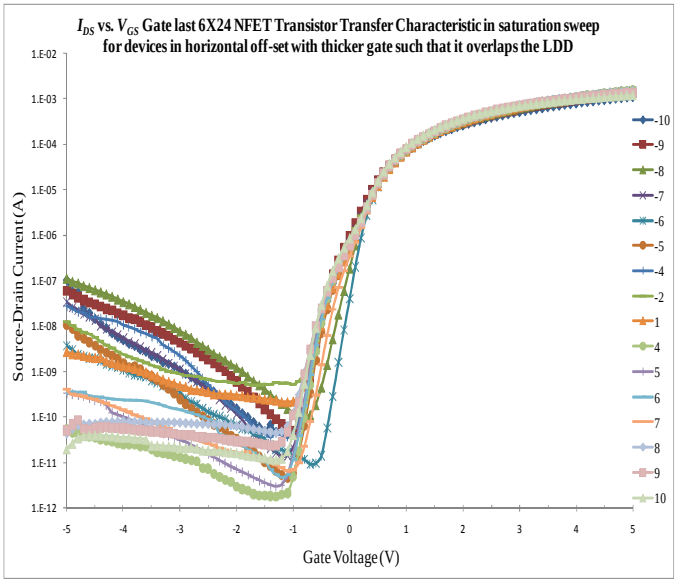


(a)

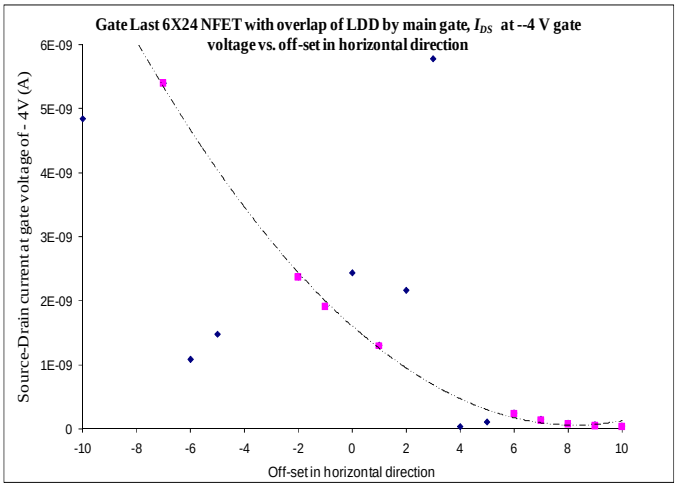


(b)

Figure 5.7: Overlay of I_D-V_G transfer characteristic for non-self-aligned NFET *(dummy-gate undercut, broad main-gate last)* with monitor in saturation mode sweep (a) log scale (b) linear scale. V_{DS} was set to a magnitude of 5 V for the NFET, with plot (a) showing a slight improvement in GIDL behavior over monitor.



(a)

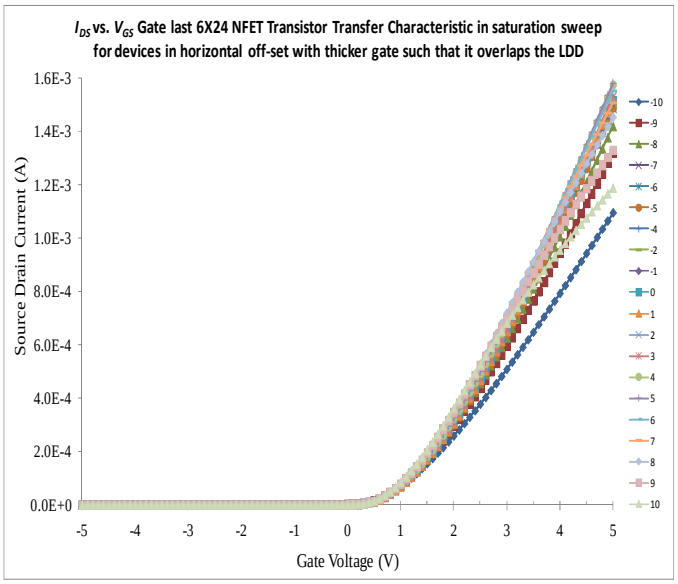


(b)

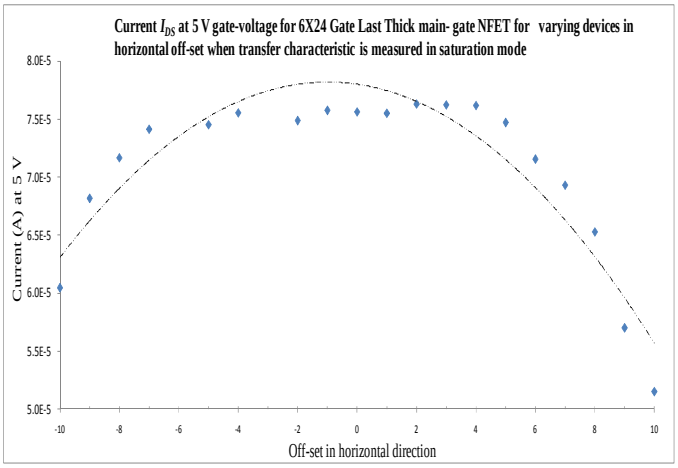
Figure 5.8: Saturation-mode transfer characteristics for various designed offsets (a), with the value of GIDL current measured at V_G = -4 V plotted versus the designed offset (b).

Regarding the current drive, this NFET variety shows a very interesting dependence on the designed offset of the structures. Figure 5.9 shows a parabolic relationship for drive current with respect to the designed offset, which can be explained

by the amount of series resistance associated with the LDD structures on both the source and drain regions. As the gate overlap shifts from an aligned position (offset ~ -0.1 µm) towards either the source or drain, the net decrease in LDD overlap increases the total series resistance and thus decreases current drive.



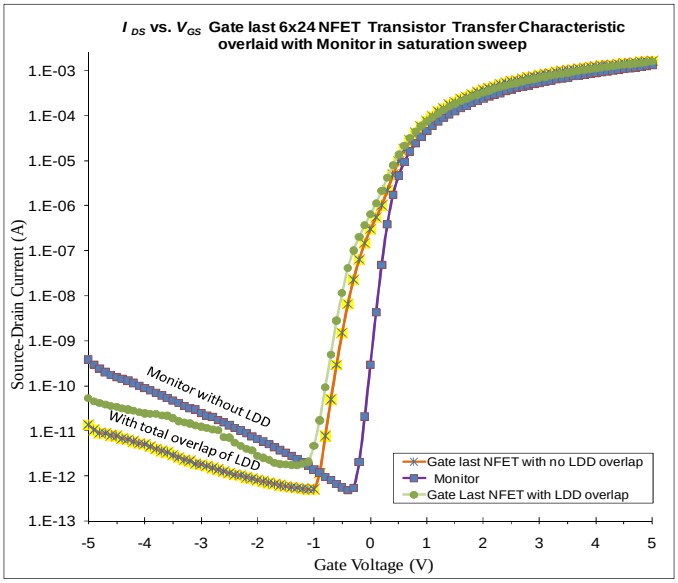
(a)



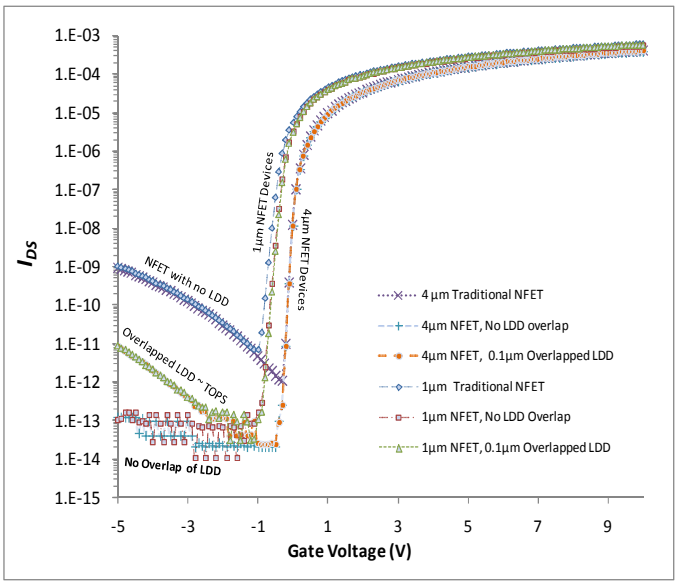
(b)

Figure 5.9: Saturation-mode transfer characteristics for various designed offsets in linear scale (a), with the value of current drive measured at V_G = 5 V plotted versus the designed offset (b).

To reiterate the off-state performance of the gate-last NFET devices, both the narrow and broad gate variations exhibited improvement in GIDL characteristic as anticipated from the simulation results shown in Figure 5.10. The monitor performance in Figure 5.10(a) is analogous to a traditional NFET; the broad main gate-last NFET with total overlap of LDD is equivalent to TOPS and the narrow main gate last NFET corresponds NFET with no overlap of LDD [5]. In terms of device off-state performance the narrow main gate last NFET with no overlap off LDD exhibited considerable improvement in GIDL behavior; the broad main gate last NFET with total overlap of LDD also exhibited improvement over the monitor, but not as significant. While both LDD devices demonstrate interface trapping effects in the subthreshold region, this may be attributed to the process deviations discussed Section 4.6.



(a)



(b)

Figure 5.10: I_D-V_G transfer characteristics for non-self-aligned NFETs overlaid with monitor in saturation mode sweep. (a) electrical characteristics of devices fabricated at RIT in the SMFL. (b) device characteristics simulated using Silvaco Atlas.

5.4.3 NON-*SELF-ALIGNED S/D, LDD LAST NFET*

It was expected that the NFET strategy with S/D first and LDD last, self-aligned to the main gate (option discussed in Section 4.3.3) would also yield significant improvement in GIDL current, since it is guaranteed to result in a non-overlapped LDD version. Unfortunately due to process issues, wafers with this variation were not successfully completed. Problems which occurred during the process deviations, discussed in Section 4.4, on these particular samples were not recoverable.

5.4.4 *LDD FIRST, SELF-ALIGNED S/D NFET*

The S/D last with main gate such that it totally overlapped the LDDs (placed first) yielded off-state characteristics that were not in agreement with simulation. This device

would be expected to behave similar to the TOPS-like device described in Section 5.4.2, although there is a different dependence on process alignment. The GIDL observed on this variation was as high as that observed on the monitor device sample (high-GIDL device chosen for comparison), shown in Figure 5.11. This result suggests that the actual process alignment on the gate pattern definition was not within the tolerance needed to provide a protective overlap of the LDD region prior to S/D implant. Another possible reason may be the gate RIE process bias causing the gate to pull away from the LDD edge. Either of these scenarios could result in a disappearance of the LDD structure, thus resulting in a similar level of GIDL as a monitor device without an LDD.

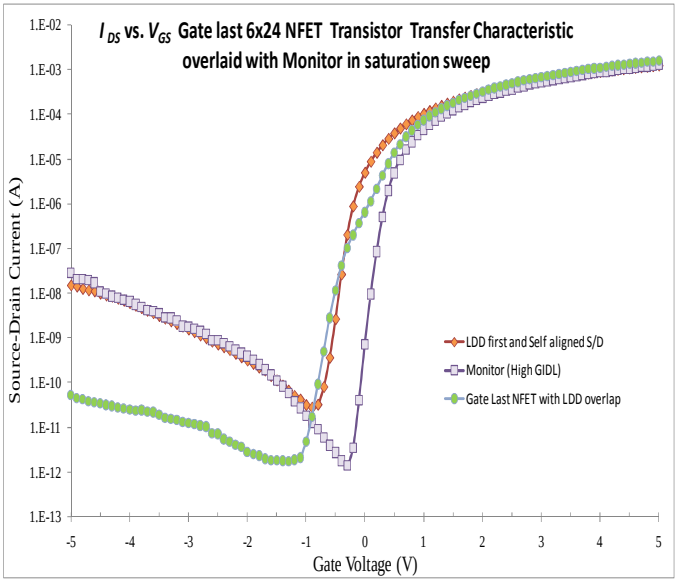


Figure 5.11: Overlay of I_D-V_G transfer characteristic for self-aligned S/D NFETs (LDD first), along with monitor and gate-last NFET in saturation mode sweep. The monitor chosen for comparison exhibited a similar level of GIDL as the treatment device. The gate-last device with total LDD overlap is also shown for comparison.

While the I-V characteristic on this treatment demonstrates a left-shift compared to the monitor device, there is no pronounced distortion as that observed on the gate-last NFET variations. This suggests that the distortion in the subthreshold regions on the gate-last NFET devices may be associated with some attribute of the LDD structure processed under low temperature constraints (T = 600°C).

5.5 CHARACTERIZING THE PFET BARRIER/ SURFACE HALO INFLUENCE ON GIDL AND DIBL

There were four varieties of PFET devices designed. Variations included the different barrier structures, design of the S/D regions and gate electrode, and the fabrication sequence. All combinations yielded devices for characterization, with differences and trends observed between treatments. While comparisons in the off-state behavior of the PFET treatments in this study were reasonable, the on-state current drive of all PFET device treatments was notably inferior to the control devices. The lack of on-state performance may be attributed to the device structure design in some cases. However certain noted inconsistencies in electrical behavior suggest some influence of the process deviations described in Section 4.4. This section will show representative data collected for the different variations, and provide a discussion on the interpretation of electrical test results along with comparisons to the control devices.

5.5.1 *ASYMMETRIC NON-SELF-ALIGNED SURFACE HALO, SELF-ALIGNED S/D PFET*

The asymmetric PFET was designed to use the NFET LDD structure (phosphorus implant) as a barrier at the source end of the device without influencing the drain region. These devices have exhibited certain improvements in the off-state device transfer characteristic for short channel length devices. To form the asymmetric PFET, the surface halo implant was aligned to the dummy gate such that the dummy gate covered the drain region, as discussed in Section 4.3.2; the S/D implant was then aligned to the main gate. Figure 5.16 shows this PFET device in comparison to the non-implanted control devices.

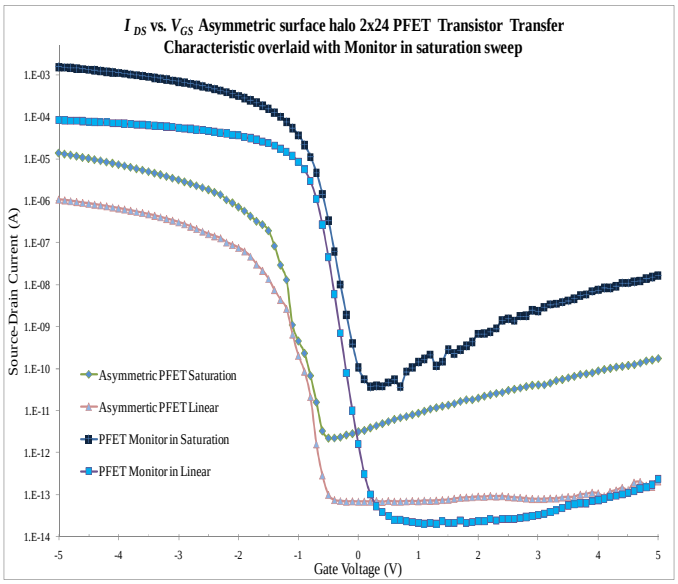
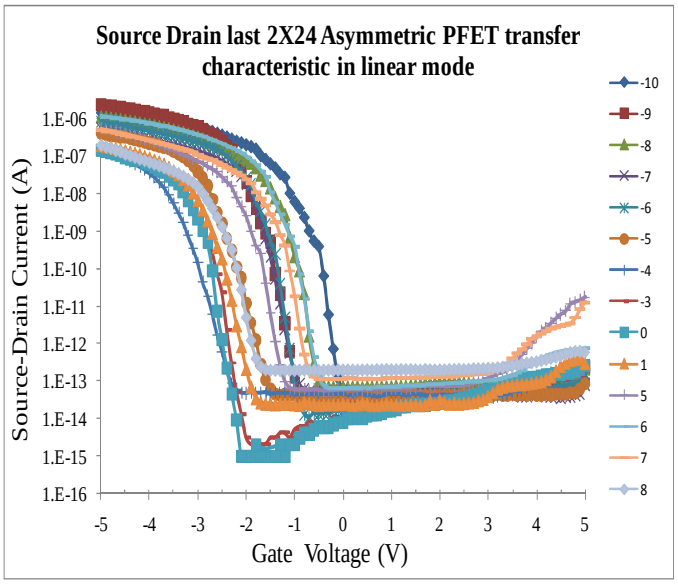


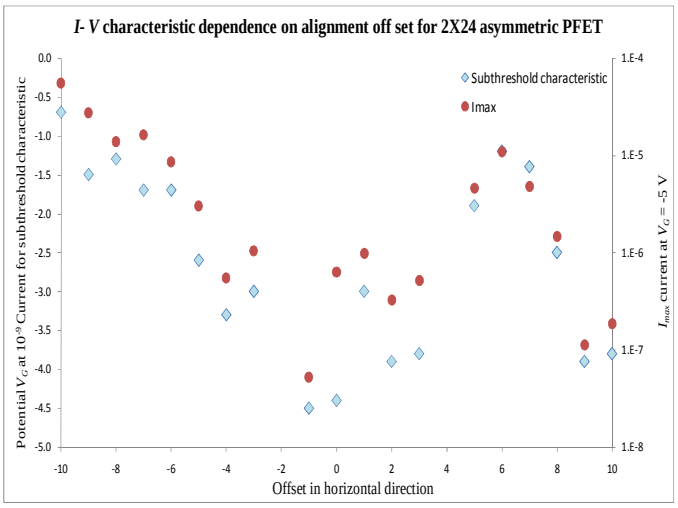
Figure 5.12: The I_D-V_G transfer characteristics for an asymmetric PFET (L = 2 µm) at low and high drain bias (-0.1 V and -5 V, respectively) compared to a control device.

The addition of the surface halo implant provides an n-type barrier at the source and appears to suppress DIBL, however there is a significant compromise in current

drive. Simulated asymmetric PFET characteristics were discussed in Section 3.3; a barrier region of 0.1 µm length demonstrated a negligible degradation of current drive on an L = 4 µm device, and minor degradation (~ 20%) of current drive on an L=1 µm device. The fine overlay offset increments (0.1 µm) provided in the mask design should have provided barrier regions of varying length. Figure 5.17 shows asymmetric PFET device characteristics over an entire grouping of designed overlay offsets. The significant reduction in current drive even under the best case conditions suggests that either the overlay error did not enable a "short enough" barrier region, or that the phosphorus implant and annealing processes that were used failed to produce said region.



(a)



(b)

Figure 5.13: (a) Transfer characteristics for various designed offsets producing barrier regions of varying length. (b) the value of gate voltage (V_G) measured at I_{DS} = 10^9 A/μm (y1 axis) and the saturation Imax (y2 axis) plotted versus the designed offset.

The transfer characteristics show a wide spread of data with large variations in both threshold voltage and current drive. Figure 5.17(b) shows two quantified responses from the transfer characteristics plotted against the designed alignment offset. The value of gate voltage that corresponds to a subthreshold current level of 10^{-9}A/μm was used to assess a characteristic shift. The maximum current drive was used to assess the effective channel resistance. These parameters track closely over the designed alignment offset values; however there does not appear to be a systematic trend in the data shown. While this result is quite unexpected, the correlation between the lateral shift (related to V_T) and the I_{max} clearly demonstrate the two-dimensional influence of the barrier implant on the device operation. The "longer" barrier should be associated with a higher V_T, and a lower I_{max} related to both the increase in channel resistance due to less hole carriers in the

channel (more phosphorus ions), and a longer effective channel length associated with the barrier region.

5.5.2 *SYMMETRIC NON-SELF-ALIGNED SURFACE HALO, SELF-ALIGNED S/D PFET*

The asymmetric PFET provides an n-type barrier only at the source end of the device where it is intended to reduce DIBL. However, in general this type of device arrangement is difficult to integrate into a standard TFT fabrication process without an additional lithography step and/or process complexity. A symmetric PFET structure was also investigated which could be easily integrated into a CMOS process, simultaneously formed along with the NFET LDD structures. In this PFET strategy the dummy gate did not extend over the drain region during the surface halo implant, thus forming an n-type barrier at both the source and drain regions which was totally overlapped by the main gate, as discussed in Section 4.3.1. The characteristics of this device are shown in Figure 5.18, in comparison to the asymmetric PFET results.

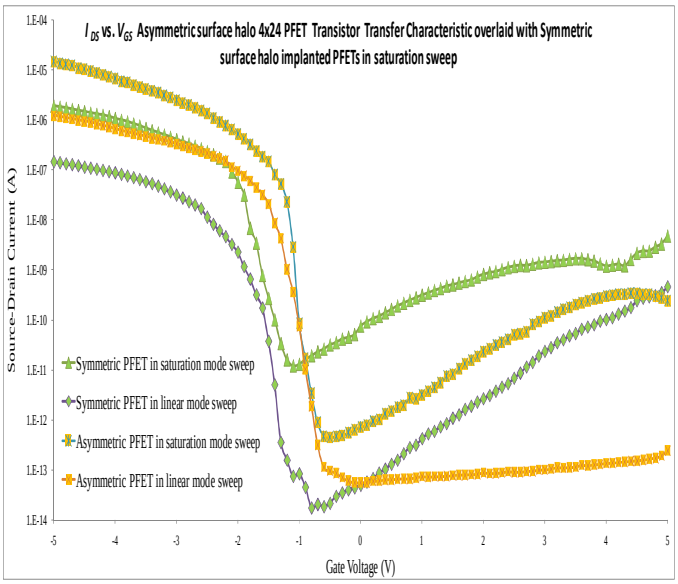


Figure 5.14: Overlay of the I_D-V_G transfer characteristics for the PFET (L = 4 µm) at low and high drain bias (-0.1 V and -5 V, respectively) for the symmetric and asymmetric PFET with surface halo implant.

The plot suggests that the DIBL behavior for the symmetric PFET structure is worse than that of the asymmetric device (which is almost negligible down to L = 2 µm, shown in Figure 5.16), however it appears to be dominated by a high I_{min} and GIDL. This surface halo at the drain end presents a center for band-to-band tunneling, which enhances the GIDL level significantly. The drive current is lower in comparison to the asymmetric PFET, which can be explained using the same arguments in comparing the asymmetric PFET device to the control device; the added barrier further reduces channel inversion charge and adds to the effective channel length of the device.

5.5.3 *NON- SELF-ALIGNED S/D PFET WITH GATE LAST AND NO SURFACE HALO IMPLANT (GATE UNDERLAP)*

In this strategy the S/D implants were aligned to the dummy gate and there was no surface halo implant. The main gate was designed to either provide S/D overlap, when considering a center-aligned broad gate, or S/D underlap (gap formation), when considering a center-aligned narrow gate. This strategy was designed to have "native" LDD structures formed by the lightly doped background p-type silicon regions, resulting in either single-sided (offset broad gate) or double-sided (narrow gate) LDD PFETs. Representative characteristics for both variations are shown in Figure 5.19.

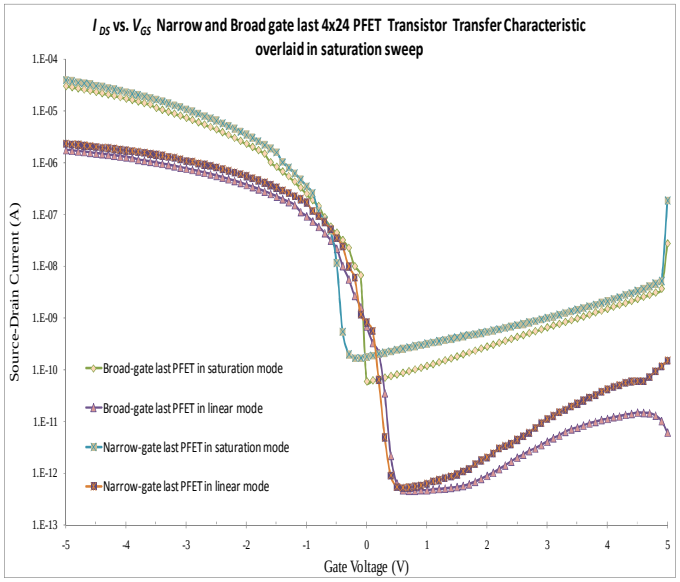


Figure 5.15: The I_D-V_G transfer characteristics for single-sided and double-sided LDD PFETs at low and high drain bias (-0.1 V and -5 V, respectively).

Neither of the "native LDD" PFET structures demonstrated performance results as expected. The current drive of these devices was degraded significantly from the self-aligned control device, which can be only partially explained by the added series

resistance of the LDD (channel/drain gap) region. The center-aligned broad gate PFET should have provided gate overlap to the S/D regions, and thus the same current as the control device; this was not the case. Part of the performance degradation may be due to the process deviations discussed in Section 4.4. The characteristics in Figure 5.19 also show a significant amount of GIDL, even in the linear mode (low drain bias) transfer characteristic. While there may be a genuine issue with the gate underlapped native LDD PFET, the obtained results on these particular treatments are not easily interpreted. An improved self-aligned version of the double-sided native LDD PFET could have been implemented by performing a main gate undercut following the p+ S/D implant; this variation was not investigated in this study.

5.6 CONCLUDING REMARKS

The narrow and broad main-gate-last NFET demonstrated improvement in GIDL, consistent with the simulation results and published reference material [5]. The narrow main-gate-last NFET with no LDD overlap exhibited the most pronounced improvement in GIDL, whereas results from the broad main-gate-last NFET with total overlap of LDD suggests a decreased benefit in the LDD structure. While the S/D last NFET strategy produced a similar total-overlap LDD structure, there were no observed benefits by implementing this device variation. These results offer guidance on engineering the NFET LDD structures and the details of CMOS process integration.

The interpretation of results from the investigation on enhancing the PFET off-state performance through variations in the structure design was not as well established as in the case of the NFET devices. The asymmetric PFETs with the surface halo implant

exhibited DIBL suppression in the device transfer characteristic for short channel length devices; however the current drive was markedly reduced compared to the control device. This suggests that while the phosphorus implant provides a source barrier to hole carriers, it causes a decrease in channel charge and increases the effective channel length of the device in the on-state. This appeared even more pronounced on the symmetric PFETs, with barrier structures adjacent to both the source and drain ends of the device. These results suggest that the implant used to form this barrier did not provide a region of required length (~ 0.1 µm), regardless of the designed overlay offset. While the gate-underlapped LDD PFETs were expected to yield improvements in GIDL with only a minor compromise in current drive due to added series resistance, the results exhibited a significant degradation of current drive (comparable to the surface halo implanted devices) and elevated GIDL. Further study on this strategy is required.

CHAPTER 6

SUMMARY AND CONCLUSIONS

This study on the use of phosphorus implants for off-state improvement of SOI CMOS fabricated at low temperature encountered several challenges, primarily with fabrication issues which may have compromised electrical performance, making interpretation of electrical characteristics quite difficult. A considerable engineering effort was invested in order to realize functional transistors for several different NFET and PFET variations. While there were some results that were difficult to explain, most electrical characteristics demonstrated behavior and trends that were consistent with expectations. This chapter will summarize the various sections, revisiting and reinforcing the points of primary importance.

6.1 EXPERIMENTAL DESIGN

The formation of implanted features, including NFET LDDs and PFET source barrier enhancement, can be implemented using several process integration strategies. This focus of this study was to investigate a single implant that would serve both of these purposes, thus suppressing both NFET GIDL and PFET DIBL behavior while minimizing the compromise on the on-state current drive. An established low temperature CMOS TFT process [6] was used to fabricate the devices on SIMOX SOI,

with modifications in the mask layout and process sequence to realize the device features of interest. Constraints on the silicon layer thickness and the gate oxide thickness ensured consistency with limitations imposed by Silicon-on-Glass (SiOG) manufacture and flat panel display industry TFT manufacturing capabilities, both of which were primary considerations in the motivation of this study.

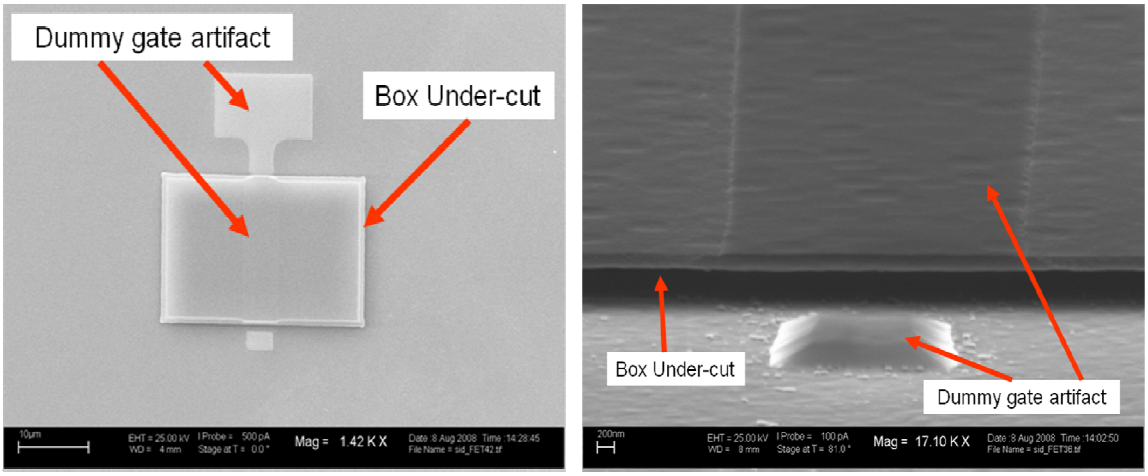
In order to avoid complex process integration schemes, non-self-aligned implant strategies were considered. Mask design features and five process flow variations were incorporated in this study, which yielded four varieties of NFET and PFETs. All the strategies were based on double-level gate layers; a dummy gate and main gate were used at different levels in the process flow to accomplish the desired structures. The dummy gate placement was arrayed with a range from -1 to +1 µm and an incremental shift of 0.1 µm to provide a spread of alignment offsets as well as account for actual overlay error. Implanted features that were aligned to the dummy gate structure would then mirror the offset to the main gate, actual results being dependent on the lithography overlay error.

6.2. FABRICATION AND PROCESS DEVIATIONS

Because of the five process flow variations, the challenge of avoiding process errors was not trivial, and in fact was not completely successful as discussed in Chapter 4. Great care was given to ensure the best possible overlay results, with thorough process record keeping and documentation of measured results for future reference. This was extremely challenging, considering that results may be influenced by

a high level of random (uncontrolled) variation, or systematic variation such as rotational error that creates inconsistent results over the wafer surface. Lithography rework was required when overlay error exceeded approximately 0.5 µm, giving additional opportunities for process mishaps. Regarding pattern definition, most of the critical levels were processed within the target tolerance. However certain observations during processing (dummy gate removal) were misleading, and led to process deviations that potentially influenced the electrical characteristics of devices.

SIMOX SOI substrates were chosen to provide the highest quality crystalline silicon, thus avoiding any confounding with imperfections in the semiconductor material. In the formation of the buried oxide during the SIMOX manufacturing process the wafers are subjected to extremely high temperature, which leads to an abrupt well defined interface between silicon and SiO_2. There seems to be no reported issues of suboxide (SiO_X) formation in commercial SIMOX material. However, a suboxide layer did appear to form beneath the molybdenum dummy gate structures used for implant masking. The suboxide layer is shown in Figure 6.1, labeled as a dummy gate artifact.



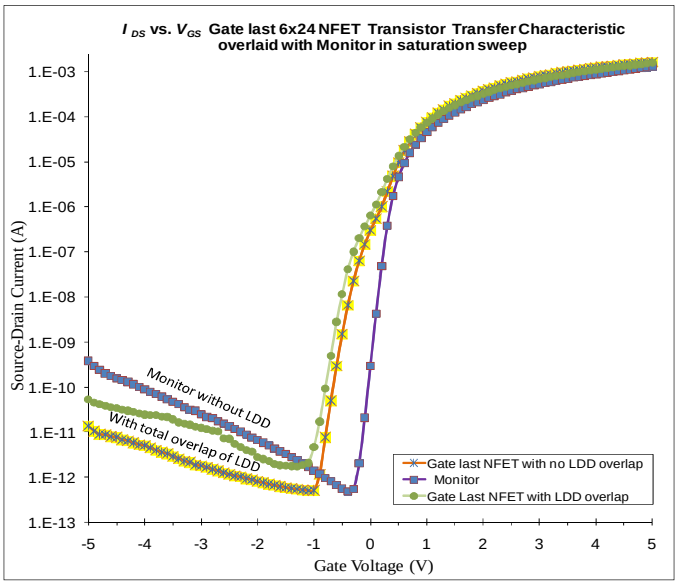
(a) (b)

Figure 6.1: Replicate of Figure 4.10 from Chapter 4. (a) SEM image exhibiting an artifact after dummy gate etch that exactly follows the original molybdenum pattern. (b) Dummy gate artifact is seen to appear directly on the silicon where the buried oxide has been removed.

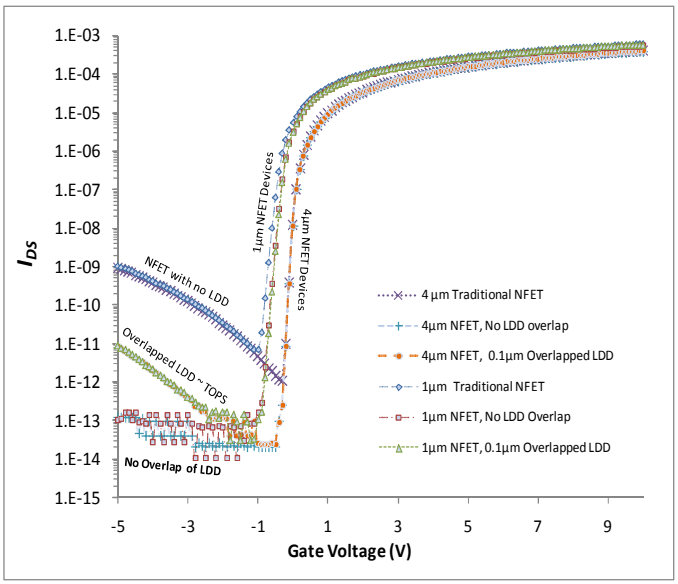
While this buried suboxide would have probably had no influence on device operation, these regions appeared to be residual molybdenum from a top-down interpretation using an optical microscope. The additional etching used in the attempt to remove this layer caused a significant undercut of the mesa, and appears to have induced surface roughness, both of which are seen in Figure 6.1. The process deviations and resulting effects on the device structure raised a significant concern regarding the ability to achieve working devices with characteristics that would isolate the influence of the factors under investigation. In spite of such difficulties the fabrication was completed, and electrical characterization demonstrated that most of the devices were operational. However, the interpretation on the electrical results is subject to a potential influence from these process-induced changes.

6.3. PROCESS AND DEVICE SIMULATION

Device simulation using Silvaco® Atlas™ simulation software was used to predict the influence of the off-state enhancement features on the electrical performance. Careful trade-offs were considered to avoid a significant compromise in the on-state current drive. The LDD/surface halo implant conditions were chosen based on these simulations, and the mask design allowed variation on dimensional parameters (length and overlap) that could not be controlled within the desired tolerance. Representative simulations that were instrumental in device design and comparisons to measured electrical characteristics are shown in Figures 6.2 and 6.3.



(a)



(b)

Figure 6.2: Replicate of Figure 5.10 from Chapter 5. Overlay of I_D-V_G transfer characteristics for non-self-aligned LDD NFETs with control device in saturation mode. (a) Electrical characteristics of devices fabricated at RIT in the SMFL. (b) Device characteristics simulated using Silvaco Atlas.

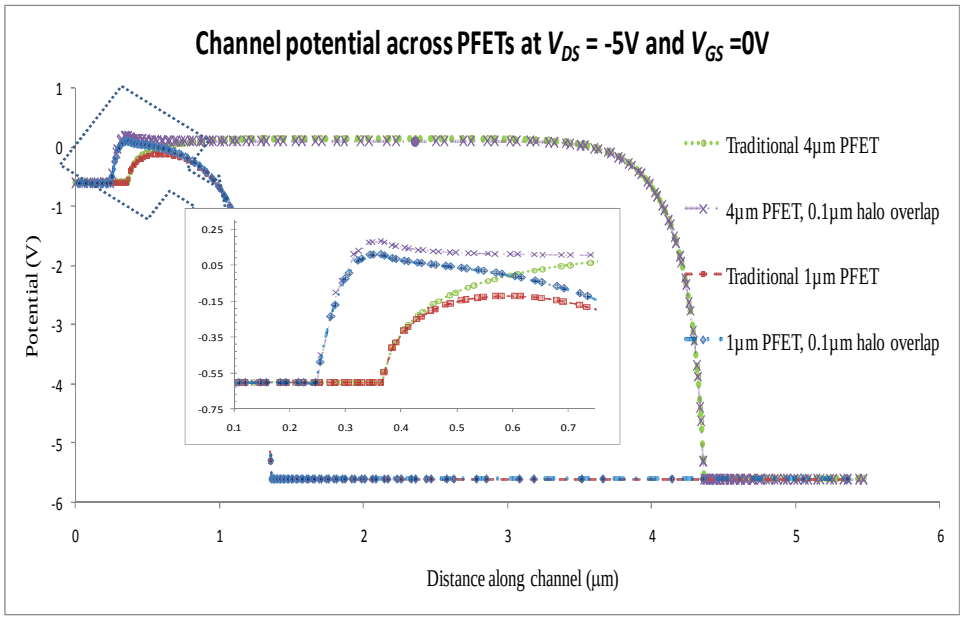


Figure 6.3: Enhanced version of Figure 3.6 from Chapter 3. Simulated channel potential across PFETs for V_{DS} = -5 V and V_{GS} = 0 V, (L_{eff} = 1 µm and 4 µm). The inset shows a zoom-in of the source barrier lowering on device structures with and without the surface halo implant, with a notable difference on the 1 µm device.

6.4. ELECTRICAL CHARACTERIZATION

Devices chosen for electrical characterization from the gate alignment offset array were identified using lithography overlay results documented during fabrication. Device performance of the control devices was presented first to establish the comparison benchmark. This was followed by the investigation on the various LDD NFET structures implemented for GIDL suppression. Finally the investigation on the various PFET structures implemented for both DIBL and GIDL suppression was presented.

The narrow and broad main-gate-last NFET demonstrated improvement in GIDL, consistent with the simulation results and published reference material [5] (see Figure 6.2). The narrow main-gate-last NFET with no LDD overlap exhibited the most pronounced improvement in GIDL, whereas results from the broad main-gate-last NFET with total overlap of LDD suggests a decreased benefit in the LDD structure. While the S/D-last NFET strategy produced a similar total-overlap LDD structure, there were no observed benefits by implementing this device variation. These results offer guidance on engineering the NFET LDD structures and the details of CMOS process integration.

The interpretation of results from the investigation on enhancing the PFET off-state performance through variations in the structure design was not as well established as in the case of the NFET devices. The asymmetric PFETs with the surface halo implant exhibited DIBL suppression in the device transfer characteristic for short channel length devices; however the current drive was markedly reduced compared to the control device (see Figure 6.4). This suggested that while the phosphorus implant provided a source barrier to hole carriers, it causes a decrease in channel charge and increases the effective

channel length of the device in the on-state. These results suggest that the implant used to form this barrier did not provide a region of required length (~ 0.1 µm), regardless of the designed overlay offset. Characterization on other PFET variations provided no additional insight on suppression of DIBL and GIDL.

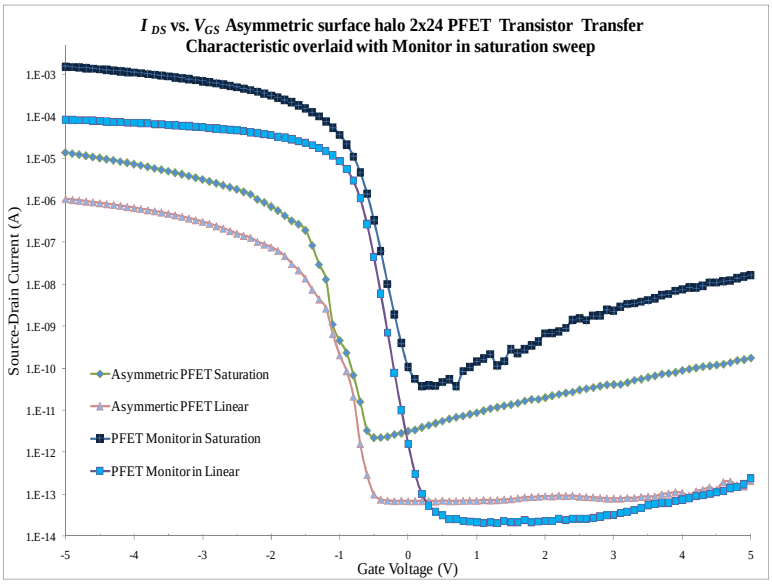


Figure 6.4: Replicate of Figure 5.16 from Chapter 5. The I_D-V_G transfer characteristics for an asymmetric PFET (L = 2 µm) at low and high drain bias (-0.1 V and -5 V, respectively) compared to a control device.

6.4 SUMMARY AND FUTURE WORK

While the investigation on off-state performance enhancement demonstrated certain characteristics that correlated with simulated device behavior, the characteristics shown in Figures 6.3 and 6.4 also indicated the presence of silicon/SiO_2 interface traps. Both the NFET and PFET devices characterized in this study were plagued with subthreshold distortion, whereas the control devices demonstrated little influence from

interface traps (see Figure 5.2). This may be due to some influence from the LDD regions, however the observations shown in Figure 6.1 may be partly responsible. Unfortunately it was not possible to separate the influence of these potential factors.

Since the focus of this study was off-state performance, perhaps less attention should have been paid to compromise in the NFET on-state current drive. While the LDD strategy worked well for the NFETs, the phosphorus implant dose was too high for the PFET source barrier and decreased the on-state drive markedly. Further study should decouple the NFET and PFET implants, allowing them to be optimized separately for each application.

There are other process integration details that should be revisited. Changing the process strategy to have more self-aligned variations would relax some of the challenges associated with lithography overlay. This would involve additional process development work for device features such as sidewall spacers that are typically used in CMOS fabrication. While there was significant motivation to maintain simplicity, some increase in process complexity for such an investigation is justified.

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APPENDIX

A-1 Traditional NMOS (without enhancement) - Thesis simulation Code

```
# NMOS Thesis simulation Code Traditional
#Siddhartha Singh
#Microelectronic Engineering Graduate Student, RIT
#################################################################################
go atlas

# Set Variables ----------------------------------------------------

set Xsi  = 0.20
set Xox  = 0.0500
set L    = 4.0
set XLDD = 0.0
set Qtop = 0
set Qbot= 0
set Nsub = 1E15
set NLDD = 1e17
set filename = Tradional_NFET_4um

## Mesh ------------------------------------------------------------

mesh  space.mult=1.0
x.mesh loc=0.00    spac=2
x.mesh loc=4       spac=1
x.mesh loc=7       spac=0.5
x.mesh loc=8       spac=0.02
x.mesh loc=8+$L/2  spac=0.1
x.mesh loc=8+$L    spac=0.02
x.mesh loc=9+$L    spac=0.5
x.mesh loc=12+$L   spac=1
x.mesh loc=16+$L   spac=2
#
y.mesh loc=-1*$Xox    spac=$Xox/10
y.mesh loc=-.001      spac=$Xox/10
y.mesh loc=0          spac=0.001
y.mesh loc=0.005      spac=0.001
y.mesh loc=$Xsi/2     spac=0.010
y.mesh loc=$xsi-0.004 spac=0.001
y.mesh loc=$Xsi       spac=0.001
y.mesh loc=$Xsi+0.01  spac=0.05
y.mesh loc=$Xsi+0.1   spac=.05

## Regions ---------------------------------------------------------
```

```
region      num=1 y.max=0    oxide
region      num=2 y.min=0    y.max=$Xsi silicon
region      num=3 y.min=$Xsi  oxide

## Electrodes -----------------------------------------------------

# #1-GATE #2-SOURCE #3-DRAIN #4-SUBSTRATE(below oxide)
electrode   name=gate    x.min=8 x.max=8+$L y.min=$Xox*(-1) y.max=$Xox*(-1)
electrode   name=source  x.max=4 y.min=0 y.max=0
electrode   name=drain   x.min=12+$L y.min=0 y.max=0
contact     name=gate workfunction=4.53

## Doping ---------------------------------------------------------

doping      uniform conc=$Nsub n.type  reg=2
doping      gauss n.type conc=1e20 char=0.2 lat.char=0.00 reg=2 x.r=8-$XLDD
doping      gauss n.type conc=1e20 char=0.2 lat.char=0.00 reg=2 x.l=8+$L+$XLDD
# LDD
#Source Side
doping    uniform n.type conc=$NLDD x.left=8-$XLDD x.right=8 y.top=0
y.bottom=$Xsi
doping    uniform n.type conc=$NLDD x.left=8+$L    x.right=8+$L+$XLDD
y.bottom=$Xsi

## Interface -----------------------------------------------------

interf    qf=$Qtop    y.max=0.05
interf    qf=$Qbot    y.min=0.05

## Models ---------------------------------------------------------

#models auger srh shi fldmob bgn fermi print temperature=300
#method gummel newton carriers=2
## GIDL Model
models srh conmob fldmob b.electrons=2 b.holes=1 evsatmod=0 hvsatmod=0 \
fermi bgn print numcar=2 temperature=300 \
impact \
bbt.std bb.a=8.5e16 bb.gamma=2.0 bb.b=7.5e6
##
method newton trap carriers=1 electron

## IDVG Sweep ----------------------------------------------------t
#
output     ex.field ey.field flowlines con.band val.band qfn photogen impact
solve init
```

```
solve vdrain=.1
log outf=Lin_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
solve name=gate vgate=-5 vfinal=10 vstep=.1
extract name="lin_vt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) -
abs(ave(v."drain"))/2.0)
extract name="lin_ss" 1/slope(maxslope(curve((v."gate"),log10(abs(i."drain")))))*1000
extract name="IDVG" curve(v."gate",i."drain"*-1) outf="pIDVG.dat"
log off
struct outfile=Lin_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot Lin_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
solve init
solve name= drain vdrain =0.1 vfinal=5 vstep =0.1
log outf=A_Sat_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
solve name=gate vgate=-5 vfinal=10 vstep=0.1
extract name="sat_vt" xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")^(1/2))))
extract name="sat_ss" 1/slope(maxslope(curve((v."gate"),log10(abs(i."drain")))))*1000
#Other
extract name="DIBL"(($"lin_vt" - $"sat_vt")*1000)/(5.0-0.1)
extract name="idsmax" max(abs(i."drain"))
log off
struct outfile=Sat_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot A_Sat_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
#
solve init
solve vdrain = +0.1
solve name=gate vgate=-.1 vfinal=0 vstep=0.1
struct outfile=Off_1_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot Off_1_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
solve init
solve vdrain = +5
solve name=gate vgate=4.9 vfinal=5 vstep=0.1
struct outfile=Off_2_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot Off_2_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
quit
```

A-2 NMOS with LDD enhancement - Thesis simulation Code

```
# NMOS with LDD enhancement  - Thesis simulation Code
#Siddhartha Singh
#Microelectronic Engineering Graduate Student, RIT
#################################################################################

go atlas

## Set Variables ----------------------------------------------------

set Xsi  = 0.20
set Xox  = 0.0500
set L    = 1.0
set XLDD = 0.1
set Qtop = 0
set Qbot= 0
set Nsub = 1E15
set NLDD = 1e17
set filename = Overlapped_LDD_NFET_1um/ Non_Overlapped_LDD_NFET_1um

## Mesh ------------------------------------------------------------

mesh  space.mult=1.0

x.mesh loc=0.00    spac=2
x.mesh loc=4       spac=1
x.mesh loc=7       spac=0.5
x.mesh loc=8       spac=0.02
x.mesh loc=8+$L/2  spac=0.1
x.mesh loc=8+$L    spac=0.02
x.mesh loc=9+$L    spac=0.5
x.mesh loc=12+$L   spac=1
x.mesh loc=16+$L   spac=2
#
y.mesh loc=-1*$Xox    spac=$Xox/10
y.mesh loc=-.001      spac=$Xox/10
y.mesh loc=0          spac=0.001
y.mesh loc=0.005      spac=0.001
y.mesh loc=$Xsi/2     spac=0.010
y.mesh loc=$xsi-0.004 spac=0.001
y.mesh loc=$Xsi       spac=0.001
y.mesh loc=$Xsi+0.01  spac=0.05
y.mesh loc=$Xsi+0.1   spac=.05
```

```
## Regions -----------------------------------------------------

region      num=1 y.max=0    oxide
region      num=2 y.min=0    y.max=$Xsi silicon
region      num=3 y.min=$Xsi  oxide

## Electrodes -------------------------------------------------

# #1-GATE #2-SOURCE #3-DRAIN #4-SUBSTRATE(below oxide)
electrode   name=gate    x.min=8-$XLDD x.max=8+$L+$XLDD y.min=$Xox*(-1)
y.max=$Xox*(-1)
electrode   name=source  x.max=4 y.min=0 y.max=0
electrode   name=drain   x.min=12+$L y.min=0 y.max=0
contact     name=gate workfunction=4.53

## Doping -----------------------------------------------------

doping      uniform conc=$Nsub n.type  reg=2
doping      gauss n.type conc=1e20 char=0.2 lat.char=0.00 reg=2 x.r=8-$XLDD
doping      gauss n.type conc=1e20 char=0.2 lat.char=0.00 reg=2 x.l=8+$L+$XLDD

# LDD
#Source Side
doping    uniform n.type conc=$NLDD x.left=8-$XLDD x.right=8 y.top=0
y.bottom=$Xsi
doping    uniform n.type conc=$NLDD x.left=8+$L    x.right=8+$L+$XLDD
y.bottom=$Xsi

## Interface -------------------------------------------------

interf    qf=$Qtop    y.max=0.05
interf    qf=$Qbot    y.min=0.05

## Models -----------------------------------------------------
#models auger srh shi fldmob bgn fermi print temperature=300
#method gummel newton carriers=2

## GIDL Model
models srh conmob fldmob b.electrons=2 b.holes=1 evsatmod=0 hvsatmod=0 \
fermi bgn print numcar=2 temperature=300 \
impact \
bbt.std bb.a=8.5e16 bb.gamma=2.0 bb.b=7.5e6
##
```

```
method newton trap carriers=1 electron
## IDVG Sweep ----------------------------------------------------t
#
output     ex.field ey.field flowlines con.band val.band qfn photogen impact
solve init

solve vdrain=.1
log outf=Lin_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
solve name=gate vgate=-5 vfinal=10 vstep=.1
extract name="lin_vt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) -
abs(ave(v."drain"))/2.0)
extract name="lin_ss" 1/slope(maxslope(curve((v."gate"),log10(abs(i."drain")))))*1000
extract name="IDVG" curve(v."gate",i."drain"*-1) outf="pIDVG.dat"

#extract name="vt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
#        - abs(ave(v."drain"))/2.0)
log off
struct outfile=Lin_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
#tonyplot Lin_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot Lin_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
solve init
solve name= drain vdrain =0.1 vfinal=5 vstep =0.1
#solve vdrain=5
log outf=A_Sat_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
solve name=gate vgate=-5 vfinal=10 vstep=0.1
extract name="sat_vt" xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")^(1/2))))
extract name="sat_ss" 1/slope(maxslope(curve((v."gate"),log10(abs(i."drain")))))*1000
extract name="DIBL"(($"lin_vt" - $"sat_vt")*1000)/(5.0-0.1)
extract name="idsmax" max(abs(i."drain"))
log off
struct outfile=Sat_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot A_Sat_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
solve init
solve vdrain = +0.1
struct outfile=Off_1_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot Off_1_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
solve init
solve vdrain = +5
struct outfile=Off_2_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot Off_2_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
quit
```

A-3 Traditional PMOS (without enhancement) - Thesis Simulation Code

```
#Traditional PMOS (without enhancement) - Thesis Simulation
#Siddhartha Singh
#Microelectronic Engineering Graduate Student, RIT
##############################################################################

go atlas

## Set Variables ------------------------------------------------

set Xsi  = 0.20
set Xox  = 0.0500
set L    = 4.0
set XLDD = 0.0
set Qtop = 0
set Qbot= 0
set Nsub = 1E15
set NLDD = 1e17
set filename =Tradional_4um_PFET

## Mesh ---------------------------------------------------------

mesh  space.mult=1.0
x.mesh loc=0.00    spac=2
x.mesh loc=4       spac=1
x.mesh loc=7       spac=.2
x.mesh loc=8       spac=0.02
x.mesh loc=8+$L/2  spac=0.2
x.mesh loc=8+$L    spac=0.02
x.mesh loc=9+$L    spac=0.1
x.mesh loc=12+$L   spac=1
x.mesh loc=16+$L   spac=2
#
y.mesh loc=-1*$Xox    spac=$Xox/10
y.mesh loc=-.001      spac=$Xox/10
y.mesh loc=0          spac=0.001
y.mesh loc=0.005      spac=0.001
y.mesh loc=$Xsi/2     spac=0.010
y.mesh loc=$xsi-0.004 spac=0.001
y.mesh loc=$Xsi       spac=0.001
y.mesh loc=$Xsi+0.01  spac=0.05
y.mesh loc=$Xsi+0.1   spac=.05

## Regions ------------------------------------------------------
```

```
region      num=1 y.max=0    oxide
region      num=2 y.min=0    y.max=$Xsi silicon
region      num=3 y.min=$Xsi  oxide

## Electrodes -----------------------------------------------------

# #1-GATE #2-SOURCE #3-DRAIN #4-SUBSTRATE(below oxide)
#electrode   name=gate    x.min=8-$XLDD x.max=8+$L+$XLDD y.min=$Xox*(-1)
y.max=$Xox*(-1)
electrode   name=gate    x.min=8 x.max=8+$L y.min=$Xox*(-1) y.max=$Xox*(-1)
electrode   name=source  x.max=4 y.min=0 y.max=0
electrode   name=drain   x.min=12+$L y.min=0 y.max=0

contact     name=gate workfunction=4.53

## Doping ---------------------------------------------------------

doping      uniform conc=$Nsub p.type  reg=2
doping      gauss p.type conc=1e20 char=0.2 lat.char=0.00 reg=2 x.r=8-$XLDD
doping      gauss p.type conc=1e20 char=0.2 lat.char=0.00 reg=2 x.l=8+$L

# LDD
#Source Side
doping    uniform n.type conc=$NLDD x.left=8-$XLDD x.right=8 y.top=0
y.bottom=$Xsi
#doping    uniform n.type conc=$NLDD x.left=8+$L    x.right=8+$L+$XLDD
#y.bottom=$Xsi

## Interface -----------------------------------------------------

interf    qf=$Qtop    y.max=0.05
interf    qf=$Qbot    y.min=0.05

## Models ---------------------------------------------------------

models auger srh shi fldmob bgn fermi print temperature=300
method gummel newton carriers=2

#tonyplot
## IDVG Sweep ----------------------------------------------------t
#
output     ex.field ey.field flowlines con.band val.band qfn photogen impact
solve init
```

```
solve vdrain=-.1
log outf=Lin_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
solve name=gate vgate=5 vfinal=-10 vstep=-.1
extract name="lin_vt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) -
abs(ave(v."drain"))/2.0)
extract name="lin_ss" 1/slope(maxslope(curve((v."gate"),log10(abs(i."drain")))))*1000
extract name="IDVG" curve(v."gate",i."drain"*-1) outf="pIDVG.dat"
log off
struct outfile=Lin_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot Lin_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
solve init
solve vdrain=-5
log outf=Sat_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
solve name=gate vgate=5 vfinal=-10 vstep=-0.1
extract name="sat_vt" xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")^(1/2))))
extract name="sat_ss" 1/slope(maxslope(curve((v."gate"),log10(abs(i."drain")))))*1000
#Other
extract name="DIBL"(($"lin_vt" - $"sat_vt")*1000)/(5.0-0.1)
extract name="idsmax" max(abs(i."drain"))
#
struct outfile=Sat_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot Sat_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
solve init
solve vdrain = -0.1
solve name=gate vgate=-.1 vfinal=0 vstep=0.1
struct outfile=Off_1_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot Off_1_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
solve init
solve vdrain = -5
solve name=gate vgate=-.1 vfinal=0 vstep=0.1
struct outfile=Off_2_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot Off_2_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
quit
```

A-4 Asymmetric PMOS (With N-Barrier) - Thesis Simulation Code

```
#Asymmetric PMOS (With N-Barrier) - Thesis Simulation Code
#Siddhartha Singh
#Microelectronic Engineering Graduate Student, RIT
#########################################################################

go atlas

## Set Variables ----------------------------------------------------
set Xsi  = 0.20
set Xox  = 0.0500
set L    = 1.0
set XLDD = 0.1
set Qtop = 0
set Qbot= 0
set Nsub = 1E15
set NLDD = 1e17
set filename = Asymmetric_1um_0.1um_Overlapped_PFET

## Mesh -------------------------------------------------------------
mesh  space.mult=1.0
x.mesh loc=0.00    spac=2
x.mesh loc=4       spac=1
x.mesh loc=7       spac=.1
x.mesh loc=8       spac=0.02
x.mesh loc=8+$L/2  spac=0.02
x.mesh loc=8+$L    spac=0.02
x.mesh loc=9+$L    spac=0.1
x.mesh loc=12+$L   spac=1
x.mesh loc=16+$L   spac=2
#
y.mesh loc=-1*$Xox    spac=$Xox/10
y.mesh loc=-.001      spac=$Xox/10
y.mesh loc=0          spac=0.001
y.mesh loc=0.005      spac=0.001
y.mesh loc=$Xsi/2     spac=0.010
y.mesh loc=$xsi-0.004 spac=0.001
y.mesh loc=$Xsi       spac=0.001
y.mesh loc=$Xsi+0.01  spac=0.05
y.mesh loc=$Xsi+0.1   spac=.05

## Regions ----------------------------------------------------------
region      num=1 y.max=0    oxide
region      num=2 y.min=0    y.max=$Xsi silicon
```

```
region      num=3 y.min=$Xsi  oxide

## Electrodes -----------------------------------------------------
# #1-GATE #2-SOURCE #3-DRAIN #4-SUBSTRATE(below oxide)
electrode   name=gate    x.min=8-$XLDD x.max=8+$L+$XLDD y.min=$Xox*(-1)
y.max=$Xox*(-1)
electrode   name=source  x.max=4 y.min=0 y.max=0
electrode   name=drain   x.min=12+$L y.min=0 y.max=0
contact     name=gate workfunction=4.53

## Doping ---------------------------------------------------------

doping      uniform conc=$Nsub p.type  reg=2
doping      gauss p.type conc=1e20 char=0.2 lat.char=0.00 reg=2 x.r=8-$XLDD
doping      gauss p.type conc=1e20 char=0.2 lat.char=0.00 reg=2 x.l=8+$L

# LDD
#Source Side
doping    uniform n.type conc=$NLDD x.left=8-$XLDD x.right=8 y.top=0
y.bottom=$Xsi

## Interface ------------------------------------------------------

interf    qf=$Qtop    y.max=0.05
interf    qf=$Qbot    y.min=0.05

## Models ---------------------------------------------------------

models auger srh shi fldmob bgn fermi print temperature=300
method gummel newton carriers=2

## IDVG Sweep ----------------------------------------------------t
#
output     ex.field ey.field flowlines con.band val.band qfn photogen impact
solve init
solve vdrain=-.1
log outf=Lin_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
solve name=gate vgate=5 vfinal=-10 vstep=-.1
extract name="lin_vt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) -
abs(ave(v."drain"))/2.0)
extract name="lin_ss" 1/slope(maxslope(curve((v."gate"),log10(abs(i."drain")))))*1000
extract name="IDVG" curve(v."gate",i."drain"*-1) outf="pIDVG.dat"
log off
struct outfile=Lin_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot Lin_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
solve init
```

```
#
solve vdrain=-5
log outf=Sat_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
solve name=gate vgate=5 vfinal=-10 vstep=-0.1
extract name="sat_vt" xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")^(1/2))))
extract name="sat_ss" 1/slope(maxslope(curve((v."gate"),log10(abs(i."drain")))))*1000
#Other
extract name="DIBL"(($"lin_vt" - $"sat_vt")*1000)/(5.0-0.1)
extract name="idsmax" max(abs(i."drain"))
#
log off
struct outfile=Sat_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot Sat_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".log
#
solve init
solve vdrain = -0.1
solve name=gate vgate=-.1 vfinal=0 vstep=0.1
struct outfile=Off_1_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot Off_1_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
solve init
solve vdrain = -5
solve name=gate vgate=-4.9 vfinal=-5 vstep=-0.1
struct outfile=Off_2_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
tonyplot Off_2_$"filename"_NLDD-$"NLDD"_XLDD-$"XLDD"_L$"L".str
quit
```