2013

Circuit solutions to compensate for device degradation in analog design in scaled technologies

Mark Pude

CIRCUIT SOLUTIONS TO COMPENSATE FOR DEVICE DEGRADATION IN ANALOG DESIGN IN SCALED TECHNOLOGIES

by

MARK PUDE

A DISSERTATION

Submitted in partial fulfillment of the requirements
For the degree of Doctor of Philosophy
in
Microsystems Engineering
at the
Rochester Institute of Technology

June 2013

Author: _____
Microsystems Engineering Program

Certified by: _____
P.R. Mukund, Ph.D.
Professor of Electrical Engineering

Approved by: _____
Bruce W. Smith, Ph.D.
Director of Microsystems Engineering Program

Certified by: _____
Harvey J. Palmer, Ph.D.
Dean, Kate Gleason College of Engineering

Circuit Solutions to Compensate for Device Degradation in Analog Design in Scaled Technologies

by

Mark Pude

Submitted by Mark Pude in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Microsystems Engineering and accepted on behalf of the Rochester Institute of Technology by the dissertation committee.

We, the undersigned members of the Faculty of the Rochester Institute of Technology, certify that we have advised and/or supervised the candidate on the work described in this dissertation. We further certify that we have reviewed the dissertation manuscript and approve it in partial fulfillment of the requirements of the degree of Doctor of Philosophy in Microsystems Engineering.

Approved by:

Dr. P.R. Mukund _____
(Committee Chair and Dissertation Advisor) Date

Dr. David Borkholder _____
Date

Dr. Robert Bowman _____
Date

Dr. James Moon _____
Date

Dr. Sean Rommel _____
Date

MICROSYSTEMS ENGINEERING PROGRAM
ROCHESTER INSTITUTE OF TECHNOLOGY
June 2013

ABSTRACT

Kate Gleason College of Engineering
Rochester Institute of Technology

Degree Doctor of Philosophy **Program** Microsystems Engineering
Name of Candidate Mark Pude
Title Circuit Solutions to Compensate for Device Degradation in Analog Design in Scaled Technologies

The continued aggressive scaling of semiconductor devices has had detrimental effects on the performance of those devices as used in analog circuitry. Specifically, the maximum intrinsic gain (MIG) of the devices continues to degrade as the device channel lengths are reduced below 100 nm and beyond. MIG is shown to degrade from 21.6 dB in a 180 nm technology to 12.2 dB in a 65 nm technology despite the application of traditional design techniques including device size scaling and bias voltage increases. This reduction in MIG along with other process scaling effects significantly complicates the design of linear amplifiers in these technologies.

This work proposes the use of positive feedback to compensate for MIG degradation in linear amplifier design in scaled technologies. Criteria for stable and process tolerant design are derived and examined in the context of amplifier models of varying degrees of complexity. This analysis defines an all-encompassing positive feedback design methodology for use in linear amplifier design of low-gain high-frequency amplifier design. Additionally, the effects of positive feedback are compared and contrasted to the effects of the commonly studied negative feedback design methodology. Finally, the methodology is applied to a differential amplifier stage in TSMC's 65 nm process using standard threshold voltage, thin oxide CMOS devices. These amplifiers were fabricated and tested to validate the positive feedback design methodology. Simulation shows that 98.4% of positive feedback amplifiers have improved gain over the baseline differential amplifier with an average improvement in gain of 10.3 dB. Silicon measurements of the amplifier gain show improvements of 17.1 dB on average. Similar to the application of negative feedback, gain improvement is achieved at the cost of frequency response. The gain-bandwidth product of the amplifier is reduced by an average of 18.4 GHz from 44.6 GHz. The circuitry required to implement this technique represent a meager 6% increase in silicon area from 460 μm^2 to 488 μm^2.

Abstract Approval: Committee Chair _____

Program Director _____

Dean KGCOE _____

For Avery Grace
and other future Elmers

ACKNOWLEDGEMENTS

This has been an interesting journey for me to say the least. First and foremost, I would like to thank my beautiful wife, Leslie. Your love and support, especially over the past 6 months, is the only reason I have been able to succeed in this endeavor. You're a wonderful and strong woman, and I am a lucky guy to have you in my life. I would also like to thank my daughter, Avery Grace. You are only one year old and have no way of knowing, but you manage to make me smile when I need it the most.

I would also like to thank the rest of my family, especially my mother and father. You have stood by me through the twists and turns of this process and have supported my decisions along the way. Also thank you for the grocery money early on, I would not have lasted long without it. Thank you to my siblings Diana, Krista, Dante, Jeff, Suzanne, Leith, and Tim. Thank you to my nieces and nephew, Kelly, Erin, Bret, and Keira. Thank you to the grandparents, Mere and Pere; Mammy; and Mena and Grampy. Finally, thank you to my in-laws, Tom and Dale. I will do my best to make sure I don't do silly things that will force you to tell me "your Ph.D. is showing." To all of you: thank you for your love, support, understanding, and belief in me over the years.

Thank you to Eric Bohannon and Chris Urban. I could not have picked two better guys to share in the challenges we all faced during this process. I would have lost interest years ago if it weren't for watching you two lap me by finishing your degrees. I wish you guys the best in your professional and personal lives. Please keep in touch.

Thank you to my colleagues at Intrinsix Corp. and Synaptics Inc. for your support, flexibility, and understanding while I finished this work. Thank you to Eric Bohannon,

Peng Chansakulporn, Imre Knausz, Primit Modi, Brian Mott, Eric Moule, Murat Ozbas, Chris Ludden, Jeff Lillie, Marshall Bell, Mujo Kozak, and Gene Petilli for your valuable technical discussions on this work and beyond. I hope we can continue to learn from each other for years to come. I would like to give a special thanks to Jeff Waldrop and Tom Quattrini for your help with last minute die micrographs included in this work.

Thank you to LSI, Jeff Burleson, Prashant Singh, Ken Paradis, Steve Howard, and Chris Macchietto for your support with and contributions to my research. Your input was invaluable and this research was improved by all of your ideas and suggestions. I would like to specially thank Ken Paradis for your support in the lab while taking silicon data. Specifically, thank you for watching over me and preventing me from ruining many thousands of dollars worth of equipment while collecting my silicon data.

Finally, thank you to my committee, Dr. Borkholder, Dr. Bowman, Dr. Moon, and Dr. Rommel, and RIT for providing me with the opportunity to perform this research. Thank you to Dr. Smith and my advisor, Dr. Mukund, for providing me the support and opportunities I needed to cross the finish line.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF COMMONLY USED SYMBOLS AND ABBREVIATIONS

μ ..... Average
σ ..... Standard deviation
ADE ..... Analog Design Environment
ASIC ..... Application specific integrated circuit
BSIM ..... Berkeley Short-channel IGFET Model
CC ..... Current conveyor
CML ..... Current mode logic
CMOS ..... Complementary metal oxide semiconductor
CMRR ..... Common-mode rejection ratio
DUT ..... Device under test
ESD ..... Electrostatic discharge
GBP ..... Gain bandwidth product
GBP_r ..... Gain bandwidth product ratio
GM ..... Gain margin
g_m ..... MOSFET transconductance
I/O ..... Input / Output
IC ..... Integrated Circuit
LG ..... Loop gain
LHP ..... Left half plane
LNA ..... Low noise amplifier
MATLAB ..... Matrix Laboratory
MIG ..... Maximum intrinsic gain
MOSFET ..... Metal oxide semiconductor field effect transistor
NFB ..... Negative Feedback
OCEAN ..... Open Command Environment for ANalysis
Opamp ..... Operational Amplifier
PFB ..... Positive feedback
PHY ..... Physical layer
PM ..... Phase margin
PVT ..... Process, voltage, and temperature
RHP ..... Right half plane
RMS ..... Root mean squared
r_o ..... MOSFET output resistance
S ..... Aspect ratio, W/L
SOC ..... System on chip
SPICE ..... Simulation Program with Integrated Circuit Emphasis
UGF ..... Unity gain frequency
VCVS ..... Voltage-controlled voltage source
V_{ds} ..... MOSFET drain to source voltage
V_{dssat} ..... MOSFET drain to source saturation voltage
V_{gs} ..... MOSFET gate to source voltage
V_T ..... MOSFET threshold voltage

CHAPTER 1
INTRODUCTION

Since the inception of the modern semiconductor industry, there has been an aggressive trend towards scaling the transistor smaller and smaller. In the past several decades, CMOS transistors have crossed the 100 nm threshold and continue towards the currently known limits of silicon technology as predicted by the International Technology Roadmap for Semiconductors [1] and shown in Figure 1.1. As the transistors become smaller, they can be packed more densely on a silicon die or wafer. This increased density leads to a transistor with higher switching speeds. Additionally, the smaller dimensions of the transistor mean that the voltage required to turn the transistor on and off is also smaller, leading to lower power consumption of the device. In digital circuit design, both of these traits are considered beneficial to a circuit's performance. While digital circuits and their performance have and will continue to drive technology trends in the semiconductor industry, the necessity for an interface to an analog world remains a

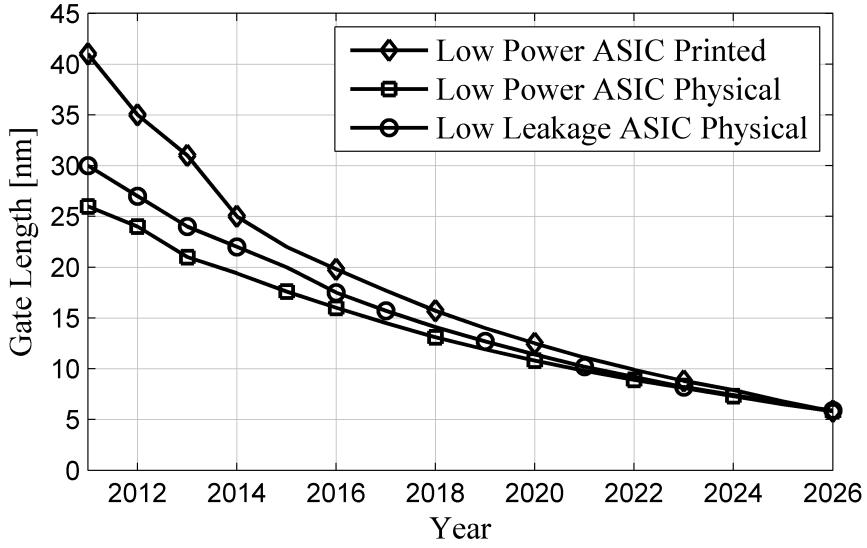

Figure 1.1 International Technology Roadmap for Semiconductors ASIC gate length predictions for technology scaling [1].

requirement in almost any conceivable application of electronics.

1.1 Analog Circuits in Scaled Technologies

The interfaces between the digital electronics and an analog world require analog circuits. These analog circuits are built from the same fundamental devices that the digital circuitry uses, NMOS and PMOS transistors. The operating principles of these analog circuits require more detailed information about the properties of the transistors beyond the on-off speeds and voltages. Even so, a recent cost-reducing push towards system-on-a-chip (SOC) designs in which both digital and analog components of a system co-exist on the same monolithic substrate has forced many analog designs into the same scaled technologies as the digital designs. With fundamentally different requirements and concerns, it should not be surprising that the effects of scaling have not been as beneficial to the analog circuits as it has to their digital counterparts.

While many device characteristics are altered in the process of scaling a technology, two of the most fundamental to analog design and analog circuits are device transconductance, g_m, and output resistance, r_o. As technologies are scaled into 90 nm, 65 nm technologies and beyond, the maximum intrinsic gain (MIG), the $g_m\, r_o$ product, is shown to degrade severely [2], [3], affecting even the most basic of analog circuit components. Generalized scaling theory coupled with the square-law equations that were relevant at the time (1972) does not predict this behavior [4]. As a result, in most traditional discussions of technology scaling, this MIG degradation problem is not adequately addressed.

1.2 Scaled Analog Design

Technology parameters are defined by process engineers during the development process. The resulting technology is used by analog design engineers and cannot be modified to serve specific purposes by that design engineer. Furthermore, in analog circuit design, the devices being used were optimized for other purposes: digital design, or chip input and output (I/O) interfaces. Therefore only circuit solutions may be applied to the problem. While analog design is currently performed in these scaled technologies using traditional design methodologies, they are almost always done using thicker oxide I/O devices. These thick oxide devices support a greater voltage across the MOSFET oxide, thus allowing for greater supply voltages.

However, in a mixed-mode SOC – one containing both digital and analog subsystems – the digital portions of the chip would likely be designed with the thin oxide devices. This allows for maximum performance and minimal power consumption of the digital subsystem. Thick oxide I/O devices are not directly compatible with these thin oxide devices and would require a separate power supply to operate them in an ideal voltage range. Creating multiple voltage domains on a chip creates complexities that continue to be carefully addressed in state of the art research [5] - [7]. Transferring signals between these voltage domains becomes more complicated and requires voltage level shifters which can often become performance-limiting components of a mixed-signal design. Multiple voltage domains also increase the chance of an electrostatic discharge (ESD) event damaging the chip [8], [9]. Having the ability to create working high-performance analog circuits in the same voltage domain as the digital subsystems would greatly reduce

this complexity. This reduced complexity allows for a more robust mixed-signal SOC by addressing the voltage level shifting and ESD concerns.

1.3 New Analog Design Solutions and This Work

This work proposes applying new circuit design techniques to address the MIG degradation problem in scaled technologies. The implementation of stable positive feedback (PFB) to existing amplifier topologies is proposed. This positive feedback increases the gain of the amplifier which would otherwise be limited by the MIG of individual transistors. Under traditional design methodologies, positive feedback causes systems to become unstable and is therefore not a viable solution. However, in scaled technologies the open-loop gain of an amplifier is inherently degraded by the process, allowing the use of positive feedback.

Chapter 2 discusses the background of technology scaling and the problems it imposes on analog design, including MIG degradation. This chapter also summarizes some current design techniques that are used to overcome these problems. Finally, as a basis for discussion regarding positive feedback, a summary of well-known negative feedback techniques and their consequences are discussed.

Chapter 3 introduces the technique of positive feedback circuits in order to compensate for device degradation. From generalized theory to circuit level implementations of positive feedback, this chapter presents mathematical analyses of positive feedback and its effects. Some of these effects must be taken into consideration for a robust positive feedback amplifier design. Good design techniques and tools for those designs are also

presented to allow a designer to maximize positive feedback amplifier performance and reliability.

Chapter 4 presents practical simulation and silicon results of the positive feedback technique presented in the previous chapter. The silicon results discussion also includes details on the test setup and data analysis required to interpret the data.

Finally, Chapter 5 discusses conclusions and recommendations regarding the work and how it can be used effectively in practical circuit design.

1.4 Software Tools Used in This Work

- Cadence Custom IC Design [10]
    - Virtuoso Schematic Editor – Used for the input and manipulation of transistor level schematics and test benches.
    - Virtuoso Analog Design Environment (ADE) – A graphical interface to the Spectre simulator engine.
    - Virtuoso Spectre Circuit Simulator – A SPICE-like circuit simulator for the Cadence Custom IC Design software suite
    - Virtuoso Layout Suite – Physical design tool set integrated with the schematic editor of Cadence Custom IC Design software.
    - SKILL Programming Language – Underlying interactive programming language of the Cadence Custom IC Design software.
    - OCEAN – Open Command Environment for ANalysis is a SKILL-based scripting language to interface with Spectre and other aspects of Cadence Custom IC Design.

- Mathworks MATLAB [11] – Matrix Laboratory is a high level mathematical computational software package used primarily for data analysis and figure generation in this work.

CHAPTER 2
BACKGROUND

This chapter discusses the issues with current scaling theory and new issues that are introduced at small device dimensions below 100 nm. New work is discussed to show MIG degradation across four technologies. This work presents MIG in the context of a design problem by mimicking the design process in terms of selecting a device size to obtain certain voltage characteristics. This is as opposed to the traditional device characterization process of using a fixed device size.

A brief overview of currently used design techniques is presented in order to give a sense of the current solutions being used to solve these small technology problems. As a preface to the positive feedback work, a review of negative feedback is presented. Starting from basic block diagram analysis through circuit analysis, the effects of negative feedback are illustrated mathematically for comparison in subsequent chapters.

2.1 Technology Scaling

Dennard, Gaensslen, Rideout, Bassous, and LeBlanc [4] were the first to suggest a generalized methodology for scaling fabrication processes. This technique involved scaling all of the device dimensions, voltages, and doping levels by a constant factor, κ. In doing this, the electric fields within the device remain constant. However, this leads to a very aggressive scaling of supply voltages that quickly become incompatible with threshold voltages and other device characteristics. As a result, this scaling methodology was soon replaced with generalized scaling.

Under this scaling technique, the physical dimensions and doping levels were also scaled by a factor, κ, while the electric field was scaled by a separate factor, α. This separation allowed the voltage to be scaled less aggressively (α/κ) than the device dimensions, providing better device performance by increasing the voltage headroom the devices could support. As long as the electric field experienced by the gate oxide does not exceed the breakdown voltage, this method of process scaling is acceptable.

Using square-law MOSFET theory, this basic scaling theory has been used to predict circuit performance parameters [12], [13] in newly scaled technologies. However, as technologies have been scaled into the deep submicron region a host of new problems occur which are not predicted by the original work by Dennard et al. [14] - [21]. Small channel effects have made it more difficult to predict the behavior of device parameters as technologies have decreased in size.

More recent work [2], [22], [24] has shown that predictions made by scaling theory and square-law device models do not follow the results seen in fabricated test structures. Some work has been performed in an attempt to explain this degradation [25], [26] and results in velocity overshoot as the primary reason for this deviation from long-channel predictions.

2.2 MIG Degradation

Understanding MIG degradation and what it means as a design concept is paramount to developing methodologies that compensate for it. In order to address this, a new MIG extraction methodology was devised to define the problem for this work. This MIG extraction methodology mimics the design process by using an algorithm to select device

sizes based on desired voltage characteristics. This is in contrast to typical device evaluation where devices of a specific size are characterized and their voltage characteristics are simply reported as a consequence.

Working directly with the physics-based device equations can be complicated and generally provides expressions that require computer-aided analysis to achieve meaningful results. Due to the unwieldy nature of the short channel model mathematics, the parameters of interest were extracted directly from circuit simulation using the Berkeley Short-channel IGFET Model (BSIM) [27] - [29].

2.2.1 Test Bench

BSIM is useful because it keeps track of small signal model parameters such as the transconductance, g_m, output resistance, r_o, saturation voltage, V_{DSsat}, and others. In order to extract these parameters over a wide range of scenarios, the test bench in Figure 2.1 was used. The purpose of this test bench is to mimic the design process, allowing the

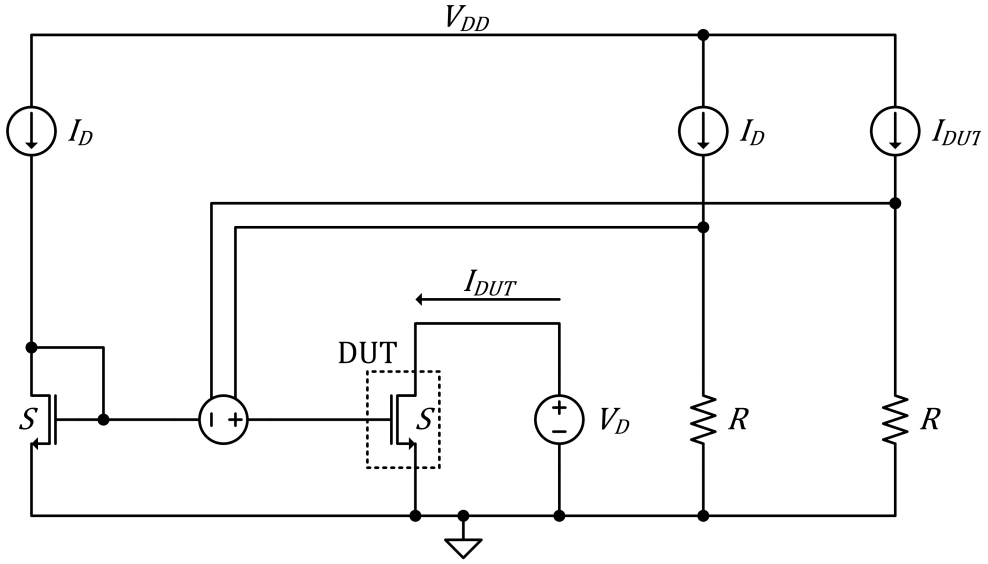

Figure 2.1 g_m and r_o extraction test bench. The servo loop drives the gate of DUT such that i_{DUT} is equal to a predefined I_D value.

designer to achieve a current, I_D, and voltage characteristics, V_{Gov} and V_{Dov}, by varying the aspect ratio, $S = W/L$, of the device.

The test bench is a control loop that is working to drive I_{DUT} to I_D by varying the gate voltage, V_G, of the device under test (DUT) through the voltage-controlled-voltage-source error amplifier. The diode-connected MOSFET has the same S as the DUT and exists as a zero-error offset to the error amplifier. While the test bench itself finds the gate voltage required to achieve $I_{DUT} = I_D$, the designer can vary S to achieve other voltage characteristics. Specifically, the voltage characteristics of interest are the gate voltage overdrive, V_{Gov}, and drain voltage overdrive, V_{Dov}.

V_{Gov} is defined as the gate voltage in excess of the threshold voltage, V_T, or $V_{Gov} = V_G - V_T$. V_T cannot be defined as a fixed value as the threshold voltage changes with transistor size as well as bias voltages [18]. Fortunately, BSIM keeps track of the end result of V_T and can be extracted from the model without calculation.

V_{Dov} is defined as the drain voltage in excess of the saturation voltage, V_{DSsat}, or $V_{Dov} = V_D - V_{DSsat}$. In long channel models, V_{DSsat} is simply equal to V_{Gov}, however including short channel effects; V_{DSsat} is more complicated [18].

$$V_{DSsat} = \frac{(V_G - V_T)E_{sat}L}{(V_G - V_T) + E_{sat}L} \tag{2.1}$$

where E_{sat} is the electric field at the point of velocity saturation in the MOSFET channel and L is the device gate length. The BSIM does not give information about E_{sat}. The model does, however, give V_{DSsat} directly, so V_{Dov} can be calculated easily.

In order to simplify the design process, the Spectre optimizer was used to play the role of designer by varying S and V_D to obtain the desired V_{Gov} and V_{Dov} for a given I_D. At this design point, the g_m and r_o (g_{ds}) of the device can be extracted directly from the DC operating point simulation results of BSIM.

This process was repeated over a wide range of device sizes and bias voltages. In order to automate the process, an OCEAN script was created to run each simulation and extract the pertinent information. The information, stored in a text file, could then be tabulated and compared across several technologies. An example of this OCEAN script and the optimization process is shown in Section A.1.

2.2.2 Simulation Results

Transconductance and output impedance data for four technologies was extracted over a wide variation of devices sizes and bias voltages. The largest technology has a 0.18 µm minimum feature size with a $V_{DD} = 1.8$ V supply voltage. Below this in feature size is the 0.11 µm technology with a $V_{DD} = 1.2$ V supply voltage. The two most modern technologies used were 90 nm and 65 nm technologies with supply voltages of $V_{DD} = 1$ V. It has commonly been stated that the largest concern in technology scaling is the scaling of the supply voltage. While this is generally cited in terms of reduced voltage headroom, the supply voltage reduction also severely affects the devices parameters g_m and r_o. By observing g_m and r_o trends across these technologies, it can be definitively shown that MIG degradation is indeed a problem.

Using the methodology described in the previous section to extract this data reflects typical design procedures. Because power consumption and, directly related to power, current draw is a large concern in design, the data was taken under two conditions:

1) Constant current, $I_D = 130$ µA remains constant across each technology

2) Constant power, $I_D V_{DD} = 130$ µW is kept constant across each technology.

This is to say, that the desired I_D in all devices in Case 1 is set to 130 µA, but in Case 2 they are set to 130 µA, 108 µA and 72 µA for the 1 V, 1.2 V and 1.8 V V_{DD} supply voltages, respectively. The absolute values of 130 µA and 130 µW are representative current values. These tests could be performed at other current values and the results would be similar because the test methodology will scale the device aspect ratio, S, to support the chosen drain current. The purpose of this comparison is to dispel concerns that devices perform better in the larger technologies simply because they are dissipating

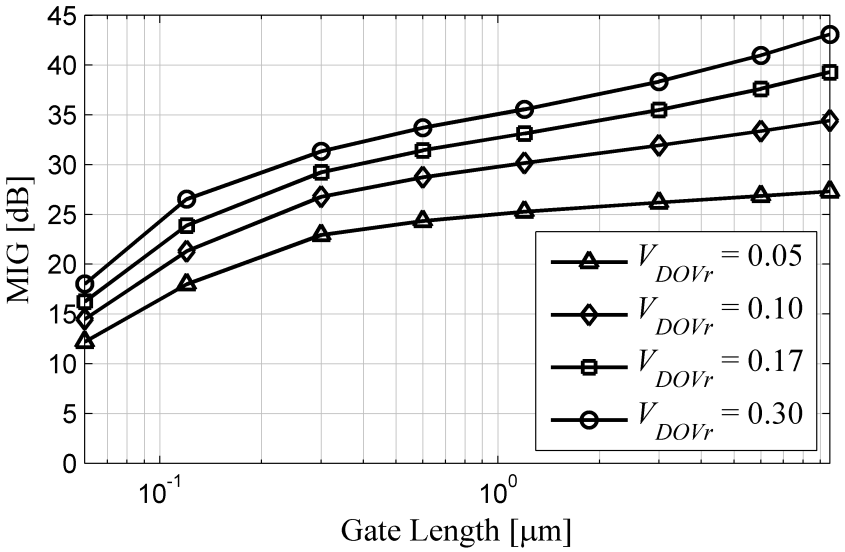

Figure 2.2 65 nm technology MIG versus gate length for various V_{DOVr} values with a fixed drain current of $I_D = 130$ µA.

more power. Furthermore, the simulations were performed at multiple V_{Dov} voltages. These voltages are selected as a fraction of V_{DD} such that technologies with more headroom available can use that headroom. This target value of V_{Dov} is described as a ratio $V_{DOVr} = V_{Dov}/V_{DD}$.

As an example, Figure 2.2 shows MIG simulation results for the 65 nm technology. The figure shows that at minimum gate length, the MIG is indeed quite small, on the order of 12 dB. Upon first inspection, a designer might attempt to increase the gate length in order to increase the output resistance, r_o, and thus increase the MIG; however, as Figure 2.2 shows, this technique approaches a point of diminishing returns at approximately $5 \cdot L_{min}$ to $10 \cdot L_{min}$ where L_{min} is the minimum gate length, $L_{min} = 60$ nm in the 65 nm technology. While increasing the drain overdrive voltage does improve the performance, even large values of V_{DOVr} show the plateau behavior at long gate lengths. This all but eliminates the typical practice of simply increasing gate length to improve device

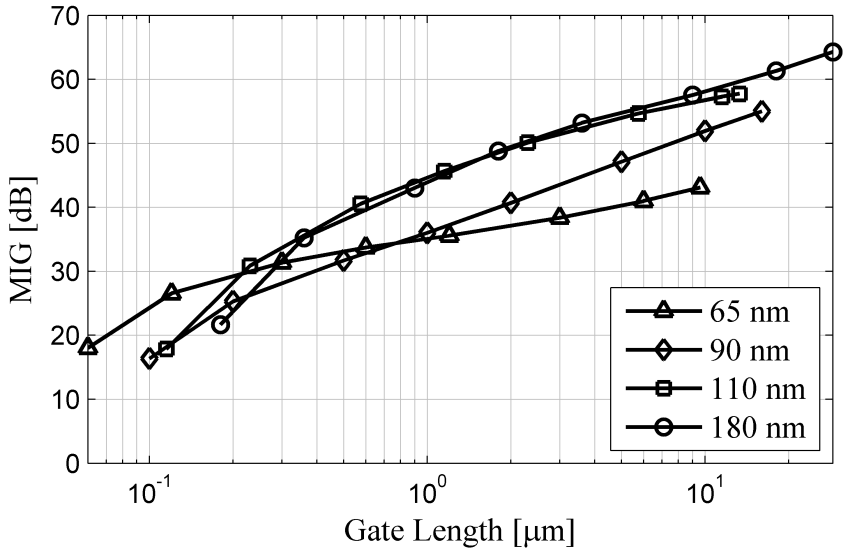

Figure 2.3 Maximum intrinsic gain versus gate length in 65 nm, 90 nm, 110 nm, and 180 nm technologies for constant drain current, $I_D = 130$ μA.

performance.

Figure 2.3 shows the scaling trends across all four of the technologies under consideration with $V_{DOVr} = 0.3$ and constant drain current, $I_D = 130$ µA. As is the case in the stand-alone 65 nm node data, each of the technologies approach a MIG plateau at a relatively small multiple of L_{min}. Additionally, this plateau decreases as the technology is scaled. At the maximum gate lengths that the technology will allow, the difference between the 180 nm and 65 nm nodes is approximately 21.2 dB, which corresponds to over an order of magnitude difference in MIG.

The data in Figure 2.2 shows four curves for varying drain overdrive voltages based on a percentage of V_{DD}. Because V_{DD} changes across the technologies, one could argue that the amount of power dissipated in the device channel is increasing with increased supply voltage and this is the reason for increased MIG. To show that this degradation remains a

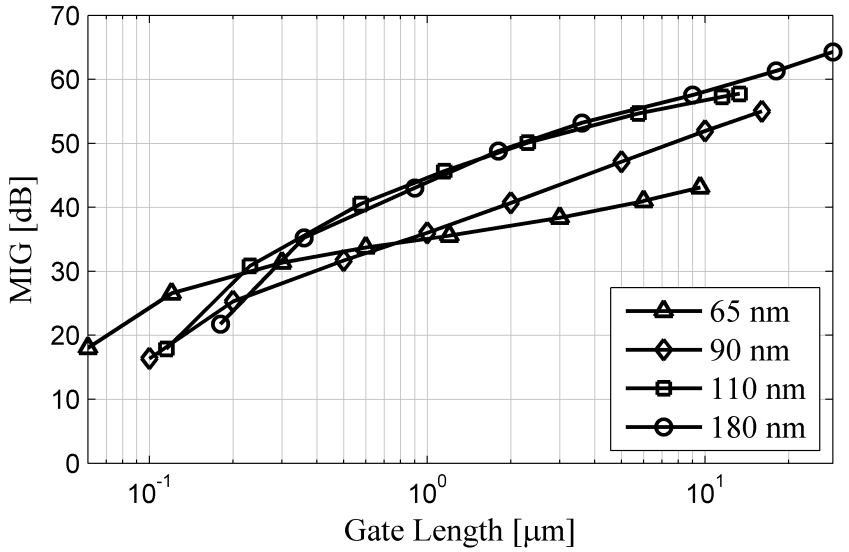

Figure 2.4 Maximum intrinsic gain versus gate length length in 65 nm, 90 nm, 110 nm, and 180 nm technologies for constant device power, $I_D V_{DD} = 130$ µW.

problem regardless of power dissipation, the g_m and r_o data was extracted across all of the technologies with a constant $I_D V_{DD}$ product equal to 130 µW. In the 65 and 90 nm technologies, I_D was set to 130 µA, and in the 1.2 V and 1.8 V technologies, I_D was set to 108 µA and 72 µA, respectively. The results of these simulations are shown in Figure 2.4.

Figure 2.3 and Figure 2.4 look almost identical and, in fact, the MIG values are within fractions of a decibel of each other. The reason for the similar data is the opposing behavior of g_m and r_o as a function of I_D. As I_D increases, g_m will increase but r_o will decrease. The resulting $g_m r_o$ product remains relatively constant. This fact also limits the design practice of increasing drain current in order to increase the MIG. While the transconductance of the device will increase, the output resistance will decrease.

Figure 2.5 shows the MIG for minimum gate length devices in each technology. It can be seen from this figure that there is a general degrading trend in the minimum sized

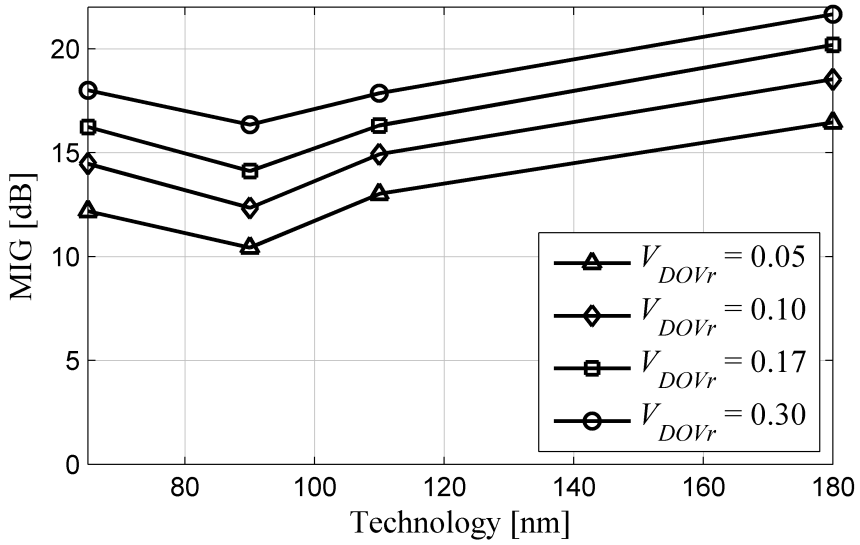

Figure 2.5 Maximum intrinsic gain for devices with $L = L_{min}$ in 65 nm, 90 nm, 110 nm, and 180 nm technologies with various V_{DOVr} values and constrant drain current $I_D = 130$ µA.

devices. One interesting anomaly to note in Figure 2.5 is the smaller MIG in the 90 nm node than the 65 nm for minimum gate lengths. This data confirms what is discussed in [4], [12] - [14], [16] in that supply voltage scaling is more detrimental to device performance than the process components themselves. Because there was no supply voltage scaling between the 65 nm and 90 nm technologies, the overall performance actually increases at the 65 nm node. For smaller technologies, 45 nm and beyond, any further reduction in supply voltage will likely show the same degradation depicted in the other scaling examples.

Figure 2.6 shows a set of devices, all with $L = 360$ nm, $S = 30$ and $I_D = 130$ uA with different values of V_{DOVr} applied as the drain overdrive voltage. This comparison shows that even with identical geometry and drain current there is still an overall degradation in performance at smaller technology nodes. This limitation in maximum intrinsic gain is

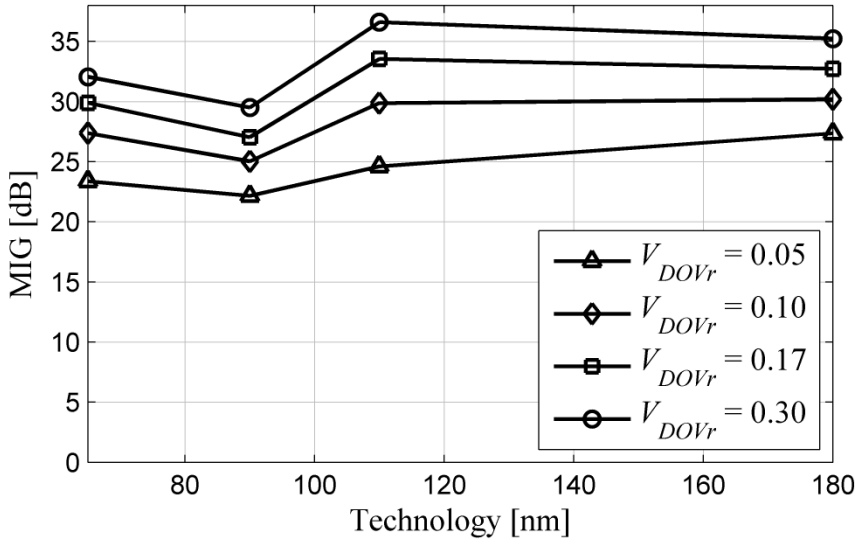

Figure 2.6 Maximum intrinsic gain for devices with $L = 360$ nm in 65 nm, 90 nm, 110 nm, and 180 nm technologies with various V_{DOVr} values and constrant drain current $I_D = 130$ µA.

the result of a limitation in device output impedance r_o due to drain-induced threshold voltage shift (DITS) [30]. In this phenomenon, the modulation of the drain voltage forces an energy barrier shift, thereby limiting the output impedance of the device.

The methodology and results in this chapter describe in further detail what is briefly touched upon in the literature: that the critical analog device parameters transconductance, g_m, and output resistance, r_o, are degrading as technologies are scaled. While MIG degradation has been shown to be a problem in previous work, this method shows that the degradation also occurs in the context of traditional design methodologies. This treatment displays the problem from the perspective of a circuit designer rather than from the perspective of a device or process engineer.

2.3 Current Design Techniques

Many high-performance analog designs are being created in sub-100 nm technologies. This section discusses a few of the currently prevailing techniques to successfully design analog circuits in these technologies.

2.3.1 Thick Oxide Devices

The most common design technique for analog design in modern CMOS technologies revolves around using thicker oxide, higher voltage I/O devices in the critical analog circuits. These higher voltage devices allow for more gate overdrive and more voltage headroom in general as well as address issues with gate current seen in thin oxide devices [31]. This eases a lot of the concerns and issues created by trying to use the low voltage digital devices. Alternatively, if low voltage devices are used for the analog design, they are usually formed from low threshold voltage variant devices. These lower V_T devices

have the same effect as the I/O devices in that high voltage overdrive, and therefore better performance, can be achieved. These devices, however, tend to have high leakage currents and cause increased power consumption. In analog circuit designs, this leakage current cannot be ignored and may be intolerable in many low-power applications.

For circuits that use I/O devices for analog design, there are several considerations that cause difficulties for this as a design methodology. First and foremost, when a process is created, the optimization of the device performance is always surrounding the low voltage core devices in the process. The performance of the I/O devices is secondary to that of the core devices and therefore is not optimized for analog use.

Secondly, the use of I/O devices requires a separate higher voltage supply. This supply must be generated on chip or be provided by the system that the IC resides in. Furthermore, the digital core of the SOC will have to interface with the analog circuitry, necessitating level-shifting circuitry. This level-shifting circuitry can be complicated to design and generally have problems with slow propagation delay and cross conduction current consumption.

Lastly, the multiple voltage domain requirements of the I/O device analog designs create complications for ESD design. An analog design methodology that did not require I/O devices and multiple voltage domains to achieve the desired circuit performance would greatly reduce the complexity of the IC or ASIC, however the use of I/O devices may still be required by other design considerations, e.g., system interface requirements in legacy technologies.

2.3.2 General Low Voltage Design Techniques

The primary limiting factor of the analog performance of devices in scaled technologies is the inability to drive high voltages on the devices to achieve the desired performance characteristics. As opposed to the use of high-voltage I/O devices, there has been work to define circuit topology and design techniques to address these voltage headroom constraints. These techniques include using the lateral BJT inherent in a MOSFET structure, operating the MOSFETs in the sub-threshold region, and forward biasing the body-source junction to reduce V_T [32] - [34]. Additionally, more traditional approaches have been proposed such as self-cascoding [31], [35], rail-to-rail input and output stages [36], and input level shifting techniques [37].

2.3.3 Current Mode Circuits

One well-explored area of circuit design is the use of current mode circuits to perform analog signal amplification and processing. This concept acknowledges the voltage headroom problems posed by decreasing voltage supplies by moving analog processes out of the voltage domain and into the current domain. Additionally, current mode circuitry simplifies the implementation of several circuit functions including summation, difference, and mixing circuits.

The original current mode circuits proposed by Sedra and Smith in 1970 [38] are referred to as current-controlled conveyors, or current conveyors (CC). Proposed as a generic circuit block, practical implementations of CC circuits have since been proposed [39] - [41]. CC circuits have continued to find applications in modern analog design [42], [43], but these implementations include voltage-mode amplifiers that suffer from the same voltage headroom concerns when designed with low voltage CMOS devices.

2.3.4 Bulk-Driven Devices

A less explored, but still plausible design technique that also addresses voltage headroom issues is the area of bulk-driven devices and circuits [44] - [49]. This concept makes use of the generally unused bulk terminal as the input to the device. Doing so allows the gate voltage to be driven to a proper bias point, but not have that bias negatively impact signal voltage ranges.

The main concerns with bulk-drive techniques are latch-up and device performance. By manipulating the bulk terminal of a device, there is a risk of forward conduction of the source-bulk device diodes. This conduction could potentially cause latch-up issues in a larger circuit. Secondly, there are currently no CMOS processes in which the device design has been optimized for bulk-driven use. This leads to a series of unnecessary degradations to device performance that limits this technique's utility in standard CMOS technologies. Some work has been done in designing a device process to produce more useful bulk driven devices [50].

2.4 Negative Feedback Theory Review

Negative feedback (NFB) is an extremely well understood and studied technique that has been traditionally used to control closed-loop gain [51] - [53]. Some basic negative feedback concepts are included here as discussion points for comparison against work in subsequent chapters.

By designing a system with high open-loop gain and applying negative feedback, one can achieve a well-controlled closed-loop gain with increased bandwidth based mainly on the

feedback factor, $\beta(s)$. The cost of this control is a reduction from the high open-loop gain of the original amplifier.

2.4.1 Block Diagram Analysis

Figure 2.7 shows a traditional negative feedback system. $X(s)$ and $Y(s)$ are the input and output signals respectively. $A(s)$ is the open-loop system transfer function, $\beta(s)$ is the feedback factor, and $e(s)$ is the error signal.

The equivalent system, $H(s)$, of the feedback system in Figure 2.7 can be shown to be

$$H(s) = \frac{A(s)}{1+A(s)\beta(s)}. \tag{2.2}$$

In this expression, $A(s)\beta(s)$ is referred to as the loop gain (LG). In order to illustrate the effect of the feedback on frequency response, the open-loop transfer function, $A(s)$, is assumed to be a single pole system of the form

$$A(s) = \frac{A_{DC}p_1}{s+p_1} \tag{2.3}$$

where A_{DC} is the DC gain and p_1 is the -3 dB bandwidth of the open-loop system. Additionally the feedback factor is assumed to be frequency-independent, $\beta(s) = \beta$.

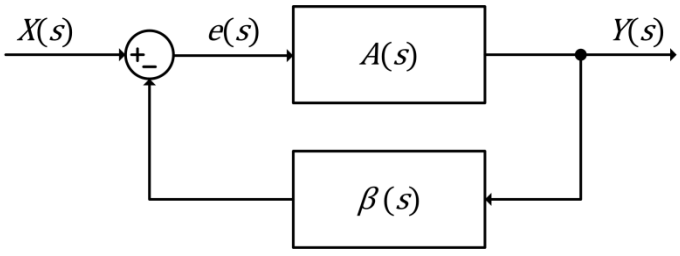

Figure 2.7 Traditional negative feedback block diagram system with forward gain $A(s)$ and feedback factor $\beta(s)$.

Substituting these assumptions into the closed-loop system provides an equivalent system

$$H(s) = \frac{A_{DC} \cdot p_1}{s + p_1(1 + A_{DC}\beta)}. \tag{2.4}$$

In this system, the DC gain has become

$$H_{DC} = \frac{A_{DC}}{1 + A_{DC}\beta} \tag{2.5}$$

and the -3 dB bandwidth is $p_{1H} = p_1(1 + A_{DC}\beta)$.

Assuming the loop gain, $A_{DC}\beta$, is a positive quantity, these equations show that the DC gain is decreased and the bandwidth is increased by the application of negative feedback. By traditional design methodologies, A_{DC} would be designed to be extremely large. Under this assumption, and more specifically, $A_{DC}\beta \gg 1$, the closed-loop behavior becomes controlled by the feedback factor with DC gain of $1/\beta$ and bandwidth of

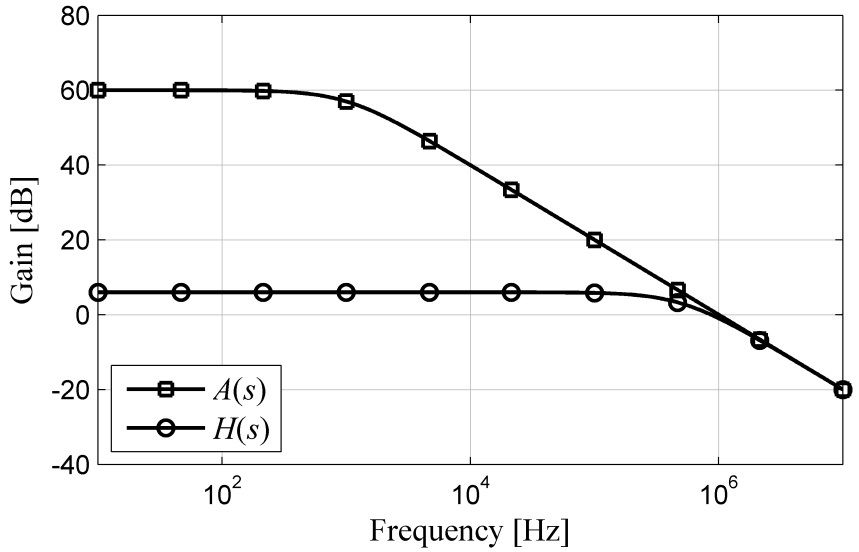

Figure 2.8 Basic negative feedback system with open-loop gain $A_{DC} = 1000$, and $p_1 = 1000$ Hz and $\beta = 0.5$.

$p_1 A_{DC}\beta$. It is also worth noting that under this analysis the gain-bandwidth product (GBP) of the open-loop system, $GBP_{A(s)} = A_{DC}p_1$, is equal to the gain-bandwidth of the closed-loop system, $GBP_{H(s)} = A_{DC}p_1$. The ratio of these two gain bandwidths, the gain-bandwidth product ratio, GBP_r, is equal to one. This implies that the reduced gain was traded for increased bandwidth while applying negative feedback. Figure 2.8 shows an example of the open- and closed-loop systems' frequency behavior with $A_{DC} = 1000$ V/V, $p_1 = 1$ kHz, and $\beta = 0.5$ V/V. This example illustrates the fact that the gain and bandwidth of the amplifier have moved, but their product has not.

2.4.2 Ideal Operational Amplifier Analysis

Using an ideal opamp model for the base amplifier as shown in Figure 2.9, the negative feedback transfer function can be calculated as

$$H(s) = \frac{V_{out}}{V_{in}} = -\frac{A(s)\frac{R_2}{R_1+R_2}}{1+A(s)\frac{R_1}{R_1+R_2}} = -\frac{A_f}{1+A_f\beta_f} \tag{2.6}$$

where $A(s)$ is the forward voltage gain transfer function of the opamp, the closed-loop forward gain is

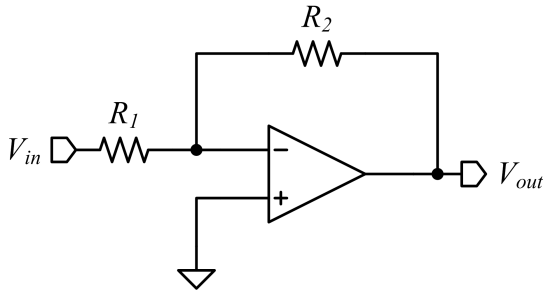

Figure 2.9 Negative feedback system with ideal opamp having zero output impedance and infinite input impedance and voltage gain transfer function $A(s)$.

$$A_f = \mathrm{A(s)}\frac{R_2}{R_1+R_2} \tag{2.7}$$

and the feedback factor is $\beta_f = R_1/R_2$. For the single-pole model of $A(s)$ in (2.3) this becomes

$$H(s) = -\frac{p_1 A_{DC}\frac{R_2}{R_1+R_2}}{s+p_1\left(1+A_{DC}\frac{R_1}{R_1+R_2}\right)} \tag{2.8}$$

with a DC gain of

$$H_{DC} = |H(0)| = \frac{A_{DC}\frac{R_2}{R_1+R_2}}{1+A_{DC}\frac{R_1}{R_1+R_2}} = \frac{A_{DCf}}{1+A_{DCf}\beta_{DCf}} \tag{2.9}$$

and -3 dB bandwidth of

$$p_{1H} = p_1\left(1 + A_{DCf}\beta_{DCf}\right) \tag{2.10}$$

where

$$A_{DCf} = A_{DC}\frac{R_2}{R_1+R_2} \tag{2.11}$$

and $\beta_{DCf} = \beta_f = R_1/R_2$.

In this traditional analysis, the loop gain $A_f\beta_f$ and $A_{DCf}\beta_{DCf}$ are designed such that they are much greater than one, and the closed-loop gain simplifies to $H(s) \approx -1/\beta_f$.

2.4.2.1 Input and Output Impedance

The ideal operational amplifier has infinite input impedance but finite output impedance. In the case of output impedance, the output terminal of the opamp is connected directly to

the output net. The ideal source and sink capabilities of that opamp are not altered by the application of negative feedback which means that the output impedance remains ideal as $Z_{out} = 0$.

The input impedance, however, is altered because the input signal does not drive the opamp directly, but instead drives the feedback network. Analysis of this network means the input impedance of the negative feedback amplifier is

$$Z_{in}(s) = \frac{R_1(1+A(s))+R_2}{(1+A(s))} \approx R_1. \tag{2.12}$$

This approximation of R_1 holds true if $A(s)$ is large, as is the case in traditional feedback design systems. This implies that the infinite input impedance has been reduced by the application of feedback. Figure 2.10 shows this Z_{in} reduction for various values of A_{DC}.

One often un-discussed repercussion of (2.12) is that the previously frequency-

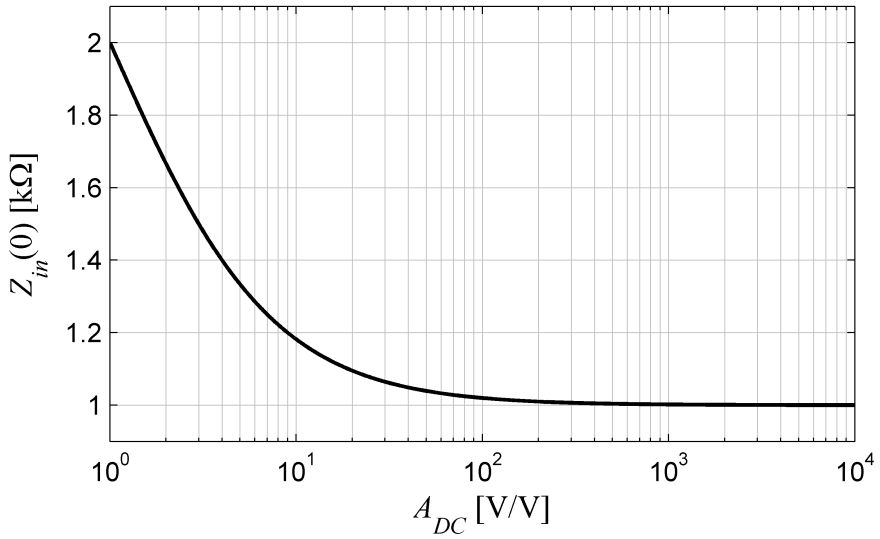

Figure 2.10 DC input impedance of a negative feedback amplifier versus A_{DC} with $R_1 = 1$ kΩ and $R_2 = 2$ kΩ, and therefore $\beta = 0.5$.

independent input impedance now has frequency dependence. Applying the single-pole model (2.3), Z_{in} becomes

$$Z_{in}(s) = \left\{\frac{s+p_1\left[\frac{R_1}{R_1+R_2}(1+\mathrm{A_{DC}})+\frac{R_2}{R_1+R_2}\right]}{s+p_1(1+\mathrm{A_{DC}})}\right\}(R_1+R_2). \tag{2.13}$$

which contains a zero at

$$z_{1in} = p_1\left[\frac{R_1}{R_1+R_2}(1+A_{DC})+\frac{R_2}{R_1+R_2}\right] \tag{2.14}$$

and a pole at

$$p_{1in} = p_1(1+A_{DC}). \tag{2.15}$$

Figure 2.11 shows this frequency behavior for various values of A_{DC}. This figure shows that as the frequency increases, the input impedance increases in magnitude and therefore

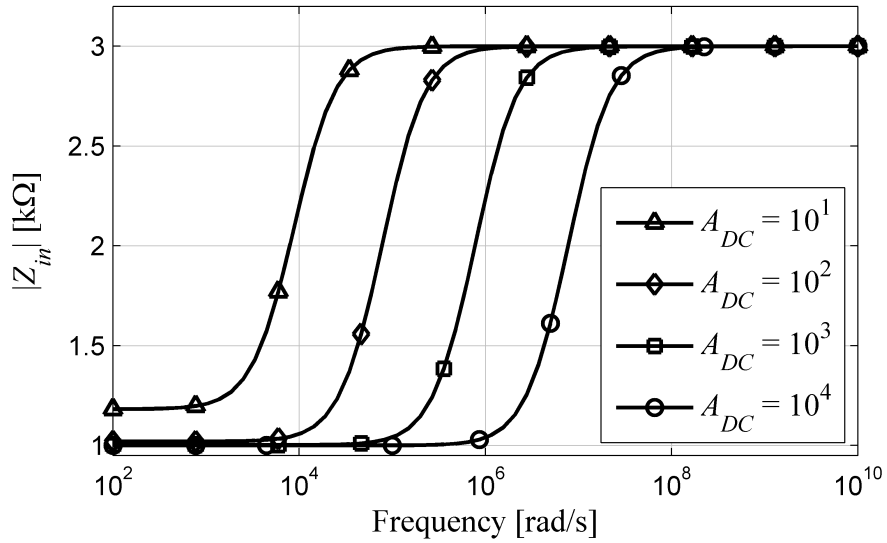

Figure 2.11 Magnitude of $Z_{in}(s)$ versus frequency for negative feedback amplifiers with $p_1 = 1000$ Hz, $R_1 = 1$ kΩ, and $R_2 = 2$ kΩ.

becomes more ideal.

2.4.2.2 Negative Feedback with Input-Referred Offset

While many designs attempt to minimize it, every amplifier has input-referred offset. The negative feedback opamp shown in Figure 2.12 shows an ideal opamp with DC gain A_{DC} and an input-referred offset of V_{os}. Since input-referred offset is a DC value, there is no frequency dependence in this analysis. The effects of this offset are calculated at the output of the opamp

$$H_{os} = \frac{V_{out}}{V_{os}} = \frac{A_{DC}}{1+A_{DC}\frac{R_1}{R_1+R_2}} = \frac{A_{DCf}(1+\beta_{DCf})}{1+A_{DCf}\beta_{DCf}} \tag{2.16}$$

and then the output value, V_{out}, is divided by the open-loop gain, H_{DC}, to derive the input-referred offset expression

$$V_{os,in} = \frac{H_{os}}{\mathrm{H_{DC}}}V_{os} = -(1+\beta_{DCf})V_{os}. \tag{2.17}$$

In this traditional analysis, β_{DCf} is less than one, but greater than zero. This implies that the input-referred offset of the baseline amplifier is increased through the application of negative feedback.

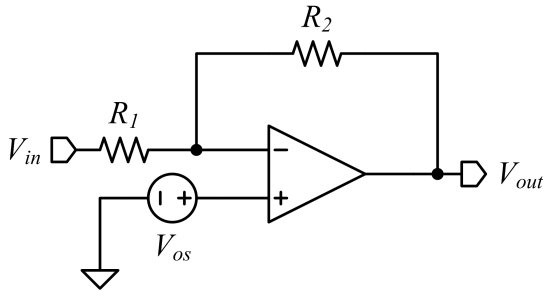

Figure 2.12 Negative feedback system with ideal opamp having input-referred offset, V_{os}.

2.4.2.3 Negative Feedback with Input-Referred Noise

Another important amplifier parameter is input-referred noise. While it is well known that the addition of resistive elements to a circuit will add resistive thermal noise, the application of negative feedback will shape this noise. To calculate this effect, superposition is used on the amplifier in Figure 2.13 to calculate each noise source's effect on the output signal. The contribution from the baseline amplifier noise is

$$V_{out,ea} = e_a \frac{A_f(1+\beta_f)}{1+A_f\beta_f} \tag{2.18}$$

where e_a is the baseline amplifier input-referred noise. The contributions from the feedback resistors R_1 and R_2 can be calculated as

$$V_{out,e1} = -e_1 \frac{A_f}{1+A_f\beta_f} \tag{2.19}$$

and

$$V_{out,e2} = e_2 \frac{A_f\beta_f}{1+A_f\beta_f} \tag{2.20}$$

respectively. Summing the square of these signals to get the total noise power at the

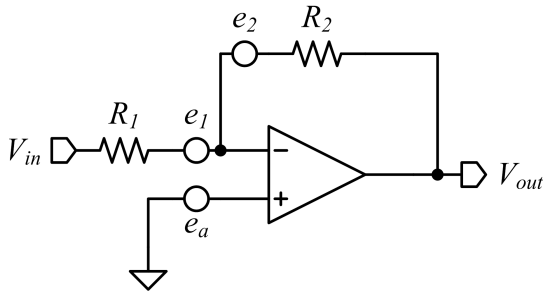

Figure 2.13 Negative feedback system with ideal opamp having input-referred noise noise and resistive feedback with thermal noise sources.

output gives

$$V_{out}^2 = e_a^2\left[\frac{A_f(1+\beta_f)}{1+A_f\beta_f}\right]^2 + e_1^2\left[\frac{A_f}{1+A_f\beta_f}\right]^2 + e_2^2\left[\frac{A_f\beta_f}{1+A_f\beta_f}\right]^2. \quad (2.21)$$

Finally, referring this output noise power back to the input by diving by the closed-loop gain squared gives

$$E_{in}^2 = V_{out}^2\left[\frac{1+A_f\beta_f}{A_f}\right]^2. \quad (2.22)$$

This expression simplifies to $E_{in}^2 = e_a^2(1+\beta_f)^2 + e_1^2 + e_2^2\beta_f^2$, and $E_{in}^2 = e_a^2(1+\beta_f)^2 + 4kT\Delta f R_1(1+\beta_f)$.

While the resistive components of thermal noise are new, the input-referred noise from the opamp itself is shaped by $(1+\beta_f)^2$. Because β_f is between zero and one, this represents an increase in the input-referred noise of the negative feedback structure.

2.4.2.4 Negative Feedback Gain-Bandwidth Product

In the ideal block diagram analysis of positive feedback, the GBP remained constant before and after the application of negative feedback. In the case of the opamp analysis, the same single-pole model can be assumed for the baseline amplifier. In this case, the DC gain of the negative feedback amplifier is known, and the -3 dB bandwidth becomes $p_{1H} = p_1(1 + A_{DCf}\beta_{DCf})$ and the gain-bandwidth product can be calculated as

$$GBP = \frac{R_2}{R_1+R_2}A_{DC}p_1. \quad (2.23)$$

Comparing this value to the baseline amplifier gain-bandwidth product, the gain-bandwidth product ratio can be defined as

$$GBP_r = \frac{R_2}{R_1+R_2} = \frac{1}{1+\beta_{DCf}}. \tag{2.24}$$

With β_{DCf} assumed to be between zero and one, the GBP_r will always be less than one. This means that the gain-bandwidth product conservation shown in the block diagram analysis does not hold true in a more realistic implementation of negative feedback. This GBP_r decrease is primarily due to the closed-loop forward gain, A_{DCf}, degradation by the feedback resistive divider ratio. This degradation is illustrated in Figure 2.14. This simulation was performed with the same parameters as Figure 2.9 with $A_{DC} = 1000$ V/V, $p_1 = 1$ kHz, $R_1 = 1$ kΩ, and $R_2 = 2$ kΩ.

2.4.3 Differential Amplifier Analysis

To review some of the more nuanced behavior of negative feedback, a more realistic

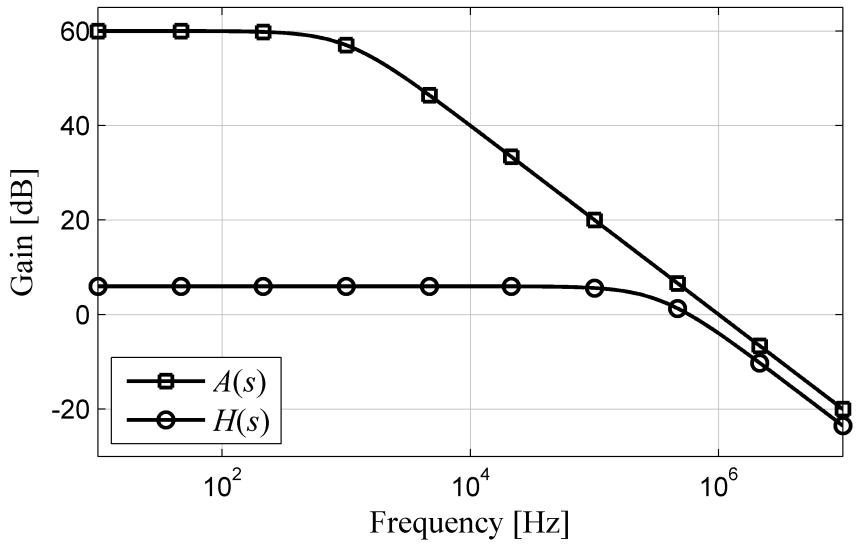

Figure 2.14 Negative feedback system with ideal opamp gain bandwidth product degradation with $A_{DC} = 1000$, $p_1 = 1000$ Hz, $R_1 = 1$ kΩ, and $R_2 = 2$ kΩ.

structure of a typical differential amplifier is used. Figure 2.15 shows a differential amplifier with resistive negative feedback via R_1 and R_2 resistors. Nodal analysis of the small-signal model of this amplifier, shown in Figure 2.16, gives the voltage gain transfer function

$$H = \frac{V_{out}}{V_{in}} = \frac{\frac{R_2}{R_2+R_L}\cdot\frac{R_2}{R_1+R_2}\left(g_m R_L - \frac{R_L}{R_2}\right)}{1+\frac{R_2}{R_2+R_L}\cdot\frac{R_1}{R_1+R_2}\left(g_m R_L - \frac{R_L}{R_2}\right)} = \frac{A_f}{1+A_f\beta_f} \tag{2.25}$$

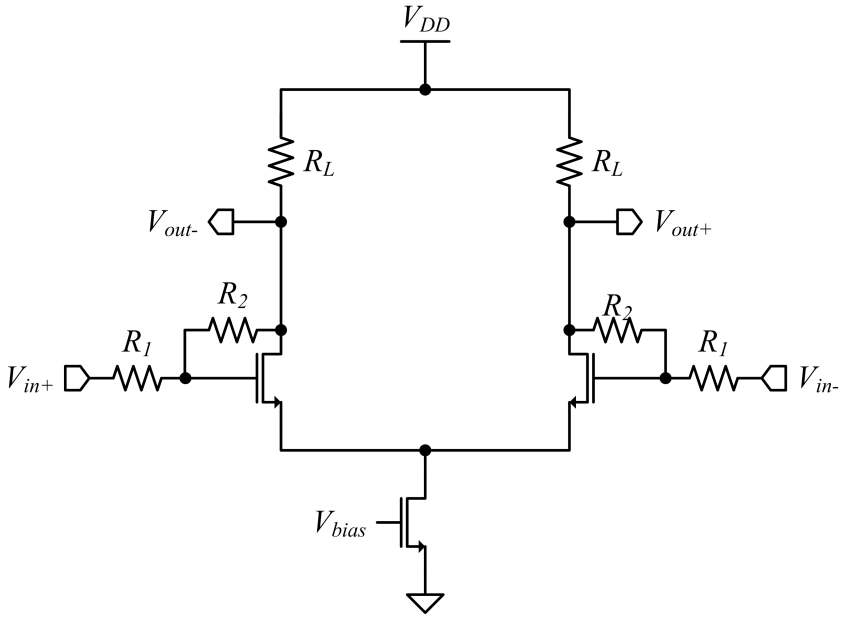

Figure 2.15 Differential amplifier with differential negative feedback formed by the resistive network R_1 and R_2.

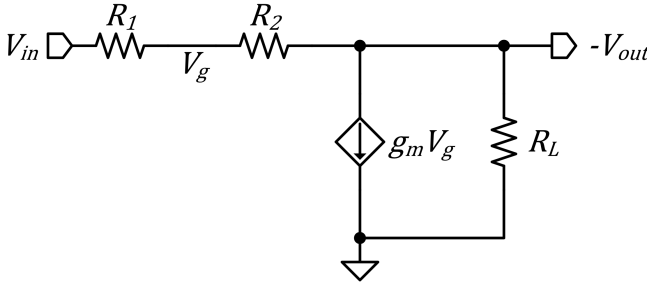

Figure 2.16 Small-signal model of negative feedback differential amplifier using the virtual ground principal of common-source node of the input differential pair.

where g_m is the small-signal transconductance of the input MOSFETs, the closed-loop forward gain is defined as

$$A_f = \frac{R_2}{R_2+R_L} \cdot \frac{R_2}{R_1+R_2}\left(g_m R_L - \frac{R_L}{R_2}\right) \tag{2.26}$$

and the feedback factor is defined as $\beta_f = R_1/R_2$.

In this model the small-signal output impedance of the input devices, r_o, is assumed to be very large for clarity. However, r_o could easily be factored into the load component, $R_L = R_L||r_o$. This result is identical to the ideal opamp case. However, because the open-loop gain A_f is degraded by a series of resistive dividers, the assumption of $A_f\beta_f$ being much greater than one may not always hold true.

2.4.3.1 Negative Feedback with Input-Referred Offset

This analysis shows how applying negative feedback to a differential amplifier circuit

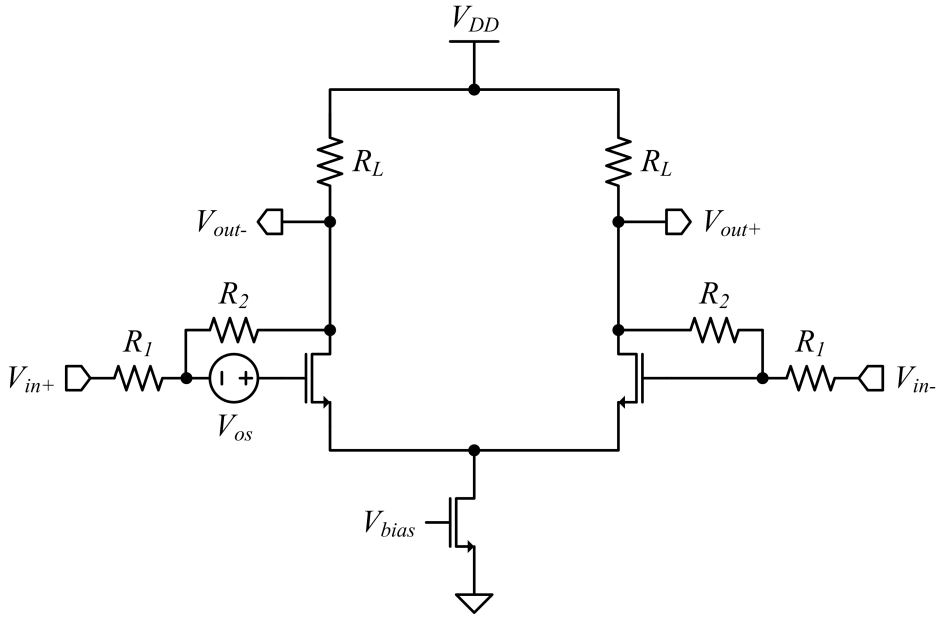

Figure 2.17 Differential amplifier with input-referred offset, V_{os} and differential negative feedback formed by the resistive network R_1 and R_2.

with input-referred offset, V_{os}, affects that offset. Figure 2.17 shows such an example amplifier. In this analysis, first the offset transfer function of V_{os} to V_{out} is defined

$$H_{os} = \frac{V_{out}}{V_{os}} = \frac{\frac{R_2}{R_2+R_L}(g_m R_L)}{1+\frac{R_2}{R_2+R_L}\frac{R_1}{R_1+R_2}\left(g_m R_L - \frac{R_L}{R_2}\right)}. \tag{2.27}$$

From this expression, the input-referred offset can be found by dividing V_{out} by the forward voltage gain, $H(s)$,

$$V_{os,in} = \frac{\mathrm{V_{out}}}{\mathrm{H}} V_{os} = \frac{g_m R_L(1+\beta_f)}{g_m R_L - \frac{R_L}{R_2}} V_{os}. \tag{2.28}$$

Under the assumption that $g_m R_L$ is larger than R_L/R_2, this expression can be simplified to $V_{os,in} \approx (1+\beta_f)V_{os}$.

While β_f can take on many values, it is always a positive quantity in negative feedback and usually less than one. As a result, the input-referred offset of the negative feedback amplifier is increased from that of the baseline amplifier by a factor of $(1+\beta_f)$.

2.4.3.2 Negative Feedback with Input-Referred Noise

Calculating the input-referred noise of the negative feedback differential amplifier is also an important concept to look at. In Figure 2.18 the resistor noise sources are modeled as e_1 and e_2 while the input-referred noise of the baseline amplifier is defined as e_a. Using superposition to calculate each noise source's impact on the output, the baseline amplifier noise contribution is

$$V_{out,ea} = e_a \frac{\frac{R_2}{R_2+R_L}(g_m R_L)}{1+\frac{R_2}{R_2+R_L}\frac{R_1}{R_1+R_2}\left(g_m R_L - \frac{R_L}{R_2}\right)} \tag{2.29}$$

while the contribution from R_1 is

$$V_{out,e1} = e_1 \frac{\frac{R_2}{R_2+R_L}\cdot\frac{R_2}{R_1+R_2}\left(g_m R_L - \frac{R_L}{R_2}\right)}{1+\frac{R_2}{R_2+R_L}\cdot\frac{R_1}{R_1+R_2}\left(g_m R_L - \frac{R_L}{R_2}\right)} \tag{2.30}$$

and finally R_2's contribution is

$$V_{out,e2} = -e_2 \frac{\frac{R_2}{R_2+R_L}\cdot\frac{R_1}{R_1+R_2}\left(g_m R_L + \frac{R_L}{R_1}\right)}{1+\frac{R_2}{R_2+R_L}\cdot\frac{R_1}{R_1+R_2}\left(g_m R_L - \frac{R_L}{R_2}\right)}. \tag{2.31}$$

The squared sum of these contributions leads to a total RMS noise at the amplifier output of $V_{out}^2 = V_{out,ea}^2 + V_{out,e1}^2 + V_{out,e2}^2$.

Transferring this quantity back to the input gives an input-referred noise of

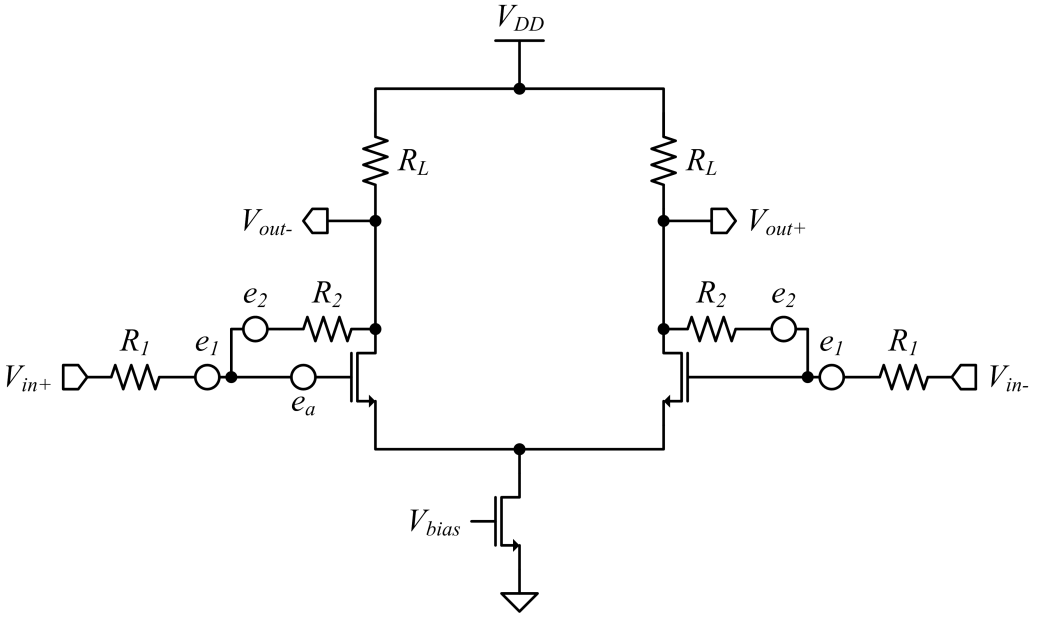

Figure 2.18 Differential amplifier with differential negative feedback and noise sources consisting of the differential amplifier input-referred noise, e_a, and the thermal noise of resistors R_1 and R_2, e_1 and e_2.

$$E_{in}^2 = V_{out}^2 \left[\frac{1+A_f\beta_f}{A_f}\right]^2 \tag{2.32}$$

which expands to

$$E_{in}^2 = e_a^2 \left[\frac{g_m R_L(1+\beta_f)}{g_m R_L - \frac{R_L}{R_2}}\right]^2 + 2e_1^2 + 2e_2^2 \left[\beta_f \frac{g_m R_L + \frac{R_L}{R_1}}{g_m R_L - \frac{R_L}{R_2}}\right]^2. \tag{2.33}$$

Applying the thermal noise contributions from the resistors R_1 and R_2 gives the input-referred noise as

$$E_{in}^2 = e_a^2 \left[\frac{g_m R_L(1+\beta)}{g_m R_L - \frac{R_L}{R_2}}\right]^2 + 8kT\Delta f R_1 + 8kT\Delta f R_2 \left[\beta_f \frac{g_m R_L + \frac{R_L}{R_1}}{g_m R_L - \frac{R_L}{R_2}}\right]^2 \tag{2.34}$$

which simplifies to $E_{in}^2 \approx e_a^2(1+\beta)^2 + 8kT\Delta f R_1\left(1+\beta_f\right)$ under the condition that $g_m R_L$ is greater than R_L/R_2. This relationship shows that the input-referred noise of the amplifier is increased by a factor of $\left(1+\beta_f\right)^2$. This noise increase is in addition to the thermal noise contributions from R_1 and R_2.

2.4.3.3 Negative Feedback Common-Mode Rejection Ratio

The baseline amplifier CMRR is well understood to be $CMRR_{OL} = 1 + 2g_m R_{tail}$ [51], [52], [54] where R_{tail} is the output impedance of the current source in the differential pair's source terminals as shown in Figure 2.19. Using the half-amplifier model, the common-mode gain, H_c, can be calculated as a function of $CMRR_{OL}$

$$H_c = \frac{\frac{R_2}{R_2+R_L}\cdot\frac{R_2}{R_1+R_2}\left(\frac{g_m R_L}{CMRR_{OL}} - \frac{R_L}{R_2}\right)}{1+\frac{R_2}{R_2+R_L}\cdot\frac{R_1}{R_1+R_2}\left(\frac{g_m R_L}{CMRR_{OL}} - \frac{R_L}{R_2}\right)} = \frac{A_{f,c}}{1+A_{f,c}\beta_f} \tag{2.35}$$

where

$$A_{f,c} = \frac{R_2}{R_2+R_L} \cdot \frac{R_2}{R_1+R_2}\left(\frac{g_m R_L}{CMRR_{OL}} - \frac{R_L}{R_2}\right) \tag{2.36}$$

and $\beta_{f,c} = R_1/R_2$.

CMRR is defined as the ratio of the differential gain to the common-mode gain. The CMRR of the negative feedback amplifier is shown to be

$$CMRR = \left|\frac{A_f}{A_c}\right| = \frac{A_f}{A_{f,c}} \cdot \frac{1+A_{f,c}\beta_f}{1+A_f\beta_f}. \tag{2.37}$$

2.4.3.4 Negative Feedback Gain-Bandwidth Product

To observe the effects of negative feedback on gain-bandwidth product in the differential amplifier, the frequency response of the baseline amplifier is calculated as

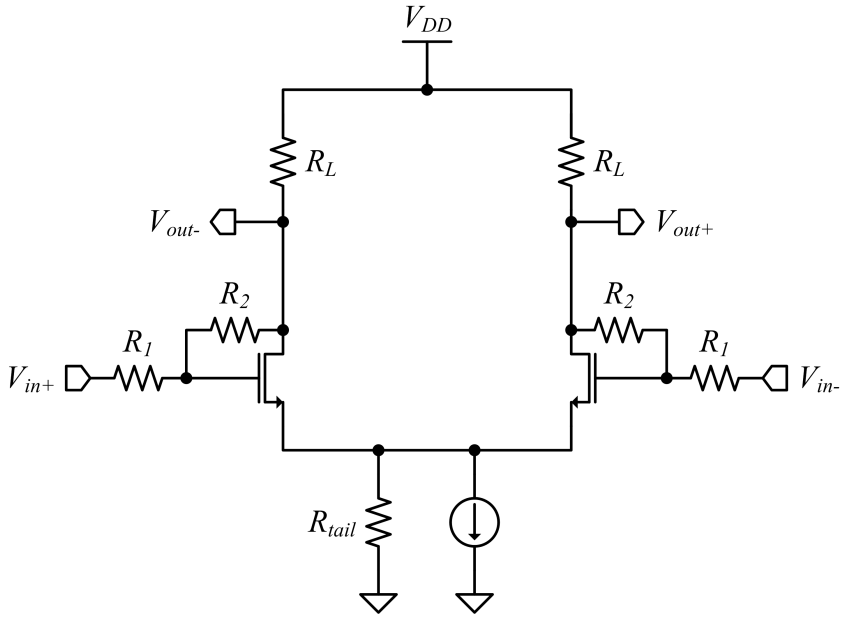

Figure 2.19 Differential amplifier with differential negative feedback for CMRR analysis with finite output impedance, R_{tail}, current source supplying the input differential pair.

$$A(s) = \frac{g_m R_L}{1+sR_L C_L} \tag{2.38}$$

where C_L is the capacitive load as shown in Figure 2.20. The DC gain of this amplifier is $A_{DC} = g_m R_L$ and the -3 dB bandwidth is $p_1 = 1/(R_L C_L)$ yielding a gain-bandwidth product of $GBP = g_m/C_L$.

Analysis of the negative feedback structure with the same capacitive load as in Figure 2.21 gives a transfer function

$$H(s) = \frac{\frac{R_2}{R_1+R_2}\frac{R_2}{R_2+R_L}\left(g_m R_L - \frac{R_L}{R_2}\right)}{s\frac{R_2 R_L C_L}{R_2+R_L} + 1 + \frac{R_1}{R_1+R_2}\frac{R_2}{R_2+R_L}\left(g_m R_L - \frac{R_L}{R_2}\right)}. \tag{2.39}$$

The DC gain here is as was previously defined, and the -3 dB bandwidth is

$$p_{1H} = p_1 \frac{R_2+R_L}{R_2}\left(1 + A_f \beta_f\right) \tag{2.40}$$

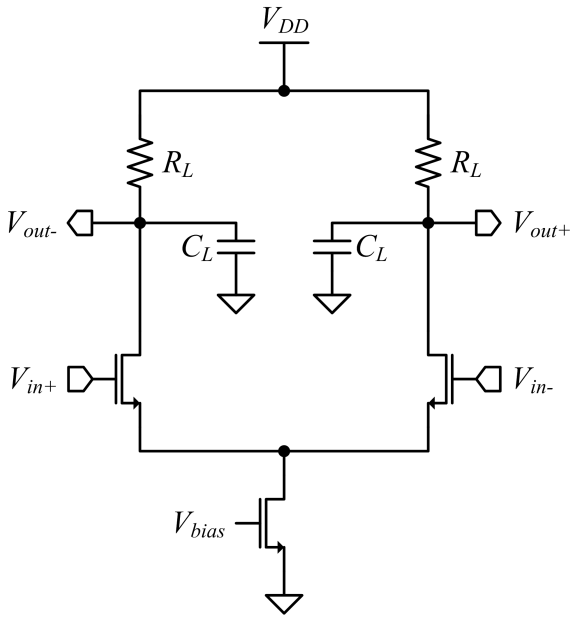

Figure 2.20 Differential amplifier with capacitive load, C_L, for frequency response analysis.

yielding a gain-bandwidth product of

$$GBP = p_1 \frac{R_2}{R_1+R_2}\left(g_m R_L - \frac{R_L}{R_2}\right) \tag{2.41}$$

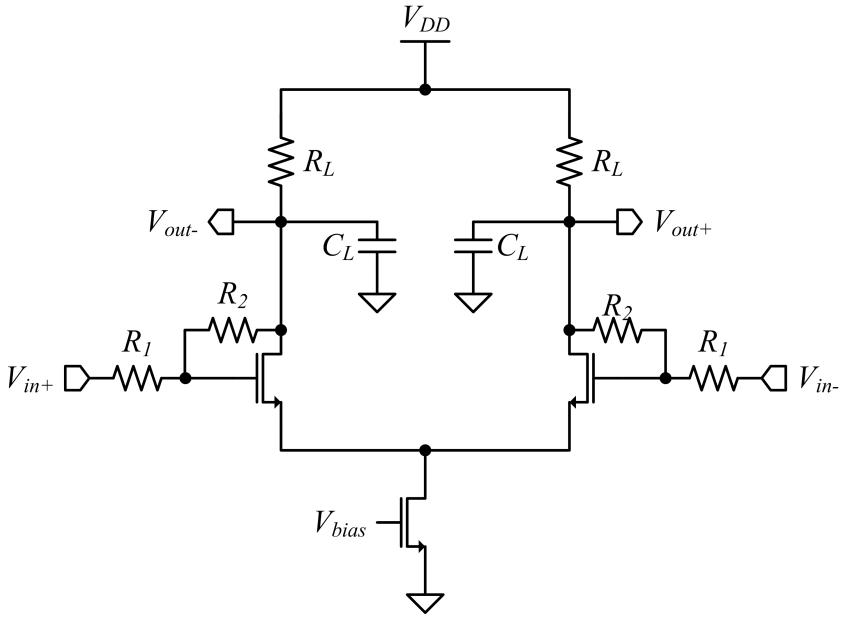

Figure 2.21 Differential amplifier with negative feedback and capacitive load, C_L, for frequency response analysis.

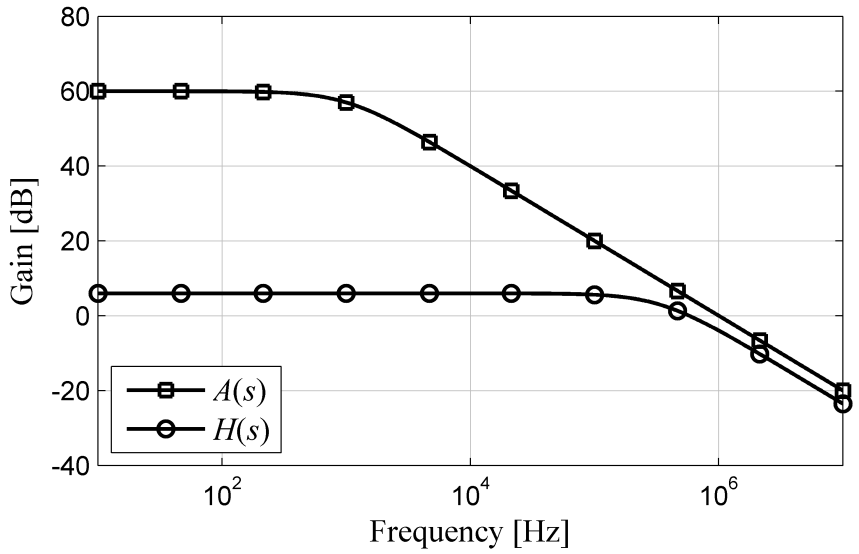

Figure 2.22 Differential amplifier with negative feedback gain bandwidth product with $g_m = 1$ S, $R_L = 1$ kΩ, $C_L = 1$ µF, $R_1 = 1$ kΩ, and $R_2 = 2$ kΩ.

and a gain-bandwidth product ratio of

$$GBP_r = \frac{R_2}{R_2+R_L}\left(1 - \frac{1}{g_m R_2}\right). \tag{2.42}$$

Both multiplicands in this equation are less than one. This corresponds to a decrease in the gain-bandwidth product of the negative feedback differential amplifier. Figure 2.22 shows an example of this degradation with $g_m = 1$ S, $R_L = 1$ kΩ, $C_L = 1$ μF, $R_1 = 1$ kΩ, and $R_2 = 2$ kΩ. While these g_m and C_L values are unrealistic for a single stage differential amplifier implemented on an IC, there are used here for comparison to the other analyses.

2.5 Summary

This chapter has discussed the issues facing analog circuit designers working in modern sub-100 nm technologies. Specifically, the maximum intrinsic gain of transistors used in these designs has begun to degrade to the point of complicating traditional analog design techniques. While these device degradations are the natural course of process scaling, it is outside of the scope of a typical analog circuit design to address these issues at a process level. Therefore, the circuit designer must apply circuit solutions to address these process problems.

New techniques have been proposed to address this MIG degradation problem and design in scaled technologies in general. While some of these proposals are useful in some applications, there are fundamental issues with each that would prevent its general widespread use in analog circuit design. As an addition to these techniques, this work proposes a new design methodology to address these process issues. A formal review of

negative feedback design techniques and implications was provided as a basis for discussion of the new proposed design methodology in this work.

CHAPTER 3
APPROACH

The degradation of intrinsic gain with technology scaling was described in the previous chapter. As a circuit designer, the process is predefined and has characteristics and performance optimized for digital circuitry. Therefore any useful solution must be circuit-based. As is the case with any circuit solution, there is no single ideal topology that will address all problems.

3.1 Positive Feedback Theory

Applying positive feedback to traditional amplifier topologies is the lowest risk circuit solution to intrinsic gain degradation in scaled technology [55], [56]. Positive feedback has been discussed previously in the literature and can be broken down into two categories: digital positive feedback and analog positive feedback. The digital positive feedback is used in digital switching circuits to cause transitions to occur more quickly, to add hysteresis, or to reduce power consumption in low power modes [57], [59]. This methodology is of little concern to analog design as the input and output signals are generally rail-to-rail. The digital positive feedback circuits generally have little concern for linearity.

The second type of positive feedback is applied to analog circuitry. Because of the sensitive nature of positive feedback and a high likelihood of causing amplifier instability, most treatments of analog positive feedback are extremely topology-specific as in [60] - [68] and most famously, the regenerative AM receiver by Armstrong in 1914 [69]. This implies that the positive feedback presented in that work can only be used with those topologies. The most generic description of positive feedback is shown in [70]

but speaks of it in the context of using negative feedback in a larger loop to keep the system stable. It does not address where and when positive feedback may be used on its own and to what extent it will change the system performance. Additionally, positive feedback has been proposed for self-biasing [71] which does not incorporate feedback on the entire amplifier as well as for RF low-noise amplifiers (LNA) [72], [73]. The application to LNAs is the closest to the goals achieved by this work. Because LNAs are generally low gain to start with, the authors were able to apply positive feedback in a stable fashion. However, this positive feedback is still strictly defined by the amplifier topology. The work presented here treats positive feedback in the most generic manner as it could possibly be applied to any circuit topology with the addition of only small resistors and without a larger negative feedback loop.

The analysis in this section is meant to closely model the negative feedback analysis commonly found in text books [51]. The models and implementations have been changed to form positive feedback systems, but much of the sub-circuit nomenclature has remained the same. The purpose of this is to facilitate comparisons between negative feedback work.

3.1.1 Generalized Theory

Figure 3.1 shows a positive feedback system. The only difference between this and the negative feedback system is that the difference node of the negative feedback system has become a summation node. The equivalent system of this configuration can be shown to be

$$H(s) = \frac{Y(s)}{X(s)} = \frac{A(s)}{1-A(s)\beta(s)}. \tag{3.1}$$

The loop gain of this system, $LG = A(s)\beta(s)$, is critical in defining the performance of the closed-loop system. Figure 3.2 shows the relationship between $H(s)$ and LG for $A(s) = 10$. The purpose of applying positive feedback to an amplifier is to increase the gain of the open-loop amplifier, $A(s)$. Evaluating (3.1) under the condition of increased gain, if the value of the LG is greater than zero and less than one, then the value of $H(s)$ will be larger than the value of $A(s)$.

For the LG range of one to two, the magnitude of $H(s)$ will be greater than the magnitude of $A(s)$, but its phase will have shifted 180°. In a linear system, this phase shift would

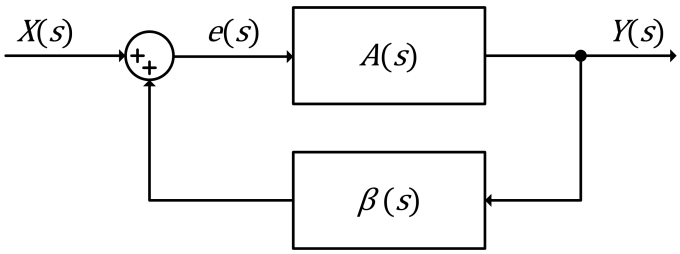

Figure 3.1 Generalized positive feedback system with forward gain $A(s)$ and feedback factor $\beta(s)$.

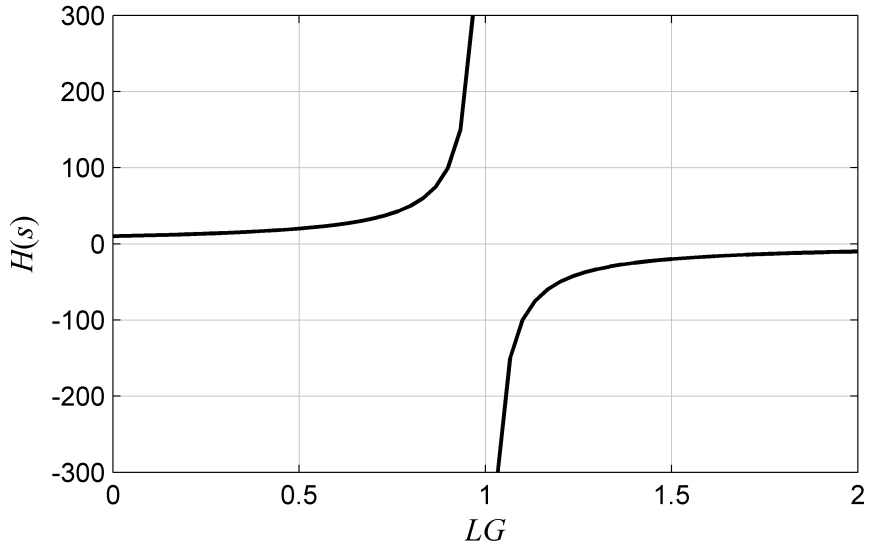

Figure 3.2 Positive feedback system, $H(s)$, versus loop gain with $A(s) = 10$.

not have an impact on the amplifier's performance. Considerations in the frequency domain, however, prevent this secondary range's usefulness and stability.

3.1.1.1 Stability Considerations for Positive Feedback

To investigate general stability considerations, the single-pole open-loop system model in (2.3) can be applied to the positive feedback system. The resulting frequency-dependent system is

$$H(s) = \frac{A_{DC} \cdot p_1}{s + p_1(1 - A_{DC}\beta)}. \tag{3.2}$$

The closed-loop gain of this system is $H_{DC} = A_{DC}/(1 - A_{DC}\beta)$ with a -3 dB bandwidth of $p_{1H} = p_1(1 - A_{DC}\beta)$. As is the case with the negative feedback system, the gain-bandwidth product remains constant as compared to the open-loop amplifier at $GBP = p_1 A_{DC}$.

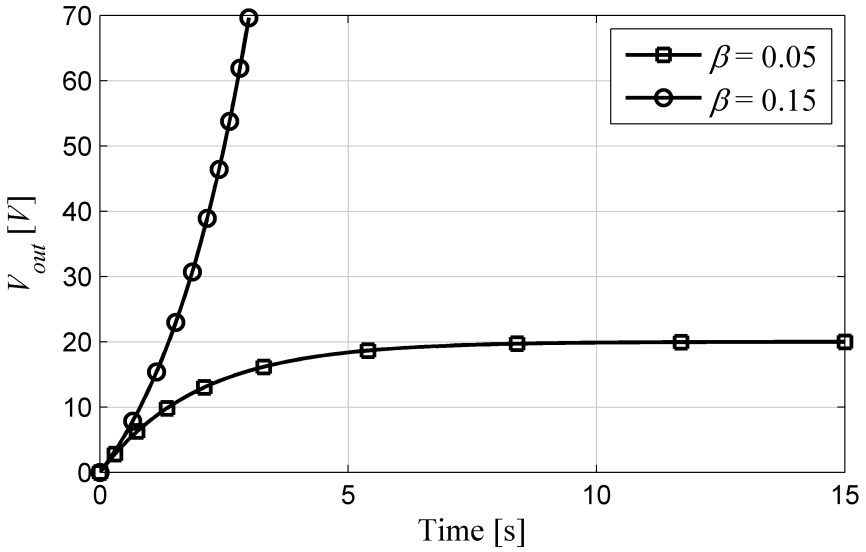

Figure 3.3 Step response of equivalent magnitude $H(s)$ positive feedback systems – stable, $\beta = 0.05$, and unstable, $\beta = 0.15$, with $A_{DC} = 10$ and $p_1 = 1$ kHz.

The step response in the time domain of two example systems is shown in Figure 3.3 with $A_{DC} = 10$, $p_1 = 1$ kHz, and two feedback factors $\beta_1 = 0.05$ and $\beta_2 = 0.15$. The resulting closed-loop systems are

$$H_1(s) = \frac{10{,}000}{s+500} = \frac{20}{s/500+1} \tag{3.3}$$

and

$$H_2(s) = \frac{10{,}000}{s-500} = \frac{20}{s/500-1}. \tag{3.4}$$

The only difference between (3.3) and (3.4) is the sign of the pole location. Shown in Figure 3.5, system $H_1(s)$ has a left-half plane (LHP) pole because $s = -500$ on the complex Cartesian coordinate system is to the left of the imaginary axis. $H_2(s)$ on the other hand, has a right-half plane (RHP) pole with $s = 500$.

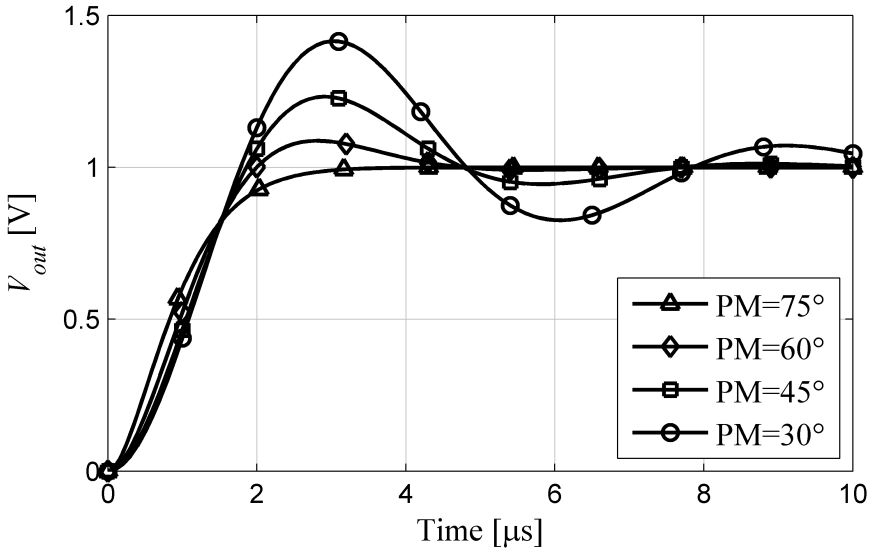

Figure 3.4 Step response of systems with various phase margins with $A_{DC} = 1000$ and $\omega_{UGF} = 1$ rad/s.

Figure 3.3 shows the systems' response to a unit step input. The system with the LHP pole is stable and achieves a final value of $V_{out}(t) = 20$. The output of the RHP pole system, however, is unbounded with a bounded input. This implies that the system is unstable.

Therefore for a positive feedback system to remain stable, the closed-loop system must contain only LHP poles. Any RHP pole would cause instability. In terms of the system described by (3.2), this implies $(1 - A_{DC}\beta) > 0$. This can be combined with the previously defined condition to increase the closed-loop gain. This implies a second bound of $A_{DC}/(1 - A_{DC}\beta) > A_{DC}$. Under these conditions and $A_{DC} > 0$, the range of valid feedback factors can be shown to be

$$0 < \beta < \frac{1}{A_{DC}}. \tag{3.5}$$

Equation (3.5) illustrates the fundamental problem with applying positive feedback using

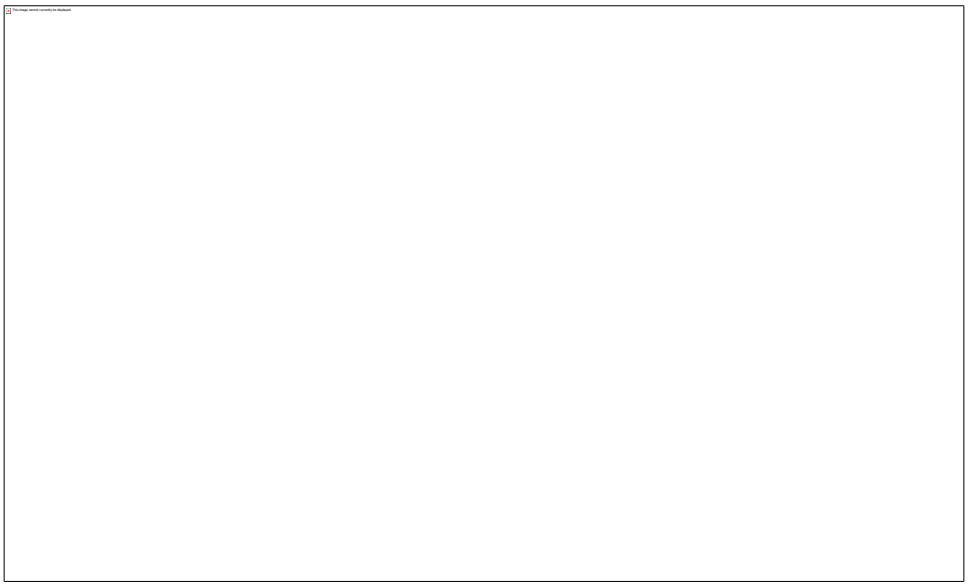

Figure 3.5 Pole plot for stable, $\boldsymbol{\beta = 0.05}$, and unstable, $\boldsymbol{\beta = 0.15}$, positive feedback amplifiers with $\boldsymbol{A_{DC} = 10}$ and $\boldsymbol{p_1 = 1}$ kHz.

traditional design methodologies. Because amplifiers are generally designed to have large A_{DC}, the valid range of feedback factors becomes extremely narrow. In scaled technologies, however, the $g_m r_o$ product has a strong impact on amplifier gain and is decreasing, thereby decreasing A_{DC}. This means that as technologies are scaled, the application of positive feedback becomes more feasible. The very problem that this work is meant to address is also what makes the solution of positive feedback feasible.

To summarize, the stability criteria for a positive feedback system design are

$$\begin{aligned} H_{DC} &> A_{DC} \\ p_{1H} &> 0 \end{aligned} \tag{3.6}$$

3.1.1.2 Traditional Stability Considerations

Traditional stability analysis of a negative feedback system involves observing the magnitude and phase of the LG, $A(s)\beta(s)$ [51] - [53], [74] - [76]. Qualitatively, the stability analysis can be described in terms of the ideal negative feedback system in Figure 2.7. As long as the difference node remains a difference node, the system will remain stable. However, because of the frequency dependence of the LG, the phase will change. If this phase change reaches $\pm 180°$, the difference node essentially becomes a summation node. For a system with sufficient poles and zeros to achieve $\pm 180°$ phase shift, this transformation is inevitable. The stability of the system, however, is a function of the magnitude of the LG when this phase reversal occurs. If the LG is greater than or equal to one, the system output becomes unbounded as the error signal adds to itself and grows in magnitude. This is regenerative positive feedback.

Qualitatively, the stability of a system can be described by observing two calculations: phase margin (PM) and gain margin (GM). Phase margin is the LG phase in excess of $-180°$ at the unity gain frequency, ω_{UGF}. ω_{UGF} is defined as the frequency at which the gain crosses 0 dB. Mathematically, the phase margin is described as $PM = 180 + \angle A\beta(j\omega_{UGF})$ where $\angle A\beta(j\omega_{UGF})$ is the angle of the loop gain at the unity gain frequency. With 0° or less of phase margin, the system is unstable with regenerative positive feedback. While systems with greater than 0° of phase margin do not exhibit regenerative positive feedback, there are time-domain considerations such as overshoot and settling behavior. Figure 3.4 shows the behavior of multiple systems with varying phase margin using the MATLAB model in Section A.2. This figure shows that with more PM, the system does not overshoot or ring as much. It is necessary to point out that, in order to evaluate PM, the loop gain transfer function must contain at least one pole in order for the gain to cross 0 dB. To model systems with phase margins below 90°, the system needs to have at least two poles. Finally, unstable negative feedback systems with regenerative positive feedback require three or more poles for the phase to cross $-180°$.

Gain margin, the other common stability metric, is 0 dB minus the amount of gain when the phase of the loop gain is $-180°$. The frequency at which this occurs is ω_{INV}, meaning the gain margin of the loop gain is $GM = -A\beta(j\omega_{INV})$. In order to evaluate GM, the loop gain transfer function must contain at least three poles for the gain to cross $-180°$ – a two pole system's phase will approach $-180°$ but not cross it.

3.1.1.3 Positive Feedback and Phase Margin

Equation (3.5) limits β with respect to A_{DC} to achieve a stable and improved gain positive feedback system. This constraint can be manipulated to define limits on the loop gain, specifically $0 < LG < 1$. This limit means that the loop gain of a stable positive feedback system will never cross 0 dB, leaving PM undefined. However, this fact is not problematic in that the LG range also prevents regenerative positive feedback from ever occurring. The signal fed back into the summation node is defined to always be less than one. Therefore, PM itself is not a measure of stability in positive feedback systems. Instead the requirement of LHP poles is the sole consideration for stabilization.

Although the system may be stable under the LHP pole criterion, it is still important to understand how positive feedback moves the poles of the open-loop amplifier. This is specifically important in the case that the positive feedback amplifier is used in a larger negative feedback system as has been proposed in [60]. To observe the effects on the pole locations, a two-pole system can be inserted into (3.1) for the forward amplifier

$$A(s) = \frac{A_{DC}}{(1+s/p_1)(1+s/p_2)} \tag{3.7}$$

where p_1 is the dominant pole and p_2 is a secondary higher frequency pole. This amplifier model gives a closed-loop transfer function for frequency-independent β as

$$H(s) = \frac{A_{DC}p_1p_2}{s^2+s(p_1+p_2)+p_1p_2(1-A_{DC}\beta)}. \tag{3.8}$$

The poles of this new transfer function are located at

$$p_{1H} = \frac{p_1+p_2-\sqrt{(p_2-p_1)^2+4p_1p_2A_{DC}\beta}}{2} \tag{3.9}$$

and

$$p_{2H} = \frac{p_1+p_2+\sqrt{(p_2-p_1)^2+4p_1p_2A_{DC}\beta}}{2}. \tag{3.10}$$

Typical amplifier stabilization technique involves spreading the two poles p_1 and p_2 far enough apart such that the gain crosses 0 dB before p_2 has reduced the phase significantly and degraded the phase margin. In this sense, an amplifier with large separation between p_1 and p_2 is considered a stable amplifier. If we observe the pole spread of the original amplifier $\Delta p = p_2 - p_1$ and compare it to the spread of the positive feedback amplifier using (3.9) and (3.10),

$$\Delta p_H = \sqrt{(p_2 - p_1)^2 + 4p_1p_2A_{DC}\beta} = \sqrt{\Delta p^2 + 4p_1p_2A_{DC}\beta} \tag{3.11}$$

it is simple to show that the positive feedback always has more pole spread than the stand-alone amplifier for $A_{DC}\beta > 0$. Evaluating (3.11) as a Pythagorean equation [77], we see that $\Delta p_H^2 = \Delta p^2 + 4p_1p_2A_{DC}\beta$ and can conclude that Δp_H will always be larger than Δp.

3.1.2 Ideal Operational Amplifier Analysis

The ideal opamp analysis that was performed for negative feedback can be repeated for positive feedback using the schematic in Figure 3.6. Using nodal analysis and assuming an opamp transfer function $A(s)$, the closed-loop transfer function is

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{\mathrm{A(s)}\frac{R_2}{R_1+R_2}}{1-\mathrm{A(s)}\frac{R_1}{R_1+R_2}} = \frac{A_f}{1-A_f\beta_f} \tag{3.12}$$

where the closed-loop forward gain is

$$A_f = A(s)\frac{R_2}{R_1+R_2} \tag{3.13}$$

and the feedback factor is $\beta_f = R_1/R_2$. This result differs from the ideal block level analysis in (3.1) in that the closed-loop forward gain is degraded by the resistive divider factor $R_2/(R_1 + R_2)$. Using the single pole model of (2.3), (3.12) becomes

$$H(s) = \frac{A_{DC}\frac{R_2}{R_1+R_2}p_1}{s+p_1\left(1-A_{DC}\frac{R_1}{R_1+R_2}\right)} = \frac{A_{DCf}p_1}{s+p_1(1-A_{DCf}\beta_f)} \tag{3.14}$$

where

$$A_{DCf} = A_{DC}\frac{R_2}{R_1+R_2}. \tag{3.15}$$

This system has a DC gain of

$$H_{DC} = \frac{A_{DCf}}{1-A_{DCf}\beta_f} \tag{3.16}$$

and a -3 dB bandwidth of

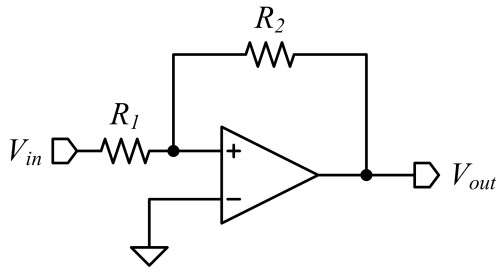

Figure 3.6 Positive feedback system with ideal opamp having zero output impedance, infinite input impedance, and voltage transfer function $A(s)$.

$$p_{1H} = p_1(1 - A_{DCf}\beta_f). \tag{3.17}$$

Applying the positive feedback stability criteria of (3.6) to this system, it can be shown that the feedback factor must adhere to

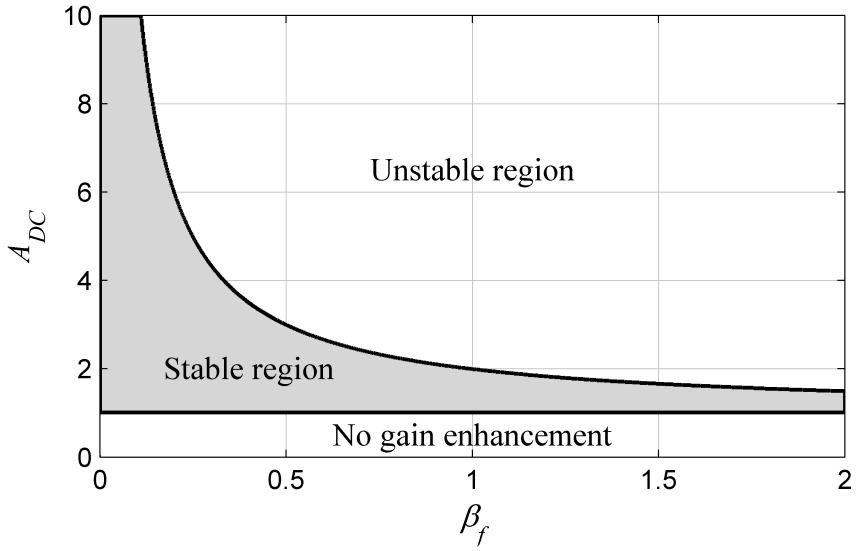

Figure 3.7 Valid A_{DC} and β_f ranges for a positive feedback system with an ideal opamp with DC gain A_{DC}.

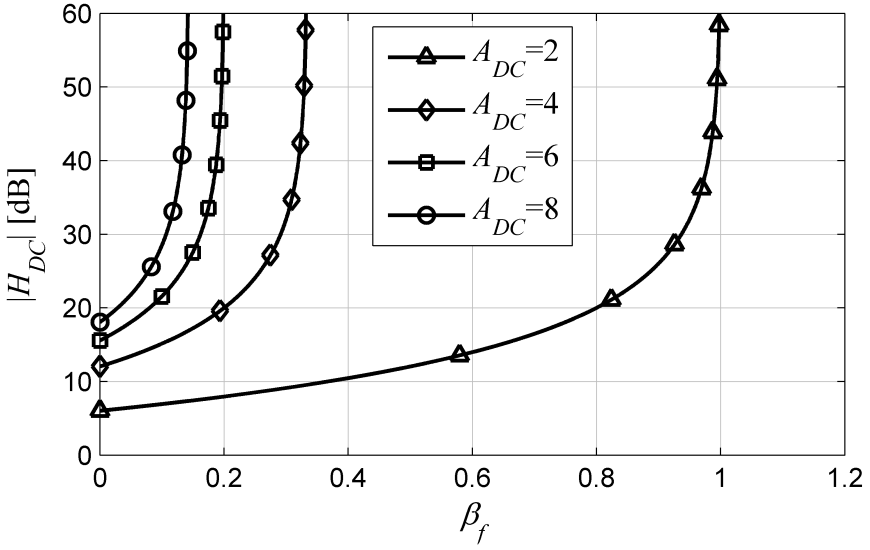

Figure 3.8 DC gain, H_{DC}, of positive feedback systems with ideal opamp of various A_{DC} values versus β_f

$$\beta_f < \frac{1}{A_{DC}-1} \tag{3.18}$$

for stability. For improved gain the open amplifier gain must have DC gain

$$A_{DC} > 1. \tag{3.19}$$

Figure 3.7 illustrates this relationship by highlighting the valid ranges for A_{DC} and β_f. Figure 3.8 shows the gain improvements across β_f for various V_{DC} values. If (3.18) and (3.19) are met, the resulting positive feedback system will be stable with improved gain over the open-loop amplifier $A(s)$.

3.1.2.1 Input and Output Impedance

The application of positive feedback also modifies the impedances of the ideal opamp. As was the case with the negative feedback opamp, the output node of the opamp is still connected to the output of the amplifier and therefore its source and sink capabilities remain the same. This means that the output impedance remains ideal as $Z_{out} = 0$.

The input impedance, however, is modified because the input to the positive feedback amplifier is no longer the opamp itself, but instead the resistive network that forms the feedback network. Calculating the input impedance change due to positive feedback gives the result

$$Z_{in}(\mathrm{s}) = \mathrm{R}_1 \frac{1-A_f\beta_f}{1-A_f\beta_f-\frac{1}{1+\beta_f}} = \frac{R_1\left(1-A(s)\right)+R_2}{1-A(s)}. \tag{3.20}$$

Figure 3.9 shows this relationship for various A_{DC} values. While the high A_{DC} behavior is similar to that of negative feedback where Z_{in} approaches R_1, a premise of this work is that A_{DC} will not be high. Under the conditions of low A_{DC}, the behavior of the input impedance is in contrast to that of negative feedback. For positive feedback the input impedance is lower than its high A_{DC} value, implying that the input impedance is further degraded from the ideal case.

Additionally, (3.20) implies that Z_{in} could become a negative number. The point at which this occurs is identical to the stability conditions placed on β_f in (3.18) or stated in the context of Figure 3.9, A_{DC} must meet the criterion

$$A_{DC} < \frac{1}{\beta_f} + 1. \tag{3.21}$$

3.1.2.2 Positive Feedback with Input-Referred Offset

Figure 3.10 shows a positive feedback opamp with input-referred offset V_{os}. As stated

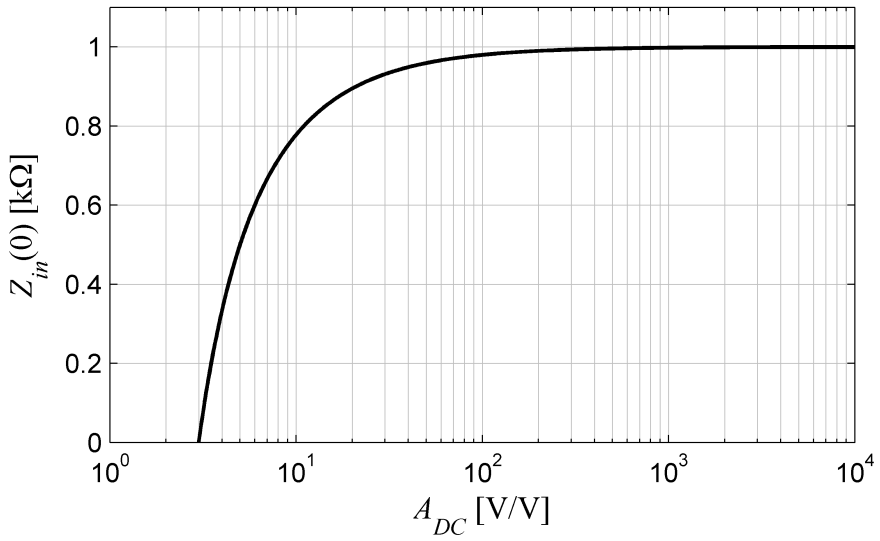

Figure 3.9 DC input impedance for positive feedback system with ideal opamp with $R_1 = 1$ kΩ, and $R_2 = 2$ kΩ.

previously, input-referred offset is an unavoidable consequence of device mismatch in the fabrication process. While this value can be minimized with good design practices and circuit topologies, it cannot be eliminated altogether. The opamp offset transfer function can be calculated as

$$H_{DCos} = \frac{V_{out}}{V_{os}} = \frac{A_{DC}}{1-A_{DC}\frac{R_1}{R_1+R_2}} = \frac{A_{DCf}(1+\beta_f)}{1-A_{DCf}\beta_f}. \tag{3.22}$$

This can be referred back to the input by dividing V_{out} by the closed-loop gain, $H(s)$, giving an input-referred offset of

$$V_{os,in} = \frac{H_{DCos}}{H_{\mathrm{DC}}}V_{os} = (1+\beta_f)V_{os}. \tag{3.23}$$

As was the case with negative feedback, β_f is a positive quantity and therefore input-referred offset is increased by the application of positive feedback. Unlike negative feedback, however, under certain A_{DC} conditions, β_f can be greater than one as shown in Figure 3.7. This creates the potential for larger increases in input-referred offset than a negative feedback system would likely experience. This fact must be taken into consideration when positive feedback is applied to amplifiers with very low A_{DC} values.

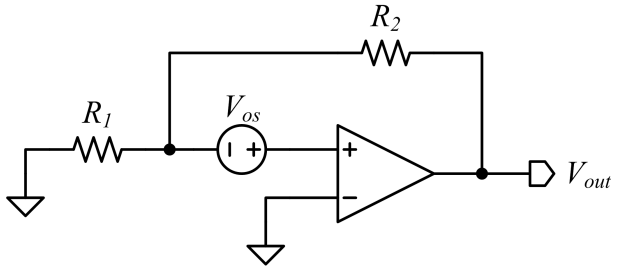

Figure 3.10 Positive feedback system with an ideal opamp having DC offset, V_{os}.

3.1.2.3 Positive Feedback with Input-Referred Noise

The effects of noise on the positive feedback opamp model can be evaluated through analysis of Figure 3.11. Superposition is used to calculate each noise source's effect on the output voltage. The contribution of baseline amplifier's input-referred noise, e_a, is

$$V_{out,ea} = e_a \frac{A_f(1+\beta_f)}{1-A_f\beta_f}. \tag{3.24}$$

The thermal noise contributions from R_1 and R_2 to the output voltage are calculated as

$$V_{out,e1} = e_1 \frac{A_f}{1-A_f\beta_f} \tag{3.25}$$

and

$$V_{out,e2} = e_2 \frac{A_f\beta_f}{1-A_f\beta_f}. \tag{3.26}$$

Summing the noise contributors' power together gives the following total noise power at the output node of

$$V_{out}^2 = e_a^2 \left[\frac{A_f(1+\beta_f)}{1-A_f\beta_f}\right]^2 + e_1^2 \left[\frac{A_f}{1-A_f\beta_f}\right]^2 + e_2^2 \left[\frac{A_f\beta_f}{1-A_f\beta_f}\right]^2. \tag{3.27}$$

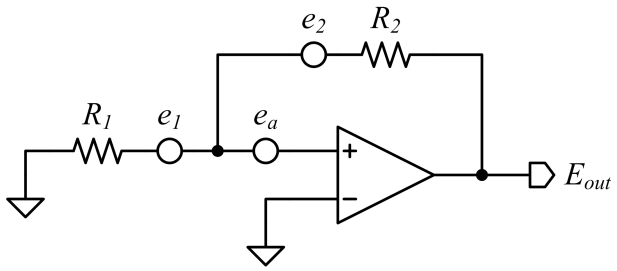

Figure 3.11 Positive feedback system for noise analysis with noise sources of input-referred opamp noise, e_a, and thermal noise for R_1 and R_2, e_1 and e_2.

This value is referred back to the input of the amplifier by dividing V_{out}^2 by the closed-loop gain of the amplifier

$$E_{in}^2 = V_{out}^2 \left[\frac{1-A_f\beta_f}{A_f}\right]^2 \tag{3.28}$$

giving

$$E_{in}^2 = e_a^2\left(1+\beta_f\right)^2 + e_1^2 + e_2^2\beta_f^2. \tag{3.29}$$

e_1 and e_2 are known to be thermal noise contributions so the total input-referred noise can be further elaborated as

$$E_{in}^2 = e_a^2\left(1+\beta_f\right)^2 + 4kT\Delta f R_1\left(1+\beta_f\right). \tag{3.30}$$

This result is identical to the negative feedback feedback result, indicating that positive feedback does not alter input-referred noise in a fundamentally different way than negative feedback. However, because the value of β_f can become greater than one under some A_{DC} values, care must be taken to avoid unnecessary increases in input-referred noise.

3.1.2.4 Positive Feedback Gain-Bandwidth Product

The gain-bandwidth product can be calculated from (3.16) and (3.17), yielding

$$GBP = \frac{R_2}{R_1+R_2} A_{DC} p_1. \tag{3.31}$$

Comparing this to the open-loop amplifier gain-bandwidth product of $A_{DC}p_1$, the gain-bandwidth product ratio can be calculated as

$$GBP_r = \frac{R_2}{R_1+R_2} = \frac{1}{1+\beta_f}. \quad (3.32)$$

This expression is identical to that of the negative feedback result, indicating that positive feedback does not alter the gain-bandwidth product in a fundamentally different way than negative feedback. Figure 3.12 shows this GBP_r degradation for a range of β_f values. As is the case with other previous analysis, the extended range of β_f for amplifiers with low A_{DC} can cause gain-bandwidth product degradation beyond negative feedback trends and should be account for in baseline amplifier and positive feedback amplifier design.

3.1.3 Voltage Amplifier Model Analysis

Applying the concepts of the previous analyses to an amplifier model with non-idealities and a realistic feedback network allows us to take the analysis a step further. Figure 3.13 shows such a model with finite input impedance, R_{in}, non-zero output impedance, R_{out}, and a feedback network formed by R_1 and R_2. The output of this model is the voltage

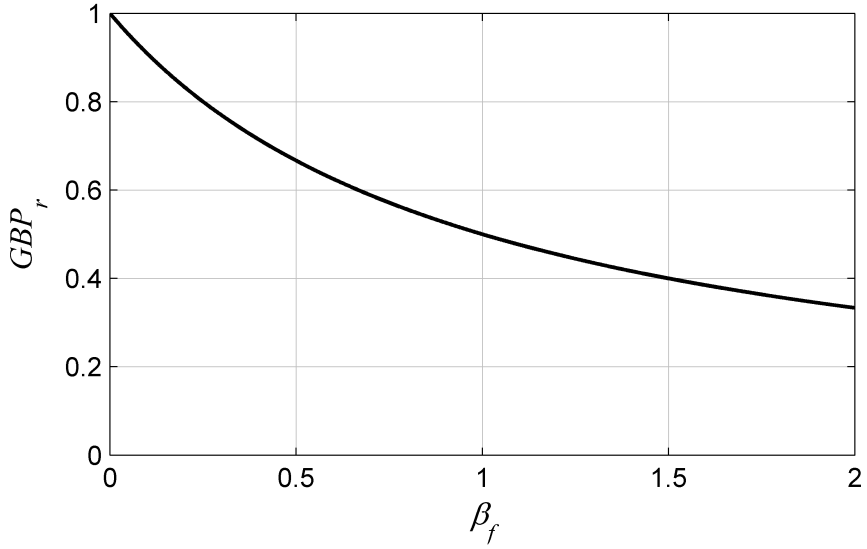

Figure 3.12 Gain-bandwidth product ratio, GBP_r, for a positive feedback system with an ideal opamp.

seen at the input terminals, V_x, multiplied by the amplifier's gain transfer function, $A(s)$, through the resistance R_{out}. As R_{in}, R_{out}, and $A(s)$ are functions of the baseline amplifier, R_1 and R_2 are the design handles to be adjusted to optimize amplifier performance.

Nodal analysis of this model shows the resulting transfer function to be

$$H(s) = \frac{\frac{G_1}{G_1+G_2+G_{in}} \times \frac{G_2+A(s)G_{out}}{G_2+G_{out}}}{1-\frac{G_2}{G_1+G_2+G_{in}} \times \frac{G_2+A(s)G_{out}}{G_2+G_{out}}} \tag{3.33}$$

where G_{in}, G_{out}, G_1 and G_2 are the conductances of R_{in}, R_{out}, R_1 and R_2, respectively. In traditional feedback form, Equation (3.33) can be written as

$$H(s) = \frac{A_f(s)}{1-A_f(s)\beta_f} \tag{3.34}$$

where

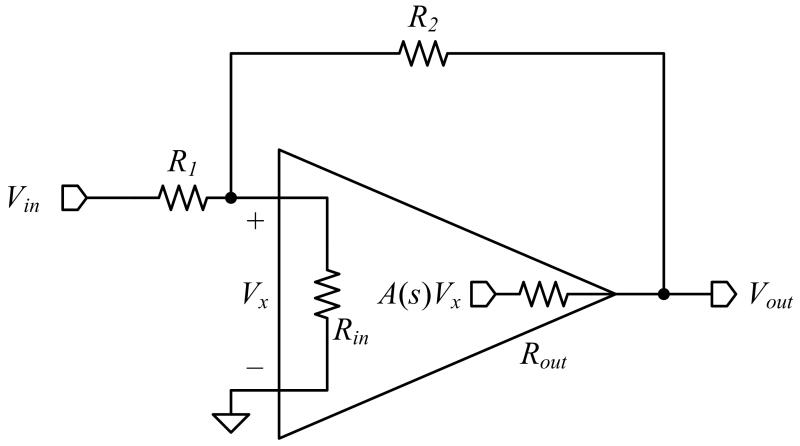

Figure 3.13 Voltage amplifier model having finite input impedance, non-zero output impedance, and voltage transfer function $A(s)$.

$$A_f(s) = \frac{G_1}{(G_1+G_2+G_{in})} \frac{G_2+A(s)G_{out}}{(G_2+G_{out})} \tag{3.35}$$

and $\beta_f = G_2/G_1$.

Applying a single pole model of $A(s)$ to Equation (3.33) with a DC gain of A_{DC} and -3 dB bandwidth of p_1, results in $H(s)$

$$H(s) = \frac{G_1 G_2}{(G_1+G_2+G_{in})(G_2+G_{out})-G_2^2} \frac{s+p_1\left(1+\frac{A_{DC}G_{out}}{G_2}\right)}{s+p_1\frac{(G_1+G_2+G_{in})(G_2+G_{out})-G_2^2-A_{DC}G_2G_{out}}{(G_1+G_2+G_{in})(G_2+G_{out})-G_2^2}} \tag{3.36}$$

with a DC gain of

$$H_{DC} = \frac{G_1(G_2+A_{DC}G_{out})}{(G_1+G_2+G_{in})(G_2+G_{out})-G_2^2-A_{DC}G_2G_{out}} \equiv \frac{\Phi}{\Psi} \tag{3.37}$$

and -3 dB bandwidth of

$$p_{1H} = p_1 \cdot \frac{\Psi}{\Psi+A_{DC}G_2G_{out}} \tag{3.38}$$

where Φ and Ψ have been defined as the numerator and denominator, respectively, of (3.37) for convenience.

The analysis here involves finding a range of R_2 values which provide an increase in gain but does not produce a RHP pole. The boundary value of R_2 which creates the RHP pole is also the value of R_2 which causes the denominator of (3.37) to go to zero, causing the closed-loop gain to approach infinity. The solutions to these conditions produce the following valid R_2 range

$$R_2 > -\frac{G_1+G_{in}+G_{out}(1-A_{DC})}{G_{out}(G_1+G_{in})} \tag{3.39}$$

and

$$R_2 < \frac{G_1(1-A_{DC})-G_{in}A_{DC}-G_{out}(1-A_{DC})A_{DC}}{A_{DC}G_{in}G_{out}} \tag{3.40}$$

Equation (3.39) and (3.40) show the valid feedback resistance range based on stability and increased gain. Equation (3.39), however, suggests there might be a minimum required gain such that the lower bound of the R_2 range remains positive. Under this condition, the open-loop gain must be at least

$$A_{DC} > 1 + \frac{G_1+G_{in}}{G_{out}} \approx 1 + \frac{R_{out}}{R_1} \tag{3.41}$$

The approximation in (3.41) is based on the input impedance being much larger than R_1 and R_{out} – a reasonable expectation for MOSFET-based input stages. An additional constraint can be placed on A_{DC} such that (3.36) does not have a RHP pole:

$$A_{DC} < 1 + (R_2 + R_{out}) \cdot (G_1 + G_{in}) \approx \frac{R_2+R_{out}}{R_1} \tag{3.42}$$

Equations (3.39) and (3.40) help place limits on the designer for R_2 values given an open-loop gain or feedback factor. Equations (3.41) and (3.42) help define limits for the open-loop amplifier design. The combination of these four equations allows the designer to implement positive feedback loops with this generic architecture. Figure 3.14 shows the magnitude of H_{DC} as a function of R_2 and R_1. The vertical asymptote at which H_{DC} approaches infinity corresponds to the R_2 boundary described by Equation (3.39). This R_2 value is the point below which the system becomes unstable.

3.1.3.1 Input and Output Impedance

As is the case with negative feedback, applying positive feedback causes a change in the amplifier's input impedance. The input impedance can be described as

$$Z_{in}(s) = \left[G_1\left(1 - \frac{G_1(G_2+G_{out})}{(G_1+G_2+G_{in})(G_2+G_{out})-G_2(G_2+A(s)G_{out})}\right)\right]^{-1} \tag{3.43}$$

A design adhering to the stability conditions proposed in the previous sections leads to an amplifier with decreased input impedance. Interestingly, this quantity can become negative under certain gain and impedance conditions. This should be an important consideration in the design process.

The output impedance of the closed-loop amplifier is also changed by the application of positive feedback. The resulting output impedance of the amplifier can be shown as

$$Z_{out}(s) = \frac{G_1+G_2+G_{in}}{(G_1+G_2+G_{in})(G_2+G_{out})-G_2(G_2+A(s)G_{out})} \tag{3.44}$$

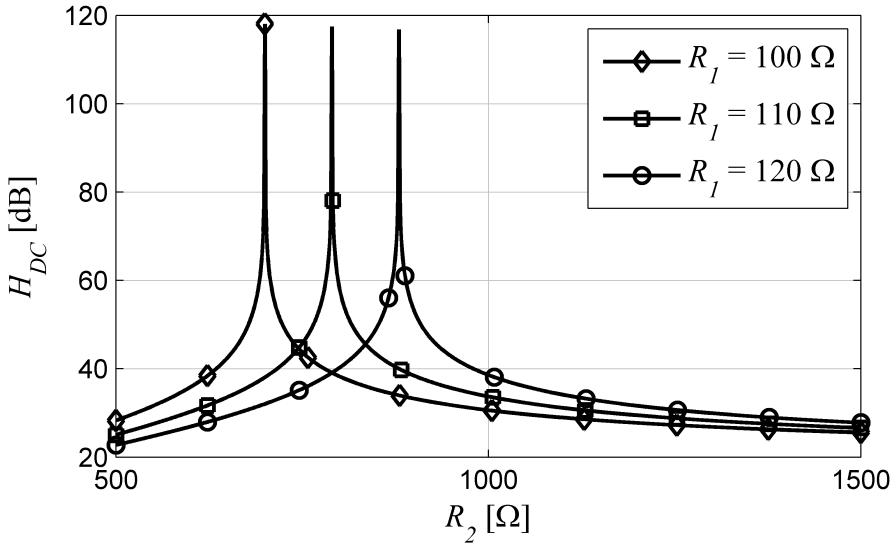

Figure 3.14 Magnitude of H_{DC} versus R_2 for various R_1 values with $A_{DC} = 10$, $R_{in} = 10$ MΩ, and $R_{out} = 200$ Ω.

Applying the stability conditions of this work, positive feedback works to increase the output impedance of the amplifier. These results are in contrast with negative feedback.

3.1.3.2 Positive Feedback with Input-Referred Offset

The input-referred offset of the voltage amplifier model, V_{os}, can be referred back to the input using the schematic in Figure 3.15. The offset transfer function can be calculated as

$$H_{os}(s) = \frac{V_{out}}{V_{os}} = \frac{A_f(1+\beta_f) - \frac{G_2}{G_2+G_{out}}}{1-A_f\beta_f} \tag{3.45}$$

and V_{os} can be referred back to the input through the closed-loop transfer function

$$V_{os,in} = \frac{H_{os}(s)}{H(s)} V_{os} = \left[\left(1+\beta_f\right) - \frac{1}{A_f}\frac{G_2}{G_2+G_{out}}\right] V_{os}. \tag{3.46}$$

This expression is similar to that of the opamp model in (3.23) with the additional factor of $G_2 \,/\, \left[A_f(G_2 + G_{out})\right]$. This factor will almost certainly be less than one and greater than zero. This implies that the input-referred offset change will be reduced from that of the opamp model. This in confirmed with analysis shown in Figure 3.16 which shows the

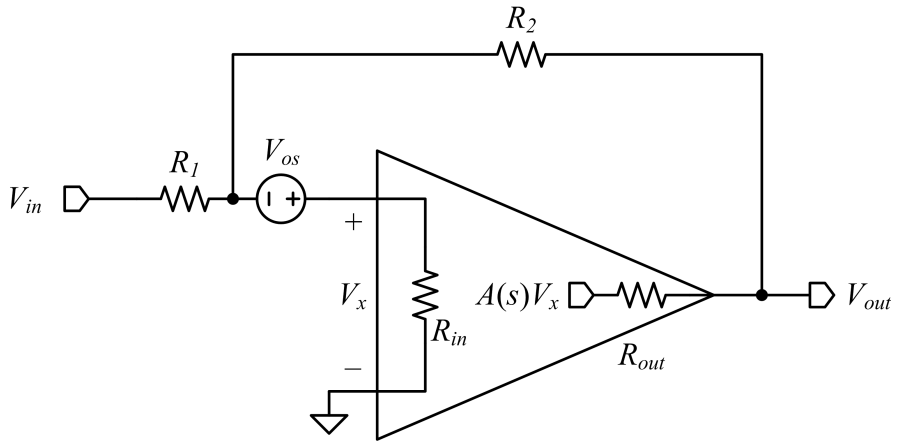

Figure 3.15 Voltage amplifier model with input-referred offset, V_{os}.

offset ratio $V_{os,in}/V_{os}$ over the valid range of β_f values. While only marginally so, the voltage amp model gives a smaller ratio, implying that the input-referred offset is not increased as much as in the opamp model case.

3.1.3.3 Positive Feedback with Input-Referred Noise

The input-referred noise analysis for this model is performed in a similar fashion as that of the previous positive feedback and negative feedback models. Figure 3.17 shows the voltage amp model with noise sources from the resistive feedback, e_1 and e_2, and the input-referred noise of the amplifier, e_a. Using superposition to calculate each source's effect on the total output noise voltage, the amplifier noise contributes

$$\frac{V_{out}}{e_a} = \frac{A_f(1+\beta_f) - \frac{G_2}{G_2+G_{out}}}{1-A_f\beta_f} \tag{3.47}$$

the resistor R_1 contributes

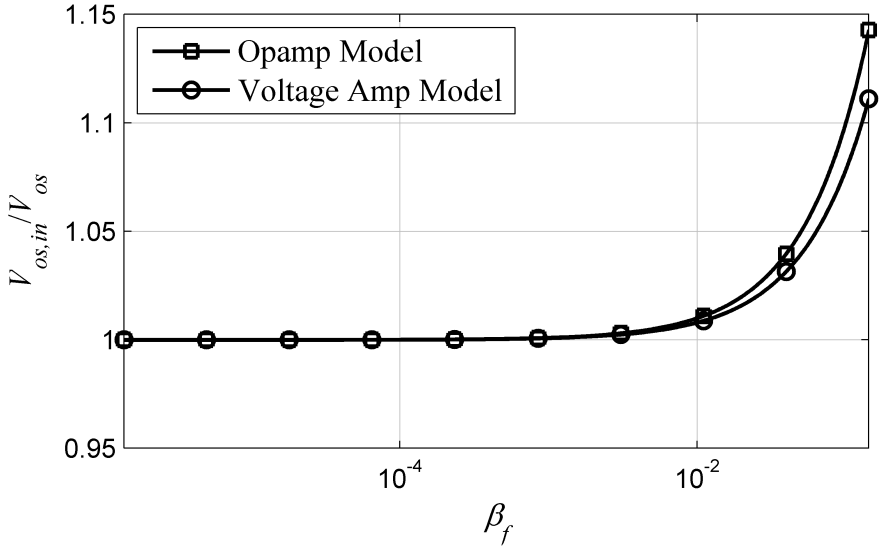

Figure 3.16 Offset ratio comparison of opamp model and voltage amp model with $A_{DC} = 10$, $R_{in} = 10$ MΩ, $R_{out} = 200$ Ω, $R_1 = 100$ Ω, and R_2 varying with β_f.

$$\frac{V_{out}}{e_1} = -\frac{A_f}{1-A_f\beta_f} \tag{3.48}$$

and the resistor R_2 contributes

$$\frac{V_{out}}{e_2} = -\frac{A_f\beta_f - \frac{G_2}{G_2+G_{out}}}{1-A_f\beta_f}. \tag{3.49}$$

The total output noise power can be calculated by summing the squares of each of these contributors, giving

$$V_{out}^2 = e_a^2\left[\frac{A_f(1+\beta_f)-\frac{G_2}{G_2+G_{out}}}{1-A_f\beta_f}\right]^2 + e_1^2\left[\frac{A_f}{1-A_f\beta_f}\right]^2 + e_2^2\left[\frac{A_f\beta_f-\frac{G_2}{G_2+G_{out}}}{1-A_f\beta_f}\right]^2. \tag{3.50}$$

Transposing this noise power back to the input gives

$$E_{in}^2 = e_a^2\left[\left(1+\beta_f\right) - \frac{1}{A_f}\frac{G_2}{G_2+G_{out}}\right]^2 + e_1^2 + e_2^2\left[\beta_f - \frac{1}{A_f}\frac{G_2}{G_2+G_{out}}\right]^2. \tag{3.51}$$

Substituting the known resistive noise of e_1 and e_2, the final noise expression is

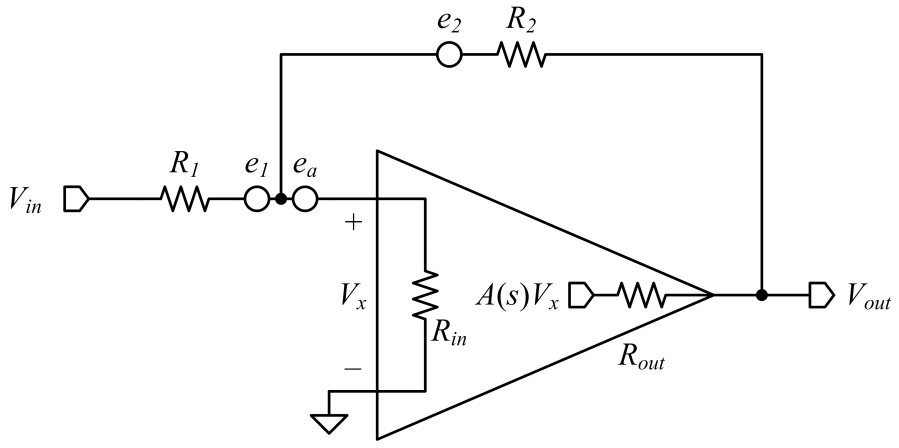

Figure 3.17 Voltage amplifier model with input-referred noise, e_a, and resistive thermal noise from R_1 and R_2, e_1 and e_2.

$$E_{in}^2 = \begin{matrix} e_a^2\left[\left(1+\beta_f\right)-\frac{1}{A_f}\frac{G_2}{G_2+G_{out}}\right]^2 + 4kT\Delta f R_1 \\ +4kT\Delta f R_2\left[\beta_f - \frac{1}{A_f}\frac{G_2}{G_2+G_{out}}\right]^2 \end{matrix} . \quad (3.52)$$

As expected from previous analysis the contributions from R_1 and R_2 are new, but the amplifier noise is shaped. In fact, this noise is shaped in an identical fashion to the DC input-referred offset. In this previous section it was shown that this noise, while increased from that of the baseline amplifier, is increased less than was the case of the ideal opamp model.

3.1.3.4 Positive Feedback Gain-Bandwidth Product

Ideal analysis of a positive feedback structure shows the gain-bandwidth product remains constant after applying feedback. With the non-ideal impedances in place, however, this does not remain true. The relationship between the two can be shown as

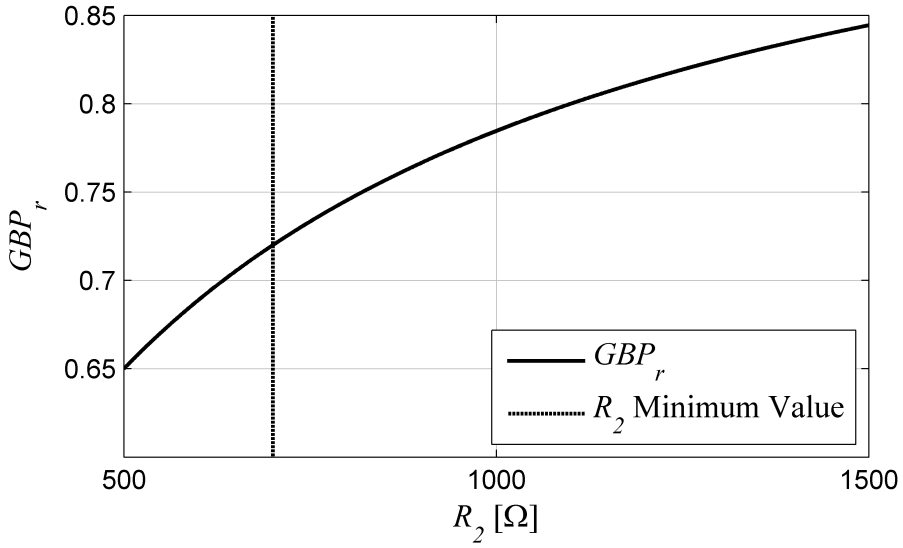

Figure 3.18 GBP_r versus R_2 over valid feedback resistance range of the voltage amplifier model with $A_{DC} = 10$, $R_{in} = 10$ MΩ, $R_{out} = 200$ Ω, and $R_1 = 100$ Ω.

$$GBP_r = \frac{GBP_{CL}}{GBP_{OL}} = \frac{\Phi}{A_{DC}[\Psi + A_{DC}G_2G_{out}]} \tag{3.53}$$

where GBP_r is the gain-bandwidth product ratio, GBP_{CL} is the gain-bandwidth product of the closed-loop amplifier and GBP_{OL} is the gain-bandwidth product of the open-loop amplifier. Ideally, this ratio would be 1, but due to the non-ideal amplifier impedances it is less than 1. However, Figure 3.18 shows that using a larger value for R_2 provides a higher GBP_r. This is in contrast to the gain analysis as lower R_2 provides a greater increase in closed-loop gain.

3.1.4 Differential Amplifier Analysis

The final level of analysis of the positive feedback structure is performed on an actual circuit. The differential amplifier with positive feedback is shown in Figure 3.19. The small-signal model for analysis is shown in Figure 3.20. Performing nodal analysis on

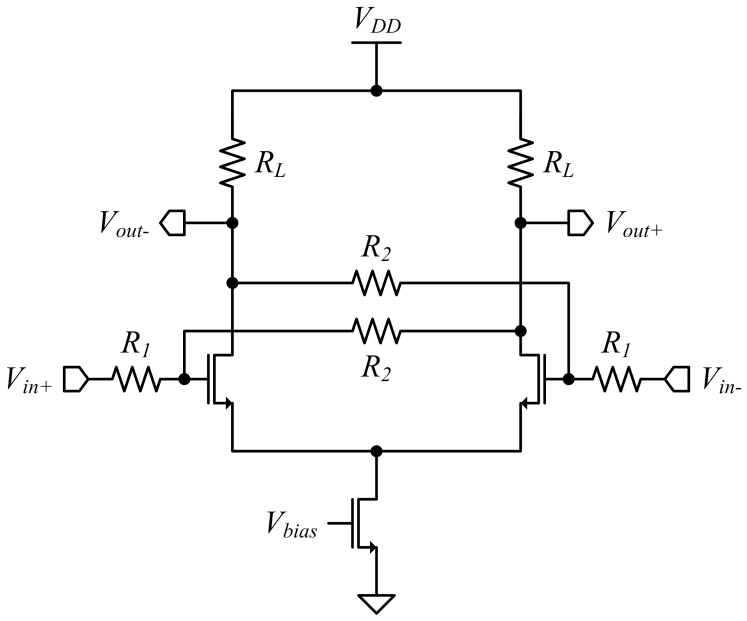

Figure 3.19 Differential amplifier with positive feedback implemented with the resistive network consisting of R_1 and R_2 resistors.

this small-signal circuit yields the DC transfer function

$$H_{\mathrm{DC}} = \frac{V_{out}}{V_{in}} = \frac{\frac{R_2}{R_2+R_L}\cdot\frac{R_2}{R_1+R_2}\left(g_m R_L+\frac{R_L}{R_2}\right)}{1-\frac{R_2}{R_2+R_L}\cdot\frac{R_1}{R_1+R_2}\left(g_m R_L+\frac{R_L}{R_2}\right)} = \frac{A_{DCf}}{1-A_{DCf}\beta_{DCf}} \tag{3.54}$$

where the closed-loop forward gain is

$$A_{DCf} = \frac{R_2}{R_2+R_L}\cdot\frac{R_2}{R_1+R_2}\left(g_m R_L+\frac{R_L}{R_2}\right) \tag{3.55}$$

and the feedback factor is $\beta_{DCf} = R_1/R_2$. Applying the stability criteria of (3.6) to (3.54), the feedback factor must exceed a threshold,

$$\beta_{DCf} > \frac{1}{A_{DCf}} - \frac{1}{g_m R_L}. \tag{3.56}$$

Applying the A_{DCf} and β_{DCf} expressions, then

$$R_1 > \frac{1}{g_m}. \tag{3.57}$$

The analysis of (3.56) makes an additional assumption that A_{DCf} is a positive number. To ensure this case, there is a minimum value placed on R_2,

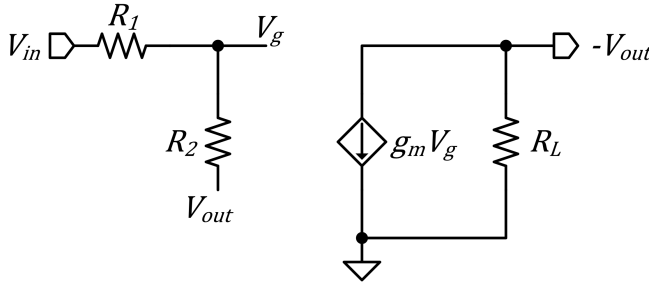

Figure 3.20 Differential amplifier positive feedback system small-signal model under the virtual ground approximation used previously.

$$R_2 > R_1(g_m R_L - 1) - R_L. \tag{3.58}$$

Figure 3.21 shows H_{DC} compared to $g_m R_L$ for various R_2 values within the range defined in this section.

3.1.4.1 Input and Output Impedance

The input of the differential amplifier drives a MOSFET directly. The input impedance of a MOSFET is generally capacitive in nature. Figure 3.22 shows a small-signal model of the half-circuit differential amplifier with gate-to-drain capacitance C_{gd}. The gate-to-source capacitance, C_{gs}, will also contribute, but for reasons discussed below, C_{gd} is the dominant capacitance affecting input impedance. Calculating the input impedance of this structure gives

$$Z_{in}(s) = \frac{sR_L C_{gd}+1}{sC_{gd}(1+g_m R_L)}. \tag{3.59}$$

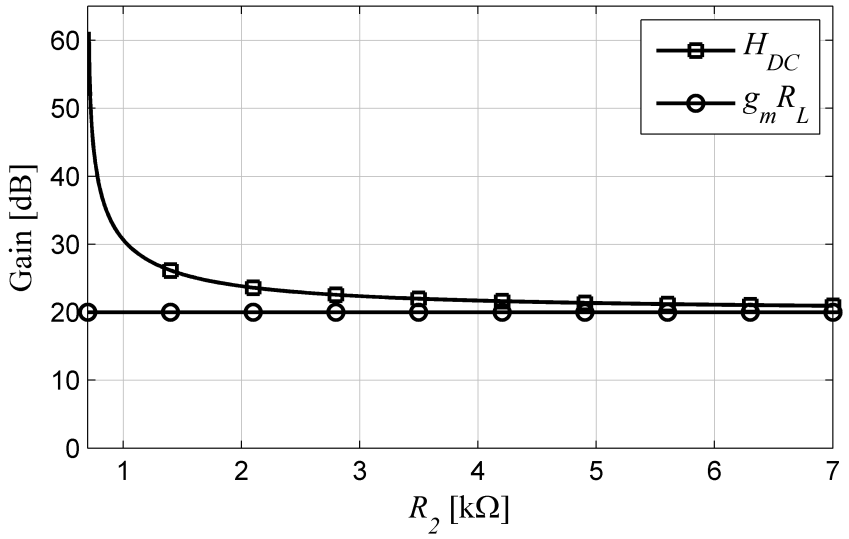

Figure 3.21 R_2 sweep of positive feedback differential amplifier with $g_m = 50$ mS, $R_L = 200\ \Omega$, $R_1 = 100\ \Omega$, across valid R_2 values.

At low frequencies, this appears to be capacitive, but at high frequencies when C_{gd} looks like a low impedance, the input impedance looks resistive. Assuming this transition occurs at high frequencies beyond those of interest, the input impedance can be simplified as being purely capacitive,

$$Z_{in}(s) \approx \frac{1}{sC_{gd}(1+g_m R_L)} = \frac{1}{sC_{gd}(1+A_{DC})}. \tag{3.60}$$

This expression also illustrates the well-known Miller effect where the input capacitance is multiplied by one plus the DC gain of the amplifier. This causes this apparent capacitance to be larger by a factor of $1 + g_m R_L$. This is the reason that C_{gd} dominates the input impedance, and C_{gs} does not.

The output impedance of this structure can also be calculated from Figure 3.22 as

$$Z_{out}(s) = \frac{R_L}{sR_L C_{gd}+1}. \tag{3.61}$$

In this case, the Miller effect does not affect the magnitude of the capacitance as there is simply a pole at $1/R_L C_{gd}$ at which the output impedance begins to roll off.

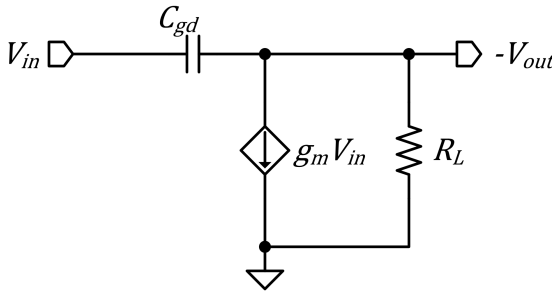

Figure 3.22 Differential amplifier small-signal model under virtual ground approximation with gate-to-drain capacitance modeled.

In modern technologies, gate leakage is a significant component to the input impedance of a MOSFET. This means that at low frequencies the input impedance looks resistive as in [2], Figure 3.23, and Figure 3.24. Extensive work has been performed to model this gate leakage [78], [79] and it has been included in the BSIM 4 [27] - [29] models used for the SPICE simulations. For further detail, SPICE simulations are discussed in Section 4.1 and the actual behavior of the devices is investigated.

Assuming infinite MOSFET input impedance, the positive feedback input impedance can

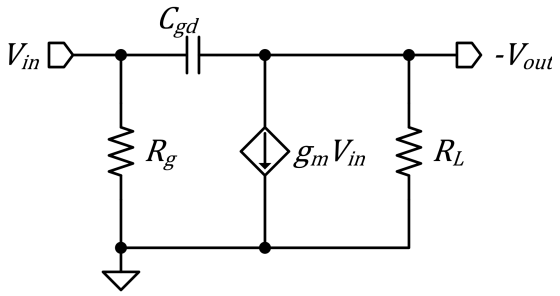

Figure 3.23 Differential amplifier small-signal model under virtual ground approximation with gate-to-drain capacitance and gate current modeled.

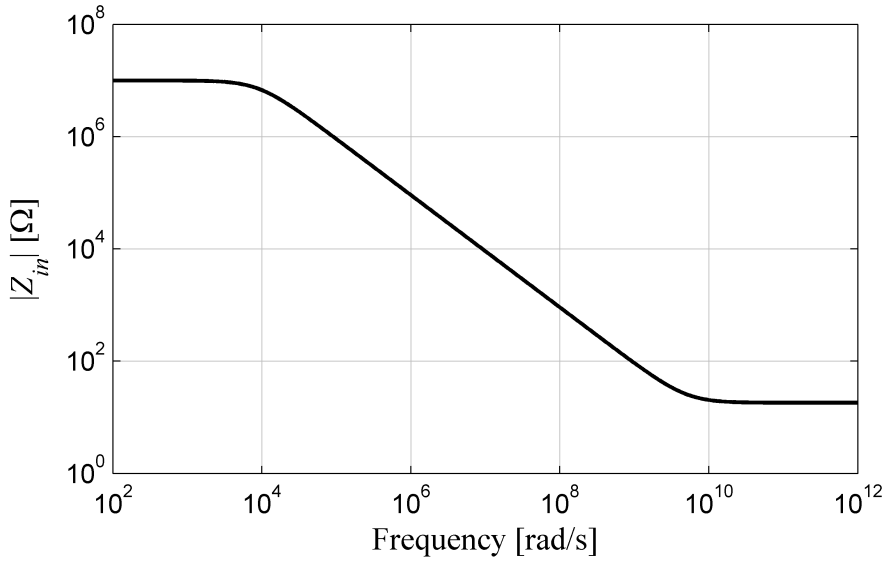

Figure 3.24 Differential amplifier input impedance with gate-to-drain capacitance and gate current, $g_m = 50$ mS, $R_L = 200$ Ω, $R_g = 10$ MΩ, $C_{gd} = 1$ pF.

be calculated using Figure 3.20 as

$$Z_{in} = R_1 \frac{1-\mathrm{A_{DCf}}\beta_{DCf}-\frac{1}{1+\beta_{DCf}}}{1-\mathrm{A_{DCf}}\beta_{DCf}} = \frac{R_1(g_m R_L-1)}{(g_m R_L-1)-\frac{R_2}{R_1}-\frac{R_L}{R_1}} \tag{3.62}$$

and an output impedance of

$$Z_{out} = R_L \frac{\frac{R_2}{R_2+R_L}}{1-A_{DCf}\beta_{DCf}} = R_L \frac{R_1+R_2}{R_1(g_m R_L-1)-R_2-R_L}. \tag{3.63}$$

To prevent the output impedance from becoming negative, a limit is defined for R_2 of

$$R_2 < R_1(g_m R_L - 1) - R_L. \tag{3.64}$$

Under this condition, the denominator of the Z_{in} expression will always be positive. Therefore to ensure a non-negative Z_{in}, the numerator must always be greater than zero. This places a limitation on the open-loop gain of the baseline amplifier such that

$$g_m R_L > 1. \tag{3.65}$$

These conditions, specifically (3.64), are in contrast with the stability requirements defined by (3.58). Previous analysis has shown that negative impedances correlate with unstable systems; however, in the case of the differential amplifier, the implication of negative input and output impedances do not correspond to unstable systems.

3.1.4.2 Positive Feedback with Input-Referred Offset

The input-referred offset of the differential amplifier is primarily driven by process mismatch between the two input MOSFET devices. Modeled as a DC voltage at the input

of one of the MOSFETs, Figure 3.25 shows a positive feedback with input-referred offset, V_{os}. Calculating the offset transfer to the output node gives the relationship

$$H_{os} = \frac{V_{out}}{V_{os}} = \frac{\frac{R_2}{R_2+R_L}(g_m R_L)}{1-\frac{R_2}{R_2+R_L}\cdot\frac{R_1}{R_1+R_2}\left(g_m R_L+\frac{R_L}{R_2}\right)}. \tag{3.66}$$

This can be referred back to the input of the positive feedback amplifier by dividing by the closed-loop gain, giving the input-referred offset equation

$$V_{os,in} = \frac{H_{os}}{H}V_{os} = \frac{g_m R_L(1+\beta_f)}{g_m R_L+\frac{R_L}{R_2}}V_{os}. \tag{3.67}$$

As was the case for negative feedback, under the assumption that $g_m R_L \gg R_L/R_2$, this expression simplifies to $V_{os,in} \approx (1+\beta_f)V_{os}$. This assumption, however, may not apply in scaled technologies as $g_m R_L$ is degraded. Over a range of valid R_2 values Figure 3.26

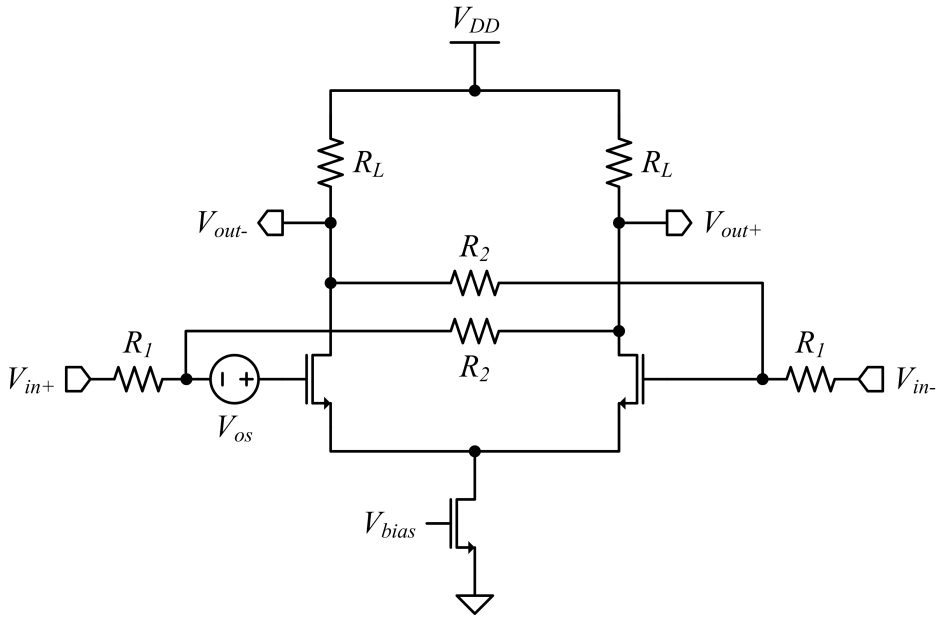

Figure 3.25 Differential amplifier with positive feedback and input-referred offset, V_{os}.

shows this input-referred offset voltage increase due to the application of positive feedback.

3.1.4.3 Positive Feedback with Input-Referred Noise

Using Figure 3.27, the impact of the noise sources in the circuit can be referred back to the input to calculate the input-referred noise. Using superposition, the baseline amplifier input-referred noise, e_a, transfer function is calculated as

$$V_{out,ea} = e_a \frac{\frac{R_2}{R_2+R_L}(g_m R_L)}{1-\frac{R_2}{R_2+R_L}\cdot\frac{R_1}{R_1+R_2}\left(g_m R_L+\frac{R_L}{R_2}\right)}. \tag{3.68}$$

The contribution from the resistor R_1 is calculated as

$$V_{out,e1} = e_1 \frac{\frac{R_2}{R_2+R_L}\cdot\frac{R_2}{R_1+R_2}\left(g_m R_L+\frac{R_L}{R_2}\right)}{1-\frac{R_2}{R_2+R_L}\cdot\frac{R_1}{R_1+R_2}\left(g_m R_L+\frac{R_L}{R_2}\right)} \tag{3.69}$$

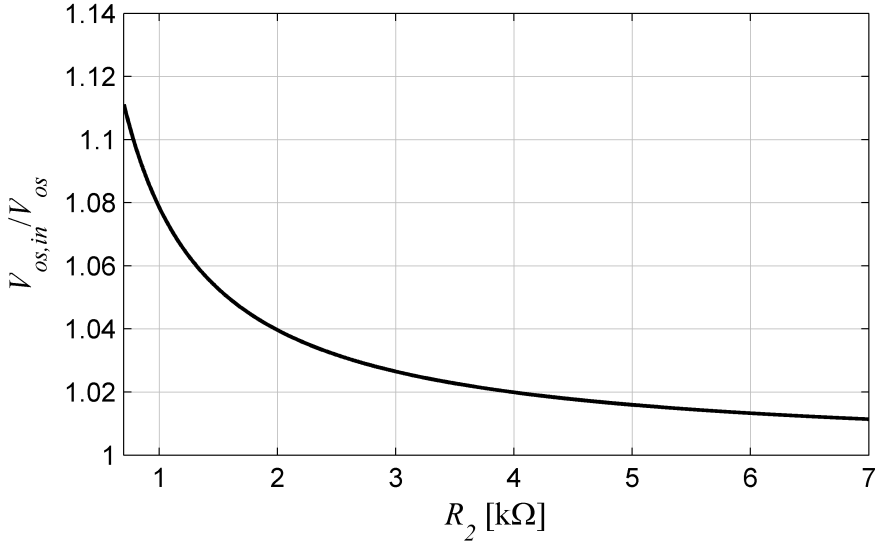

Figure 3.26 Differential amplifier with positive feedback input-referred offset increase versus valid R_2 values with $g_m = 50$ mS, $R_L = 200\ \Omega$, and $R_1 = 100\ \Omega$.

and R_2 gives

$$V_{out,e2} = -e_2 \frac{\frac{R_2}{R_2+R_L}\cdot\frac{R_1}{R_1+R_2}\left(g_m R_L+\frac{R_L}{R_1}\right)}{1-\frac{R_2}{R_2+R_L}\cdot\frac{R_1}{R_1+R_2}\left(g_m R_L+\frac{R_L}{R_2}\right)}. \tag{3.70}$$

The total noise power at the output node is the contribution from the baseline amplifiers as well as two R_1 resistors and two R_2 resistors

$$V_{out}^2 = V_{out,ea}^2 + 2V_{out,e1}^2 + 2V_{out,e2}^2. \tag{3.71}$$

This noise power can be referred back to the input by dividing by the closed-loop gain transfer function, giving

$$E_{in}^2 = V_{out}^2 \left[\frac{1-A_f\beta_f}{A_f}\right]^2. \tag{3.72}$$

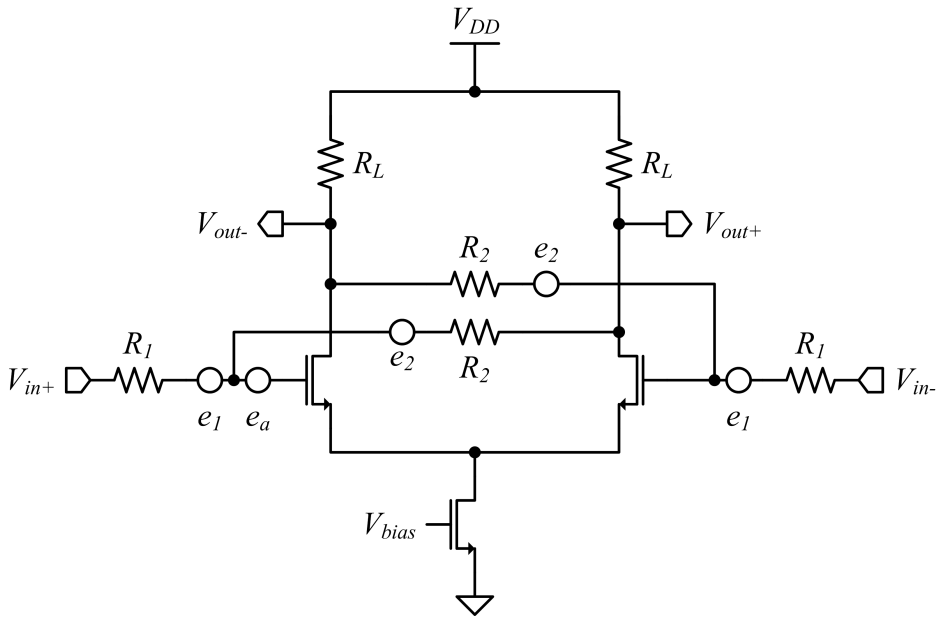

Figure 3.27 Differential amplifier with positive feedback and noise sources, e_a, e_1, and e_2.

Substituting the above expressions yields the expanded input-referred noise expression

$$E_{in}^2 = e_a^2 \left[\frac{g_m R_L(1+\beta)}{g_m R_L + \frac{R_L}{R_2}}\right]^2 + 2e_1^2 + 2e_2^2 \left[\beta \frac{g_m R_L + \frac{R_L}{R_1}}{g_m R_L + \frac{R_L}{R_2}}\right]^2. \quad (3.73)$$

Inserting the known thermal noise contributions from the resistors gives the final input-referred noise expression

$$E_{in}^2 = e_a^2 \left[\frac{g_m R_L(1+\beta)}{g_m R_L + \frac{R_L}{R_2}}\right]^2 + 8kT\Delta f R_1 + 8kT\Delta f R_2 \left[\beta \frac{g_m R_L + \frac{R_L}{R_1}}{g_m R_L + \frac{R_L}{R_2}}\right]^2. \quad (3.74)$$

As was the case in previous analysis, the thermal noise contributions from the resistors are new noise sources. The input-referred noise of the baseline amplifier is a shaped noise source. The factor by which e_a is shaped is identical to the input-referred offset expression and is illustrated in Figure 3.26.

3.1.4.4 Positive Feedback Common-Mode Rejection Ratio

The baseline amplifier common-mode rejection ratio for the circuit of Figure 3.28 was previously shown to be $CMRR_{OL} = 1 + 2g_m R_{tail}$. Using this, the common-mode rejection for the positive feedback amplifier can be calculated as

$$H_c(s) = \frac{\frac{R_2}{R_2+R_L} \cdot \frac{R_2}{R_1+R_2}\left(\frac{g_m R_L}{CMRR_{OL}} + \frac{R_L}{R_2}\right)}{1 - \frac{R_2}{R_2+R_L} \cdot \frac{R_1}{R_1+R_2}\left(\frac{g_m R_L}{CMRR_{OL}} + \frac{R_L}{R_2}\right)} = \frac{A_{f,c}}{1 - A_{f,c}\beta_f} \quad (3.75)$$

where the common-mode forward gain is

$$A_{f,c} = \frac{R_2}{R_2+R_L} \cdot \frac{R_2}{R_1+R_2}\left(\frac{g_m R_L}{CMRR_{OL}} + \frac{R_L}{R_2}\right) \quad (3.76)$$

and the common-mode feedback factor is $\beta_{f,c} = R_1/R_2$. Finally, the rejection ratio can be calculated by comparing (3.75) to the open-loop gain, giving

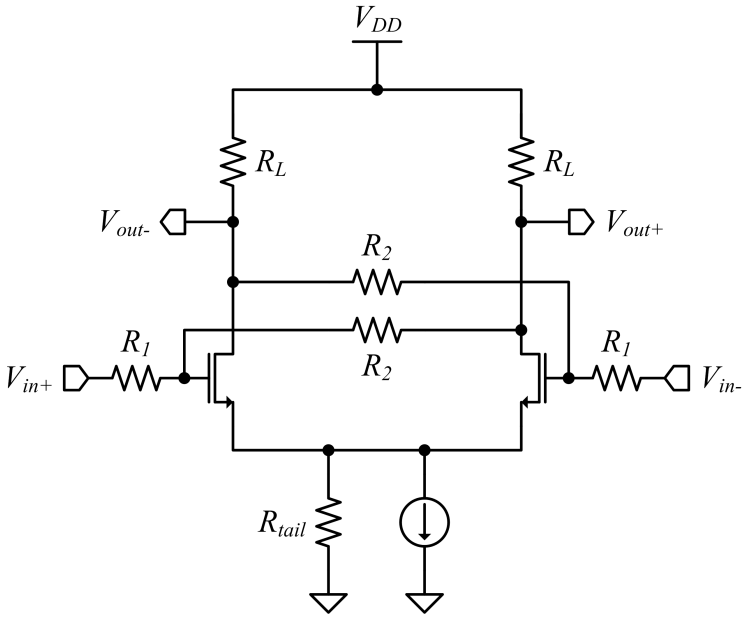

Figure 3.28 Differential amplifier with positive feedback for CMRR analysis and finite tail current source output impedance, R_{tail}.

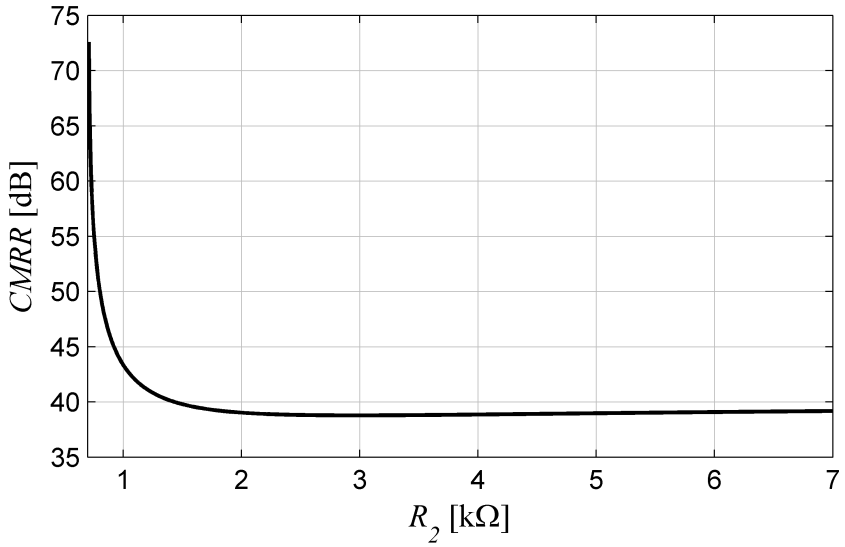

Figure 3.29 Differential amplifier with positive feedback CMRR over valid R_2 range with $g_m = 50$ mS, $R_L = 200$ Ω, $R_1 = 100$ Ω, and $R_{tail} = 1$ kΩ.

$$CMRR = \left|\frac{A_f}{A_c}\right| = \frac{A_f}{A_{f,c}} \cdot \frac{1-A_{f,c}\beta_f}{1-A_f\beta_f}. \tag{3.77}$$

Over the valid R_2 range, Figure 3.29 shows CMRR for the positive feedback differential amplifier.

3.1.4.5 Positive Feedback Gain-Bandwidth Product

To calculate the effect of positive feedback on the differential amplifier's gain-bandwidth product, frequency-dependent components, specifically capacitors, must be added to the model. As indicated in Section 3.1.4.1 the addition of MOSFET capacitances such as C_{gd} and C_{gs} complicate the analysis and do not provide significant insight into the circuit relationships. Instead, the gain-bandwidth product behavior is observed in a capacitor-loaded differential amplifier as shown in Figure 3.30. Calculating the transfer function of this circuit gives

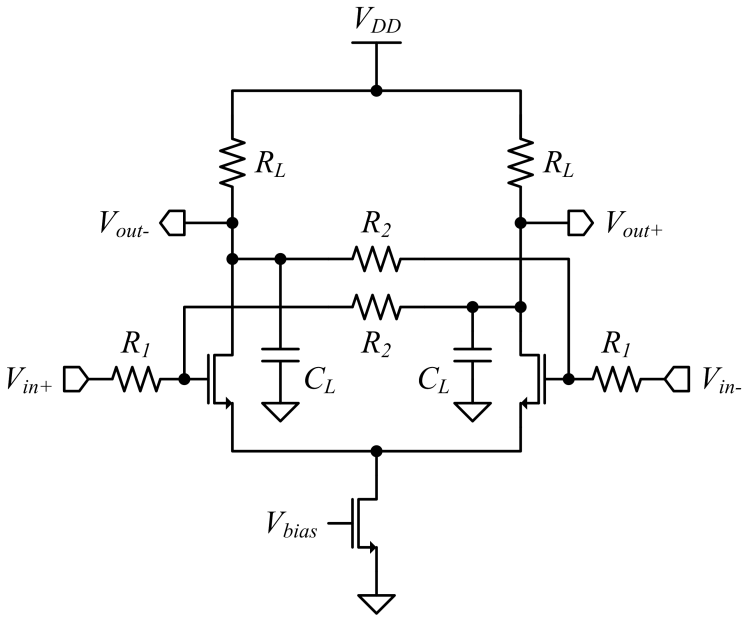

Figure 3.30 Differential amplifier with positive feedback and capacitive load, C_L, for frequency response analysis.

$$H(s) = \frac{\frac{R_2}{R_1+R_2}\frac{R_2}{R_2+R_L}\left(g_m R_L+\frac{R_L}{R_2}\right)}{s\frac{R_2 R_L C_L}{R_2+R_L}+1-\frac{R_1}{R_1+R_2}\frac{R_2}{R_2+R_L}\left(g_m R_L+\frac{R_L}{R_2}\right)}. \tag{3.78}$$

The DC gain of this structure is identical to the unloaded amplifier and its -3 dB bandwidth is

$$p_{1H} = p_1 \frac{R_2+R_L}{R_2}\left(1 - A_f\beta_f\right) = p_1 \frac{R_1(1-g_m R_L)+R_2+R_L}{R_1+R_2} \tag{3.79}$$

where $p_1 = 1/R_L C_L$. This gives a gain-bandwidth product of

$$GBP = p_1 A_f \frac{R_2+R_L}{R_2} = p_1 \frac{R_2}{R_1+R_2}\left(g_m R_L + \frac{R_L}{R_2}\right) \tag{3.80}$$

and a gain-bandwidth product ratio of

$$GBP_r = \frac{R_2}{R_1+R_2}\left(1 + \frac{1}{g_m R_2}\right). \tag{3.81}$$

Figure 3.31 shows GBP_r across valid R_2 values as compared to a negative feedback differential amplifier with the same parameters. Both positive feedback and negative feedback show degradation in GBP_r, but the positive feedback degradation is slightly less pronounced than that of the negative feedback.

3.1.5 Positive Feedback Summary

This section has discussed the impact positive feedback has on multiple types of amplifier structures and models. In addition to its impact on the DC gain of the amplifier, the positive feedback also affects the input and output impedances, the input-referred DC offset and noise, the common-mode rejection ratio, and the gain-bandwidth product of the

closed-loop amplifier. Table 3.1 summarizes these effects on the amplifier and compares those effects to that of negative feedback.

3.2 Sensitivity Analysis

As MIG degrades with technology scaling, the ability to use positive feedback as a stable technique to increase DC gain at the cost of bandwidth becomes more feasible. The open-loop gain degradation – as a result of MIG degradation – yields an increasing and more practical range of the feedback factor, β. The positive feedback components can be chosen such that extreme increases in DC gain can be achieved; however these gain increases come at the cost of sensitivity to variation in the positive feedback components and open-loop amplifier parameters [80].

Using the voltage amplifier model from Section 3.1.3 and (3.37), the sensitivities of H_{DC} can be defined. Partial derivatives of H_{DC} with respect to each variable are a simple

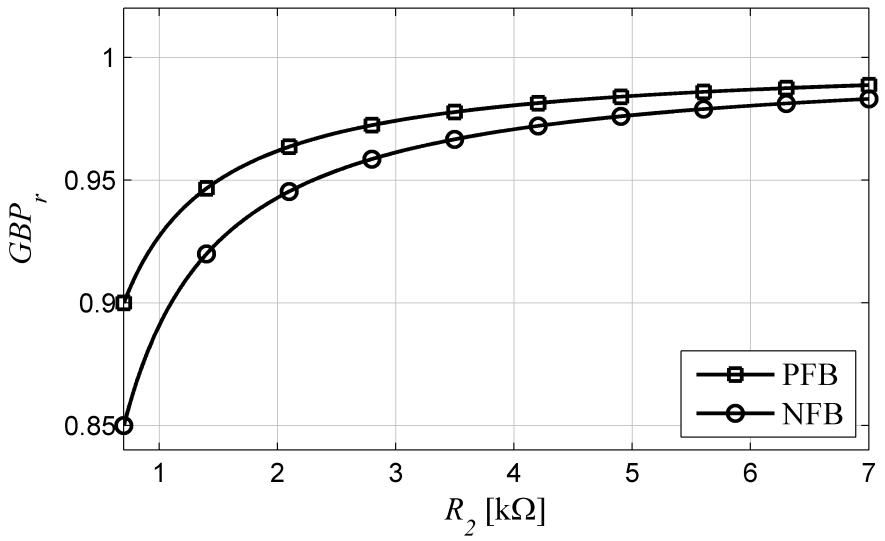

Figure 3.31 GBP_r for a positive feedback differential amplifier over valid R_2 range with $g_m = 50$ mS, $R_L = 200\ \Omega$, $R_1 = 100\ \Omega$, and $R_{tail} = 1$ kΩ.

measure of the sensitivity of the closed-loop gain to that variable. This analysis yields the following five equations:

$$\frac{\partial H_{DC}}{\partial A_{DC}} = \frac{G_{out}(G_1 + H_{DC}G_2)}{\Psi} \tag{3.82}$$

$$\frac{\partial H_{DC}}{\partial R_{in}} = \frac{G_{in}^2(G_2 + G_{out})H_{DC}}{\Psi} \tag{3.83}$$

$$\frac{\partial H_{DC}}{\partial R_{out}} = -\frac{G_{out}^2\{G_1 A_{DC} - H_{DC}[G_1 + \mathrm{G_{in}} + G_2(1 - A_{DC})]\}}{\Psi} \tag{3.84}$$

$$\frac{\partial H_{DC}}{\partial R_1} = -\frac{G_1^2[G_2 + A_{DC}G_{out} - H_{DC}(G_2 + G_{out})]}{\Psi} \tag{3.85}$$

$$\frac{\partial H_{DC}}{\partial R_2} = -\frac{G_2^2\{G_1 - H_{DC}[G_1 + \mathrm{G_{in}} + G_{out}(1 - A_{DC})]\}}{\Psi} \tag{3.86}$$

Equations (3.82) through (3.86) are greatest when Ψ approaches zero. When evaluated at design points consistent with the positive feedback methodology here, (3.82) through (3.86) yield the results shown in Figure 3.32, Figure 3.33, and Figure 3.34. These graphs show enhanced sensitivities around $\Psi = 0$. Due to the large magnitude of R_{in} with

Table 3.1 Positive feedback configuration summary

Parameter	PFB	NFB
Gain	↑	↓
Bandwidth	↓	↑
GBP	↓	↓
Input Impedance	↓	↓
Output Impedance	↑	↓
Offset	↑	↑
Noise	↑	↑
CMRR	↑	↓

respect to the other impedances, there is little sensitivity to this parameter. The other sensitivities, however, are similar in magnitude and must receive equal attention in order to create a robust amplifier design.

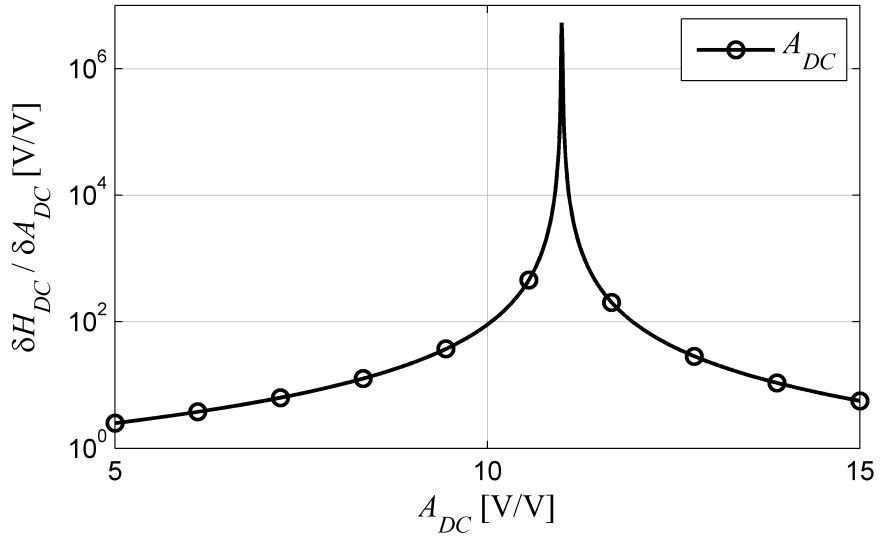

Figure 3.32 H_{DC} Sensitivity to A_{DC} variation with $R_{in} = 10$ MΩ, $R_{out} = 200$ Ω, $R_1 = 100$ Ω, and $R_2 = 800$ Ω.

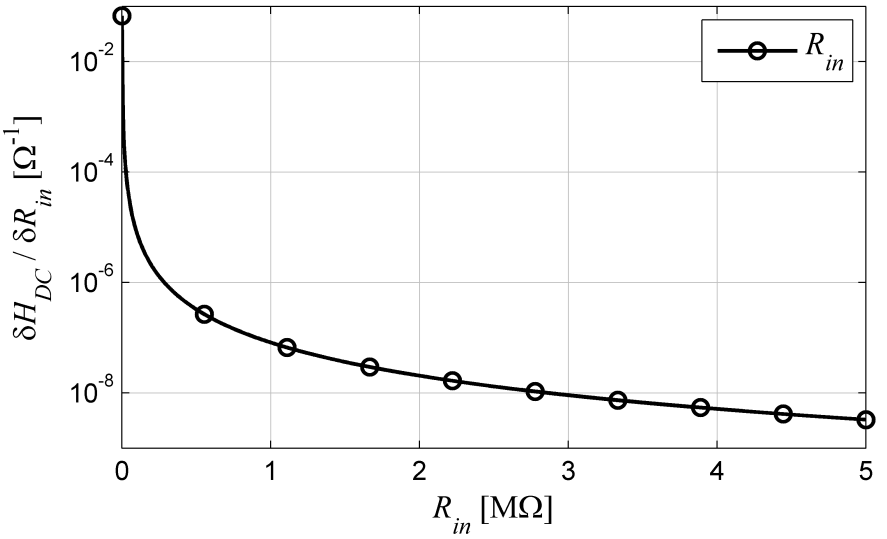

Figure 3.33 H_{DC} Sensitivity to R_{in} variation with $A_{DC} = 10$, $R_{out} = 200$ Ω, $R_1 = 100$ Ω, and $R_2 = 800$ Ω.

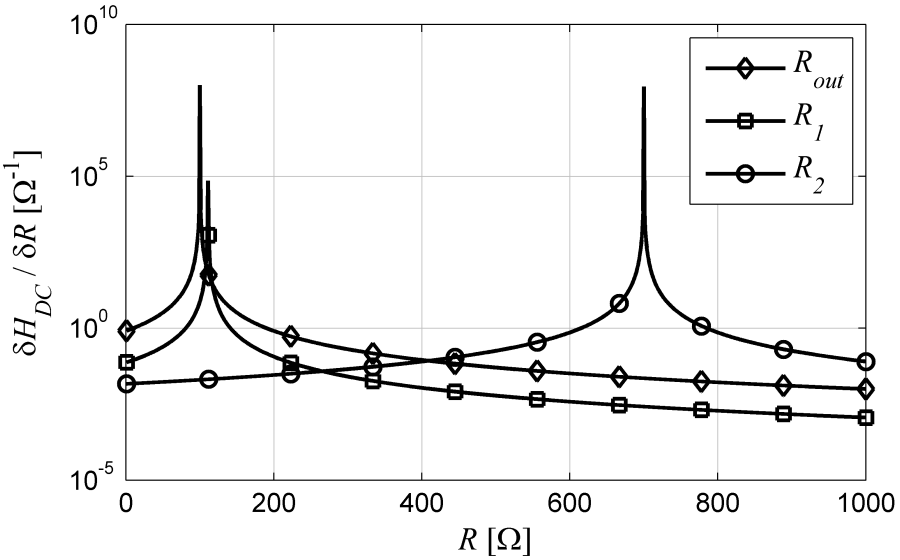

Figure 3.34 H_{DC} Sensitivity to R_{out}, R_1, and R_2 variations with $A_{DC} = 10$, $R_{in} = 10$ MΩ, $R_{out} = 200$ Ω, $R_1 = 100$ Ω, and $R_2 = 800$ Ω.

3.2.1 Optimization Algorithm

While there are quite a few methods to optimize this system of equations, this work uses a simple genetic algorithm as one example to perform the task [81], [82]. Genetic algorithms in general can have the tendency of becoming stuck in a local minimum, but the implementation of random mutations can help avoid this situation [82]. In this technique a predefined number of members, the population, is seeded with random or pre-defined values of genes; these are an array of values of interest that define each member of the population. In this case the genes are $[A_{DC}\ R_{in}\ R_{out}\ R_1\ R_2]$.

Each member of the population is then evaluated by a fitness function. Defining this fitness function is the most important step in the implementations of this and any other optimization algorithm. The fitness function can be defined to match a specific application, but for generic amplifier design the following can be used

$$w = \begin{cases} 0, & \frac{H_{DC}}{A_{DC}} \leq 1 \\ \frac{H_{DC}/A_{DC}}{S_{ADC}+S_{Rin}+S_{Rout}+S_{R1}+S_{R2}+b}, & \frac{H_{DC}}{A_{DC}} > 1 \end{cases} \tag{3.87}$$

where $S_x = \log_{10}(\delta H_{DC}/\delta x)$, and b is a fixed bias of sufficient value to provide the proper weight to negative values of S_x. This is to say that b has to be large enough such that the denominator of (3.87) is always positive. The logarithm of the sensitivity function is used because of the wide range in sensitivity values as Ψ approaches zero.

This fitness function achieves two things: high closed-loop gain ratios, H_{DC}/A_{DC}, and low sensitivity to all parameters. Additionally, Equation (3.87) is a piecewise function and defined as zero for $H_{DC}/A_{DC} < 1$ to further discourage solutions that are highly insensitive, but lack the gain enhancement that positive feedback is supposed to address. This piecewise behavior also prevents the propagation of unstable systems because the magnitude of H_{DC} becomes negative outside of the stability criteria and therefore $H_{DC}/A_{DC} < 1$.

Members of the population are chosen at random with a probability weighted by their fitness score to propagate to the next generation. The next generation is then formed using crossover and mutation techniques, and the process is repeated for a fixed number of generations. The crossover technique is a finite probability that a pair of next-generation members will cross genes at a random point. For example, if one member had the genes $m_1 = [A_{DC,1}\ R_{in,1}\ R_{out,1}\ R_{1,1}\ R_{2,1}]$ and another has the genes $m_2 = [A_{DC,2}\ R_{in,2}\ R_{out,2}\ R_{1,2}\ R_{2,2}]$, one crossover could be $m_3 = [A_{DC,1}\ R_{in,1}\ R_{out,2}\ R_{1,2}\ R_{2,2}]$. The mutation technique is a finite probability that a random change happens to a single gene within a single member of the population.

3.2.2 Optimization Results

The algorithm described in Section 3.2.1 was implemented in MATLAB™. The population size was 200 and it was performed over 1,000 generations. The initial population is seeded with uniformly distributed random genes, $0 < A_{DC} < 20$, $0 < R_{in} < 20\ \text{M}\Omega$, $0 < R_{out} < 1\ \text{k}\Omega$, $0 < R_1 < 10\ \text{k}\Omega$, $0 < R_2 < 10\ \text{k}\Omega$. The mutation rate is 10%, and mutated genes are randomly modified from 50% to 200% of their nominal value. Additionally, these mutations are limited to reasonable values of the given parameter: $A_{DC} < 20$, $R_{in} < 20\ \text{M}\Omega$, $R_{out} < 1\ \text{k}\Omega$, $R_1 < 10\ \text{k}\Omega$, and $R_2 < 10\ \text{k}\Omega$. After a few sample runs, the offset was chosen as $b = 500$ to sufficiently bias the denominator of the fitness function.

Figure 3.35 shows one example of an optimization run. The member of the final generation with the maximum fitness score has the performance and sensitivities shown in Table 3.2. While this yields impressive results in terms of gain enhancement with

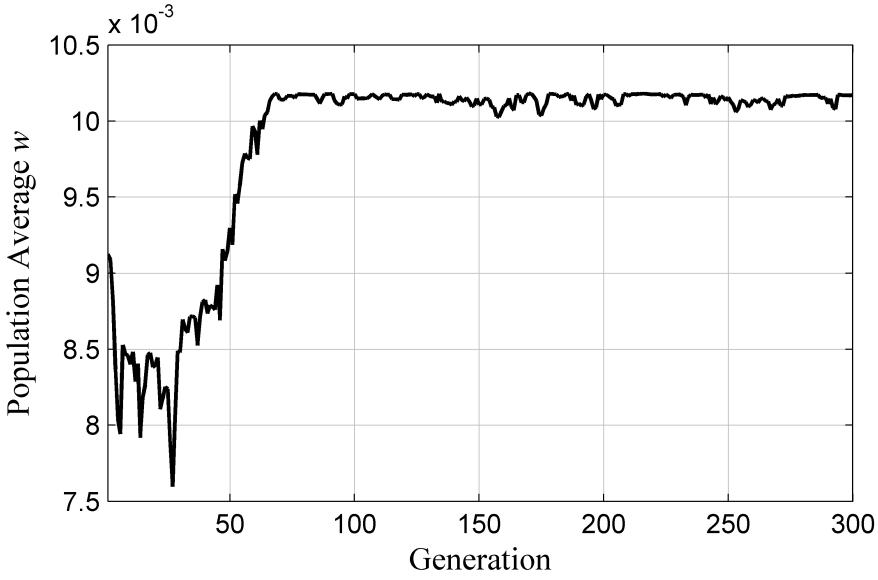

Figure 3.35 Example Optimization Run

Table 3.2 Optimization run results with no limitations on amplifier parameters

Parameter	Value	Sensitivity
A_{DC} [V/V]	20	31.88
R_{in} [MΩ]	20	22.56
R_{out} [Ω]	891	27.88
R_1 [kΩ]	10	29.16
R_2 [kΩ]	189	27.88
H_{DC} [V/V]	1.69×10^{17}	–

$H_{DC} = 1.69 \times 10^{17}$, it assumes that the designer has significant control over system parameters – specifically A_{DC}, R_{in}, and R_{out} – which is unlikely to be the case in a realistic implementation.

A more useful tool has the capability to either limit or fix the values of certain parameters. With this option, the designer can limit or fix the parameters that cannot be controlled and focus on those that can be modified. For example, for a given open-loop amplifier A_{DC}, R_{in}, and R_{out} will be fixed and the designer will have control over R_1 and R_2. Implementing this feature in the MATLAB script and rerunning with the values of A_{DC}, R_{in}, and R_{out}, the member of the final population with the highest fitness score is $R_1 = 5.98\,\text{k}\Omega$, $R_2 = 53.6\,\text{k}\Omega$. This results in $H_{DC} = 7.89 \times 10^{16}$ as shown in Table 3.3. Again, these results are impressive but the tool is still missing a major consideration: The valid range of R_2 values that is defined by Equation (3.39) and (3.40).

Table 3.3 Optimization run results with fixed values for $A_{DC} = 10$, $R_{in} = 10$ MΩ, and $R_{out} = 200$ Ω.

Parameter	Value	Sensitivity
A_{DC} [V/V] fixed	10	31.84
R_{in} [MΩ] fixed	10	22.57
R_{out} [Ω] fixed	200	28.07
R_1 [kΩ]	5.98	29.02
R_2 [kΩ]	53.6	28.07
H_{DC} [V/V]	7.89×10^{16}	–

Equations (3.39) and (3.40) show that the feedback resistor must be in the range $53.545\ \text{k}\Omega < R_2 < 89.7\ \text{M}\Omega$ to maintain stability for the given A_{DC}, R_{in}, R_{out} and R_1. The optimization algorithm has placed R_2 a fraction of an ohm from its limit, and there will surely be die in which process variability yields a low R_2 and causes the system to go unstable.

The final addition to the optimization algorithm is the dynamic restriction of R_2 based on all other values in the system. While this limitation could be on any variable, R_2 is chosen here because its limits have already been defined. This component will restrict R_2 to the values described by (3.39) and (3.40) including a designer input for known resistor uncertainty due to process variation. Using a typical resistor variation of 20%, the optimization algorithm converges on the solution $R_1 = 10\ \text{k}\Omega$, and $R_2 = 112.1\ \text{k}\Omega$. This results in $H_{DC} = 49.96$ as shown in Table 3.4. These results are much more reasonable and realistic.

Table 3.4 Optimization run results with fixed values for $A_{DC} = 10$, $R_{in} = 10$ MΩ, and $R_{out} = 200$ Ω including 20% resistor variation for R_1 and R_2.

Parameter	Value	Sensitivity
A_{DC} [V/V] fixed	10	1.43
R_{in} [MΩ] fixed	10	−7.60
R_{out} [Ω] fixed	200	−2.66
R_1 [kΩ]	10	−1.70
R_2 [kΩ]	112.1	−2.75
H_{DC} [V/V]	49.96	–

Additionally, limiting R_1 and R_2 variations to below 1 kΩ for reasonable resistor sizes, the algorithm yields $R_1 = 165.8\,\Omega$, and $R_2 = 1.615\,\text{k}\Omega$, with $H_{DC} = 50.6$ as shown in Table 3.5. The final MATLAB code is shown in Section A.3.

Table 3.5 Optimization run results with fixed values for $A_{DC} = 10$, $R_{in} = 10$ MΩ, and $R_{out} = 200$ Ω including 20% resistor variation for R_1 and R_2 limiting R_1 and R_2 to 1 kΩ maximum.

Parameter	Value	Sensitivity
A_{DC} [V/V] fixed	10	1.49
R_{in} [MΩ] fixed	10	−9.33
R_{out} [Ω] fixed	200	−0.81
R_1 [Ω]	165.8	−0.15
R_2 [Ω]	1615	−0.90
H_{DC} [V/V]	50.6	–

3.3 Summary

In this chapter, the use of positive feedback as a method to increase the gain of a linear amplifier was described. In addition, criteria for keeping the system stable while applying positive feedback were also derived. As was shown in the previous chapter, the application of feedback will affect other circuit parameters such as input and output impedance, input-referred offset and noise, common-mode rejection ratios, and gain-bandwidth products. Positive feedback is shown to affect these circuit parameters as well.

These stability criteria and circuit effects were evaluated and explored in four different positive feedback structures with varying level of detail. These structures were the block diagram, the ideal operational amplifier model, the voltage amplifier model, and finally a practical circuit implementation, the differential amplifier. While this chapter focused on voltage amplifier models, this analysis can be extended to other amplifier types with different feedback configurations. Some other feedback topology examples are explored in Appendix B.

The mathematical nature of applying positive feedback in an amplifier circuit involves pushing the system's transfer function towards a vertical asymptote of high DC gain. As a result, the sensitivity of the circuit's behavior is enhanced around these operating regions. This chapter concludes with an exploration of this sensitivity and presents one design methodology solution to address and design around the inevitable process variation in a practical implementation in an integrated circuit.

CHAPTER 4
RESULTS

The positive feedback method described in Chapter 3 is most applicable for amplifiers with relatively small gains and high bandwidths. The small gain creates a valid feedback factor range that is usable by realistic circuits with realistic process and device variations. Positive feedback has been shown to degrade the gain-bandwidth product, so the high bandwidth allows for the final amplifier to still have amplified frequency responses in the MHz or GHz range. The proposed technique is well suited for circuits that meet these criteria. The basic differential amplifier stage explored in Chapter 3 is a simple example of a circuit that meets these criteria.

4.1 Design and Simulation Results

This amplifier was designed and fabricated in TSMC's 65 nm logic process using only thin oxide, standard threshold voltage devices with $V_{DD} = 1\,\text{V}$ power supply [83]. The basic amplifier symbol is shown in Figure 4.1 and has two power supplies, V_{DD} and ground, two inputs V_{IN+} and V_{IN-}, two outputs, V_{OUT+} and V_{OUT-}, and a power down, PD, signal. The amplifier itself is shown with devices' sizing in Figure 4.2. In order for

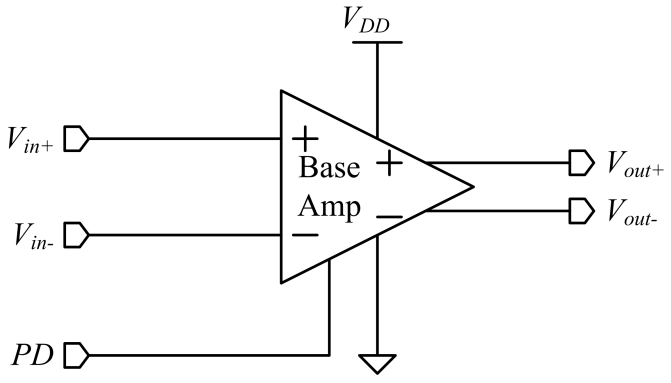

Figure 4.1 Top level symbol of a practical implementation of differential amplifier with differential inputs, differential output, and a power down signal.

the tail current to operate, it requires a DC bias voltage on the gate of MN2, V_{bias}.

In order to provide this bias, a constant transconductance, or constant g_m, circuit was designed as shown in Figure 4.3. This type of circuit is well understood and has been improved upon [84] - [86], but for the purposes of this application, the basic well-known implementation is sufficient. Typically, the transconductance of a MOSFET is defined as

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_d} \tag{4.1}$$

where μ is the mobile carrier mobility, C_{ox} is the oxide capacitance per unit area, I_d is the device's DC drain current and W and L are the device width and length, respectively. This indicates that g_m is a function of the device parameters, current and geometry. As defined in [86], the transconductance of the constant g_m circuit output device, MN1, is

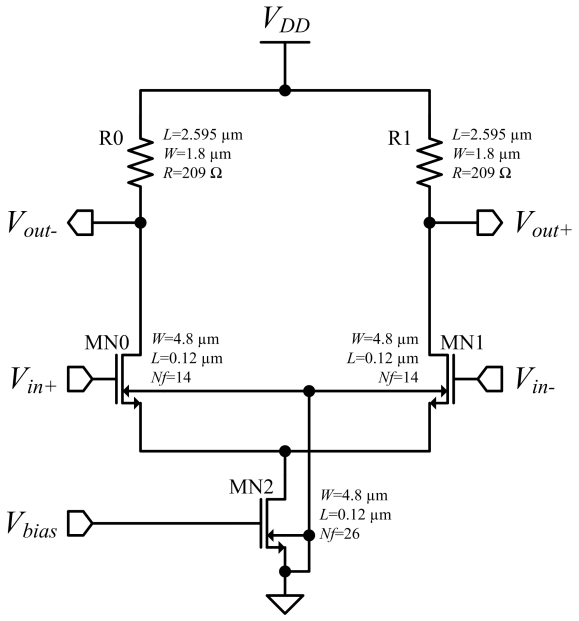

Figure 4.2 Transistor level schematic of the baseline differential amplifier implemented with 65 nm, thin oxide, standard V_T, 1 V transistors.

$$g_{m,N1} = \frac{2}{R0}\left(1 - \sqrt{\frac{W_{N1}L_{N0}}{W_{N0}L_{N1}}}\right). \tag{4.2}$$

This indicates that the transconductance of the output device is no longer a function of the device parameters and bias currents, but instead it is a function of R0 and the size ratio between MN1 and MN0. The transconductance of MN1 is process-independent with the exception of local geometry variation and resistor variation. As a result, R0 is often implemented as a high-precision external component to further eliminate variation in the device transconductance. In the case of this work, high precision was not required and R0 was implemented as an on-chip polysilicon resistor with dimensions shown in Figure 4.3.

The gate of the tail-current device in the baseline amplifier in Figure 4.2 is driven with the constant g_m generated V_{bias} to generate the DC current source for the differential

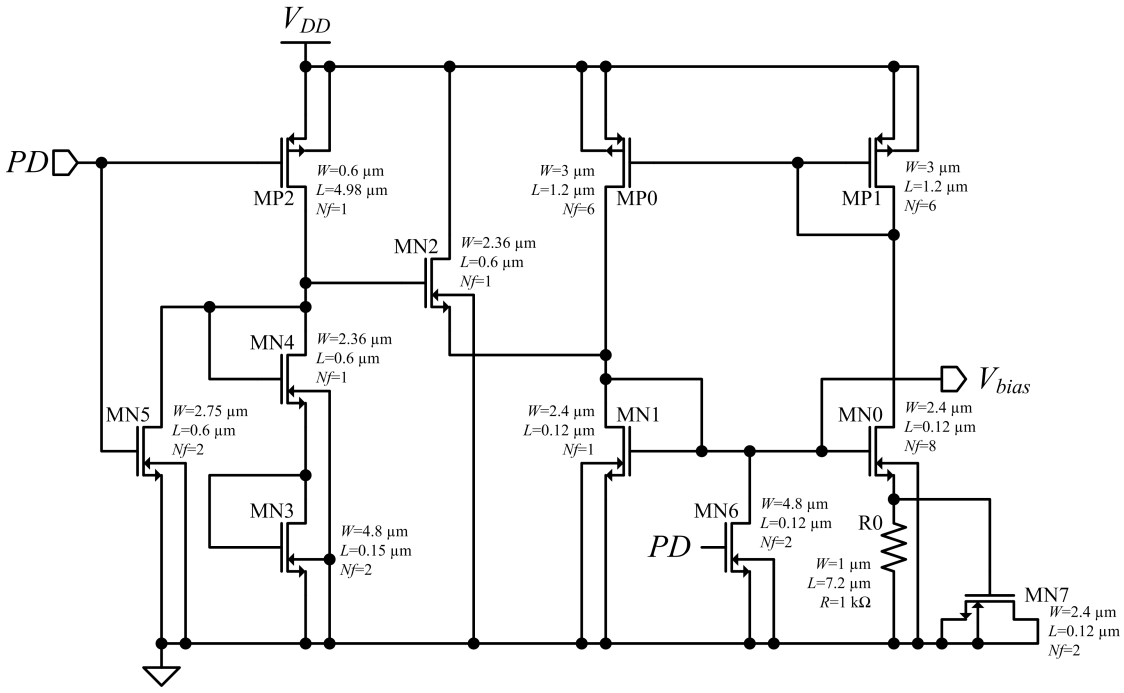

Figure 4.3 Transistor level schematic of constant g_m bias voltage generator for baseline amplifier implemented with 65 nm, thin oxide, standard V_T, 1 V transistors.

amplifier. Knowing the target g_m of the bias circuitry, the tail current of the differential amplifier can be calculated as

$$I_{tail} = \frac{g_m^2}{2\mu C_{ox}\frac{W}{L}}. \tag{4.3}$$

While this conversion from constant g_m to I_{tail} re-introduces some process variation in μ and C_{ox}, simulations show that the tail current remains sufficiently well controlled for the purposes of this application.

Finally, the constant g_m circuitry requires assistance in starting up. The stacked current mirrors formed by MN0/MN1 and MP0/MP1 in Figure 4.3 have two stable current operating points: the point described by the equations above, and zero current. While the circuitry is powered down with $PD = 1$ V, MN6 ensures the zero current state by pulling

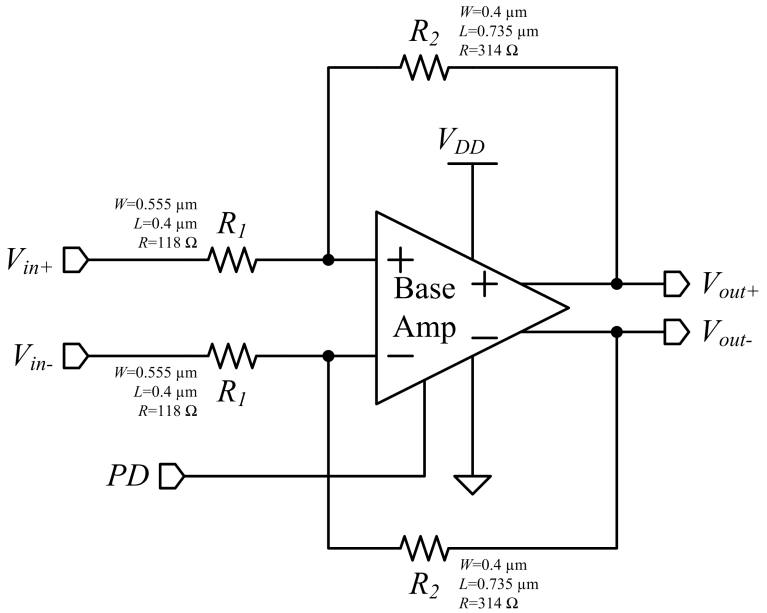

Figure 4.4 Combined baseline amplifier, bias circuitry and resistive feedback to form a positive feedback amplifier (PFBa) implemented with 65 nm, thin oxide, standard V_T, 1 V transistors.

the gate of the NMOS mirror to ground and turning off the current flow. When the circuit is started and $PD = 0\,\mathrm{V}$, the circuit will remain in this stable state unless something pushes the current into the circuit, therefore forcing the other intended stable operating state. With MN6 driven off, the gate of MN2 is pulled towards V_{DD} by MP2 biased by the two diodes MN3 and MN4. This turns on MN2 slightly, allowing a small amount of current to flow from MN2 to the NMOS current mirror MN1/MN0. This current forces the constant g_m circuit out of the stable zero-current operating point and into the intended constant g_m operating point. Once the circuit has started up, the injected startup current will continue to flow. As a result, this current is designed to be as small as possible to eliminate g_m errors due to the extra current while still being large enough to allow the circuitry to start up over all process, voltage and temperature corners.

Finally, Figure 4.4 shows the baseline amplifier and bias generator used as a core amplifier inside of a fully differential positive feedback loop. The baseline amplifier without feedback and two positive feedback amplifiers were designed. Subsequent sections in this chapter discuss in detail the simulation results of each individual circuit block, and the design results are summarized here. The positive feedback was implemented with polysilicon resistors with a fixed $R_1 = 118\,\Omega$ and two R_2 values, $R_2 = 314\,\Omega$ and $375\,\Omega$. The baseline amplifier used a $V_{DD} = 1\,\mathrm{V}$ supply voltage and had typical simulated characteristics of $A_{DC} = 12.9\,\mathrm{dB}$, $R_{in} = 3.77\,\mathrm{M\Omega}$, $R_{out} = 168\,\Omega$, $GBP = 44.7\,\mathrm{GHz}$, and $p_1 = 10.1\,\mathrm{GHz}$.

4.1.1 Simulation Conditions

In order to verify that the design is robust, the amplifiers and support circuitry are simulated over a variety of process, voltage and temperature (PVT) conditions, referred to as corners. Additionally, Monte Carlo simulations are used to model statistical process variation and device mismatch that occur in fabricated circuitry. The process corners are summarized in Table 4.1 and are intended to cover the extremes of the device variation defined as acceptable by the manufacturer. This table shows that the semiconductor devices are described in three categories: MOSFETs, resistors, and capacitors. Although there is little correlation between the variation in these groups of devices, they are varied together to keep the number of permutations to a manageable amount. Table 4.2 describes the temperature corner variation. These corners are defined at room temperature as well as a hot and cold extreme defined by typical commercial grade electronics temperature ranges. Finally, Table 4.3 describes the variation in input supply voltage.

Table 4.1 Qualitative description of process corner definition including MOSFET, resistor and capacitor models variation

Process Code	MOSFET Models	Resistor Models	Capacitor Models	Description
ab	typical NMOS typical PMOS	typical resistance	typical capacitance	Typical process
NP	low V_T NMOS low V_T PMOS	low resistance	low capacitance	Fast process
np	high V_T NMOS high V_T PMOS	high resistance	high capacitance	Slow process
Np	low V_T NMOS high V_T PMOS	typical resistance	typical capacitance	Skew process, fast NMOS
nP	high V_T NMOS low V_T PMOS	typical resistance	typical capacitance	Skew process, fast PMOS

Each of the process, voltage, and temperature variables are permuted together to obtain a list of 45 total corners over which the circuit behavior is observed.

For simplicity, each corner is named by a process code as described in Table 4.1, Table 4.2, and Table 4.3. For example, a typical PVT corner would have the code 'abcd' whereas a fast process, low temperature, and high voltage corner would have the code "NPtV." Furthermore, to simplify graphical displays of corner data, each corner is numbered according to Table 4.4.

Monte Carlo simulation is another valuable statistical tool for robust analog design. In the case of the corners analysis above, the process variation is essentially assumed to be uniform in distribution – that is each process corner has an equally likely chance of occurring. The actual distribution of the process variation, however, is more Gaussian in nature. While the corners analysis is useful to help prove circuit operation at the extremes of process variation, it does not indicate what percentage of individual circuits one could

Table 4.2 Temperature corner definitions.

Process Code	Temperature	Description
c	$27°C$	Room temperature
t	$0°C$	Cold
T	$80°C$	Hot

Table 4.3 Voltage supply voltage definition.

Process Code	V_{DD}	Description
d	1.0 V	Typical voltage
v	0.9 V	Low voltage
V	1.1 V	High voltage

expect to exist at these process extremes. The Monte Carlo analysis, however, does provide this statistical information.

In addition to modeling realistic process variation, Monte Carlo can also model mismatch between individual devices on a given die [87]. Although significant care is taken to reduce this physical mismatch between devices, its presence is inevitable and a robust circuit should be able to operate properly.

Table 4.4 Complete corner list by corner code and corner number.

Corner Number	Corner Code	Process	Voltage	Temperature
1	abcd	Typical	Typical	Typical
2	abcv	Typical	Low	Typical
3	abcV	Typical	High	Typical
4	abtd	Typical	Typical	Low
5	abtv	Typical	Low	Low
6	abtV	Typical	High	Low
7	abTd	Typical	Typical	High
8	abTv	Typical	Low	High
9	abTV	Typical	High	High
10	npcd	Slow	Typical	Typical
11	npcv	Slow	Low	Typical
12	npcV	Slow	High	Typical
13	nptd	Slow	Typical	Low
14	nptv	Slow	Low	Low
15	nptV	Slow	High	Low
16	npTd	Slow	Typical	High
17	npTv	Slow	Low	High
18	npTV	Slow	High	High
19	NPcd	Fast	Typical	Typical

Corner Number	Corner Code	Process	Voltage	Temperature
20	NPcv	Fast	Low	Typical
21	NPcV	Fast	High	Typical
22	NPtd	Fast	Typical	Low
23	NPtv	Fast	Low	Low
24	NPtV	Fast	High	Low
25	NPTd	Fast	Typical	High
26	NPTv	Fast	Low	High
27	NPTV	Fast	High	High
28	nPcd	Skew P	Typical	Typical
29	nPcv	Skew P	Low	Typical
30	nPcV	Skew P	High	Typical
31	nPtd	Skew P	Typical	Low
32	nPtv	Skew P	Low	Low
33	nPtV	Skew P	High	Low
34	nPTd	Skew P	Typical	High
35	nPTv	Skew P	Low	High
36	nPTV	Skew P	High	High
37	Npcd	Skew N	Typical	Typical
38	Npcv	Skew N	Low	Typical
39	NpcV	Skew N	High	Typical
40	Nptd	Skew N	Typical	Low
41	Nptv	Skew N	Low	Low
42	NptV	Skew N	High	Low
43	NpTd	Skew N	Typical	High
44	NpTv	Skew N	Low	High
45	NpTV	Skew N	High	High

4.1.2 Bias Circuit Simulation Results

The purpose of the bias circuitry is to provide a signal to drive the tail current MOSFET of the differential baseline amplifier. While this is an auxiliary circuit, its performance is fundamentally important to that of the baseline and therefore positive feedback amplifiers.

In order to ensure robust operation of the bias circuitry, it is simulated under transient and DC operation conditions. These tests are performed both across PVT corners as well as Monte Carlo process and mismatch variations. In the transient operation case, the startup and shutdown behavior is observed. These tests verify that the startup circuitry operates as expected and proves that the circuitry can be turned off when the amplifier is disabled. The DC operating point simulations verify the robustness of the output voltage and transconductance. The final layout of this circuit is shown in Figure 4.5.

4.1.2.1 Corners Simulations

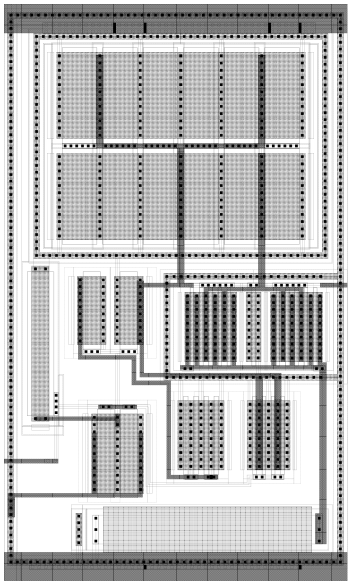

Figure 4.5 Bias circuitry layout in TSMC 65 nm with low voltage, nominal V_T transistors, dimensions are approximately 12 μm by 20 μm or 240 μm^2.

Figure 4.6 shows the transient startup and shutdown behavior of the bias circuitry over all 45 corners. In this simulation at $t = 0$ ns, the circuitry is held in power down, $PD = 1$ V. At $t = 50$ ns, the power down signal is released and the circuitry is started, allowing V_{bias} to reach its steady-state value. At $t = 150$ ns, after the circuitry has stabilized, it is then powered down with $PD = 1$ V. As would be expected, the V_{bias} signal returns to 0 V under this condition. Figure 4.6 indicates that the bias circuitry can start up under all of the corner conditions defined for this work.

The DC behavior of the circuitry is captured in Figure 4.7 and Figure 4.8. Figure 4.7 shows the output voltage, V_{bias}, over corners. The typical PVT corner shows $V_{bias} = 490$ mV with a minimum of $V_{bias} = 442$ mV at NptV and a maximum of $V_{bias} = 531$ mV at nPTv. Figure 4.8 shows the small-signal transconductance, g_m, of the output device NM1. While the output voltage is relatively constant over PVT corners, the

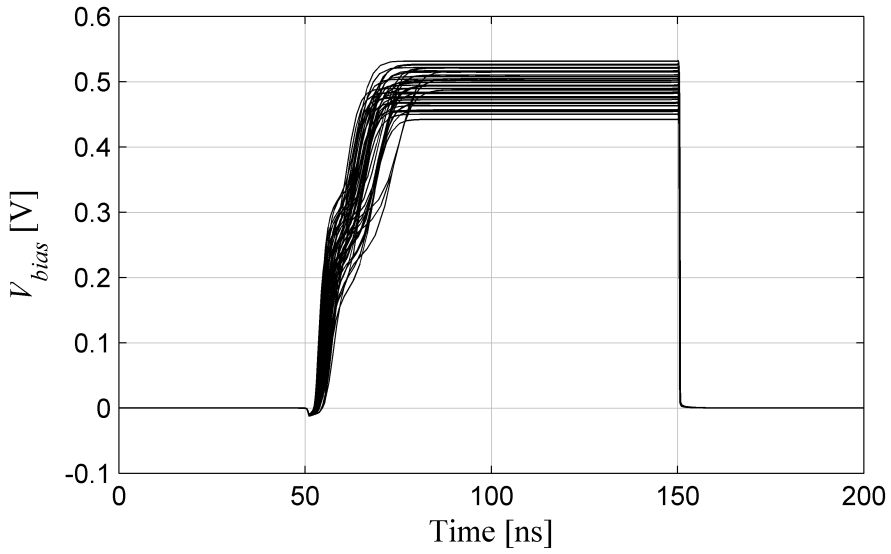

Figure 4.6 Bias circuit startup and shutdown over corners showing output voltage V_{bias} versus time. PD transitions from 1 V to 0 V at $t = 50$ ns and from 0 V to 1 V at $t = 150$ ns.

transconductance varies significantly. This is primarily due to the use of an on-chip resistor to set the transconductance as indicated by (4.2). Figure 4.8 shows typical results of $g_m = 1.09$ mS, with a minimum of $g_m = 0.84$ mS at nptV and a maximum of $g_m = 1.46$ mS at NPTv.

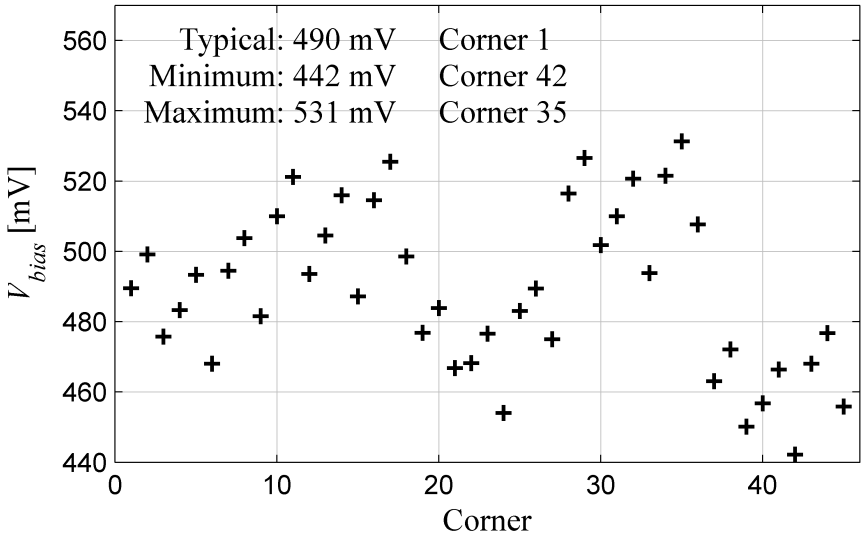

Figure 4.7 Bias circuit DC voltage output voltage, V_{bias}, over corners with $PD = 0$ V.

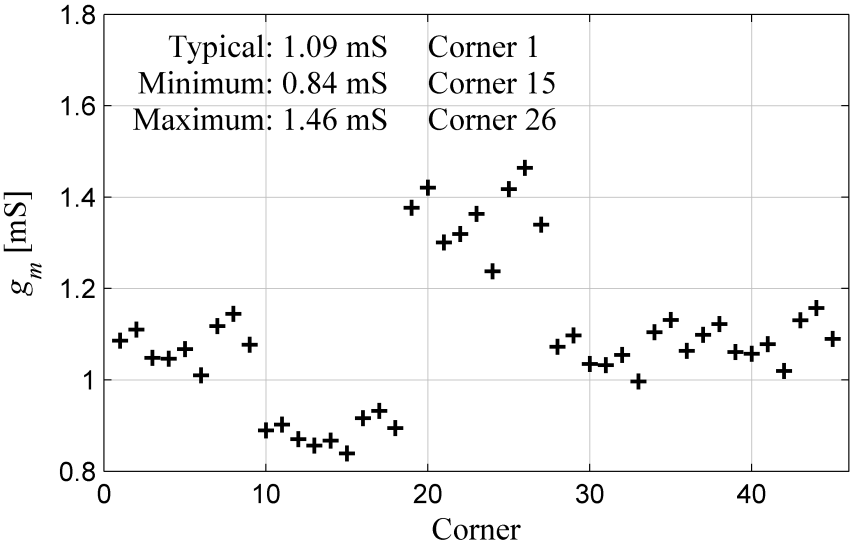

Figure 4.8 Bias circuit output device, NM1, transconductance, g_m, over corners with $PD = 0$ V.

4.1.2.2 Process Variation and Device Mismatch Simulations

As indicated by (4.2), the bias circuitry is sensitive to device mismatch in MN0/MN1 and MP0/MP1 as well as process variation in R0. Monte Carlo simulations were performed on the circuit in order to assess the impact of the process variation and device mismatch on the output bias voltage, V_{bias}, and the output device transconductance, g_m. In order to obtain a statistically significant distribution, 1000 sample simulations were run. In these simulations temperature is held constant at $27°C$ and the supply voltage is held at $V_{DD} = 1$ V.

Figure 4.9 shows the distribution of V_{bias} values while Figure 4.10 shows the distribution of g_m values. Additionally, these figures are overlaid with a normal distribution, labeled Normal, of equivalent mean, μ, and standard deviation, σ, to illustrate that the distributions are indeed Gaussian or Normal. V_{bias} shows an average value close to that of the corners simulations at $\mu = 491$ mV with a standard deviation of $\sigma = 21.3$ mV, a variation of 4.3% as compared to the average. g_m, on the other hand, shows an average value of $\mu = 1.09$ mS and a standard deviation of $\sigma = 0.065$ mS. As indicated by the corners simulations this variation of 6.0% is greater than the variation of V_{bias} primarily due to R0 variation.

Ultimately, the bias circuitry shows robust operation over both corners analysis as well as process and mismatch analysis. This circuit's performance is sufficient to supply the baseline amplifier tail MOSFET with a bias voltage.

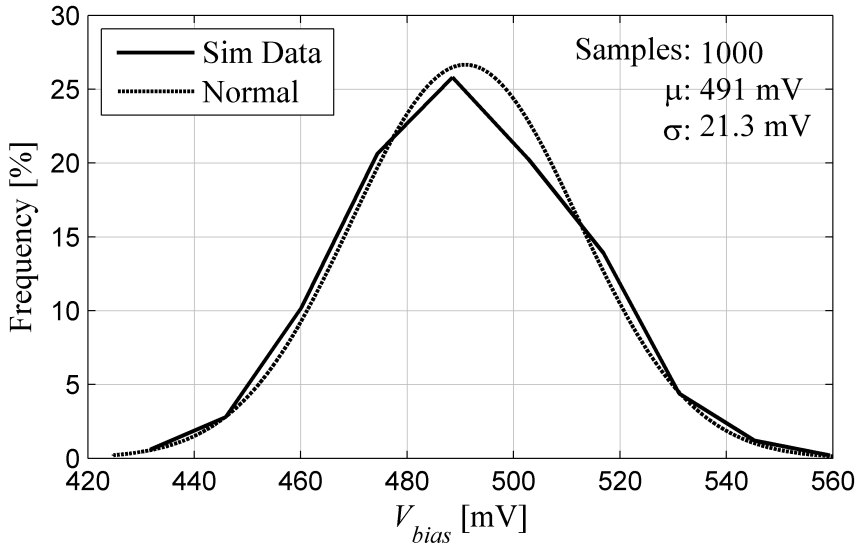

Figure 4.9 Bias circuit bias voltage output, V_{bias}, with process variation and device mismatch at $V_{DD} = 1$ V, $T = 27$℃, and $PD = 0$ V.

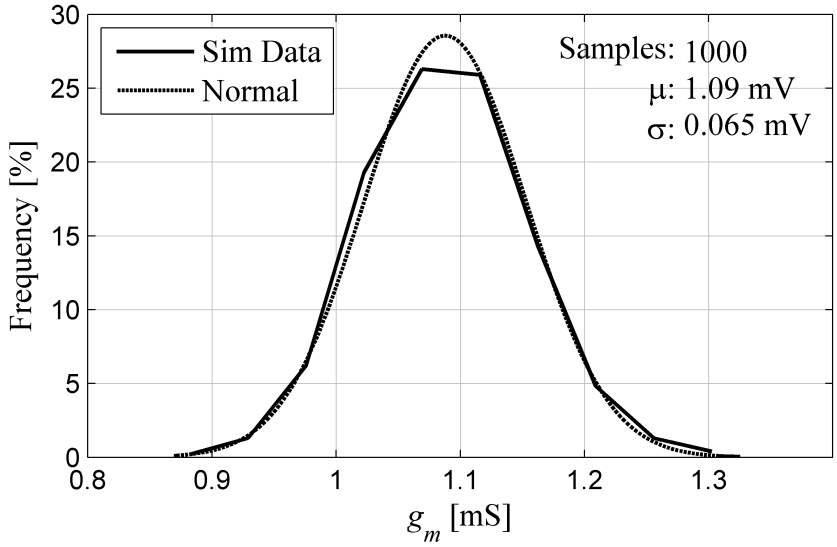

Figure 4.10 Bias circuit output device, NM1, transconductance, g_m, with process variation and device mismatch at $V_{DD} = 1$ V, $T = 27$℃, and $PD = 0$ V.

4.1.3 Baseline Amplifier Simulation Results

The baseline amplifier performance is at the core of the positive feedback amplifier behavior. Therefore its design must be robust and complete if further positive feedback work is to be built on top of it. The final layout of this amplifier is shown in Figure 4.11.

4.1.3.1 Design Considerations

Traditional design considerations generally focus on creating high-gain open-loop amplifiers. This amplifier, however, will be used inside a positive feedback loop. This indicates restrictions on the open-loop gain, A_{DC}, that makes positive feedback feasible. Additionally, the mathematical analysis of the positive feedback differential amplifier has indicated that the gain-bandwidth product of the closed-loop positive feedback will be reduced from that of the open-loop baseline amplifier.

Table 4.5 lists a group of design targets for the baseline amplifier that would be compatible with positive feedback amplifier design methodology derived in Chapter 3.

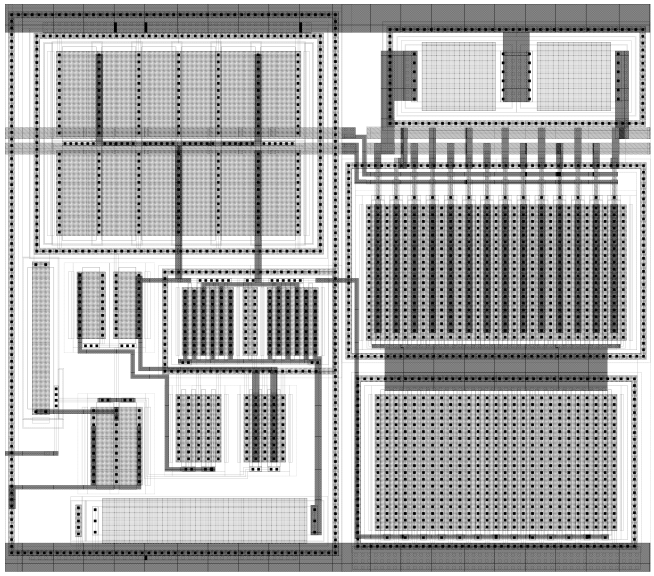

Figure 4.11 Baseline amplifier layout in TSMC 65 nm with low voltage, nominal V_T transistors, dimensions are approximately 23 μm by 20 μm or 460 μm^2.

As per the differential amplifier analysis, A_{DC} must be greater than one, but not so large that the feedback factor range is prohibitively small. The input impedance, R_{in}, of the amplifier is intended to be large enough to be inconsequential in the stability equations. As indicated by (3.54), R_L has an impact on the output impedance R_{out} which, in turn, has an impact on the open-loop gain. Therefore R_{out} must be large enough to achieve the desired A_{DC}, but small enough that the amplifier can drive external loads. Finally, because gain-bandwidth product is lost in the application of positive feedback, the gain-bandwidth product of the open-loop amplifier must be large enough such that the frequency response of the closed-loop amplifier is still useful in GHz type applications.

Under these requirements, the amplifier in Figure 4.2 was designed to be driven by the bias circuitry in Figure 4.3.

4.1.3.2 Corners Simulations

The designed baseline amplifier has to be evaluated in order to define the design parameters of the positive feedback amplifier it will be used in. First, the behavior of the amplifier and its gain are observed across in the input common-mode voltage range, V_{cm}. Essentially, V_{cm} must be large enough that the current source device, MN2, and the input differential pair, MN0 and MN1, have enough gate drive to be turned on. As V_{cm} goes

Table 4.5 Baseline amplifier design targets for compliance with requirements of positive feedback design methodology.

Parameter	Minimum Target	Maximum Target
A_{DC} [V/V]	1.0	10.0
R_{in} [MΩ]	1.0	-
R_{out} [Ω]	100.0	500.0
GBP [GHz]	10.0	-

above this value, the output common-mode voltage will begin to drop. Once the output common-mode voltage is low enough that MN0 and MN1 are no longer in saturation, the gain of the amplifier will begin to drop. This means that there is an optimal region of V_{cm} in which the amplifier has the highest gain. Figure 4.12 shows the DC gain of the baseline amplifier, A_{DC}, as V_{cm} is swept. This figure shows an optimal $V_{cm} = 600$ mV and therefore for subsequent tests, V_{cm} is held at this potential.

At the optimized V_{cm}, the frequency behavior of the amplifier can be observed over corners. Figure 4.13 shows the frequency sweep of the magnitude of $A(s)$ of the baseline amplifier for all 45 corners. Figure 4.14 and Figure 4.15 further break down this data into DC gain values and gain-bandwidth product values, respectively, at each corner. The DC gain remains well controlled with a typical value of $A_{DC} = 12.9$ dB, a minimum of $A_{DC} = 9.53$ dB, and a maximum of $A_{DC} = 13.8$ dB. The gain-bandwidth product is also relatively well controlled with a typical value of $GBP = 44.7$ GHz, a minimum value of

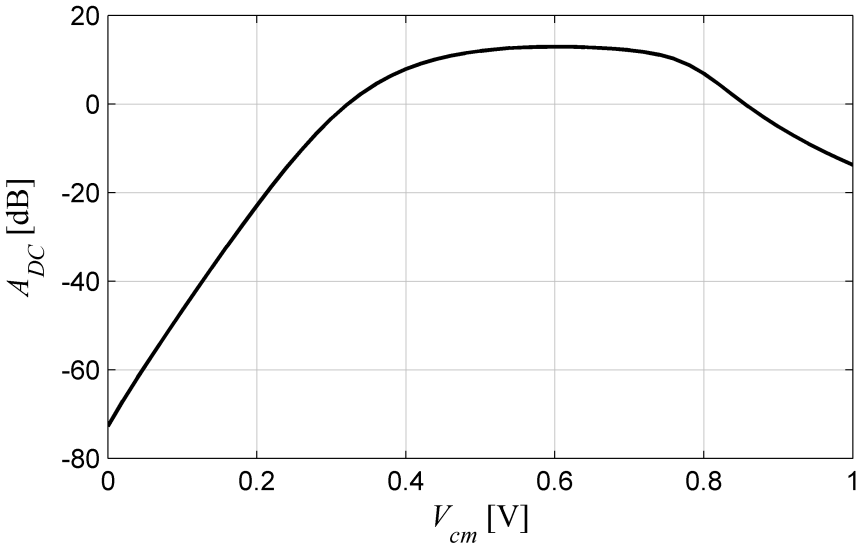

Figure 4.12 Baseline amplifier gain, A_{DC}, versus input common-mode voltage, V_{cm}, at typical process, $V_{DD} = 1$ V, $T = 27$℃, and $PD = 0$ V.

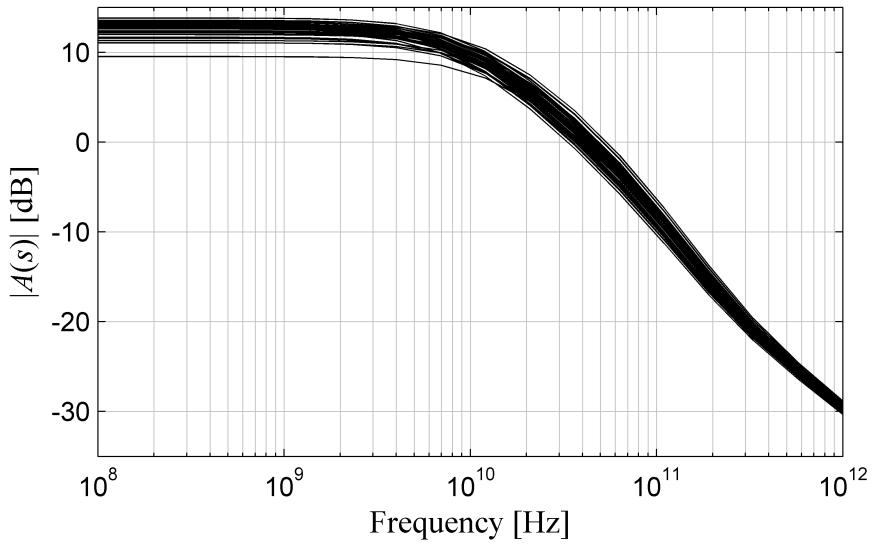

Figure 4.13 Baseline amplifier voltage gain magnitude frequency response over corners with $V_{cm} = 600$ mV and $PD = 0$ V.

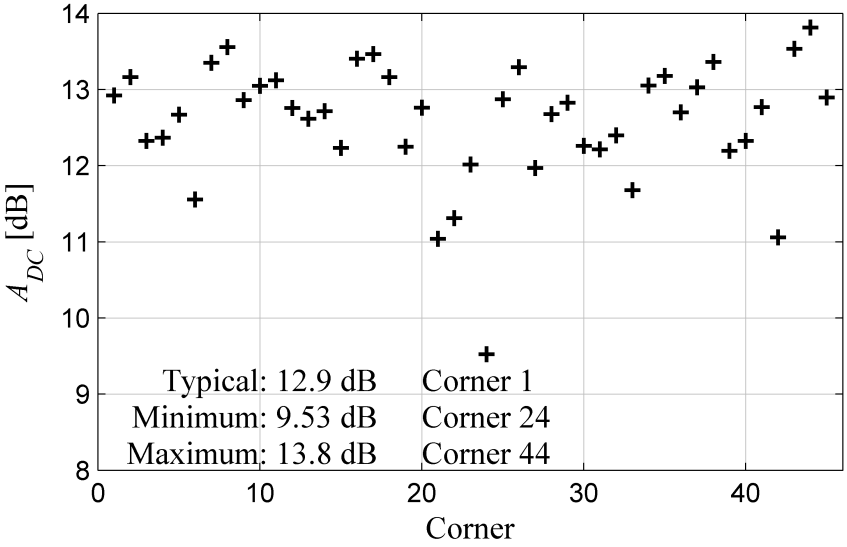

Figure 4.14 Baseline amplifier DC gain magnitude, A_{DC}, over corners with $V_{cm} = 600$ mV and $PD = 0$ V.

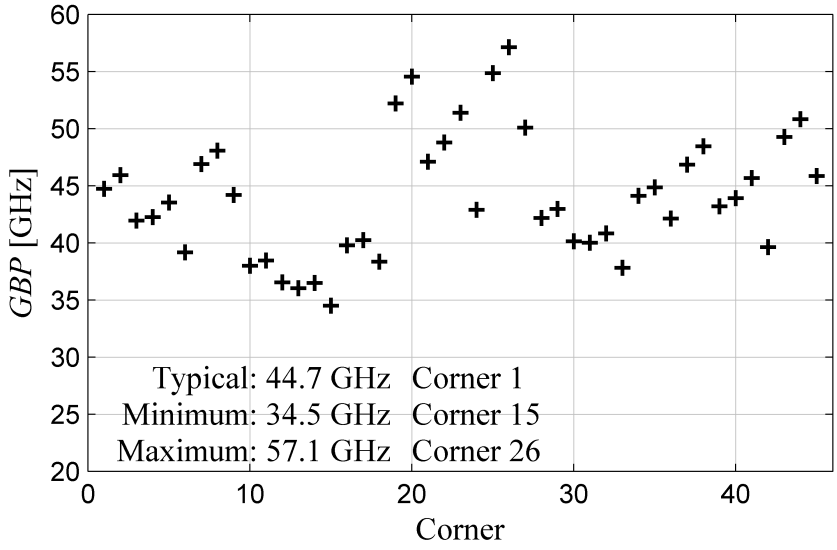

Figure 4.15 Baseline amplifier gain-bandwidth product, GBP, over corners with $V_{cm} = 600$ mV and $PD = 0$ V.

$GBP = 34.5$ GHz and a maximum value of $GBP = 57.1$ GHz.

Finally, the input and output impedances, $Z_{in}(s)$ and $Z_{out}(s)$, of the amplifier are observed. Figure 4.16 shows the magnitude $Z_{in}(s)$ versus frequency for all 45 corners while Figure 4.17 shows the DC magnitude of each corner, $R_{in} = |Z_{in}(0)|$. As the theory predicted, the input impedance is not purely capacitive at low frequencies due to gate current through the input device. Additionally, the high frequency zero in (3.59) due to R_L and C_{gd} can be seen between 100 GHz and 1 THz. The output impedance versus frequency is shown in Figure 4.18 over corners with the corresponding DC output impedance, $R_{out} = |Z_{out}(0)|$, shown in Figure 4.19. The output impedance is primarily dictated by the load resistors, R0 and R1 of Figure 4.2, in parallel with the small signal output impedance of the input differential pair MN0 and MN1, r_o. R_L dominates r_o, but the total output impedance is still slightly less than R_L with a typical value of

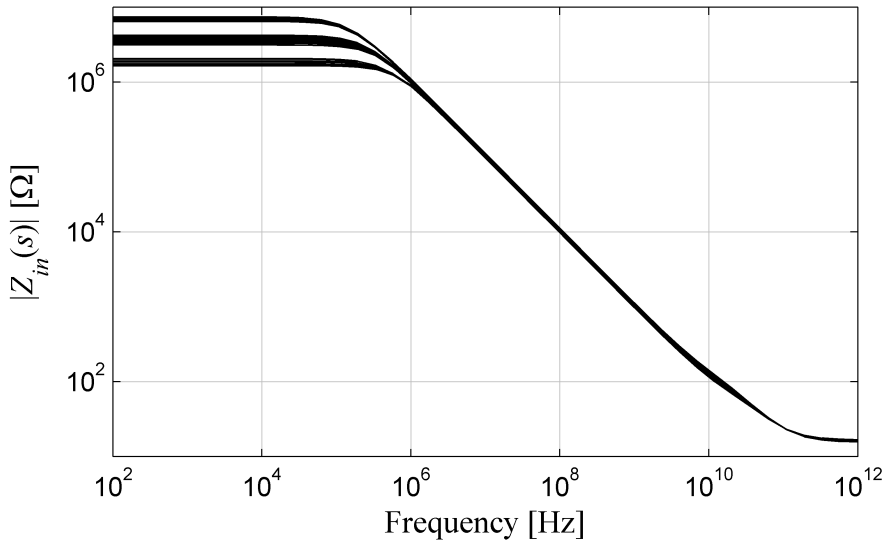

Figure 4.16 Baseline amplifier input impedance magnitude versus frequency over corners with $V_{cm} = 600$ mV and $PD = 0$ V.

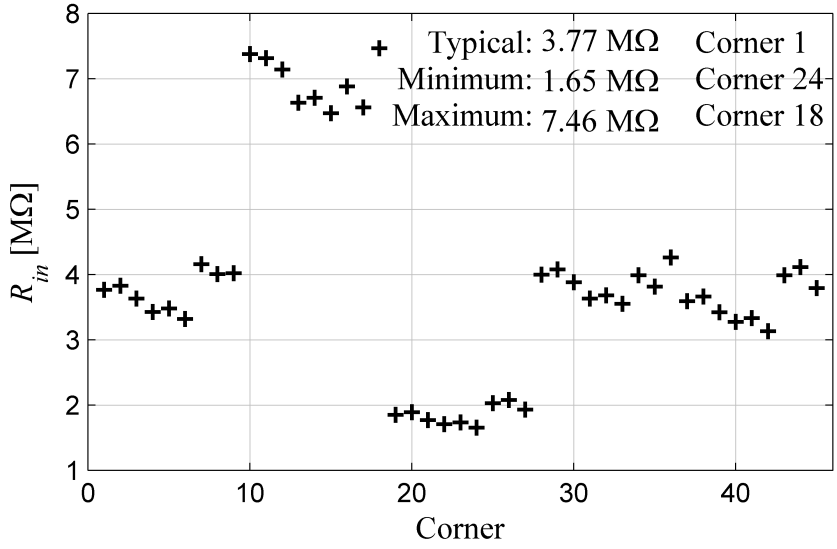

Figure 4.17 Baseline amplifier DC input impedance over corners with $V_{cm} = 600$ mV and $PD = 0$ V.

$R_{out} = 168\,\Omega$, a minimum value of $R_{out} = 106\,\Omega$, and a maximum value of $R_{out} = 215\,\Omega$. This R_L dominance of the output impedance is reinforced by the three distinct groupings of R_{out} values in Figure 4.19 representing the low, typical, and high resistance corners.

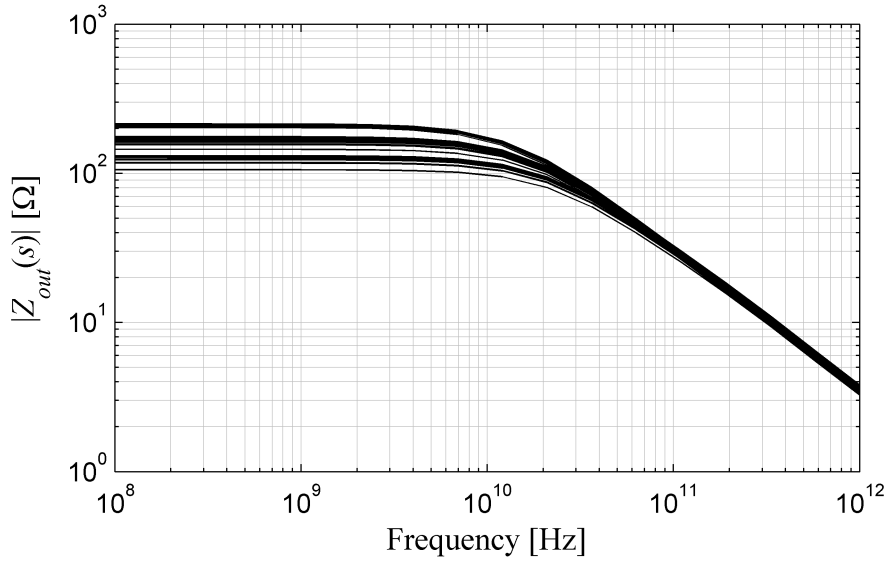

Figure 4.18 Baseline amplifier output impedance magnitude versus frequency over corners with $V_{cm} = 600$ mV and $PD = 0$ V.

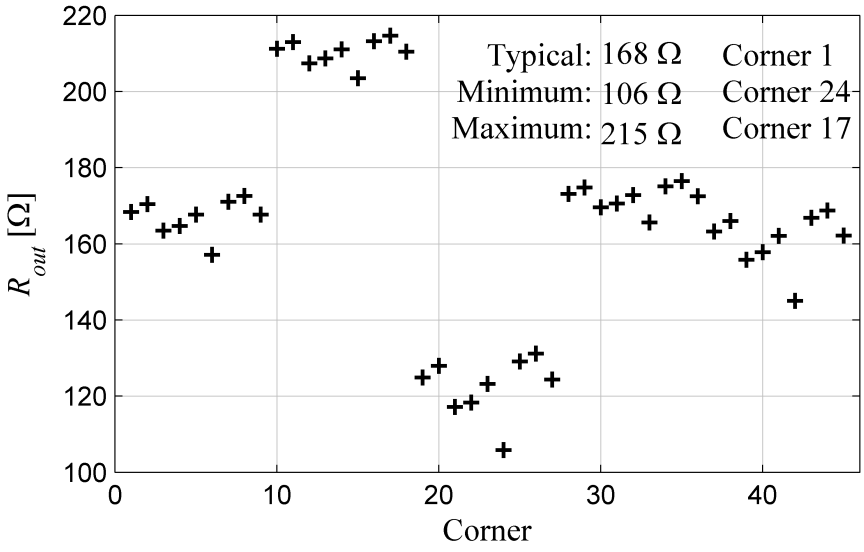

Figure 4.19 Baseline amplifier DC output impedance over corners with $V_{cm} = 600$ mV and $PD = 0$ V.

4.1.3.3 Process Variation and Device Mismatch Simulations

The effects of process variation and device mismatch on the performance of the baseline amplifier are examined by using the Monte Carlo tool in Spectre and ADE. The inputs are held at $V_{cm} = 600$ mV, the supply is fixed at $V_{DD} = 1$ V, and the temperature is held at $T = 27°$C while the process and device matching are allowed to vary in a manner statistically realistic to the manufacturer's actual process.

The resulting variation of the DC gain of the baseline amplifier, A_{DC}, is shown in Figure 4.20. A sample size of 1000 was used and the resulting average DC gain is $\mu = 12.8$ dB with a standard deviation of $\sigma = 0.297$ dB. This behavior correlates to the typical simulation values of the corners analysis very well.

Next, the variation in the gain-bandwidth product, GBP, was observed under the same conditions. 1000 samples were taken and the resulting distribution of GBP is shown in

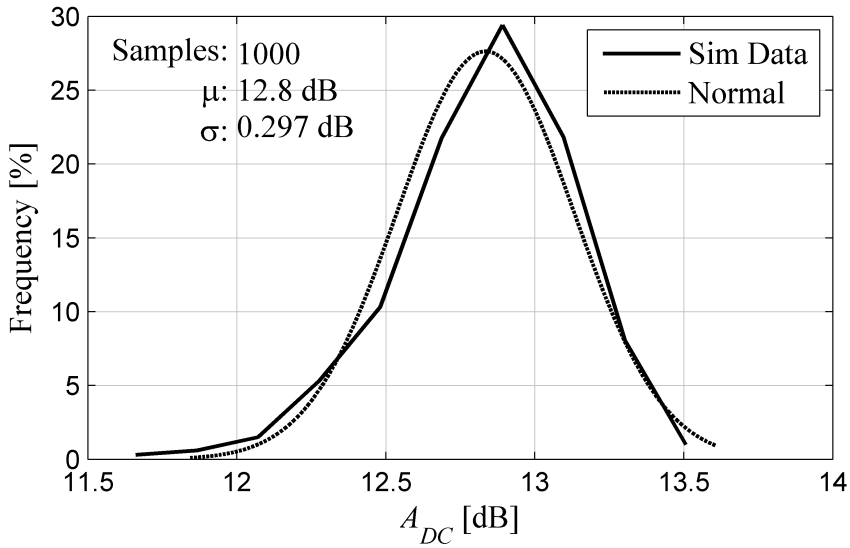

Figure 4.20 Baseline amplifier DC gain with process variation and device mismatch with $V_{cm} = 600$ mV, $PD = 0$ V, $V_{DD} = 1$ V, and $T = 27°C$.

Figure 4.21 with an average value of $\mu = 44.5$ GHz, and a standard deviation of $\sigma = 2.09$ GHz.

Finally, the input-referred offset of the baseline amplifier is observed. Figure 4.22 shows the test bench used in simulation to extract the input-referred offset of the baseline amplifier. The test bench utilizes an auxiliary amplifier, modeled by an ideal voltage-controlled voltage source (VCVS), with very high gain, $A_{DC} = 10^4$. This auxiliary amplifier drives the inputs of the baseline amplifier such that the outputs are equal in voltage. The resulting voltage difference across the input of the baseline amplifier is the measured input-referred offset, V_{os}. This circuit was simulated 1000 times with the resulting V_{os} distribution shown in Figure 4.23. With no process variation and device mismatch, one would expect V_{os} to be zero or at least very small. These simulation results support this theory with an average value very close to zero, $\mu = 49.6$ µV. The variation in the process is shown in the standard deviation of V_{os} of $\sigma = 3.36$ mV. This data will be

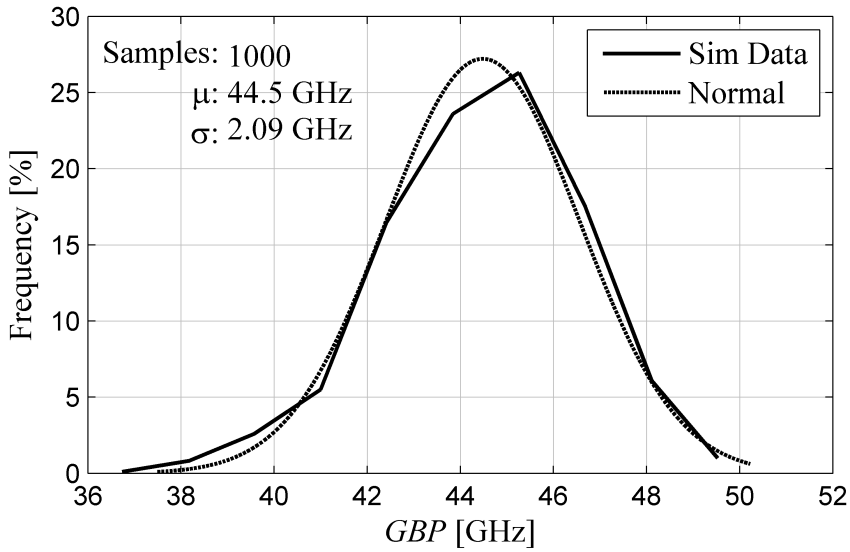

Figure 4.21 Baseline amplifier gain-bandwidth product with process variation and device mismatch with $V_{cm} = 600$ mV, $PD = 0$ V, $V_{DD} = 1$ V, and $T = 27°C$.

used as a basis for comparison against the performance of the positive feedback amplifier that is built around this baseline amplifier in the next section.

Figure 4.22 Baseline amplifier input-referred offset measurement test bench schematic – the high gain auxiliary amplifier drives the input of the opamp such that the outputs are equal

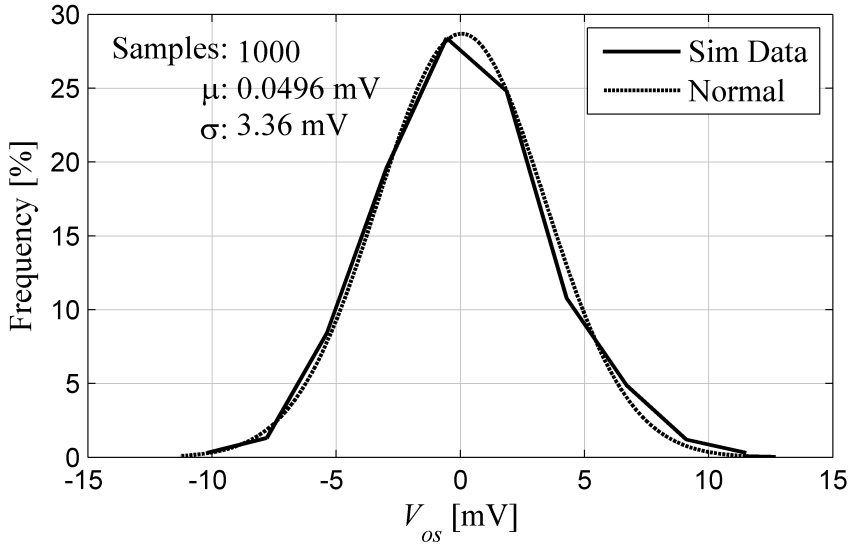

Figure 4.23 Baseline amplifier input-referred offset with process variation and device mismatch with $V_{cm} = 600$ mV, $PD = 0$ V, $V_{DD} = 1$ V, and $T = 27°C$.

4.1.4 Positive Feedback Amplifier Simulation Results

The positive feedback amplifier design utilizes the baseline amplifier designed in Section 4.1.3. The feedback network is built around the baseline amplifier using the stability criteria derived in 3.1.3 and 3.1.4. The final layout for this amplifier is shown in Figure 4.24.

4.1.4.1 Design Considerations

The pertinent parameters of the baseline amplifier designed in Section 4.1.3 are summarized in Table 4.6. To design a value for R_1, (3.57) is evaluated at the typical design point, indicating that $R_1 > 38.0\,\Omega$. Using the worst case value for g_m, however, the minimum value for R_1 becomes $R_1 > 49.8\,\Omega$. To avoid R_1 variation of process, temperature and voltage constraints, a value of $R_1 = 118\,\Omega$ is chosen through iterative simulations over various process corners. Given this R_1 value and the typical baseline

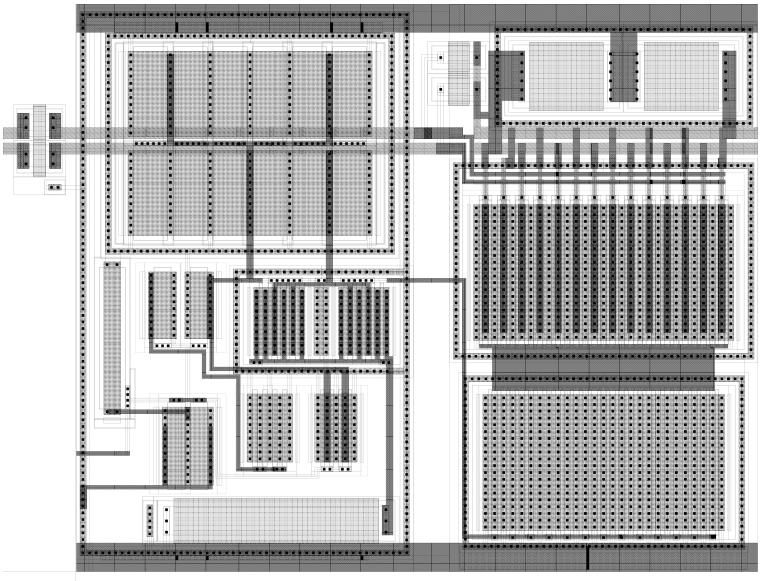

Figure 4.24 Positive feedback amplifier layout with $R_1 = 118\,\Omega$ and $R_2 = 314\,\Omega$ (PFBa) in TSMC 65 nm with low voltage, nominal V_T transistors; dimensions are approximately $24.4\,\mu m$ by $20\,\mu m$ or $488\,\mu m^2$.

Table 4.6 Baseline amplifier critical parameters for positive feedback amplifier design.

Parameter	Typical	Minimum	Maximum
A_{DC} [dB]	12.9	9.53	13.8
R_{in} [MΩ]	3.77	1.65	7.46
R_{out} (R_L) [Ω]	168	106	215
g_m [mS]	26.3	20.1	35.2

amplifier parameters, R_2 can be bound by (3.58) to the value of $R_2 > 235\ \Omega$. Based on the performance around corners, the feedback resistor value must be $R_2 > 245\ \Omega$. This analysis is validated through simulation as shown in Figure 4.25 for various values of R_1. Two variations of the positive feedback amplifier were designed, one with $R_2 = 314\ \Omega$ (PFBa), one with $R_2 = 375\ \Omega$ (PFBb) and both with $R_1 = 118\ \Omega$. These R_2 values were chosen through an iterative simulation process to ensure that amplifier and resistor variation does not cause instability in the positive feedback amplifier.

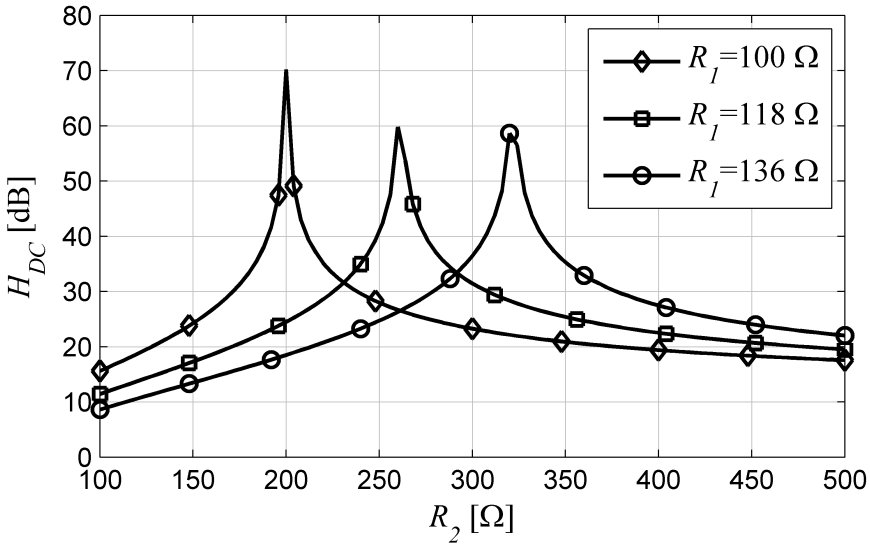

Figure 4.25 Positive feedback amplifier simulation, H_{DC} value versus R_2 for various R_1 values, typical process, $V_{DD} = 1$ V, and $T = 27$°C.

4.1.4.2 Corners Simulations

Similarly to the baseline amplifier, the positive feedback amplifier is characterized over the input common-mode range, V_{cm}. At typical process, voltage, and temperature, Figure 4.26 shows the DC gain of the positive feedback amplifier, H_{DC}, versus V_{cm}. This simulation indicates that the optimal input common-mode voltage is approximately $V_{cm} = 750$ mV. This differs from the baseline amplifier's optimum V_{cm} because of the resistive feedback network. The resistive network causes the input common-mode voltage of the embedded baseline amplifier, $V_{cm,base}$ to differ from the applied common-mode voltage, V_{cm}, through the relationship

$$V_{cm,base} = V_{cm}\frac{R_2}{R_1+R_2} + V_{cm,out}\frac{R_1}{R_1+R_2} \tag{4.4}$$

where $V_{cm,out}$ is the common-mode output voltage for a given input common-mode voltage. Under the assumption that the input differential pair, MN0/MN1, is operating in

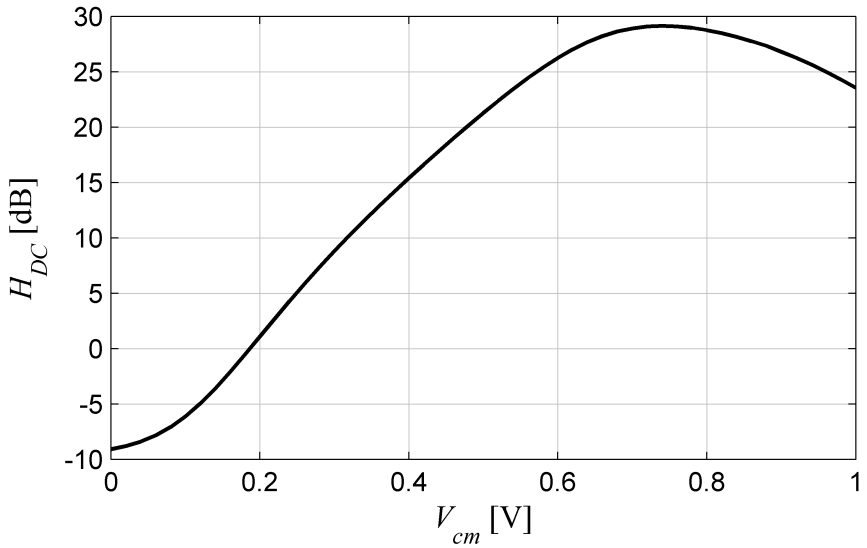

Figure 4.26 Positive feedback amplifier gain, H_{DC}, versus input common-mode voltage, V_{cm}, with $R_1 = 118\ \Omega$, $R_2 = 314\ \Omega$ at typical process, $V_{DD} = 1$ V, $T = 27$°C, and $PD = 0$ V.

saturation, $V_{gs} > V_T$ and $V_{ds} > V_{dssat}$, and the tail current is fixed at I_{tail}, the output common-mode voltage can be calculated as

$$V_{cm,out} = V_{DD}\frac{R_1+R_2}{R_1+R_2+R_L} + V_{cm}\frac{R_L}{R_1+R_2+R_L} - \frac{I_{tail}}{2}\frac{R_L(R_1+R_2)}{R_1+R_2+R_L}. \quad (4.5)$$

At this optimized common-mode voltage of $V_{cm} = 750$ mV, the frequency behavior of the positive feedback amplifier, PFBa, can be observed over corners as shown in Figure 4.27. The DC gain of the PFBa amplifier, H_{DC}, over corners is shown in Figure 4.28 and the gain-bandwidth product, GBP, is shown in Figure 4.29. As expected due to the sensitivity analysis, the spread of the H_{DC} values is increased from that of the baseline amplifier. However, H_{DC} is increased from A_{DC} in every corner case. The gain-bandwidth product also follows the expected behavior, reducing from its baseline amplifier counterpart.

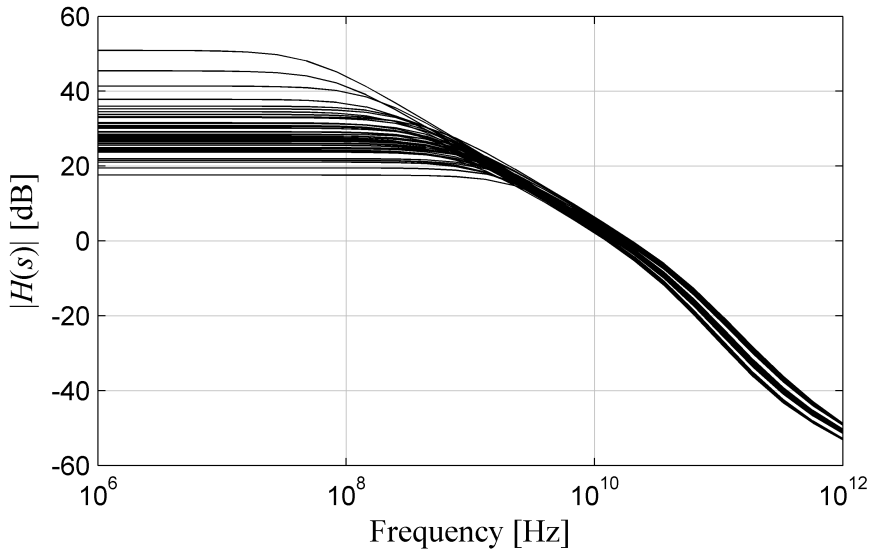

Figure 4.27 Positive feedback amplifier voltage gain magnitude frequency response over corners with $R_1 = 118\ \Omega$, $R_2 = 314\ \Omega$, $V_{cm} = 750$ mV and $PD = 0$ V.

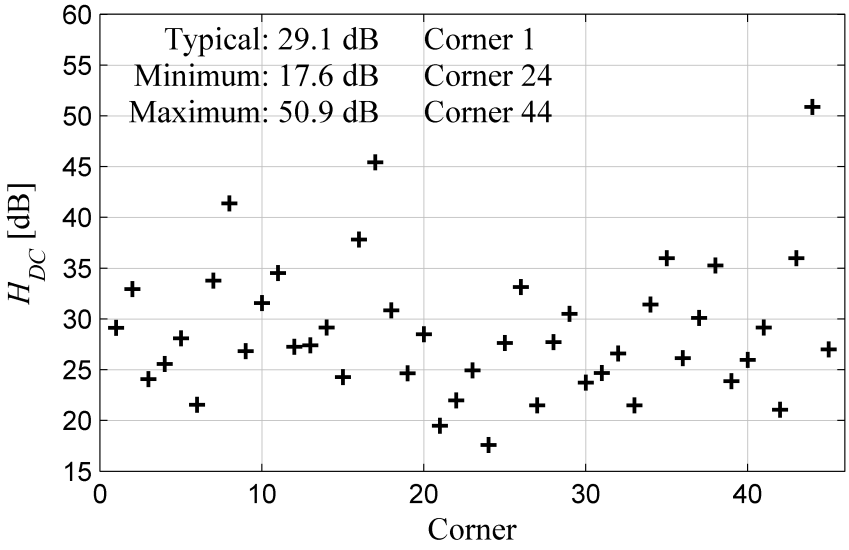

Figure 4.28 Positive feedback amplifier DC gain magnitude, H_{DC}, over corners with $R_1 = 118\ \Omega$, $R_2 = 314\ \Omega$, $V_{cm} = 750$ mV and $PD = 0$ V.

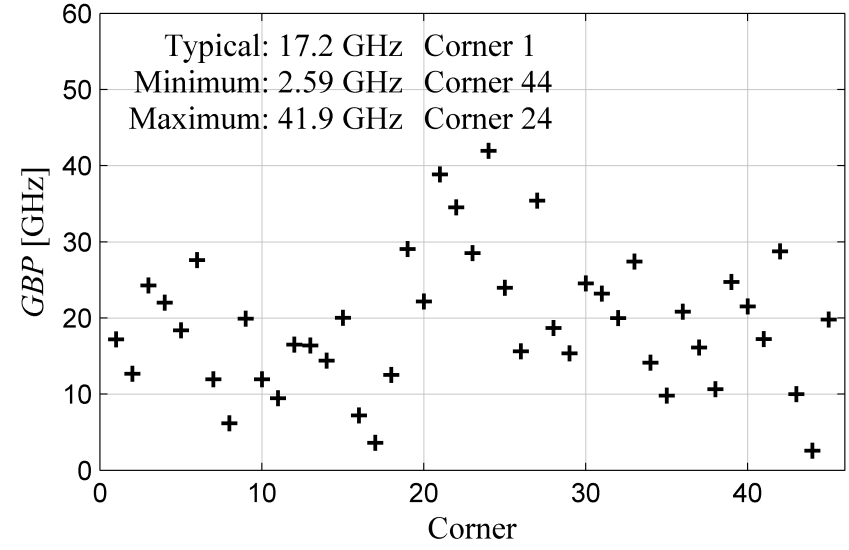

Figure 4.29 Positive feedback amplifier gain-bandwidth product, GBP, over corners with $R_1 = 118\ \Omega$, $R_2 = 314\ \Omega$, $V_{cm} = 750$ mV and $PD = 0$ V.

Finally, the corners analysis includes the observation of the input and output impedance of the positive feedback amplifier. Figure 4.30 shows the magnitude of the input impedance, $Z_{in}(s)$, and Figure 4.31 is a map of the DC values of that impedance, R_{in}. As predicted by the theory, this value is reduced from the baseline amplifier value and is a function of R_1 and the feedback factor β_f. With $R_1 = 118\ \Omega$, the input impedance is typically $R_{in} = 15.6\ \Omega$ with a minimum of $R_{in} = 1.23\ \Omega$ and a maximum of $R_{in} = 44.5\ \Omega$. The output impedance versus frequency, $Z_{out}(s)$, is shown in Figure 4.32 with the corresponding DC values, R_{out}, shown in Figure 4.33 across corners. The positive feedback theory predicts this output impedance is increased from that of its baseline amplifier counterpart. The typical output impedance is $R_{out} = 1.25\ \text{k}\Omega$, with a minimum value of $R_{out} = 298\ \Omega$, and a maximum value of $R_{out} = 14.8\ \text{k}\Omega$.

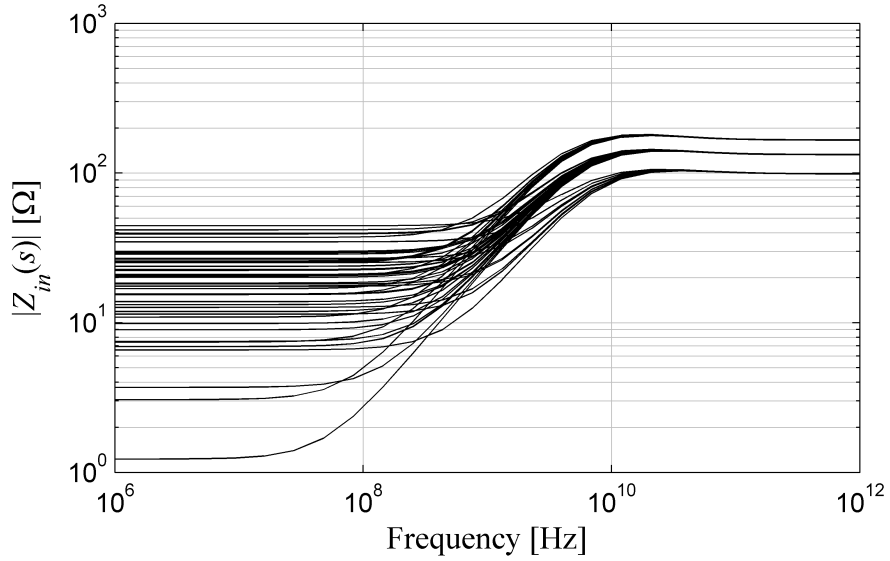

Figure 4.30 Positive feedback amplifier input impedance magnitude versus frequency over corners with $R_1 = 118\ \Omega$, $R_2 = 314\ \Omega$, $V_{cm} = 750$ mV and $PD = 0$ V.

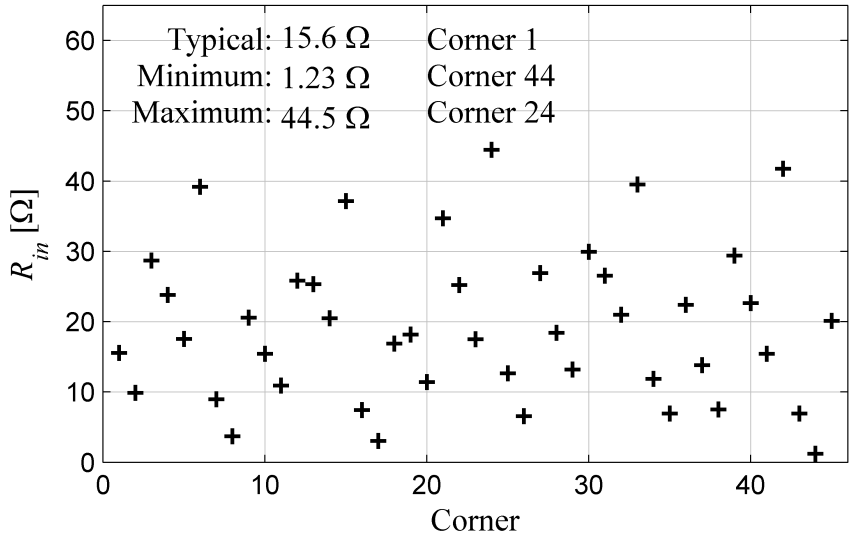

Figure 4.31 Positive feedback amplifier DC input impedance over corners with $R_1 = 118\ \Omega$, $R_2 = 314\ \Omega$, $V_{cm} = 750$ mV and $PD = 0$ V.

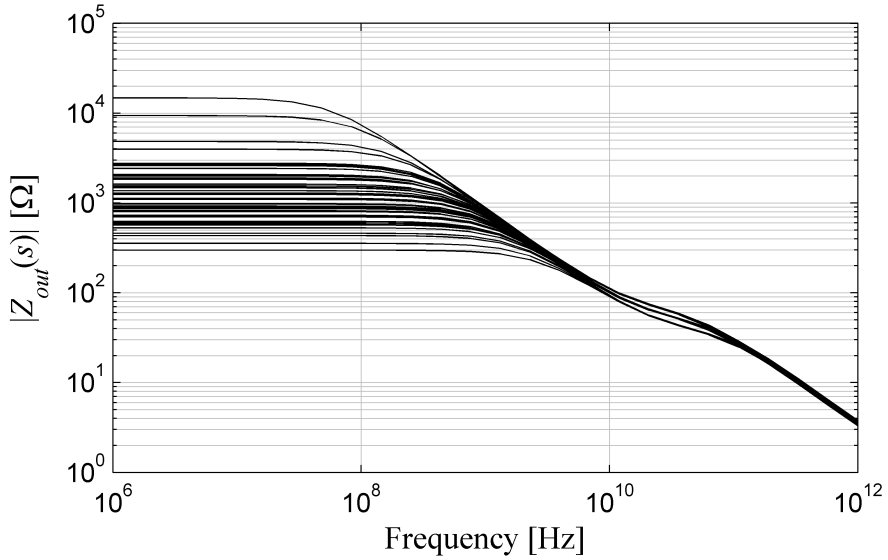

Figure 4.32 Positive feedback amplifier output impedance magnitude versus frequency over corners with $R_1 = 118\ \Omega$, $R_2 = 314\ \Omega$, $V_{cm} = 750$ mV and $PD = 0$ V.

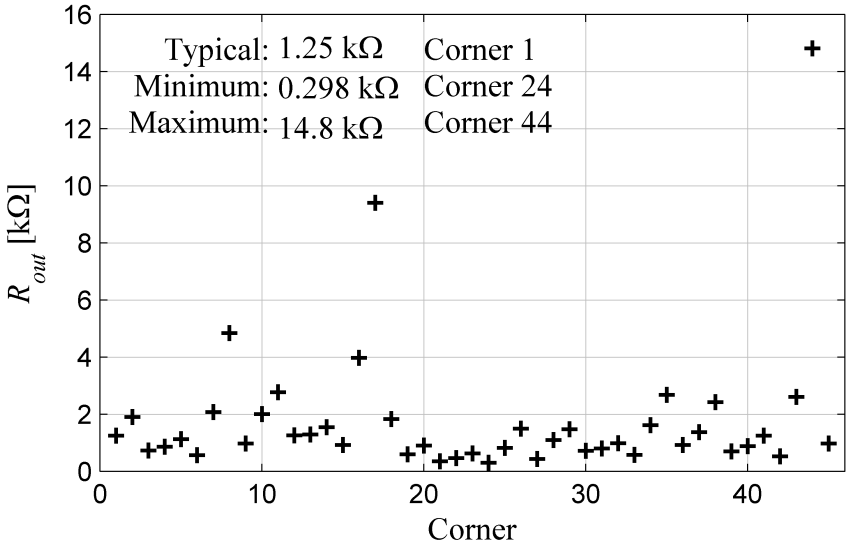

Figure 4.33 Positive feedback amplifier DC output impedance over corners with $R_1 = 118\ \Omega$, $R_2 = 314\ \Omega$, $V_{cm} = 750$ mV and $PD = 0$ V.

4.1.4.3 Process Variation and Device Mismatch Simulations

Like the other circuits, the positive feedback amplifier is also simulated with process variation and device mismatch. The positive feedback amplifier has more components and therefore more opportunities for device mismatch. These Monte Carlo simulations are performed with $V_{DD} = 1$ V, $T = 27$°C, and $PD = 0$ V at the optimized common-mode voltage, $V_{cm} = 750$ mV. The PFBa amplifier with $R_1 = 118\ \Omega$ and $R_2 = 314\ \Omega$ is examined first. The DC gain of the amplifier, H_{DC}, is shown in Figure 4.34. As this figure indicates, the average DC gain is increased from that of the baseline amplifier (from $\mu = 12.8$ dB to $\mu = 23.1$ dB), but the spread of values has also increased from $\sigma = 0.297$ dB to $\sigma = 4.81$ dB. This spread in variation is expected due to the sensitivity analysis in Section 3.2.

The statistical comparison between the baseline and positive feedback amplifiers can be analyzed with the normal difference distribution [88]. This is defined as the statistical

distribution between two normally distributed random variables. The normal difference distribution of the baseline to positive feedback amplifier gain difference has $\mu = \mu_{PFBa} - \mu_{base} = 10.3$ dB and $\sigma = \sqrt{\sigma_{PFBa}^2 + \sigma_{base}^2} = 4.82$ dB. Figure 4.35 shows this normal difference distribution of the positive feedback and baseline amplifier. This figure shows that 98.4% of positive feedback amplifiers show a gain improvement over the baseline amplifier.

The reduction in gain-bandwidth product can be similarly analyzed. Figure 4.36 shows the distribution of 1000 Monte Carlo runs with process variation and device mismatch with $\mu = 26.1$ GHz and $\sigma = 7.19$ GHz. The developed theory predicts that the gain-bandwidth product will be reduced through the application of positive feedback. The normal difference distribution shown in Figure 4.37 has $\mu = -18.4$ GHz and

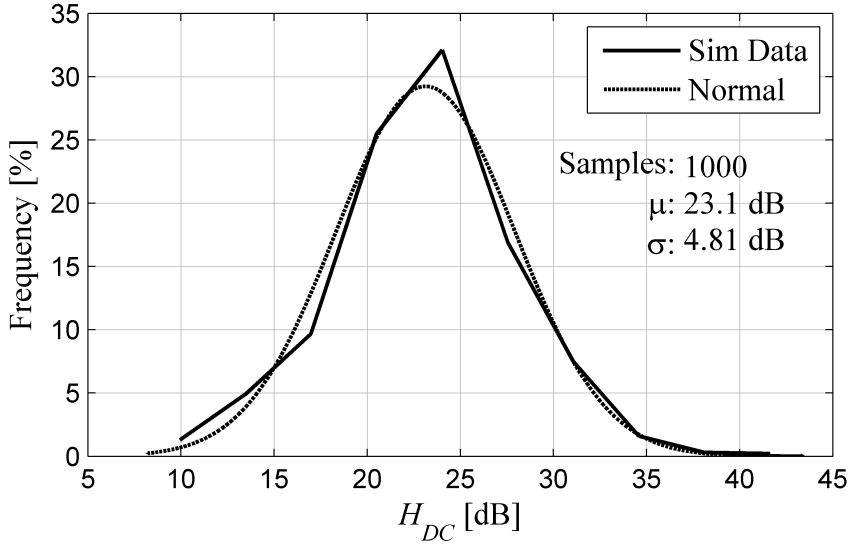

Figure 4.34 Positive feedback amplifier DC gain with process variation and device mismatch with $R_1 = 118\ \Omega$, $R_2 = 314\ \Omega$, $V_{cm} = 750$ mV, $PD = 0$ V, $V_{DD} = 1$ V, and $T = 27°C$.

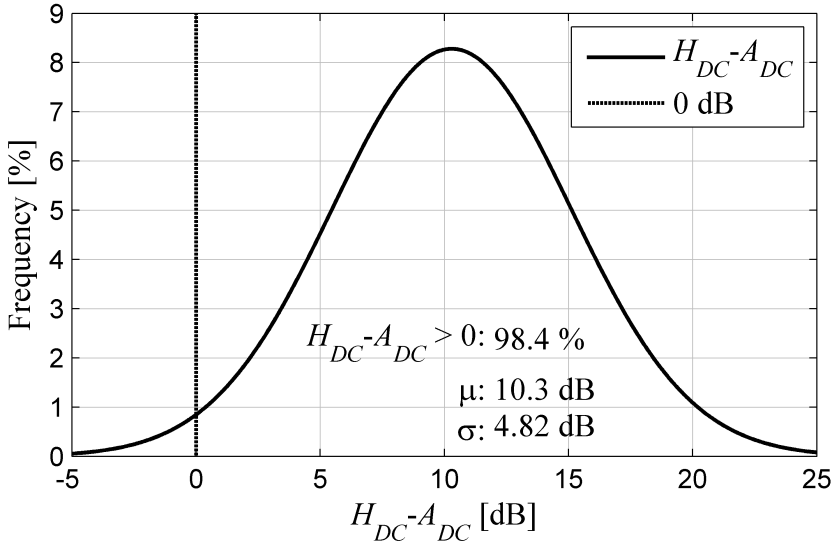

Figure 4.35 Positive feedback amplifier DC gain improvement over baseline with process variation and device mismatch with $R_1 = 118\ \Omega$, $R_2 = 314\ \Omega$, $V_{cm} = 750$ mV, $PD = 0$ V, $V_{DD} = 1$ V, and $T = 27°C$.

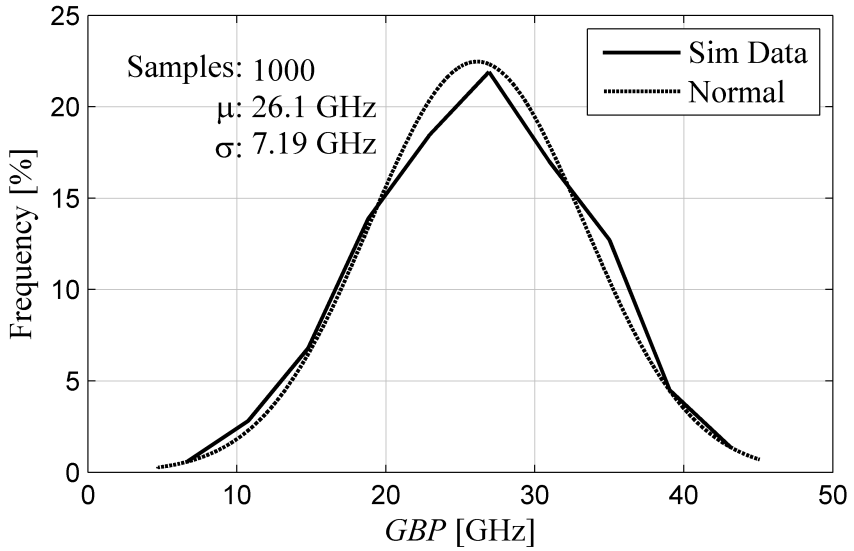

Figure 4.36 Positive feedback amplifier gain-bandwidth product with process variation and device mismatch with $R_1 = 118\ \Omega$, $R_2 = 314\ \Omega$, $V_{cm} = 750$ mV, $PD = 0$ V, $V_{DD} = 1$ V, and $T = 27°C$.

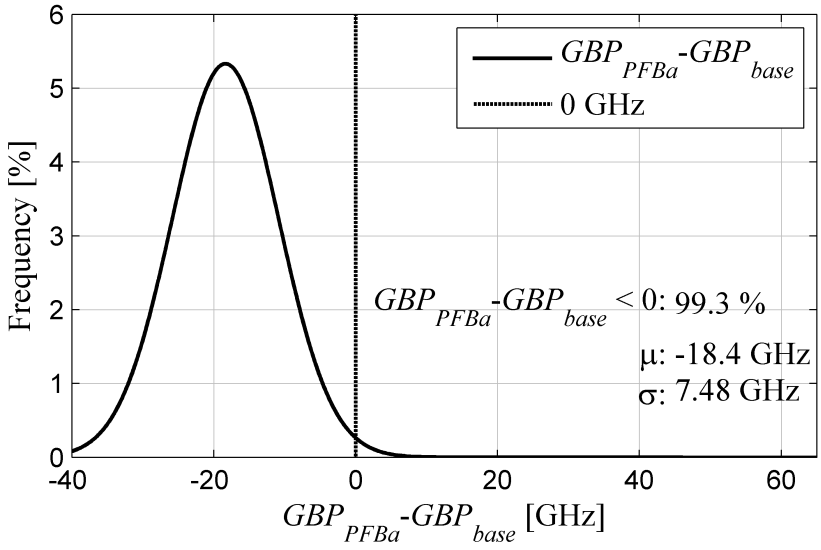

Figure 4.37 Positive feedback amplifier gain-bandwidth product reduction from baseline with process variation and device mismatch with $R_1 = 118\ \Omega$, $R_2 = 314\ \Omega$, $V_{cm} = 750$ mV, $PD = 0$ V, $V_{DD} = 1$ V, and $T = 27°C$.

$\sigma = 7.48$ GHz. Analyzing this normal difference distribution indicates that 99.3% of the positive feedback amplifiers will show degradation in gain-bandwidth product as compared to the baseline amplifier.

The input-referred offset of the positive feedback amplifier is also observed statistically with Monte Carlo simulation and a similar test bench to that of Figure 4.22. Figure 4.38 shows the results of 1000 Monte Carlo simulations with $\mu = -58.8$ μV and $\sigma = 11$ mV. The spread of this distribution is increased as compared to that of the baseline amplifier as expected by the developed theory in Section 3.1.4.2.

Previous simulations have not required a measure of stability. The positive feedback amplifier, PFBa, with process variation and device mismatch, however, shows some unstable behavior. Resistor mismatch causes hysteresis in the DC behavior of the

amplifier. Hysteresis is the direction-dependent threshold voltage of an amplifier or comparator. This means that a negative-to-positive input transition will cause the output to switch state at a different input voltage than a positive-to-negative input transition. While this is not a direct indication of instability, it is undesired operation in a linear amplifier. Figure 4.39 shows the hysteresis of the DC sweeps in the positive feedback amplifier measured as the difference in negative-to-positive and positive-to-negative input transitions, $V_{hyst} = |V_{tnp} - V_{tpn}|$.

Over the course of 1000 Monte Carlo simulations, 17 simulations, or 1.7%, show non-zero hysteresis. While hysteresis is undesirable, a more pertinent concern is the existence of right-half-plane poles. In this case, the DC phase of the positive feedback amplifier would be $\angle H_{DC} = \pm 180°$. Figure 4.40 shows the results of the measurement over the 1000 Monte Carlo simulations. In this case, 2 of the 1000 runs, or 0.2% show

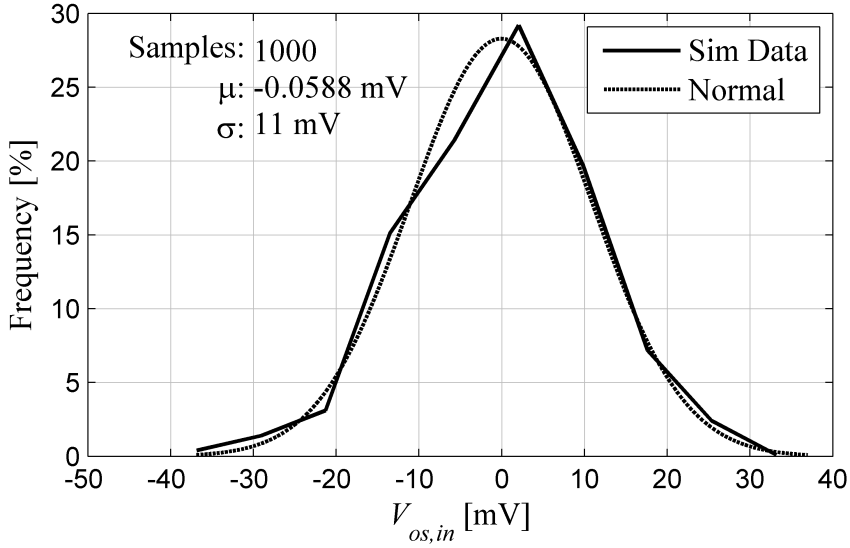

Figure 4.38 Positive feedback amplifier input-referred offset with process variation and device mismatch with $R_1 = 118\ \Omega$, $R_2 = 314\ \Omega$, $V_{cm} = 750$ mV, $PD = 0$ V, $V_{DD} = 1$ V, and $T = 27°C$.

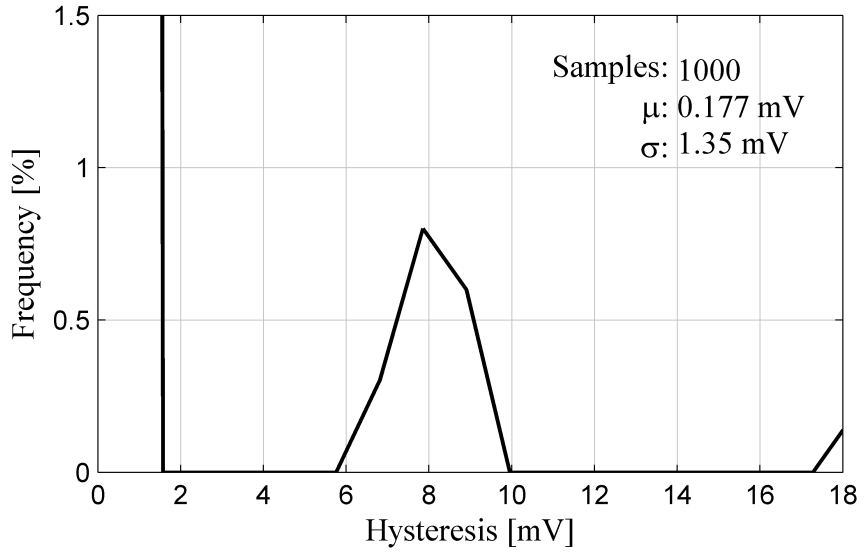

Figure 4.39 Positive feedback amplifier hysteresis simulations with process variation and device mismatch with $R_1 = 118\ \Omega$, $R_2 = 314\ \Omega$, $V_{cm} = 750$ mV, $PD = 0$ V, $V_{DD} = 1$ V, and $T = 27°C$.

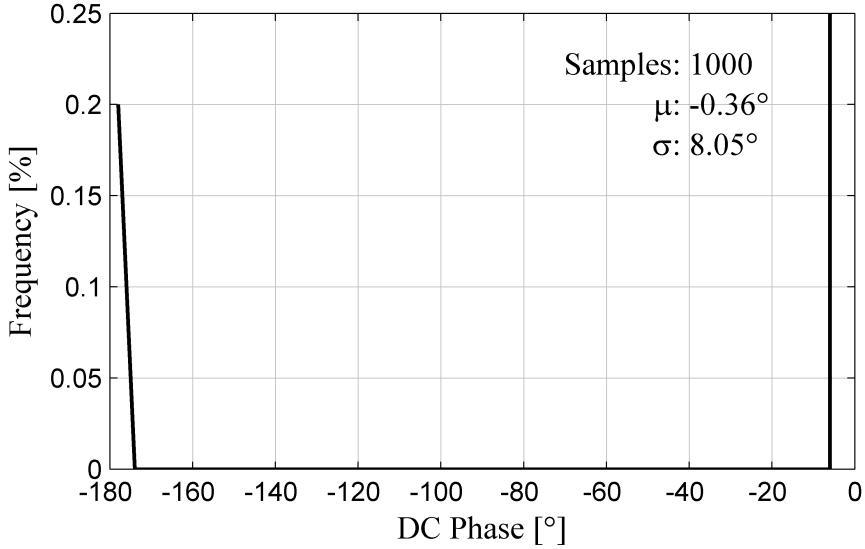

Figure 4.40 Positive feedback amplifier simulation DC phase measurement for stability indication with process variation and device mismatch with $R_1 = 118\ \Omega$, $R_2 = 314\ \Omega$, $V_{cm} = 750$ mV, $PD = 0$ V, $V_{DD} = 1$ V, and $T = 27°C$.

$\angle H_{DC} = -180°$ and are therefore unstable systems. In the PFBa cases, $R_2 = 314\ \Omega$ is pushed closer to the unstable point of the amplifier, $R_2 > 235\ \Omega$, than PFBb. To verify that the unstable Monte Carlo runs are the result of R_2 being too close to the stability criteria, a second amplifier, PFBb, with $R_2 = 375\ \Omega$ is simulated under the same criteria. Figure 4.41 shows the result of 1000 Monte Carlo simulations. As expected, with a larger R_2 value, the DC gain is reduced from that of PFBa with $\mu = 22$ dB. The distribution spread, however, is reduced to $\sigma = 2.75$ dB. As a result, the normal difference distribution shown in Figure 4.42 shows a lower likelihood of die showing no gain improvement. 99.95% of die will show gain improvement over the baseline amplifiers. Hysteresis and stability of the PFBb amplifier are also improved. Figure 4.43 shows only 1 case in 1000 in which there is hysteresis. Figure 4.44 shows zero cases in which the DC

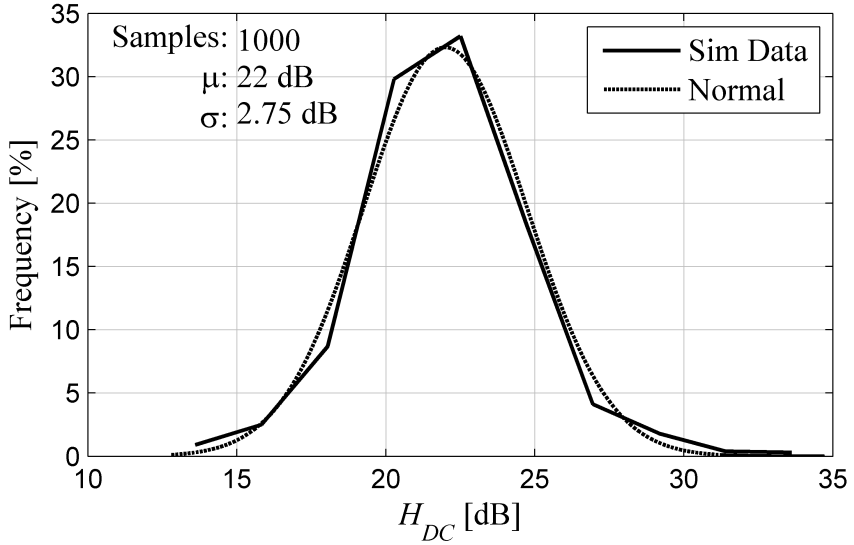

Figure 4.41 Positive feedback amplifier gain with process variation and device mismatch with $R_1 = 118\ \Omega$, $R_2 = 375\ \Omega$, $V_{cm} = 750$ mV, $PD = 0$ V, $V_{DD} = 1$ V, and $T = 27°C$.

Figure 4.42 Positive feedback amplifier DC gain improvement over baseline with process variation and device mismatch with $R_1 = 118\ \Omega$, $R_2 = 375\ \Omega$, $V_{cm} = 750$ mV, $PD = 0$ V , $V_{DD} = 1$ V, and $T = 27°C$.

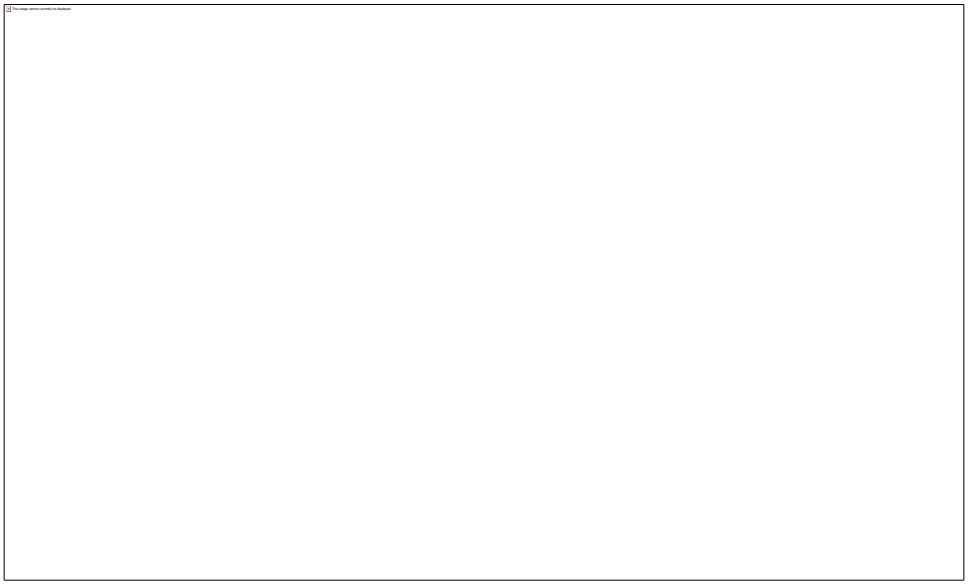

Figure 4.43 Positive feedback amplifier hysteresis simulations with process variation and device mismatch with $R_1 = 118\ \Omega$, $R_2 = 375\ \Omega$, $V_{cm} = 750$ mV, $PD = 0$ V, $V_{DD} = 1$ V, and $T = 27°C$.

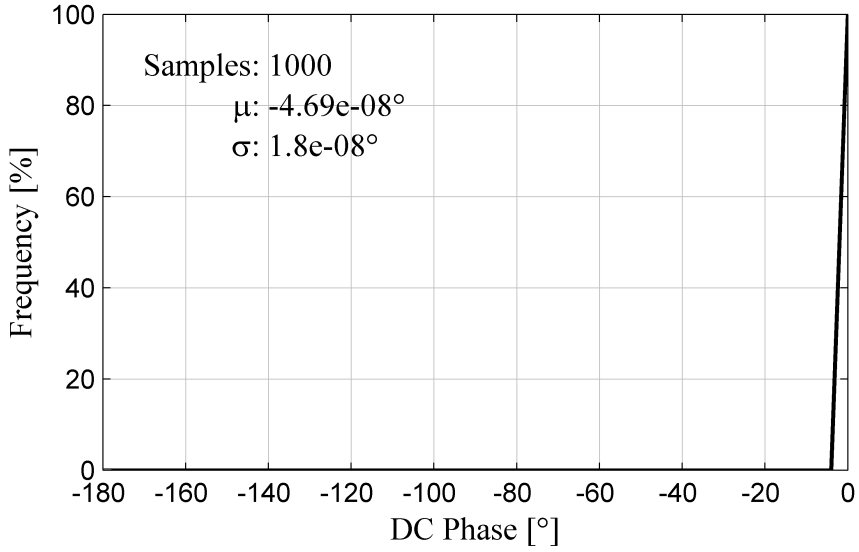

Figure 4.44 Positive feedback amplifier simulation DC phase measurement for stability indication with process variation and device mismatch with $R_1 = 118\ \Omega$, $R_2 = 375\ \Omega$, $V_{cm} = 750$ mV, $PD = 0$ V, $V_{DD} = 1$ V, and $T = 27°C$.

phase is $\angle H_{DC} = -180°$, therefore 100% of the amplifiers are stable.

4.2 Silicon Results

The amplifiers designed in the previous section were fabricated in the TSMC 65 nm process using low-voltage, nominal V_T transistors. Three variants of amplifiers were designed and fabricated: the baseline amplifier, a positive feedback with $R_1 = 118\ \Omega$, and $R_2 = 314\ \Omega$ (PFBa), and a positive feedback amplifier with $R_1 = 118\ \Omega$ and $R_2 = 375\ \Omega$ (PFBb). These fabricated amplifiers were tested by two methodologies: AC and DC tests. The purpose, setup, measurement methodology, and results for each are described in this section.

The fabricated amplifier is shown in Figure 4.45. Because of the nine layers of metallization in this process, it is impossible to see the actual circuitry underneath, but the basic form of the amplifier is outlined. Figure 4.46 shows the whole test structures with I/O pads included. Power, V_{DD}, and ground, GND, and the control signal, PD, are

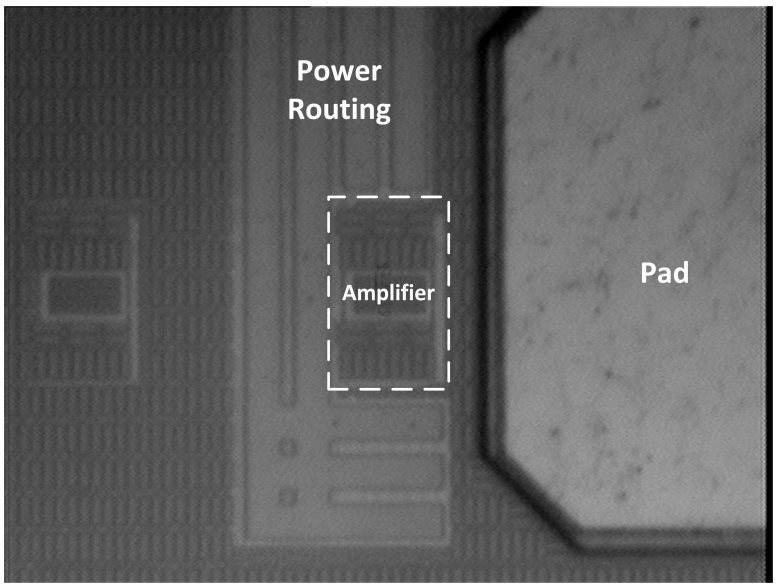

Figure 4.45 Baseline amplifier silicon micrograph of fabricated TSMC 65 nm with power routing and top level metallization visible.

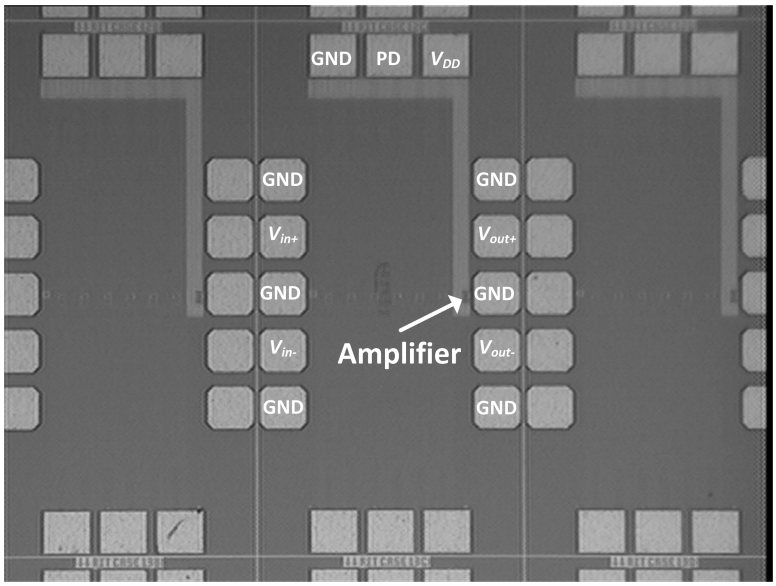

Figure 4.46 Amplifier test structure micrograph of fabricated TSMC 65 nm test chip.

supplied from a series of pads at the top of the structure. The input and output signals are connected through GSGSG (ground-signal-ground-signal-ground) microprobe connection with the inputs on the left side and outputs on the right side. The bottom row of pads is unused. Figure 4.47 shows a single test structure in the context of the entire test wafer with other amplifier test structures surrounding it.

4.2.1 DC Tests

The purpose of the DC test was to observe general functionality of the amplifiers as well as provide a general sense of the magnitude of gains to be expected. Furthermore, this is a fast test to implement and run that is easily automated so an entire wafer of die were tested in order to provide some statistically meaningful results.

4.2.1.1 Test Setup

To evaluate DC performance of the amplifier, the test setup in Figure 4.48 was used. The DUT was driven and evaluated with an HP4156A Precision Semiconductor Parameter

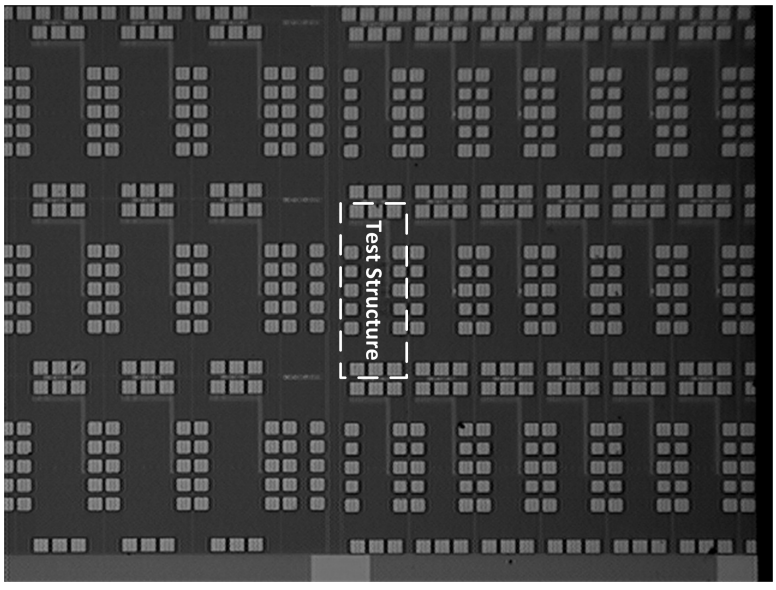

Figure 4.47 Array of amplifier test structures micrograph of fabricated TSMC 65 nm test chip.

Analyzer (4156A). Data was captured with the HP4156A and transferred to a computer to be post processed and analyzed in MATLAB.

4.2.1.2 Measurement Methodology

The positive amplifier terminal, V_{in+}, was driven from $V_{cm} - 100\,\text{mV}$ to $V_{cm} + 100\,\text{mV}$ in 1 mV steps at three common-mode voltages (350 mV, 500 mV, and 750 mV) on the negative terminal, V_{in-}. The derivative of the total output voltage, $V_{out+} - V_{out-}$, with respect to the total input voltage, $V_{in+} - V_{in-}$, corresponds to the DC gain of the amplifier as in

$$A_{DC} = \mathrm{H_{DC}} = \frac{\delta(V_{out+} - V_{out-})}{\delta(V_{in+} - V_{in-})}. \tag{4.6}$$

This simplified test can be run quickly and could be performed across an entire wafer to obtain trends of DC gain.

4.2.1.3 Results

This data was compiled over an entire wafer (92 die) and is summarized in Table 4.7.

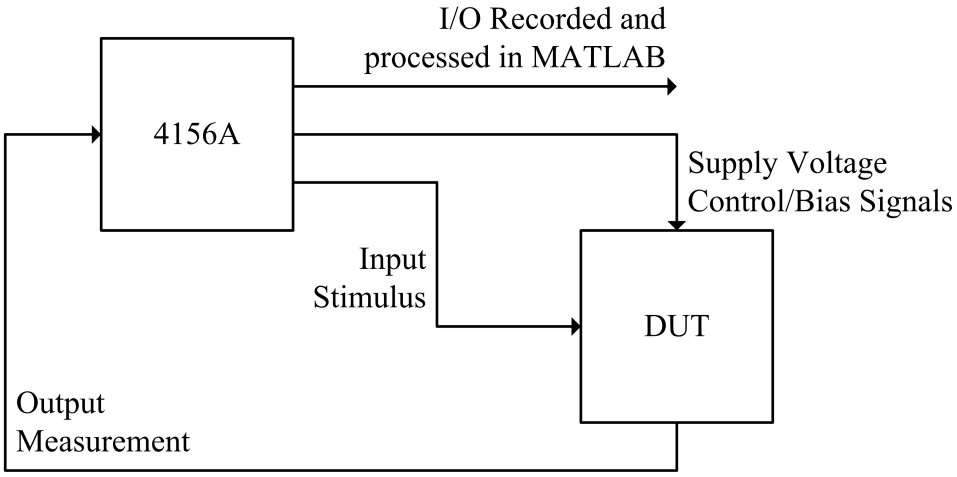

Figure 4.48 DC measurement test bench with semiconductor parameter analyzer driving inputs and collecting data for post processing in MATLAB

Table 4.7 DC sweep results summary

Amplifier	V_{cm} (mV)	Mean Gain (dB)	Max Gain (dB)	Std Dev (dB)
Baseline	350	10.71	16.44	2.12
	500	13.55	14.53	1.91
	750	12.68	14.47	1.48
$R_2 = 375\ \Omega$	350	36.08	51.78	39.8
	500	51.50	52.40	22.1[a]
	750	51.81	55.06	15.4[a]
$R_2 = 314\ \Omega$	350	46.34	52.25	27.0[a]
	500	52.77	54.59	21.0[a]
	750	53.32	54.58	14.3[a]

a – measurements likely skewed low by test limitations

Across the entire wafer there were 3 non-operational die (96.7% yield) and these were not included in the statistics. There was no other sorting of the data based on amplifier performance.

The baseline amplifier corresponds very closely on average to the expected simulation results with 13.55 dB DC gain. Figure 4.49 and Figure 4.50 show a typical DC transfer function and gain of a baseline amplifier. All of the positive feedback amplifiers showed significant increases in gain over the baseline amplifier as predicted by the positive feedback theory. Under some R_2 and V_{cm} conditions, this gain increase was in excess of 38 dB. Figure 4.51 and Figure 4.52 show a typical DC transfer function and gain of a PFBa amplifier and Figure 4.53 and Figure 4.54 show PFBb performance. These maximum measured gain increases, however, are limited by the minimum voltage step of 1 mV of the HP4156A. With a 1 V supply voltage and an output voltage swing of approximately 600 mV for this amplifier, a 1 mV step corresponds to a maximum

possible DC gain measurement of approximately 55 dB. This limitation can clearly be seen in the maximum gain column of Table 4.7. Based on histograms of the data, the amplifier and V_{cm} conditions that exhibit clear statistical skew due to this measurement limitation are marked as such in the table.

The increase in gain is also accompanied by an increase in standard deviation of that gain across the wafer. While part of this standard deviation increase is due to the addition of four new components in the circuitry, most of it is due to the increased sensitivity of the DC gain to variation in R_1 and R_2 values as Ψ approaches zero. While this statistical spreading of the gain is undesirable, the increases in gain more than compensate for the increases in standard deviation. For reasons mentioned above, most of the positive feedback statistics are skewed because of the measurement limitations. However, one case which is not skewed based on observation of the data's histogram is the positive feedback amplifier $R_2 = 375\,\Omega$ with $V_{IN,CM} = 350$ mV. Under this condition, the standard deviation was increased from 2.12 dB to 22.1 dB with an increase in mean gain from 10.71 dB to 36.08 dB, an increase of over 25 dB. The normal difference distribution of these two distributions has a mean of 35.60 dB and a standard deviation of 116.83%. While this spread seems significant, this distribution shows more than 80% of the amplifiers are expected to have DC gain enhancements and over 76% of the amplifiers will have a gain enhancement of 20 dB or more (i.e., the gain is enhanced by at least an order of magnitude).

To describe why so many of the amplifiers in Table 4.7 show measurement limitations, the wafer acceptance test (WAT) data provided by TSMC was used. This WAT data

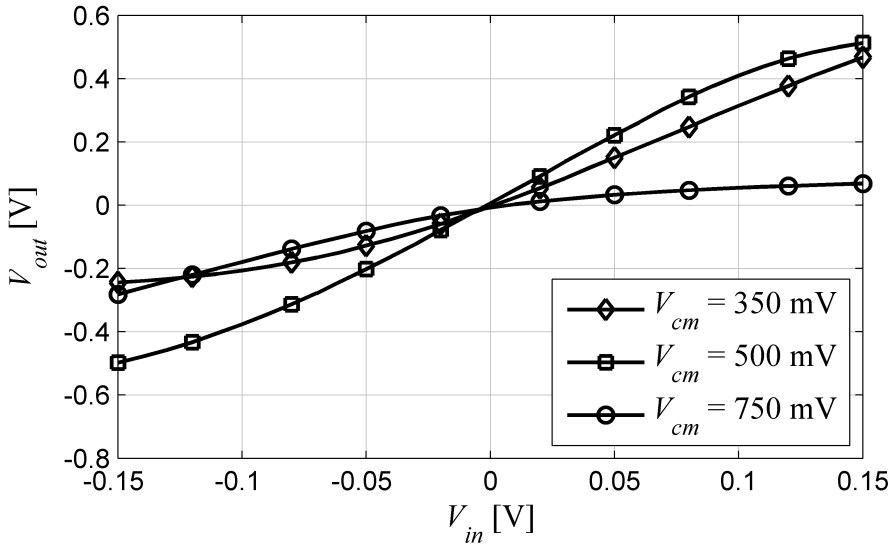

Figure 4.49 Silicon measurement of baseline amplifier DC sweep at multiple input common-mode voltages, V_{cm}.

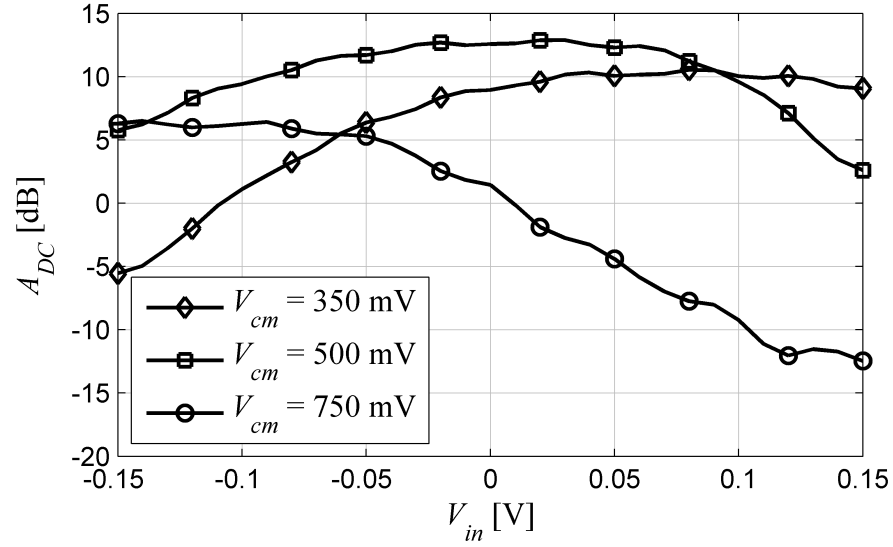

Figure 4.50 Silicon measurement of baseline amplifier DC sweep gain at multiple input common-mode voltages, V_{cm}.

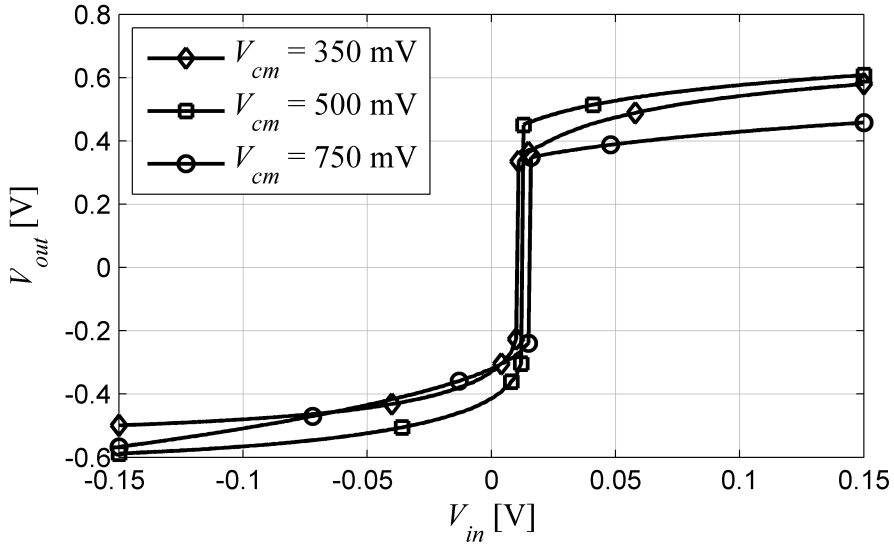

Figure 4.51 Silicon measurement of positive feedback amplifier with $R_1 = 118\ \Omega$ and $R_2 = 314\ \Omega$ (PFBa) DC sweep at multiple input common-mode voltages, V_{cm}.

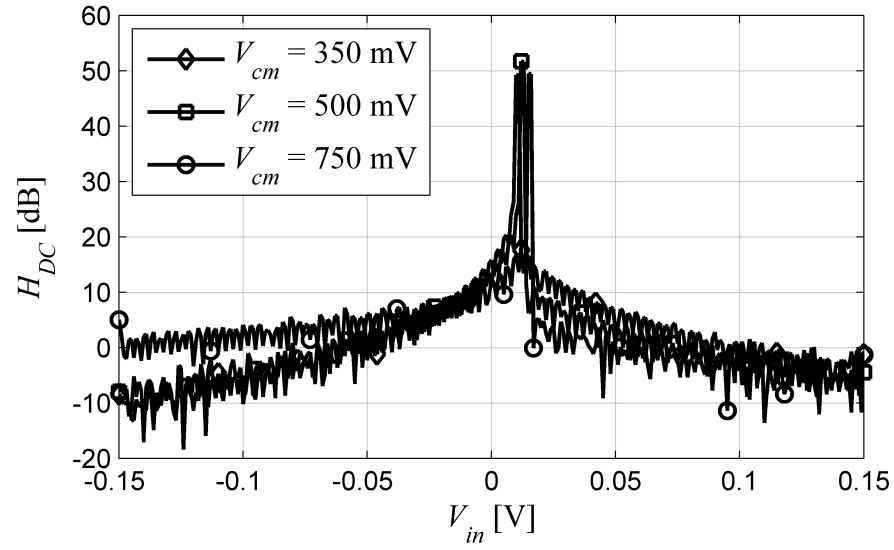

Figure 4.52 Silicon measurement of positive feedback amplifier with $R_1 = 118\ \Omega$ and $R_2 = 314\ \Omega$ (PFBa) DC sweep gain at multiple input common-mode voltages, V_{cm}.

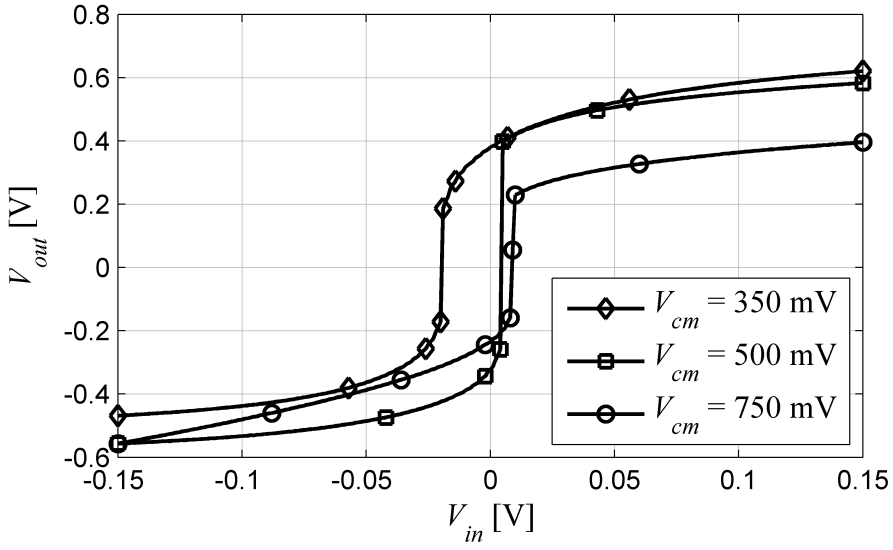

Figure 4.53 Silicon measurement of positive feedback amplifier with $R_1 = 118\ \Omega$ and $R_2 = 375\ \Omega$ (PFBa) DC sweep at multiple input common-mode voltages, V_{cm}.

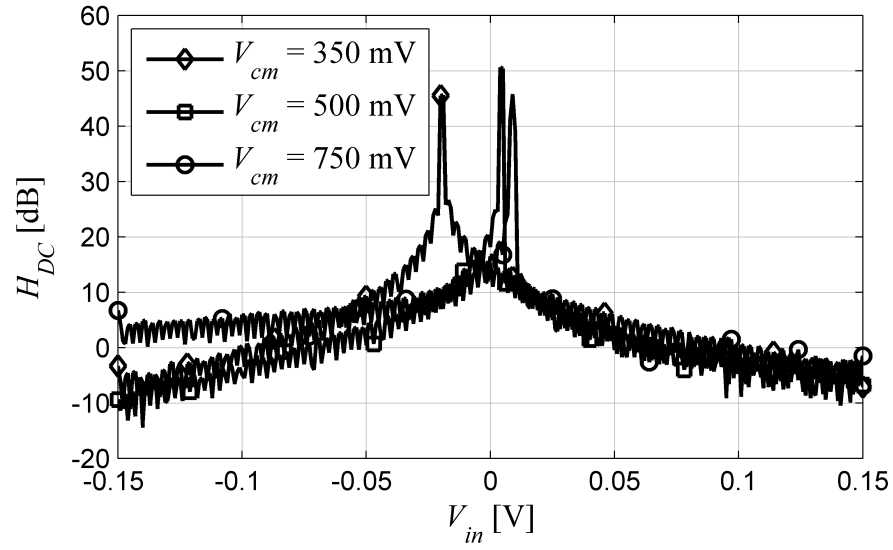

Figure 4.54 Silicon measurement of positive feedback amplifier with $R_1 = 118\ \Omega$ and $R_2 = 375\ \Omega$ (PFBa) DC sweep gain at multiple input common-mode voltages, V_{cm}.

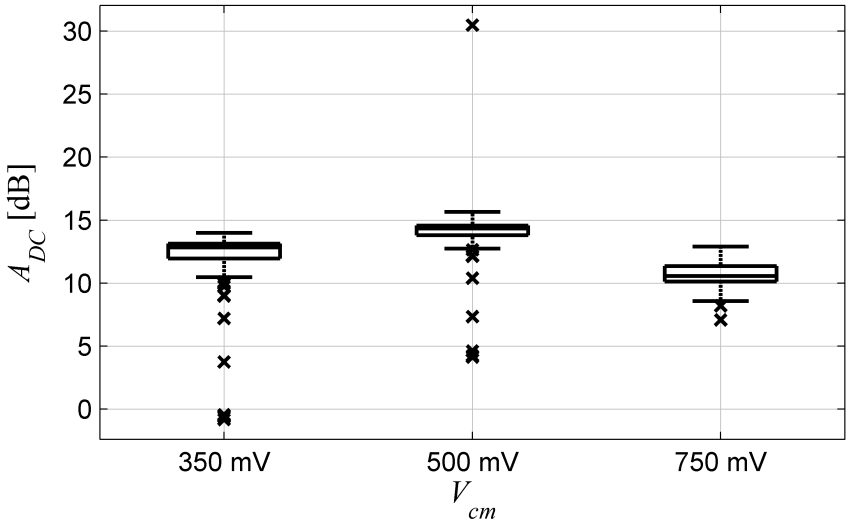

Figure 4.55 Boxplot of silicon measurement of baseline amplifier DC gain across entire wafer and multiple input common-mode voltages, V_{cm}.

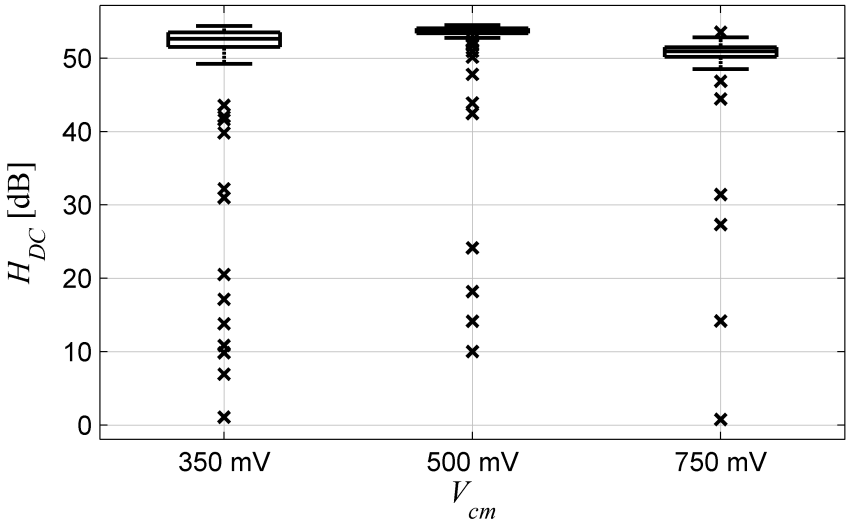

Figure 4.56 Boxplot of silicon measurement of positive feedback amplifier DC gain with $R_1 = 118\ \Omega$ and $R_2 = 314\ \Omega$ (PFBa) across entire wafer and multiple input common-mode voltages, V_{cm}.

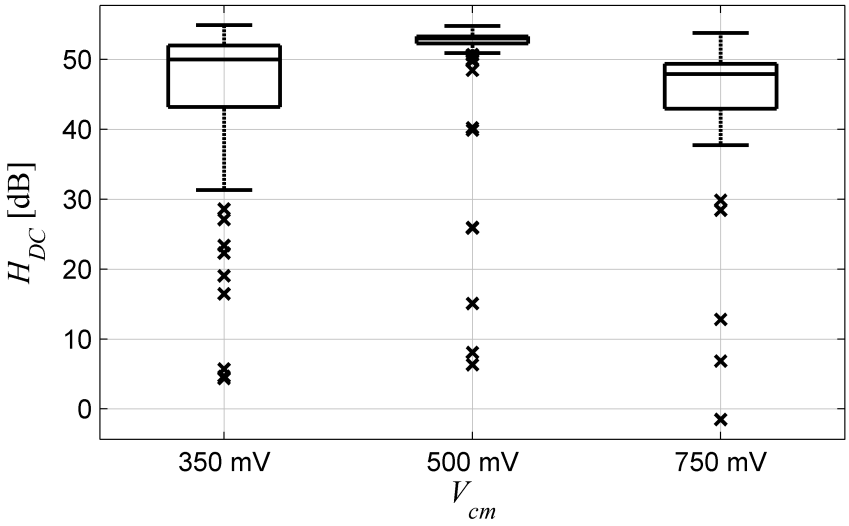

Figure 4.57 Boxplot of silicon measurement of positive feedback amplifier DC gain with $R_1 = 118\ \Omega$ and $R_2 = 375\ \Omega$ (PFBb) across entire wafer and multiple input common-mode voltages, V_{cm}.

showed that the MOSFETs were performing between the slow and typical device model corners as were the resistors (e.g., higher sheet resistance than nominal). Given slow MOSFETs and resistors, simulations show amplifiers yielding higher gains than typical silicon. Figure 4.55 shows the baseline amplifier's silicon results across the wafer. As expected, the silicon DC gain is above average. As a result, PFBa and PFBb amplifier performance, shown in Figure 4.56 and Figure 4.57, respectively, is also above average and saturated at the measurement limitation. Furthermore, Monte Carlo simulation showed that resistor mismatch could cause hysteresis in the positive feedback amplifiers. With hysteresis, any thermal or switching noise in the test fixture could cause the amplifier to falsely switch, appearing to be an artificially high DC gain value.

4.2.2 AC Tests

The AC tests were more time consuming to perform and were intended to target a limited number of die. Specifically, the frequency behavior of these die was observed in order to

confirm the theories of this work. The low frequency (50 MHz) gain was also recorded in order to confirm the test bench and obtain correlation with the DC tests of the previous section [89].

4.2.2.1 Test Setup

Figure 4.58 is a block diagram of the S-parameter measurement test bench [90] used in this work. An Agilent E5071C 4-port Network Analyzer was used to perform and collect the S-parameter data. These tests could also be performed with a 2-port network analyzer as in [91]. Supply voltages and control signals were provided via an HP4156A Precision Semiconductor Parameter Analyzer. HP11612A Bias Tees were used to provide DC common-mode voltage, V_{cm}, to the amplifier inputs and SD3244 $0.1 - 18$ GHz DC Blocks were used at the amplifier outputs to prevent the VNA from loading the amplifier outputs with $50\ \Omega$ – this $50\ \Omega$ loading affects the input V_{CM} when the amplifier is in a resistive positive feedback configuration.

4.2.2.2 Measurement Methodology

The 4-port S-parameter measurements were collected from the E5071C over a range of

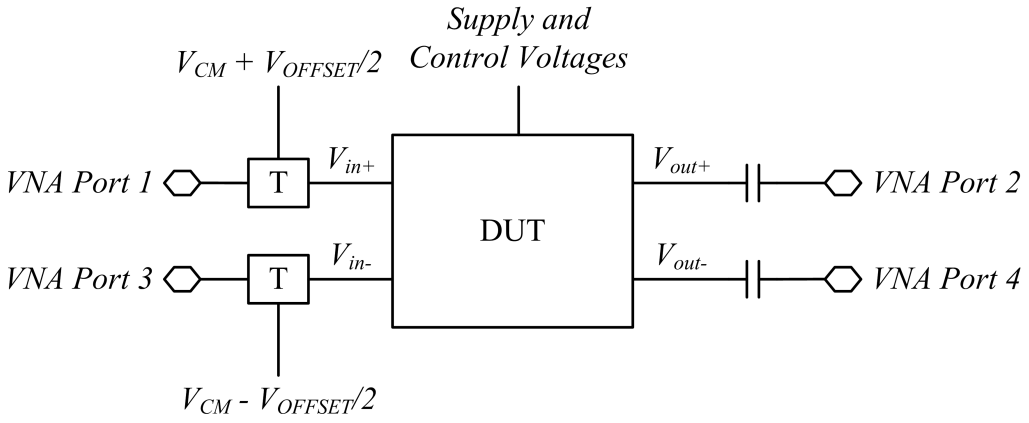

Figure 4.58 S-parameter test bench using four-port s-parameter analyzer, semiconductor parameter analyzer, and data post processing in MATLAB.

50 MHz to 8.5 GHz on a log scale. To obtain meaningful amplifier data from these 4-port parameters, they are converted to mixed-mode S-parameters, as in [92], [93]. The mixed-mode parameters describe the amplifier behavior in terms of differential and common-mode inputs and outputs. Further discussion of mixed-mode S-parameters can be found in Appendix C. The differential-differential mixed mode S-parameters, S_{dd}, were used to evaluate the voltage gain of the amplifier through the relationship [94]

$$A_V = \frac{S_{21}(1+\Gamma_L)}{(1-S_{22}\Gamma_L)+S_{11}(1-S_{22}\Gamma_L)+S_{21}\Gamma_L S_{12}} \tag{4.7}$$

where A_V is the voltage gain, S_{11}, S_{12}, S_{21}, S_{22} are the S_{dd} mixed mode S-parameters and Γ_L is the load reflection coefficient and assumed to be zero (unloaded) in this analysis. These measurements were taken over a range of V_{cm} values. The test bench in Figure 4.58 also has the ability to manually compensate for input-referred offset due to device mismatch by adding a fixed offset to the amplifier input to allow for further improvement in the optimum gain measurement. Half of the offset voltage, V_{os}, is applied to each terminal in opposite directions to maintain the specified V_{cm}.

In addition to the amplifier structures, open and short structures were created to de-embed the test setup, pad, and routing parasitics. This is a commonly used and well-known technique [95] to decouple the test setup from the behavior of the DUT.

The amplifier analysis procedure consisted of the following steps:

1) Measure and store ‘open’ structure S-parameters
2) Measure and store ‘short’ structure S-parameters
3) At a given V_{cm} and V_{os} value, measure 4 port S-parameters
4) De-embed parasitics

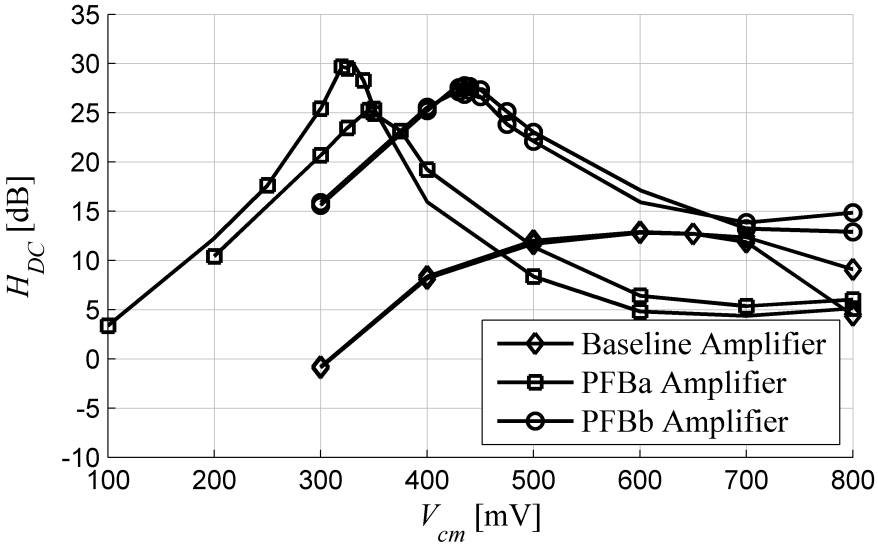

Figure 4.59 Silicon AC measurement of DC gain versus V_{cm} for baseline, PFBa, and PFBb amplifiers.

5) Convert DUT S-parameters to mixed-mode S-parameters

6) Calculate voltage gain, A_V

This analysis is repeated for multiple V_{cm} and V_{os} values to find the maximum gain operating point of the amplifier as follows:

1) A V_{cm} sweep was performed and the data analyzed to determine the V_{cm} voltage at which the DC gain was maximized for a given amplifier. See Figure 4.59 for reference.
2) At the optimized V_{cm} voltage, a V_{os} sweep was performed to compensate for input-referred offset and further refine the maximum DC gain measurement. See Figure 4.60 for reference.

At an optimized V_{cm} and V_{os}, the frequency behavior of an amplifier is then observed. Figure 4.61 and Figure 4.62 show the frequency response of a baseline amplifier and positive feedback amplifier respectively, each at their respective optimum V_{cm} and V_{os}.

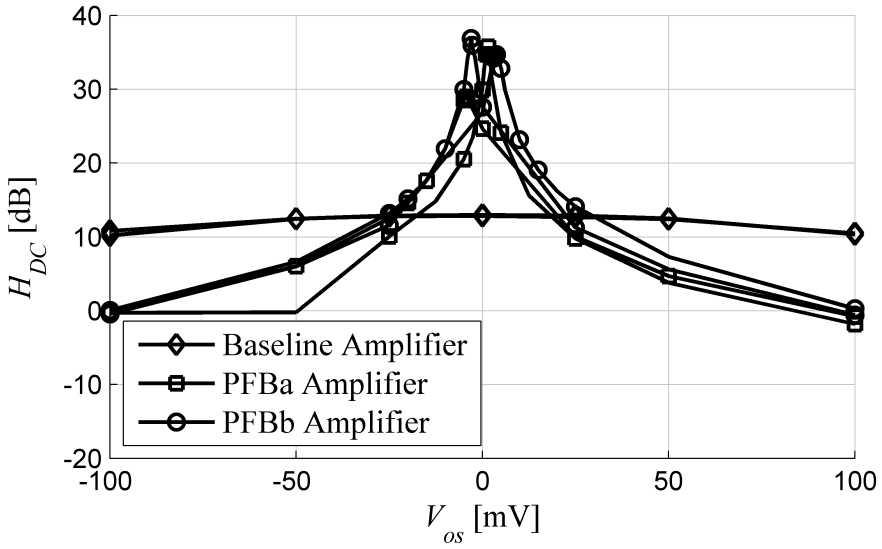

Figure 4.60 Silicon AC measurement of DC gain versus V_{os} for baseline, PFBa, and PFBb amplifiers.

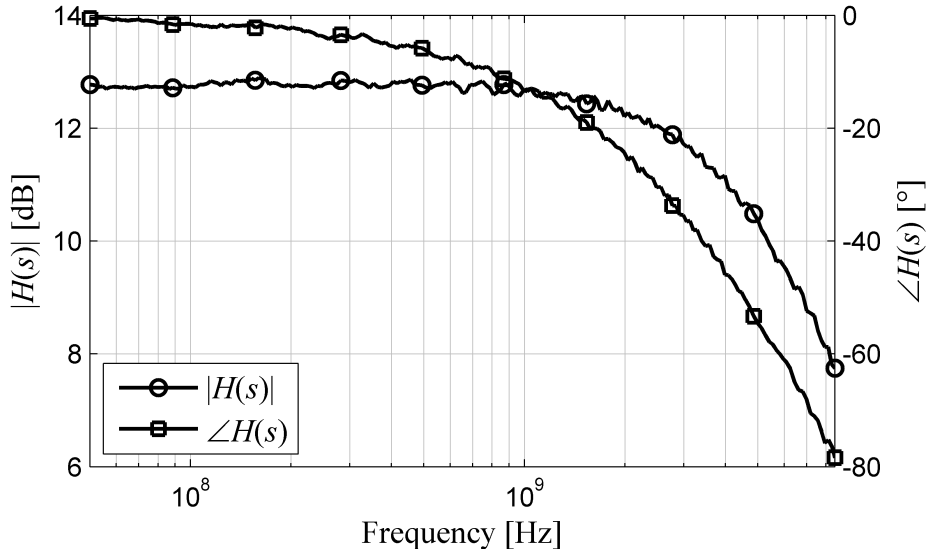

Figure 4.61 Silicon measurement of baseline amplifier frequency response from 50 MHz to 8.5 GHz.

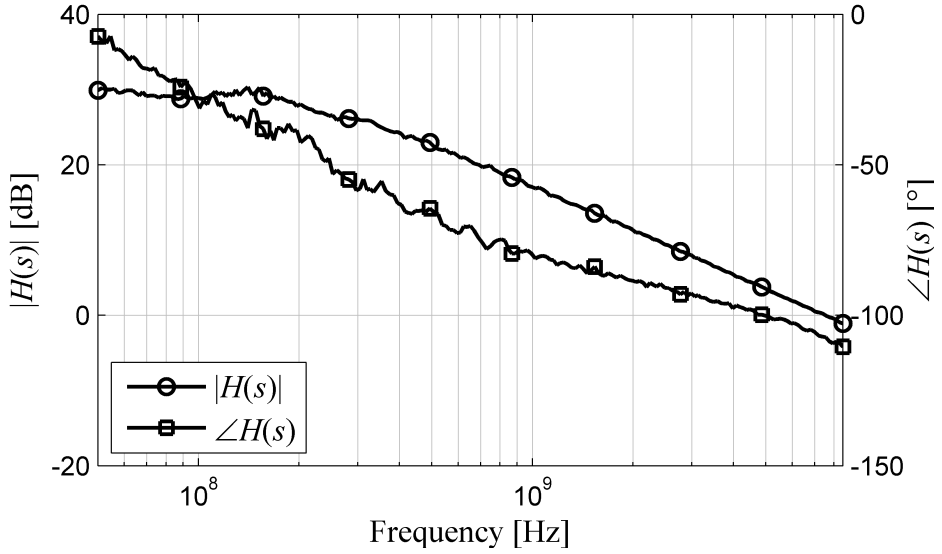

Figure 4.62 Silicon measurement of positive feedback amplifier with $R_1 = 118\ \Omega$ and $R_2 = 314\ \Omega$ (PFBa) frequency response from 50 MHz to 8.5 GHz.

4.2.2.3 Results

This analysis was performed for a total of 15 amplifiers, five of each amplifier type: Baseline, Low R_2 (PFBa) and High R_2 (PFBb). The summary results of these measurements are shown in Table 4.8. As expected, both PFBa and PFBb amplifiers show significant DC gain improvement over the baseline amplifier from 12.7 dB to 29.8 dB for PFBa and to 34.7 dB for PFBb. The average increase in gain is larger for the PFBb amplifier than that of the PFBa amplifier. This is in contrast to the expected trend predicted by the theory in which lower R_2 values would yield higher gains. However, since only a small number of die were tested, conclusions based on the statistics of these

Table 4.8 DC gain from S-parameter measurements

	Min (dB)	Max (dB)	Mean (dB)
Baseline	12.5	13.0	12.7
$R_2 = 314\ \Omega$	27.0	35.0	29.8
$R_2 = 375\ \Omega$	27.0	39.2	34.7

measurements cannot be made with any certainty. Instead, the main conclusion to be drawn from this data is general trend of increased gain with the application of positive feedback.

4.3 Summary

This chapter uses the theory developed in Chapter 3 to implement a positive feedback amplifier in TSMC's 65 nm logic process. The intent for this design was to use only standard threshold and low supply voltage MOSFETs and passive devices such that no special process steps would be required to implement the circuit. The baseline amplifier was designed as a fully differential amplifier having relatively low gain and high bandwidth. This design intent was targeted to match the requirements for the positive feedback design methodology. Bias circuitry was designed to provide consistent bias voltages to the baseline amplifier as well as power down capabilities for consistent testing purposes. Finally, the positive feedback amplifier was designed according to the positive feedback design methodology and using the baseline amplifier at its core with fully differential positive feedback implemented with polysilicon resistors.

The designed circuit blocks were simulated extensively on their own as well as together as the final system. These simulations were performed over all permutations of process, voltage, and temperature corners as well as with process variation and device mismatch in Monte Carlo simulations. These simulations show that the positive feedback amplifiers exhibit consistent and repeatable gain improvement over the baseline amplifier's performance. Some extreme cases of process variation and process mismatch indicated that hysteresis and instability could be an issue at positive feedback design points

approaching the stability criteria. It was also shown that moving the positive feedback design point further away from the stability criteria alleviated these issues.

Finally, the designed circuitry was fabricated and the resulting silicon tested to compare against simulation. The DC simulations showed large improvements in the DC gain of the positive feedback amplifier, but these tests were limited by a minimum step size of the available test equipment, limiting the usefulness of the results beyond a cursory observation that the positive feedback implementation did in fact increase the gain performance of the amplifier. The AC tests, on the other hand, provided significantly useful results that confirmed the DC test findings in that low frequency gain was improved with the application of positive feedback. Furthermore, the AC tests were able to confirm the predicted behavior of gain-bandwidth product degradation with the application of feedback.

The positive feedback design methodology was proven to provide significant gain enhancement in low-gain, high-frequency amplifiers. This is a direct circuit solution to the device degradation of this scaled technology. This application also confirms the side effects of positive feedback in that the input-referred offset is increased as well as the overall sensitivity of the circuit to process variation and device mismatch.

CHAPTER 5
CONCLUSIONS AND RECOMMENDATIONS

This work shows that the continued size reduction of transistors in the semiconductor industry has detrimental effects on the fundamental parameters of those transistors as used in traditional analog circuitry. Specifically, the maximum intrinsic gain of the core process transistors continues to degrade as technology is scaled deep into sub-100 nm device geometries. Using a test bench that mimics the design process, it was shown that traditional design methodologies to improve the maximum intrinsic gain of a device cannot alone solve the degradation problem. Currently methodologies to design successful analog circuits in these technologies center on the use of thick oxide I/O devices that can support large overdrive voltages to improve maximum intrinsic gain. This methodology can complicate a design in terms of managing multiple voltage domains.

5.1 Positive Feedback Findings Summary

This work proposed the solution of positive feedback to address maximum intrinsic gain degradation in linear amplifier design using thin oxide devices that are core to the process and compatible with the digital logic voltage levels. The positive feedback design methodology was explored in detail at various levels of abstraction from block diagram analyses to transistor level circuit analysis. In each case, the criteria for stable application of the positive feedback were derived in the context of that system. Furthermore, effects of positive feedback on the other aspects of the system were explored. These effects include the input and output impedance, input-referred offset, input-referred noise, common-mode rejection ratio, and gain-bandwidth product. Through this analysis it was

shown that the application of positive feedback can have the impact of increasing the spread in variation of these amplifier parameters, if applied improperly. To avoid these issues, a sensitivity analysis of the positive feedback systems was performed. The result of this sensitivity analysis was used to develop an algorithm to optimize a positive feedback amplifier's design to improve gain while avoiding a design point in which process variation causes unnecessary deviation of other amplifier parameters.

To prove the positive feedback concepts derived for this work, a series of test amplifiers were design in TSMC's 65 nm technology using only standard threshold voltage, thin oxide, digital transistors. This circuitry was simulated extensively using the Cadence Custom IC Design software suite and then fabricated at TSMC. Both simulation and silicon measurements validated the positive feedback design theory. This demonstrated that positive feedback could be applied to a linear amplifier to increase its gain while the overall system remains stable. The simulation and silicon data also confirm the other amplifier effects such as the decrease in input impedance and gain-bandwidth product as well as the increase in output impedance and input-referred offset. Furthermore, the increase in amplifier parameter variation due to the sensitivity analysis is also seen in the simulation and silicon analyses.

5.2 Areas of Application for Positive Feedback

This work has proven that stable and gain-improving positive feedback can be applied to low-gain, high-frequency linear amplifiers in a consistent and robust manner. In order to do this, the designer must pay careful attention to avoid sensitive design points using the optimization algorithm outlined in this work. The positive feedback amplifier design methodology could find applications in circuit design in which high gain is desired and

increased variation in that gain is tolerable. Areas of application would include high-speed current mode logic (CML) circuitry, and high-speed physical layer (PHY) development for serial communications links.

5.3 Suggestions for Future Work

This work has proposed a generic framework on top of which physical circuit topologies can be built. The physical implementation of positive feedback here was presented as a proof-of-concept vehicle. This was not intended to imply that the resistive feedback method on a differential amplifier stage is the only valid implementation of positive feedback. Future work should include further investigation of more implementations of this positive feedback methodology. New positive feedback circuit topologies will also open the door for new applications not foreseen in this work.

Furthermore, the inclusion of more detailed process specific information from technology foundries would simplify the positive feedback design process. The information could be incorporated into parameterized cell (PCell) design for standard amplifier topologies. This would allow for reliable usage of the positive feedback techniques.

Finally, the maximum intrinsic gain degradation problem should have continued monitoring. As technologies scale past 22 nm [1], new and novel processing techniques may begin to alter the way in which the maximum intrinsic gain in degraded. In an ideal situation, the gain would turn a corner and become improved. A more likely scenario, however, is that the gain will either remain constant or continue to degrade. In this latter case, the continued addressing of device process problem with circuit solutions is

imperative to the successful design of analog linear amplifiers and circuits in these scaled technologies.

REFERENCES

[1] (2013, March) International Technology Roadmap for Semiconductors 2012 Updates. [Online]. http://www.itrs.net/Links/2012ITRS/Home2012.htm

[2] A.-J. Annema, "Analog circuit performance and process scaling," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 6, pp. 711-725, June 1999.

[3] M. Pude, C. Macchietto, P. Singh, J. Burleson, and P. R. Mukund, "Maximum intrinsic gain degradation in technology scaling," in *International Semiconductor Device Research Symposium*, 2007, pp. 1-2.

[4] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of Solid-State Circuits*, vol. 9, no. 5, pp. 256-268, October 1974.

[5] D. Pan, H. W. Li, and B. M. D. Wilamowski, "A low voltage to high voltage level shifter circuit for MEMS application," in *Proceedings of the 15th Biennial University/Government/Industry Microelectronics Symposium*, 2003, pp. 128-131.

[6] D. Dwivedi, S. Dwivedi, and E. Potladhurthi, "Voltage up level shifter with improved performance and reduced power," in *25th IEEE Canadian Conference on Electrical & Computer Engineering*, 2012, pp. 1-4.

[7] R. Garg, G. Mallarapu, and S. P. Khatri, "A Single-supply True Voltage Level Shifter," in *Design, Automation and Test in Europe*, 2008, pp. 979-984.

[8] H. Gossner, "ESD protection for the deep sub micron regime - a challenge for design methodology," in *17th International Conference on VLSI Design*, 2004, pp. 809-818.

[9] S.-H. H. Chen, M.-D. D. Ker, and H.-P. Hung, "Active ESD Protection Design for Interface Circuits Between Separated Power Domains Against Cross-Power-Domain ESD Stresses," *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 3, pp. 549-560, March 2008.

[10] (2013, March) Cadence Custom IC Design. [Online]. http://www.cadence.com/products/cic/pages/default.aspx

[11] (2013, March) MATLAB - The Language of Technical Computing. [Online]. http://www.mathworks.com/products/matlab/

[12] H.-S. P. Wong, D. J. Frank, P. M. Solomon, C.H. J. Wann, and J. J. Welser, "Nanoscale CMOS," *Proceedings of the IEEE*, vol. 87, no. 4, pp. 537-570, April 1999.

[13] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*.: Cambridge University Press, 1998.

[14] S. S. Suryagandh, M. Garg, and J. C. S. Woo, "A device design methodology for sub-100-nm SOC applications using bulk and SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 51, no. 7, pp. 1122-1128, July 2004.

[15] M. Gupta and J. Woo, "Device design for sub 90 nm MOSFETs for sample and hold circuits," in *Proceeding of the 34th European Solid-State Device Research*, 2004, pp. 377-380.

[16] G. G. Shahidi, "Challenges of CMOS scaling at below 0.1 μm," in *Proceedings of*

the 12th International Conference on Microelectronics, 2000, pp. 5-8.

[17] Y. Taur et al., "CMOS scaling into the nanometer regime," *Proceedings of the IEEE*, vol. 85, no. 4, pp. 486-504, April 1997.

[18] D. J. Frank et al., "Device scaling limits of Si MOSFETs and their application dependencies," *Proceedings of the IEEE*, vol. 89, no. 3, pp. 259-288, March 2001.

[19] B. Davari, R. H. Dennard, and G. G. Shahidi, "CMOS scaling for high performance and low power-the next ten years," *Proceedings of the IEEE*, vol. 83, no. 4, pp. 595-606, April 1995.

[20] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*.: John Wiley & Sons, 2003.

[21] Y. Tsividis, *The MOS Transistor*, 2nd ed.: Oxford University Press, 1999.

[22] A.-J. Annema, B. Nauta, R. van Langevelde, and H. Tuinhout, "Analog circuits in ultra-deep-submicron CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 132-143, January 2005.

[23] M. Garg, S. S. Suryagandh, and J. C. S. Woo, "Scaling impact on analog performance of sub-100nm MOSFETs for mixed mode applications," in *33rd Conference on European Solid-State Device Research*, 2003, pp. 371-374.

[24] C. Hu, "Future CMOS scaling and reliability," *Proceedings of the IEEE*, vol. 81, no. 5, pp. 682-689, May 1993.

[25] M. R. Pinto, E. Sangiorgi, and J. Bude, "Silicon MOS transconductance scaling into the overshoot regime," *IEEE Electron Device Letters*, vol. 14, no. 8, pp. 375-378, August 1993.

[26] G. A. Sai-Halasz, M. R. Wordeman, D. P. Kern, S. Rishton, and E. Ganin, "High transconductance and velocity overshoot in NMOS devices at the 0.1- mu m gate-length level," *IEEE Electron Device Letters*, vol. 9, no. 9, pp. 464-466, September 1988.

[27] T. H. Morshed et al. (2011) BSIM4v4.7 MOSFET Model User's Manual. PDF. [Online]. http://www-device.eecs.berkeley.edu/bsim/Files/BSIM4/BSIM470/BSIM470_Manual.pdf

[28] Y. Cheng and C. Hu, *MOSFET Modeling & BSIM3 User's Guide*.: Kluwer Academic Publishers, 1999.

[29] W. Liu, *MOSFET Models for SPICE Simulation including BSIM3v3 and BSIM4*.: John Wiley & Sons, Inc., 2001.

[30] K. M. Cao et al., "Modeling of pocket implanted MOSFETs for anomalous analog behavior," in *International Electron Devices Meeting*, 1999, pp. 171-174.

[31] E. Bohannon, C. Washburn, and P. R. Mukund, "Analog IC Design in Ultra-Thin Oxide CMOS Technologies With Significant Direct Tunneling-Induced Gate Current," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 4, pp. 645-653, April 2011.

[32] P. E. Allen, B. J. Blalock, and G. A. Rincon, "Low voltage analog circuits using standard CMOS technology," in *Proceedings of the 1995 International Symposium on Low Power Design*, 1995, pp. 209-214.

[33] S. S. Rajput and S. S. Jamuar, "Low voltage analog circuit design techniques," *IEEE*

Circuits and Systems Magazine, vol. 2, no. 1, pp. 24-42, January 2002.

[34] M. Sumita et al., "Mixed body bias techniques with fixed Vt and Ids generation circuits," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 60-66, January 2005.

[35] S. Yan and E. Sanchez-Sinencio, "Low Voltage Analog Circuit Design Techniques: A Tutorial," *IEICE Transactions on Analog Integrated Circuits and Systems*, vol. E00-A, no. 2, pp. 179-196, February 2000.

[36] J. H. H. Huijsing, R. Hogervorst, and K.-J. J. De Langen, "Low-power low-voltage VLSI operational amplifier cells," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 42, no. 11, pp. 841-852, November 1995.

[37] Y. Tang and R. L. Geiger, "A 0.6 V ultra low voltage operational amplifier," in *IEEE International Symposium on Circuits and Systems*, 2002, pp. 611-614.

[38] A. Sedra and K. Smith, "A second-generation current conveyor and its applications," *IEEE Transactions on Circuit Theory*, vol. 17, no. 1, pp. 132-134, January 1970.

[39] W. Surakampontorn, V. Riewruja, K. Kumwachara, and K. Dejhan, "Accurate CMOS-based current conveyors," *IEEE Transactions on Instrumentation and Measurement*, vol. 40, no. 4, pp. 699-702, August 1991.

[40] A. Fabre, O. Saaid, F. Wiest, and C. Boucheron, "High frequency applications based on a new current controlled conveyor," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 43, no. 2, pp. 82-91, February 1996.

[41] C.-H. Lee, J. Cornish, K. Clellan, and J. Jr. Chama, "Current-mode approach for wide gain bandwidth product architecture," in *IEEE International Symposium on Circuits and Systems*, 1997, pp. 229-232.

[42] B. Babaei and S. Mirzakuchaki, "High CMRR, Low Power and Wideband Current-Mode Instrumentation Amplifier," in *24th Norchip Conference*, 2006, pp. 121-124.

[43] M. Kumngern, "A new CMOS second generation current conveyor with variable current gain," in *IEEE International Conference on Circuits and Systems*, 2012, pp. 272-275.

[44] A. Guzinski, M. Bialki, and J. C. Matheau, "Body-Driven Differential Amplifier for Application in Continuous-Time Active C-Filter," in *Proceedings of the European Conference on Circuit Theory and Design*, 1987, pp. 315-319.

[45] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 7, pp. 769-780, July 1998.

[46] X. Zhang and E. I. El-Masry, "A Novel CMOS OTA Based on Body-Driven MOSFETs and its Applications in OTA-C Filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 6, pp. 1204-1212, June 2007.

[47] X. Zhang and E. I. El-Masry, "A regulated body-driven CMOS current mirror for low-voltage applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 51, no. 10, pp. 571-577, October 2004.

[48] J. Rosenfeld, M. Kozak, and E. G. Friedman, "A bulk-driven CMOS OTA with 68 dB DC gain," in *11th IEEE International Conference on Electronics, Circuits and*

Systems, 2004, pp. 5-8.

[49] S. Chatterjee, Y. P. Tsividis, and P. R. Kinget, "0.5-V analog circuit techniques and their application in OTA and filter design," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2373-2387, December 2005.

[50] C. Urban, J. E. Moon, and P. R. Mukund, "Designing bulk-driven MOSFETs for ultra-low-voltage analogue applications," *Semiconductor Science and Technology*, vol. 25, no. 11, pp. 1-8, November 2010.

[51] B. Razavi, *Design of Analog CMOS Integrated Circuits*.: McGraw-Hill, 2001.

[52] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed.: John Wiley & Sons, Inc., 2001.

[53] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*.: Oxford University Press, 1998.

[54] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2nd ed.: Oxford University Press, 2002.

[55] M. Pude, P. R. Mukund, P. Singh, K. Paradis, and J. Burleson, "Amplifier gain enhancement with positive feedback," in *53rd IEEE International Midwest Symposium on Circuits and Systems*, 2010, pp. 981-984.

[56] M. Pude, P. R. Mukund, P. Singh, and J. Burleson, "Using positive feedback to overcome $g_m r_o$ limitations in scaled CMOS amplifier design," in *51st Midwest Symposium on Circuits and Systems*, 2008, pp. 807-810.

[57] J. K. Kim and T. S. Kalkur, "High-speed current-mode logic amplifier using positive feedback and feed-forward source-follower techniques for high-speed CMOS I/O buffer," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 3, pp. 796-802, March 2005.

[58] M. Alioto, L. Pancioni, S. Rocchi, and V. Vignoli, "Modeling and evaluation of positive-feedback source-coupled logic," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 12, pp. 2345-2355, December 2004.

[59] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*.: John Wiley and Sons, Inc., 2005.

[60] M. M. Amourah and R. L. Geiger, "A high gain strategy with positive-feedback gain enhancement technique," in *IEEE International Symposium on Circuits and Systems*, 2001, pp. 631-634.

[61] J. Ramos and M. S. J. Steyaert, "Positive feedback frequency compensation for low-voltage low-power three-stage amplifier," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 10, pp. 1967-1974, October 2004.

[62] F. Schlogl and H. Zimmerman, "120nm CMOS operational amplifier with pseudo-cascodes and positive feedback," in *The 3rd IEEE International Workshop on System-on-Chip for Real-Time Applications*, 2003, pp. 277-280.

[63] L. Bouzerara, M. T. Belaroussi, and B. Amirouche, "Low-voltage, low-power and high gain CMOS OTA using active positive feedback with feedforward and FDCM techniques," in *23rd International Conference on Microelectronics*, 2002, pp. 573-576.

[64] M. M. Amourah and R. L. Geiger, "All digital transistor high gain operational

amplifier using positive feedback technique," in *IEEE International Symposium on Circuits and Systems*, 2002, pp. I701-I704.

[65] G. R. Lahiji, O. Oleyaie, and A. Abrishamifar, "New operational amplifier using a positive feedback," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, no. 5, pp. 412-417, May 1997.

[66] H. Venkatram, T.-H. Oh, J. Guerber, and U.-K. K. Moon, "Class A+ amplifier with controlled positive feedback for discrete-time signal processing circuits," in *IEEE International Symposium on Circuits and Systems*, 2012, pp. 428-431.

[67] P. T. Tran, H. L. Hess, K. V. Noren, and S. U. Ay, "Gain-enhancement differential amplifier using positive feedback," in *International Midwest Symposium on Circuits and Systems*, 2012, pp. 718-721.

[68] K. Ragab, R. Gharpurey, and M. Orshansky, "Embracing local variability to enable a robust high-gain positive-feedback amplifier: Design methodology and implementation," in *13th International Symposium on Quality Electronic Design*, 2012, pp. 143-150.

[69] E. H. Armstrong, "Wireless Receiving System," US Patent 1,113,149, October 6, 1914.

[70] M. E. Schlarmann, S. Q. Malik, and R. L. Geiger, "Positive feedback gain-enhancement techniques for amplifier design," in *IEEE International Symposium on Circuits and Systems*, 2002, pp. II37-II40.

[71] B. Kim, S. Mandal, and R. Sarpeshkar, "Power-adaptive operational amplifier with positive-feedback self biasing," in *IEEE International Symposium on Circuits and Systems*, 2006, pp. 4883-4886.

[72] L. Lee, R. M. Sidek, S. S. Jamuar, and S. Khatun, "Design of a Dual-Band Low Noise Amplifier (LNA) Utilizing Positive Feedback Technique," in *4th Student Conference on Research and Development*, 2006, pp. 22-24.

[73] A. Liscidini, M. Brandolini, D. Sanzogni, and R. Castello, "A 0.13 μm CMOS front-end, for DCS1800/UMTS/802.11b-g with multiband positive feedback low-noise amplifier," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 4, pp. 981-989, April 2006.

[74] M. W. Tian, V. Visvanathan, J. Hantgan, and K. S. Kundert, "Striving for small-signal stability," *IEEE Circuits and Devices Magazine*, vol. 17, no. 1, pp. 31-41, January 2001.

[75] P. J. Hurst and S. H. Lewis, "Determination of stability using return ratios in balanced fully differential feedback circuits," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 42, no. 12, pp. 805-817, December 1995.

[76] R. D. Middlebrook, "Measurement of loop gain in feedback systems," *International Journal of Electronics*, vol. 38, no. 4, pp. 485-512, April 1975.

[77] E. W. Weisstein. (2013, March) "Pythagorean Theorem." From MathWorld--A Wolfram Web Resource. [Online]. http://mathworld.wolfram.com/PythagoreanTheorem.html

[78] S. P. R. Bandi et al., "Accurate MOS Gate Impedance Model for 200MHz-20GHz

Frequency Range," in *International Semiconductor Device Research Symposium*, 2005, pp. 372-373.

[79] X. Jin et al., "An effective gate resistance model for CMOS RF and noise modeling," in *International Electron Devices Meeting*, 1998, pp. 961-964.

[80] M. Pude, P. R. Mukund, and J. Burleson, "Process Tolerant Design of Sub-100 nm Multi-GHz Positive Feedback CMOS Amplifiers," *Microelectronics Journal (Submitted for Review)*.

[81] J. H. Holland, "Genetic Algorithms," *Scientific American*, vol. 267, no. 1, pp. 66-72, January 1992.

[82] P. Guo, X. Wang, and Y. Han, "The enhanced genetic algorithms for the optimization design," in *3rd International Conference on Biomedical Engineering and Informatics*, 2010, pp. 2990-2994.

[83] (2013, March) Taiwan Semiconductor Manufacturing Company Limited 65 nm Technology. [Online]. http://www.tsmc.com/english/dedicatedFoundry/technology/65nm.htm

[84] N. Talebbeydokhti and P. K. Hanumolu, "Constant transconductance bias circuit with an on-chip resistor," in *IEEE International Symposium on Circuits and Systems*, 2006, pp. 2860-2863.

[85] S. T. Nicolson and K. Phang, "Improvements in biasing and compensation of CMOS opamps," in *International Symposium on Circuits and Systems*, 2004, pp. 665-668.

[86] J. Chen and B.-X. Shi, "Novel constant transconductance references and the comparisons with the traditional approach," in *Southwest Symposium on Mixed-Signal Design*, 2003, pp. 104-107.

[87] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433-1439, May 1989.

[88] E. W. Weisstein. (2013, March) "Normal Difference Distribution." From MathWorld--A Wolfram Web Resource. [Online]. http://mathworld.wolfram.com/NormalDifferenceDistribution.html

[89] M. Pude, P. R. Mukund, and J. Burleson, "Positive Feedback for Gain Enhancement in Sub-100 nm Multi-GHz CMOS Amplifier Design," *International Journal of Circuit Theory and Applications (Pending Publication)*.

[90] (2006, June) Agilent Technologies. [Online]. http://cp.literature.agilent.com/litweb/pdf/5952-1087.pdf

[91] L. Sun, Z.-G. G. Wang, and J. Gao, "A method for on-wafer S-parameter measurement of a differential amplifier by using two-port network analyzer," in *Asia-Pacific Conference Proceedings Microwave Conference Proceedings*, 2005, pp. 1-4.

[92] D. E. Bockelman and W. R. Eisenstadt, "Pure-mode network analyzer for on-wafer measurements of mixed-mode S-parameters of differential circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 7, pp. 1071-1077, July 1997.

[93] D. E. Bockelman and W. R. Eisenstadt, "Combined differential and common-mode

scattering parameters: theory and simulation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 43, no. 7, pp. 1530-1539, July 1995.

[94] G. Gonzalez, *Microwave Transistor Amplifiers Analysis and Design*.: Prentice Hall, 1997.

[95] M.C. A.M. Koolen, J.A. M. Geelen, and M.P. J.G. Versleijen, "An improved de-embedding technique for on-wafer high-frequency characterization," in *Proceedings of the 1991 Bipolar Circuits and Technology Meeting*, 1991, pp. 188-191.

APPENDIX A
CODE AND SCRIPTS

This appendix includes some of the code used in the data analysis of this work.

A.1 OCEAN Script for g_m and r_o Extraction

This OCEAN script is used for the g_m and r_o extraction in Section 2.2.

```
ocnWaveformTool( 'wavescan )
simulator( 'spectre )
design(
"/projects/lsi2/engs/mwp4065/cadence/simulation/mig_extract_g65/spectre/schematic/netlist
/netlist")
resultsDir(
"/projects/lsi2/engs/mwp4065/cadence/simulation/mig_extract_g65/spectre/schematic" )
modelFile(
    '("$MMSM_PATH/cadence/lib/g65gplus/models/G65_mos.scs" "SS")
    '("$MMSM_PATH/cadence/lib/g65gplus/models/G65_res.scs" "SS_RES")
    '("$MMSM_PATH/cadence/lib/g65gplus/models/G65_cap.scs" "TT"))

analysis('dc ?saveOppoint t  )
desVar(   "vd" 0.2168  )
desVar(   "S" 30       )
desVar(   "res" 1000   )
desVar(   "gain" 10000 )
desVar(   "cur" 130u   )
desVar(   "vdd33" 3.3  )
desVar(   "vdd12" 1.2  )
desVar(   "vdd10" 1.0  )
desVar(   "cap_mismatch" 0     )
desVar(   "res_mismatch" 0     )
desVar(   "fet_mismatch" 0     )
desVar(   "rgflag" 1   )
desVar(   "ccoflag" 0  )
desVar(   "default_lod" 0      )
option( 'temp  "125.0" )
saveOption( 'currents "all" )
saveOption( 'pwr "subckts" )
saveOption( 'save "all" )
temp( 125.0 )

optimizeGoal("Vd_ov" '(VDC("/VD")-pv("MN0.mx" "vdsat" ?result "dcOpInfo-info")) 'match
'vd_ov '2 t)
optimizeGoal("Vg_ov" '(VDC("/VG")-pv("MN0.mx" "vth" ?result "dcOpInfo-info"))   'match
'150m '2 t)
optimizeVar("S" 30 10 60)
optimizeVar("vd" 200m 0 1)
optimizeVar("cur" 130u 0 1m)
optimizeAlgoControl(?relDelta "" ?relFunTol "" ?relVarTol "")
optimizePlotOption(?auto t ?varHist t ?scalHist t ?funcObjHist t ?numIter 5 ?fontSize 9
?width 630 ?height 376 ?xloc 509 ?yloc 378)

out=outfile("./mig_extract_g65.out" "w")
fprintf(out "L\tS\tID\tVG\tVD\tVT\tVdsat\tVD_OV\tVG_OV\tgm\tgds\n")
close(out)


foreach( vd_ov '(50m 100m 170m 300m)
    foreach( L '(60n 120n 180n 300n 360n 600n 1200n 3000n 6000n 9600n)
        desVar(   "len" L      )
```

```
        run()
        optimizeRun(?goals '("Vd_ov" "Vg_ov") ?vars '("S" "vd") ?algo 'Auto ?continue t)

        S = pv("S" "value" ?result "variables")
        ID = pv("cur" "value" ?result "variables")
        VG = VDC("/VG")
        VD = VDC("/VD")
        VT = pv("MN0.mx" "vth" ?result "dcOpInfo-info")
        Vdsat = pv("MN0.mx" "vdsat" ?result "dcOpInfo-info")
        VD_OV = (VDC("/VD") - pv("MN0.mx" "vdsat" ?result "dcOpInfo-info"))
        VG_OV = (VDC("/VG") - pv("MN0.mx" "vth" ?result "dcOpInfo-info"))
        gm = pv("MN0.mx" "gm" ?result "dcOpInfo-info")
        gds = pv("MN0.mx" "gds" ?result "dcOpInfo-info")

        out=outfile("./mig_extract_g65.out" "a")
        fprintf(out
"%1.3e\t%1.3e\t%1.3e\t%1.3e\t%1.3e\t%1.3e\t%1.3e\t%1.3e\t%1.3e\t%1.3e\t%1.3e\n" L S ID VG
VD VT Vdsat VD_OV VG_OV gm gds)
        close(out)
    )
)


foreach( vd_ov '(50m 100m 170m 300m)
    foreach( L '(60n 180n 360n)
        desVar(   "len" L      )
        desVar(   "S" 30       )

        run()
        optimizeRun(?goals '("Vd_ov" "Vg_ov") ?vars '("cur" "vd") ?algo 'Auto ?continue t)

        S = pv("S" "value" ?result "variables")
        ID = pv("cur" "value" ?result "variables")
        VG = VDC("/VG")
        VD = VDC("/VD")
        VT = pv("MN0.mx" "vth" ?result "dcOpInfo-info")
        Vdsat = pv("MN0.mx" "vdsat" ?result "dcOpInfo-info")
        VD_OV = (VDC("/VD") - pv("MN0.mx" "vdsat" ?result "dcOpInfo-info"))
        VG_OV = (VDC("/VG") - pv("MN0.mx" "vth" ?result "dcOpInfo-info"))
        gm = pv("MN0.mx" "gm" ?result "dcOpInfo-info")
        gds = pv("MN0.mx" "gds" ?result "dcOpInfo-info")

        out=outfile("./mig_extract_g65.out" "a")
        fprintf(out
"%1.3e\t%1.3e\t%1.3e\t%1.3e\t%1.3e\t%1.3e\t%1.3e\t%1.3e\t%1.3e\t%1.3e\t%1.3e\n" L S ID VG
VD VT Vdsat VD_OV VG_OV gm gds)
        close(out)
    )
)
exit
```

A.2 Amplifier Model Generator

This MATLAB amplifier model generator is used for phase margin examples in Section 3.1.1.2. This function takes as an input the amplifier DC gain, A_{DC}, the unity gain frequency, ω_{UGF}, and the phase margin, PM, and returns a transfer function object, H, as

well as the two pole locations, p_1 and p_2, required to obtain these amplifier characteristics.

```
function [H p1 p2]=amp_model(ADC, UGF, PM)
% AMP_MODEL
% Author: Mark Pude, 2010
%
% Modified: 01/04/2011 to handle PM >=90
%
% Create transfer function and pole locations for two pole amplifier model.
% [H p1 p2] = amp_model(ADC, UGF, PM)
%
% Inputs:
% ADC - DC Gain in V/V, 1000 V/V default
% UGF - Unity gain frequency in rad/s, 1 Mrad/s default
% PM - Phase margin in degrees, 60 degrees default
%
% Outputs:
% H - 'tf' object of amp model - Requires control systems toolbox
% p1 - Dominant pole location in rad/s
% p2 - Secondary pole location in rad/s
%
% NOTE:  As PM approaches 90, the required minimum
% gain for real pole locations (no imaginary component) increases (See
% Amin calculation below).
%

% Set default args if not provided
if nargin < 3, PM = 60; end
if nargin < 2, UGF = 1e6; end
if nargin < 1, ADC = 1000; end

% Basic out-of-range error checking
assert((PM > 0)&&(PM <= 180), 'PM = %d invalid. Must be between (0:180]', PM);
assert(UGF > 0, 'UGF = %d invalid. Must be a positive number', UGF);
assert(ADC > 0, 'ADC = %d invalid. Must be a positive number', ADC);

% Convert PM to rads
PM_rad = PM*pi/180;

alpha = tan(PM_rad-pi);
beta = abs(sec(PM_rad-pi));

if (PM < 90)
    % Basic two pole system, most straight forward

    % Minimum required gain for non-complex p1 and p2, for reference
    % Amin = 2*beta*(beta+1)/(beta^2-1);

    pp = UGF^2*beta*(ADC-beta)/(ADC^2-beta^2); % pole product, pp = p1*p2
    ps = -alpha * (pp - UGF^2) / UGF;          % pole sum, ps = p1 + p2

    p1 = (ps - sqrt(ps^2 - 4*pp))/2;
    p2 = ps - p1;

elseif (PM == 90)
    % No one-pole solution exists. Many non-unique two-pole solutions exist,
    % just pick one that works...

    p1 = UGF/ADC;
    p2 = UGF*ADC;

else
    % Toughest to nail down - Easiest to approximate single pole system,
    % but user still has too many variables. Modify ADC if necessary to
    % achieve UGF and PM. Give option to modify PM instead by setting
```

```
    % PM=180 in the function call
    disp('Approximating single pole system for PM > 90 (e.g. p2 = 1000x UGF).');

    if (PM ~= 180)
        disp('WARNING: For PM > 90, ADC might be modified to achieve UGF and PM');
        disp('         To override PM instead, set PM = 180 in function call.');

        p2 = 1000*UGF; % Just get it out of the way
        p1 = -UGF/alpha;

        % Find ADC value that fits UGF and PM
        ADC_new = sqrt(p1^2+UGF^2)/p1;

        % Sometimes its more trouble that its worth to change ADC, check.
        if (ADC_new > ADC)
            % Close enough to looking like PM=90 case that we don't want to
            % modify other paramters
            p1 = UGF/ADC;
            p2 = UGF*ADC;
        else
            disp(['Changing ADC from ' num2str(ADC) ' to ' num2str(ADC_new) ...
                  ' to achieve specified UGF and PM.']);
            ADC = ADC_new;
        end

    else
        disp('WARNING: For PM > 90, PM might be modified to achieve UGF and ADC');
        disp('         To override ADC instead, set PM ~= 180 in function call.');

        p2 = 1000*UGF;
        p1 = UGF/sqrt(ADC^2-1);

        % Find PM value that results from ADC and UGF
        PM_new = (atan(-sqrt(ADC^2 - 1))+pi)*180/pi;

        disp(['Changing PM from ' num2str(PM) ' to ' num2str(PM_new) ...
              ' to achieve specified UGF and ADC.']);
        PM = PM_new;
    end
end

% Return transfer function - comment out if you don't have Control System
% Toolbox
H = tf(ADC,[1/(p1*p2) (1/p1+1/p2) 1]);
```

A.3 MATLAB Optimization Code

This is the implementation of the genetic optimization algorithm discussed in Section 3.2.1.

```
clear
clc
clf

crossover = 0.7;
mutation = 0.1;
genes = 5;
vary = [0 0 0 1 1];
abs_limits =  [0 20 0 20e6 0 1e3 0 1e3 0 1e3];
init_limits = [0 20 0 20e6 0 1e3 0 1e3 0 1e3];
```

```
pop_size = 200;
gens = 1000;

r_variation = 0.2;

pop = zeros(pop_size,genes);

% pop(:,1) = init_limits(1)+(init_limits(2)-init_limits(1))*rand(pop_size,1);    %ADC
pop(:,1) = 10*ones(pop_size,1);
% pop(:,2) = init_limits(3)+(init_limits(4)-init_limits(3))*rand(pop_size,1);    %Rin
pop(:,2) = 10e6*ones(pop_size,1);
% pop(:,3) = init_limits(5)+(init_limits(6)-init_limits(5))*rand(pop_size,1);    %Rout
pop(:,3) = 200*ones(pop_size,1);
pop(:,4) = init_limits(7)+(init_limits(8)-init_limits(7))*rand(pop_size,1);    %R1
% pop(:,4) = 100*ones(pop_size,1);
pop(:,5) = init_limits(9)+(init_limits(10)-init_limits(9))*rand(pop_size,1);   %R2
% pop(:,5) = 255*ones(pop_size,1);


new_pop = pop;

for m=1:gens
    pop = new_pop;

    %check abs_limit and limits due to finite R2 range
    for i=1:pop_size
        for j=1:genes
            if (pop(i,j) < abs_limits(2*j-1))
                pop(i,j) = abs_limits(2*j-1);
            end
            if (pop(i,j) > abs_limits(2*j))
                pop(i,j) = abs_limits(2*j);
            end
        end

        ADC = pop(i,1);
        Gin = 1/pop(i,2);
        Gout = 1/pop(i,3);
        G1 = 1/pop(i,4);

        R2min(i) = -(G1+Gin+Gout*(1-ADC))/(Gout*(G1+Gin));
        R2max(i) = (G1*(1-ADC)-Gin*ADC-Gout*(1-ADC)*ADC)/(ADC*Gin*Gout);

        if (pop(i,5) < R2min(i)/(1-r_variation))
            pop(i,5) = R2min(i)/(1-r_variation);
        end
        if (pop(i,5) > R2max(i)/(1+r_variation))
            pop(i,5) = R2max(i)/(1+r_variation);
        end
    end

    %extract parameter names and call them useful variables
    ADC = pop(:,1);
    Gin = 1./pop(:,2);
    Gout = 1./pop(:,3);
    G1 = 1./pop(:,4);
    G2 = 1./pop(:,5);

    %calculate closed loop gain
    Num = G1.*(G2+ADC.*Gout);
    Den = (G1+G2+Gin).*(G2+Gout)-G2.^2-ADC.*G2.*Gout;
    HDC = Num./Den;

    %calculate sensitivites
    S_ADC  = log10(abs(Gout.*(G1+HDC.*G2)./Den));
    S_Rin  = log10(abs(Gin.^2.*(HDC.*(G2+Gout))./Den));
    S_Rout = log10(abs(Gout.^2.*(G1.*ADC-HDC.*(G1+Gin+G2.*(1-ADC)))./Den));
    S_R1   = log10(abs(G1.^2.*(G2+ADC.*Gout-HDC.*(G2+Gout))./Den));
    S_R2   = log10(abs(G2.^2.*(G1-HDC.*(G1+Gin+Gout.*(1-ADC)))./Den));

    %calculate score
```

```
    score = floor((sign(HDC./ADC-...
            1)+1)/2).*(HDC./ADC)./(S_ADC+S_Rin+S_Rout+S_R1+S_R2+500);
    score(isnan(score)) = 0;
    total = sum(score);

    %calculate average - for GUI reporting purposes only
    average(m) = mean(score);
    avg_score = average(m);
    disp(['Gen ' num2str(m) ' Average Score: ' num2str(avg_score)]);

    plot(average,'b')
    drawnow

    %pair up for mating
    for n=1:(pop_size/2)

        %first weighted pick
        pick_1 = total*rand(1);
        for i=1:pop_size
            pick_1 = pick_1 - score(i);
            if pick_1 < 0
                 break
             end
        end

        %second weighted pick
        pick_2 = total*rand(1);
        for j=1:pop_size
            pick_2 = pick_2 - score(i);
            if pick_2 < 0
                break
            end
        end

        %new genes of offspring
        new_i = pop(i,:);
        new_j = pop(j,:);

        %finite chance that genes cross over in mating at a random point
        if (rand(1) < crossover)
            break_point = ceil(genes*rand(1));
            new_i = [pop(i,1:break_point) pop(j,break_point+1:end)];
            new_j = [pop(j,1:break_point) pop(i,break_point+1:end)];
        end

        %finite chance that a mutation occurs, mutation is from 50-200%
        for i=1:genes
            if (rand(1) < mutation)
                new_i(i) = new_i(i)+vary(i)*new_i(i)*(-0.5+1.5*rand(1));
            end
            if (rand(1) < mutation)
                new_j(i) = new_j(i)+vary(i)*new_j(i)*(-0.5+1.5*rand(1));
            end
        end

        %integrate into next generation population
        new_pop(2*n-1,:) = new_i;
        new_pop(2*n,:) = new_j;
    end
end

[y i] = max(score);

disp(' ');
disp(['ADC  = ' num2str(pop(i,1)) ' V/V']);
disp(['Rin  = ' num2str(pop(i,2)/1e6) ' MOhms']);
disp(['Rout = ' num2str(pop(i,3)) ' Ohms']);
disp(['R1   = ' num2str(pop(i,4)) ' Ohms']);
disp(['R2   = ' num2str(pop(i,5)) ' Ohms']);
disp(' ');
disp(['R2min= ' num2str(R2min(i)) ' Ohms']);
```

```
disp(['R2max= ' num2str(R2max(i)) ' Ohms']);
disp(' ');
disp(['HDC  = ' num2str(HDC(i)) ' V/V']);
disp(['SADC = ' num2str(S_ADC(i))]);
disp(['SRin = ' num2str(S_Rin(i))]);
disp(['SRout= ' num2str(S_Rout(i))]);
disp(['SR1  = ' num2str(S_R1(i))]);
disp(['SR2  = ' num2str(S_R2(i))]);
```

APPENDIX B
EXTENDED POSITIVE FEEDBACK STRUCTURE ANALYSIS

The work in the body of this document primarily discusses series-shunt (or voltage-voltage) feedback systems. There are other types of feedback structures that one might be using, but the analysis is repetitive [51], [53]. As a result, these analyses are included in this appendix for completeness while not detracting from the core principles of the work.

B.1 Series-Shunt Feedback

Figure B.1 shows an example of an idea series-shunt feedback system. We start with this configuration because it is most like the block diagram analysis shown above. The ideal system in this configuration implies that the forward loop gain, $A(s)$, and feedback factor, $\beta(s)$, have infinite input impedance and zero output impedance. The name 'series-shunt' can easily identify the circuit because the input side of the circuit has the elements connected in series and the output side has them connected in parallel or 'shunt.' This system is also known as voltage-voltage feedback because a voltage is fed back and voltages are summed at the error node. As might be expected, the analysis of this system yields the same transfer function as the generalized system in Equation (3.1) and (3.2). However, this format allows further examination of the system when it is no longer ideal.

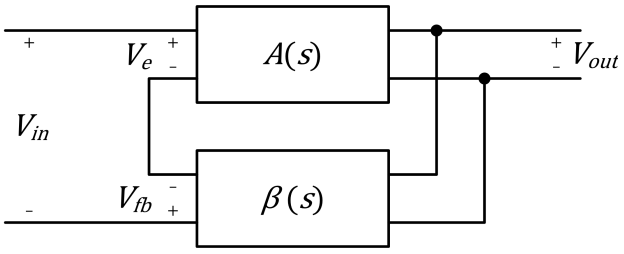

Figure B.1 Series-Shunt ideal feedback system with ideal forward voltage gain block, $A(s)$, and ideal voltage feedback factor block, $\beta(s)$.

Specifically, what happens to the transfer function when $A(s)$ and $\beta(s)$ have non-ideal input and output impedances is observed.

B.1.1 With Non-ideal Amplifier

Figure B.2 shows such a system. This system as an example has a non-ideal amplifier model with finite input impedance, Z_{in}, and non-zero output impedance, Z_{out}. The closed-loop system's input and output impedances are now non-ideal as well. Analysis of these impedances of the system in Figure B.2 gives

$$Z_{in,CL} = Z_{in}\big(1 - A(s)\beta(s)\big) \tag{B.1}$$

and

$$Z_{out,CL} = \frac{Z_{out}}{1-A(s)\beta(s)}. \tag{B.2}$$

The limitations imposed by (3.5) limit $A\beta$ to a value between 0 and 1, meaning the quantity $\big(1 - A\beta\big)$ would be valued between 0 and 1 as well. Because of this, (B.1) and (B.2) show that positive feedback in the series-shunt configuration works to decrease input impedance and increase output impedance.

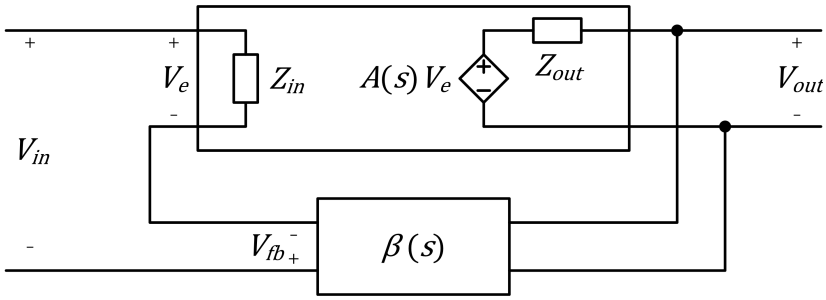

Figure B.2 Series-Shunt feedback system with non-ideal amplifier having finite input impedance Z_{in} and non-zero output impedance Z_{out}.

B.1.2 With Non-ideal Feedback Network

Figure B.3 shows a series-shunt system with a non-ideal amplifier and a non-ideal feedback network. As in [51], the feedback network is modeled as a linear two-port network model. The feedback element, G_{12}, has been removed to simplify and more closely model the analysis in [51]. Analysis of this system simplifies to

$$H(s) = \frac{A(s)\frac{Z_{in}}{Z_{in}+G_{22}^{-1}}\frac{G_{11}^{-1}}{G_{11}^{-1}+Z_{out}}}{1-G_{21}A(s)\frac{Z_{in}}{Z_{in}+G_{22}^{-1}}\frac{G_{11}^{-1}}{G_{11}^{-1}+Z_{out}}}. \tag{B.3}$$

The closed-loop transfer function in this form can be used to show the effects of these non-ideal components on the amplifier. The system can be modeled in the same form as the ideal case by redefining the open-loop gain as

$$A_{OL}(s) = A(s)\frac{Z_{in}}{Z_{in}+G_{22}^{-1}}\frac{G_{11}^{-1}}{G_{11}^{-1}+Z_{out}} \tag{B.4}$$

and the feedback factor as

$$\beta_{OL}(s) = G_{21}. \tag{B.5}$$

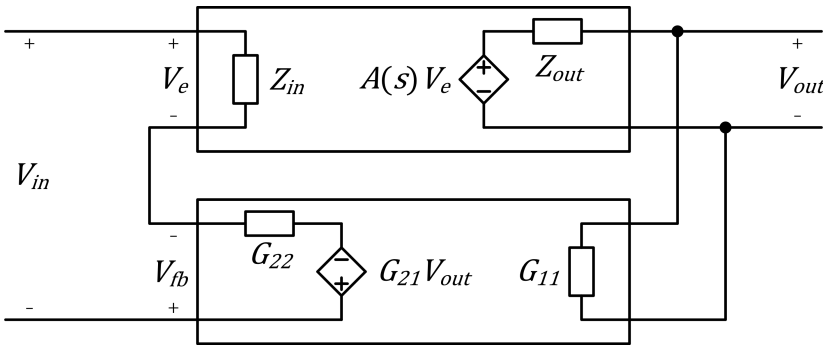

Figure B.3 Series-Shunt feedback system with non-ideal feedback network having finite input impedance G_{11}^{-1} and non-zero output impedance G_{22}^{-1}.

As (B.5) shows, the feedback factor is not degraded by the component non-idealities. All of the degradation is related to the open-loop forward gain in (B.4). Furthermore, under ideal conditions with infinite input impedance and zero output impedance, (B.4) reverts to the expected ideal case.

B.1.3 Comparison to Negative Feedback

A similar analysis for the series-shunt negative feedback system has been performed in prior work [51] and shows similar behavior in the resulting open-loop gain and feedback factor. Where positive feedback deviates from negative feedback behavior is in its effects on input and output impedance. Negative feedback's effect on input and output impedances is to further approach ideal behavior by increasing input impedance and decreasing output impedance. The denominator of the positive feedback transfer function, with its difference in sign, causes the reverse in behavior to occur.

B.2 Series-Series Feedback

The next positive feedback implementation is referred to as series-series because both input and output elements are in series with one another as shown in Figure B.4. This configuration is also known as current-voltage feedback because current is fed back and

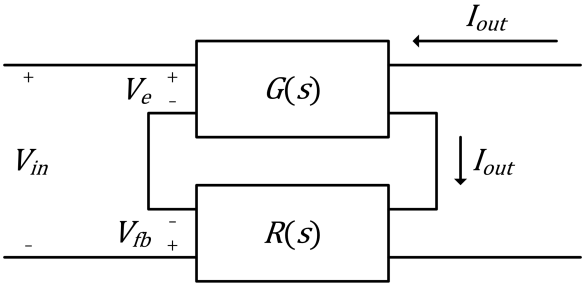

Figure B.4 Series-Series ideal feedback system with ideal forward transconductance gain block, $G(s)$, and ideal feedback transimpedance block, $R(s)$.

voltages are summed at the error node. The nature of this system is such that a voltage is put into the system and a current comes out. This means that the forward amplification path must be a transconductance, $G(s)$. Additionally, to perform the conversion in the opposite direction, the feedback network is a transimpedance, $R(s)$. The resulting closed-loop transfer function of this system looks similar to the previous systems

$$H(s) = \frac{I_{out}}{V_{in}} = \frac{G(s)}{1-G(s)R(s)}. \tag{B.6}$$

Assuming a single pole $G(s)$ with DC transconductance G_{DC}, a frequency-independent feedback factor R, and a primary pole located at p_1, the closed-loop system becomes

$$H(s) = \frac{G_{DC}p_1}{s+p_1(1-G_{DC}R)} \tag{B.7}$$

with a DC gain of $G_{DC}/(1 - G_{DC}R)$ and a -3dB bandwidth of $p_1(1 - G_{DC}R)$. To avoid right-half-plane poles, the feedback factor R must be chosen between

$$0 < R < \frac{1}{G_{DC}}. \tag{B.8}$$

B.2.1 With Non-ideal Amplifier

To evaluate the series-series effects on input and output impedance, Figure B.5 shows the system with a non-ideal amplifier. In the case of the transconductance amplifier, the modeled non-idealities include finite input impedance, Z_{in}, as well as finite output impedance, Z_{out}. Analysis of this system shows the input impedance of the closed-loop system becomes

$$Z_{in,CL} = Z_{in}\big(1 - G(s)R(s)\big) \tag{B.9}$$

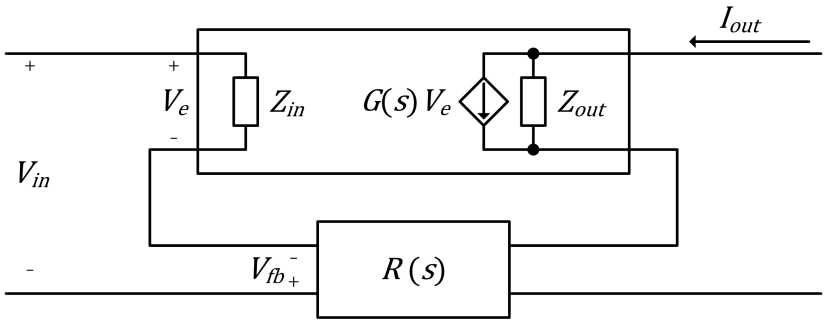

Figure B.5 Series-Series feedback system with non-ideal amplifier having finite input impedance, Z_{in}, and finite output impedance Z_{out}.

and the output impedance becomes

$$Z_{out,CL} = Z_{out}\big(1 - G(s)R(s)\big). \tag{B.10}$$

As was the case with previous positive feedback implementations, both input and output impedances are degraded from their ideals. Ideal input and output impedances would be high numbers in both cases, and the limitations on R shown in (B.8) imply that both would be reduced from their open-loop values.

B.2.2 With Non-ideal Feedback Network

Finally, the complete non-ideal system is shown in Figure B.6. The feedback network has been replaced with a linear two-port Z-model. Analysis of this system yields the

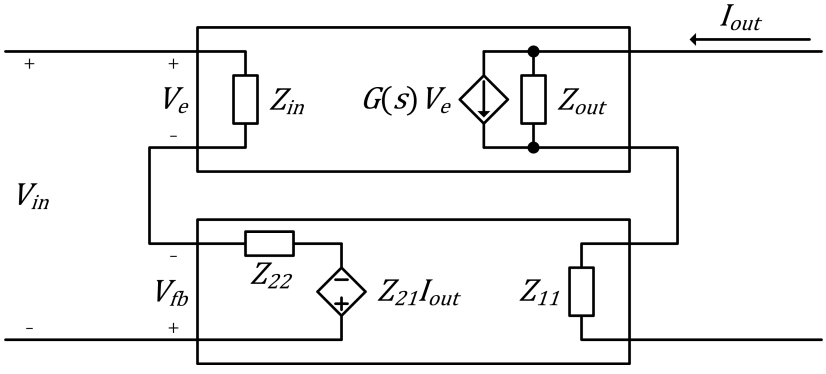

Figure B.6 Series-Series feedback system with non-ideal feedback network having non-zero input impedance, Z_{11}, and non-zero output impedance Z_{22}.

following transfer function

$$H(s) = \frac{I_{out}}{V_{in}} = \frac{G(s)\frac{Z_{in}}{Z_{in}+Z_{22}}\frac{Z_{out}}{Z_{out}+Z_{11}}}{1-Z_{21}G(s)\frac{Z_{in}}{Z_{in}+Z_{22}}\frac{Z_{out}}{Z_{out}+Z_{11}}}. \quad \text{(B.11)}$$

This can be broken down into an open-loop gain of

$$G_{OL}(s) = G(s)\frac{Z_{in}}{Z_{in}+Z_{22}}\frac{Z_{out}}{Z_{out}+Z_{11}} \quad \text{(B.12)}$$

and a feedback factor of

$$R_{OL}(s) = Z_{21}. \quad \text{(B.13)}$$

As was the case in the series-shunt configuration, non-ideal degradation manifests itself in the open-loop gain expression. In the idealized case of large Z_{in} and Z_{out}, this expression simplifies to the expected ideal results.

B.2.3 Comparison to Negative Feedback

As was similar with the series-shunt configuration, the open-loop gain and feedback factor expressions remain unchanged from negative feedback to positive feedback. The effects of positive feedback on the nature of the input and output impedances, however, are negative in that they reduce ideally high values to low values based on the loop gain.

B.3 Shunt-Shunt Feedback

The third type of feedback topology is shunt-shunt. This means that both the input side and the output side are connected in parallel. This structure is also known as voltage-current feedback because a voltage is fed back and currents are summed at the error node. This structure, shown in Figure B.7, is current in and voltage out and therefore its

forward gain is a transimpedance and its feedback network is a transconductance. The closed-loop transfer function, similar in structure to the previous configurations, of this system is

$$H(s) = \frac{V_{out}}{I_{in}} = \frac{R(s)}{1-R(s)G(s)}. \tag{B.14}$$

To obtain the range of valid frequency-independent feedback factors, G, we replace $R(s)$ with the single pole approximation with a -3 dB bandwidth of p_1 and a DC transimpedance of R_{DC}. This results in the open-loop transfer function of

$$H(s) = \frac{R_{DC}p_1}{s+p_1(1-R_{DC}G)} \tag{B.15}$$

with DC gain of $R_{DC}/(1 - R_{DC}G)$ and a -3 dB bandwidth of $p_1(1 - R_{DC}G)$. Based on the stability criterion of left-half-plane poles, the feedback factor range can be shown as

$$0 < G < \frac{1}{R_{DC}}. \tag{B.16}$$

B.3.1 With Non-ideal Amplifier

To illustrate the impact of shunt-shunt feedback on the input and output impedance of the open-loop amplifier, the forward path is replaced with a non-ideal amplifier model as

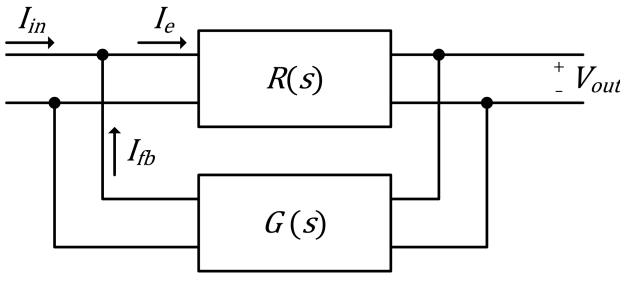

Figure B.7 Shunt-Shunt ideal feedback system with ideal forward transimpedance, $R(s)$, and ideal feedback transconductance, $G(s)$.

shown in Figure B.8. This non-ideal transimpedance amplifier model has non-zero input impedance, Z_{in}, and non-zero output impedance, Z_{out}.

$$Z_{in.CL} = \frac{Z_{in}}{1-R(s)G(s)} \tag{B.17}$$

$$Z_{out,CL} = \frac{Z_{out}}{1-R(s)G(s)} \tag{B.18}$$

Equations (B.17) and (B.18) show that shunt-shunt feedback, again, degrades Z_{in} and Z_{out} from their ideal low values.

B.3.2 With Non-ideal Feedback Network

To complete the analysis on the shunt-shunt feedback system, the feedback network is replaced with a Y model network of admittances as shown in Figure B.9. Analysis of this circuit gives the following transfer function

$$H(s) = \frac{R(s)\frac{Y_{22}^{-1}}{Y_{22}^{-1}+Z_{in}}\frac{Y_{11}^{-1}}{Y_{11}^{-1}+Z_{out}}}{1-Y_{21}R(s)\frac{Y_{22}^{-1}}{Y_{22}^{-1}+Z_{in}}\frac{Y_{11}^{-1}}{Y_{11}^{-1}+Z_{out}}}. \tag{B.19}$$

Molding this into the format of the ideal system, the open-loop transimpedance becomes

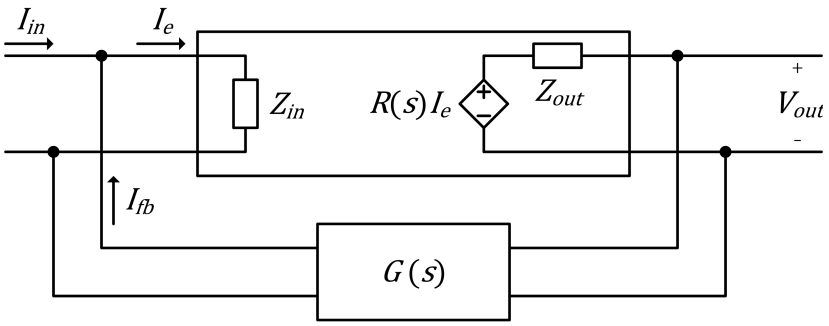

Figure B.8 Shunt-Shunt feedback system with non-ideal amplifier having non-zero input impedance, Z_{in}, and non-zero output impedance, Z_{out}.

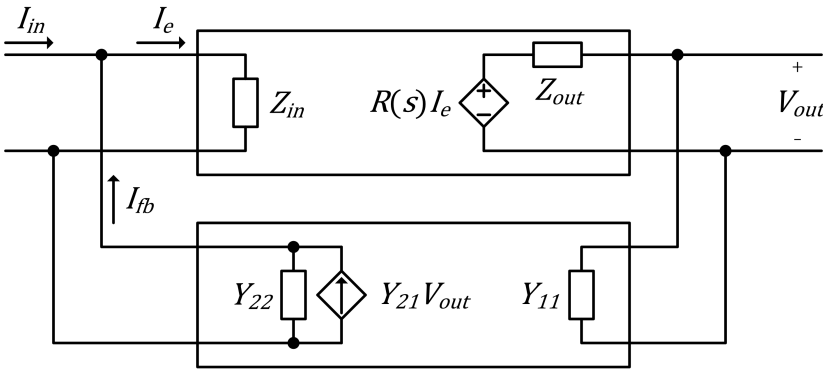

Figure B.9 Shunt-Shunt feedback system with non-ideal feedback network having finite input impedance, Y_{11}^{-1}, and finite output impedance, Y_{22}^{-1}.

$$R_{OL}(s) = R(s)\frac{Y_{22}^{-1}}{Y_{22}^{-1}+Z_{in}}\frac{Y_{11}^{-1}}{Y_{11}^{-1}+Z_{out}} \tag{B.20}$$

and the open-loop feedback factor is

$$\mathrm{G_{OL}(s) = Y_{21}}. \tag{B.21}$$

Degradation in the open-loop transfer function due to loading by non-idealities occurs in the open-loop gain and not in the feedback factor.

B.3.3 Comparison to Negative Feedback

Continuing with the anti-parallels to negative feedback, shunt-shunt feedback acts to further degrade amplifier non-idealities, while negative feedback improves them. The forward gain, however, is improved.

B.4 Shunt-Series Feedback

The final permutation of positive feedback configuration is the shunt-series configuration: the input side is placed in parallel and the output side is placed in series. This is also known as current-current feedback because a current is fed back and currents are summed at the error node. With current in and current out of the system, the feed-

forward and feedback nomenclature returns to a current gain, $A(s)$, and a unit-less feedback factor $\beta(s)$. Analysis of the shunt-series feedback system, shown in Figure B.10, yields a familiar result

$$H(s) = \frac{I_{out}}{I_{in}} = \frac{A(s)}{1-A(s)\beta(s)}. \tag{B.22}$$

To observe the stability requirement, we replace $A(s)$ with a single-pole model with DC gain of A_{DC} and -3 dB bandwidth p_1, and obtain a transfer function

$$H(s) = \frac{A_{DC}p_1}{s+p_1(1-A_{DC}\beta)} \tag{B.23}$$

with DC gain of $A_{DC}/(1 - A_{DC}\beta)$ and -3 dB bandwidth of $p_1(1 - A_{DC}\beta)$. To avoid right-half-plane poles, the β restriction is

$$0 < \beta < \frac{1}{A_{DC}}. \tag{B.24}$$

B.4.1 With Non-ideal Amplifier

Replacing the current mode amplifier with a non-ideal model, we can observe the effects on input and output impedances. The non-ideal model has non-zero input impedance, Z_{in}, and finite output impedance, Z_{out}. The model including these non-idealities is shown in

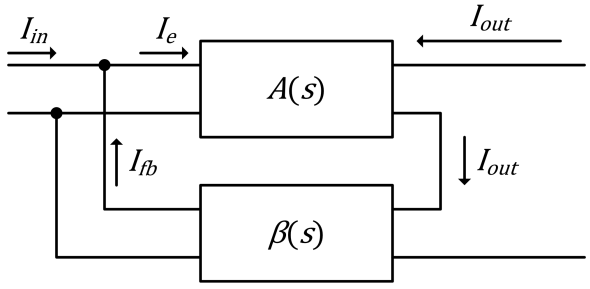

Figure B.10 Shunt-Series ideal feedback system with ideal forward current gain, $A(s)$, and ideal feedback current factor, $\beta(s)$.

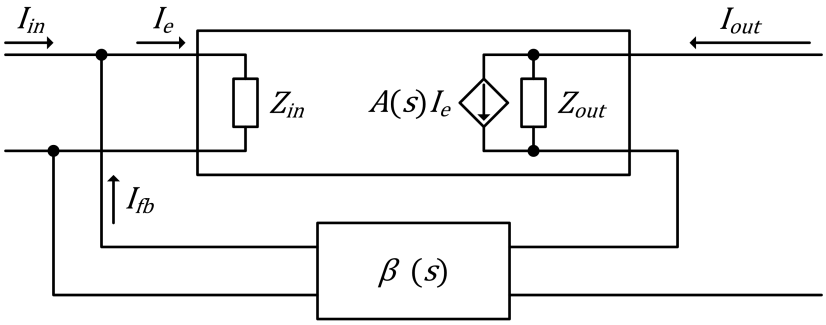

Figure B.11 Shunt-Series feedback system with non-ideal amplifier having non-zero input impedance, Z_{in}, and finite output impedance, Z_{out}.

Figure B.11. Analysis shows the effects on input impedance to be

$$Z_{in,CL} = \frac{Z_{in}}{1-A(s)\beta(s)} \tag{B.25}$$

and output impedance

$$Z_{out,CL} = Z_{out}\big(1 - A(s)\beta(s)\big). \tag{B.26}$$

The closed-loop input impedance is increased, a departure from ideal. The output impedance is reduced, another departure from idea.

B.4.2 With Non-ideal Feedback Network

The feedback network is replaced with a non-ideal hybrid model shown in Figure B.12. This hybrid network changes the transfer function of the shunt-shunt feedback system to

$$H(s) = \frac{G(s)\frac{H_{22}^{-1}}{H_{22}^{-1}+Z_{in}}\frac{Z_{out}}{Z_{out}+H_{11}^{-1}}}{1-H_{21}G(s)\frac{H_{22}^{-1}}{H_{22}^{-1}+Z_{in}}\frac{Z_{out}}{Z_{out}+H_{11}^{-1}}}. \tag{B.27}$$

Formatting this into the ideal format, the open-loop gain becomes

$$A_{OL}(s) = G(s)\frac{H_{22}^{-1}}{H_{22}^{-1}+Z_{in}}\frac{Z_{out}}{Z_{out}+H_{11}^{-1}} \tag{B.28}$$

and the feedback factor becomes

$$\beta_{OL}(s) = H_{21}. \tag{B.29}$$

The open-loop gain is degraded by the circuit non-idealities, but the feedback factor remains as expected.

B.4.3 Comparison to Negative Feedback

This final implementation suffers from the same effects of the previous three: most open-loop parameters are sacrificed in order to improve open-loop gain.

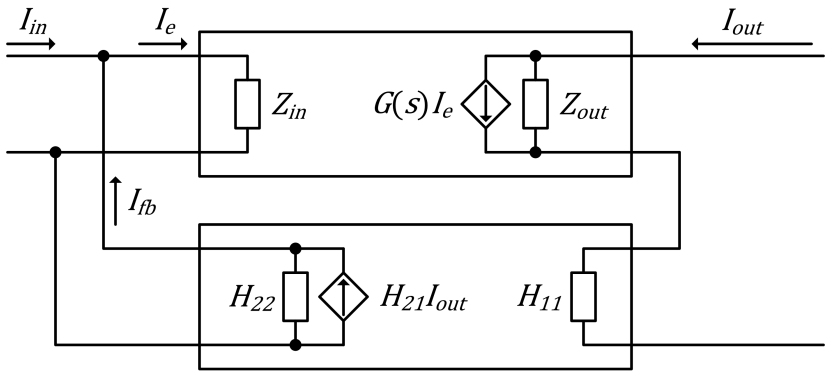

Figure B.12 Shunt-Series feedback system with non-ideal feedback network having non-zero input impedance, H_{11}^{-1}, and finite output impedance, H_{22}^{-1}.

APPENDIX C
MIXED-MODE S-PARAMETERS

The four-port s-parameter measurement methodology used in Section 4.2.2 works by stimulating one of the four ports with an incident power wave while simultaneously measuring the impact of that stimulus on all four terminals with proper termination. This measurement is repeated on the remaining three ports at a given frequency and combined into a matrix. Using superposition, the reflected power waves can be expressed as a combination of the S-parameters and incident power waves. The input frequency can then be swept to obtain the four-port S-parameters over a given frequency range.

Quantitatively, this can be described by

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} = S_{std} \cdot \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \tag{C.1}$$

and the system shown in Figure C.1 where a_n is the incident power wave and b_n is the reflected power wave of the n^{th} port of the four-port network. For a two-port network,

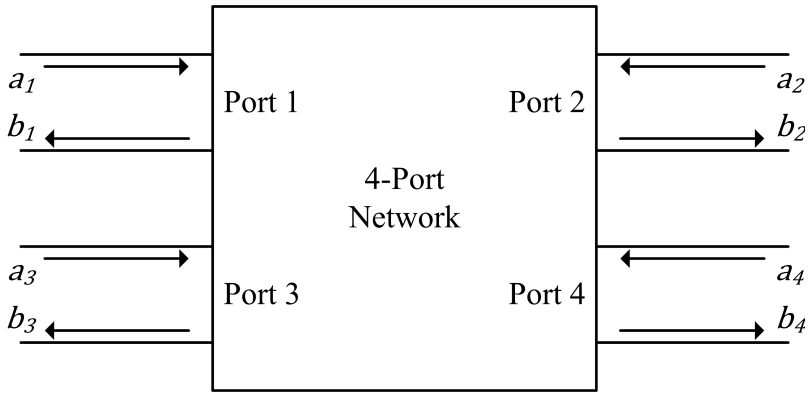

Figure C.1 Four-port network for s-parameter analysis showing incident and reflected power waves.

this s-parameter information can easily be transformed into other network types – Y, Z, H, etc. – for circuit analysis. In the case of the four-port system in this work, however, the data must be manipulated into a useful format before it can be analyzed.

The methodology of mixed-mode S-parameters was introduced to analyze fully differential systems [92], [93] like the amplifiers presented in this work. This methodology assumes that the four inputs are used as two differential pairs, one for the differential input and one for the differential output as shown in Figure C.2. This system assumes that the differential input port, Port 1_{mm}, consists of Port 1 and Port 3 of the four-port system, and the differential output port, Port 2_{mm}, consists of Port 2 and Port 4 of the four-port system. It utilizes a conversion from traditional four-port S-parameters to a set of S-parameters that describe differential- and common-mode behavior as in

$$\begin{bmatrix} b_{\mathrm{d1}} \\ b_{\mathrm{d2}} \\ b_{\mathrm{c1}} \\ b_{\mathrm{c2}} \end{bmatrix} = \begin{bmatrix} S_{\mathrm{dd}} & S_{\mathrm{dc}} \\ S_{\mathrm{cd}} & S_{\mathrm{cc}} \end{bmatrix} \cdot \begin{bmatrix} a_{\mathrm{d1}} \\ a_{\mathrm{d2}} \\ a_{\mathrm{c1}} \\ a_{\mathrm{c2}} \end{bmatrix} = S_{mm} \cdot \begin{bmatrix} a_{\mathrm{d1}} \\ a_{\mathrm{d2}} \\ a_{\mathrm{c1}} \\ a_{\mathrm{c2}} \end{bmatrix} \tag{C.2}$$

where a_{dc} and b_{dn} are the differential-mode incident and reflected power waves for the

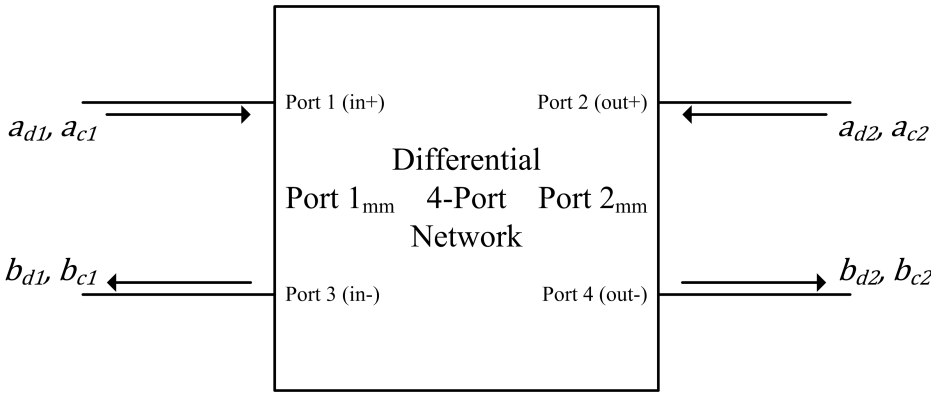

Figure C.2 Four-port network for a differential system showing incident and reflected power waves for common-mode and differential mode.

n^{th} differential port, and a_{cn} and b_{cn} are the common-mode incident and reflected power waves for the n^{th} differential port. S_{dd} is a 2×2 sub-matrix describing the differential S-parameters, S_{cc} is a sub-matrix describing the common-mode S-parameters, and S_{dc} and S_{cd} are the conversion-mode parameters describing the conversion of differential power waves into common-mode power waves and vice versa.

Conversion from normal four-port S-parameters to mixed-mode parameters can be achieved with the transformation matrix described in [92],

$$M = \frac{1}{\sqrt{2}}\begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \tag{C.3}$$

and the equation

$$S_{mm} = MS_{std}M^{-1} \tag{C.4}$$

where

$$M^{-1} = M^{T} = \frac{1}{\sqrt{2}}\begin{bmatrix} 1 & 0 & 1 & 0 \\ -1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & -1 & 0 & 1 \end{bmatrix}. \tag{C.5}$$

This conversion is easily implemented in MATLAB and has even been built into the RF toolbox. With these tools, the fully differential behavior of the silicon measurements can be analyzed and converted into voltage gain and phase as displayed in Section 4.2.2.