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Concept, design, simulation, and fabrication of an ultra-scalable vertical MOSFET

Keith H. Tabakman

Concept, Design, Simulation, and Fabrication of an Ultra-Scalable Vertical MOSFET

By

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July 26th, 2003

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Abstract

A new orientation to the conventional MOSFET is proposed. Processing issues, as well as short channel effects have been making planar MOSFET scaling increasingly difficult. It is predicted by the 2001 International Technology Roadmap for Semiconductors (ITRS) that non-planar devices will be needed for production as early as 2007. The device proposed in this thesis is similar in operation to the planar MOSFET, however the current transport from source to drain, normally in the same plane as the wafer surface, is oriented perpendicular to the die surface. The proposed device has successfully been simulated, showing a proof of concept. Fabrication of the proposed devices led to the creation of vertical MOS Gated Tunnel Diodes. This work, in fact, represents possibly the first demonstration of this type of technology. Suggestions are made to improve upon the proposed vertical MOSFET as well as the vertical MOS Gated Tunnel Diode.

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Chapter 1

INTRODUCTION AND MOTIVATION

The fuel of the integrated electronics industry is the transistor. In 1965, Gordon E. Moore (Intel Corp.), made his famous prediction that the number of transistors per square inch on an integrated circuit would double every 18 months [1]. The scaling of the transistors in integrated circuits allows for four major improvements (i) higher speed (ii) lower power (iii) higher density and (iv) lower cost. In all of manufacturing history, no other product has exhibited the characteristics of the transistor, in which the speed increases and the cost of production decreases as the size is reduced [2]. Over the past twenty years, the speed of the transistor has increased 20 times and the size has shrunk to occupy less that 1% of the area originally required.

By demonstrating smaller and faster devices the world has become hungry for more performance and integration. This has accelerated the scaling trends of lithography, the effective channel length (L_{eff}), the gate dielectric thickness (t_{ox}), supply voltage, device leakage, etc [3]. Many innovations have gone into extending the life of the MOSFET such as the use of strained silicon [4], silicon on oxide [5], and pocket / halo implants [6,7]. However, even with all of these additions it is widely accepted that at

some point, the physical challenges that impede the transistor's progress will overcome the research thrusts powering Moore's law. These challenges take the form of process related as well as physics related issues.

The International Technology Roadmap for Semiconductors (ITRS) [3], developed by International SEMATECH in communications with the Semiconductor Industry Association (SIA), the European Electronic Component Association (EECA), the Japan Electronics and Information Technology Industries Association (JEITA), the Korean Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA), predicts the future of the integrated circuit industry. The roadmap outlines the needs of future process technologies in order to realize the aggressive scaling defined by Moore's law.

The long-term challenges identified in the 2001 ITRS roadmap are control of critical dimensions as well as L_{eff}, high-k materials as gate insulators due to the extremely thin nature of these films, the thermal stability of these high-k films, and the use of metal gates just to name a few. These issues are currently in research, however none of which has an answer ready to move to the manufacturing sector. These technologies, however, are projected to be ready (or necessary) by 2006-7 [3].

Additionally the roadmap identifies future technologies that may eventually overcome the planar transistor in order to prolong the effectiveness of Moore's law (figure 1.1). Many methods for achieving the process technologies needed for future scaling of the planar MOSFET are not known.

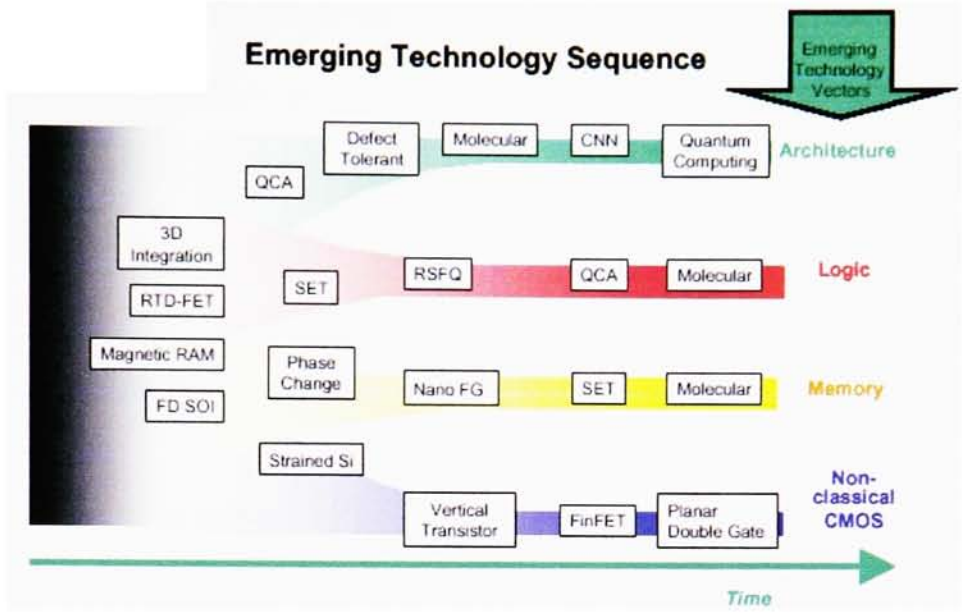

Figure 1.1: The future of semiconductor devices predicted by the 2001 ITRS

Strained Si, in which the active area silicon is stretched increasing carrier mobility, is already being used in the most advanced production integrated circuits. Strained Si is described in Chapter 2 in more detail. Much work has shown the improved scalability of the finFET [8-10], however, the finFET device is still limited by the process technologies currently under question by the ITRS. The use of the extremely thin fins of the finFET raises some concern with series resistances. In addition, the gate length of the finFET is still ultimately defined by lithography and etching techniques, and is subject to process variations [11]. Some work has recently been presented on the Vertical Transistor (VMOSFET), this device similarly exhibits improved scalability over the planar MOSFET. However, the VMOSFET does benefit from relaxed requirements of the process technologies currently under question [12,13].

1.1 Vertical MOSFET Features

The Vertical MOSFET proposed in this study features three major points (i) the channel is oriented perpendicular to the plane of the starting substrate, (ii) the device is created almost wholly through the process of epitaxy, and (iii) delta-doping planes exist between each source / drain and the channel. Figure 1.2 compares a planar MOSFET to the proposed Vertical MOSFET device.

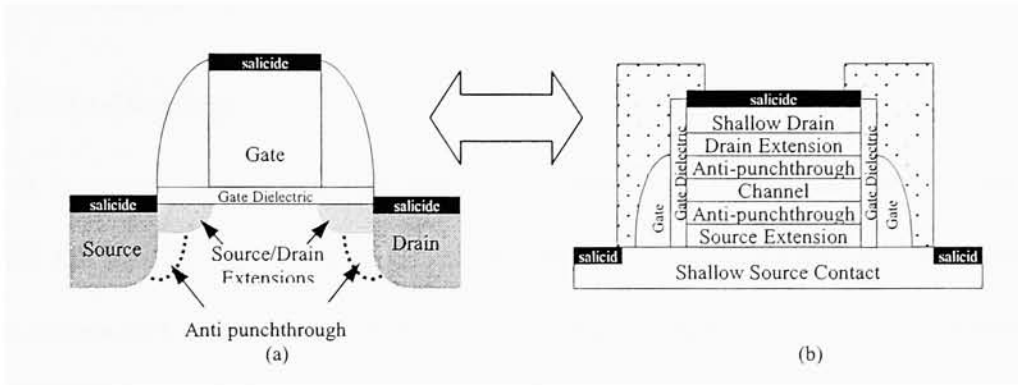

Figure 1.2: Comparison of a planar MOSFET (a) and the proposed Vertical MOSFET (b)

1.1.1 Vertical Channel

The channel region of the proposed Vertical MOSFET is oriented such that the direction of current flow is perpendicular to the surface of the starting substrate. Using advanced lithography and etching techniques then, a fully depleted structure may be made in a similar method to finFETs [8,10,13] or SOI MOSFETs [10].

It is observed that the channel region exists completely above the surface of the substrate. The channel region is completely surrounded by the gate. Since the channel does not reside in the bulk the device is essentially built in an SOI fashion. Due to the fully surrounding nature of the gate, the gate acts to shield the device making it increasingly resistance to soft errors.

1.1.2 Epitaxy

Molecular Beam Epitaxy (MBE) is used to define the device doping profiles. MBE is capable of growing atomic thickness films. Because of this the doping profiles can be controlled extremely well. Junctions may be made very abrupt, and the use of MBE allows for the use of delta-doping [14]. The doping of the channel region may be tailored to alter the electric field properties within the channel, aiding carrier transport in the desired direction.

1.1.3 Delta-Doping

It is our hypothesis that this layer is essential to the scalability of the vertical MOSFET device. The delta-doped layer is doped at a significantly higher concentration then the source and drain regions. Because of this the δ-doped layers effectively balances the charges between the channel and source or drain within a depletion region extending into the source or drain and terminating at the δ-doping plane.

The control of the depletion regions acts similar to that of pocket, or halo implants in today's planar CMOS devices. Since the delta-doped region exists everywhere between the source / drain and the channel, the possibility of punch-through is almost eliminated.

Straddling the δ-doped plane are very thin layers of SiGe. It has been shown that diffusion of p-type dopants is retarded in the presence of Ge [15]. This aids in keeping the δ -doping plane extremely thin, increasing the probability of tunneling, as the δ doping plane is not intended to limit current flow in the devices on-state.

1.2 Vertical MOSFET Benefits

1.2.1 Higher Speed

In the on state, a majority carrier from a MOSFET's source terminal is injected into the channel region. Due to interactions with the crystalline structure of the semiconductor, a collision, or scattering event is statistically inevitable. The statistical mean of the time it takes for a carrier to experience a scattering event is known as the mean free time. A similar explanation can be given to the mean free path. Using these two statistical pieces of information one may determine a maximum velocity at which the average carrier may move throughout the semiconductor. A long channel transistor in its normal on state, is generally in the saturation region of operation. In this region, carriers within the channel move with the saturation velocity.

It is obvious then, that by decreasing the distance between the source and the drain of a MOSFET device, the time it takes for a carrier to travel this distance is decreased. This in turn increases the speed of the device.

The probability of a collision is proportional to the electric field in the channel of the transistor, increasing towards the drain of the device. The field strength increases as the channel length of the transistors decreases. These collisions can create electron-hole pairs. The created electrons can be injected into the gate oxide degrading its quality while the hole may be swept into the bulk creating a potential drop in the bulk, which may lead to snapback. By controlling the depletion regions within the channel, the speed of the Vertical MOSFET benefits in three ways: (1) by limiting the depletion width into the channel, the source and drain may be brought closer together without fears of short channel effects dominating device operation; (2) by controlling the electric fields within

the channel, hot carrier effects are less likely; (3) the charge balance occurs between the delta-doped regions and the source/drains allowing for reduced channel doping.

1.2.2 Lower Power

Associated with the decreased length of the MOSFET channel is a decrease in the power supply voltage. This is done to maintain a constant field in the device throughout the scaling process. While the decrease in power helps in controlling short channel effects created by high fields within the device, a certain potential range must be maintained in order to extend the usability of the small transistor in integrated circuits.

A significant portion of the total power used by a chip is the standby power associated with transistors not being used. This standby power becomes even more significant as leakage currents increase with decreased device dimensions. It is very important, then, to minimize this leakage current, more commonly known as the off state current or I_{off}. I_{off} occurs due to drift and diffusion within the MOSFETs junctions. The use of epitaxy to define the source, channel, and drain of the vertical MOSFET limits some of this leakage current, by creating extremely abrupt junctions with little damage. Damage associated with high-energy particles, such as those found in plasmas, have been shown to create defects that increase leakage currents [16]. If the damage induced by the ion implantation process is not properly annealed out, it will cause excessive leakage current. The vertical MOSFET device is essentially built by epitaxy. Defects can be present in epitaxially grown layers, however the density of the majority defects is significantly reduced if the process temperature is kept above 600°C [17]. By using the epitaxy process, ion implantation is not used.

It is predicted that the use of delta-doping planes will assist in minimizing leakage current.

1.2.2 Higher Density

The vertical MOSFET leads to a significant jump in the achievable density of integrated circuits [3]. By aligning the device such that the drain is directly on top of the source, the real estate taken up by these regions will decrease. Various methods have been identified, of stacking the vertical devices in order to create multiple transistor gates with the footprint of one such transistor.

1.2.3 Lower Cost

No advanced device can be considered for manufacturing before it can be shown that the cost of producing integrated circuits would be no more expensive, if not less expensive of those being created today. Taking into account the increasing number of interconnect levels in the backend processing of modern IC's, the back end accounts for a significant portion of fabrication costs. Since the fabrication details of the vertical MOSFET device proposed in this study includes no ion implant steps, a decreased number of masking levels, and a lower thermal budget, the cost of producing IC's using the vertical MOSFET process will be less than that of the IC's being produced today.

It should be noted that in the past the epitaxy process has been considered a lengthy and expensive process. The major disadvantage for epitaxy is throughput, as it is often a single-wafer at a time process. Single wafer systems, however, have been optimized to the point that they not only approach, but in some cases exceed batch processes [18]. More and more planar MOSFET devices are beginning to use epitaxy

due to decreased junction depths. The tightening of specifications has reached the point at which epitaxial substrates are required. The profitability of polished wafer products has been deteriorating while the margins in epitaxial wafer preparation remain decent [19].

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Chapter 2

BACKGROUND

As the need for smaller, faster, and cheaper devices speeds up, the need for advanced device structures becomes more and more evident. Many advanced devices have been proposed and explored. The three major competing technologies are those of advanced planar MOSFETs, Multiple Gate Ultra-thin Body Sidewall FETs, and Vertical MOSFETs. In this chapter, each device will be discussed, along with processing details and resulting electrical characteristics. It is important, in comparison, to discuss competing device technologies in terms of the metrics involved in characterizing the devices.

2.1 Device Metrics

2.1.1 On and Off State Currents

According to the 2001 ITRS [18,19], the device metric CV/I can be used to estimate device switching speed. The metric can be derived from intrinsic device capacitances, the voltage swing necessary to drive a following stage, and the drive current. Since the intrinsic capacitances are proportional to device size the CV/I metric is

independent of device size. From this definition it can be determined that drive or on-state current in a device is an important metric when attempting to design fast devices. Often the on state current for a device is reported at a constant off state or standby current.

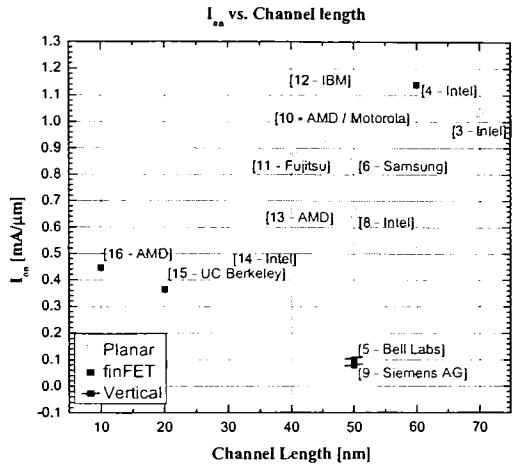

Figure 2.1: Typical Drive Currents vs. Channel Length

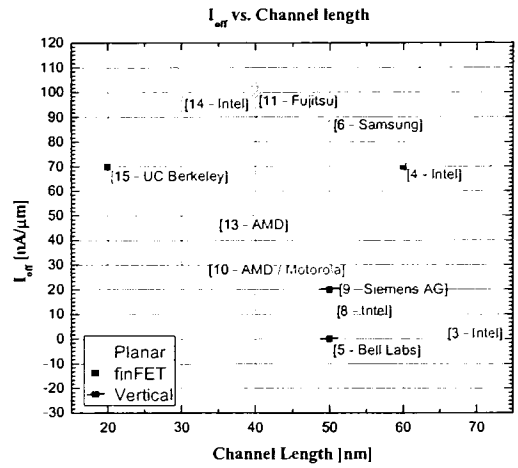

Figure 2.2: Typical Leakage Currents vs. Channel Length

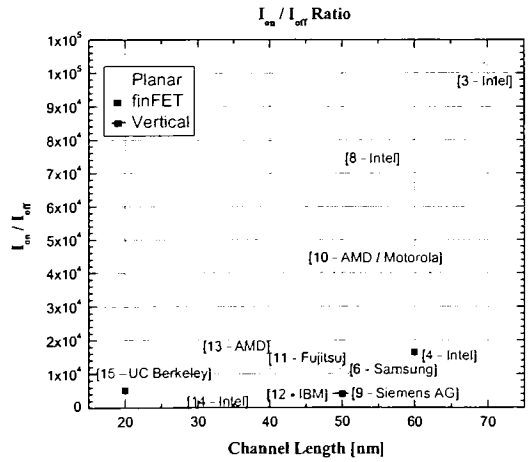

Figure 2.3: Ion / Ioff Ratio vs. Channel Length

Figures 2.1 and 2.2 show some typical on and off state currents with respect to channel length. Figure 2.3 illustrates a ratio of on to off state current. Taking 50nA/µm

as an average value, and assuming that 1/3 of the transistors on an integrated circuit are on, and that the IC contains a million transistors, the leakage current due to transistors in standby mode would be 33mA. 33mA is not a large leakage current, but considering today's integrated circuits are approaching 1 billion transistors, the standby current using the same parameters would be 33 Amps! It is easy to see, then, that it is important to keep the off state current low. Table 2.1 illustrates the 2001 ITRS requirements for I_{on} and I_{off} parameters through 2016 [18] where 'MPU' stands for Microprocessor Unit, 'LOP' stands for Low Operating Power, and 'LSTP' stands for Low Standby Power.

Ion [μA/μm]												
Year	1999	2000	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
MPU	1041	1022	926	959	967	954	924	960	1091	1250	1492	1507
LOP	636	591	600	600	600	600	600	600	700	700	800	900
LSTP	300	300	300	300	400	400	400	400	500	500	600	800
Ioff [μA/μm]												
Year	1999	2000	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
MPU	0 .	0.01	0.01	0.03	0.07	0.1	0.3	0.7	1	3	7	10
LOP	1.0E-04	1.0E-04	1.0E-04	1.0E-04	1.0E-04	3.0E-04	3.0E-04	3.0E-04	7.0E-04	1.0E-03	3.0E-03	1.0E-02
LSTP	1.0E-06	1.0E-06	1.0E-06	1.0E-06	1.0E-06	1.0E-06	1.0E-06	1.0E-06	1.0E-06	3.0E-06	7.0E-06	1.0E-05

Table 2.1: ITRS Ion/Ioff Requirements (2001 ITRS)

A transistor, in the digital sense is essentially a switch. In order for the switch to be effective the ratio between on state current and off state current must be large, otherwise there would be no way to reliably chain millions of transistors together while considering the noise margins associated with each gate.

2.1.2 Subthreshold Characteristics

As mentioned above, the range of on current to off current is important in modern semiconductor devices. The rate of this turn off region is extremely important. The

subthreshold slope is defined by equation 2.1. The subthreshold slope is considered to indicate how well a transistor turns off.

$$S = \left(\frac{\partial \left(\log_{10} I_{ds} \right)}{\partial V_g} \right)^{-1} = 2.3 \frac{kT}{q} \left(1 + \frac{C_{dm}}{C_{ox}} \right) \qquad \text{Equation 2.1}$$

In equation 2.1, C_{dm} is the depletion layer capacitance [19]. The subthreshold slope is reported in terms of mV per decade of current. The theoretical limit of subthreshold slope is kT/q or the thermal energy of carriers, however typical values of the subthreshold slope are between 70 to 100 mV/decade. Figure 2.4 show typical subthreshold characteristics for current research devices vs. their channel lengths.

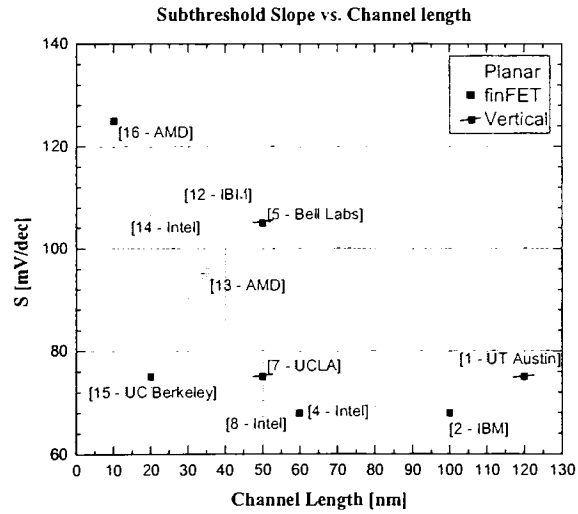

Figure 2.4: Typical Subthreshold Characteristics vs. Channel Length

In order to control subthreshold characteristics, the insulator separating the gate from the channel of MOSFETs has decreased to thicknesses on the order of a few angstroms.

2.1.3 Drain Induced Barrier Lowering

Drain Induced Barrier Lowering (DIBL) describes the effect the drain potential has on the threshold voltage of a transistor. As a reverse bias is applied to one p-n junction a field pattern is created that can lower potential barriers separating the junction from an adjacent junction. If this lowering of the barrier is significant enough the adjacent junction behaves as a source of carriers, resulting in undesirable current.

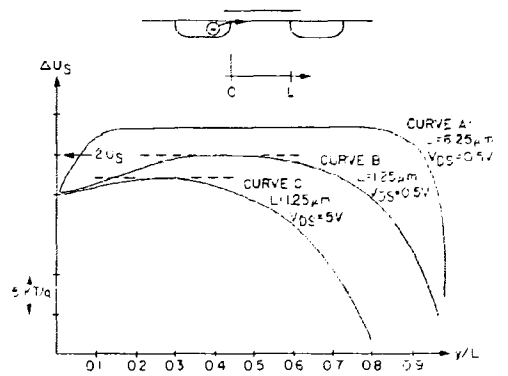

Figure 2.5: An Illustration of DIBL (figure adapted from [20])

In order to control the barrier lowering in modern devices, channel doping has increased significantly. The use of super-steep retrograde wells (SSRW), and halo or pocket implants, performed to place highly doped, channel-type, regions immediately below the source/drain extensions helps limit DIBL. Figure 2.6 illustrates typical DIBL parameter values versus channel length in modern research devices.

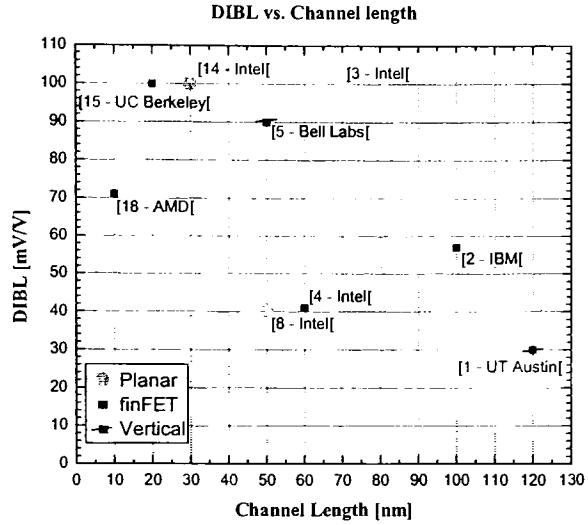

Figure 2.6: Typical DIBL vs. Channel Length

2.2 Advanced Planar MOSFETs

The original design for a planar MOSFET required very few doping steps, solid-source diffusion or implant. The device featured two similar-type diffused regions separated by an alternate type channel region. A metal gate was placed above a thin insulator. However, as device dimensions shrunk the need for adjustments to the device arose. For example, in order to integrate devices a controlled threshold voltage is required. In order to accomplish this, additional implants must be preformed in the channel region during device fabrication. Similar additions such as retrograde well implants, source/drain extensions, silicidation, and isolation have been added to the fabrication process. The channel length of the planar device is limited to the availability of advanced lithography and etch-back techniques.

However, all of these additions still cannot completely control the short channel effects that dominate device characteristics of deep submicron and nanoscale devices. Because of this more advancements have been proposed to the planar MOSFET.

2.2.1 Silicon On Insulator

Devices built on a thin layer of crystalline silicon above an insulator were first reported in the 1960's in order to produce devices that were fast, low power, and well isolated [23]. The devices were built on silicon-on-sapphire substrates. Currently Silicon on Insulator (SOI) substrates feature a thin device region separated from bulk silicon by a silicon dioxide layer. Figure 2.7 illustrates CMOS built on an SOI substrate.

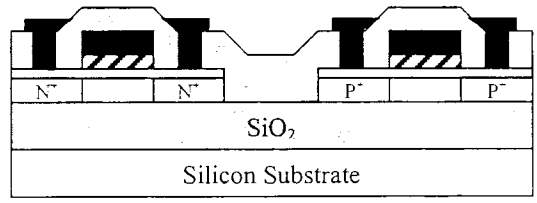

Figure 2.7: SOI CMOS

Because of the complete isolation of devices, latch-up is prevented. Since wells are not needed for device isolation higher circuit densities can be achieved. In addition since the source and drain junctions extend to the buried oxide (BOX) the capacitances associated with those junctions are significantly reduced. Because of this the devices may operate faster while dissipating less static and dynamic power. The junction area of the drain/channel junction is limited. As a result, short channel effects associated with the charge sharing between the gate and the drain are reduced. Similarly the subthreshold slope of SOI devices improves (see figure 2.4) [8,10,17].

2.2.2 Strained Silicon

As mentioned earlier in this chapter, the on state current is inversely proportional to device speed. The mobility of carriers is directly proportional to the saturation current. Hence, any improvement in carrier mobility will result in faster devices. By using a layer of a $Si_{1-x}Ge_x$ alloy, the lattice of active region silicon is stretched by about one percent. The SiGe layer is grown thick enough to relax. The silicon lattice on top of this layer then adopts the lattice constant of SiGe, so long as the silicon layer is below a critical thickness. This increase in lattice spacing reduces scattering, resulting in a 3X increase in mobility. A strained silicon MOSFET is illustrated in figure 2.8.

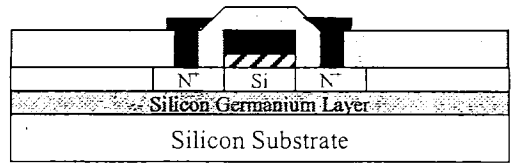

Figure 2.8: Illustration of a Strained Silicon MOSFET

Figure 2.9 illustrates carrier mobility improvements due to different mole fractions of germanium.

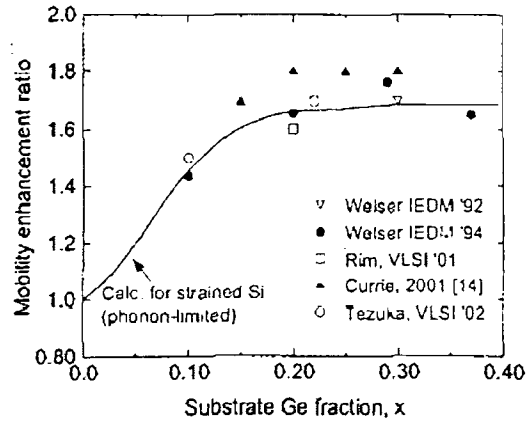

Figure 2.9: Mobility Enhancement for Strained Silicon MOSFETs (adapted from [21])

Strained silicon and SOI have been incorporated to produce planar transistors on a Silicon Germanium on Insulator (SGOI) platform. That is, planar transistors that feature both strained silicon as well as the benefits of a buried insulator.

2.3 Multiple Gate Ultra-thin Body Sidewall FETs

The benefit of an ultra thin body SOI planar MOSFET is that the subthreshold characteristics are superior to that of bulk planar transistors. However in order to create a fully depleted SOI MOSFET the top silicon thickness must be sufficiently thin to allow depletion with small applied biases (e.g. < 100nm). The Multiple Gate Ultra-thin Body Sidewall FET structure alleviates some of this concern. A Multiple Gate Ultra-thin Body Sidewall FET features a thin fin of silicon over which a gate is placed. The Multiple Gate Ultra-thin Body Sidewall FET can be of a double-gate or a Tri-gate configuration, meaning that the device depletes and inverts from either two or three sides. A cross sections of a Multiple Gate Ultra-thin Body Sidewall FET is depicted in figure 2.10.

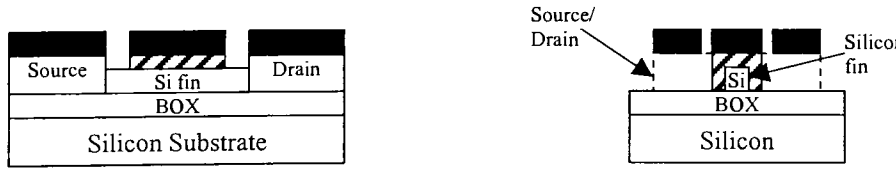

Figure 2.10: Cross Sections of a Multiple Gate Ultra-thin Body Sidewall FET structure

The Multiple Gate Ultra-thin Body Sidewall FET is a proposed replacement for the planar MOSFET, however similar to it's planar counterpart, the channel of the device is still defined by advanced lithography, and is subject to the limitations of lithography

and etch-back techniques. Because of the fully depleting nature of a Multiple Gate Ultra-thin Body Sidewall FET it exhibits excellent electrostatic scaling properties [22].

2.3.1 Double Gate Structures

A double gate structure depletes from two sides of the silicon fin. The transistor width then is double the fin height. When fabricating a double gate Multiple Gate Ultra-thin Body Sidewall FET, a hard mask is used to define the silicon fin. This hard mask may either be silicon dioxide, nitride, or any other insulating etch-resistant material. This hard mask is then left in place during gate oxidation, and subsequent gate material deposition [4,15].

Since the gate resides on either side of the device, during turn-on the channel region depletes from either side of the silicon fin, allowing the existence of a fully depleted device with somewhat relaxed fin width requirements. Because of this the Multiple Gate Ultra-thin Body Sidewall FET has demonstrated some of the best subthreshold parameters of any field effect transistor; such as a subthreshold slope of 68mV/decade for a 40nm channel length device [4].

It should be pointed out that the double gate FET does not necessarily have to take the form of a Multiple Gate Ultra-thin Body Sidewall FET. The double gate transistor may be oriented in three basic directions (figure 2.11)

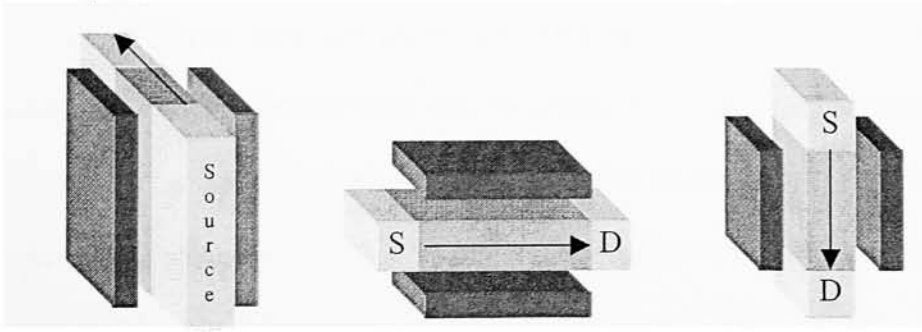

Figure 2.11: Orientations of Double Gate Devices (adapted from [22])

2.3.2 Tri-Gate Structures

Recently Multiple Gate Ultra-thin Body Sidewall FET structures were developed with even more relaxed fin width requirements [4]. The hard-mask used to etch the silicon fin was removed prior to gate oxidation and gate deposition. This created a device that depleted from three sides. While the double gate Multiple Gate Ultra-thin Body Sidewall FET has limited fin width, the tri-gate Multiple Gate Ultra-thin Body Sidewall FET requires dimensionally similar fin height and width to maintain the full depletion.

The tri-gate Multiple Gate Ultra-thin Body Sidewall FET demonstrated by [4] demonstrates some of the best subthreshold parameters compared to planar 65nm transistors. The subthreshold slope matched that of the double gate Multiple Gate Ultra-thin Body Sidewall FET at 68 mV/decade. However the DIBL parameter is very low at 41 mV/V. This speaks very well for this orientation of the Multiple Gate Ultra-thin Body Sidewall FET since as transistors scale smaller it is the off state that seems to be the killer.

2.4 The Vertical MOSFET

Ever since epitaxy was introduced the concept of creating a MOSFET structure featuring current flow perpendicular to the substrate has existed. Due to the methods of epitaxy, dopants can be very well controlled. Doping profiles can be tailored such that charge distributions and electric fields may be controlled. This was demonstrated by [1], using epitaxy to grade the channel doping in a vertical MOSFET. The DIBL parameter for the device demonstrated in [1] is 30 mV/V. The subthreshold slope of these devices is also respectable at 75 mV/decade.

Planar SOI MOSFETs benefit from the increased isolation associated with the surrounding insulator. Vertical MOSFETs are almost always mesa isolated, which is similar to the SOI concept. In mesa isolation islands of device material are etched, the channel of these vertical MOSFETs is then on the sidewall of the silicon pillar or mesa. The inner layer dielectric separating the front-end from the backend then isolates device from device. In bulk silicon, only the source/drain at the bottom of the vertical MOSFET then would be common across an integrated circuit. If these devices were fabricated on SOI substrates the devices would be completely isolated.

There are multiple types of vertical MOSFETs.

2.4.1 Sidewall Vertical MOSFETs

Epitaxial silicon may be grown on top of implanted islands, or the epitaxial layers may be doped in-situ. Sidewall vertical MOSFETs are mesa defined before gate oxidation. A contact to the bottom source/drain is then deposited on one side of the device, while the gate is deposited and defined on the other side [9]. Only one side of the device, then, is used as the transistor. The integration of this type of transistor is far more straightforward then that of fully surrounding gate transistors.

2.4.2 Surrounding Gate Transistors

If the channel region of the epitaxially grown silicon mesa is completely surrounded by the gate, the vertical MOSFET is considered an SGT or surrounded gate transistor [1,5,7]. The surrounding nature of the gate, coupled with a very thin silicon pillar can produce fully depleting devices. Since the entire perimeter of the channel is

associated with a gate, the surrounding gate transistor exhibits the best electrostatic scaling properties [22].

Subsequently since the gate completely envelopes the channel region, the device is quite resilient in the presence of radiation [24]. This is because the gate acts to shield the channel of the device similar to a coaxial cable. Figure 2.12 illustrates a fully surrounding gate vertical MOSFET.

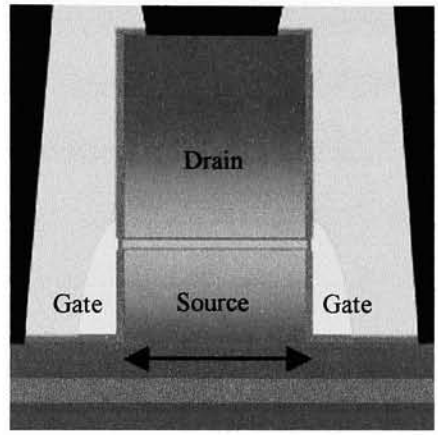

Figure 2.12: Surrounding Gate Transistor

The device proposed in this thesis is of the form of a vertical surrounding gate transistor. Using Molecular Beam Epitaxy (MBE) dopant distributions are controlled in the channel region such that two delta-doping planes exist. That is, two extremely thin regions of highly doped silicon of the same type as the channel region. The use of δ-doping aids in controlling charge balance between the source/drain and the channel, confining the depletion regions to the delta-doping plane as well as within the source/drain. Without the depletion regions extending into the channel region, short channel effects should be minimized, if not eliminated.

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Chapter 3

DEVICE DESIGN

Modern day MOSFETs are complex structures. Extensions have been added to the source and drain in order to control hot carrier effects, as well as to decrease the depletion layer within the channel region [1-3]. The channel itself contains multiple implants required to reduce the probability of snap-back, punch-through, and to control the threshold voltage [4,5]. Much work is being conducted in the research settings to replace the traditional SiO_2 gate insulator with a material with a high-k dielectric. Additionally, a metal gate will be replacing the traditional polysilicon gate due to high series resistances. Devices are being built on increasingly advanced substrates including SOI, strained silicon, as well as the combined Strained Silicon on Insulator (SGOI) [6-8].

The primary design goal of the epitaxial layer structures proposed is to create the vertical analog to a "conventional" planar MOSFET incorporating the aforementioned advancements. Fig. 3.1 presents a schematic representation of the features of the basic VMOS structure as well as a conventional MOSFET for side-by-side comparison of the doping profiles. The structure presented incorporates the epitaxially grown version of features such as highly doped shallow source/drain contacts, lightly doped source-drain

extensions, anti-punchthrough (HALO) implants, and highly doped shallow source-drain contact regions. In the sections that follow, the proposed methodologies for realizing these structural features are discussed.

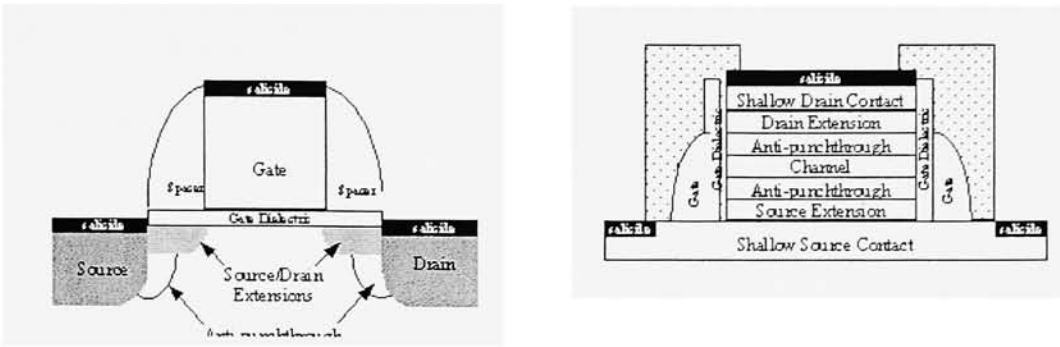

Figure 3.1: Schematic comparison of a planar MOSFET and the proposed VMOS structure.

3.1 Shallow Source / Drain Contact Regions

As planar MOSFETs are scaled from generation to generation, the series resistance of the source and drain regions has increased from technology node to technology node. Under constant field scaling theory, as the channel length is reduced by a factor κ, the junction depth (x_j) in the source and drain region is reduced by the same factor. However, this results in an increased series resistance. In order to overcome this, conventional MOS technology has investigated low energy, high dose implants to achieve a sheet resistance of ~600 Ω/□ and specific contact resistivity of $1x10^{-7}$ Ω/cm^{-3} [9]. The drain contact region in the proposed device is oriented parallel to the current flow vector. This, as well as the shape of the device, leads to reduced contract resistance. Resistance is proportional to contact length and width by equation 1.

$$R = \frac{\rho \cdot L}{W \cdot H} \tag{1}$$

Since the width of the device is parallel to the substrate surface, and the length is perpendicular, the L/W factor is small reducing the overall resistance of the contact region.

The source contact region is extremely highly doped, on the order of 10^{20} cm^{-3} reducing the resistivity (ρ) and therefore the contact region's resistance.

3.2 Source / Drain Extension

Lightly doped drain (LDD) structures have been developed in order to extend the usable lifetime of otherwise conventional CMOS. By optimizing the doping and length of LDD structures, the lateral electric field in the channel region of a MOSFET can be reduced [1]. This reduction in lateral electric field results in a minimization of the short channel effects caused by hot carriers. The reduced electric field also contributes to an increase in breakdown voltage for the MOSFET [2]. These benefits of using LDD structures have been demonstrated and show an increase in device lifetime in excess of an order of magnitude for some device parameters [3]. Device drive current is somewhat sacrificed for the aforementioned parameters, however it is a small price to pay for increased scalability, reduced probabilities of breakdown, and increased device lifetimes.

The vertical MOSFET structure proposed features extensions from the source and drain, extending to the channel region in which to control the charge distribution near the channel, as well as increase series resistance to reduce hot carrier effects.

3.3 Anti-Punchthrough Delta-Doping

Virtually all planar MOSFETs incorporate a localized, high dose implant sandwiched between the source/drain regions and the channel which is typically referred

to as a HALO or pocket implant [10]. The analog to this technology in a vertical device is delta-doping. The formal definition of delta-doping is highly doped region of dopants localized to one atomic monolayer. Delta-doping has been extensively characterized in Si since the early 1990s [11]. The primary use of Si delta-doping was the creation of a channel region for high electron mobility transistors (HEMTs) [12], but also was widely employed in Si quantum electronics in the late 1990s [13].

Since the delta-doped plane of the vertical MOSFET is extremely highly doped, (e.g. $\sim 1 \times 10^{14}$ cm^{-2}) the p^+ delta-doping plane may be used to balance charge of the n^- extension region on either side of the channel, confining the depletion regions associated with the source/channel and drain/channel junctions to the source and drain respectively. Since the depletion region associated with either junction terminates at the delta-doping plane, the delta-doping acts as a field screening layer similar to the HALO or pocket implant.

A recent paper published in the 2002 IEDM Technical Digest notes that MOSFETs using pocket implants may be modeled as three transistors [14]. Parasitic transistors with high threshold voltages corresponding to each pocket implant, and one for the channel region. The structure proposed above will have these parasitic transistors. However since these regions will be on the order of nanometers, transport across these regions will be dominated by tunneling, which is not governed by charge storage delays.

3.4 Channel Doping

A major design constraint for the channel region is that the channel is nearly intrinsic to reduce the ϕ_f component of the threshold voltage. However, a slight gradient may be introduced to the channel doping level to accelerate carriers from the source to

the drain [15]. The use of in-situ doping during the epitaxy process allows for control of the doping in each plane of the devices channel. The doping profile then in the channel region from source to drain may be tailored to aid majority carrier transport.

As can be seen by figure 3.2, mobility decreases with increasing doping.

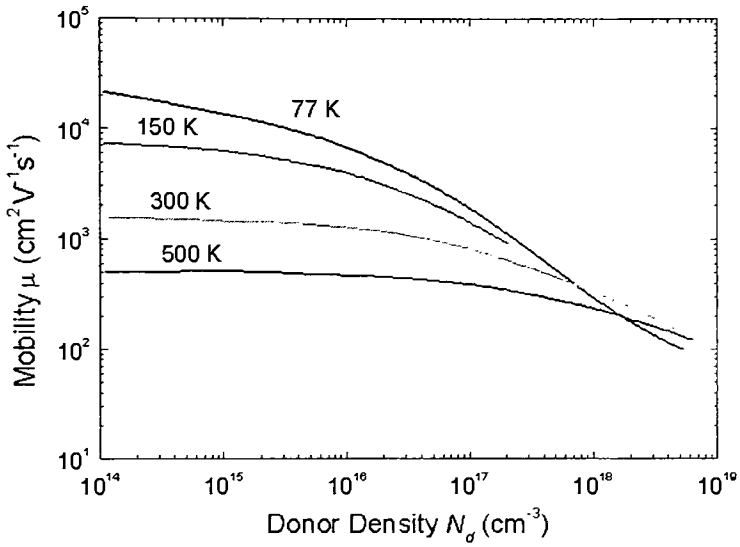

Figure 3.2: Mobility vs. Doping

Constant field scaling dictates that as devices are scaled by a parameter κ the doping associated with the devices increases by 1/ κ. This means that as devices are scaled further and further, the doping associated with the channel increases. This in turn reduces the mobility within the channel. Figure 3.2 illustrates bulk mobility, channel mobility is significantly less than in the bulk due to surface interactions and field effects, however mobility is still proportional to doping density. Since the delta-doping planes in the vertical MOSFET structure act as field screens, the doping within the channel of the device need not be high.

3.5 $Si_{1-x}Ge_x$

The proposed vertical device structure incorporates $Si_{1-x}Ge_x$ localized to the source/drain edges of the channel region. The reason for this is to prevent the outdiffusion of delta-doping into the channel with subsequent thermal steps. The major challenge with the use of delta-doping involves careful management of the thermal budget to suppress diffusion. Because of the extreme doping level in a delta-doping plane, diffusion is enhanced at lower temperatures. For example, Gossman states that a B delta-doping plane will typically double its full width at half maximum (FWHM) after 30 min. of diffusion at 740oC [11]. However, this outdiffusion may be suppressed for Boron by surrounding the delta-doping plane with In or Ge which inhibits diffusion of p-type dopants [16]. Therefore, in the n-VMOS structures, a thin layers of SiGe will be strap the Boron delta-doping plane to act as a diffusion barrier.

The channel region may alternately be comprised entirely of $Si_{1-x}Ge_x$. The purpose of this is twofold. First, the oxidation rate of SiGe alloys varies from that of pure silicon. This allows for selective oxidation to occur, therefore allowing the oxidation rate to be tailored to the device requirements [17]. Second, SiGe has a larger lattice spacing then crystalline silicon. The increased lattice spacing leads to an increase in mobility of both electrons and holes.

3.6 Metal Gate and Advanced Gate Insulators

Deep sub-micron devices feature gate widths in the nanometer range. Such thin gates leads to large resistances. The addition of silicides has been used to combat the problem of this as well as contact resistances. However, gates are getting so thin, that even the low sheet resistances of silicides are too high. It has been identified that metal

gates should be used in order to reduce the resistances associated with the gate electrode [9,18].

Figure 3.3 shows the ITRS prediction for gate dielectrics in future planar devices.

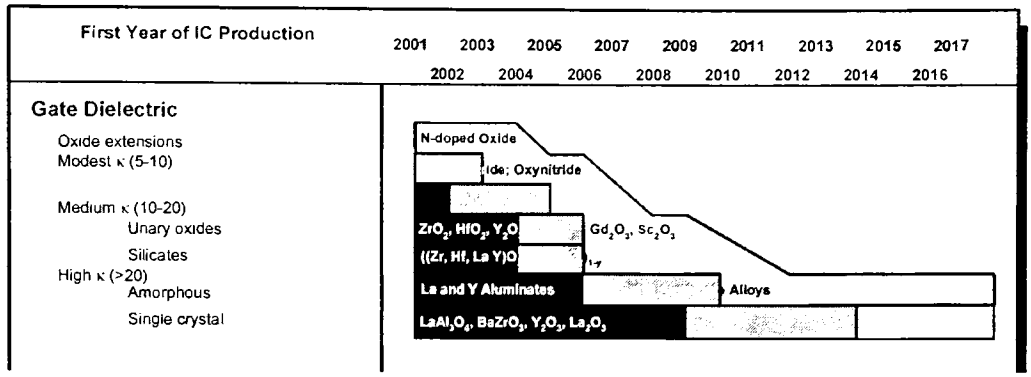

Figure 3.3: Gate Dielectric Roadmap 2001 [9]

The dielectrics listed in the above figure may be used in addition to SiO_2 or in place of it. As the incorporation of the proposed vertical MOSFET device will not occur in the near future, it follows that purely deposited high-k gate dielectrics will be used. The use of deposited gate dielectrics aids the construction of the proposed device, as deposited films are often processed at lower temperatures than those that are grown.

3.7 Minimization of the Miller Overlap Capacitance via Selective Oxidation

A parasitic capacitance known as the Miller capacitance results when the gate overlaps the source and drain [19]. Virtually all conventional modern CMOS devices employ a self-aligned ion implantation using the gate and sidewall spacers as an implant mask. In these structures, the overlap results due to the tendency for ions to travel underneath the gate. This capacitance will clearly be a challenge for the vertical devices proposed.

It is hypothesized that the key element for isolating the source and drain regions from the gate, lies in the different heats of formation of semiconductor oxides. For instance, SiO_2 (-204 kcal/mol) has nearly double the heat of formation of GeO_2 (-119 kcal/mol) [20-26]. Thus, the channel of a transistor comprised of a SiGe layer could conceivably have a thinner oxide layer grown than the source and drain regions. This would enable the engineering of the Miller overlap capacitance.

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Chapter 4

DEVICE SIMULATION

Since prototyping a process and / or a device in silicon is costly, and open to process variations it is often a good idea to use a numerical simulation tool to predict trends. One such simulation tool is Silvaco's Atlas and Athena software packages. The vertical MOSFET device proposed operates using the principles of quantum effects such as tunneling. It is important then, in modeling, to assure that quantum effects are taken into account.

4.1 Introduction to Silvaco

Silvaco's Quantum module to its Atlas device simulator can be used to simulate the effects of quantum confinement of carriers in semiconductor devices [1]. The simulator is set up to handle MOS devices, as well as light emitting devices. To model these effects the Quantum module uses both a Poisson's equation solver (Eqn. 1) in addition to an Schrodinger's equation solver (Eqn. 2). The Poisson's solver is completed in two dimensions while the Schrodinger's solver is completed in one-dimensional slices

across a device. The combinations of these solvers provide calculations of bound state energies, wave functions, and carrier concentrations in the presence of quantum mechanical confining potential variations.

$$\frac{\partial^2}{\partial x^2}V(x,y)+\frac{\partial^2}{\partial y^2}V(x,y)=\rho(x,y) \tag{1}$$

$$H\psi=-ih_{bar}\frac{\partial\psi}{\partial t}=\frac{-h_{bar}{}^2}{2m}\nabla^2\psi+V(0,x)\psi \tag{2}$$

Where ρ is the charge in the semiconductor, H is the hamiltonian, ψ is the wavefunction, and V is the potential of the system. In one dimension Schrodinger's equation is reduced from ∇ to d/dx.

Quantum confinement is modeled in a semi-empirical manner using Van Dort [2] and Hansch models [3]. The Van Dort model accounts for the splitting of the eigenvalues near the surface by an increase in ΔE_g of the bandgap at the surface. To do so it qualitatively reproduces the energy band quantization effects and neglects the wave function repulsion effects. The change in energy gap at the surface is modeled by equation 3.

$$\Delta E_g=\frac{13}{9}\cdot\beta\cdot\left(\frac{\varepsilon}{4qkT}\right)^{1/3}\left|E_{surf}\right|^{2/3} \tag{3}$$

Where the E_{surf} parameter is the magnitude of the electric field at the silicon – insulator interface. The Hansch model represents quantum confinement by reducing the effective density of states near the silicon surface. The Hansch model (eqn. 4) can easily be included into carrier transport equations, making it ideal for numerical modeling.

$$N_c(z) = N_c \cdot \left(1 - e^{\frac{-(z+z_o)^2}{\lambda_{TH}^2}} \right) \tag{4}$$

where $$\lambda_{TH} = \frac{\sqrt{2mkT}}{h_{bar}}$$

In order to simulate multiple quantum wells, often found in laser diodes, as well as the proposed vertical MOSFET device the Quantum module uses two advanced models. These are the Li model and the Yan model. Both models can be used to calculate optical gain as well as spontaneous recombination. However the Li model takes into account both light and heavy hole valence bands, while the Yan model only takes into account one valence band.

4.2 Model Parameters

In order to enable the one-dimensional Schrodinger's equation solver for electrons the 'schro' parameter is used in the model statement. With this set, Atlas will solve the one-dimensional Schrodinger's equation along a series of slices in the y direction relative to the device. For a PMOS device, or devices in which holes are the dominant carriers the 'p.schro' parameter is used instead. When either of these parameters is turned on, one solution to Schrodinger's Equation is taken, the carrier concentrations are then calculated.

The potential at each particular node is then derived from Poisson's equation, and substituted back into the Schrodinger equation. This alternating process is repeated until a solution converges. Eigen energies and functions can be written by specifying the 'eigens' parameter from the output statement.

Quantum moments are required for the simulation of HEMT channel confinements, as well as thin oxides, and small geometry MESFETs and Heterojunction diodes. These effects can be modeled in Atlas using the quantum moments model, which is based on the moments of the Wigner Function Equations-of-Motion. This model is used to correct the quantum temperature within the quantum potential used in Schrodinger's equation. For electrons using the 'quantum' statement in the 'models' statement can activate this. For holes, substitute 'p.quantum' as the switch in the 'models' statement. The distributions of carriers given by these models can vary greatly from distributions predicted by standard drift and diffusion equations. The standard 'init' command is usually not suitable for obtaining solutions in the case of quantum moments. A damping factor is available as a correction to this. By solving the 'qfactor' parameter the problems involved in initial guesses may be overcome. A 'qfactor' of zero implies the quantum moments model is turned off, while a 'qfactor' of one implies this solution is turned on.

As discussed before the Van Dort and Hansch models may also be used to account for the bandgap widening near the silicon surface. To turn on the Hansch model the 'lambda' switch is used in the 'models' statement. Using the 'n.dort' switch or 'p.dort' switch in the 'models' statement for electrons and holes respectively may turn on the Van Dort Model. The 'mqw' statement can turn on the multiple quantum well

solutions previously discussed. The parameter 'delta' is user definable spin-orbital splitting energy. The default value for this splitting energy is 0.341 eV.

4.3 Simulation of Advanced Devices

A vertical n-channel MOSFET was simulated without using Silvaco's quantum package. After introducing the quantum models and equations, the characteristics of the nMOSFET were not significantly altered. However the addition of the quantum modules allow for added cross-sectional extractions such as the valence band and conduction band profiles, total electric fields, etc. The electric fields given are illustrated in figure 4.1.

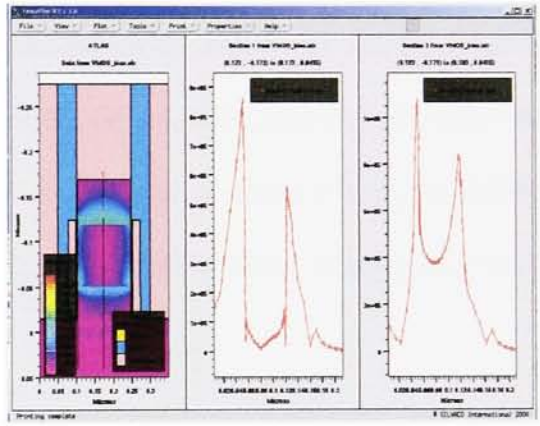

Figure 4.1: Electric Field, including cross sections at the surface and in the bulk.

In addition the vertical MOSFET showed proof of the devices concept, illustrating that the threshold voltage of the device is dependant upon the channel doping and not the delta-doped regions, which act as tunnel barriers as can be seen in figure 4.2.

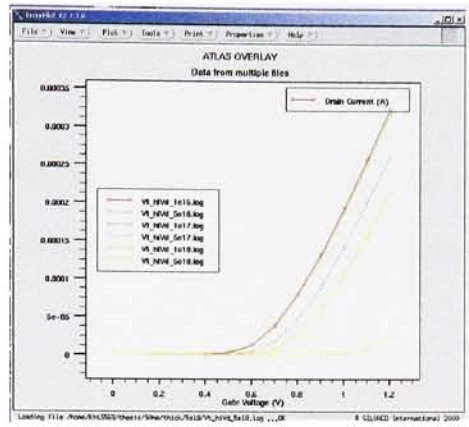

Figure 4.2: Ids / Vgs characteristics with different channel dopings.

It is fortunate that Resonant Interband Tunnel Diodes (RITD's) were fabricated successfully at the University of Delaware and at RIT [4,5]. Using the true data captured from these devices, a simulation to match the device structures was set up. After adjusting doping levels of the device, I-V characteristics were obtained. The simulations show a backwards diode. A RITD has a region of negative differential resistance, while a backwards diode does not. The simulations of an optimized RITD are illustrated in figure 4.3.

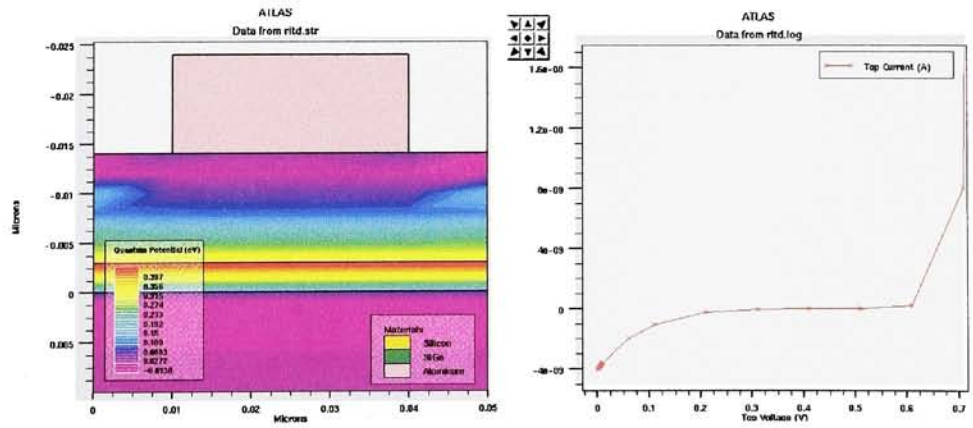

Figure 4.3: RITD structure and I-V Characteristics

Simulations of a p-channel vertical MOSFET device did not successfully illustrate the tunneling operation of the proposed vertical MOSFET device. Threshold voltage simulations do not vary with channel doping, instead the threshold voltage seems to change by varying the delta-doping concentration, suggesting that tunneling is not occurring.

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Chapter 5

DEVICE FABRICATION

A standard CMOS front end process contains on the order of eight mask layers; Isolation, N-well, P-well, Gate, N-active, P-active, Contact, and Metal 1. There are many implants, and associated, multiple anneals. In order for a new device technology to be feasible it must offer many things. The new technology must offer technological benefits over the conventional device. In fact, Semiconductor Research Corporation (SRC) program managers often seek a 100X performance gain in the new technology over conventional technologies. The device must be able to be integrated on a large scale. Finally the fabrication must not be significantly more difficult as well as costly. Chapter 3 explained the technological benefits of the proposed Vertical MOSFET. This chapter will attempt to defend the simplicity of integration of devices as well as ease of fabrication. Process details will be discussed and characterization experiments will be presented.

5.1 VMOSFET Fabrication Process

The process flow for the proposed Vertical MOSFETs is summarized in Table 5.1. Antimony doped (100) substrates were used at a starting resistivity of 0.025 to 0.05 ohm-cm. These wafers were chosen due to availability as well as to reduce series resistances in the finished device.

Process Step #	Process	Tool
1	Epitaxial Layer Growth	Performed at NRL
2	SiO_2 hard mask deposition	AME P-5000 PECVD
3	Device pillar definition	SVG-88 Coat / Develop Track GCA 6700 G-Line Stepper
4	Pillar Etch	Drytek Quad 482 RIE
5	Resist Removal	PRS-1000
6	RCA Clean	Megasonics RCA Wet Bench
7	Gate Oxidation	AME P-5000 PECVD
8	Oxide Densification	Bruce Horizontal Furnace
9	Gate Deposition	CHA Evaporator
10	Gate Top Define	SVG-88 Coat / Develop Track GCA 6700 G-Line Stepper
11	Gate Top Etch	Hot Phosphoric
12	Resist Removal	PRS-1000
13	MESA-2 Define	SVG-88 Coat / Develop Track GCA 6700 G-Line Stepper
14	Gate Bottom Etch	Hot Phosphoric
15	MESA-2 Etch	Buffered HF LAM-490 Autoetch
16	Resist Removal	PRS-1000
17	ILD0 Deposition	AME P-5000 PECVD
18	Contact Define	SVG-88 Coat / Develop Track GCA 6700 G-Line Stepper
19	Contact Etch	Buffered HF
20	Resist Removal	PRS-1000
21	Metal Deposition	CVC-601 Sputterer
22	Metal 1 Definition	SVG-88 Coat / Develop Track GCA 6700 G-Line Stepper
23	Metal 1 Etch	Hot Phosphoric
24	Resist Removal	PRS-1000

Table 5.1: VMOSFET Fabrication Process

5.2 Process Technology Development

5.2.1 Sidewall Oxidation

Since the gate of the proposed Vertical MOSFET resides on the sides of an etched profile it is important to determine the characteristics of an oxide on an etched profile. It is assumed that the etched profile will introduce an increased level of charges within the oxide as well as at the oxide-semiconductor interface. An experiment was completed to analyze the effects of growing an oxide on an etched profile.

A highly doped substrate was chosen due to low series resistance, which was required for the VMOS devices. Unfortunately this limited the C-V measurement capabilities, as quasistatic measurements cannot be obtained if carriers cannot fully recombine.

Positive G-line photoresist (Arch 812) was spun-on using a SVG 88 track coating system. The process consists of a dehydration bake with gas phase introduction of HMDS. The resist is then spun on to a target thickness is 11,600Å. The resist is then soft baked for reflow.

The first level lithography defines the active area of VMOS devices as well as the "pillar" region of the test structure capacitors. The sidewall height and perimeter were eventually used to calculate electrical oxide thicknesses of the etch-profile oxide. The lithography was carried out on a GCA G-line stepper using a clear field quartz mask. Due to the large size of the devices the wafers were intentionally over-exposed to assure total thickness development.

Again the wafers were placed in the develop track of the SVG 88 track coat system. The resist is developed using a spin-puddle technique prior to hard bake.

The pillar must then be etched. As this study intends to recreate the processes associated with VMOS and finFET devices, a RIE etch is required for adequate sidewall angle using SF_6 and CHF_3 [1]. The Drytek 482 quad-chamber RIE system was used. Chamber 2 is used for silicon etching using a combination of SF_6 and CHF_3. This particular chemistry was used in order to obtain an anisotropic profile. The CHF_3 is used in order to create a sidewall polymer to aid in anisotropy. The conditions of the etch were as follows: 30 sccm of SF_6 and 30 sccm of CHF_3 at 185 Watts. Due to this a substantial post-etch clean is required to remove the polymer. The crystalline silicon was etched to a depth of 2.25μm in order to produce a significant increase in capacitor area for electrical parameter extraction.

Following the etch a modified RCA clean is performed to clean the wafers surface, remove the sidewall polymer, and to create a hydrophobic surface for proper gate oxidation. A 50:1 HF solution was used last in order to remove any oxide grown by the hydrogen peroxide in the APM and HPM baths in order to assure a hydrophobic surface.

Immediately following the RCA clean, the gate oxide was grown using a Bruce horizontal furnace. The tube used was specified solely for dry oxidation, and a Trans-LC clean was performed within one week of the oxide growth. The standard 200Å "SMFL" recipe was used. The wafers were introduced into the furnace at 700°C, and ramped to the process temperature of 900°C. A diffuser was placed on the source side of the quartz wafer boat to aid gas flow uniformity.

As to prevent environmental defects from entering the oxide, the wafers were immediately placed in the ASM 6" LPCVD tool. Polysilicon was used as the top contact in order to eliminate the chance of spiking associated with metal top contacts. 3000Å of

polysilicon were deposited using SiH_4 at a base pressure of roughly 180mTorr. Again a standard "SMFL" recipe was used with a modified deposition time. The deposition thickness was chosen to run in parallel with similar devices.

Following polysilicon deposition a phosphorous spin-on glass was used to dope the top gate. Phosphorous was chosen as the dopant due to availability and to eliminate the possibility of dopant segregation into the oxide. The phosphorous was spun-on using a manual hand spinner, calibrated with a strobe light at 4500rpm. The dopant was then driven in using the Bruce horizontal furnace n-type tube at 1000°C for 30 minutes.

A buffered oxide etch was then performed to remove the spin on glass. BOE etches thermal SiO_2 at a rate of roughly 1000Å per minute while deposited glass etches faster. The spin-on glass was etched for 12 minutes to assure removal.

A top metal contact of aluminum was then deposited by sputtering. The CVC-601 upward sputter tool was used after a 3-hour pump down. The cold-cathode type pressure gauge was unable to detect the base pressure of the chamber prior to deposition, but the pressure was estimated to be $5\text{-}8x10^{-6}$ Torr. A 5 minute 1250W presputter was performed to remove any surface oxide and contamination from an 8 inch Al / 1% Si target. Aluminum was then deposited at 1250W for 15 minutes to a target thickness of 2000Å.

The SVG 88 track coating system was again for resist deposition and development. The second level lithography defines the capacitor top gate and subsequently the area of the capacitors in addition to the contact material for the vertical MOSFET devices. Again the GCA G-line stepper tool was used to expose the wafers.

Hot phosphoric acid at 50°C was used to etch the aluminum. The 2000Å was removed in approximately 2 minutes. A five minute deionized water rinse was performed prior to spin-rinse-drying.

Using the resist and aluminum as a mask, the polysilicon top electrode was then etched using the LAM 490 Autoetch tool. The LAM 490 is an isotropic plasma etching system. The etch was performed in SF_6 at a process pressure of 260mTorr. The etch was completed with endpoint detection with a 40% overetch. The overetch completes the polysilicon etch in addition to creating mesa-type isolation to reduce the overlap fringe capacitance of the test structures.

The resist was then removed in PRS-1000 resist strip at 90°C for 12 minutes. PRS-1000 is a chemical resist strip-removing approximately 1000Å of organic resist per minute.

Following C-V testing one wafer was sintered at 425°C for 20 minutes in the Bruce horizontal furnace using forming gas (5% H_2 in N_2).

The devices were tested using extensive C-V and I-V analysis. Due to the substrate doping level, only high frequency analysis could be performed. The C-V measurements were taken in accordance with the ASTM F1153-92 standard [2]. As with any C-V measurement extensive calibration and zeroing of the metrology system is required.

In order to determine the charge density, often the flatband capacitance and voltage are often required. In order to obtain this, high frequency C-V analysis was performed on all samples. The reciprocal of the square of the normalized capacitance was plotted versus the input voltage. The location knee of this curve occurs at the

flatband voltage. Extracting back on a C-V plot the flatband capacitance can be determined [3] see figure 5.1.

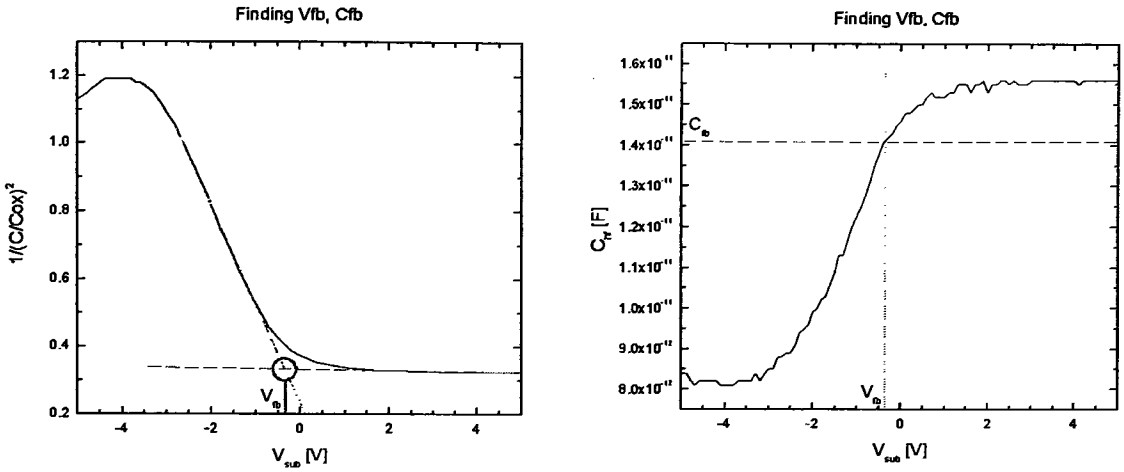


Figure 5.1 Flatband extraction

Fixed charge is generally positive stemming from structural damages such as ionized silicon within 2nm of the oxide-semiconductor interface. In order to extract the fixed charge all other sources of flatband shift must be eliminated or reduced. Because of this, a sinter must be peformed prior to extraction. The fixed charge can then be characterized by equation 1.

$$Q_f = \left(\phi_{ms} - V_{fb}\right) C_{ox} \tag{1}$$

The metal semiconductor workfunction must be known in order to extract data by this method. Using degenerately doped polysilicon as the top gate the metal-semiconductor workfunction can be determined by:

$$\phi_{ms} = \phi_f - 0.56V \tag{2}$$

Oxide trapped charge can be determined by using either the etch-off method or the photo I-V method. However oxide trapped charges are generally only a concern in devices subjected to radiation and electrical stresses.

Mobile charge is extracted using a temperature-bias test. The room temperature – post processing high frequency C-V curves are first obtained. The sample is then heated to 200°C for 15 minutes with a bias of 5V applied. The standard measurement technique requires an applied field of >1MV/cm. The sample is then cooled to room temperature with the bias continuously applied. A repeat of the C-V measurement is done and the shift is noted. The mobile charge can be determined by equation 3.

$$Q_{ot} = -\Delta V_{fb} C_{ox} \tag{3}$$

Interface charge is often characterized by a change in minimum capacitance between low and high frequency C-V measurements. Due to the substrate doping of these capacitors, a high frequency method must be used. The Terman method is a suitable room temperature, high frequency test. A non-parallel shift in the C-V curve results from the presence of interface trapped charge. This charge can be extracted by the following equation. Unfortunately the Terman method of extraction is limited to interface charge energies away from the band edges. Many interface-trapped charges however reside at an energy state near the band edge.

$$Q_{it} = \frac{C_{ox}}{q} \frac{d(\Delta V_G)}{d\phi_s} \tag{4}$$

I-V analysis is useful in determining the critical field strength of an insulator. To extract the field strength the device under test is placed in series with a large resistance. The potential across the circuit is then ramped to a voltage significant enough to break

through the oxide. Plotting current versus voltage a spike in current will be observed (see figure 5.2) at the point where this occurs. A second voltage sweep can be added to the plot. The difference in voltage between the breaking point and a comparable current on the appended plot is the critical potential drop across the oxide. This divided by the oxide thickness gives the field strength of the dielectric.

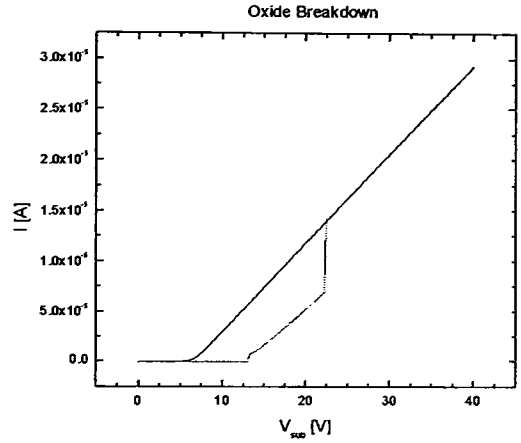


Figure 5.2: Critical field extraction

While electrical oxide thickness can be derived from the accumulation capacitance measured by C-V techniques, it is often beneficial to directly observe the device under test. In order to view the dimensions of the devices in this study a cross sectional scanning electron microscope is required.

The wafers were cleaved along the <100> direction through the vertical capacitor devices. Cross sectional SEM images were acquired. Energy Dispersive X-Ray (EDX) analysis was then used to determine bulk as well as film compositions (see figure 5.3).

Figure 5.3: Cross Sectional SEM and EDX analysis

A formula was derived for extraction of electrical oxide thickness. The resulting thicknesses for multiple vertical shapes are summarized in table 5.2. The values given is the extracted oxide thickness of the vertical-only regions of the devices.

$$t_{ox} = \frac{k_{SiO_2}\varepsilon_o A'}{C_{VMOS-C} - C_{MOS-C}} \tag{5}$$

Shape (perimeter [μm])	Average EOT [Å]
Circle (200)	57.5
Square (200)	51.6
Diamond (226)	35.8
Square (226)	62.0

Table 5.2: Electrical Oxide Thickness of Vertical Oxide

Assuming the square-shaped devices are perfectly parallel and perpendicular to the wafer flat, oxidation kinetics suggest that these shapes should have the lowest oxidation rate while the diamond shape, 45° off from the square shapes should have a higher oxidation rate. This is obviously not the case suggesting either a different crystal orientation for each. Notice the spacer-like profile at the bottom of the pillar in figure 5.3, the orientation of this profile could easily alter the extracted thicknesses.

Since all shapes were processed in parallel, on the same substrates, with only crystal orientation as a factor, the orientation must be the source of the electrical oxide thickness variations.

The mobile charge was extracted to be $5.779x10^{11}cm^{-2}$ which is smaller then reported previously [4]. This is most likely due to the use of a polysilicon top electrode as opposed to an aluminum top electrode used in [4]. The mobile charge was found to be positive suggesting an alkali metal contamination such as Sodium or Lithium. A non-parallel shift was observed during the temperature bias testing suggesting interface trapped charge was present.

The Terman method of extracting interface-trapped charge yields a value of $2.88x10^{12}cm^{-2}$, which while high is not outside of the realm of reason. The interface-trapped charge was found to be positive. As this value is an order of magnitude larger then that of the extracted mobile charge, it follows that metal contamination is not the root cause of interface trapped charge for the vertical capacitors.

Fixed charge was found to be $2.556x10^{-11}cm^{-2}$ suggesting that this charge accounts for the least of the oxide charges. This stands to reason as fixed charge is confined to within 2nm of the silicon-oxide interface, and is generally due to interstitial silicon atoms. However, the sign of the fixed charge is negative. According to [3] fixed charge is always positive, suggesting an error in extraction. This is believable as the error associated with fixed charge extraction derives from error in the metal-semiconductor work function which was calculated based upon the assumption that the polysilicon was degenerately doped, and the substrate was doped at $1x10^{18}cm^{-3}$.

The field strength of all devices is summarized in Table 5.3. The strength of each oxide is just below 4.0MV/cm. A high quality oxide has a field strength of 10 MV/cm suggesting that the etched profile and the charges associated with the oxide weaken the dielectric. While the values reported are low, they may still be suitable for low voltage device operation.

Shape (perimeter)	Square (226μm)	Diamond (226μm)	Square (200μm)	Circle (200μm)
Avg. Field Strength	3.9MV/cm	3.4MV/cm	3.8MV/cm	3.5MV/cm

Table 5.3: Field Strength

5.2.2 Thermal Budget Testing

Due to the proposed device design, including delta-doping, the thermal budget of the fabrication process must be kept low. A SiGe diffusion barrier surrounds each delta-doped plane. This only buys some leeway in terms of diffusion of the profile [5]. Prior work done by P.E. Thompson et al. illustrates devices exhibiting tunneling behavior even after annealing for one minute at 825°C [6]. A follow up study by N. Jin et. al. showed that placing the B in-between SiGe was essential to ensuring optimal device performance [7]. The devices described however do display lower operating currents then those annealed at lower temperatures. It was important then, to determine acceptable limits for the vertical MOSFETs thermal processes.

An epitaxy wafer grown by silicon Molecular Beam Epitaxy (MBE) [8] at the United States Naval Research Labs using the proposed Vertical MOSFET design featuring a 65nm channel length was cleaved into 10 pieces, five of which were set aside for thermal budget testing.. MBE was required to create the doping profiles making this device design conceptually effective [9].

The epitaxial growth performed at the US Naval Research Labs was performed at a base pressure of $4x10^{-8}$ mbar. The epitaxial layers proceeded as follows. First a 20Å buffer layer was grown, followed by silicon doped with phosphorous at a concentration of roughly $8x10^{18}$ cm^{-3}, confirmed by calibration standard samples. The phosphorous-doped layer thickness is 110nm. The phosphorous-doped layer is followed by a delta-doping plane, which contains an extremely thin (~10Å) layer of $Si_{0.6}Ge_{0.4}$ followed by a boron delta of roughly $3.5x10^{19}$ cm^{-3} again followed by the $Si_{0.6}Ge_{0.4}$. A 63nm intrinsic region was grown and terminated again by another delta-doping plane. The growth was concluded by a 100nm thick layer of phosphorous-doped silicon at $8x10^{18}$ cm^{-3} and capped by a contact layer doped with both phosphorous and antimony ($4.5x10^{19}$ cm^{-3} Sb, and $8x10^{18}$ cm^{-3} P).

One of the five samples was not subjected to a high temperature. The four other samples were subjected to 30 minutes at temperatures of 775°C, 800°C, 825°C, and 850°C. These temperatures were chosen based on prior work, which observed the growth of native dry oxide at 775°C. The oxide was measured by ellipsometer to be 60Å. Attempts to grow an oxide at 750°C were unsuccessful, as any oxide, if grown was immeasurable by ellipsometer. Aluminum was sputtered on the front and backside of each sample. The aluminum was subsequently patterned using contact lithography. The front side aluminum was etched using phosphoric acid at 54.7°C. The Drytek Quad 482 Reactive Ion Etching system was used to etch pillars in the epitaxially grown layers, isolating each epitaxial layer from others. The photoresist was then removed.

A bias was swept on the top contact while the backside contact was held as common. The current through the epitaxial layers was monitored. As the doping profiles

diffuse, the current through the device doping profiles will change. Figure 5.4 illustrates the current through each of the devices both before and after sintering of the samples. The current through these samples suggests the potential I_{off} state current through the final VMOS devices. The comparison of sintered (420°C, 20 minutes in H_2N_2) and non-sintered devices is used to eliminate any variation due to non-ohmic contacts.

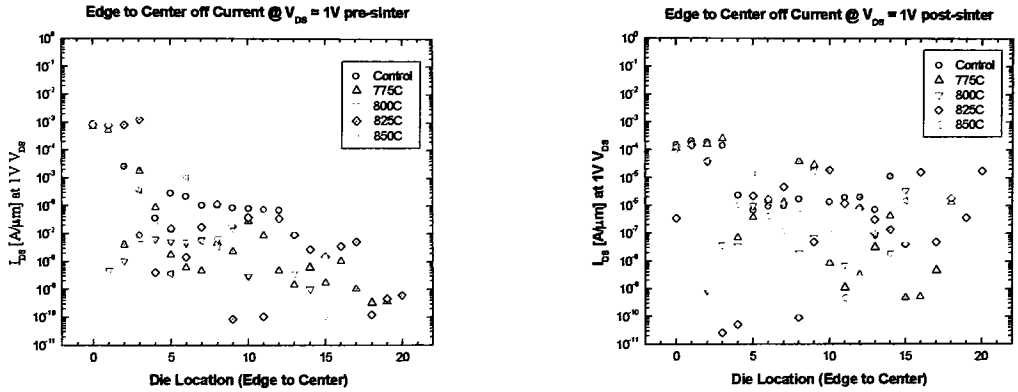
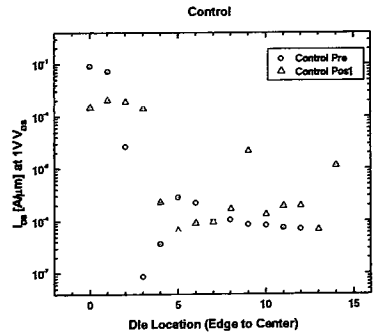


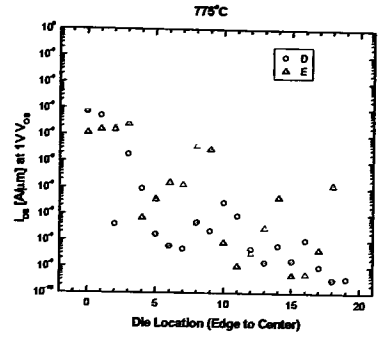
Figure 5.4: Comparison of off state currents

The following table compares each sample before and after sintering.

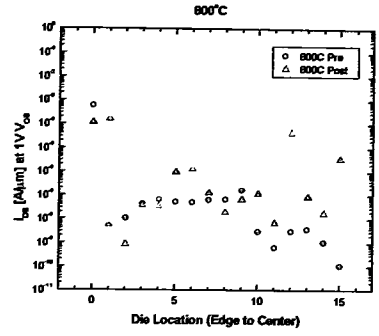
Control



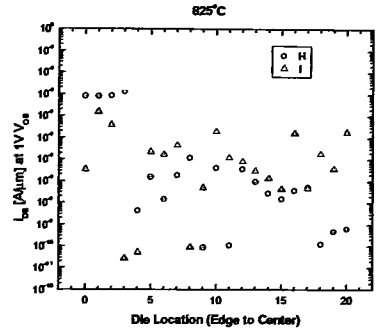
775°C



800°C



825°C



850°C

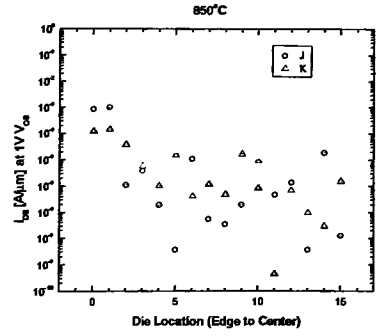


Table 5.4: Comparison of thermal budget tests pre and post sinter

As shown in table 5.4 and figure 5.4, the current through the control samples is comparable to the current through the sample subjected to 850°C. The samples with the lowest, and therefore the most desirable currents are those subjected to 775°C and 800°C.

It can be concluded from these results then, that the current through the epitaxial layers for the devices as grown is high due to a significant number of defect sites in the epitaxial layers. At comparably lower temperatures the doping profiles do not diffuse significantly, however defects due to epitaxy are annealed out. At higher temperatures, the doping profiles diffuse making the channel region more conductive producing higher observable off state currents.

5.2.3 PETEOS Oxide Characterization

Due to thermal budget constraints, the gate oxide would be limited in thickness. Because of this, alternate options were explored. The use of a thermal steam oxide allows for a thicker oxide at the same thermal budget. However at the temperatures determined above, a safety cutoff prevents the flow of hydrogen in the Bruce Horizontal Furnace, making this option impossible. A second option is the deposition of SiO_2 by chemical vapor deposition (CVD), however the qualities of these films are often extremely poor. A recent option is the use of plasma enhanced CVD [10,11]. However, the quality of the PECVD oxide is unknown. It was necessary then to determine the field strength of these films.

The AME P-5000 cluster tool was used to deposit 40nm of PECVD TEOS oxide. Aluminum was then deposited on the wafer, and patterned using a capacitor test mask. The breakdown test used to determine the critical field strength of the sidewall oxide was used. The dielectric strength of the PETEOS was determined to be between 7MV/cm and

8MV/cm. Considering the ideal strength for SiO2, is 10MV/cm this alternative was determined to be acceptable.

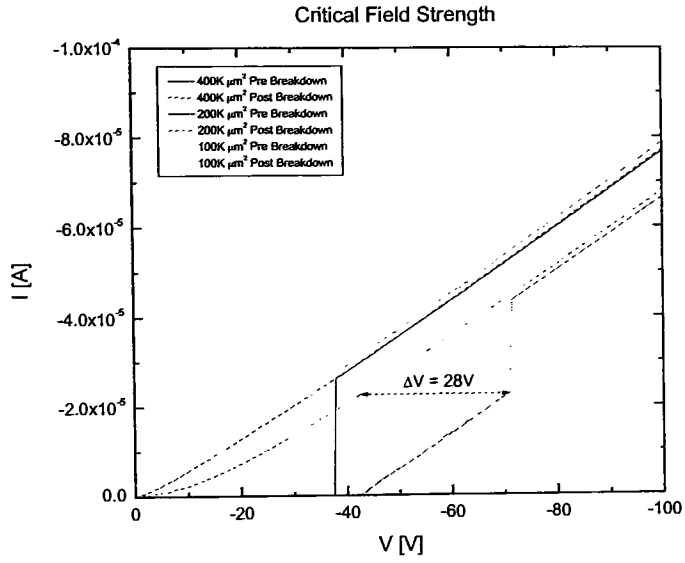


Figure 5.5: Dielectric Field Strength of PECVD Oxide

As can be seen in figure 5.5, the 400,000 μm^2 and the 100,000 μm^2 area capacitors did not show any leakage through the oxide. The 200,000 μm^2 area capacitor does show some conduction. The current through the 200,000 μm^2 capacitor before the point of breakdown may be due to Fowler-Nordheim tunneling.

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Chapter 6
ANALYSIS OF RESULTS

Electrical testing was conducted subsequent to fabrication of the vertical MOSFET devices, as well as subsequent to preparation of processed test samples. First, calibration samples were tested for resistivity to verify the doping densities grown for the vertical devices. Pre-fabrication I_{off} testing was conducted to determine what temperatures were acceptable in device fabrication. The results of that study are summarized in chapter 5. Device testing was conducted on a manual probe station using a Keithley 4200 Semiconductor Parameter Analyzer connected through a switch matrix.

All tests performed were repeated using multiple die and verified on multiple wafers.

6.1 Calibration Sample Testing

Along with the device wafers epitaxially grown calibration samples from the US Naval Research labs were obtained. Resistivity testing was conducted using a CDE ResMap four point probe resistivity measurement tool. Each 3" wafer was probed in 169 locations to determine sheet resistance as well as doping concentration. The calibration

samples illustrate the performance of the MBE tool to deposit: Sb at 350°C and 400°C, B at 1800°C and 1870°C, GaP at 700°C and 750°C. Table 6.1 illustrates the sheet resistance measurements for the different calibration samples.

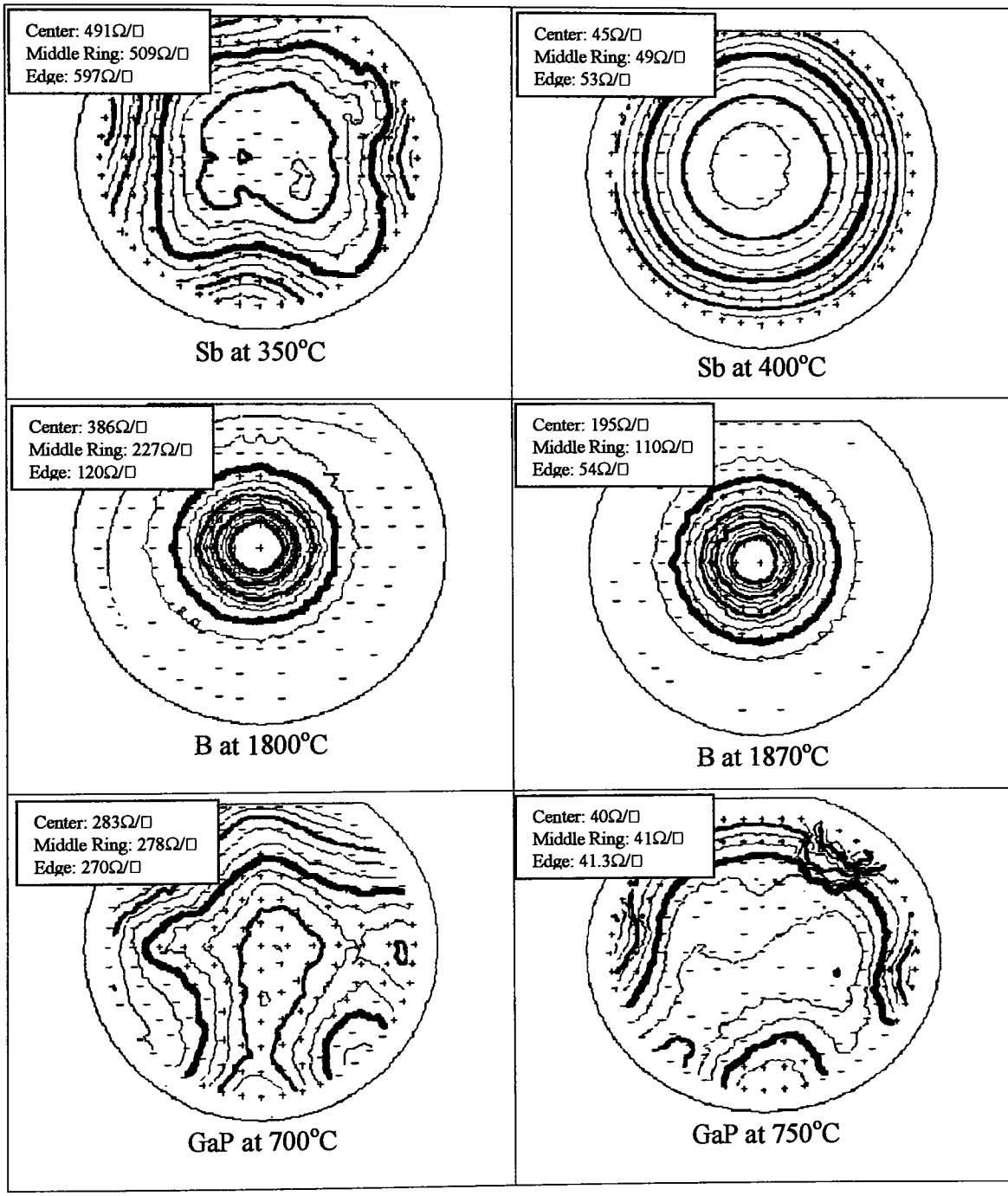


Table 6.1: Calibration Sample Sheet Resistance Measurements

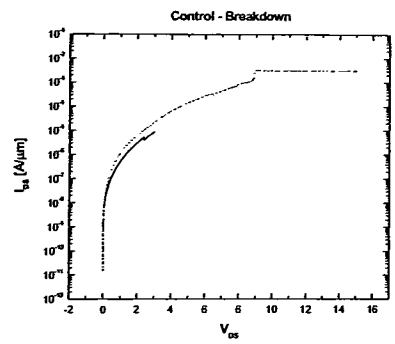
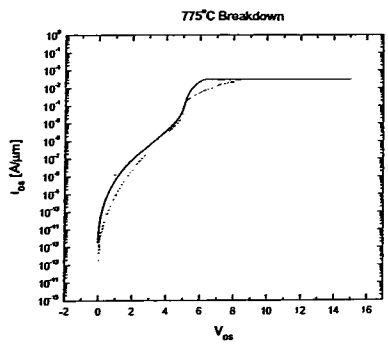
As can be seen in table 6.1, Sb and B show strong radial variations while GaP is somewhat less radial. The average sheet resistance for Sb at 350°C is 509.7 Ω/□ while the 400°C average is 49.5 Ω/□. The standard deviation for the 350°C Sb is 14 Ω/□ while the 400°C samples standard deviation is 2.8 Ω/□. These average values correspond to roughly $2x10^{18}$ cm^{-3} and $7x10^{18}$ cm^{-3} for the 350°C and 400°C samples respectively. The average sheet resistance for B at 1800°C is 147.1 Ω/□ while the 1870°C average is 68.5 Ω/□. The standard deviation for the 1800°C B is 79.9 Ω/□ while the 1870°C samples standard deviation is 42.4 Ω/□. These average values correspond to roughly $2x10^{19}$ cm^{-3} and $4x10^{19}$ cm^{-3} for the 1800°C and 1870°C samples respectively. The large standard deviation values are due to a large increase in sheet resistance within 2 cm of the center of the wafer. In fact, the calculated concentration at the center of the 1800°C wafer is approximately $6x10^{18}$ cm^{-3}. The average sheet resistance for GaP at 700°C is 278.2 Ω/□ while the 750°C average is 40.8 Ω/□. The standard deviation for the 700°C GaP is 3.7 Ω/□ while the 750°C samples standard deviation is 0.2 Ω/□. These average values correspond to $7x10^{18}$ cm^{-3} and $5x10^{19}$ cm^{-3} for the 700°C and 750°C samples respectively.

The significant difference in carrier concentration for the B samples suggests that the devices created within a 2 cm radius of the center of the wafer will not reproduce the results obtained in device simulation. This is because the use of the B delta-doping planes is critical to the ability to control charge distribution near the channel, and therefore the electric field within the channel.

6.2 Thermal I_{off} / Breakdown Testing

Chapter 5 contains the information obtained by subjecting the epitaxial layers to a high temperature for 30 minutes. A bias was swept over the top contact while the bottom contact was held at ground. Since the samples were etched, but did not include a gate the results obtained from the I-V characteristics suggest the off state current at a given V_{ds}. Similarly the point at which the current through the device crosses a specified level may be considered the breakdown for the device. Otherwise, when the slope of the I-V characteristic changes (increases) significantly may also be considered the point of source to drain punchthrough.

The results of the I_{off} testing can be found in Chapter 5, the results for breakdown testing are included in table 6.2. In table 6.2, solid black lines represent data collected prior to sintering, while the gray dashed lines represent data collected after sintering.

Control Sample		Breakdown Pre-Sinter (not pictured): 5.5V Breakdown Post-Sinter: 9V
775°C Sample		Breakdown Pre-Sinter: 5V Breakdown Post-Sinter: 5V

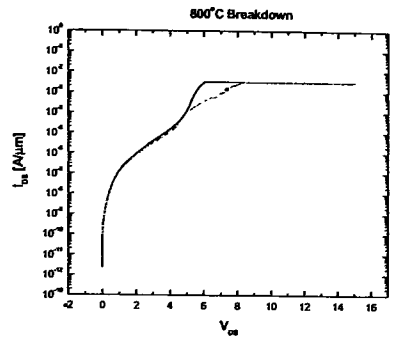
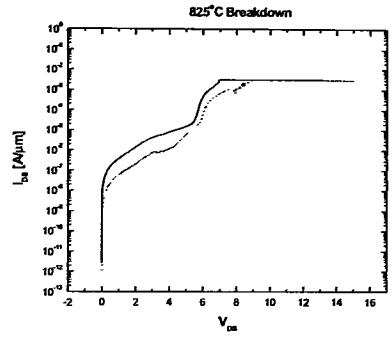
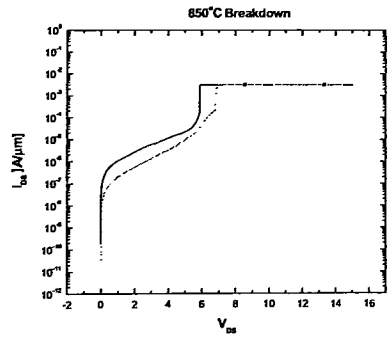
800°C Sample		Breakdown Pre-Sinter: 5V Breakdown Post-Sinter: 4V
825°C Sample		Breakdown Pre-Sinter: 4.5V Breakdown Post-Sinter: 6V
850°C Sample		Breakdown Pre-Sinter: 5.5V Breakdown Post-Sinter: 6V

Table 6.2: Thermal Testing – Breakdown

In table 6.2 the breakdown voltage is considered to be the point at which the slope of the I-V characteristics dramatically increase. It is evident that there is a tradeoff between off state current at 1V (from Ch. 5) and breakdown voltage. The samples prepared at 775°C and 800°C display the best off state current at $1x10^{-8}$ A/μm. However

the samples prepared at 825°C and 850°C, as well as the control sample show the best breakdown voltages from 5.5V to 9V.

6.3 Vertical MOSFET Testing

Vertical MOSFET devices were fabricated as described in chapter 5 to the design illustrated by chapter 3. During the back end of the device fabrication, the contact holes used to connect the device to metal bond pads blew out, most likely due to the increased etch rate of PECVD TEOS over thermal SiO_2. Unfortunately many of the devices gave characteristic shorts between drain and gate. Figure 6.1 illustrates I_{ds} vs. V_{ds} curves showing a field effect obtained from a device that did not show this shorting.

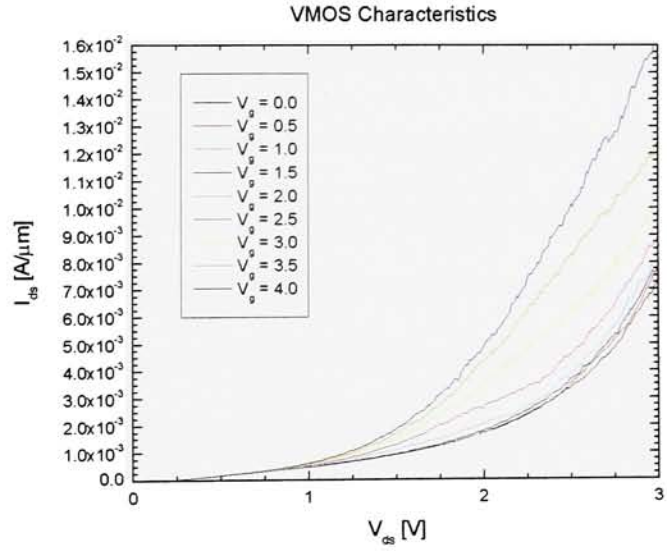


Figure 6.1: MOS I_{ds} - V_{ds} for a Vertical MOSFET

As figure 6.1 illustrates MOS characteristics can be observed for the fabricated devices. However, the I-V relationships seem to be combined with an excess diode current, if this V_g=0V current is subtracted from the curves obtained a normal family of

curves should be obtained, assuming that the added current is in fact parasitic diode current. Figure 6.2 illustrates the same curve, however with the V_g=0V current removed.

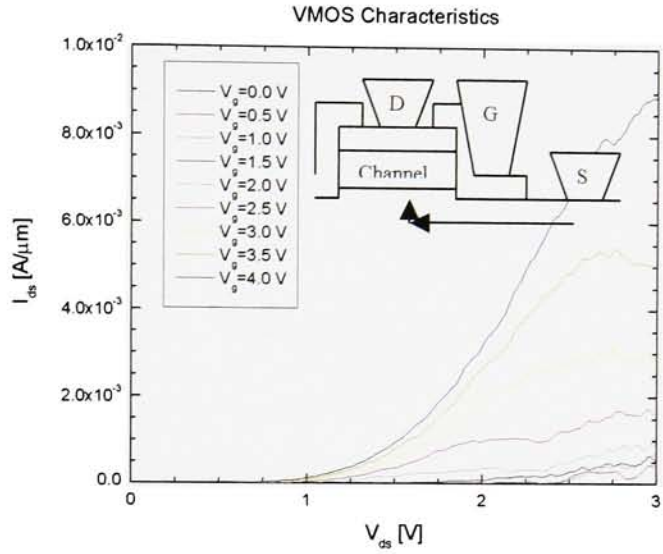


Figure 6.2: MOS I_{ds} - V_{ds} for Vertical MOSFET with V_g=0V Removed

It is observed in figure 6.2 that a field effect is demonstrated with excessive series resistance. This was anticipated as the device design places the source contact far from the channel region and in a manner that carriers must round an etched corner. The inset of figure 6.2 illustrates this. To obtain a plot featuring the saturation region of the vertical MOSFET device the voltage sweep on the drain was increased. However what was observed was not a MOSFET, instead a negative differential region was observed (NDR). Figure 6.3 shows the observed characteristic.

Upon reviewing the epitaxy growth process information, the observed characteristics are explainable. The as-grown samples featured a source / drain extension (SDE) region that was higher in concentration than originally planned. With two back-to-back p^+n^+ junctions a backwards diode was created. Figure 6.4 describes the as-grown epitaxial layers.

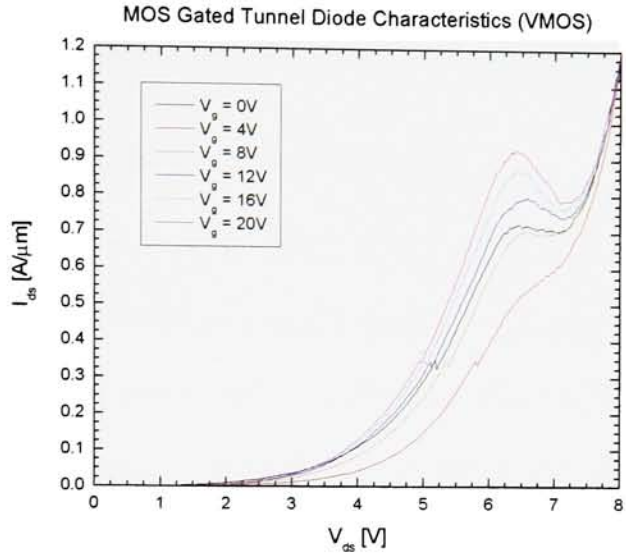


Figure 6.3: Increased V_{dd} Sweep on Vertical MOSFET Device

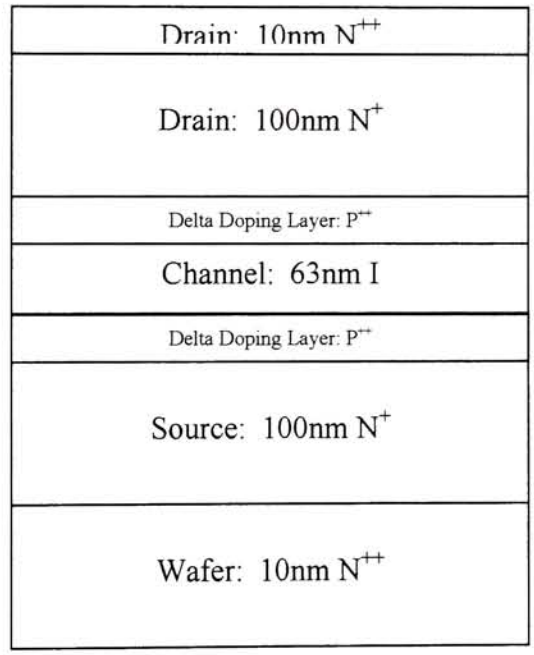


Figure 6.4: Epitaxial Layers

The results observed are consistent with those observed by Esaki in 1957 [1,2] and Chynoweth [3,4]. Esaki and Chynoweth were studying internal field emission in

very narrow Ge p-n junctions when they realized NDR in the I-V relationships of the diodes created by alloying. The results also concur with those of Rommel [5].

6.4 Analysis of MOS Gated Tunnel Diodes

It should be pointed out first that the device created by epitaxy is of the form of an Esaki diode. An Esaki diode features two degenerate, alternately typed regions adjacent to one another to create a band structure such as the one illustrated by Esaki (figure 6.5). The delta-doping planes cause an increased level of degeneracy of the band structure at the p^+n^+ junction. In the epitaxial growth of the vertical MOSFET device, SiGe was used as a diffusion inhibitor strapping the B delta-doping planes. Since the band gap for SiGe is thinner then that of normal Si, tunneling mechanisms may be enhanced due to the decreased tunneling barrier. Furthermore p-Si/SiGe heterointerfaces are well known to have a valence band discontinuity. This discontinuity enhances the δ–doping quantum welll.

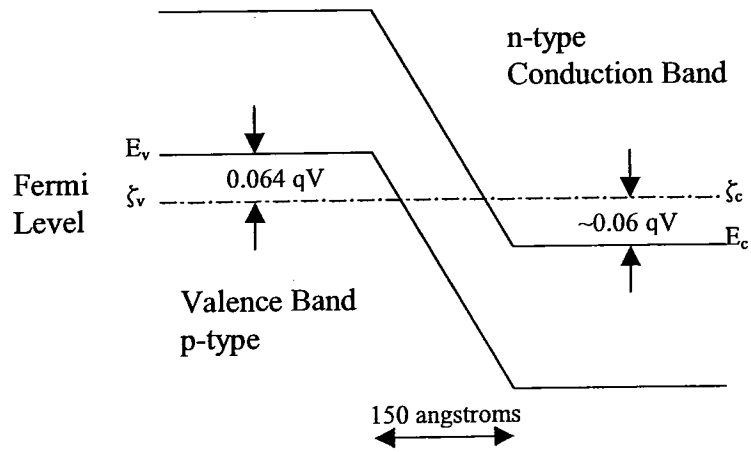


Figure 6.5: Energy Diagram of the p-n Junction at 300°K and No Bias Voltage. Adapted from [1]

When a bias is applied to the p^+ side of the device electrons tunnel from the n side of the junction to the empty valence band states on the p side. As this bias is increased fewer and fewer available states exist, and the probability of tunneling decreases [6]. At a high enough bias thermal carrier conduction occurs as is found in a normal p-n junction diode. The resulting characteristics can be seen in figure 6.6 [7,8].

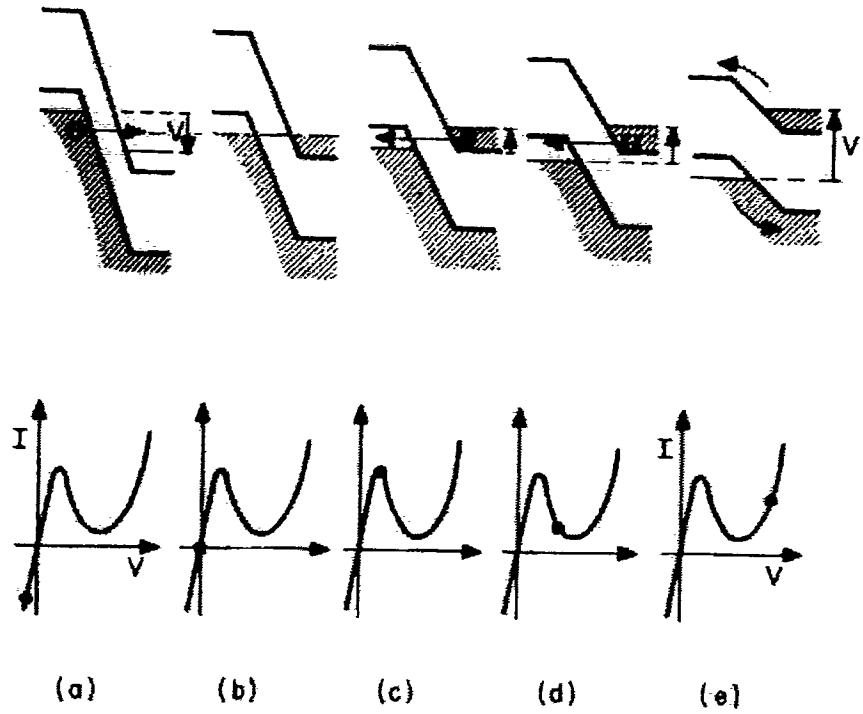


Figure 6.6: Simplified energy-band diagrams of tunnel diode at (a) reverse bias; (b) thermal equilibrium, zero bias; (c) forward bias such that peak current is obtained; (d) forward bias such that valley current is approached; and (e) forward bias with thermal current flowing. Adapted from [7*]

In the case of the fabricated vertical MOS Gated Tunnel Diode (MOSGTD), the device with no bias takes the form of a backwards diode, that is, a p^+n^+ junction diode in which the doping levels are not quite degenerate enough to form a tunnel diode. The backward diode does not form a NDR in its I-V characteristics, however the slope does flatten prior to thermal current becoming the dominant transport mechanism.

The device was designed for vertical MOSFET devices that could be easily contacted, and were not optimized for high speed. Because of this, the gate overlapped much of the drain, and a significant portion of the source. When a positive bias is applied to the gate, the n^+ SDE regions accumulate, while the p^{++} δ -doping planes deplete. The δ-doping planes are doped significantly high enough such that the depletion does not prevent the regions from being degenerate. However the n^+ region, which is weakly degenerate at V_g=0, accumulates to become degenerate at the surface. This combination of extremely highly doped regions forms a true Esaki diode [1,7].

Therefore, the device as grown is a backward diode, however, as a bias is applied to the gate, the device, at the silicon surface becomes an Esaki diode (figure 6.7). Furthermore, in device processing the epitaxial layers were subjected to a high temperature (775°C) for 30 minutes. A similar anneal temperature yielded a high peak-to-valley current ratio (PVCR) in a study by Duschl and Eberl [9], as well as Rommel, Thompson, Jin, and Berger [10,11].

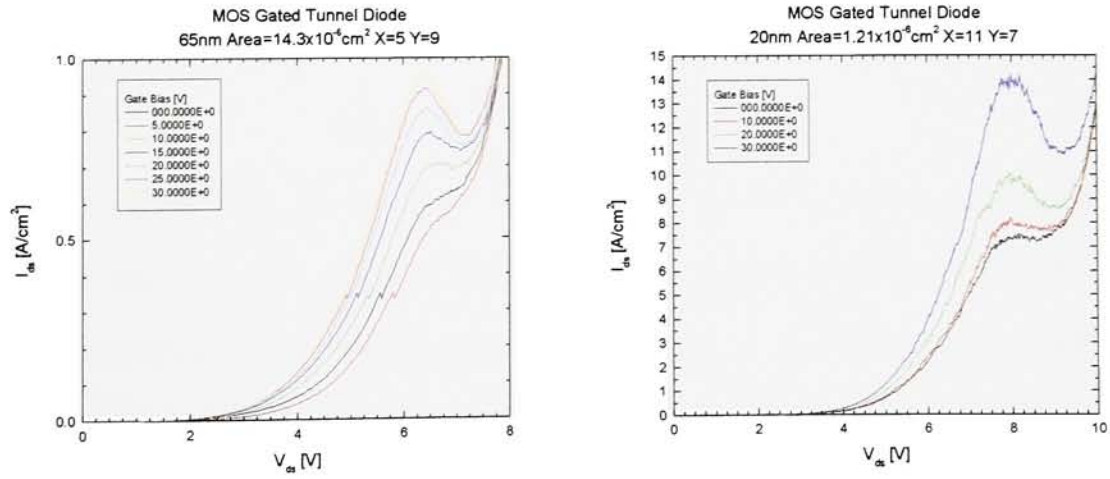


Figure 6.7: Demonstration of MOS Gated Tunnel Diodes

6.5 Wafer Variation and Effects on MOSGTDs

As reported previously in this chapter, the doping concentrations were not completely consistant across the diameter of each wafer. Similarly only one wafer featured a 65nm intrinsic region, while another featured a 20nm intrinsic region. These design and process variations allow for in-depth analysis of the fabricated devices, and the effects of delta-doping plane doping concentration, along with intrinsic region length.

Figure 6.8 illustrates the results of PVCR and Peak current density (I_{peak}) versus distance from center of the wafer.

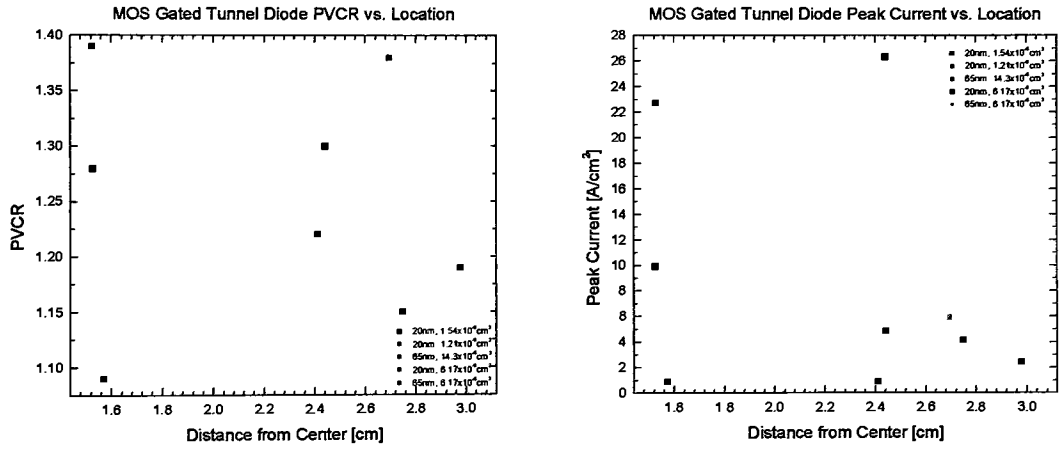


Figure 6.8: PVCR and I_{peak} vs. Location

Location does not appear to have an effect on PVCR for the devices built, however there is some correlation between device location and peak current. This is consistant with the work of RITDs fabricated by Thompson. It should also be noted that the areas of the devices are listed in the key for the plots above. The smaller the device area, the larger the percentage of depleted region is when the device is "on." Similarly the PVCR and I_{peak} may be observed with respect to varying device areas.

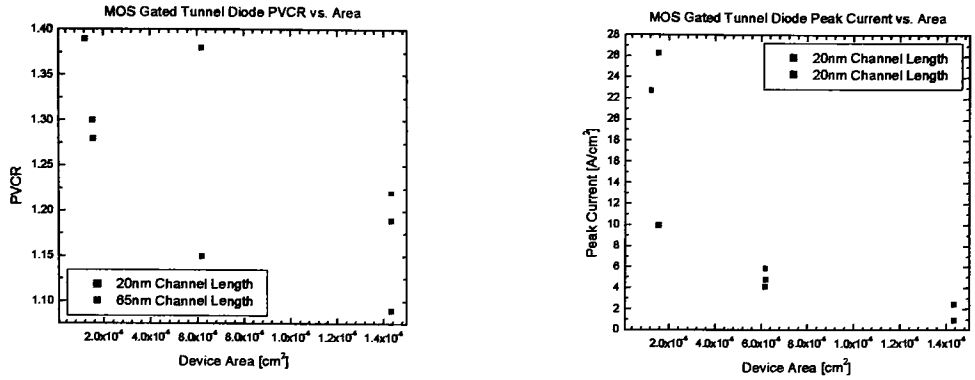


Figure 6.9: PVCR and I_{peak} vs. Device Size

There are good correlations between both PVCR and I_{peak} vs. device area as shown in figure 6.9. This makes sense since as noted above the percentage of area depleted by the use of a gate is larger in smaller area devices with respect to the larger area devices. The larger the device the larger the off-state current will be, in the case of the backward diode, thermal current. Superimpose tunneling current occurring in the depleted regions over this thermal current and the PVCR is obtained. The valley changing with different device sizes.

A comparison of PVCR vs. gate voltage for four devices of differing sizes and channel lengths shows a trend. The PVCR for each device increases with increasing gate voltage, until a "saturation" point in which the PVCR becomes constant. At this saturation point, the device is sufficiently degenerate on either side of the junction.

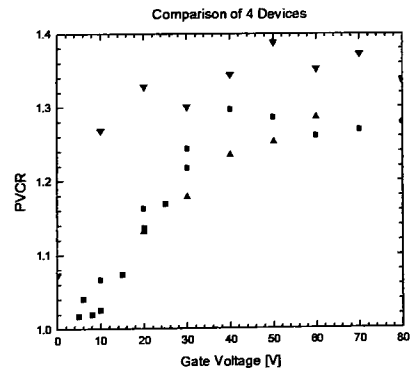


Figure 6.10: PVCR vs. Gate Voltage

[1] Esaki, L. "New Phenomenon in Narrow Germanium p-n Junctions," Physical Review, Vol. 109, Pg. 603, 1958.

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[5] Rommel, S.L.; "Si-Based Tunnel Diodes for Integrated Circuit Applications," Ph.D. Dissertation, University of Delaware, 1999.

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Chapter 7
CONCLUSIONS AND SUGGESTIONS

The concept for an ultra-scalable vertical MOSFET has been presented. The theoretical device has been simulated, proving the device's concept. Fabrication of the proposed device was completed, however the devices created did not exhibit the characteristics of a normal MOSFET. Instead the devices created, possibly the first of their kind, demonstrated characteristics befitting a three terminal MOS Gated Tunnel Diode.

The fabricated devices are far from ideal in terms of three terminal tunnel diodes, as well as from MOSFETs. In this chapter, suggestions for future work will be discussed to improve upon the designed device, as well as the demonstrated device.

7.1 Vertical MOSFET

The demonstrated devices do not exhibit characteristics of a MOSFET. The junctions preventing current transport from the source to the channel, and subsequently into the drain do not adequately prevent this transport in the devices off state. This is because carriers are able to tunnel through the junctions. The solution would be to use a

lesser doping in the source and drain extensions (SDEs). Similarly a relatively larger doping level should be used in the channel. The devices as-grown featured an intrinsic, or near intrinsic channel in order to improve channel mobility. The doping of the channel should be kept low, for this reason, however should be raised such that a potential barrier exists to carriers. The devices fabricated are very large, thin body devices have been proven to show improved subthreshold and short channel characteristics [1]. The vertical MOSFET can also benefit from the use of an ultra-thin body. Finally, the gate insulator used was 26nm of PECVD deposited TEOS oxide. Today's research devices, featuring channel lengths on the order of those studied here, use oxide thicknesses more then a decade thinner for appropriate control of the channel. The finished device should take the form of figure 7.1.

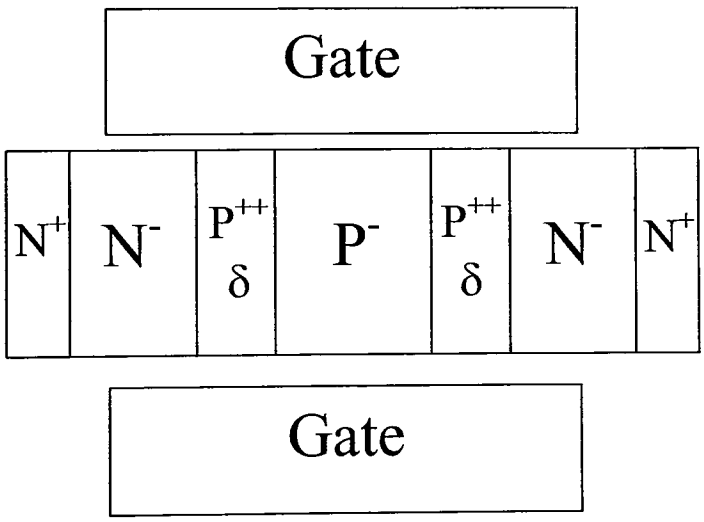

Figure 7.1: An optimized vertical MOSFET

7.2 MOS Gated Tunnel Diode

The MOS Gated Tunnel Diodes fabricated work very well, however they were not designed to be tunnel diodes. The design then can be optimized to serve their purpose

more appropriately. First only one $p^{++}n^{+}$ junction is required, separated by an intrinsic region such that both regions do not deplete further then the delta-doping planes that define them. The dopings on either side of the diode should be optimized such that when a threshold turn on voltage is reached, the p^{++} side does not deplete far enough to make the carrier concentration less than degenerate. Similarly at the same threshold gate voltage, the n^{+} side should become degenerate. Along these lines, the delta-doping plane on the n^{+} side of the device should be replaced with a n^{++} delta-doping plane [2]. SiGe should be incorporated entirely in the intrinsic region of the device. The thinner energy bandgap provides a thinner barrier for tunneling, making the probability of tunneling higher. The device should be made ultra-thin body. As was seen in this study, the current through the bulk of the device limited the devices PVCR. Finally, again the gate oxide should be made thinner, in order to better influence the carrier concentrations in the semiconductor. A schematic for an optimized MOS Gated Tunnel Diode would take the form of figure 7.2.

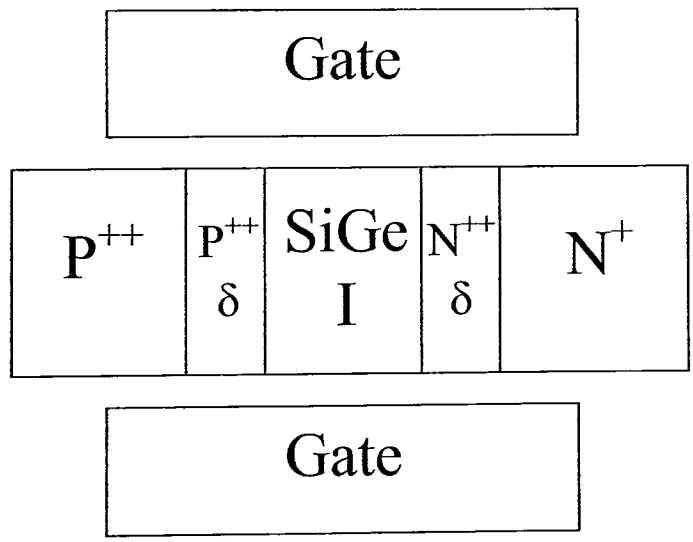

Figure 7.2: An optimized MOS Gated Tunnel Diode

[1] B.S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, R. Chau; "High Performance Fully-Depleted Tri-Gate CMOS Transistors," IEEE Electron Device Letters, Vol. 24, No. 4, April 2003 Page(s) 263-265.

[2] S.L. Rommel, N. Jin, T. E. Dillon, S. J. Di Giacomo, J. Banyai, B. M. Cord, C. D'Imperio, D. J. Hancock, N. Kirpalani, V. Emanuele, P. R. Berger, P. E. Thompson, K. D. Hobart, and R. Lake, "Development of d-B/i-Si/d-Sb and d-B/i-Si/d-Sb/i-Si/d-B Resonant Interband Tunnel Diodes For Integrated Circuit Applications," Proc. of the 58th Annual Device Research Conference, pp. 159-160, (2000).