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# A Simulation study of dispatching rules and rework strategies in semiconductor manufacturing

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# A SIMULATION STUDY OF DISPATCHING RULES AND REWORK STRATEGIES IN SEMICONDUCTOR MANUFACTURING

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A Simulation Study of Dispatching Rules and Rework Strategies in Semiconductor Manufacturing

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# ABSTRACT

The semiconductor industry is fast paced and on the cutting edge of technology, resulting in very short life spans of semiconductor products. In order to stay competitive, manufacturers must be able to quickly adapt to produce new products, and they must achieve a high level of productivity. Two major operational components of semiconductor fabrication plants (fabs) that effect productivity are dispatching rules and rework strategies. Although prior research has been conducted independently on these two issues, the hypothesis is that the interrelationship between the dispatching rules and rework strategies has a significant effect on the productivity of the fab. Moreover, the goal is to determine which combination of widely-used dispatching rules and new and existing rework strategies results in the highest level of fab productivity. To test this hypothesis, the significance of rework is evalutated, and a four-factor experiment is conducted to determine the effect of dispatching rules, rework strategies, fab types, and rework levels on key fab performance measures. Five dispatching rules are combined with three previously studied rework strategies and the first bottleneck strategy which is developed in this study. The treatment combinations are compared based on fab performance measures including cycle time, percentage on time, work-in-process, and the XTheoretical value. Simulation models based on actual fab data are constructed to carry out the experiments. The detailed results of the experiment show that combinations of dispatching rules and rework strategies have a significant impact on fab performance measures at each rework level in both fab types. In general, two dispatching rules, rework priority and first-in-first-out, in combination with the first bottleneck rework strategy perform the best. Further analysis concludes that the rework priority dispatching rule and the first bottleneck rework strategy result in the highest level of fab performance and are most robust over alterative fab configurations.

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# 1. INTRODUCTION

Semiconductor manufacturing refers to the production of integrated circuits, or devices. These devices have many functions, from simple transistors to memory chips and processors. Nearly everyone relies on such devices every day, whether they realize it or not. Some common places semiconductor devices are found are in computers, cellular phones, and automobiles.

Semiconductor devices are manufactured on silicon substrate material commonly referred to as a wafer. On the surface of each wafer are the integrated circuits (chips) that are formed during production. There can be hundreds of chips on a single wafer. These wafers travel through the semiconductor fabrication plant (fab) in lots, typically made up of 25 or 50 wafers.

Typically, the amount of processing that the device endures increases as the circuit design becomes more complex, and it is common for a wafer to go through three hundred or more processes during production. During this time, wafers may enter the same process, such as lithography, thirty or more times. The idea of going through the same process multiple times is referred to as re-entrant flow. Also, because of the high level of precision that the processes must adhere to, mistakes can be made and some wafers must be reworked, adding to the complexity of the fab. Therefore, there can be multiple products at various stages of fabrication (that is, at different masking layers) and wafers needing rework all waiting in the same queue. Furthermore, some stations process wafers individually, some process entire lots, and some process several lots simultaneously (batching). All of these things make the study and analysis of fabs very difficult.

For semiconductor manufacturers to stay competitive, they must be able to properly make decisions. Making these proper decisions allows them to quickly adapt to produce new products in a profitable manner, as the technology governing this industry changes daily. The importance

making the proper decisions is apparent when considering that the value of a finished wafer is at least $10,000 (Berkeley 2003). If the decisions used allow the fab to produce even one more lot per day, that would increase daily revenue by $240,000 - $500,000.

Two decisions that must be made in semiconductor manufacturing are what dispatching rule and rework strategy to use. Dispatching rules determine which lot is processed next from a queue when there is more than one lot waiting. Rework strategies define the relationship between the wafers from the lot that need rework, and those that do not need rework, as usually rework is not required for the entire lot. The term mother lot refers to the portion of the lot that does not need rework, and the term child lot refers to the portion of the lot that needs rework. An example of a rework strategy is to hold the mother lot while the child lot is being reworked, and then combine the two lots for all further processing (Zargar 1995).

There are many different dispatching rules and rework strategies that are used in fabs throughout the world. Fabs choose dispatching rules and rework strategies based on how they effect key performance measures, such as throughput, cycle time and its variability, and on time delivery. Much research has been undertaken focusing on dispatching rules and rework strategies independently. The result of these studies shows that choosing appropriate dispatching rules and rework strategies can greatly effect the performance of a fab and are essential for efficient and profitable production (Sheng-Yuan et al. 2001). This research focuses on how the interaction of dispatching rules and rework strategies effect performance measures. As small improvements in fab performance can have a large economic impact, an optimal combination of a dispatching rule and a rework strategy would be of great value to the semiconductor industry.

## 2. PROBLEM STATEMENT

Modern day fabs must be able to manufacture semiconductor devices in an efficient manner to stay competitive. In order do this, proper decisions must be made to maximize the productivity of the fab. Simulation has been the main tool used in research to test different operational decisions in fabs. The goal of such studies has been to develop rules and strategies that can be implemented in a full production fab. In order to validate these rules and strategies for such a purpose, all components of a realistic production fab must be accurately modeled. One of these components is rework. Reworking wafers adversely effects the performance of a fab, but is necessary because of the high costs associated with scrapping a wafer. However, the importance of including rework in simulation modeling has been inconclusive.

Since rework is present in fabs, determining how significant of an effect that rework has on the performance of a fab is important. If the presence of rework is shown to make significant differences in the performance of a fab, ways to lessen the detrimental effects that rework causes should be explored. Two major operational decisions that previous research has targeted are dispatching rules and rework strategies. Past research has explored these two decisions independently and has shown that choosing effective dispatching rules and rework strategies can lessen the adverse impact of rework in fabs. Therefore, these rules and strategies become important to the overall productivity (and thus profitability) of the fab.

The goal of this thesis is to determine if the presence of rework significantly effects the performance of a fab, and consequently to investigate how a combination of a rework strategy and dispatching rule at different rework levels and in different fab types effect key fab performance measures. Moreover, it is of interest to determine if there is a combination of a

rework strategy and a dispatching rule that is robust or if not, which combinations are best for various fab types and rework levels.

Simulation is used to execute a four-factor experiment, using dispatching rules, rework strategies, rework levels, and fab types as the factors. Realistic fab data is used to construct the simulation models and conclusions are formed based on detailed statistical analysis of the experimental results. One of the fab setups represents a make-to-order fab and the second fab represents a make-to-stock manufacturing environment. The rework data for each fab is set to three levels; one, five, and ten percent at all steps containing rework. Dispatching rules that are used include first-in-first-out (FIFO), shortest processing time (SPT), earliest due date (EDD), critical ratio (CR), and rework priority (RWK).

Four rework strategies are tested. The wait strategy holds the mother lot at the rework step until the child lot has gone through all rework steps, then the mother lot and child lot are combined for all further processing (Zargar 1995). The second strategy, the split strategy, permanently splits the mother lot and the child lot, therefore allowing the mother lot to continue processing while the child lot is being reworked (Zargar 1995). The next rework strategy that is tested is the rendezvous strategy, which splits the mother lot and the child lot, allowing the mother lot to go through the next processing step. After the mother lot goes through the next processing step, it is held there until the child lot has been reworked and goes through the next processing step, at which point they are combined for all further processing (Sha et al. 2001).

The last strategy, named the first bottleneck strategy, is developed in this research and splits the mother lot and child lot when rework occurs. The mother lot then goes thorough all processing stations until it reaches the first bottleneck station. The mother lot then waits to be processed at this bottleneck station until the child lot catches up to it, then the two are combined

for all further processing. The rework strategies and dispatching rules are evaluated based on fab performance measures including average cycle time, standard deviation of cycle time, percentage on time, percent idle, average work in process (WIP), and average XTheoretical (XT) value.

# 3. LITERATURE REVIEW

The semiconductor industry is an extremely fast paced, technology driven industry that is always changing. Currently it is at another major turning point in an attempt to take its technology to a new level when many companies increase their wafer size from 200mm to 300mm (sizes refer to the diameter of the wafer). This move should immensely improve the throughput for manufacturers, as a 300mm wafer can have more than twice the number of chips as a 200mm wafer (Aalund and Mathia 2001). Two of the main determinants of success in a fab are the ability to rapidly change to newer technologies and keep deliveries on time (Mittler and Schoemig 1999). The ability to do these things are closely related to being able to keep cycle times low which in turn keeps the fab more flexible to the volatile industry. This is magnified as the average life cycle of semiconductor product is roughly six months (Qi and Tang 2002).

In the semiconductor industry it is important to understand the relationships between WIP, utilization, yield, and time in the system. It is obvious that the more WIP a fab has the higher its machine utilization is as there are always lots waiting to be processed at each machine. This may seem like a good thing, but by overloading the system with WIP, for a given throughput rate ($\lambda$) the cycle time ($w$) is increased proportionally to the increase in WIP ($L$) as proven by Little's Law (Hopp 2001):

$$L = \lambda w .$$

This causes the fab to be rather inflexible to changes in demand and technology, as it takes a long time to get lots through the system. This is also major problem in the semiconductor industry because cycle time directly affects the quality of the wafer. The longer a wafer is on the floor, the more chance it has to become contaminated and consequently scrapped or sent for rework (Miller 1990).

### 3.1 Semiconductor versus Traditional Manufacturing

Semiconductor manufacturing deals mostly with high volume, low product mix production. This sort of mass production is traditionally characterized by an assembly line setup in a manufacturing plant where a station carries out the same process on the same or similar product all the time (Hopp 2001). Also, in a traditional assembly line, material moves down the line, therefore once it has gone through a certain station, it most likely will not return to that station for processing again. This is not at all the case in semiconductor manufacturing.

Fabs are much more complex than the traditional manufacturing plant. The greatest difference comes with the idea of re-entrant flow. A typical wafer must go through over three hundred process steps at a relatively small number of process stations before it becomes a finished product. This means that the lots enter the same process many times and are also moving about the manufacturing floor in a rather chaotic manner. To add to the difficulty, lots are batched in some operations to gain efficiencies in scale (i.e. oxidation), yet go through some processes, such as photolithography, as single wafers. A further cause of difficulty is the large number of different products that a fab produces simultaneously. The setup for the same machine can be different for each product and performing the setups can be time consuming and costly.

Another main reason for fab complexity is the cutting edge nature of the silicon wafer industry. New state-of-the-art machines are frequently being tried out in the line to test their capabilities and can disrupt the normal production flow. Also, because of the demanding nature of wafer specifications, machine downtime for adjustment and calibration is high. Resulting from these tight specifications is the need for some wafers to be reworked or even scrapped.

It is also important point to understand the extreme cleanliness that all of the processes must adhere to. Clean rooms are held to standards 1000 times more exacting than those of hospital rooms (Microelectronics 101 2002), and a single particle of smoke can ruin an entire wafer. Highly automated material handling systems minimize the need for human hands to interact with wafers during the process, and some fabs are now almost completely automated.

Lastly, the short product life of a wafer is a main contributor to the difficulty of wafer fabrication. Because of the intense pace of the industry, better components and processes are introduced quite often and this leads to changes in the product flow, routings, and also to the manufacturing equipment itself. As a result of the rapid development of wafer technology, in some fabs, research and development wafers with a high priority are sent through the manufacturing line and tie up resources that would otherwise be working on production wafers. In addition, much of the time it is hard to predict what the demand for a product will be at some period in the future. Therefore, it is not wise to build up large quantities of stock in such a volatile industry.

### 3.2 Overview of Semiconductor Fabrication Processes

This section gives an overview of the basic processes that are used in the production of silicon wafers. Unless specified otherwise, the primary source of this information was gathered from Jaeger (1993).

Silicon is the main material used for the production of integrated circuits, which are built on thin, circular frames called wafers. Currently, most wafers are being produced at 200mm (~8in.) in diameter and some companies are now in full production with 300mm (~12in.) fabs.

Wafers cycle through a set of processes many times in order to reach their finished state. These processes include:

- Oxidation
- Photolithography
- Etching
- Diffusion/Ion Implantation
- Chemical Vapor Deposition (CVD)/Evaporation/Sputtering
- Epitaxy

Oxidation is generally the first step in the wafer production. It involves the heating of a wafer in an oven at high temperatures to form a silicon dioxide layer on the surface of the wafer. To accomplish this, wafers are baked in either pure oxygen or water vapor, which act as the reactants that form the layer of silicon dioxide. Wafers are placed in the oven in batches to maximize the efficiency of this operation.

Photolithography (see Figure 3.1), next in the process, is the term used to describe all of the steps involved in transferring a pattern from a mask to the surface of the silicon wafer. After the silicon dioxide layer is formed, the wafer is thoroughly cleaned with an agent such as deionized water or hydrofluoric acid to remove any surface impurities. A photoresist is then applied and uniformity of thickness is achieved by spinning the wafer at high speeds in a process called coating. The wafer then goes through a soft baking process whose purpose is to improve photoresist adhesion to the silicon dioxide.

After the photoresist is applied, a photomask is placed onto the surface of the wafer. The photomask is used as a means of showing the future integrated circuit pattern. The photoresist that is not covered by the mask is exposed to high intensity ultra violet light in a stepper tool.

Next is a hard bake step to improve the adhesion between the unexposed photoresist and the silicon dioxide below it. The last step is called the developing step where the exposed photoresist is removed with a developing agent. Each time wafers go through photolithography, a new layer is formed. The amount of layers that are necessary for semiconductor devices varies greatly with the complexity of the device, as each layer plays an integral role in its functionality.

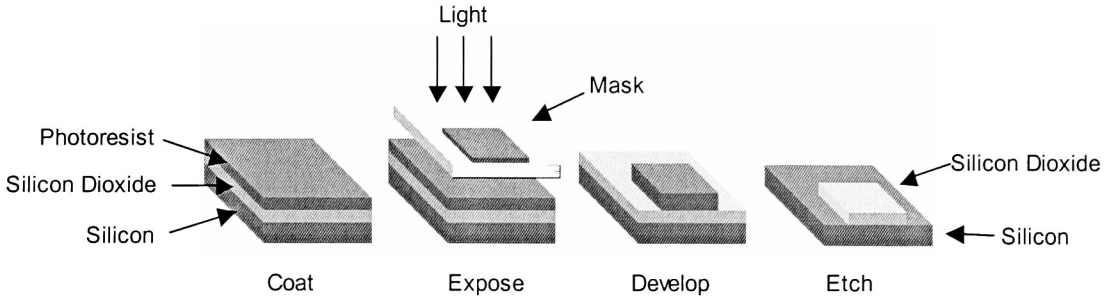


Figure 3.1. The Steps of Photolithography (www.ece.gatech.edu)

Following photolithography is an etching process that removes the silicon dioxide not protected by the photoresist. A couple different methods of etching are available, but the main techniques are wet and dry etching. Wet etching uses a chemical, which, when at room temperature, attacks and removes the silicon dioxide much faster than it attacks the exposed photoresist. Dry etching uses gases to remove the silicon dioxide while leaving the exposed photoresist still adhered to the silicon dioxide. After the etching is completed, an ashing step is carried out in which the remaining photoresist is removed leaving a silicon dioxide pattern and the rest of the silicon wafer exposed.

The next step for the wafer is a diffusion process that introduces conductive material (dopants) into the silicon lattice to change the electrical characteristics of the wafer's layers. The dopants that are commonly used are boron and phosphorous. There are two common ways that this process is carried out; by a spin-on dopant, or by a gaseous dopant. With the spin-on

method, the dopant is applied and the wafers are spun at high speeds to ensure uniformity across the wafer. The wafer is then heated at high temperatures to diffuse the impurities to a desired depth into the wafers surface. The gaseous method is similar, but instead of using a spin-on dopant, the wafer is placed in an oven with the dopant being an ambient gas flowing through the oven. The heating causes the impurities, which are in a gaseous form, to diffuse into the wafer's silicon crystal structure. Diffusion is a temperature dependent process, and therefore can occur at many different rates, but slow rate diffusion offers the most control and repeatability of the process.

Ion implantation can be used to perform the same function as diffusion. In ion implantation, the impurity atoms are shot into the surface of the wafer with a particle accelerator. There are some disadvantages of ion implantation. Wafers can only be implanted one at a time, while diffusion can process a batch of wafers simultaneously. Also, ion implantation causes damage to the lattice structure of the silicon and a subsequent annealing step must be done to repair the damage. Ion implantation is advantageous over diffusion as it allows for more precise doping through the control of the particle accelerator beam. Another advantage is that this process is done at low temperatures, preventing the undesired spreading of the impurity.

Thin film deposition refers to various materials that are required to be deposited on the wafer in many steps of wafer fabrication. Two of the methods of deposition are evaporation and chemical vapor deposition (CVD). Evaporation involves materials being heated to the point of vaporization, and are then evaporated on the wafer's surface. CVD is quite a bit different, as it forms the layer by directly applying the desired material from its gaseous state to a solid. Another form of deposition is sputtering, where the wafer's surface is bombarded with chosen ions. Sputtering is commonly used to form the gate and the source and drain contacts.

The last process to be discussed is epitaxy, which is the growth of a silicon crystal layer that is the same as the underlying lattice structure. This is done to create an ultra pure, contaminate free crystalline layer to enhance the performance of complex devices. This layer is deposited with a specific thickness and resistivity based on the customer demands (Epitaxy 2003).

The processes that are used in wafer manufacturing must be monitored closely to ensure that they meet the tight specifications placed upon them. When something goes wrong during processing, the effected wafers must be considered for rework, as scrapping them is extremely costly to the manufacturer, especially when they are far into production. While some defective wafers must be scrapped, most of the time defects caused at photolithography stations can be reworked. These defects are mainly caused by coating problems, focus and exposure defects, developer defects, edge-bead removal problems, contamination, and scratches (Ashkenaz 2002). When a wafer needs rework at the photolithography stations, it must go through an etch process to remove the resist, and then go through the photolithography steps again. This series of steps is commonly referred to as a rework loop (see Figure 3.2).

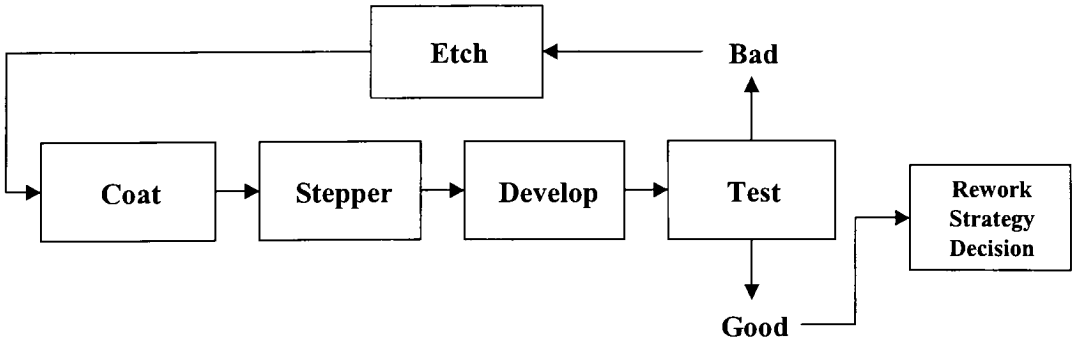


Figure 3.2. Typical Lithography Rework Loop

The presence of rework intuitively increases the cycle time and processing costs for not only the wafers being reworked, but for all of the wafers in the fab. Those increases must be

compared with the increased yield due to reworking nonconforming wafers. Since wafers are very expensive and each processing step adds value to the wafer, it is usually beneficial to rework wafers when possible. Also, many fabs produce wafers to order, therefore if a wafer has to be scrapped during production, a new wafer must be started and go through processing as a small lot, decreasing efficiencies gained by producing full lots.

### 3.3 Semiconductor Research Using Simulation

There are enormous amounts of rules and decision-making techniques that can govern the way that a manufacturing operation controls its floor. As stated in "The Goal" by Goldratt, the overall goal of any manufacturing operation is to make money; therefore key decision rules should developed around this specific goal. There are no closed form solutions to decide what dispatching rule or rework strategy to use in a particular fab because of the complexity and variability of the fabrication process. Simulation is the main tool used to compare and contrast these rules and strategies, as its main purpose is to analyze complex systems that contain variability. This makes simulation a great tool to use to test different rules in various scenarios and draw valid conclusions from the resulting data. Much research has been conducted that utilizes simulation in the semiconductor area, mainly dealing with dispatching rules, order release rules, and rework strategies.

Dispatching rules are decisions that determine the order that product will be processed from a queue. The purpose of these rules is to promote the efficient and profitable flow of product. Simple examples of dispatching rules are FIFO and SPT. FIFO dictates lots to beprocessed in order of their arrival while the SPT rule sends the product that has the shortest processing time on that given machine to the front of the queue. Other common dispatching rules

are based on: order of entry into the queue, how long a product has been in queue, when the product's due date is, how much processing time the product has left, how the tool is currently setup, etc. The method of determining what will be processed next from the queue can greatly alter key performance measures governing the overall efficiency of the fab and should be closely analyzed.

A literature review of relevant research done in the area of dispatching rules and rework strategies is conducted. Much of the early literature on dispatching and order release rules (rules governing when to release product into the fab) does not include rework in the modeling. Unfortunately there are not many reasons given to substantiate these claims. For instance, Collins, Torsina, and Balgemann (1999) assume that rework and scrap are not significant and are therefore omitted in their study. More recent research has included rework and has determined that rework does have an effect on some key performance measures in fabs. A study done by Grewal et al. (1999) focusing on validating cycle times discusses how sensitive the simulation results are to the rework level. The following literature review is divided into the following four areas:

1. Wafer Rework Strategies;
2. Dispatching Rules;
3. Order Release and Dispatching Rules; and
4. Order Release and Dispatching Rules with Rework.

### 3.3.1 Rework Strategies

As discussed previously, wafer rework strategies decide the relationship between rework wafers (child lot) and rest of the lot (mother lot) when rework occurs. Zargar (1995) researches

ways to deal with rework in the queue with respect to cycle time. The following four ways of dealing with rework are discussed:

1. Hold the mother lot while the child lot is reworked, and combine the two lots before moving it to the next processing station. The child lot gets priority in the rework loop.
2. Move the mother lot on, and send the child lot through the rework loop. The child lot does not have priority in queue, and then the child lot becomes a mother lot when the rework is completed.
3. Move the mother lot on, and introduce a new lot composed of numerous child lots when a predefined number of wafers have accumulated. These combined child lots then become a single mother lot.
4. Move the mother lot on, and add the child lot to the next mother lot of the same product at the tool.

There are positive and negative points concerning each of the strategies. The first strategy is favorable to management for tracking reasons, as the wafers continue on the same boat with the same lot throughout processing. The obvious downside is that the mother lot loses processing time while the wafers are reworked, and the cycle time of all lots will increase when queuing priority is given to the child lot in the rework loop. The second strategy allows the mother lot to continue processing, and since priority is not given to the child lot, the cycle time of other lots is effected to a lesser extent than with the first strategy. However, with this strategy, small lots are created and efficiencies associated with large lot sizes cannot be exploited. This strategy also makes tracing lots difficult.

The third strategy is like the second, except the efficiencies are not lost. However, the cycle time of the child lot is dramatically increased, as it must wait for a certain amount of

wafers of the same product type and at the same lithography step to accumulate before it can be processed. Tracking lots also becomes extremely difficult as wafers from many different lots are being combined. The fourth strategy attempts to balance the pros and cons of the previous strategies as efficiencies in scale are not lost and child lots should not have to wait very long before being joined with a mother lot. However, as Zargar points out, this strategy is not practical for use in the semiconductor industry. The main reason for this is that wafers travel in "boats" in the fab that are usually full, therefore there is no extra space for reworked wafers to join a mother lot. Leaving extra space in a boat in hope that the lot will pick up reworked wafers during processing is very risky, as throughput is lost if there is extra space at the end of processing. Tracing wafers is also difficult with this strategy.

This research uses a fairly simple fab model with three products, all of which have the same process flow and processing times. However, they cannot be processed together. Also, with the fourth strategy, lot size was not used as a constraint when adding the reworked wafers to the mother lot. Lastly, there were no machine failures allowed.

From the study, even in a small fab, it is shown that the rework strategy chosen can greatly alter the products cycle time. The conclusion drawn is that the fourth strategy decreases the average cycle time the most. While this is a significant conclusion, as previously discussed, this strategy is difficult to implement in a fab.

Sha et al. (2001) attempt to critique the work done by Zargar (1995) by highlighting the disadvantages of his strategies and also introduce two alternative strategies to deal with rework. Five strategies, three from Zargar (1995) and the two new strategies, are evaluated with respect to total cycle time, the quantity of WIP, machine utilization, and queue length at photolithography stations. Zargar's strategies that are used are the first, second, and fourth (see

above). The two new strategies that are introduced are the lot staging strategy and the rendezvous strategy. The lot staging strategy is similar to Zargar's third strategy except the child lots are reworked, and then wait for a certain number to accumulate before moving on. Child lots are not given priority in queue with this strategy. With the rendezvous strategy, the mother lot goes on for processing at the next station, then waits there for the child lot to be reworked and processed at the next station. The child lot is given priority, or "hot lot" status during the rework steps. The mother and child lot are then combined for all further processing. This strategy aims to lessen the amount of time that the mother lot waits for the child lot to be reworked, and is also good for wafer tracking purposes.

The fab that is used for simulation is based on the line introduced by Wein (1988), and consists of 24 stations. The simulation software AweSim is used to build the model, and each strategy is run for thirty replications for throughputs of 300, 400, and 500 lots. Lots are released into the fab using a poisson arrival process, and the FIFO dispatching rule is used at all stations. Processing times, machine failures, and machine repair times are all exponentially distributed.

A detailed analysis is done on the performance measures listed above and in all cases the rendezvous strategy is the superior strategy. Hypothesis tests are then conducted to show that there is a statistically significant difference between the rendezvous and Zargar's fourth strategy, which shows the second best results. The tests show the differences are significant at a 95 percent confidence level for all statistics except the waiting time in photolithography. This study concludes that the proposed rendezvous strategy is the best option for this for dealing with rework in the studied fab, as it has the best performance and makes lot tracing fairly simple.

### 3.3.2 Dispatching Rules

As stated previously, the purpose of a dispatching rule is to optimize key performance measures of a system by ensuring the efficient flow of product. The most typical performance measures looked at in semiconductor fabs are machine utilization, product yield, throughput, and cycle time (Mittler and Schoemig 1999, 709). Other performance measures that are commonly looked at are the variability of cycle time and the percentage of on time deliveries (Rose 2002 and Mittler et al. 1999). Certain dispatching rules are geared to the improvement of a given performance measurement. A good example of this is how using an EDD rule tends to improve on time delivery. While this may be true, it may also be negatively effecting other performance measures, such as cycle time. As a result of this effect, a combination of key performance measures should be analyzed when picking an optimal dispatching rule.

There is sound logic behind all proposed dispatching rules, yet some fit certain situations much better than others. This can be seen by comparing the FIFO and SPT rules, as there are obvious benefits and downsides to each. With the FIFO rule, a job may be in the back of the line, but it may be the most important job to get through that machine. That job has to wait for all lots in front of it to be processed. An advantage to FIFO is that lots will not get stuck in queue for large amounts of time because lots are processed in order of arrival. The SPT rule maximizes the throughput of the station as it always processes the job with the shortest processing time. However, it has trouble when there is a wide range of processing times for products in queue. In this case, jobs with large processing times may sit in queue for a very long time before being processed. One rule that can be used to combat the SPT problem is called $SPT^x$ (also known as absolute waiting time limit (AWTL)). This states that the "job to be worked next will be the one with the shortest processing time unless a job has waited $x$ time units

or longer, in which case it becomes the next job" (Hopp, 2001). It can be seen from this simple example that choosing a dispatching rule tailored to the specific needs of the manufacturing floor and processing station is instrumental to profitable product flow.

Arzi and Raviv (1998) discuss how the performance of a re-entrant production line with sequence dependent setup times can be improved with real-time dispatching rules. An extensive experiment is conducted to study the effect of four different dispatching heuristics on the performance measures of throughput, total setup time, and work in process (WIP).

The model constructed is based on two workstations, lithography and all of the other stations combined into one. When the machine finishes processing, a dispatching rule is used to determine what job is processed next. Then, all of the waiting jobs of chosen type are processed. This type of rule is useful at stations that have large setup times required when changing the product being processed.

The four dispatching rules studied are marginal set-up time, marginal set-up time with look ahead, marginal set-up with grouping principle, and marginal set-up time with grouping principle and look ahead. Marginal set-up time is a ratio of the set-up time for job j divided by the number of job j in queue. These ratios are calculated for each job, and the minimum ratio is chosen for dispatching. Choosing the minimum ratio allows the job with a small set-up time or with a large amount of jobs in queue to be processed next. Look ahead takes the total processing time for all of job j to be processed and uses this time to determine how many jobs of type j will arrive in this time. The jobs that will arrive during processing are added to the amount of jobs in the ratio calculation. The grouping principle looks to combine jobs with relatively short set-up times between the jobs, and these groups are then looked at as single jobs. As with the look ahead rule, all of the jobs in the group are added to the amount of jobs in the ratio calculation.

The marginal set-up time with grouping and look ahead is simply a combination of all three and uses the same ratio to determine what is processed next.

The simulations are run using SIMAN IV for a six-week production week with a warm-up period of twelve weeks. Two commonly used dispatching rules were also tested, FIFO and improved FIFO. Improved FIFO chooses the first job in queue unless there is a machine already running that job type, in which case the job is sent directly to that machine. The fab is loaded with five products that visit each workstation twelve times. Fab loading is tested at three levels, with exponentially distributed interarrival times of 58,67, and 49 min.

After all of the experiments are run, an analysis of variance (ANOVA) test is done to determine the significance of the individual factors. The factors that are concluded to be significant are the dispatching rule, loading level, and set-up time. Following this analysis, pairwise tests are carried out to determine if there is significance between each of the systems. The best results are obtained by using the marginal set-up with the grouping principle and no added value was found using look ahead.

Hung and Chen (1998) conduct a simulation study that compares many commonly used static dispatching rules with two "look-ahead" rules. The means of comparison in this study is based on product flow time, or cycle time. The goal of the study is to find a dispatching rule that reduces flow times while maintaining high machine utilization. They discuss the inherent trade off between flow time and machine utilization based and its relation to WIP.

The common dispatching rules that are studied are FIFO, SPT, shortest remaining processing time (SRPT), next queue length (NextQL), next queue time (NextQT), and EDD. The two proposed look-ahead rules that these are compared with are called SimBased and Queue Prediction (QP). SimBased uses a simulation within the simulation to determine the flow times

of the products in a given queue to determine what should be processed next. The product with the smallest expected flow time is chosen. The flow times are determined by simulating ahead a given number of processing steps. QP uses an analytical model to determine, based on historical data, the number of products in queue at a given point in time. The QP rule then chooses the lot that has the least average waiting time for a number of subsequent operations to be processed next. The number of processing steps to "look ahead" for each of these rules was optimized to four using simulation.

A ten-product fab with thirty workstations was used for the simulation. The fab is run for 24 months, using the first two months as a warm-up period. A fixed product mix and a changing product mix are also run in the fab. The results of the simulation show that the SRPT rule performs the best in terms of machine utilization and bottleneck flow time in both fabs. Hung and Chen reason that because SRPT uses more global information than the other dispatching rules, it performs the best. They go on to say that there is a great possibility for future research with the development of a shortest remaining flow time rule (SRFT). This rule would add the expected waiting time to the remaining processing time.

Cigolini et al. (1999) try to improve the current dispatching rules in place in a semiconductor manufacturing facility in Milan, Italy. The fab is very large, with over 250 different products being routed through more than 120 machine groups.

In the fab, the current dispatching rules that are used are dependent on the type of machine. For machines that can handle a single lot at a time, the lots are split into two queues, one for urgent jobs and one for normal jobs. If the machine requires a large set-up time, the lots are ordered in each of these queues according their setup times, with the shortest given priority. If two job lots have the same set-up time, the FIFO rule is used. When the machine becomes

idle, the first lot is taken from the urgent queue and if the urgent queue is empty, the first lots is taken from the normal queue.

Dispatching for machines that can batch lots is handled differently. It is first necessary to define the criteria for this dispatching strategy. MaxBS and MinBS refer to the maximum and minimum batch size, respectively, and WNLTT refers to the wait-no-longer-than-time. MaxBS, MinBS, and WNLTT are all predetermined values. At machines that batch lots, there is a single queue that contains both the normal and the urgent jobs. When the machine becomes idle, the queues are scanned for a batch that is greater or equal to MaxBS. If this is the case, that batch is immediately started. If there is not MaxBS in the queue, the machine will wait for WNLTT, or until MaxBS has accumulated in queue. If MaxBS occurs during the WNLTT, that batch is immediately started. If MaxBS has not occurred and WNLTT has passed, the queues will be scanned for MinBS, and if there is a batch meeting this criterion, it is immediately started. If MinBS is not met, a new WNLTT is started and the same rules are applied.

Cigolini et al. were tasked to develop new dispatching criteria for this fab. They again used different dispatching strategies for single lot and batching machines. For single lot machines, each is carefully categorized based upon its criticality to flexibility and capacity. A machine is said to be flexibility critical if it requires sequence-dependent set-up times and is said to be capacity critical if its average utilization rate accounts for more than a pre-determined threshold. For machines that are flexibility and capacity critical, a maximum capacity gain (MCG) dispatching rule is proposed. This rule attempts to minimize the overall set-up time among possible sequences of lots in queue. For machines that are only capacity critical, lots are divided into two queues. One of the queues contains lots that have processing times less than a predesignated level and are ordered by the SPT rule. The other queue contains the remaining

lots and is ordered by a slack per operation (S/OPN) rule. For machines that are only critical by flexibility, the minimum setup rule is used, with the S/OPN used in case of ties. In the last case, machines without either criticality, the S/OPN rule is used.

For workstations that batch lots, the criticality to capacity is again used, as well as MaxBS and WNLTT. For machines that are capacity critical, when the machine becomes idle it will check to see if MaxBS is available, and if it is, that batch is immediately processed. If this is not the case, WNLTT is used, and if MaxBS has not been reached by the WNLTT, the largest batch is immediately processed. The SPT rule is used to break ties if more than one batch has MaxBS available when the machine becomes idle. For non-critical machines, as soon as the machine becomes idle, the largest batch available is processed.

This new dispatching scheme was tested using a simulation model written in Siman V on a UNIX operating system. For the simulation, one worker was assigned to each machine and tools and fixtures were left out of the model. Also, there is no material handling and all buffer constraints are eliminated. The simulation model does include machine breakdown and repair data, preventative maintenance schedules, scrap losses, and random arrivals of urgent and normal lots to the system. The simulation model was run at three levels of loading: an average of 27, 30, and 33 lot starts per day.

The results of the simulation show that the new system improves average cycle time, WIP, and on time delivery. Also, it seems more capable of handling high workloads than the previous system. One downside of the new system is that it introduces more variability into the system. Implementation of the new dispatching strategies was not discussed in the paper.

A study done by Mittler and Schoemig (1999) compares three dispatching rules that claim to reduce the mean and variance of cycle time of small fabs (see Mittler and Schoemig

(1999) for a detailed explanation of the proposed rules). They are minimum inventory variability scheduling (MIVS), fluctuation policies for the mean of the cycle time (FSMCT), and the fluctuation policies for the variance of the cycle time (FSVCT). These three rules are compared to the traditional rules FIFO and EDD. The test is conducted on two MIMAC (Measurement and Improvement of Manufacturing Capacities) datasets, set one and three, which are available from the Arizona State University web site (Test Beds 2003). Dataset one has two products and 16,000 wafer starts per month, while dataset three has eleven products with 21,400 wafer starts per month. Both datasets contain rework but the rework strategy used in the study is not discussed. The statistics gathered are the mean cycle time (MCT) and the standard deviation of the cycle time (SCT).

For dataset one, FSVCT outperforms all other dispatching rules in MCT and SCT while MIVS only outperforms FIFO and EDD by a moderate amount. Both FIFO and EDD outperformed the FSMCT rule for dataset one. Very different results are obtained for dataset two, as MIVS outperforms the others in terms of mean cycle time. However, it only shows a 2.5 percent improvement over FIFO. For SCT, FSVCT performs better than all other dispatching rules and is about 22 percent better than FIFO. The conclusions drawn from this research are that the dispatching rules that are appropriate for small models are not applicable to these larger models. The performance of a given dispatching rule depends on characteristics of the fab, such as size and product mix and they recommend that managers use a dedicated simulation model of their particular fab for choosing dispatching rules.

Dabbas et al. (2001) attempt to validate the approach taken by Dabbas and Fowler (1999) on using a combined dispatching criterion to optimize multiple performance measures simultaneously. Simulation, using ManSim/X, is used to test the combined dispatching rule

against singular dispatching rules. This test is conducted on a mini-fab model and also on a full fab model.

The individual dispatching criterion that are combined in this study are critical ratio (CR), throughput (TP), flow control (FC), and Line Balance (LB). These criterion are given different weights, and the combined value of their weights is used to make dispatching decisions. Their respective weights are determined through experimental design and data transformation. This combined criterion is tested against the CR, fewest lots at next queue (FLNQ), and SPT rules individually. The performance measures used to compare these dispatching rules are on-time delivery (OTD), variance of OTD, MCT, and variance of MCT.

The simulation that is run is interrupted after some time has passed, and sends the current system state to a remote "User-Access" module. This module then generates a new list of priorities for all lots based on the current system status and sends the information back to the simulation. The simulation then runs until it is again interrupted.

The mini-fab model used has six workstations with three products, all of which use the same routing. The model analysis led to the following weights of .19, .19, .62, and 0 to LB, CR, TP, and FC, respectively. The results of this show that the combination dispatching rule significantly improves all performance measures versus the best single dispatching rule from those tested (CR, FLNQ, and SPT). Similar results were obtained in the full fab model. The weights used in the full model were .31, 0, .16, and .53 for LB, CR, TP, and FC, respectively. Statistically significant improvements were obtained between the combination rule and the best single dispatching rule for all performance measures except for the variation of MCT. For this measure, the CR rule performed as well as the combination rule.

This combination rule has been implemented in one of Motorola's semiconductor fabs since October 1998. Improvements in OTD, CT and lateness have been observed at this facility, giving the criterion credibility in industry. Recommended future research includes applying different weights to different types of machines, and developing a model where the weights will change with the status of the model.

Lee et al. (2001) introduce a new dispatching rule in this study, the balancing work content (BWC) rule. This rule gives priority in queue to those products that have more work and longer processing times at the bottleneck workstation ahead. The idea for this rule comes from the desire to never starve a bottleneck station, as that equates to forever lost throughput. It is considered to be a dynamic rule because it takes the current state of the system into account when making dispatching decisions.

The fab is modeled as two workstations (both bottlenecks) that product flows between with a delay time between leaving one and arriving at the other. The model is developed using Extend 4.0. Three different dispatching rules are considered, FIFO, SPT, and BWC, and the performance measures captured are the mean cycle time and the standard deviation of cycle time. Orders are released at a constant rate into the fab. Two situations are examined; deterministic processing times and stochastic processing times. For the stochastic processing times, three different coefficients of variation are used, .5, 1.0, and 1.5.

The results of this simulation show that the BWC rule gives a smaller mean cycle time and smaller standard deviation of cycle time than the other two rules in both situations. In fact, in the more realistic stochastic situation, BWC showed greater improvements than in the deterministic system. While these results are easy to see, there are no hypothesis tests done to prove that the differences in mean cycle time and the standard deviation of cycle time are

statistically significant. Furthermore, this model is very simplistic in nature and needs to be validated in a full fab model before its results can be credible in industry.

Rose (2001) conducts a study that focuses on the SPT rule and its effect on cycle time in a full fab simulation model. He proves that using this rule will decrease cycle time in a simple single stage model and is interested in whether extending these findings to a complex fab is an appropriate leap. Factory Explorer 2.6 from WWK is used to build the model, and the data used is set 6 from the Arizona State University MIMAC test bed.

Rose (2001) compares the FIFO rule to three variants of the SPT rule:

1. SPT and absolute waiting time limit (AWTL) – chooses the lot with the shortest processing time unless a lot has waited longer than the AWTL, in which case that lot gains priority in the queue.
2. SPT and mean waiting time limit (MWTL) – chooses the lot with the shortest processing time unless a lot has waited longer than a multiple of the average waiting time of all lots, in which case it gains priority in the queue.
3. FIFO or SPT according to queue length (FSQL) – ranks lots using FIFO unless a specified queue length is reached, in which case SPT becomes the raking rule.

A series of experiments are run varying the waiting time limits from one to thirty hours. The results show that there is no predictability when changing from the FIFO rule to an SPT rule. Some of the products had small increases or decreases in cycle time, but the majority showed no significant difference. Also, all of the variants tested result with cycle times that fall between the basic SPT rule and the FIFO rule. He attributes these findings to the fact that the SPT rule is a "local" rule and changes from workstation to workstation. "As a consequence, the effect of

using SPT depends both on the products' recipes and the product mix." He concludes that there is no general way to predict the change in cycle time using an SPT rule.

Rose (2002) examines the cycle time and on time delivery performance of a fab using the critical ratio (CR) dispatching rule. The CR rule is a ratio of the due date (Due) minus the current time (Now) divided by the total remaining processing time (TRPT),

$$CR = \begin{cases} \dfrac{1 + Due - Now}{1 + TRPT}, & if\ Due > Now \\ \dfrac{1}{(1 + Now - Due)(1 + TRPT)}, & otherwise. \end{cases}$$

He then discusses the importance of correctly determining the due dates of product when using the CR dispatching rule. He goes on to say that many fabs use a flow factor (FF) to determine due dates by multiplying the FF by the raw processing time to get an expected due date. FF refers the ratio of the actual processing time to the raw processing time of a product. FF is referred to as XTheoretical (XT) or the "X" Factor in other literature.

Six of the MIMAC datasets are used (1,3,4,5,6,7) using Factory Explorer 2.6 from WWK with a replication length of seven years with the first two years truncated as a warm up period. Datasets one and three contain rework data, but the rework strategy used is not discussed. The FIFO rule is used as a benchmark, and then the CR rule is used with the FF ranging from 1.0 to 3.5 in increments of .1.

The results of this study are rather striking, as a .1 step increase in the FF makes the cycle time drop nearly 100% in a some of cases. The magnitude of the cycle time improvements when the FF is increased are not seen in all the fabs tested, and depend heavily upon the loading of the fab. Rose concludes that in order to accurately set due dates using the CR dispatching rule, the fab must be simulated under heavily loaded conditions using the FIFO dispatching rule. From there, the average cycle times can be gathered, and dividing them by the raw processing time

gives the FF value for the product. He suggests that a small safety buffer of .1 or .2 is added to the FF value. He also notes using this methodology as compared to the FIFO rule will increase average cycle times by a small amount, but the increase in time delivery is worth the trade-off.

### 3.3.3 Order Release and Dispatching Rules

Wein (1988) performs a benchmark study in the semiconductor simulation field. This research is concerned with the effect that scheduling, particularly order release and dispatching rules, have on cycle time in a semiconductor fab. The order release rules tested are poisson, deterministic, constant work in process (CONWIP), and workload regulation (WR). Many dispatching rules are tested, including FIFO, SRPT, and lowest number in the next queue per machine (LWNQ/M). Refer to Wein (1988) for a detailed list and description of all of the proposed dispatching rules.

Three fabs are tested, each of which being slightly different than the other two. The differences in the fabs are based on the number of workstations and the number of operators. The configuration changes alter the number of bottleneck workstations in the fabs. All fabs have one job type with 124 operations. Some simplifying assumptions are made in this simulation. These include constant processing times at all stations, one product loading, no "hot" lots, and a simplified fab model.

The results of this study show that scheduling has a significant effect on average cycle time. It also concludes that the effect of order release rules have a greater impact than that of dispatching rules. In all three fabs, WR performed better than all other order release rules, followed by deterministic, CONWIP, and poisson. The optimal dispatching rule is dependent on the fab and the order release rule. For instance, SRPT performs better than FIFO for poisson

input, performs the same as FIFO with CONWIP policy, and performs worse than FIFO with a deterministic release policy.

Resulting from these findings, Wein concludes that input control (order release rule) can significantly improve the performance of wafer fabs. The amount of the improvement depends on the fab type and dispatching rule used. There are also some simplifying assumptions made in this research, and the effect of them must be understood in a full fab model to truly understand what impact scheduling can have.

Jeong and Lee (unknown) conduct a study to show how a combination of order release and dispatching rules effect fab performance. They use the fab line from Wein (1988) and make four variants of that line based on different types of machine failure in the wafer fab line. Four different order release strategies are used, deterministic, poisson process, WR, and starvation avoidance (SA). The dispatching rules used are FIFO, SRPT, LWNQ/M. Thirty replications of one year are performed for each combination.

In this experiment, Jeong and Lee compare the twelve combinations of policies at a level which 90% of the maximum throughput is observed. The deterministic order release rule gives the best cycle time performance, regardless of the dispatching rule used in combination. The best and worst policies are found to be the SRPT-SA and LWNQ/M-Poisson, respectively. This analysis is lacking more in depth statistical analysis including whether the differences in the different policies are significantly significant.

Bahaji, Nizar (2000) researches the effect that combinations of order release rules and dispatching rules have on various performance measures in fabs. These combinations are tested in two different fab settings, a make-to-order and a make-to-stock fab. The order release policies tested are a fixed release policy (push) and a constant WIP policy (pull). Fourteen dispatching

rules are tested in combination with these order release policies in both fab types. This study attempts to improve multiple performance measures simultaneously by using dynamic, composite dispatching rules that take the current state of the fab into account when making decisions.

Bahaji models dataset five from the MIMAC test beds using AutoSched AP. Dataset five is chosen as it is known to be the most complex from the test bed. This data set contains 21 products with 10,000 wafer starts per month. Rework is not included in this fab. The full fab is used for the make-to-order type fab, while three of the twenty-one products are used in the make-to-stock fab. The dispatching rules used include FIFO, CR, EDD, LWNQ, ESD, and many composite rules based upon these rules. Refer to the original research for an in-depth discussion of the dispatching rules used. Many performance measures are analyzed, including mean cycle time, standard deviation of cycle time, 98 percent cycle time, mean WIP level, mean throughput rate, mean tool group utilization, and mean tardiness. The method of replication and deletion is used to run ten replications of each of experiments.

When modeling the two different fab types, percent utilization, percent down, and average queue length are the factors that were taken into consideration. The releases of product in the three product fab are increased in an attempt to make these factors close to the same between fabs. To determine the due dates of the products, two times the theoretical processing time of the lot is added to the start date.

ANOVA and Ryan multiple comparison tests are used to determine which rules are significantly different from the others. The results, based upon these tests, conclude that the composite dispatching rule developed by Bahaji, Wt(PT+WINQ)/XF, performs very well for both fab types, both order release strategies, and for most performance measures. This rule uses

a ratio of the processing time (PT) of the lot plus the sum of processing times of lots in the next queue (WINQ) divided by the X Factor (XF) to attempt to give priority to lots that have small workloads at the next processing station and that are behind schedule. The formula for this rule is

$$Wt(PT + WINQ) / XF = \mathbf{exp}(-XF) \cdot \left( \frac{PT + WINQ}{XF} \right) + \mathbf{exp}(XF) \cdot \left( \frac{1}{XF} \right).$$

Bahija's findings are significant as a thorough statistical analysis is performed that compares many common benchmarked rules to the composite rules he developed. Also, the results show that the dispatching rules found to be robust are superior for most of the performance measures tested.

### 3.3.4 Order Release and Dispatching Rules with Rework

Some studies focus on the effect of rework, such as the study done by Sheng-Yuan et al. (2001) that concludes order release rules and dispatching strategies are affected by the presence of rework in the system. They go on to investigate the effect of three different levels of rework (1%, 5%, 10%) when different order release rules and dispatching strategies are used. The study uses a medium size fab in Taiwan for the simulation data.

The dispatching rules that used are divided into four categories that are developed by Blackstone et al. (1982).

1) Strategies involving processing time
2) Strategies involving due dates
3) Strategies involving neither processing time nor due dates (simple)
4) Strategies involving two or more of the first three classes (combined)

The rework strategy used is to hold the mother lot until the child lot has been reworked, then combine the child lot and the mother lot after the child lot has been reworked. This strategy is chosen because it is the most practical way that rework is handled in industry. The performance measures chosen are average WIP, average cycle time, standard deviation of cycle time, average tardiness, tardy rate, delay cost, and daily throughput. Due dates were established by using a flow factor of 4.4.

A full factor experiment is carried out with seven order release strategies, eight dispatching rules, and three levels of rework. The order release strategies used are WR, CONWIP, SA, uniform distribution (UNIF), poisson distribution (POISS), two-boundary (TB), and WCEDD. Dispatching strategies used are FIFO, EDD, CR, next queue length (NexQL), SRPT, COVERT, SA+, and TB+. Descriptions of the order release strategies and dispatching rules are not discussed. The three levels of rework are specified to be one, five, and ten percent. Each combination of strategies is run for six replications.

The conclusion to the study is that the overall system performance can be greatly improved by selecting appropriate order release strategies and dispatching rules based on different rework levels. The combinations of TB*EDD, TB*NexQL, WR*EDD, and WR*NexQL are the most stable combinations under the different rework conditions.

Some shortcomings of the research done by Sheng-Yuan et al. are that the conclusions are drawn on one fab that ran a three-product mix. It is appropriate to determine if similar conclusions can be drawn from different fabs running different product mixes. Also, hypothesis tests should be carried out on the performance measures to determine if there is differences are statistically significant.

# 4. THE SIGNIFICANCE OF REWORK

One thing for certain is that whether or not rework was included in previous research, rework is present in modern fabs (Reduce 2003). In past research, there are many different viewpoints on the importance of including rework in simulation models of semiconductor fabs that are discussed in Chapter 3. Some papers find that the inclusion of rework greatly alters performance measures (Grewal et al. 1999, Sheng-Yuan et al. 2001) while others use models that do not contain rework to draw conclusions (Collins, Torsina, and Balgemann, 1999, Rose 2001). This study's hypothesis is that the presence of rework significantly effects key fab performance measures, including average cycle time, standard deviation of cycle time, and average WIP.

To test this hypothesis, a simulation model of a fab without rework is constructed so the comparison of performance measures can be explored when rework is introduced to the model. Experiments are then run for both of these fabs, and the results are analyzed to determine whether the performance measures of these two fabs are significantly different. By showing that rework does significantly effect the performance measures in a fab and with the knowledge that rework is present in most modern fabs, including rework in semiconductor research becomes imperative.

## 4.1 Fab Description

Previous research shows the importance of modeling realistic fabs. For example, Mittler and Schoemig (1999) find that their proposed dispatching rules perform very well in small fab models, but perform poorly when tested in a larger, realistic fab model. Therefore, in an effort to draw conclusions valid to the semiconductor industry, realistic fab data is needed. The Arizona State University website (Test Beds 2003) contains the MIMAC datasets, which contain real fab

data that is largely used in past research. Three of the seven datasets contain rework, and of those three, dataset three is the most comprehensive, as it has the most products, eleven, and the most wafer starts per month, approximately 21,400. Therefore, dataset three is used to model the fab in this research. Refer to Appendix K for a more detailed description and data from this fab.

In this fab, a constant lot release policy is followed for all eleven products, processing times are constant, and the time between machine failures, machine repairs, and preventative maintenance tasks are exponentially distributed. Also, the products go through a range of 275 to 500 processing steps, with 7 to 15 masking layers. A masking layer refers to when a new pattern

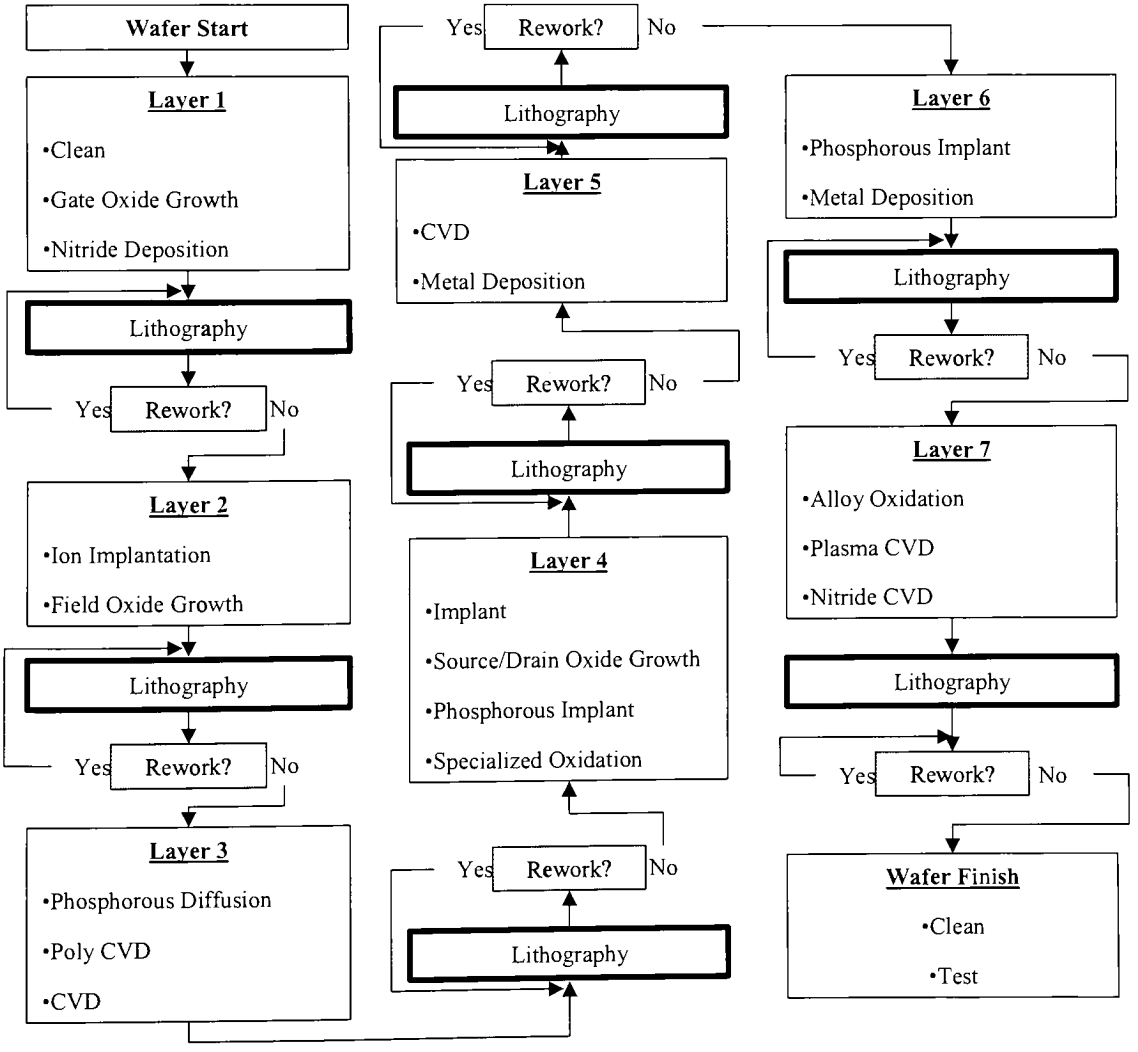


Figure 4.1. Flow of Product 9 through the Fab

is transferred to the wafers, which happens at lithography steps. It is at these lithography steps when the possibility for rework arises. Wafers travel through the fab in lots of fifty, therefore when the lot passes through a lithography step, some of the wafers will likely need to be reworked. The dataset contains values that specify the percentage of wafers that need to be reworked at each one of these steps. The values of potential rework range from .7 to 27 percent. Figure 4.1 shows the flow of product 9 through its processing. This particular product has the smallest routing of the eleven products, with 7 masking layers and 304 processing steps. The full routing for this product can be seen in Appendix K.

When rework occurs, the lot splits into a mother lot consisting of all of the wafers that do not need to be reworked, and into a child lot with all of the wafers needing rework. The mother lot then waits for the child lot to go through the necessary rework steps and once the child lot has completed the rework loop, the mother and child lot are combined together for all further processing.

There are 73 tool groups on which the wafers are processed. Some of these tool groups contain one machine, while some contain multiple machines. For instance, there are thirteen steppers that available for the lithography process. Wafers travel through these tool groups in a re-entrant manner, meaning the same wafer will visit the same machine numerous times. This behavior is one of the main difficulties in modeling semiconductor fabs. Also setups are needed at tools when a lot arrives that has different characteristics that the previous lot that the tool processed. These setup times and characteristics are defined in the dataset.

## 4.2 Simulation Model

To model this fab, the simulation software AutoSched AP developed by Brooks Automation is used. This software is geared towards semiconductor manufacturing and easily handles the complex processing parameters of a fab, such as rework and re-entrant flow. The interface of this software is based in Microsoft Excel, which allows for easy data transfer and manipulation.

All of the data described above is transferred into the AutoSched AP. There are some modeling assumptions that are important to note. One assumption deals with batching, which refers to tools being capable of handling multiple wafers or lots simultaneously. At such stations, the dataset gives the number of wafers that the tool can handle, which can then divided by fifty to give the number of lots that the tool can handle. The problem lies in that, in some cases, the tool can only handle 16 wafers at a time. Wafers travel in lots of 50, therefore at such tools, the load, unload, and processing times are quadrupled to adjust for the batching restrictions. However, the setup time will not be quadrupled, as the four batches are processed consecutively, therefore not needing setups between them. Also, the FIFO dispatching rule is used for all queuing decisions.

Two models are built, one containing rework and one without rework. These models are then evaluated to determine if the presence of rework effects key performance measures in the fabs. In the model containing rework, the rework strategy that is used holds the mother lot at the rework step until the child lot has completed the rework loop, and then combines them for all further processing. The performance measures analyzed are average cycle time, standard deviation of cycle time, and average WIP for both fabs.

### 4.3 Verification and Validation

After the simulation model is constructed, verification and validation steps are done to ensure that the model is working as intended and correctly represents the actual system. AutoSched AP has an extensive trace feature that allows each step of the simulation model to be closely scrutinized. This feature is used to verify that such things as the rework strategy, batching, setups, and machine downtimes are being modeled correctly.

After these things are verified, the model is validated against results for the fab from the MIMAC Test Bed (Test Beds 2003), which were obtained using Factory Explorer simulation software. These results are derived from one replication, with a warm-up period of 10,000 hours and a run length of 50,000 hours. Table 4.1 shows how similar the throughput is for each part between this model results and the reference values. Also, the cycle times are collected, and the differences in cycle times range from 5 to 10 percent, with an average of 7.3 percent. Based upon these results from only one replication, it is concluded that the fab is accurately representing the actual system.

Table 4.1. Validation Run Against Factory Explorer Results

| | Throughput (lots) | |
|---|---|---|
| Part | This Study | Reference |
| A | 2449 | 2445 |
| AT | 686 | 687 |
| C | 687 | 686 |
| D | 587 | 586 |
| F | 490 | 489 |
| H | 5976 | 5974 |
| R | 5192 | 5195 |
| U | 1909 | 1906 |
| X | 3233 | 3234 |
| Y | 2056 | 2056 |
| Z | 540 | 540 |

## 4.4 Analysis Methodology

Following the experiments, the results are analyzed using ANOVA tests to determine if there are statistically significant differences in the performance measures between the fab with rework and the fab without rework. The Minitab software program is used for this testing. From the ANOVA test, a p-value is generated, which denotes the level of confidence to which the values of the performance measures are different. For the purposes of this study, the performance measures in the fabs are said to be different if their p-values are .05 or smaller, meaning that the differences are significant at a confidence level of 95 percent.

## 4.5 Experimentation and Analysis

After the model is verified and validated, the experiments are run. As discussed above, the objective of this analysis is to determine the role that the presence of rework has on the chosen performance measures. The simulation models of the two systems are run, one with rework present, and one without rework. Each model was run for 10 replications of 50,000 hours each with a warm-up period of 10,000 hours.

An ANOVA test is then performed to determine if there are significant differences in the performance measures due to the presence of rework. The results in Table 4.2 show that at an alpha level of .05 (the detailed results of these simulation models can be seen in Appendix A), there is a significant difference between the fab with rework and the fab without rework for all of the performance measures studied. The results show that the average cycle time increases by five percent, the standard deviation of cycle time increases by six percent, and the average WIP increases by five percent when rework is included. Such differences can have a significant financial impact in semiconductor fabs.

Table 4.2. The Effect of Rework on Fab Performance Measures

| | Rework Fab | No Rework Fab | P-value |
|---|---|---|---|
| Avg. CT (hrs.) | 339.987 | 323.857 | 0.000 |
| St. Dev. CT (hrs.) | 83.238 | 78.721 | 0.000 |
| Avg. WIP (lots) | 189.137 | 180.166 | 0.000 |

## 4.6 Summary

From these results, it can be concluded that rework significantly effects the productivity of a fab. Consequently, research that does not include rework can lead to findings that are significant, but may not be achievable in a real fab. As the goal of most research is to have the findings be accepted in industry, rework should be included in semiconductor research involving shop floor control decisions.

Rework exists in and significantly impacts the performance of modern day fabs. Therefore, anything that can be done to minimize the detrimental impact that rework causes should be investigated. The rest of this research focuses on identifying operational decisions that can help to reduce the impact of rework, and to test these decisions in a simulation model.

# 5. A STUDY OF DISPATCHING RULES AND REWORK STRATEGIES

As discussed earlier, the semiconductor industry is fast paced and manufacturers must be able to quickly adapt to changes in the market. To do this, the dynamics of the fab must be thoroughly understood in order to make proper decisions that optimize the system relative to key performance measures. Based on the research in Chapter 4, the presence of rework is shown to have a significant effect on these key performance measures. Consequently, it is beneficial to investigate possible ways to minimize the negative impact that rework has in fabs. Past research has targeted dispatching rules and rework strategies independently to help fabs run efficiently in the presence of rework.

The scope of this work of this experiment is to evaluate alternative combinations of previously studied dispatching rules and new and existing rework strategies for use in semiconductor fabs. In particular, this study evaluates whether there is a robust combination that is best for all (or a large class of) fabs, or which combinations are best for various fab types and rework levels. Simulation is used to develop a valid model based on realistic fab data from the MIMAC test beds (Test Beds 2003). Using this model, a four-factor experiment is conducted to determine the effect of dispatching rules, rework strategies, rework levels, and fab types on fab performance measures. These performance measures include average cycle time, standard deviation of cycle time, percentage on time, average WIP, and average XT. Finally, conclusions are formed based on a detailed statistical analysis of the experimental results.

## 5.1 Methodology

### 5.1.1 Experimental Design

To evaluate combinations of rework strategies and dispatching rules, a four-factor full factorial experiment is conducted. The factors include dispatching rules, rework strategies, rework levels, and fab types. These factors and the factor levels are summarized in Table 5.1. A total of 120 experiments are run when all of the combinations of the factors are exhausted.

Table 5.1. Experimental Design

| Factors | Levels |
|---|---|
| Dispatching Rules | FIFO, SPT, EDD, CR, RWK |
| Rework Strategies | Wait, Split, Rendezvous, First Bottleneck |
| Rework Levels | 1%, 5%, 10% |
| Fab Types | Make-to-Order, Make-to-Stock |

#### 5.1.1.1 Dispatching Rules

The dispatching rules that are used include first-in-first-out (FIFO), shortest processing time (SPT), earliest due date (EDD), critical ratio (CR), and rework priority (RWK). These rules are chosen as they are commonly used in fabs and are the benchmark rules used in most of the semiconductor simulation research (see Mittler and Schoemig 1999, Lee et al 2001, Rose 2001, and Rose 2002). Although these rules are previously discussed in this research, the will be defined to avoid any confusion.

FIFO is the most common dispatching rule used in all manufacturing. This rule states that lots are processed in order of their arrival. This rule is beneficial in that it guarantees that lots do not get stuck in queue for large amounts of time resulting from other lots getting priority over them. The major drawback to FIFO is that lots cannot be expedited to improve performance, such as a lot gaining priority so that it can finish on time.

The SPT rule ranks lots in order of their processing time at that given station, with the shortest processing time given priority. If two lots have equal processing times, the FIFO rule is

used to break the tie. The advantage of using this rule is that the station's output rate will be maximized, with the disadvantage being that lots with relatively large processing times at a station may get stuck in queue for a long time. The third rule tested is the EDD rule that gives priority to lots that have the earliest due date. Intuitively, this rule aims to improve on time performance.

The next rule, CR, behaves similarly to EDD, but with one major difference. The CR rule uses a ratio,

$$CR = \frac{Time\ Until\ Due}{Remaining\ Processing\ Time},$$

to determine the queuing order, lowest value first. This ratio gets smaller as the value of the remaining processing time subtracted from the time until due gets small. Note that this calculation is slightly different than the CR formula presented by Rose (2002). This value is known as the slack time, or time remaining that the lot can spend in non-processing operations and still finish on time. When the CR equals one, the lot's time until due equals the remaining processing time, and if any time is spent in non-processing operations, it will be late.

The last rule tested is the RWK rule, which gives priority in queue to lots that are designated as rework lots. If there is more than one rework lot, the FIFO dispatching rule is used to determine the order in which the reworked lots are processed. With this rule, all non-rework lots are ordered using the FIFO rule. Once the rework lot joins the mother lot, which is dependent on the rework strategy chosen, the lot is no longer considered a rework lot. This rule is chosen as this study aims to minimize the impact of rework on a fab.

All of these rules are fairly simple to implement in a production fab. Of these rules, the most difficult to implement is the CR rule, as each time a new lot enters the queue, the CR of

each lot in queue must be calculated and ordered accordingly. Some sort of automated control system would make implementation of this rule much simpler.

#### 5.1.1.2 Rework Strategies

Four rework strategies are tested. Three of the strategies are previously studied, and one is developed in this research. The first strategy holds the mother lot at the rework step until the child lot has gone through all of the rework steps, then the mother lot and child lot are combined for all further processing (Zargar 1995). This strategy is called the wait (WAIT) strategy in further discussion. The second permanently splits the mother lot and the child lot, therefore allowing the mother lot to continue processing while the child lot is being reworked (Zargar 1995). This strategy is appropriately named the split (SP) strategy. The third strategy that is tested is the rendezvous strategy (RV), which splits the mother lot and the child lot, allowing the mother lot to go through the next processing step. After the mother lot goes through the next processing step, it is held at that processing step until the child lot has been reworked and goes through the next processing step, at which point they are combined for all further processing (Sha et al. 2001). The other rework strategies proposed by Zargar and Sha et al. are not used, as they are not practical in a semiconductor fab.

The fourth rework strategy that is tested is one that is derived in this research and named the first bottleneck (FBN) strategy.

**Definition:** *First Bottleneck (FBN) Rework Strategy* – Mother lot proceeds through all processing stations until the first bottleneck station and then waits to be rejoined with the reworked child lot.

This strategy splits the mother and the child lot when rework occurs, then sends the mother lot ahead for processing until it reaches the first bottleneck station. The mother lot then waits at the first bottleneck until the child lot arrives. The two lots are then combined for processing at the bottleneck station and for all further processing.

The first bottleneck station for the FBN rule is determined by running an experiment where the mother and child lots are split after rework occurs, and are then recombined at the station before the next possibility of rework. This gives the worst-case scenario in terms of station loading for each set of stations. The first station in each set that has above 85 percent utilization under this scenario is designated as the first bottleneck (Tyan et al. 2002). Before processing at this station, the mother lot waits for the child lot, and when the child lot arrives, they are combined for all further processing.

This strategy aims to capitalize on the underutilized stations following rework steps that are not considered to be bottlenecks. The mother lot and child lot will flow through these stations independently rather than as a combined lot, as they would with the WAIT and RV strategies. This major benefit of this strategy comes when some of these underutilized stations have per part processing times. Allowing the mother lot to flow through such stations ahead of the child lot can significantly reduce the cycle time of the lot. Furthermore, the mother lot waits at the bottleneck machine for the child lot, where it would be waiting in queue anyways. It is rather clear how this rework strategy can be advantageous when it is considered in this manner.

#### 5.1.1.3 Rework Levels and Fab Types

The rework data for each fab are set to three levels; one, five, and ten percent at all steps containing rework. These levels are chosen as they approximately span the range of the rework

level found in the MIMAC datasets. Rework levels range from .7 to 27 percent at lithography stations in the dataset, however, the majority of rework percentages are between one and ten percent. Furthermore, previous research that has been done that included rework has used these same three rework levels, such as the work done by Sheng-Yuan et al. (2001).

To model the two different fab types, fab three from the MIMAC Test Bed, which is described in Chapter 4.1, is used. The first fab uses all eleven products from the dataset to represent a make-to-order (MTO) type of fab. The second fab is the same fab with only two of the eleven products, to represent a make-to-stock (MTS) fab. The two chosen products have their arrivals increased so that the utilizations of the bottleneck stations are equivalent in both fabs. This allows the results to show whether the combinations of dispatching rules and wafer strategies are effected by fabs of different size and complexion while taking out variability of using completely different fabs. The data, including the routings, from these fabs can be seen in Appendix K.

### 5.1.2 Performance Measures

As discussed previously, the performance measures that are analyzed in this study are the average cycle time, standard deviation of cycle time, percentage on time, percent idle, average WIP, and average XT. These are chosen for a couple of reasons. First and foremost, they are very good indicators of the overall performance of a fab. Also, they are many of the commonly used performance measures in the papers discussed in the literature review chapter. Throughput was not used as a performance measure, as in this case, the throughput is not restricted by the capacity of the fab, rather it is restricted by the release rate of lots into the fab. Therefore, regardless of the strategy used, the throughput remains the same.

Average cycle time, standard deviation of cycle time, and average WIP are all easily understood performance measures. One that needs more explaining is percentage on time. In order to use percentage on time as a performance measure, there must be an acceptable way to determine product due dates. Rose (2002) proposes a method to do this using a flow factor approach (FF) that takes a ratio of the average cycle time and the raw processing time and adds a small buffer to the ratio to determine the due date. This is the method that is used to assign due dates in both of the fabs (see Chapter 3.3.2).

The FIFO/WAIT strategy is used for each of the three rework levels and in both fab types to determine the average cycle time for each product in each fab and at each rework level. From the average cycle time, the FF is determined by dividing the average cycle time by the raw processing time for that product.

Experiments are run that used different buffers to try and select a buffer that causes the fabs to achieve an on time percentage of approximately 90 percent. Ninty percent is chosen as it not only seems to be a realistic goal for a manufacturing facility to achieve, but is not too large so that differences in the strategies tested cannot be seen. The buffer chosen to achieve approximately 90 percent on time performance is .09.

The percent idle performance measure is a measure of the overall utilization of the fab, with higher percent idle being superior as the same throughput is being obtained with less utilization, therefore the product is being produced more efficiently. Finally, the average XT performance measure is a ratio of the actual cycle time to the raw processing time. The ideal XT value is 1, meaning that the lot has not waited at all during its processing, therefore its actual cycle time is equal to the raw processing time. Any time that the product waits during its

processing increases its XT value. This is a commonly used performance measure in semiconductor manufacturing.

### 5.1.3 Simulation Modeling

The simulation model developed for the experiment in Chapter 4 is used to model the MTO and MTS fabs. All of the of the different dispatching rules, rework strategies, and rework levels needed for these experiments are incorporated into the each of the models. These modifications were verified using the same methods as described in Section 4.3.

#### 5.1.3.1 Modeling the Make-to-Order Fab

As stated previously, the MTO fab uses all eleven products from the dataset. Appendix K contains information regarding this dataset. During verification of this fab, it is noticed that, at the ten percent rework level, the furnaces are highly utilized (over 99%) with a large average WIP in each queue. This is of concern, as any combination of rework strategy and dispatching rule that cause this queue to build up to a slightly larger amount could cause the system to never reach steady state, or explode. To alleviate this problem, furnaces are added to the model and tested in the 10 percent rework fab using all of the dispatching rules in this experiment. It is determined that adding four furnace 3's and two furnace 5's is enough to ensure that none of the dispatching rules cause the fab to explode under the WAIT, RV, and FBN rework strategies. Adding these furnaces does not significantly change the WIP at the rework stations, which are of main interest in this study.

### 5.1.3.2 Modeling the Make-to-Stock Fab

After the MTO fab (11 products) is built and verified, the MTS fab is constructed. Two products from the MTO fab (products 1 and 5) are used in the MTS fab. These products are chosen as they use all but two of the stations in the fab. The two stations that are not used are not bottleneck stations or involved in the rework steps. The interarrival times of these two products are decreased so that the bottleneck stations, mainly the furnaces and photolithography stations, have approximately the same utilization rates and average queue lengths as the MTO fab. The interarrival times of products one and five are changed from 20.81 to 4.16 hours and 17.47 to 10.48 hours, respectively.

As the interarrival times of these two products are decreased, the utilization of the furnaces become roughly the same as the MTO fab, but some small changes are needed at the furnaces, photolithography, and implant stations. The utilizations and queue lengths of these stations are not as large as they are in the MTO fab, therefore some minor changes are made to the fab and can be seen in Table 5.2. Making these changes is important because having small or empty queues at these stations renders the dispatching rules useless.

Table 5.2. Variation in Quantity of Stations between Fabs

| | Initial Fab | MTO | MTS |
|---|---|---|---|
| Stepper | 13 | 13 | 9 |
| Furnace3 | 8 | 12 | 8 |
| Furn 4 | 2 | 2 | 1 |
| Furnace5 | 2 | 4 | 2 |
| High Implant | 3 | 3 | 2 |
| Med Implant | 4 | 4 | 3 |

The utilizations and average queue lengths of stations with above 50 percent utilization in the MTO and MTS fabs can be seen below in Table 5.3.

### 5.1.3.3 Warm-up Period Determination

As semiconductor fabs are generally run continuously (non-terminating), there needs to be a warm-up period at the beginning of each simulation run to get the fab to steady state production prior to collecting the statistics that will be used for analysis. Even though the test bed contains a warm-up period to use, it needs to be verified as the models contains different rework

Table 5.3. Comparison of Station Utilization and Average Queue Length Between the Make-to-Stock and Make-to-Order Fabs

| | Utilization Comparison | | | Average Queue Length (lots) | | |
|---|---|---|---|---|---|---|
| **Station Name** | **MTO** | **MTS** | **Difference** | **MTO** | **MTS** | **Difference** |
| FURN3_Furnace_Tube | 99.92 | 99.91 | 0.01 | 5.87 | 5.53 | 0.34 |
| STEP_Photo_Stepper | 97.67 | 98.90 | -1.23 | 3.89 | 5.27 | -1.38 |
| FURN5_Furnace_Tube | 97.32 | 99.67 | -2.35 | 1.72 | 2.68 | -0.96 |
| FURN4_Furnace_Tube | 97.30 | 96.86 | 0.44 | 1.95 | 1.44 | 0.51 |
| FURN1_Furnace_Tube | 92.90 | 89.87 | 3.03 | 0.87 | 0.82 | 0.05 |
| HIGH_High_Current_Implant | 92.28 | 89.40 | 2.88 | 3.04 | 2.56 | 0.48 |
| MED_Med_Current_Implant | 90.72 | 87.41 | 3.31 | 3.89 | 3.18 | 0.71 |
| PR3_Probe | 89.68 | 86.87 | 2.81 | 0.61 | 0.55 | 0.06 |
| PHOS_Furnace_Tube | 82.85 | 51.39 | 31.46 | 0.41 | 0.06 | 0.35 |
| COAT5_Coater | 76.83 | 60.17 | 16.66 | 0.42 | 0.16 | 0.26 |
| PLAM_Dry_Etch | 75.78 | 59.21 | 16.57 | 0.62 | 0.21 | 0.41 |
| CVD1_CVD | 69.89 | 42.25 | 27.64 | 0.81 | 0.07 | 0.74 |
| PIRH2_Strip | 69.77 | 49.27 | 20.50 | 0.50 | 0.12 | 0.38 |
| CVD5_CVD | 69.65 | 48.88 | 20.77 | 0.67 | 0.21 | 0.46 |
| CVD4_CVD | 67.89 | 43.71 | 24.18 | 0.59 | 0.13 | 0.46 |
| LFE_Asher | 66.19 | 43.11 | 23.08 | 0.35 | 0.05 | 0.30 |
| WATJ_Metal_Dep | 65.72 | 46.85 | 18.87 | 0.34 | 0.06 | 0.28 |
| PR1_Probe | 65.56 | 16.31 | 49.25 | 0.04 | 0.00 | 0.04 |
| FURN2_Furnace_Tube | 62.27 | 35.40 | 26.87 | 0.21 | 0.03 | 0.18 |
| COAT1_Coater | 59.93 | 49.23 | 10.70 | 0.28 | 0.17 | 0.11 |
| PR2_Probe | 59.48 | 86.81 | -27.33 | 0.02 | 0.51 | -0.49 |
| CVD2_CVD | 50.27 | 33.19 | 17.08 | 0.06 | 0.01 | 0.05 |
| ITP_Metrology | 50.20 | 33.00 | 17.20 | 0.35 | 0.10 | 0.25 |
| EVAP_Metal_Dep | 50.01 | 28.97 | 21.04 | 0.24 | 0.07 | 0.17 |

percentages, dispatching rules, and rework strategies than the original dataset. A graphical method is used to determine the warm-up time in both the MTO and MTS fabs at ten percent rework using the WAIT rework strategy and the FIFO dispatching rule. If the appropriate warm-

up period is determined for the ten percent fabs, it is also large enough for the one and five percent rework fabs.

After the simulations are run, the average cycle time and WIP are plotted against time. Upon analyzing these plots, it is clear that the MTO system reaches steady state around 8,000 hours and the MTS fab previous to that. An example of this can be seen in Figure 5, which contains the first 20,000 hours of average cycle time and WIP data for the MTO fab. Therefore, the warm-up period is determined to be 10,000 hours, as a small buffer is added as a precaution to ensure the system is at steady state when data collection starts. It is interesting to note that this warmup time is the same as the given warmup time in the test bed.

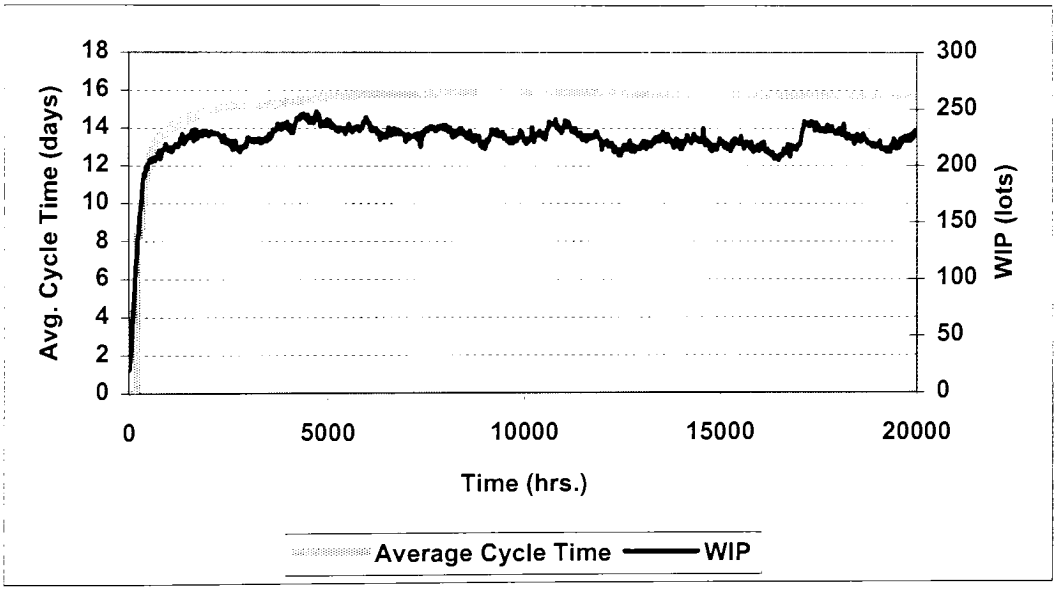


Figure 5.1. Average Cycle Time and WIP Plotted Against Time to Determine the Warmup Period

### 5.1.3.4 Data Collection Technique and Replication Length

The method of collecting data needs to be determined before experimentation can begin. There are a few common approaches that can be used, including the method of batch means and method of replication and deletion. The method of batch means allows each replication to begin with the system in the same state as when the previous replication ended and is the chosen for

this study. The method of batch means is chosen over the other common approach, the method of replication and deletion, as the method of batch means does not need a warm-up period for each replication. This becomes important when simulation time is taken into account, as the 10,000 hour warm-up period takes approximately 45 minutes to run.

In general, the longer the simulation replications are, the more representative of the actual system the resulting data will be. However, as previously stated, with this complex of a model, simulation time becomes a limiting factor. Therefore, ten replications of 50,000 hours each is chosen as an upper limit for run length. In an effort to reduce the length of the simulation replication runs, simulations are run with different replication lengths to determine if the differences in the results are statistically different than the 50,000 hour replications. If the results from between the 50,000 hour replications and shorter replications are not significantly different, the shorter replication length will be used.

Five simulations are run for ten replications each with run lengths at intervals of 10,000 hours, starting at 10,000 and ending at 50,000 hours in the MTO fab at ten percent rework using the FIFO/WAIT strategy. Hypothesis tests are done for each product, using paired t-tests at a 95 percent confidence level, to determine if the average cycle time and standard deviation of cycle time for each of the different run lengths differs from that of the 50,000 run length trial. It is determined that there are no significant differences in average cycle time between the 50,000 hour replication length and any of the others (see Table 5.4). For the standard deviation of cycle time, there was a significant difference between the 50,000 and 10,000 replication lengths for two of the products, but no significant differences for any of the other run lengths (see Table 5.3). Therefore, an appropriate replication run length was determined to be 20,000 hours.

Table 5.4 Paired T-Test for Difference in Means between 10,000 and 50,000 Hour Replications

| 10,000 vs. 50,000 hour replications | | |
|---|---|---|
| | P-value | 95% CI (hrs.) |
| A | 0.832 | (-9.17. 7.55) |
| AT | 0.797 | (-9.55, 7.54) |
| C | 0.805 | (-9.32, 7.44) |
| D | 0.916 | (-2.96, 3.26) |
| F | 0.988 | (-2.45, 2.49) |
| H | 0.89 | (-3.21, 2.83) |
| R | 0.861 | (-6.92, 5.89) |
| U | 0.822 | (-9.78, 7.96) |
| X | 0.843 | (-6.46, 5.39) |
| Y | 0.868 | (-7.18, 6.16) |
| Z | 0.61 | (-4.13, 2.57) |

Table 5.5. Paired T-Test for Difference in Standard Deviations between 10,000 and 50,000 Hour Replications, and 20,000 and 50,000 Hour Replications

| | 10,000 vs. 50,000 Hour Replications | | 20,000 vs. 50,000 Hour Replications | |
|---|---|---|---|---|
| | P-value | 95% CI (hrs.) | P-value | 95% CI (hrs.) |
| A | 0.21 | (-9.00, 2.27) | | |
| AT | 0.21 | (-10.15, 2.56) | | |
| C | 0.175 | (-10.36, 2.18) | | |
| D | 0.209 | (-2.246, 0.566) | | |
| F | 0.047 | (-2.865, -0.023)** | 0.15 | (-2.007, 0.361) |
| H | 0.132 | (-2.759, 0.427) | | |
| R | 0.156 | (-6.45, 1.21) | | |
| U | 0.174 | (-9.62, 2.02) | | |
| X | 0.164 | (-6.05, 1.20) | | |
| Y | 0.027 | (-7.72, -0.59)** | 0.202 | (-5.03, 1.22) |
| Z | 0.134 | (-2.782, 0.438) | | |

### 5.1.4 Statistical Analysis Methods

As stated previously, the goal of this thesis is to determine which dispatching rules, rework strategies, and combinations of the two are robust across performance measures in both fabs and at each rework level. In order to draw such conclusions, detailed statistical analysis is done. The statistical software program Minitab is used for this analysis.

Based upon the results previous research, it is expected that the factors tested in this research are significant. Bahaji (2000), Hsu et al. (2001), Sha et al. (2001), conclude that

dispatching rules and fab types, dispatching rules and rework levels, and rework strategies, respectively, are all significant factors. The following analysis methodology focuses on validating these findings and understanding how the interaction of these factors effect fab performance. All of the tests below are conducted for each of the performance measures tested.

Initially, an ANOVA test is conducted on all four factors studied to determine whether each of the factors (main effects) and their interactions (interaction effects) are significant. The output of the ANOVA test generates a confidence level, or p-value, that each of the factors and their interactions are significant at. In this study, a 95 percent confidence level is used to determine the significance of the factor and interaction terms. Therefore, a factor or interaction term with a p-value of .05 or smaller is said to be significant.

The significance of the interaction terms are of main interest from the four factor analysis. Specifically, the four factor interactions are expected to be significant, concluding that the different combinations of the four factors significantly effect the results of the performance measures. Based upon this result, the next step is to test for the significance of the three way interaction of dispatching rule, rework strategy, and rework level in each fab type. Once again, these three way interactions are expected to be significant.

After the three way interactions are shown to be significant, two factor ANOVA tests are done in each fab type and at each rework level. The results of these tests show, at each rework level and in each fab type, whether the dispatching rule and rework strategy are significant independently, and also whether the combination of a dispatching rule and rework strategy is significant. The hypothesis of this thesis anticipates this two way interaction to be significant.

Next, Tukey pairwise comparison tests are done on all factors determined to be significant from the two factor ANOVA tests. The dispatching rule, rework strategy, and

combination of the two are all anticipated to be significant. The Tukey test determines which factor levels are statistically significant from each other. Significance is determined by evaluating the confidence intervals generated for mean value of the performance measure of each factor level. Using this test, if the confidence intervals overlap for two factor levels, the factors are said to not be statistically different from each other. Alternatively, if the confidence intervals do not overlap, the factors are said to be statistically different from each other.

After this analysis, the dispatching rules, rework strategies, and combinations of dispatching rules and rework strategies that are the best for each performance measure, in each fab, and at each rework level can be determined (Law and Kelton 2000). It is important to note that, in some cases, there may be more than one dispatching rule, rework strategy, or combination of them that are significantly the best, but not significantly different from each other. For example, in the MTO fab at one percent rework, the FBN rework strategy may have the best results for average cycle time, but the results may not be significantly different from the WAIT strategy. In such cases, there is said to be a top group of strategies.

Now that the two factor analysis is complete, the top group of dispatching rules, rework strategies, and combinations can be charted to determine which are robust for most or all performance measures at all rework levels and fab types. For the purpose of this study, a strategy is considered if it appears in the top group of at least twenty-five percent of the performance measures.

From the previous analysis, if the fab type and rework level are known, the best combination of dispatching rule and rework strategy can be chosen to optimize one or more performance measures. However, determining whether there are dispatching rules and rework

strategies that are robust regardless of the fab type and rework level is important, as the fab type and rework level may not be fully understood or may change over time.

In order to make this generalization, the strategies that perform well in each fab type, regardless of rework level, are chosen. In each fab type there are three rework levels and five performance measures (percent idle is left out and is discussed in chapter seven); therefore there are fifteen separate groups a strategy may appear in. Based upon the criterion discussed previously, for a strategy to be considered, it must appear in the top group of at least four of the 15 performance measures groups.

Two factor ANOVA tests are done on this top group of strategies for each performance measure in each fab type using the dispatching rules and rework strategies as the factors. The data from all three rework levels is analyzed together, and the rework level is used as a blocking factor in the ANOVA analysis. This means that the differences in the performance measures due to the change in rework level are accounted for. Resulting from this ANOVA analysis, Tukey pairwise comparison tests are then done for all of the significant factors and interactions. These results show, in each fab type, which dispatching rule and rework strategy are the best regardless of rework level.

After the two factor analysis, another two factor analysis is done do determine which dispatching rule and rework strategy are the best regardless of rework level and fab type. To do this, the factor fab type is included in the ANOVA analysis as another blocking level. The same criterion is used to determine if a strategy is robust, that is, the strategy must appear in the top group of at least twenty-five percent of the performance measures. In this analysis, there are five performance measures, three rework levels, and two fabs, for a total of thirty top groups. Therefore, a strategy must appear in at least eight of the thirty to be considered robust.

Following ANOVA analysis of the robust strategies, for all factors that are considered significant, Tukey pairwise comparison tests are done to determine which dispatching rules and rework strategies are significantly different than the rest. From these tests, the best dispatching rule and rework strategy regardless of rework level and fab type are determined.

## 5.2 Analysis of Results

From the results of the analysis discussed in Section 5.1.4, there are some interesting observations regarding the split rework strategy and percent idle performance measure that need to be addressed. Following those sections, the results from the analysis are discussed in detail.

### 5.2.1 Split Strategy Results

During experimentation, it is discovered that using the SP rework strategy with any combination of dispatching rule and rework strategy at all rework levels causes the fabs to become overloaded and never reach steady state. Recall that the SP strategy causes all lots that need rework, which are usually of small quantities, to become their own independent lot and are never rejoined with their mother lot. Resulting from this, these small lots are being processed in tools that require long processing times, such as the oxidation furnaces. These stations are already highly utilized, therefore adding more lots at these stations causes their queues to build up faster than the station can process lots, causing WIP levels to constantly increase. Consequently, the SP strategy is not recommended in a fab with such numerous possibility for rework. A graph is shown below (Figure 5.2) that shows the average cycle time of the first 200 days for the WAIT and SP strategy. From this result, the SP strategy will be left out of the statistical analysis.

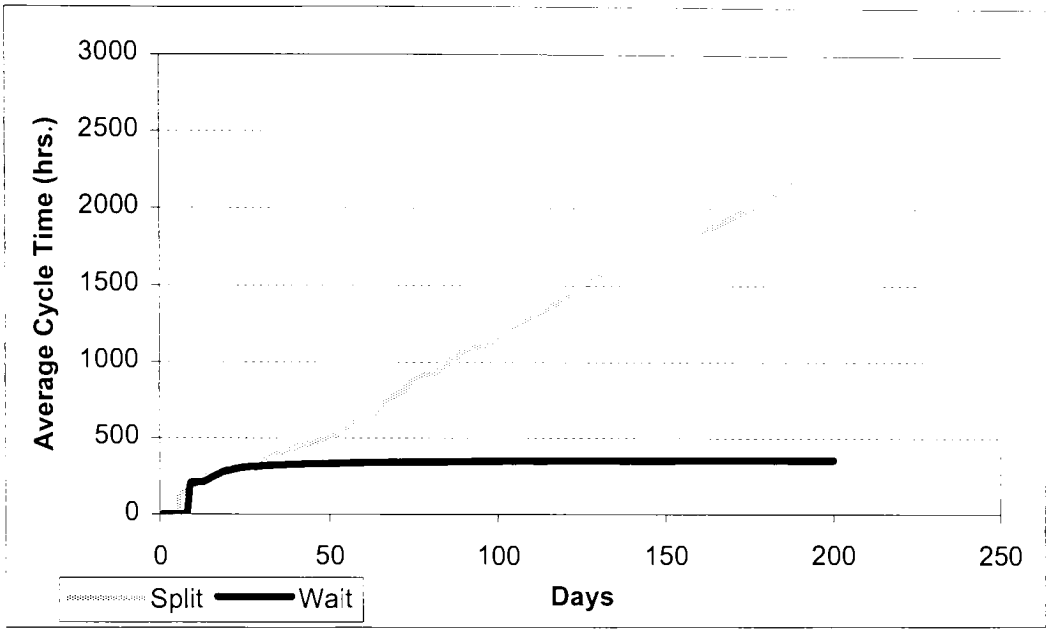


Figure 5.2. Comparison of Average Cycle Time between the Split and Wait Rework Strategies

### 5.2.2 Percent Idle Performance Measure

While initially looking at the experimental results, the percent idle performance measure becomes a concern. As previously stated, if a fab can achieve the same throughput with a higher idle rate, it is producing lots more efficiently. While this is true, the FBN and RV rework strategies inherently perform worse in this measure than the WAIT strategy. This is because all processing stations before the first bottleneck and the rendezvous point have their loading increased as both the child and mother lots travel through these stations independently. Therefore, this performance measure is biased towards the WAIT rework strategy. The results from this performance measure are tabulated in the analysis, but are not used when determining the robustness of a strategy.

### 5.2.3 Four Factor Analysis

After all of the experiments are run, an ANOVA analysis is conducted on all four factors in this experiment. The purpose of doing this is to determine which of the factors significantly effect the performance measures in the fabs. The results of this test show that all of the factors and their interactions are significant at 95 percent confidence for all of the performance measures tested. Table 5.6 shows the ANOVA results for average cycle time. In the ANOVA table, the factors, fab type, dispatching rule, rework strategy, and rework level, are denoted Fab, DR, RS, and RL respectively. The ANOVA tables for the other performance measures can be seen in Appendix C. Now that the all of the factors and their interactions are shown to be significant, ANOVA analysis is done for each fab type.

Table 5.6. Four-Factor ANOVA Table for Average Cycle Time

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| Fab | 1 | 559924.000 | 559924.000 | 559924.000 | 40000.000 | 0.000 |
| DR | 4 | 230462.000 | 230462.000 | 57615.000 | 4077.990 | 0.000 |
| RS | 2 | 79710.000 | 79710.000 | 39855.000 | 2820.920 | 0.000 |
| RL | 2 | 520896.000 | 520896.000 | 260448.000 | 18000.000 | 0.000 |
| Fab*DR | 4 | 1628.000 | 1628.000 | 407.000 | 28.800 | 0.000 |
| Fab*RS | 2 | 464.000 | 464.000 | 232.000 | 16.410 | 0.000 |
| Fab*RL | 2 | 12813.000 | 12813.000 | 6406.000 | 453.440 | 0.000 |
| DR*RS | 8 | 77275.000 | 77275.000 | 9659.000 | 683.680 | 0.000 |
| DR*RL | 8 | 130628.000 | 130628.000 | 16328.000 | 1155.720 | 0.000 |
| RS*RL | 4 | 48641.000 | 48641.000 | 12160.000 | 860.700 | 0.000 |
| Fab*DR*RS | 8 | 911.000 | 911.000 | 114.000 | 8.060 | 0.000 |
| Fab*DR*RL | 8 | 3124.000 | 3124.000 | 391.000 | 27.640 | 0.000 |
| Fab*RS*RL | 4 | 1329.000 | 1329.000 | 332.000 | 23.510 | 0.000 |
| DR*RS*RL | 16 | 35314.000 | 35314.000 | 2207.000 | 156.220 | 0.000 |
| Fab*DR*RS*RL | 16 | 4959.000 | 4959.000 | 310.000 | 21.940 | 0.000 |
| Error | 810 | 11444.000 | 11444.000 | 14.000 | | |
| Total | 899 | 1719521.000 | | | | |

### 5.2.4 Analysis of the Make-to-Order Fab

Following the fourfactor analysis, it is now necessary to determine if, for each fab type, each of the threefactors, dispatching rule, rework strategy, and rework level, and their interactions are significant. To determine their significance of these factors in the MTO fab,

ANOVA analysis is once again performed. The analysis concludes that, for all performance measures, all of the factors and their interactions are significant at a confidence level of 95 percent. The ANOVA tables for these tests can be seen in Appendix D.

Based upon these threefactor results, twofactor ANOVA analysis using the dispatching rule and rework strategy factors is now done for each rework level. The results of these tests show that the factors and their interactions are significant for all performance measures and at all rework levels. The raw data from these experiments can be seen in Appendix B. The ANOVA table for average cycle time at one percent rework can be seen in Table 5.7. The p-values in the right hand column show the level of significance that the factors are significant to. The p-values of .000 conclude that the factors are all significant to at least a 99.9 percent confidence level. The rest of the ANOVA tables for the MTO fab can be seen in Appendix E.

Table 5.7. ANOVA Table for Average Cycle Time in the MTO Fab at 1 Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 4 | 11127.730 | 11127.730 | 2781.930 | 2093.760 | 0.000 |
| **RS** | 2 | 157.390 | 157.390 | 78.690 | 59.230 | 0.000 |
| **DR*RS** | 8 | 103.810 | 103.810 | 12.980 | 9.770 | 0.000 |
| **Error** | 135 | 179.370 | 179.370 | 1.330 | | |
| **Total** | **149** | **11568.310** | | | | |

Now it can be said that the dispatching rule, rework strategy, and their interaction are all significant at each rework level in this fab. The next step in the analysis is to determine which dispatching rules, rework strategies, and combinations are significantly better than the others. Simply ranking the results from best to worst is not an acceptable method as there is variability associated with the experimental data. This variability has to be taken into account when determining whether one factor is significantly better than another. Therefore, Tukey pairwise comparison tests are used for this purpose, as they determine whether each dispatching rule,

rework strategy, and combination of them is statistically significant from each other at a predetermined confidence level. A 95 percent confidence level used in this research.

A pairwise comparison chart based upon these Tukey test results for average cycle time at one percent rework can be seen in Figure 5.3. The vertical lines in the significance column show the strategies that are statistically the same as each other. For example, in the leftmost table in Figure 5.3, the first strategy is not statistically different from the next three, but is statistically different that the fifth. The rest of the pairwise comparison tables for the MTO fab can be seen in Appendix E. After all of the Tukey pairwise comparison tests are done in the MTO fab, the top group of strategies for each performance measure and each rework level were charted to determine if a strategy is robust across rework levels and performance measures.

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 325.562 | |
| FIFO | FBN | 325.649 | |
| FIFO | RV | 326.826 | |
| RWK | RV | 326.838 | |
| RWK | WAIT | 327.826 | |
| FIFO | WAIT | 328.115 | |
| CR | FBN | 330.179 | |
| CR | WAIT | 331.295 | |
| CR | RV | 335.318 | |
| EDD | FBN | 335.957 | |
| EDD | WAIT | 337.769 | |
| EDD | RV | 338.190 | |
| SPT | FBN | 348.611 | |
| SPT | RV | 350.300 | |
| SPT | WAIT | 351.029 | |

| DR | Avg. CT | Significance |
|---|---|---|
| RWK | 326.7421 | |
| FIFO | 326.8633 | |
| CR | 332.2639 | |
| EDD | 337.3053 | |
| SPT | 349.9799 | |

| RS | Avg. CT | Significance |
|---|---|---|
| FBN | 333.1915 | |
| WAIT | 335.2068 | |
| RV | 335.4944 | |

Figure 5.3. Tukey Pairwise Comparison Test for Average Cycle Time in the MTO Fab at 1 Percent Rework

Table 5.8. Top Groups of Dispatching Rules in the Make-to-Order Fab

| % Rework | Avg. CT | Std. Dev. CT | % On Time | Avg. WIP | Avg. XT |
|---|---|---|---|---|---|
| 1 | RWK<br>FIFO | CR | RWK<br>FIFO<br>CR | RWK<br>FIFO | RWK<br>FIFO |
| 5 | RWK<br>FIFO | RWK<br>FIFO | RWK<br>FIFO | RWK<br>FIFO | RWK<br>FIFO |
| 10 | RWK | RWK<br>FIFO | RWK | RWK | RWK |

From these tables it is clear that the RWK and FIFO dispatching rules are robust at one and five percent rework (see Table 5.8), and then at ten percent rework, the RWK rule outperforms all other rules. For rework strategies, the FBN strategy created in this research is robust across all performance measures and rework levels, while the WAIT strategy only appears in a few instances (see Table 5.9).

Table 5.9. Top Groups of Rework Strategies in the Make-to-Order Fab

| % Rework | Avg. CT | Std. Dev. CT | % On Time | Avg. WIP | Avg. XT |
|---|---|---|---|---|---|
| 1 | FBN | WAIT<br>FBN | FBN | FBN | FBN |
| 5 | FBN | WAIT<br>FBN | FBN | FBN | FBN |
| 10 | FBN | FBN<br>WAIT | FBN | FBN | FBN<br>WAIT |

The primary interest in this research, the combination of a dispatching rule and rework strategy, shows that the rework strategy created in this study, FBN, performs very well in combination with the RWK and FIFO dispatching rules (see Table 5.10) at all rework levels. Once again, the reason that the FBN strategy is superior is that it allows the mother lot to go through non-bottleneck processing stations, especially per piece processing stations ahead of the child lot, thus saving processing time at these stations. For simplicity, the combination of a dispatching rule and a rework strategy will be referred to as a strategy from this point on in discussion. It is important to note that, although the RWK/FBN strategy finishes ahead of the

FIFO/FBN strategy for almost every performance measure, the differences between them are not statistically significant at a 95 percent confidence level.

It is also interesting to note that the CR rule, which is shown to be an effective rule for on time performance in previous research, performed poorly in general. This rule is only in a few top groups at one percent rework, and in none at five and ten percent rework. Also, the EDD and SPT dispatching rules are not in the any of the top groups at any rework level. Possible reasons for these findings are discussed in Section 5.3.

Table 5.10. Top Groups of Strategies in the Make-to-Order Fab

| % Rework | Avg. CT | Std. Dev. CT | % On Time | Avg. WIP | Avg. XT |
|---|---|---|---|---|---|
| 1 | RWK / FBN<br>FIFO / FBN<br>FIFO / RV<br>RWK / RV | CR / WAIT<br>CR / FBN | CR / FBN<br>CR / WAIT<br>RWK / FBN<br>FIFO / FBN<br>RWK / RV<br>FIFO / RV<br>RWK / WAIT<br>FIFO / WAIT | RWK / FBN<br>FIFO / FBN<br>FIFO / RV<br>RWK / RV | RWK / FBN<br>FIFO / FBN<br>FIFO / RV<br>RWK / RV |
| 5 | RWK / FBN<br>FIFO / FBN | RWK / FBN<br>FIFO / FBN<br>RWK / WAIT<br>FIFO / WAIT<br>CR / WAIT<br>RWK / RV<br>FIFO / RV | RWK / FBN<br>FIFO / FBN | RWK / FBN<br>FIFO / FBN | RWK / FBN<br>FIFO / FBN |
| 10 | RWK / FBN<br>FIFO / FBN | RWK / FBN<br>RWK / WAIT<br>FIFO / FBN<br>FIFO / WAIT<br>RWK / RV<br>FIFO / RV | RWK / FBN<br>FIFO / FBN<br>RWK / WAIT<br>FIFO / WAIT | RWK / FBN<br>FIFO / FBN | RWK / FBN<br>FIFO / FBN<br>RWK / WAIT |

### 5.2.5 Analysis of the Make-to-Stock Fab

Analysis of the data from the MTS fab experiments show results that are very similar to those of the MTO fab. The raw data from these experiments can be seen in Appendix B. Once again, the three factor ANOVA analysis is done with the dispatching rule, rework strategy, and rework level factors. The results show that the factors and their interactions are all significant at

95 percent confidence for all performance measures. These ANOVA tables can be seen in Appendix F.

Based upon these results, twofactor ANOVA tests are done on all combinations of dispatching rules and rework strategies at each level of rework. For all of the performance measures and at all rework levels, the factors and their interactions are found to be significant at a 95 percent confidence level with the following exceptions. At one percent rework, the rework strategy and the interaction of dispatching rule and rework strategy for the standard deviation of cycle time are not significant. Also, at one percent rework, the interaction of dispatching rule and rework strategy for percent idle is not significant. The full ANOVA results can be seen in Appendix G.

As done in the MTO fab, Tukey pairwise comparison tests are conducted for each of the factors and their interactions to determine what factors and interactions are statistically superior to the others. The full results can be seen in Appendix G. Table 5.11 shows the top groups of dispatching rules, and from this table, it is clear that the RWK and FIFO dispatching rules are again the best for the one and five percent rework levels, and for the ten percent rework level, the RWK rule becomes superior.

Table 5.11. Top Group of Dispatching Rules in the Make-to-Stock Fab

| % Rework | Avg. CT | Std. Dev. CT | % On Time | Avg. WIP | Avg. XT |
|---|---|---|---|---|---|
| 1 | RWK | FIFO | CR | RWK | RWK |
| | FIFO | RWK | RWK | FIFO | FIFO |
| | | | FIFO | | |
| 5 | RWK | RWK | RWK | RWK | RWK |
| | FIFO | FIFO | FIFO | FIFO | FIFO |
| 10 | RWK | RWK | RWK | RWK | RWK |
| | | FIFO | | | |

Furthermore, the FBN rework strategy is once again very robust across all performance measures and rework levels (see Table 5.12). There are only two instances where there are other

strategies in the top group, and they are both in the standard deviation of cycle time performance measure. Also very similar to the MTO fab, the strategies that are the most robust are again RWK/FBN and FIFO/FBN (see Table 5.13). It can once again be noticed that the CR, EDD, and SPT dispatching rules do not perform well for most of the performance measures. The CR rule is only in the top group of dispatching rules for percentage on time at one percent rework, and in a couple of top strategies at one percent rework. The EDD and SPT rules are once again not in any top groups. Possible reasons for these findings will be discussed in Chapter 5.3.

Table 5.12. Top Groups of Rework Strategies in the Make-to-Stock Fab

| % Rework | Avg. CT | Std. Dev. CT | % On Time | Avg. WIP | Avg. XT |
|---|---|---|---|---|---|
| 1 | FBN | FBN<br>WAIT<br>RV | FBN | FBN | FBN |
| 5 | FBN | FBN | FBN | FBN | FBN |
| 10 | FBN | FBN<br>WAIT | FBN | FBN | FBN |

Table 5.13. Top Groups of Strategies in the Make-to-Stock Fab

| % Rework | Avg. CT | Std. Dev. CT | % On Time | Avg. WIP | Avg. XT |
|---|---|---|---|---|---|
| 1 | RWK / FBN<br>FIFO / FBN<br>RWK / RV<br>FIFO / RV<br>RWK / WAIT | RWK / FBN<br>FIFO / FBN<br>FIFO / RV<br>RWK / RV<br>FIFO / WAIT<br>RWK / WAIT<br>CR / FBN<br>CR / RV | CR / FBN<br>CR / WAIT<br>FIFO / FBN<br>RWK / FBN | RWK / FBN<br>FIFO / FBN<br>RWK / RV<br>FIFO / RV<br>RWK / WAIT | FIFO / FBN<br>RWK / FBN<br>RWK / RV<br>FIFO / RV<br>RWK / WAIT<br>FIFO / WAIT |
| 5 | RWK / FBN<br>FIFO / FBN | RWK / FBN<br>FIFO / FBN<br>RWK / RV<br>FIFO / RV<br>RWK / WAIT<br>FIFO / WAIT | RWK / FBN<br>FIFO / FBN<br>CR / FBN<br>RWK / WAIT<br>RWK / RV<br>FIFO / RV | RWK / FBN<br>FIFO / FBN | RWK / FBN<br>FIFO / FBN |
| 10 | RWK / FBN<br>FIFO / FBN | RWK / FBN<br>FIFO / FBN<br>RWK / WAIT<br>RWK / RV<br>FIFO / WAIT<br>FIFO / RV | RWK / FBN<br>FIFO / FBN<br>RWK / WAIT | RWK / FBN<br>FIFO / FBN | RWK / FBN<br>FIFO / FBN<br>RWK /WAIT |

## 5.3 Performance of the CR, EDD, and SPT Dispatching Rules

In previous research, the CR and EDD dispatching rules are shown to be good for the percentage on time performance measure. Rose (2002) derives a heuristic for using the flow factor (FF) to set due dates in combination with the CR dispatching rule to achieve good on time performance. That methodology for setting due dates is used in this research, yet the results are contradictory to the findings from his study. The reason for this could be that these rules tend to make the products finish processing very close to their due dates with a small amount of slack. Slack refers to the difference in the time until due and the remaining processing time. In other words, the slack time is the maximum amount of time the lot can spend waiting to be processed before it becomes late. Therefore, when a has a small slack time and needs rework, the added time it spends in the rework loop will most likely make the lot late regardless of the dispatching rule or rework strategy used.

Figure 5.4 shows the slack time remaining when the lot finished processing for the EDD/WAIT and the FIFO/WAIT strategies in the MTO fab with ten percent rework. In this case, negative and positive slack denote the lot being early and late, respectively, with zero being the exactly on time. As a result, any lots finishing processing after their due date have a positive slack value. These graphs show how the EDD/WAIT dispatching rule has a rather peculiar distribution with two distinct peaks and a large upper tail. This is much different than the FIFO/WAIT distribution, which appears to be normally distributed. Consequently, the EDD distribution causes many lots to be late by a small amount of time and the range of slack values is much larger than with FIFO.

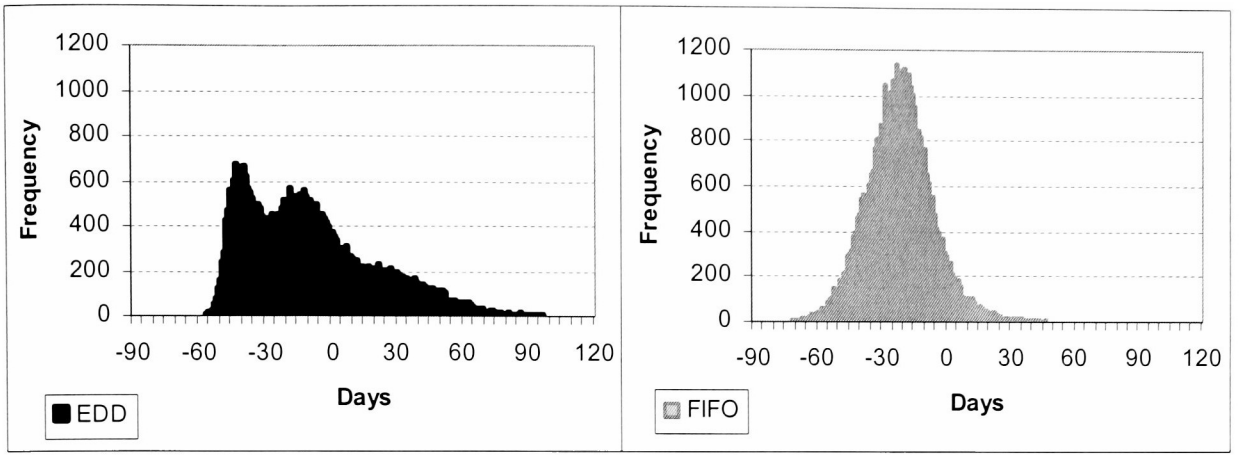


Figure 5.4. Slack Time for the EDD/WAIT and FIFO/WAIT strategies

The SPT rule performs poorly for all of the performance measures. The cause of this is most likely that the products with large processing times at a station get stuck in queue for a long time before they are selected for processing. The difference in on time performance between the SPT/WAIT and FIFO/WAIT strategies at ten percent rework can be seen in Figure 5.5. The parts are denoted with a lettering scheme on the x-axis. This graph shows how a few parts have good on time performance (e.g. Z) with the SPT rule, but others suffer at the expense of them (e.g. X). The routings for these parts can be seen in Appendix K.

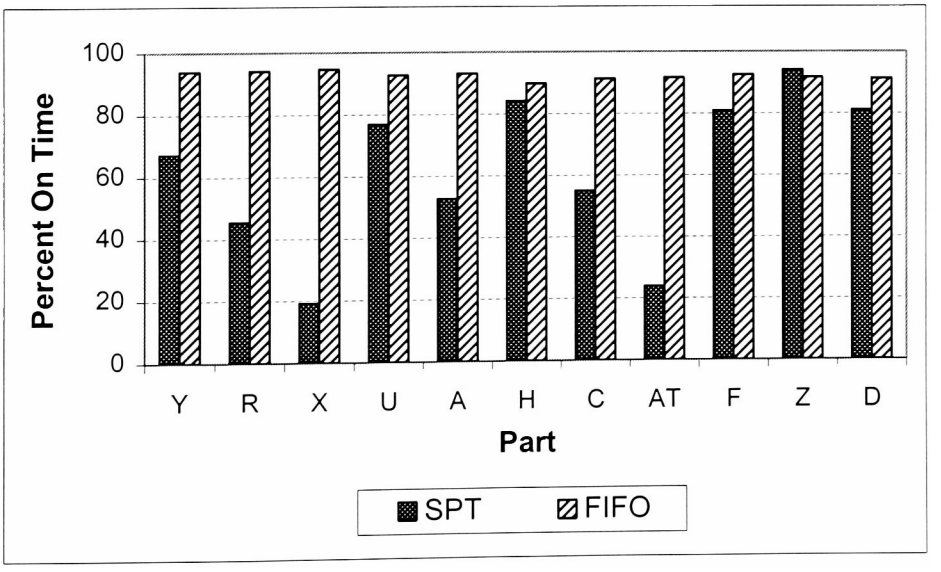


Figure 5.5. Percent On Time Comparison Between SPT/WAIT and FIFO/WAIT at Ten Percent Rework

## 5.4 Analysis of Robust Strategies

Resulting from the RWK/FBN and FIFO/FBN strategies being superior, it is decided to further analyze these two, along with the other strategies that perform fairly well across rework levels and fab types. The purpose of doing this is to determine if there is a strategy that is significantly superior across all performance measures regardless of rework level, and subsequently, regardless of rework level and fab type. A strategy is considered for this study if it appears in the top group of at least twenty-five percent of the performance measures.

### 5.4.1 Two Factor Analysis to Determine Robust Strategy in Each Fab Type

To determine if there is a dispatching rule and rework strategy that is superior regardless of rework level, a two factor analysis is conducted for the strategies that perform wellin each fab type using rework level as a blocking factor For this analysis, there are three rework levels and five performance measures; therefore there are fifteen separate groups a strategy may appear in. Consequently, for a strategy to be considered, it must appear in the top group of at least four of the 15 performance measures groups. Based upon this criterion, the strategies that are considered robust are RWK/FBN, FIFO/FBN, RWK/RV, FIFO/RV, RWK/WAIT, and FIFO/WAIT in both the MTO and MTS fabs.

ANOVA tests are done on this top group of strategies for each performance measure in each fab type. From the analysis of these top groups, in the MTO fab the dispatching rule and rework strategy are significant independently, but their interaction is not significant for any of the performance measures. These ANOVA tables can be seen in Appendix H. This signifies that, regardless of rework level, the dispatching rule and rework strategy chosen is important, but there is not a significant interaction between them. Tukey tests are then done for both

dispatching rule and rework strategy on every performance measure. The results from these tests show that RWK dispatching rule is significantly better than the FIFO rule for all performance measures. Also, for every performance measure, the FBN rework strategy is significantly better than the WAIT strategy, which is significantly better than the RV strategy. These Tukey test results can also be seen in Appendix H.

The results from the MTS fab are very similar, with only a few small differences. The ANOVA analysis shows that the combination of a dispatching rule and rework strategy is not significant in all of the performance measures except percentage on time (see Appendix I for ANOVA tables). Also, the dispatching rule and rework strategy are independently significant for all performance measures. Once again, the Tukey tests, which can be seen in Appendix I, reveal that the RWK dispatching rule is significantly better than FIFO for all performance measures. Furthermore, the FBN rework strategy is significantly better than the WAIT and RV strategies, and WAIT is significantly better than RV for all performance measures except for standard deviation of cycle time. For this performance measure, there is no significant difference between the WAIT and RV strategies.

These results are very interesting as with any amount of rework and in either fab type, the RWK dispatching rule and the FBN rework strategy are superior to the others tested. This concludes that in general, using the RWK/FBN strategy in either fab type with any rework level will be a very good solution.

### 5.4.2 Two Factor Analysis to Determine Robust Strategy Overall

From the previous section, it is determined that the RWK/FBN strategy is good to use in both fabs independent of the rework level. Now, the factor fab type will be included in the

ANOVA analysis as another blocking level so that the generalization can be further made that a strategy is robust across rework levels and fab types. The same criterion is used to determine strategies to be analyzed, that is, the strategy must appear in the top group of at least twenty-five percent of the performance measures. In this analysis, there are five performance measures, three rework levels, and two fabs, for a total of thirty top groups. Therefore, a strategy must appear in at least eight of the thirty to be considered. Based upon this criterion, the strategies used for this analysis are the same as in the previous section, the RWK/FBN, FIFO/FBN, RWK/RV, FIFO/RV, RWK/WAIT, and FIFO/WAIT. Following the ANOVA analysis, for all factors that are considered significant, Tukey tests are done to determine which strategies are significantly different than the rest.

The ANOVA analysis reveals that for all of the performance measures, the dispatching rule and rework strategy are significant at a 95 percent confidence level (see Appendix J). The Tukey tests for the dispatching rules shows that the RWK rule is significantly better than FIFO for all performance measures. Also, the Tukey tests for the rework strategies conclude that the FBN strategy is superior to the WAIT and RV strategies for all performance measures. These tests also show that the WAIT strategy is superior to the RV strategy across all performance measures.

From the ANOVA analysis, the combination of dispatching rule and rework strategy is also found to be significant for percentage on time, average WIP, and average XT. For the percentage on time measure, the RWK/FBN and FIFO/FBN strategies are statistically superior to all of the others tested, but are not significantly different than each other. This is not the case with average WIP and average XT, as these two measures show that the RWK/FBN strategy is superior to all others.

The conclusion that can be drawn from these results are that, regardless of the rework level and fab type, the RWK dispatching rule and FBN rework strategy will give good results in terms of the performance measures studied. Also, for some of the performance measures, the interaction between the dispatching rule and rework strategy is significant, therefore using them together will improve the performance of the fab.

## 5.5 Summary

The results of this experiment show the best combinations of dispatching rule and rework strategy to use at different rework levels and in different fab types to optimize various performance measures. These results show the RWK/FBN and FIFO/FBN strategies to be superior at one and five percent rework, and the RWK/FBN rule to be superior at ten percent rework in both fab types for most performance measures.

Also, resulting from the analysis of the robust strategies, the RWK/FBN strategy is shown to be robust for regardless of the rework level and fab type. It is important to note that in most other research, a dispatching rule or rework strategy has been shown to be superior in one or two performance measures, but perform poorly in others. The results of this study show that the top strategies are superior for most, if not all, of the performance measures studied.

This research used the FIFO/WAIT strategy as a baseline, as it is easy to implement and is benchmarked in most previous research. Therefore, it is useful to quantify the amount of improvement that the RWK/FBN strategy achieves over the FIFO/WAIT strategy to understand the impact that this strategy can have in a fab. These improvements can be seen in Table 5.14. The values in boldface are statistically significant at a 95 percent confidence level.

Table 5.14. Improvement of RWK/FBN over FIFO/WAIT strategies

| Fab | Rework | Average CT (hrs.) | Std. Dev. CT (hrs.) | Percent On Time | Average WIP (lots) | Average Xtheor |
|---|---|---|---|---|---|---|
| MTO | 1% | **2.55** | 0.07 | 1.77 | **1.42** | **0.01** |
| | 5% | **7.91** | 0.70 | **4.00** | **4.40** | **0.03** |
| | 10% | **15.20** | 2.25 | 6.92 | **8.46** | **0.05** |
| MTS | 1% | **2.85** | 0.57 | **1.49** | **0.96** | 0.01 |
| | 5% | **11.08** | 2.63 | **5.17** | **3.72** | **0.04** |
| | 10% | **21.42** | 5.11 | **9.36** | **7.19** | **0.07** |

The FBN rework strategy created in this research shows superior performance in both fab types and at all rework levels. This strategy capitalizes on the under-utilized stations following rework possibilities by allowing the mother and child lot to travel through these stations separately. Another important aspect of the FBN strategy is that is would be fairly easily to implement, even in a complex fab setting. This strategy is simply an extension of the wait strategy, with the mother lot going through some number of processing steps before it waits to be joined with the child lot. This strategy also keeps the reworked wafers with their original lot, making lot tracing simple. These things make the FBN strategy attractive from a management perspective.

# 6. CONCLUSIONS & RECOMMENDATIONS FOR FUTURE RESEARCH

## 6.1 Conclusions

The semiconductor industry is extremely competitive. Based on the nature of the industry, small improvements in performance can have a large financial impact. Rework is present in modern day fabs and is inherently harmful to the performance and thus the profitability of fabs. However, previous research in the semiconductor field is found to be rather inconclusive on the importance of including rework in research studies. Initially, this research determines if the presence of rework significantly effects fab performance.

An experiment is conducted which concludes that the presence of rework does have a significant effect on key fab performance measures such as average cycle time and average WIP. Therefore, including rework in semiconductor research is necessary, and investigating methods to lessen the detrimental effect that rework has in fabs should be explored.

Two operational decisions made in fabs that literature has shown to effect fab performance are dispatching rules and rework strategies. This experiment focuses on the interaction between existing dispatching rules and rework strategies, and how they effect key performance measures at different rework levels and in different fab types.

The results show the RWK/FBN and FIFO/FBN strategies to be superior at one and five percent rework, and the RWK/FBN rule to be superior at ten percent rework in both fab types. Also, the RWK/FBN strategy is shown to be robust for regardless of the rework level and fab type. The FBN rework strategy, which is developed in this study, is shown to be superior to the others proposed in previous literature. Furthermore, most other research has shown a dispatching rule or rework strategy to be superior in one or two performance measures, but perform poorly in others. These results show that the top strategies are superior for most, if not

all, of the performance measures studied. The RWK/FBN strategy shows significant improvements in performance measures including average cycle time, percentage on time, and average WIP over the FIFO/WAIT strategy. Such improvement can have large economic implications for semiconductor fabs.

## 6.2 Recommendations for Future Research

Resulting from this study is the opportunity for further research based upon findings and conclusions from this work. Such ideas include running more replications to determine if there is a statistically significant difference between the top two strategies. Also, with the FBN rework strategy, other methods of determining the first bottleneck after the possibility for rework can be explored. Furthermore, more complex dispatching rules can be tested in combination with the FBN rework strategy in an attempt to further improve fab performance. Also, in this research, when the RWK dispatching rule is used, if there is no rework in queue, the secondary dispatching rule is FIFO. Perhaps a different secondary dispatching rule could be used to improve the performance measures. Lastly, further validation of the FBN strategy in other simulation models can give the strategy further credibility in industry.

### 6.2.1 Discrimination between Top Strategies

This research has shown that the RWK/FBN strategy is robust and gives the best statistical results for most of the performance measures in both fabs. However, some of these results are not statistically significant from the top group of strategies. These results are based on ten replications for each experiment and at a confidence level of 95 percent.

Running additional replications for these top strategies can be done to get a better estimation of the true values of the performance measures and to make the sample standard deviation smaller. This will allow the confidence intervals generated by the Tukey test to be smaller and therefore the test will discriminate between the strategies to a further extent. Additional replications of each of these strategies can be run at all of the rework levels to determine if there are statistically significant differences between the top strategies.

### 6.2.2 New Methods for Determining First Bottleneck

The current method for determining what is the first bottleneck station after a rework step has passed is discussed in Chapter 5.1. Currently, a station with above 85 percent station utilization is determined to be a bottleneck. Experimenting with this utilization cutoff could help to see further increases in fab performance measures. There are also other measures that can be looked at to determine the first bottleneck, such as average or maximum queue size. The impact of setup times on bottleneck stations is ignored in this research and can also be investigated.

### 6.2.3 Alternative Dispatching Rules

The dispatching rules tested in this study, FIFO, SPT, EDD, RWK, and CR are very common and widely understood rules. Much literature has attempted to derive new, more complex dispatching rules, many of which are based upon these and other commonly used rules. This study focused on these simple rules in an attempt to begin to understand how dispatching rules and rework strategies can independently and interactively impact fab performance.

The RWK dispatching rule is found to be the best of the five tested in this study. When the RWK dispatching rule is used, if there is no rework in the queue, the secondary dispatching

rule used is FIFO. Perhaps a different secondary dispatching rule could be specified that would positively effect the overall performance of the fab. Also, stations could have different dispatching rules depending on how they effect the performance of a fab. For instance, stations that are under utilized may benefit from such rules as CR or EDD, as lots with large processing times or large due dates are not likely to get stuck in queue there. Similarly, stations with high utilizations may benefit from rules such as FIFO to ensure that one lot does not get stuck in the queue for a large amount of time. Determining the number of times that the queuing order changes at each station as a result of the chosen dispatching rule could also be beneficial in choosing different rules for different stations. There are also various other dispatching rules proposed in literature that could be attempted in combination with the FBN rework strategy.

### 6.2.4 First Bottleneck Validation

In this study, the FBN rework strategy is developed and proven to be better than the previously studied strategies. Now, it should be simulated in other fab models to further validate these findings. If other studies can prove this strategy to be superior and significantly impact fab performance, the implementation of this strategy in a full-scale production fab would give it further credibility in industry.

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# APPENDECIES

The following Appendices contain raw data and statistical analysis from this research. Each appendix has an explanation of what it contains, and all tables and figures are labeled accordingly.

## Appendix A. Results of Rework Strategy

This Appendix shows the results from test done to determine if rework makes a significant difference in fab performance.

Table A.1. Results from the Fab Without Rework

| | No Rework Fab | | |
|---|---|---|---|
| Rep. | Avg. CT (hrs.) | St. Dev. CT (hrs.) | Avg. WIP (lots) |
| 1 | 323.323 | 78.546 | 179.870 |
| 2 | 323.326 | 78.492 | 179.870 |
| 3 | 324.188 | 78.718 | 180.360 |
| 4 | 324.913 | 79.002 | 180.750 |
| 5 | 322.917 | 78.355 | 179.640 |
| 6 | 324.086 | 78.917 | 180.290 |
| 7 | 323.873 | 78.717 | 180.170 |
| 8 | 324.191 | 78.867 | 180.360 |
| 9 | 323.470 | 78.722 | 179.950 |
| 10 | 324.281 | 78.875 | 180.400 |
| **Avg.** | **323.857** | **78.721** | **180.166** |

Table A.2. Results from the Fab With Rework

| | Rework Fab | | |
|---|---|---|---|
| Rep. | Avg. CT (hrs.) | St. Dev. CT (hrs.) | Avg. WIP (lots) |
| 1 | 339.312 | 83.153 | 188.760 |
| 2 | 339.683 | 83.200 | 188.970 |
| 3 | 340.372 | 83.214 | 189.350 |
| 4 | 340.742 | 83.273 | 189.550 |
| 5 | 339.421 | 83.069 | 188.830 |
| 6 | 339.905 | 83.263 | 189.090 |
| 7 | 340.045 | 83.301 | 189.170 |
| 8 | 340.064 | 83.299 | 189.180 |
| 9 | 339.883 | 83.227 | 189.090 |
| 10 | 340.439 | 83.381 | 189.380 |
| **Avg.** | **339.987** | **83.238** | **189.137** |

## Appendix B. Experimental Data

This appendix contains the raw data from the MTO and MTS fabs. All data shown is an average of ten replications.

Table B.1. MTO Fab Raw Data

| | DR | RS | Average CT (hrs.) | Std. Dev. CT (hrs.) | Percent On Time | Percent Idle | Average WIP (lots) | Average XTheor |
|---|---|---|---|---|---|---|---|---|
| | FIFO | WAIT | 328.12 | 79.65 | 92.45 | 59.24 | 182.53 | 1.45 |
| | FIFO | RV | 326.83 | 79.87 | 93.10 | 59.09 | 181.82 | 1.44 |
| | FIFO | FBN | 325.65 | 79.60 | 94.14 | 58.73 | 181.16 | 1.44 |
| | SPT | WAIT | 351.03 | 99.73 | 56.34 | 59.47 | 195.29 | 1.54 |
| | SPT | RV | 350.30 | 101.10 | 58.14 | 59.31 | 194.88 | 1.53 |
| | SPT | FBN | 348.61 | 99.86 | 59.73 | 58.96 | 193.95 | 1.53 |
| | EDD | WAIT | 337.77 | 102.39 | 72.96 | 59.35 | 187.90 | 1.47 |
| 1% | EDD | RV | 338.19 | 104.30 | 71.17 | 59.21 | 188.14 | 1.47 |
| | EDD | FBN | 335.96 | 102.75 | 74.39 | 58.84 | 186.90 | 1.46 |
| | CR | WAIT | 331.30 | 77.78 | 94.84 | 59.21 | 184.30 | 1.47 |
| | CR | RV | 335.32 | 80.19 | 88.72 | 59.09 | 186.54 | 1.48 |
| | CR | FBN | 330.18 | 77.85 | 95.56 | 58.71 | 183.68 | 1.46 |
| | RWK | WAIT | 327.83 | 79.59 | 92.75 | 59.23 | 182.37 | 1.45 |
| | RWK | RV | 326.84 | 79.92 | 93.12 | 59.08 | 181.82 | 1.44 |
| | RWK | FBN | 325.56 | 79.58 | 94.21 | 58.73 | 181.11 | 1.44 |
| | FIFO | WAIT | 338.51 | 82.21 | 92.43 | 58.16 | 188.31 | 1.50 |
| | FIFO | RV | 336.73 | 83.46 | 92.31 | 57.76 | 187.32 | 1.49 |
| | FIFO | FBN | 330.86 | 81.61 | 96.38 | 56.81 | 184.06 | 1.47 |
| | SPT | WAIT | 362.44 | 102.66 | 55.27 | 58.41 | 201.63 | 1.59 |
| | SPT | RV | 369.11 | 115.05 | 52.32 | 58.01 | 205.34 | 1.61 |
| | SPT | FBN | 355.57 | 103.62 | 63.81 | 57.05 | 197.81 | 1.56 |
| | EDD | WAIT | 348.92 | 106.48 | 71.57 | 58.27 | 194.11 | 1.52 |
| 5% | EDD | RV | 355.19 | 114.18 | 60.18 | 57.91 | 197.60 | 1.53 |
| | EDD | FBN | 342.76 | 106.49 | 76.89 | 56.93 | 190.68 | 1.50 |
| | CR | WAIT | 346.69 | 82.82 | 88.30 | 58.16 | 192.87 | 1.54 |
| | CR | RV | 426.61 | 116.33 | 0.68 | 58.10 | 237.33 | 1.87 |
| | CR | FBN | 346.11 | 84.41 | 89.20 | 56.83 | 192.55 | 1.54 |
| | RWK | WAIT | 337.32 | 81.94 | 93.13 | 58.16 | 187.65 | 1.49 |
| | RWK | RV | 335.95 | 83.32 | 92.75 | 57.76 | 186.90 | 1.48 |
| | RWK | FBN | 330.60 | 81.51 | 96.43 | 56.81 | 183.91 | 1.47 |
| | FIFO | WAIT | 359.45 | 87.86 | 91.09 | 57.29 | 199.96 | 1.59 |
| | FIFO | RV | 370.15 | 94.20 | 73.18 | 56.75 | 205.92 | 1.63 |
| | FIFO | FBN | 347.66 | 86.50 | 97.06 | 55.45 | 193.41 | 1.55 |
| | SPT | WAIT | 386.31 | 117.15 | 57.39 | 57.53 | 214.91 | 1.69 |
| | SPT | RV | 425.00 | 169.72 | 43.59 | 57.01 | 236.47 | 1.83 |
| | SPT | FBN | 380.43 | 118.12 | 61.90 | 55.69 | 211.64 | 1.68 |
| | EDD | WAIT | 372.28 | 118.32 | 65.24 | 57.41 | 207.11 | 1.61 |
| 10% | EDD | RV | 391.89 | 130.01 | 38.74 | 56.91 | 218.02 | 1.69 |
| | EDD | FBN | 363.74 | 116.60 | 73.86 | 55.56 | 202.35 | 1.59 |
| | CR | WAIT | 400.35 | 104.22 | 9.76 | 57.40 | 222.72 | 1.76 |
| | CR | RV | 490.73 | 139.39 | 0.31 | 57.08 | 273.00 | 2.15 |
| | CR | FBN | 406.22 | 106.53 | 4.44 | 55.63 | 225.98 | 1.81 |
| | RWK | WAIT | 353.47 | 86.23 | 95.36 | 57.28 | 196.64 | 1.56 |
| | RWK | RV | 362.93 | 92.18 | 82.41 | 56.73 | 201.90 | 1.60 |
| | RWK | FBN | 344.25 | 85.61 | 98.01 | 55.43 | 191.51 | 1.54 |

Table B.2. MTS Fab Raw Data

| | DR | RS | Average CT (hrs.) | Std. Dev. CT (hrs.) | Percent On Time | Percent Idle | Average WIP (lots) | Average XTheor |
|---|---|---|---|---|---|---|---|---|
| | FIFO | WAIT | 373.34 | 41.61 | 91.69 | 71.41 | 125.32 | 1.46 |
| | FIFO | RV | 372.34 | 41.25 | 91.98 | 71.31 | 124.98 | 1.46 |
| | FIFO | FBN | 370.64 | 41.14 | 93.24 | 71.08 | 124.41 | 1.45 |
| | SPT | WAIT | 392.63 | 55.12 | 61.45 | 71.55 | 131.80 | 1.53 |
| | SPT | RV | 393.29 | 57.15 | 60.90 | 71.45 | 132.02 | 1.54 |
| | SPT | FBN | 390.34 | 55.07 | 64.57 | 71.23 | 131.03 | 1.53 |
| | EDD | WAIT | 380.74 | 59.86 | 76.62 | 71.47 | 127.80 | 1.48 |
| 1% | EDD | RV | 379.46 | 59.83 | 77.56 | 71.38 | 127.37 | 1.48 |
| | EDD | FBN | 377.90 | 59.27 | 79.20 | 71.15 | 126.85 | 1.47 |
| | CR | WAIT | 376.29 | 43.56 | 95.31 | 71.39 | 126.31 | 1.47 |
| | CR | RV | 380.53 | 43.96 | 88.93 | 71.30 | 127.74 | 1.49 |
| | CR | FBN | 374.39 | 42.60 | 96.26 | 71.07 | 125.67 | 1.47 |
| | RWK | WAIT | 373.13 | 41.75 | 91.83 | 71.41 | 125.25 | 1.46 |
| | RWK | RV | 372.16 | 41.29 | 92.34 | 71.31 | 124.93 | 1.46 |
| | RWK | FBN | 370.49 | 41.05 | 93.18 | 71.09 | 124.36 | 1.45 |
| | FIFO | WAIT | 388.31 | 44.78 | 91.24 | 70.67 | 130.34 | 1.52 |
| | FIFO | RV | 386.14 | 43.25 | 91.69 | 70.40 | 129.62 | 1.51 |
| | FIFO | FBN | 378.51 | 42.25 | 95.92 | 69.78 | 127.05 | 1.49 |
| | SPT | WAIT | 407.47 | 60.02 | 62.06 | 70.82 | 136.77 | 1.59 |
| | SPT | RV | 413.15 | 65.82 | 56.71 | 70.55 | 138.68 | 1.61 |
| | SPT | FBN | 399.22 | 58.31 | 71.27 | 69.93 | 134.01 | 1.57 |
| | EDD | WAIT | 396.65 | 64.47 | 74.59 | 70.73 | 133.14 | 1.54 |
| 5% | EDD | RV | 394.71 | 65.04 | 75.78 | 70.47 | 132.49 | 1.54 |
| | EDD | FBN | 388.58 | 62.92 | 81.96 | 69.86 | 130.43 | 1.52 |
| | CR | WAIT | 402.67 | 53.11 | 75.32 | 70.66 | 135.16 | 1.57 |
| | CR | RV | 448.52 | 60.57 | 6.93 | 70.57 | 150.55 | 1.75 |
| | CR | FBN | 391.11 | 47.58 | 94.28 | 69.78 | 131.28 | 1.54 |
| | RWK | WAIT | 385.70 | 44.16 | 93.07 | 70.67 | 129.47 | 1.51 |
| | RWK | RV | 384.08 | 43.03 | 92.95 | 70.40 | 128.93 | 1.51 |
| | RWK | FBN | 377.23 | 42.15 | 96.42 | 69.78 | 126.63 | 1.48 |
| | FIFO | WAIT | 422.43 | 51.02 | 88.51 | 70.07 | 141.80 | 1.65 |
| | FIFO | RV | 434.78 | 51.46 | 68.87 | 69.68 | 145.94 | 1.70 |
| | FIFO | FBN | 407.09 | 46.86 | 96.28 | 68.86 | 136.65 | 1.61 |
| | SPT | WAIT | 440.04 | 83.52 | 67.17 | 70.22 | 147.71 | 1.72 |
| | SPT | RV | 475.83 | 124.95 | 48.73 | 69.86 | 159.72 | 1.86 |
| | SPT | FBN | 432.67 | 87.24 | 72.28 | 69.03 | 145.23 | 1.70 |
| | EDD | WAIT | 432.63 | 73.29 | 70.64 | 70.14 | 145.22 | 1.68 |
| 10% | EDD | RV | 440.40 | 74.55 | 63.17 | 69.77 | 147.83 | 1.72 |
| | EDD | FBN | 421.47 | 70.82 | 80.48 | 68.94 | 141.47 | 1.65 |
| | CR | WAIT | 474.16 | 74.89 | 10.48 | 70.15 | 159.16 | 1.85 |
| | CR | RV | 583.73 | 82.24 | 0.00 | 69.89 | 195.94 | 2.28 |
| | CR | FBN | 459.79 | 69.45 | 27.71 | 68.93 | 154.34 | 1.81 |
| | RWK | WAIT | 413.10 | 48.97 | 94.96 | 70.06 | 138.67 | 1.62 |
| | RWK | RV | 423.68 | 49.18 | 83.76 | 69.68 | 142.22 | 1.66 |
| | RWK | FBN | 401.01 | 45.90 | 97.87 | 68.85 | 134.61 | 1.59 |

## Appendix C. Four Factor ANOVA Results

This Appendix contains the ANOVA results for all performance measures when all four experimental factors were included. These results show which factors and interactions of factors are significant.

Table C.1. ANOVA Table for Average Cycle Time

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| Fab | 1 | 559924.000 | 559924.000 | 559924.000 | 40000.000 | 0.000 |
| DR | 4 | 230462.000 | 230462.000 | 57615.000 | 4077.990 | 0.000 |
| RS | 2 | 79710.000 | 79710.000 | 39855.000 | 2820.920 | 0.000 |
| RL | 2 | 520896.000 | 520896.000 | 260448.000 | 18000.000 | 0.000 |
| Fab*DR | 4 | 1628.000 | 1628.000 | 407.000 | 28.800 | 0.000 |
| Fab*RS | 2 | 464.000 | 464.000 | 232.000 | 16.410 | 0.000 |
| Fab*RL | 2 | 12813.000 | 12813.000 | 6406.000 | 453.440 | 0.000 |
| DR*RS | 8 | 77275.000 | 77275.000 | 9659.000 | 683.680 | 0.000 |
| DR*RL | 8 | 130628.000 | 130628.000 | 16328.000 | 1155.720 | 0.000 |
| RS*RL | 4 | 48641.000 | 48641.000 | 12160.000 | 860.700 | 0.000 |
| Fab*DR*RS | 8 | 911.000 | 911.000 | 114.000 | 8.060 | 0.000 |
| Fab*DR*RL | 8 | 3124.000 | 3124.000 | 391.000 | 27.640 | 0.000 |
| Fab*RS*RL | 4 | 1329.000 | 1329.000 | 332.000 | 23.510 | 0.000 |
| DR*RS*RL | 16 | 35314.000 | 35314.000 | 2207.000 | 156.220 | 0.000 |
| Fab*DR*RS*RL | 16 | 4959.000 | 4959.000 | 310.000 | 21.940 | 0.000 |
| Error | 810 | 11444.000 | 11444.000 | 14.000 | | |
| Total | 899 | 1719521.000 | | | | |

Table C.2. ANOVA Table for Standard Deviation of Cycle Time

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| Fab | 1 | 378871.400 | 378871.400 | 378871.400 | 19000.000 | 0.000 |
| DR | 4 | 129897.400 | 129897.400 | 32474.400 | 1611.370 | 0.000 |
| RS | 2 | 14065.600 | 14065.600 | 7032.800 | 348.970 | 0.000 |
| RL | 2 | 72535.800 | 72535.800 | 36267.900 | 1799.610 | 0.000 |
| Fab*DR | 4 | 1562.500 | 1562.500 | 390.600 | 19.380 | 0.000 |
| Fab*RS | 2 | 2197.900 | 2197.900 | 1099.000 | 54.530 | 0.000 |
| Fab*RL | 2 | 143.900 | 143.900 | 71.900 | 3.570 | 0.029 |
| DR*RS | 8 | 10520.700 | 10520.700 | 1315.100 | 65.250 | 0.000 |
| DR*RL | 8 | 29621.400 | 29621.400 | 3702.700 | 183.730 | 0.000 |
| RS*RL | 4 | 8603.400 | 8603.400 | 2150.800 | 106.720 | 0.000 |
| Fab*DR*RS | 8 | 1391.900 | 1391.900 | 174.000 | 8.630 | 0.000 |
| Fab*DR*RL | 8 | 1207.600 | 1207.600 | 150.900 | 7.490 | 0.000 |
| Fab*RS*RL | 4 | 984.800 | 984.800 | 246.200 | 12.220 | 0.000 |
| DR*RS*RL | 16 | 10551.000 | 10551.000 | 659.400 | 32.720 | 0.000 |
| Fab*DR*RS*RL | 16 | 661.300 | 661.300 | 41.300 | 2.050 | 0.009 |
| Error | 810 | 16324.100 | 16324.100 | 20.200 | | |
| Total | 899 | 679140.700 | | | | |

Table C.3. ANOVA Table for Percent On Time

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| Fab | 1 | 2194.000 | 2194.000 | 2194.000 | 181.800 | 0.000 |
| DR | 4 | 227271.700 | 227271.700 | 56817.900 | 4707.980 | 0.000 |
| RS | 2 | 39740.800 | 39740.800 | 19870.400 | 1646.480 | 0.000 |
| RL | 2 | 67319.000 | 67319.000 | 33659.500 | 2789.050 | 0.000 |
| Fab*DR | 4 | 3109.400 | 3109.400 | 777.300 | 64.410 | 0.000 |
| Fab*RS | 2 | 479.000 | 479.000 | 239.500 | 19.840 | 0.000 |
| Fab*RL | 2 | 541.200 | 541.200 | 270.600 | 22.420 | 0.000 |
| DR*RS | 8 | 22308.500 | 22308.500 | 2788.600 | 231.060 | 0.000 |
| DR*RL | 8 | 155159.700 | 155159.700 | 19395.000 | 1607.080 | 0.000 |
| RS*RL | 4 | 14271.800 | 14271.800 | 3567.900 | 295.640 | 0.000 |
| Fab*DR*RS | 8 | 2210.400 | 2210.400 | 276.300 | 22.890 | 0.000 |
| Fab*DR*RL | 8 | 663.000 | 663.000 | 82.900 | 6.870 | 0.000 |
| Fab*RS*RL | 4 | 355.800 | 355.800 | 89.000 | 7.370 | 0.000 |
| DR*RS*RL | 16 | 44775.000 | 44775.000 | 2798.400 | 231.880 | 0.000 |
| Fab*DR*RS*RL | 16 | 1671.500 | 1671.500 | 104.500 | 8.660 | 0.000 |
| Error | 810 | 9775.400 | 9775.400 | 12.100 | | |
| Total | 899 | 591846.300 | | | | |

Table C.4. ANOVA Table for Percent Idle

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| Fab | 1 | 35882.710 | 35882.710 | 35882.710 | 60000000.000 | 0.000 |
| DR | 4 | 4.940 | 4.940 | 1.240 | 2064.310 | 0.000 |
| RS | 2 | 165.910 | 165.910 | 82.950 | 140000.000 | 0.000 |
| RL | 2 | 656.600 | 656.600 | 328.300 | 550000.000 | 0.000 |
| Fab*DR | 4 | 0.260 | 0.260 | 0.070 | 108.790 | 0.000 |
| Fab*RS | 2 | 7.510 | 7.510 | 3.750 | 6271.650 | 0.000 |
| Fab*RL | 2 | 22.740 | 22.740 | 11.370 | 19000.000 | 0.000 |
| DR*RS | 8 | 0.610 | 0.610 | 0.080 | 127.680 | 0.000 |
| DR*RL | 8 | 0.710 | 0.710 | 0.090 | 148.390 | 0.000 |
| RS*RL | 4 | 33.600 | 33.600 | 8.400 | 14000.000 | 0.000 |
| Fab*DR*RS | 8 | 0.050 | 0.050 | 0.010 | 10.960 | 0.000 |
| Fab*DR*RL | 8 | 0.050 | 0.050 | 0.010 | 10.060 | 0.000 |
| Fab*RS*RL | 4 | 1.380 | 1.380 | 0.350 | 577.780 | 0.000 |
| DR*RS*RL | 16 | 0.280 | 0.280 | 0.020 | 29.470 | 0.000 |
| Fab*DR*RS*RL | 16 | 0.030 | 0.030 | 0.000 | 3.550 | 0.000 |
| Error | 810 | 0.480 | 0.480 | 0.000 | | |
| Total | 899 | 36777.880 | | | | |

Table C.5. ANOVA Table for Average WIP

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| Fab | 1 | 861845.000 | 861845.000 | 861845.000 | 310000.000 | 0.000 |
| DR | 4 | 45900.000 | 45900.000 | 11475.000 | 4114.450 | 0.000 |
| RS | 2 | 15848.000 | 15848.000 | 7924.000 | 2841.300 | 0.000 |
| RL | 2 | 95928.000 | 95928.000 | 47964.000 | 17000.000 | 0.000 |
| Fab*DR | 4 | 3159.000 | 3159.000 | 790.000 | 283.210 | 0.000 |
| Fab*RS | 2 | 1044.000 | 1044.000 | 522.000 | 187.130 | 0.000 |
| Fab*RL | 2 | 1039.000 | 1039.000 | 520.000 | 186.290 | 0.000 |
| DR*RS | 8 | 15306.000 | 15306.000 | 1913.000 | 686.010 | 0.000 |
| DR*RL | 8 | 24645.000 | 24645.000 | 3081.000 | 1104.600 | 0.000 |
| RS*RL | 4 | 9328.000 | 9328.000 | 2332.000 | 836.130 | 0.000 |
| Fab*DR*RS | 8 | 1046.000 | 1046.000 | 131.000 | 46.860 | 0.000 |
| Fab*DR*RL | 8 | 836.000 | 836.000 | 105.000 | 37.470 | 0.000 |
| Fab*RS*RL | 4 | 486.000 | 486.000 | 122.000 | 43.590 | 0.000 |
| DR*RS*RL | 16 | 6808.000 | 6808.000 | 425.000 | 152.560 | 0.000 |
| Fab*DR*RS*RL | 16 | 1139.000 | 1139.000 | 71.000 | 25.530 | 0.000 |
| Error | 810 | 2259.000 | 2259.000 | 3.000 | | |
| Total | 899 | 1086616.000 | | | | |

Table C.6. ANOVA Table for Average XT

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| Fab | 1 | 0.130 | 0.130 | 0.130 | 557.490 | 0.000 |
| DR | 4 | 3.828 | 3.828 | 0.957 | 4116.500 | 0.000 |
| RS | 2 | 1.130 | 1.130 | 0.565 | 2430.290 | 0.000 |
| RL | 2 | 8.873 | 8.873 | 4.436 | 19000.000 | 0.000 |
| Fab*DR | 4 | 0.015 | 0.015 | 0.004 | 15.660 | 0.000 |
| Fab*RS | 2 | 0.006 | 0.006 | 0.003 | 12.080 | 0.000 |
| Fab*RL | 2 | 0.108 | 0.108 | 0.054 | 232.750 | 0.000 |
| DR*RS | 8 | 1.294 | 1.294 | 0.162 | 695.750 | 0.000 |
| DR*RL | 8 | 2.136 | 2.136 | 0.267 | 1148.790 | 0.000 |
| RS*RL | 4 | 0.727 | 0.727 | 0.182 | 781.340 | 0.000 |
| Fab*DR*RS | 8 | 0.014 | 0.014 | 0.002 | 7.740 | 0.000 |
| Fab*DR*RL | 8 | 0.031 | 0.031 | 0.004 | 16.470 | 0.000 |
| Fab*RS*RL | 4 | 0.019 | 0.019 | 0.005 | 20.040 | 0.000 |
| DR*RS*RL | 16 | 0.586 | 0.586 | 0.037 | 157.440 | 0.000 |
| Fab*DR*RS*RL | 16 | 0.076 | 0.076 | 0.005 | 20.450 | 0.000 |
| Error | 810 | 0.188 | 0.188 | 0.000 | | |
| Total | 899 | 19.159 | | | | |

## Appendix D. MTO Three Factor ANOVA Tables

This appendix contains the ANOVA results from the make-to-order fab. These tests used the dispatching rule, rework strategy, and rework level as the factors.

Table D.1. ANOVA Table of Average Cycle Time

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 116321.000 | 116321.000 | 29080.000 | 2272.350 | 0.000 |
| RS | 2 | 39885.000 | 39885.000 | 19942.000 | 1558.320 | 0.000 |
| RL | 2 | 187088.000 | 187088.000 | 93544.000 | 7309.600 | 0.000 |
| DR*RS | 8 | 38317.000 | 38317.000 | 4790.000 | 374.260 | 0.000 |
| DR*RL | 8 | 52895.000 | 52895.000 | 6612.000 | 516.660 | 0.000 |
| RS*RL | 4 | 21219.000 | 21219.000 | 5305.000 | 414.510 | 0.000 |
| DR*RS*RL | 16 | 17308.000 | 17308.000 | 1082.000 | 84.530 | 0.000 |
| Error | 405 | 5183.000 | 5183.000 | 13.000 | | |
| **Total** | **449** | **478215.000** | | | | |

Table D.2. ANOVA Table of Standard Deviation of Cycle Time

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 76724.400 | 76724.400 | 19181.100 | 818.620 | 0.000 |
| RS | 2 | 13362.500 | 13362.500 | 6681.200 | 285.150 | 0.000 |
| RL | 2 | 37693.000 | 37693.000 | 18846.500 | 804.340 | 0.000 |
| DR*RS | 8 | 8165.600 | 8165.600 | 1020.700 | 43.560 | 0.000 |
| DR*RL | 8 | 12607.500 | 12607.500 | 1575.900 | 67.260 | 0.000 |
| RS*RL | 4 | 7496.500 | 7496.500 | 1874.100 | 79.990 | 0.000 |
| DR*RS*RL | 16 | 7074.500 | 7074.500 | 442.200 | 18.870 | 0.000 |
| Error | 405 | 9489.500 | 9489.500 | 23.400 | | |
| **Total** | **449** | **172613.500** | | | | |

Table D.3. ANOVA Table of Percentage On Time

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 132043.000 | 132043.000 | 33010.700 | 3412.670 | 0.000 |
| RS | 2 | 20660.000 | 20660.000 | 10330.000 | 1067.920 | 0.000 |
| RL | 2 | 39955.300 | 39955.300 | 19977.700 | 2065.300 | 0.000 |
| DR*RS | 8 | 11332.900 | 11332.900 | 1416.600 | 146.450 | 0.000 |
| DR*RL | 8 | 83048.200 | 83048.200 | 10381.000 | 1073.200 | 0.000 |
| RS*RL | 4 | 7971.100 | 7971.100 | 1992.800 | 206.020 | 0.000 |
| DR*RS*RL | 16 | 27972.700 | 27972.700 | 1748.300 | 180.740 | 0.000 |
| Error | 405 | 3917.600 | 3917.600 | 9.700 | | |
| **Total** | **449** | **326900.800** | | | | |

Table D.4. ANOVA Table of Percent Idle

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 3.715 | 3.715 | 0.929 | 1240.680 | 0.000 |
| RS | 2 | 121.942 | 121.942 | 60.971 | 81000.000 | 0.000 |
| RL | 2 | 461.849 | 461.849 | 230.925 | 310000.000 | 0.000 |
| DR*RS | 8 | 0.497 | 0.497 | 0.062 | 82.900 | 0.000 |
| DR*RL | 8 | 0.555 | 0.555 | 0.069 | 92.600 | 0.000 |
| RS*RL | 4 | 24.286 | 24.286 | 6.072 | 8110.150 | 0.000 |
| DR*RS*RL | 16 | 0.241 | 0.241 | 0.015 | 20.130 | 0.000 |
| Error | 405 | 0.303 | 0.303 | 0.001 | | |
| Total | 449 | 613.388 | | | | |

Table D.5. ANOVA Table of Average WIP

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 36013.700 | 36013.700 | 9003.400 | 2355.480 | 0.000 |
| RS | 2 | 12351.500 | 12351.500 | 6175.800 | 1615.710 | 0.000 |
| RL | 2 | 57908.500 | 57908.500 | 28954.300 | 7575.030 | 0.000 |
| DR*RS | 8 | 11859.900 | 11859.900 | 1482.500 | 387.850 | 0.000 |
| DR*RL | 8 | 16370.300 | 16370.300 | 2046.300 | 535.350 | 0.000 |
| RS*RL | 4 | 6573.800 | 6573.800 | 1643.500 | 429.960 | 0.000 |
| DR*RS*RL | 16 | 5359.200 | 5359.200 | 335.000 | 87.630 | 0.000 |
| Error | 405 | 1548.000 | 1548.000 | 3.800 | | |
| Total | 449 | 147985.100 | | | | |

Table D.6. ANOVA Table of Average XT

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 2.120 | 2.120 | 0.530 | 2440.960 | 0.000 |
| RS | 2 | 0.592 | 0.592 | 0.296 | 1362.720 | 0.000 |
| RL | 2 | 3.562 | 3.562 | 1.781 | 8203.140 | 0.000 |
| DR*RS | 8 | 0.698 | 0.698 | 0.087 | 402.040 | 0.000 |
| DR*RL | 8 | 0.960 | 0.960 | 0.120 | 552.880 | 0.000 |
| RS*RL | 4 | 0.333 | 0.333 | 0.083 | 383.790 | 0.000 |
| DR*RS*RL | 16 | 0.310 | 0.310 | 0.019 | 89.320 | 0.000 |
| Error | 405 | 0.088 | 0.088 | 0.000 | | |
| Total | 449 | 8.665 | | | | |

## Appendix E. MTO Two Factor ANOVA and Tukey Pairwise Comparison Results

This Appendix shows the ANOVA and Tukey pairwise comparison tables for each of the performance measures at each rework level in the MTO fab. The ANOVA tests determine whether dispatching rules and rework strategies are significant independently, and also whether their interaction is significant. The pairwise comparisons are done for the dispatching rule and rework strategy independently and also for a combination of the two. These tests are done at a 95 percent confidence level. The vertical lines on the charts refer to rules or strategies that are statistically the same as the others that are connected by the same vertical line.

Table E.1. ANOVA and Tukey Tests for Average Cycle Time at One Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 4 | 11127.730 | 11127.730 | 2781.930 | 2093.760 | 0.000 |
| **RS** | 2 | 157.390 | 157.390 | 78.690 | 59.230 | 0.000 |
| **DR*RS** | 8 | 103.810 | 103.810 | 12.980 | 9.770 | 0.000 |
| **Error** | 135 | 179.370 | 179.370 | 1.330 | | |
| **Total** | **149** | **11568.310** | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 325.562 | |
| FIFO | FBN | 325.649 | |
| FIFO | RV | 326.826 | |
| RWK | RV | 326.838 | |
| RWK | WAIT | 327.826 | |
| FIFO | WAIT | 328.115 | |
| CR | FBN | 330.179 | |
| CR | WAIT | 331.295 | |
| CR | RV | 335.318 | |
| EDD | FBN | 335.957 | |
| EDD | WAIT | 337.769 | |
| EDD | RV | 338.190 | |
| SPT | FBN | 348.611 | |
| SPT | RV | 350.300 | |
| SPT | WAIT | 351.029 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 326.742 | |
| FIFO | 326.863 | |
| CR | 332.264 | |
| EDD | 337.305 | |
| SPT | 349.980 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 333.192 | |
| WAIT | 335.207 | |
| RV | 335.494 | |

Table E.2. ANOVA and Tukey Tests for St. Dev of Cycle Time at One Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 4 | 18135.400 | 18135.400 | 4533.800 | 7681.480 | 0.000 |
| **RS** | 2 | 48.000 | 48.000 | 24.000 | 40.700 | 0.000 |
| **DR*RS** | 8 | 22.700 | 22.700 | 2.800 | 4.810 | 0.000 |
| **Error** | 135 | 79.700 | 79.700 | 0.600 | | |
| **Total** | **149** | **18285.800** | | | | |

| DR | RS | St. Dev. CT | Significance |
|---|---|---|---|
| CR | WAIT | 77.783 | |
| CR | FBN | 77.849 | |
| RWK | FBN | 79.581 | |
| RWK | WAIT | 79.585 | |
| FIFO | FBN | 79.604 | |
| FIFO | WAIT | 79.648 | |
| FIFO | RV | 79.872 | |
| RWK | RV | 79.916 | |
| CR | RV | 80.189 | |
| SPT | WAIT | 99.727 | |
| SPT | FBN | 99.858 | |
| SPT | RV | 101.097 | |
| EDD | WAIT | 102.388 | |
| EDD | FBN | 102.751 | |
| EDD | RV | 104.301 | |

| DR | St. Dev. CT | Sig. |
|---|---|---|
| CR | 78.607 | |
| RWK | 79.694 | |
| FIFO | 79.708 | |
| SPT | 100.227 | |
| EDD | 103.147 | |

| RS | St. Dev. CT | Sig. |
|---|---|---|
| WAIT | 87.826 | |
| FBN | 87.929 | |
| RV | 89.075 | |

Table E.3. ANOVA and Tukey Tests for Percentage On Time at One Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 4 | 31004.300 | 31004.300 | 7751.100 | 1818.840 | 0.000 |
| **RS** | 2 | 193.900 | 193.900 | 97.000 | 22.750 | 0.000 |
| **DR*RS** | 8 | 223.900 | 223.900 | 28.000 | 6.570 | 0.000 |
| **Error** | 135 | 575.300 | 575.300 | 4.300 | | |
| **Total** | **149** | **31997.400** | | | | |

| DR | RS | % On Time | Significance |
|---|---|---|---|
| CR | FBN | 95.555 | |
| CR | WAIT | 94.843 | |
| RWK | FBN | 94.212 | |
| FIFO | FBN | 94.138 | |
| RWK | RV | 93.124 | |
| FIFO | RV | 93.097 | |
| RWK | WAIT | 92.748 | |
| FIFO | WAIT | 92.445 | |
| CR | RV | 88.723 | |
| EDD | FBN | 74.386 | |
| EDD | WAIT | 72.959 | |
| EDD | RV | 71.171 | |
| SPT | FBN | 59.733 | |
| SPT | RV | 58.140 | |
| SPT | WAIT | 56.340 | |

| DR | % On Time | Sig. |
|---|---|---|
| RWK | 93.361 | |
| FIFO | 93.227 | |
| CR | 93.040 | |
| EDD | 72.839 | |
| SPT | 58.071 | |

| RS | % On Time | Sig. |
|---|---|---|
| FBN | 83.605 | |
| WAIT | 81.867 | |
| RV | 80.851 | |

Table E.4. ANOVA and Tukey Tests for Percent Idle at One Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 4 | 1.350 | 1.350 | 0.338 | 891.800 | 0.000 |
| **RS** | 2 | 6.826 | 6.826 | 3.413 | 9018.330 | 0.000 |
| **DR*RS** | 8 | 0.005 | 0.005 | 0.001 | 1.570 | 0.140 |
| **Error** | 135 | 0.051 | 0.051 | 0.000 | | |
| **Total** | **149** | **8.232** | | | | |

| DR | RS | % Idle | Significance |
|---|---|---|---|
| SPT | WAIT | 59.471 | |
| EDD | WAIT | 59.348 | |
| SPT | RV | 59.314 | |
| FIFO | WAIT | 59.237 | |
| RWK | WAIT | 59.233 | |
| CR | WAIT | 59.214 | |
| EDD | RV | 59.205 | |
| CR | RV | 59.093 | |
| FIFO | RV | 59.085 | |
| RWK | RV | 59.082 | |
| SPT | FBN | 58.961 | |
| EDD | FBN | 58.842 | |
| FIFO | FBN | 58.727 | |
| RWK | FBN | 58.727 | |
| CR | FBN | 58.710 | |

| DR | % Idle | Sig. |
|---|---|---|
| SPT | 59.249 | |
| EDD | 59.132 | |
| FIFO | 59.016 | |
| RWK | 59.014 | |
| CR | 59.006 | |

| RS | % Idle | Sig. |
|---|---|---|
| WAIT | 59.301 | |
| RV | 59.156 | |
| FBN | 58.793 | |

Table E.5. ANOVA and Tukey Tests for Average WIP at One Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 4 | 3448.380 | 3448.380 | 862.100 | 2116.530 | 0.000 |
| **RS** | 2 | 48.640 | 48.640 | 24.320 | 59.710 | 0.000 |
| **DR*RS** | 8 | 32.160 | 32.160 | 4.020 | 9.870 | 0.000 |
| **Error** | 135 | 54.990 | 54.990 | 0.410 | | |
| **Total** | **149** | **3584.170** | | | | |

| DR | RS | Avg. WIP | Significance |
|---|---|---|---|
| RWK | FBN | 181.111 | |
| FIFO | FBN | 181.161 | |
| FIFO | RV | 181.815 | |
| RWK | RV | 181.822 | |
| RWK | WAIT | 182.372 | |
| FIFO | WAIT | 182.533 | |
| CR | FBN | 183.682 | |
| CR | WAIT | 184.302 | |
| CR | RV | 186.542 | |
| EDD | FBN | 186.898 | |
| EDD | WAIT | 187.904 | |
| EDD | RV | 188.139 | |
| SPT | FBN | 193.947 | |
| SPT | RV | 194.883 | |
| SPT | WAIT | 195.285 | |

| DR | Avg. WIP | Sig. |
|---|---|---|
| RWK | 181.768 | |
| FIFO | 181.836 | |
| CR | 184.842 | |
| EDD | 187.647 | |
| SPT | 194.705 | |

| RS | Avg. WIP | Sig. |
|---|---|---|
| FBN | 185.360 | |
| WAIT | 186.479 | |
| RV | 186.640 | |

Table E.6. ANOVA and Tukey Tests for Average XT at One Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 4 | 0.156 | 0.156 | 0.039 | 1384.940 | 0.000 |
| **RS** | 2 | 0.002 | 0.002 | 0.001 | 38.080 | 0.000 |
| **DR*RS** | 8 | 0.002 | 0.002 | 0.000 | 7.990 | 0.000 |
| **Error** | 135 | 0.004 | 0.004 | 0.000 | | |
| **Total** | **149** | **0.164** | | | | |

| DR | RS | Avg. XT | Significance |
|---|---|---|---|
| RWK | FBN | 1.439 | |
| FIFO | FBN | 1.441 | |
| FIFO | RV | 1.443 | |
| RWK | RV | 1.443 | |
| RWK | WAIT | 1.448 | |
| FIFO | WAIT | 1.451 | |
| EDD | FBN | 1.459 | |
| CR | FBN | 1.462 | |
| EDD | RV | 1.466 | |
| EDD | WAIT | 1.467 | |
| CR | WAIT | 1.469 | |
| CR | RV | 1.483 | |
| SPT | FBN | 1.528 | |
| SPT | RV | 1.532 | |
| SPT | WAIT | 1.536 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 1.443 | |
| FIFO | 1.445 | |
| EDD | 1.464 | |
| CR | 1.471 | |
| SPT | 1.532 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 1.466 | |
| RV | 1.473 | |
| WAIT | 1.474 | |

Table E.7. ANOVA and Tukey Tests for Average Cycle Time at Five Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 34090.300 | 34090.300 | 8522.600 | 1883.920 | 0.000 |
| RS | 2 | 15122.500 | 15122.500 | 7561.300 | 1671.430 | 0.000 |
| DR*RS | 8 | 30032.500 | 30032.500 | 3754.100 | 829.840 | 0.000 |
| Error | 135 | 610.700 | 610.700 | 4.500 | | |
| Total | 149 | 79856.100 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 330.597 | |
| FIFO | FBN | 330.855 | |
| RWK | RV | 335.952 | |
| FIFO | RV | 336.727 | |
| RWK | WAIT | 337.315 | |
| FIFO | WAIT | 338.507 | |
| EDD | FBN | 342.757 | |
| CR | FBN | 346.111 | |
| CR | WAIT | 346.694 | |
| EDD | WAIT | 348.918 | |
| EDD | RV | 355.188 | |
| SPT | FBN | 355.574 | |
| SPT | WAIT | 362.435 | |
| SPT | RV | 369.109 | |
| CR | RV | 426.613 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 334.621 | |
| FIFO | 335.363 | |
| EDD | 348.954 | |
| SPT | 362.373 | |
| CR | 373.139 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 341.179 | |
| WAIT | 346.774 | |
| RV | 364.718 | |

Table E.8. ANOVA and Tukey Tests for St. Dev. Of Cycle Time at Five Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 19938.400 | 19938.400 | 4984.600 | 2267.390 | 0.000 |
| RS | 2 | 4104.200 | 4104.200 | 2052.100 | 933.470 | 0.000 |
| DR*RS | 8 | 4424.600 | 4424.600 | 553.100 | 251.580 | 0.000 |
| Error | 135 | 296.800 | 296.800 | 2.200 | | |
| Total | 149 | 28764.000 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 81.510 | |
| FIFO | FBN | 81.611 | |
| RWK | WAIT | 81.940 | |
| FIFO | WAIT | 82.210 | |
| CR | WAIT | 82.823 | |
| RWK | RV | 83.320 | |
| FIFO | RV | 83.462 | |
| CR | FBN | 84.411 | |
| SPT | WAIT | 102.660 | |
| SPT | FBN | 103.617 | |
| EDD | WAIT | 106.476 | |
| EDD | FBN | 106.490 | |
| EDD | RV | 114.175 | |
| SPT | RV | 115.049 | |
| CR | RV | 116.333 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 82.257 | |
| FIFO | 82.428 | |
| CR | 94.522 | |
| SPT | 107.109 | |
| EDD | 109.047 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| WAIT | 91.222 | |
| FBN | 91.528 | |
| RV | 102.468 | |

Table E.9. ANOVA and Tukey Tests for Percentage On Time at Five Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 39218.300 | 39218.300 | 9804.600 | 2234.650 | 0.000 |
| RS | 2 | 17647.600 | 17647.600 | 8823.800 | 2011.110 | 0.000 |
| DR*RS | 8 | 36420.100 | 36420.100 | 4552.500 | 1037.610 | 0.000 |
| Error | 135 | 592.300 | 592.300 | 4.400 | | |
| Total | 149 | 93878.300 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 96.429 | |
| FIFO | FBN | 96.384 | |
| RWK | WAIT | 93.132 | |
| RWK | RV | 92.752 | |
| FIFO | WAIT | 92.432 | |
| FIFO | RV | 92.311 | |
| CR | FBN | 89.195 | |
| CR | WAIT | 88.304 | |
| EDD | FBN | 76.889 | |
| EDD | WAIT | 71.565 | |
| SPT | FBN | 63.810 | |
| EDD | RV | 60.184 | |
| SPT | WAIT | 55.271 | |
| SPT | RV | 52.319 | |
| CR | RV | 0.682 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 94.104 | |
| FIFO | 93.709 | |
| EDD | 69.546 | |
| CR | 59.394 | |
| SPT | 57.133 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 84.541 | |
| WAIT | 80.141 | |
| RV | 59.650 | |

Table E.10. ANOVA and Tukey Tests for Percent Idle at Five Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 1.235 | 1.235 | 0.309 | 416.080 | 0.000 |
| RS | 2 | 49.466 | 49.466 | 24.733 | 33000.000 | 0.000 |
| DR*RS | 8 | 0.555 | 0.555 | 0.069 | 93.540 | 0.000 |
| Error | 135 | 0.100 | 0.100 | 0.001 | | |
| Total | 149 | 51.357 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| SPT | WAIT | 58.408 | |
| EDD | WAIT | 58.269 | |
| FIFO | WAIT | 58.163 | |
| RWK | WAIT | 58.161 | |
| CR | WAIT | 58.157 | |
| CR | RV | 58.102 | |
| SPT | RV | 58.008 | |
| EDD | RV | 57.905 | |
| FIFO | RV | 57.764 | |
| RWK | RV | 57.763 | |
| SPT | FBN | 57.046 | |
| EDD | FBN | 56.925 | |
| CR | FBN | 56.834 | |
| FIFO | FBN | 56.809 | |
| RWK | FBN | 56.808 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| SPT | 57.821 | |
| EDD | 57.700 | |
| CR | 57.698 | |
| FIFO | 57.579 | |
| RWK | 57.577 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| WAIT | 58.232 | |
| RV | 57.908 | |
| FBN | 56.884 | |

Table E.11. ANOVA and Tukey Tests for Average WIP at Five Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 4 | 10551.200 | 10551.200 | 2637.800 | 1876.030 | 0.000 |
| **RS** | 2 | 4679.700 | 4679.700 | 2339.900 | 1664.130 | 0.000 |
| **DR*RS** | 8 | 9295.600 | 9295.600 | 1162.000 | 826.390 | 0.000 |
| Error | 135 | 189.800 | 189.800 | 1.400 | | |
| Total | **149** | **24716.400** | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 183.914 | |
| FIFO | FBN | 184.059 | |
| RWK | RV | 186.897 | |
| FIFO | RV | 187.323 | |
| RWK | WAIT | 187.649 | |
| FIFO | WAIT | 188.314 | |
| EDD | FBN | 190.682 | |
| CR | FBN | 192.545 | |
| CR | WAIT | 192.868 | |
| EDD | WAIT | 194.109 | |
| EDD | RV | 197.596 | |
| SPT | FBN | 197.812 | |
| SPT | WAIT | 201.630 | |
| SPT | RV | 205.335 | |
| CR | RV | 237.331 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 186.153 | |
| FIFO | 186.565 | |
| EDD | 194.129 | |
| SPT | 201.592 | |
| CR | 207.581 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 189.802 | |
| WAIT | 192.914 | |
| RV | 202.896 | |

Table E.12. ANOVA and Tukey Tests for Average XT at Five Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 4 | 0.631 | 0.631 | 0.158 | 1742.520 | 0.000 |
| **RS** | 2 | 0.226 | 0.226 | 0.113 | 1247.810 | 0.000 |
| **DR*RS** | 8 | 0.543 | 0.543 | 0.068 | 748.720 | 0.000 |
| Error | 135 | 0.012 | 0.012 | 0.000 | | |
| Total | **149** | **1.412** | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 1.467 | |
| FIFO | FBN | 1.470 | |
| RWK | RV | 1.482 | |
| FIFO | RV | 1.488 | |
| RWK | WAIT | 1.492 | |
| EDD | FBN | 1.495 | |
| FIFO | WAIT | 1.496 | |
| EDD | WAIT | 1.515 | |
| EDD | RV | 1.534 | |
| CR | WAIT | 1.535 | |
| CR | FBN | 1.539 | |
| SPT | FBN | 1.562 | |
| SPT | WAIT | 1.587 | |
| SPT | RV | 1.608 | |
| CR | RV | 1.871 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 1.480 | |
| FIFO | 1.485 | |
| EDD | 1.515 | |
| SPT | 1.586 | |
| CR | 1.648 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 1.507 | |
| WAIT | 1.525 | |
| RV | 1.597 | |

Table E.13. ANOVA and Tukey Tests for Average Cycle Time at Ten Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 123998.000 | 123998.000 | 30999.000 | 952.670 | 0.000 |
| RS | 2 | 45824.000 | 45824.000 | 22912.000 | 704.120 | 0.000 |
| DR*RS | 8 | 25488.000 | 25488.000 | 3186.000 | 97.910 | 0.000 |
| Error | 135 | 4393.000 | 4393.000 | 33.000 | | |
| Total | 149 | 199702.000 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 344.247 | |
| FIFO | FBN | 347.660 | |
| RWK | WAIT | 353.473 | |
| FIFO | WAIT | 359.451 | |
| RWK | RV | 362.930 | |
| EDD | FBN | 363.743 | |
| FIFO | RV | 370.150 | |
| EDD | WAIT | 372.282 | |
| SPT | FBN | 380.429 | |
| SPT | WAIT | 386.310 | |
| EDD | RV | 391.888 | |
| CR | WAIT | 400.353 | |
| CR | FBN | 406.223 | |
| SPT | RV | 424.999 | |
| CR | RV | 490.730 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 353.550 | |
| FIFO | 359.087 | |
| EDD | 375.971 | |
| SPT | 397.246 | |
| CR | 432.435 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 368.461 | |
| WAIT | 374.374 | |
| RV | 408.139 | |

Table E.14. ANOVA and Tukey Tests for Std. Dev. Of Cycle Time at Ten Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 51258.100 | 51258.100 | 12814.500 | 189.830 | 0.000 |
| RS | 2 | 16706.700 | 16706.700 | 8353.300 | 123.750 | 0.000 |
| DR*RS | 8 | 10792.800 | 10792.800 | 1349.100 | 19.990 | 0.000 |
| Error | 135 | 9113.100 | 9113.100 | 67.500 | | |
| Total | 149 | 87870.600 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 85.607 | |
| RWK | WAIT | 86.234 | |
| FIFO | FBN | 86.497 | |
| FIFO | WAIT | 87.855 | |
| RWK | RV | 92.183 | |
| FIFO | RV | 94.197 | |
| CR | WAIT | 104.217 | |
| CR | FBN | 106.532 | |
| EDD | FBN | 116.604 | |
| SPT | WAIT | 117.146 | |
| SPT | FBN | 118.121 | |
| EDD | WAIT | 118.321 | |
| EDD | RV | 130.013 | |
| CR | RV | 139.387 | |
| SPT | RV | 169.724 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 88.008 | |
| FIFO | 89.516 | |
| CR | 116.712 | |
| EDD | 121.646 | |
| SPT | 134.997 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 102.672 | |
| WAIT | 102.755 | |
| RV | 125.101 | |

Table E.15. ANOVA and Tukey Tests for Percentage On Time at Ten Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 4 | 144869.000 | 144869.000 | 36217.000 | 1777.970 | 0.000 |
| **RS** | 2 | 10790.000 | 10790.000 | 5395.000 | 264.840 | 0.000 |
| **DR*RS** | 8 | 2662.000 | 2662.000 | 333.000 | 16.330 | 0.000 |
| **Error** | 135 | 2750.000 | 2750.000 | 20.000 | | |
| **Total** | **149** | **161070.000** | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 98.010 | |
| FIFO | FBN | 97.061 | |
| RWK | WAIT | 95.356 | |
| FIFO | WAIT | 91.088 | |
| RWK | RV | 82.409 | |
| EDD | FBN | 73.857 | |
| FIFO | RV | 73.184 | |
| EDD | WAIT | 65.237 | |
| SPT | FBN | 61.901 | |
| SPT | WAIT | 57.386 | |
| SPT | RV | 43.592 | |
| EDD | RV | 38.735 | |
| CR | WAIT | 9.764 | |
| CR | FBN | 4.440 | |
| CR | RV | 0.307 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 91.925 | |
| FIFO | 87.111 | |
| EDD | 59.276 | |
| SPT | 54.293 | |
| CR | 4.837 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 67.054 | |
| WAIT | 63.766 | |
| RV | 47.645 | |

Table E.16. ANOVA and Tukey Tests for Percent Idle at Ten Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 4 | 1.685 | 1.685 | 0.421 | 374.290 | 0.000 |
| **RS** | 2 | 89.936 | 89.936 | 44.968 | 40000.000 | 0.000 |
| **DR*RS** | 8 | 0.178 | 0.178 | 0.022 | 19.730 | 0.000 |
| **Error** | 135 | 0.152 | 0.152 | 0.001 | | |
| **Total** | **149** | **91.951** | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| SPT | WAIT | 57.531 | |
| EDD | WAIT | 57.406 | |
| CR | WAIT | 57.403 | |
| FIFO | WAIT | 57.292 | |
| RWK | WAIT | 57.278 | |
| CR | RV | 57.077 | |
| SPT | RV | 57.013 | |
| EDD | RV | 56.910 | |
| FIFO | RV | 56.747 | |
| RWK | RV | 56.732 | |
| SPT | FBN | 55.686 | |
| CR | FBN | 55.625 | |
| EDD | FBN | 55.564 | |
| FIFO | FBN | 55.448 | |
| RWK | FBN | 55.433 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| SPT | 56.743 | |
| CR | 56.702 | |
| EDD | 56.627 | |
| FIFO | 56.496 | |
| RWK | 56.481 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| WAIT | 57.382 | |
| RV | 56.896 | |
| FBN | 55.551 | |

Table E.17. ANOVA and Tukey Tests for Average WIP at Ten Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 38384.500 | 38384.500 | 9596.100 | 994.040 | 0.000 |
| RS | 2 | 14197.000 | 14197.000 | 7098.500 | 735.320 | 0.000 |
| DR*RS | 8 | 7891.400 | 7891.400 | 986.400 | 102.180 | 0.000 |
| Error | 135 | 1303.200 | 1303.200 | 9.700 | | |
| Total | 149 | 61776.100 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 191.506 | |
| FIFO | FBN | 193.406 | |
| RWK | WAIT | 196.639 | |
| FIFO | WAIT | 199.962 | |
| RWK | RV | 201.900 | |
| EDD | FBN | 202.353 | |
| FIFO | RV | 205.919 | |
| EDD | WAIT | 207.105 | |
| SPT | FBN | 211.639 | |
| SPT | WAIT | 214.912 | |
| EDD | RV | 218.016 | |
| CR | WAIT | 222.718 | |
| CR | FBN | 225.984 | |
| SPT | RV | 236.474 | |
| CR | RV | 273.003 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 196.682 | |
| FIFO | 199.762 | |
| EDD | 209.158 | |
| SPT | 221.008 | |
| CR | 240.568 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 204.978 | |
| WAIT | 208.267 | |
| RV | 227.062 | |

Table E.18. ANOVA and Tukey Tests for Average XT at Ten Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 2.293 | 2.293 | 0.573 | 1076.200 | 0.000 |
| RS | 2 | 0.697 | 0.697 | 0.348 | 654.240 | 0.000 |
| DR*RS | 8 | 0.464 | 0.464 | 0.058 | 108.960 | 0.000 |
| Error | 135 | 0.072 | 0.072 | 0.001 | | |
| Total | 149 | 3.526 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 1.538 | |
| FIFO | FBN | 1.553 | |
| RWK | WAIT | 1.562 | |
| EDD | FBN | 1.588 | |
| FIFO | WAIT | 1.589 | |
| RWK | RV | 1.603 | |
| EDD | WAIT | 1.611 | |
| FIFO | RV | 1.634 | |
| SPT | FBN | 1.675 | |
| SPT | WAIT | 1.687 | |
| EDD | RV | 1.688 | |
| CR | WAIT | 1.763 | |
| CR | FBN | 1.805 | |
| SPT | RV | 1.833 | |
| CR | RV | 2.149 | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 1.538 | |
| FIFO | FBN | 1.553 | |
| RWK | WAIT | 1.562 | |
| EDD | FBN | 1.588 | |
| FIFO | WAIT | 1.589 | |
| RWK | RV | 1.603 | |
| EDD | WAIT | 1.611 | |
| FIFO | RV | 1.634 | |
| SPT | FBN | 1.675 | |
| SPT | WAIT | 1.687 | |
| EDD | RV | 1.688 | |
| CR | WAIT | 1.763 | |
| CR | FBN | 1.805 | |
| SPT | RV | 1.833 | |
| CR | RV | 2.149 | |

## Appendix F. MTS Three Factor ANOVA Tables

This appendix contains the ANOVA results from the make-to-stock fab. These tests used the dispatching rule, rework strategy, and rework level as the factors.

Table F.1. ANOVA Table of Average Cycle Time

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 115769.000 | 115769.000 | 28942.000 | 1872.140 | 0.000 |
| RS | 2 | 40289.000 | 40289.000 | 20145.000 | 1303.060 | 0.000 |
| RL | 2 | 346621.000 | 346621.000 | 173311.000 | 11000.000 | 0.000 |
| DR*RS | 8 | 39869.000 | 39869.000 | 4984.000 | 322.370 | 0.000 |
| DR*RL | 8 | 80856.000 | 80856.000 | 10107.000 | 653.780 | 0.000 |
| RS*RL | 4 | 28752.000 | 28752.000 | 7188.000 | 464.960 | 0.000 |
| DR*RS*RL | 16 | 22965.000 | 22965.000 | 1435.000 | 92.850 | 0.000 |
| Error | 405 | 6261.000 | 6261.000 | 15.000 | | |
| Total | 449 | 681383.000 | | | | |

Table F.2. ANOVA Table of Standard Deviation of Cycle Time

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 54735.500 | 54735.500 | 13683.900 | 810.870 | 0.000 |
| RS | 2 | 2901.100 | 2901.100 | 1450.500 | 85.950 | 0.000 |
| RL | 2 | 34986.700 | 34986.700 | 17493.400 | 1036.610 | 0.000 |
| DR*RS | 8 | 3746.900 | 3746.900 | 468.400 | 27.750 | 0.000 |
| DR*RL | 8 | 18221.500 | 18221.500 | 2277.700 | 134.970 | 0.000 |
| RS*RL | 4 | 2091.600 | 2091.600 | 522.900 | 30.990 | 0.000 |
| DR*RS*RL | 16 | 4137.800 | 4137.800 | 258.600 | 15.320 | 0.000 |
| Error | 405 | 6834.600 | 6834.600 | 16.900 | | |
| Total | 449 | 127655.700 | | | | |

Table F.3. ANOVA Table of Percentage On Time

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 98338.100 | 98338.100 | 24584.500 | 1699.720 | 0.000 |
| RS | 2 | 19559.900 | 19559.900 | 9779.900 | 676.160 | 0.000 |
| RL | 2 | 27904.900 | 27904.900 | 13952.500 | 964.640 | 0.000 |
| DR*RS | 8 | 13186.000 | 13186.000 | 1648.300 | 113.960 | 0.000 |
| DR*RL | 8 | 72774.500 | 72774.500 | 9096.800 | 628.930 | 0.000 |
| RS*RL | 4 | 6656.500 | 6656.500 | 1664.100 | 115.050 | 0.000 |
| DR*RS*RL | 16 | 18473.700 | 18473.700 | 1154.600 | 79.830 | 0.000 |
| Error | 405 | 5857.900 | 5857.900 | 14.500 | | |
| Total | 449 | 262751.500 | | | | |

Table F.4. ANOVA Table of Percent Idle

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 1.487 | 1.487 | 0.372 | 829.210 | 0.000 |
| RS | 2 | 51.472 | 51.472 | 25.736 | 57000.000 | 0.000 |
| RL | 2 | 217.486 | 217.486 | 108.743 | 240000.000 | 0.000 |
| DR*RS | 8 | 0.167 | 0.167 | 0.021 | 46.650 | 0.000 |
| DR*RL | 8 | 0.204 | 0.204 | 0.026 | 56.900 | 0.000 |
| RS*RL | 4 | 10.701 | 10.701 | 2.675 | 5966.110 | 0.000 |
| DR*RS*RL | 16 | 0.075 | 0.075 | 0.005 | 10.470 | 0.000 |
| Error | 405 | 0.182 | 0.182 | 0.000 | | |
| Total | 449 | 281.775 | | | | |

Table F.5. ANOVA Table of Average WIP

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 13045.500 | 13045.500 | 3261.400 | 1857.750 | 0.000 |
| RS | 2 | 4540.700 | 4540.700 | 2270.300 | 1293.240 | 0.000 |
| RL | 2 | 39058.500 | 39058.500 | 19529.300 | 11000.000 | 0.000 |
| DR*RS | 8 | 4491.600 | 4491.600 | 561.500 | 319.820 | 0.000 |
| DR*RL | 8 | 9111.100 | 9111.100 | 1138.900 | 648.740 | 0.000 |
| RS*RL | 4 | 3240.100 | 3240.100 | 810.000 | 461.400 | 0.000 |
| DR*RS*RL | 16 | 2587.600 | 2587.600 | 161.700 | 92.120 | 0.000 |
| Error | 405 | 711.000 | 711.000 | 1.800 | | |
| Total | 449 | 76786.000 | | | | |

Table F.6. ANOVA Table of Average XT

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 1.722 | 1.722 | 0.431 | 1737.590 | 0.000 |
| RS | 2 | 0.544 | 0.544 | 0.272 | 1097.170 | 0.000 |
| RL | 2 | 5.419 | 5.419 | 2.709 | 11000.000 | 0.000 |
| DR*RS | 8 | 0.610 | 0.610 | 0.076 | 307.690 | 0.000 |
| DR*RL | 8 | 1.207 | 1.207 | 0.151 | 608.700 | 0.000 |
| RS*RL | 4 | 0.412 | 0.412 | 0.103 | 415.510 | 0.000 |
| DR*RS*RL | 16 | 0.351 | 0.351 | 0.022 | 88.630 | 0.000 |
| Error | 405 | 0.100 | 0.100 | 0.000 | | |
| Total | 449 | 10.365 | | | | |

## Appendix G. MTS Two Factor ANOVA and Tukey Pairwise Comparison Results

This Appendix shows the ANOVA and Tukey pairwise comparison tables for each of the performance measures at each rework level in the MTS fab. The ANOVA tests determine whether dispatching rules and rework strategies are significant independently, and also whether their interaction is significant. The pairwise comparisons are done for the dispatching rule and rework strategy independently and also for a combination of the two. These tests are done at a 95 percent confidence level. The vertical lines on the charts refer to rules or strategies that are statistically the same as the others that are connected by the same vertical line.

Table G.1. ANOVA and Tukey Tests for Average Cycle Time at One Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 8142.890 | 8142.890 | 2035.720 | 645.140 | 0.000 |
| RS | 2 | 234.730 | 234.730 | 117.370 | 37.190 | 0.000 |
| DR*RS | 8 | 124.260 | 124.260 | 15.530 | 4.920 | 0.000 |
| Error | 135 | 425.990 | 425.990 | 3.160 | | |
| Total | 149 | 8927.870 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 370.492 | |
| FIFO | FBN | 370.643 | |
| RWK | RV | 372.163 | |
| FIFO | RV | 372.343 | |
| RWK | WAIT | 373.130 | |
| FIFO | WAIT | 373.343 | |
| CR | FBN | 374.391 | |
| CR | WAIT | 376.293 | |
| EDD | FBN | 377.904 | |
| EDD | RV | 379.456 | |
| CR | RV | 380.535 | |
| EDD | WAIT | 380.738 | |
| SPT | FBN | 390.341 | |
| SPT | WAIT | 392.634 | |
| SPT | RV | 393.287 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 371.928 | |
| FIFO | 372.109 | |
| CR | 377.073 | |
| EDD | 379.366 | |
| SPT | 392.087 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 376.754 | |
| WAIT | 379.227 | |
| RV | 379.557 | |

Table G.2. ANOVA and Tukey Tests for St. Dev of Cycle Time at One Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 9172.240 | 9172.240 | 2293.060 | 572.210 | 0.000 |
| RS | 2 | 19.380 | 19.380 | 9.690 | 2.420 | 0.093 |
| DR*RS | 8 | 24.510 | 24.510 | 3.060 | 0.760 | 0.635 |
| Error | 135 | 541.000 | 541.000 | 4.010 | | |
| Total | 149 | 9757.120 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 41.046 | |
| FIFO | FBN | 41.137 | |
| FIFO | RV | 41.251 | |
| RWK | RV | 41.285 | |
| FIFO | WAIT | 41.612 | |
| RWK | WAIT | 41.752 | |
| CR | FBN | 42.603 | |
| CR | WAIT | 43.564 | |
| CR | RV | 43.956 | |
| SPT | FBN | 55.066 | |
| SPT | WAIT | 55.118 | |
| SPT | RV | 57.149 | |
| EDD | FBN | 59.273 | |
| EDD | RV | 59.830 | |
| EDD | WAIT | 59.859 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| FIFO | 41.333 | |
| RWK | 41.361 | |
| CR | 43.374 | |
| SPT | 55.778 | |
| EDD | 59.654 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 47.825 | |
| WAIT | 48.381 | |
| RV | 48.694 | |

Table G.3. ANOVA and Tukey Tests for Percentage On Time at One Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 4 | 22174.100 | 22174.100 | 5543.500 | 949.730 | 0.000 |
| **RS** | 2 | 224.000 | 224.000 | 112.000 | 19.190 | 0.000 |
| **DR*RS** | 8 | 230.100 | 230.100 | 28.800 | 4.930 | 0.000 |
| Error | 135 | 788.000 | 788.000 | 5.800 | | |
| **Total** | **149** | **23416.100** | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| CR | FBN | 96.261 | |
| CR | WAIT | 95.313 | |
| FIFO | FBN | 93.243 | |
| RWK | FBN | 93.180 | |
| RWK | RV | 92.343 | |
| FIFO | RV | 91.977 | |
| RWK | WAIT | 91.825 | |
| FIFO | WAIT | 91.686 | |
| CR | RV | 88.925 | |
| EDD | FBN | 79.199 | |
| EDD | RV | 77.561 | |
| EDD | WAIT | 76.617 | |
| SPT | FBN | 64.572 | |
| SPT | WAIT | 61.453 | |
| SPT | RV | 60.896 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| CR | 93.500 | |
| RWK | 92.449 | |
| FIFO | 92.302 | |
| EDD | 77.792 | |
| SPT | 62.307 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 85.291 | |
| WAIT | 83.379 | |
| RV | 82.340 | |

Table G.4. ANOVA and Tukey Tests for Percent Idle at One Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 4 | 0.519 | 0.519 | 0.130 | 550.070 | 0.000 |
| **RS** | 2 | 2.703 | 2.703 | 1.352 | 5725.840 | 0.000 |
| **DR*RS** | 8 | 0.001 | 0.001 | 0.000 | 0.470 | 0.878 |
| Error | 135 | 0.032 | 0.032 | 0.000 | | |
| **Total** | **149** | **3.256** | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| SPT | WAIT | 71.549 | |
| EDD | WAIT | 71.474 | |
| SPT | RV | 71.450 | |
| FIFO | WAIT | 71.406 | |
| RWK | WAIT | 71.406 | |
| CR | WAIT | 71.388 | |
| EDD | RV | 71.378 | |
| RWK | RV | 71.310 | |
| FIFO | RV | 71.309 | |
| CR | RV | 71.304 | |
| SPT | FBN | 71.230 | |
| EDD | FBN | 71.152 | |
| RWK | FBN | 71.087 | |
| FIFO | FBN | 71.084 | |
| CR | FBN | 71.070 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| SPT | 71.410 | |
| EDD | 71.335 | |
| RWK | 71.268 | |
| FIFO | 71.266 | |
| CR | 71.254 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| WAIT | 71.445 | |
| RV | 71.350 | |
| FBN | 71.125 | |

Table G.5. ANOVA and Tukey Tests for Average WIP at One Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 917.474 | 917.474 | 229.369 | 648.850 | 0.000 |
| RS | 2 | 26.480 | 26.480 | 13.240 | 37.450 | 0.000 |
| DR*RS | 8 | 13.991 | 13.991 | 1.749 | 4.950 | 0.000 |
| Error | 135 | 47.723 | 47.723 | 0.354 | | |
| Total | 149 | 1005.668 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 124.363 | |
| FIFO | FBN | 124.413 | |
| RWK | RV | 124.925 | |
| FIFO | RV | 124.984 | |
| RWK | WAIT | 125.248 | |
| FIFO | WAIT | 125.321 | |
| CR | FBN | 125.672 | |
| CR | WAIT | 126.311 | |
| EDD | FBN | 126.851 | |
| EDD | RV | 127.374 | |
| CR | RV | 127.735 | |
| EDD | WAIT | 127.803 | |
| SPT | FBN | 131.026 | |
| SPT | WAIT | 131.795 | |
| SPT | RV | 132.015 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 124.845 | |
| FIFO | 124.906 | |
| CR | 126.573 | |
| EDD | 127.343 | |
| SPT | 131.612 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 126.465 | |
| WAIT | 127.296 | |
| RV | 127.407 | |

Table G.6. ANOVA and Tukey Tests for Average XT at One Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 0.117 | 0.117 | 0.029 | 502.830 | 0.000 |
| RS | 2 | 0.003 | 0.003 | 0.001 | 25.430 | 0.000 |
| DR*RS | 8 | 0.002 | 0.002 | 0.000 | 4.380 | 0.000 |
| Error | 135 | 0.008 | 0.008 | 0.000 | | |
| Total | 149 | 0.129 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| FIFO | FBN | 1.452 | |
| RWK | FBN | 1.453 | |
| RWK | RV | 1.456 | |
| FIFO | RV | 1.458 | |
| RWK | WAIT | 1.462 | |
| FIFO | WAIT | 1.463 | |
| CR | FBN | 1.466 | |
| EDD | FBN | 1.472 | |
| CR | WAIT | 1.474 | |
| EDD | RV | 1.478 | |
| EDD | WAIT | 1.484 | |
| CR | RV | 1.489 | |
| SPT | FBN | 1.528 | |
| SPT | WAIT | 1.534 | |
| SPT | RV | 1.538 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 1.457 | |
| FIFO | 1.458 | |
| CR | 1.476 | |
| EDD | 1.478 | |
| SPT | 1.533 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 1.474 | |
| WAIT | 1.483 | |
| RV | 1.484 | |

Table G.7. ANOVA and Tukey Tests for Average Cycle Time at Five Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 23109.300 | 23109.300 | 5777.300 | 482.200 | 0.000 |
| RS | 2 | 8455.000 | 8455.000 | 4227.500 | 352.840 | 0.000 |
| DR*RS | 8 | 12254.900 | 12254.900 | 1531.900 | 127.850 | 0.000 |
| Error | 135 | 1617.500 | 1617.500 | 12.000 | | |
| Total | 149 | 45436.600 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 377.231 | |
| FIFO | FBN | 378.508 | |
| RWK | RV | 384.084 | |
| RWK | WAIT | 385.701 | |
| FIFO | RV | 386.135 | |
| FIFO | WAIT | 388.310 | |
| EDD | FBN | 388.579 | |
| CR | FBN | 391.105 | |
| EDD | RV | 394.714 | |
| EDD | WAIT | 396.653 | |
| SPT | FBN | 399.224 | |
| CR | WAIT | 402.668 | |
| SPT | WAIT | 407.465 | |
| SPT | RV | 413.148 | |
| CR | RV | 448.519 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 382.339 | |
| FIFO | 384.318 | |
| EDD | 393.315 | |
| SPT | 406.612 | |
| CR | 414.097 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 386.929 | |
| WAIT | 396.159 | |
| RV | 405.320 | |

Table G.8. ANOVA and Tukey Tests for St. Dev. Of Cycle Time at Five Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 11525.160 | 11525.160 | 2881.290 | 586.440 | 0.000 |
| RS | 2 | 602.040 | 602.040 | 301.020 | 61.270 | 0.000 |
| DR*RS | 8 | 634.020 | 634.020 | 79.250 | 16.130 | 0.000 |
| Error | 135 | 663.280 | 663.280 | 4.910 | | |
| Total | 149 | 13424.500 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 42.150 | |
| FIFO | FBN | 42.252 | |
| RWK | RV | 43.034 | |
| FIFO | RV | 43.253 | |
| RWK | WAIT | 44.156 | |
| FIFO | WAIT | 44.780 | |
| CR | FBN | 47.580 | |
| CR | WAIT | 53.111 | |
| SPT | FBN | 58.308 | |
| SPT | WAIT | 60.017 | |
| CR | RV | 60.566 | |
| EDD | FBN | 62.916 | |
| EDD | WAIT | 64.468 | |
| EDD | RV | 65.039 | |
| SPT | RV | 65.820 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 43.113 | |
| FIFO | 43.429 | |
| CR | 53.752 | |
| SPT | 61.381 | |
| EDD | 64.141 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 50.641 | |
| WAIT | 53.306 | |
| RV | 55.542 | |

Table G.9. ANOVA and Tukey Tests for Percentage On Time at Five Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 31923.500 | 31923.500 | 7980.900 | 844.110 | 0.000 |
| RS | 2 | 13679.000 | 13679.000 | 6839.500 | 723.390 | 0.000 |
| DR*RS | 8 | 30154.200 | 30154.200 | 3769.300 | 398.660 | 0.000 |
| Error | 135 | 1276.400 | 1276.400 | 9.500 | | |
| Total | 149 | 77033.100 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 96.415 | |
| FIFO | FBN | 95.918 | |
| CR | FBN | 94.283 | |
| RWK | WAIT | 93.069 | |
| RWK | RV | 92.949 | |
| FIFO | RV | 91.693 | |
| FIFO | WAIT | 91.244 | |
| EDD | FBN | 81.958 | |
| EDD | RV | 75.779 | |
| CR | WAIT | 75.316 | |
| EDD | WAIT | 74.585 | |
| SPT | FBN | 71.268 | |
| SPT | WAIT | 62.059 | |
| SPT | RV | 56.711 | |
| CR | RV | 6.928 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 94.144 | |
| FIFO | 92.952 | |
| EDD | 77.441 | |
| SPT | 63.346 | |
| CR | 58.842 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 87.968 | |
| WAIT | 79.255 | |
| RV | 64.812 | |

Table G.10. ANOVA and Tukey Tests for Percent Idle at Five Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 0.460 | 0.460 | 0.115 | 242.770 | 0.000 |
| RS | 2 | 20.953 | 20.953 | 10.477 | 22000.000 | 0.000 |
| DR*RS | 8 | 0.162 | 0.162 | 0.020 | 42.580 | 0.000 |
| Error | 135 | 0.064 | 0.064 | 0.001 | | |
| Total | 149 | 21.639 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| SPT | WAIT | 70.815 | |
| EDD | WAIT | 70.733 | |
| FIFO | WAIT | 70.672 | |
| RWK | WAIT | 70.668 | |
| CR | WAIT | 70.661 | |
| CR | RV | 70.567 | |
| SPT | RV | 70.551 | |
| EDD | RV | 70.471 | |
| FIFO | RV | 70.397 | |
| RWK | RV | 70.395 | |
| SPT | FBN | 69.933 | |
| EDD | FBN | 69.855 | |
| FIFO | FBN | 69.784 | |
| RWK | FBN | 69.781 | |
| CR | FBN | 69.779 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| SPT | 70.433 | |
| EDD | 70.353 | |
| CR | 70.336 | |
| FIFO | 70.284 | |
| RWK | 70.281 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| WAIT | 70.710 | |
| RV | 70.476 | |
| FBN | 69.826 | |

Table G.11. ANOVA and Tukey Tests for Average WIP at Five Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 4 | 2604.180 | 2604.180 | 651.050 | 485.080 | 0.000 |
| **RS** | 2 | 952.780 | 952.780 | 476.390 | 354.950 | 0.000 |
| **DR*RS** | 8 | 1380.360 | 1380.360 | 172.540 | 128.560 | 0.000 |
| **Error** | 135 | 181.190 | 181.190 | 1.340 | | |
| **Total** | **149** | **5118.510** | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 126.625 | |
| FIFO | FBN | 127.053 | |
| RWK | RV | 128.926 | |
| RWK | WAIT | 129.470 | |
| FIFO | RV | 129.615 | |
| FIFO | WAIT | 130.344 | |
| EDD | FBN | 130.434 | |
| CR | FBN | 131.284 | |
| EDD | RV | 132.494 | |
| EDD | WAIT | 133.144 | |
| SPT | FBN | 134.009 | |
| CR | WAIT | 135.164 | |
| SPT | WAIT | 136.774 | |
| SPT | RV | 138.684 | |
| CR | RV | 150.553 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 128.340 | |
| FIFO | 129.004 | |
| EDD | 132.024 | |
| SPT | 136.489 | |
| CR | 139.000 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 129.881 | |
| WAIT | 132.979 | |
| RV | 136.054 | |

Table G.12. ANOVA and Tukey Tests for Average XT at Five Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 4 | 0.337 | 0.337 | 0.084 | 421.970 | 0.000 |
| **RS** | 2 | 0.107 | 0.107 | 0.054 | 268.990 | 0.000 |
| **DR*RS** | 8 | 0.187 | 0.187 | 0.023 | 116.990 | 0.000 |
| **Error** | 135 | 0.027 | 0.027 | 0.000 | | |
| **Total** | **149** | **0.658** | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 1.483 | |
| FIFO | FBN | 1.489 | |
| RWK | RV | 1.505 | |
| RWK | WAIT | 1.510 | |
| FIFO | RV | 1.513 | |
| EDD | FBN | 1.520 | |
| FIFO | WAIT | 1.522 | |
| CR | FBN | 1.536 | |
| EDD | RV | 1.537 | |
| EDD | WAIT | 1.543 | |
| SPT | FBN | 1.567 | |
| CR | WAIT | 1.572 | |
| SPT | WAIT | 1.592 | |
| SPT | RV | 1.614 | |
| CR | RV | 1.753 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 1.499 | |
| FIFO | 1.508 | |
| EDD | 1.533 | |
| SPT | 1.591 | |
| CR | 1.620 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 1.519 | |
| WAIT | 1.548 | |
| RV | 1.584 | |

Table G.13. ANOVA and Tukey Tests for Average Cycle Time at Ten Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 165373.000 | 165373.000 | 41343.000 | 1323.350 | 0.000 |
| RS | 2 | 60351.000 | 60351.000 | 30176.000 | 965.880 | 0.000 |
| DR*RS | 8 | 50455.000 | 50455.000 | 6307.000 | 201.880 | 0.000 |
| Error | 135 | 4218.000 | 4218.000 | 31.000 | | |
| Total | 149 | 280397.000 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 401.008 | |
| FIFO | FBN | 407.090 | |
| RWK | WAIT | 413.099 | |
| EDD | FBN | 421.471 | |
| FIFO | WAIT | 422.425 | |
| RWK | RV | 423.683 | |
| EDD | WAIT | 432.627 | |
| SPT | FBN | 432.665 | |
| FIFO | RV | 434.778 | |
| SPT | WAIT | 440.042 | |
| EDD | RV | 440.402 | |
| CR | FBN | 459.787 | |
| CR | WAIT | 474.159 | |
| SPT | RV | 475.829 | |
| CR | RV | 583.728 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 412.597 | |
| FIFO | 421.431 | |
| EDD | 431.500 | |
| SPT | 449.512 | |
| CR | 505.891 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 424.404 | |
| WAIT | 436.470 | |
| RV | 471.684 | |

Table G.14. ANOVA and Tukey Tests for Std. Dev. Of Cycle Time at Ten Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 52259.600 | 52259.600 | 13064.900 | 313.260 | 0.000 |
| RS | 2 | 4371.300 | 4371.300 | 2185.600 | 52.410 | 0.000 |
| DR*RS | 8 | 7226.200 | 7226.200 | 903.300 | 21.660 | 0.000 |
| Error | 135 | 5630.300 | 5630.300 | 41.700 | | |
| Total | 149 | 69487.400 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 45.904 | |
| FIFO | FBN | 46.859 | |
| RWK | WAIT | 48.965 | |
| RWK | RV | 49.175 | |
| FIFO | WAIT | 51.016 | |
| FIFO | RV | 51.461 | |
| CR | FBN | 69.452 | |
| EDD | FBN | 70.816 | |
| EDD | WAIT | 73.291 | |
| EDD | RV | 74.552 | |
| CR | WAIT | 74.894 | |
| CR | RV | 82.243 | |
| SPT | WAIT | 83.523 | |
| SPT | FBN | 87.241 | |
| SPT | RV | 124.948 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 48.015 | |
| FIFO | 49.779 | |
| EDD | 72.886 | |
| CR | 75.530 | |
| SPT | 98.571 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 64.055 | |
| WAIT | 66.338 | |
| RV | 76.476 | |

Table G.15. ANOVA and Tukey Tests for Percentage On Time at Ten Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 117015.100 | 117015.100 | 29253.800 | 1041.070 | 0.000 |
| RS | 2 | 12313.400 | 12313.400 | 6156.700 | 219.100 | 0.000 |
| DR*RS | 8 | 1275.400 | 1275.400 | 159.400 | 5.670 | 0.000 |
| Error | 135 | 3793.500 | 3793.500 | 28.100 | | |
| Total | 149 | 134397.400 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 97.868 | |
| FIFO | FBN | 96.280 | |
| RWK | WAIT | 94.961 | |
| FIFO | WAIT | 88.507 | |
| RWK | RV | 83.760 | |
| EDD | FBN | 80.476 | |
| SPT | FBN | 72.280 | |
| EDD | WAIT | 70.636 | |
| FIFO | RV | 68.874 | |
| SPT | WAIT | 67.166 | |
| EDD | RV | 63.173 | |
| SPT | RV | 48.732 | |
| CR | FBN | 27.707 | |
| CR | WAIT | 10.476 | |
| CR | RV | 0.000 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 92.196 | |
| FIFO | 84.554 | |
| EDD | 71.428 | |
| SPT | 62.726 | |
| CR | 12.728 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 74.922 | |
| WAIT | 66.349 | |
| RV | 52.908 | |

Table G.16. ANOVA and Tukey Tests for Percent Idle at Ten Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 0.712 | 0.712 | 0.178 | 280.130 | 0.000 |
| RS | 2 | 38.516 | 38.516 | 19.258 | 30000.000 | 0.000 |
| DR*RS | 8 | 0.080 | 0.080 | 0.010 | 15.760 | 0.000 |
| Error | 135 | 0.086 | 0.086 | 0.001 | | |
| Total | 149 | 39.394 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| SPT | WAIT | 70.224 | |
| CR | WAIT | 70.154 | |
| EDD | WAIT | 70.142 | |
| FIFO | WAIT | 70.067 | |
| RWK | WAIT | 70.059 | |
| CR | RV | 69.889 | |
| SPT | RV | 69.860 | |
| EDD | RV | 69.773 | |
| FIFO | RV | 69.681 | |
| RWK | RV | 69.679 | |
| SPT | FBN | 69.033 | |
| EDD | FBN | 68.941 | |
| CR | FBN | 68.931 | |
| FIFO | FBN | 68.858 | |
| RWK | FBN | 68.848 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| SPT | 69.706 | |
| CR | 69.658 | |
| EDD | 69.619 | |
| FIFO | 69.535 | |
| RWK | 69.529 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| WAIT | 70.129 | |
| RV | 69.776 | |
| FBN | 68.922 | |

Table G.17. ANOVA and Tukey Tests for Average WIP at Ten Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 18634.900 | 18634.900 | 4658.700 | 1304.600 | 0.000 |
| RS | 2 | 6801.500 | 6801.500 | 3400.700 | 952.320 | 0.000 |
| DR*RS | 8 | 5684.900 | 5684.900 | 710.600 | 198.990 | 0.000 |
| Error | 135 | 482.100 | 482.100 | 3.600 | | |
| Total | 149 | 31603.300 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 134.607 | |
| FIFO | FBN | 136.649 | |
| RWK | WAIT | 138.666 | |
| EDD | FBN | 141.474 | |
| FIFO | WAIT | 141.796 | |
| RWK | RV | 142.220 | |
| EDD | WAIT | 145.220 | |
| SPT | FBN | 145.233 | |
| FIFO | RV | 145.944 | |
| SPT | WAIT | 147.710 | |
| EDD | RV | 147.832 | |
| CR | FBN | 154.339 | |
| CR | WAIT | 159.162 | |
| SPT | RV | 159.724 | |
| CR | RV | 195.943 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 138.498 | |
| FIFO | 141.463 | |
| EDD | 144.842 | |
| SPT | 150.889 | |
| CR | 169.815 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 142.460 | |
| WAIT | 146.511 | |
| RV | 158.333 | |

Table G.18. ANOVA and Tukey Tests for Average XT at Ten Percent Rework

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 4 | 2.475 | 2.475 | 0.619 | 1274.070 | 0.000 |
| RS | 2 | 0.845 | 0.845 | 0.423 | 870.110 | 0.000 |
| DR*RS | 8 | 0.772 | 0.772 | 0.097 | 198.790 | 0.000 |
| Error | 135 | 0.066 | 0.066 | 0.000 | | |
| Total | 149 | 4.158 | | | | |

| DR | RS | Avg. CT | Significance |
|---|---|---|---|
| RWK | FBN | 1.585 | |
| FIFO | FBN | 1.607 | |
| RWK | WAIT | 1.617 | |
| FIFO | WAIT | 1.652 | |
| EDD | FBN | 1.654 | |
| RWK | RV | 1.662 | |
| EDD | WAIT | 1.683 | |
| FIFO | RV | 1.704 | |
| SPT | FBN | 1.704 | |
| EDD | RV | 1.717 | |
| SPT | WAIT | 1.719 | |
| CR | FBN | 1.811 | |
| CR | WAIT | 1.847 | |
| SPT | RV | 1.859 | |
| CR | RV | 2.282 | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 1.621 | |
| FIFO | 1.654 | |
| EDD | 1.685 | |
| SPT | 1.761 | |
| CR | 1.980 | |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 1.672 | |
| WAIT | 1.704 | |
| RV | 1.845 | |

## Appendix H. Two Factor MTO ANOVA Tables: Determination of Robust Strategies

The following tables show the ANOVA and Tukey multiple comparison test results for the tests of the six strategies found to perform well across performance measures, rework level in the MTO fab. Tukey multiple comparison tests are done for the factors that were considered significant.

Table H.1. Average Cycle Time ANOVA Table and Tukey Multiple Comparison Test

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 1 | 204.800 | 204.800 | 204.800 | 43.370 | 0.000 |
| RS | 2 | 2685.900 | 2685.900 | 1342.900 | 284.340 | 0.000 |
| DR*RS | 2 | 17.700 | 17.700 | 8.800 | 1.870 | 0.157 |
| RL | 2 | 27860.800 | 27860.800 | 13930.400 | 2949.490 | 0.000 |
| DR*RL | 2 | 263.600 | 263.600 | 131.800 | 27.910 | 0.000 |
| RS*RL | 4 | 2179.100 | 2179.100 | 544.800 | 115.350 | 0.000 |
| Error | 166 | 784.000 | 784.000 | 4.700 | | |
| Total | 179 | 33996.000 | | | | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 338.304 | I |
| FIFO | 340.438 | I |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 334.095 | I |
| WAIT | 340.781 | I |
| RV | 343.237 | I |

Table H.2. Standard Deviation of Cycle Time ANOVA Table and Tukey Multiple Comparison Test

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 1 | 14.310 | 14.310 | 14.310 | 20.480 | 0.000 |
| RS | 2 | 329.220 | 329.220 | 164.610 | 235.560 | 0.000 |
| DR*RS | 2 | 1.180 | 1.180 | 0.590 | 0.850 | 0.431 |
| RL | 2 | 2605.730 | 2605.730 | 1302.860 | 1864.470 | 0.000 |
| DR*RL | 2 | 20.250 | 20.250 | 10.120 | 14.490 | 0.000 |
| RS*RL | 4 | 305.590 | 305.590 | 76.400 | 109.330 | 0.000 |
| Error | 166 | 116.000 | 116.000 | 0.700 | | |
| Total | 179 | 3392.280 | | | | |

| DR | Std. Dev CT | Sig. |
|---|---|---|
| RWK | 83.320 | I |
| FIFO | 83.884 | I |

| RS | Std. Dev CT | Sig. |
|---|---|---|
| FBN | 82.402 | I |
| WAIT | 82.912 | I |
| RV | 85.492 | I |

Table H.3. Percentage On Time ANOVA Table and Tukey Multiple Comparison Test

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 1 | 142.790 | 142.790 | 142.790 | 9.810 | 0.002 |
| RS | 2 | 2065.510 | 2065.510 | 1032.750 | 70.950 | 0.000 |
| DR*RS | 2 | 62.010 | 62.010 | 31.000 | 2.130 | 0.122 |
| RL | 2 | 677.880 | 677.880 | 338.940 | 23.290 | 0.000 |
| DR*RL | 2 | 207.440 | 207.440 | 103.720 | 7.130 | 0.001 |
| RS*RL | 4 | 2456.390 | 2456.390 | 614.100 | 42.190 | 0.000 |
| Error | 166 | 2416.170 | 2416.170 | 14.560 | | |
| Total | 179 | 8028.190 | | | | |

| DR | % On Time | Sig. |
|---|---|---|
| RWK | 93.130 | I |
| FIFO | 91.349 | I |

| RS | % On Time | Sig. |
|---|---|---|
| FBN | 96.039 | I |
| WAIT | 92.867 | I |
| RV | 87.813 | I |

Table H.4. Average WIP ANOVA Table and Tukey Multiple Comparison Test

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 1 | 63.390 | 63.390 | 63.390 | 43.570 | 0.000 |
| RS | 2 | 831.440 | 831.440 | 415.720 | 285.700 | 0.000 |
| DR*RS | 2 | 5.440 | 5.440 | 2.720 | 1.870 | 0.157 |
| RL | 2 | 8621.890 | 8621.890 | 4310.950 | 2962.670 | 0.000 |
| DR*RL | 2 | 81.580 | 81.580 | 40.790 | 28.030 | 0.000 |
| RS*RL | 4 | 674.420 | 674.420 | 168.600 | 115.870 | 0.000 |
| Error | 166 | 241.540 | 241.540 | 1.460 | | |
| Total | 179 | 10519.710 | | | | |

| DR | Avg. WIP | Sig. |
|---|---|---|
| RWK | 188.201 | ▌ |
| FIFO | 189.388 | ▌ |

| RS | Avg. WIP | Sig. |
|---|---|---|
| FBN | 185.860 | ▌ |
| WAIT | 189.578 | ▌ |
| RV | 190.946 | ▌ |

Table H.5. Average XT ANOVA Table and Tukey Multiple Comparison Test

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 1 | 0.005 | 0.005 | 0.005 | 48.590 | 0.000 |
| RS | 2 | 0.030 | 0.030 | 0.015 | 158.880 | 0.000 |
| DR*RS | 2 | 0.000 | 0.000 | 0.000 | 1.450 | 0.238 |
| RL | 2 | 0.587 | 0.587 | 0.293 | 3100.040 | 0.000 |
| DR*RL | 2 | 0.005 | 0.005 | 0.002 | 24.320 | 0.000 |
| RS*RL | 4 | 0.031 | 0.031 | 0.008 | 82.930 | 0.000 |
| Error | 166 | 0.016 | 0.016 | 0.000 | | |
| Total | 179 | 0.674 | | | | |

| DR | Avg. XT | Sig. |
|---|---|---|
| RWK | 1.497 | ▌ |
| FIFO | 1.507 | ▌ |

| RS | Avg. XT | Sig. |
|---|---|---|
| FBN | 1.485 | ▌ |
| WAIT | 1.506 | ▌ |
| RV | 1.516 | ▌ |

## Appendix I. Two Factor MTS ANOVA Tables: Determination of Robust Strategies

The following tables show the ANOVA and Tukey multiple comparison test results for the tests of the six strategies found to perform well across performance measures, rework level in the MTS fab. Tukey multiple comparison tests are done for the factors that were considered significant.

Table I.1. Average Cycle Time ANOVA Table and Tukey Multiple Comparison Test

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 1 | 604.500 | 604.500 | 604.500 | 52.590 | 0.000 |
| RS | 2 | 4196.700 | 4196.700 | 2098.400 | 182.560 | 0.000 |
| DR*RS | 2 | 31.500 | 31.500 | 15.700 | 1.370 | 0.257 |
| RL | 2 | 65743.900 | 65743.900 | 32871.900 | 2859.890 | 0.000 |
| DR*RL | 2 | 625.400 | 625.400 | 312.700 | 27.200 | 0.000 |
| RS*RL | 4 | 3164.900 | 3164.900 | 791.200 | 68.840 | 0.000 |
| Error | 166 | 1908.000 | 1908.000 | 11.500 | | |
| Total | 179 | 76274.800 | | | | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 388.955 | ▌ |
| FIFO | 392.620 | ▌ |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 384.162 | ▌ |
| WAIT | 392.668 | ▌ |
| RV | 395.531 | ▌ |

Table I.2. Standard Deviation of Cycle Time ANOVA Table and Tukey Multiple Comparison Test

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 1 | 21.060 | 21.060 | 21.060 | 15.060 | 0.000 |
| RS | 2 | 154.150 | 154.150 | 77.080 | 55.130 | 0.000 |
| DR*RS | 2 | 2.030 | 2.030 | 1.010 | 0.720 | 0.486 |
| RL | 2 | 1846.830 | 1846.830 | 923.420 | 660.540 | 0.000 |
| DR*RL | 2 | 27.180 | 27.180 | 13.590 | 9.720 | 0.000 |
| RS*RL | 4 | 92.300 | 92.300 | 23.070 | 16.510 | 0.000 |
| Error | 166 | 232.060 | 232.060 | 1.400 | | |
| Total | 179 | 2375.610 | | | | |

| DR | Std. Dev CT | Sig. |
|---|---|---|
| RWK | 44.163 | ▌ |
| FIFO | 44.847 | ▌ |

| RS | Std. Dev CT | Sig. |
|---|---|---|
| FBN | 43.225 | ▌ |
| RV | 45.380 | ▌ |
| WAIT | 44.910 | ▌ |

Table I.3. Percentage On Time ANOVA Table and Tukey Multiple Comparison Test

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| DR | 1 | 403.440 | 403.440 | 403.440 | 20.990 | 0.000 |
| RS | 2 | 2211.910 | 2211.910 | 1105.960 | 57.540 | 0.000 |
| DR*RS | 2 | 175.670 | 175.670 | 87.830 | 4.570 | 0.012 |
| RL | 2 | 882.790 | 882.790 | 441.400 | 22.960 | 0.000 |
| DR*RL | 2 | 494.380 | 494.380 | 247.190 | 12.860 | 0.000 |
| RS*RL | 4 | 2663.670 | 2663.670 | 665.920 | 34.650 | 0.000 |
| Error | 166 | 3190.620 | 3190.620 | 19.220 | | |
| Total | 179 | 10022.480 | | | | |

| DR | % On Time | Sig. |
|---|---|---|
| RWK | 92.930 | ▌ |
| FIFO | 89.936 | ▌ |

| RS | % On Time | Sig. |
|---|---|---|
| FBN | 95.484 | ▌ |
| WAIT | 91.882 | ▌ |
| RV | 86.933 | ▌ |

Table I.4. Average WIP ANOVA Table and Tukey Multiple Comparison Test

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 1 | 68.070 | 68.070 | 68.070 | 52.540 | 0.000 |
| **RS** | 2 | 473.050 | 473.050 | 236.520 | 182.550 | 0.000 |
| **DR*RS** | 2 | 3.550 | 3.550 | 1.780 | 1.370 | 0.257 |
| **RL** | 2 | 7408.780 | 7408.780 | 3704.390 | 2859.080 | 0.000 |
| **DR*RL** | 2 | 70.490 | 70.490 | 35.250 | 27.200 | 0.000 |
| **RS*RL** | 4 | 356.630 | 356.630 | 89.160 | 68.810 | 0.000 |
| **Error** | 166 | 215.080 | 215.080 | 1.300 | | |
| **Total** | **179** | **8595.650** | | | | |

| DR | Avg. WIP | Sig. |
|---|---|---|
| RWK | 130.561 | ▌ |
| FIFO | 131.791 | ▌ |

| RS | Avg. WIP | Sig. |
|---|---|---|
| FBN | 128.952 | ▌ |
| WAIT | 131.808 | ▌ |
| RV | 132.769 | ▌ |

Table I.5. Average XT ANOVA Table and Tukey Multiple Comparison Test

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 1 | 0.009 | 0.009 | 0.009 | 48.550 | 0.000 |
| **RS** | 2 | 0.046 | 0.046 | 0.023 | 123.830 | 0.000 |
| **DR*RS** | 2 | 0.001 | 0.001 | 0.000 | 1.630 | 0.199 |
| **RL** | 2 | 1.055 | 1.055 | 0.527 | 2857.070 | 0.000 |
| **DR*RL** | 2 | 0.009 | 0.009 | 0.004 | 23.050 | 0.000 |
| **RS*RL** | 4 | 0.041 | 0.041 | 0.010 | 55.770 | 0.000 |
| **Error** | 166 | 0.031 | 0.031 | 0.000 | | |
| **Total** | **179** | **1.190** | | | | |

| DR | Avg. XT | Sig. |
|---|---|---|
| RWK | 1.526 | ▌ |
| FIFO | 1.540 | ▌ |

| RS | Avg. XT | Sig. |
|---|---|---|
| FBN | 1.512 | ▌ |
| WAIT | 1.538 | ▌ |
| RV | 1.550 | ▌ |

## Appendix J. Two Factor ANOVA and Tukey Analysis to Determine Robust Strategies Overall

This appendix contains the ANOVA and Tukey pairwise comparison tables for the two factor analysis of the strategies that perform well. These strategies are RWK/FBN, FIFO/FBN, RWK/WAIT, FIFO/WAIT, RWK/RV, and FIFO/RV. Based upon the ANOVA results for each performance measure, if the dispatching rule or rework strategy are shown to be significant factors (at a confidence level of 95 percent), the Tukey pairwise comparison test is done on those factors. If the interaction of dispatching rules and rework strategies is shown to be significant at a 95 percent confidence level, the Tukey pairwise comparison test will also be done for the interaction.

Figure J.1. ANOVA and Tukey Results for Average Cycle Time

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| Fab | 1 | 237925.000 | 237925.000 | 237925.000 | 29000.000 | 0.000 |
| DR | 1 | 757.000 | 757.000 | 757.000 | 92.430 | 0.000 |
| Fab*DR | 1 | 53.000 | 53.000 | 53.000 | 6.450 | 0.012 |
| RS | 2 | 6798.000 | 6798.000 | 3399.000 | 415.270 | 0.000 |
| Fab*RS | 2 | 84.000 | 84.000 | 42.000 | 5.160 | 0.006 |
| DR*RS | 2 | 48.000 | 48.000 | 24.000 | 2.940 | 0.054 |
| RL | 2 | 89584.000 | 89584.000 | 44792.000 | 5472.290 | 0.000 |
| DR*RL | 2 | 849.000 | 849.000 | 424.000 | 51.850 | 0.000 |
| RS*RL | 4 | 5294.000 | 5294.000 | 1324.000 | 161.710 | 0.000 |
| Fab*RL | 2 | 4021.000 | 4021.000 | 2011.000 | 245.630 | 0.000 |
| Error | 340 | 2783.000 | 2783.000 | 8.000 | | |
| Total | 359 | 348196.000 | | | | |

| DR | Avg. CT | Sig. |
|---|---|---|
| RWK | 363.629 | I |
| FIFO | 366.529 | I |

| RS | Avg. CT | Sig. |
|---|---|---|
| FBN | 359.128 | I |
| WAIT | 366.725 | I |
| RV | 369.384 | I |

Figure J.2. ANOVA and Tukey Results for St. Deviation of Cycle Time

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| Fab | 1 | 137568.300 | 137568.300 | 137568.300 | 110000.000 | 0.000 |
| DR | 1 | 35.100 | 35.100 | 35.100 | 28.560 | 0.000 |
| Fab*DR | 1 | 0.300 | 0.300 | 0.300 | 0.260 | 0.607 |
| RS | 2 | 343.500 | 343.500 | 171.800 | 139.940 | 0.000 |
| Fab*RS | 2 | 139.900 | 139.900 | 69.900 | 56.980 | 0.000 |
| DR*RS | 2 | 3.100 | 3.100 | 1.600 | 1.270 | 0.281 |
| RL | 2 | 4418.300 | 4418.300 | 2209.100 | 1799.910 | 0.000 |
| DR*RL | 2 | 47.100 | 47.100 | 23.500 | 19.180 | 0.000 |
| RS*RL | 4 | 329.100 | 329.100 | 82.300 | 67.030 | 0.000 |
| Fab*RL | 2 | 34.300 | 34.300 | 17.100 | 13.970 | 0.000 |
| Error | 340 | 417.300 | 417.300 | 1.200 | | |
| Total | 359 | 143336.200 | | | | |

| DR | Std. Dev CT | Sig. |
|---|---|---|
| RWK | 63.741 | I |
| FIFO | 64.365 | I |

| RS | Std. Dev CT | Sig. |
|---|---|---|
| FBN | 62.813 | I |
| WAIT | 64.146 | I |
| RV | 65.201 | I |

Figure J.3. ANOVA and Tukey Results for Percentage On Time

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| Fab | 1 | 58.560 | 58.560 | 58.560 | 3.520 | 0.062 |
| DR | 1 | 513.130 | 513.130 | 513.130 | 30.830 | 0.000 |
| Fab*DR | 1 | 33.100 | 33.100 | 33.100 | 1.990 | 0.159 |
| RS | 2 | 4274.410 | 4274.410 | 2137.200 | 128.420 | 0.000 |
| Fab*RS | 2 | 3.010 | 3.010 | 1.510 | 0.090 | 0.913 |
| DR*RS | 2 | 223.060 | 223.060 | 111.530 | 6.700 | 0.001 |
| RL | 2 | 1550.880 | 1550.880 | 775.440 | 46.600 | 0.000 |
| DR*RL | 2 | 670.140 | 670.140 | 335.070 | 20.130 | 0.000 |
| RS*RL | 4 | 5114.940 | 5114.940 | 1278.740 | 76.840 | 0.000 |
| Fab*RL | 2 | 9.790 | 9.790 | 4.890 | 0.290 | 0.745 |
| Error | 340 | 5658.200 | 5658.200 | 16.640 | | |
| Total | 359 | 18109.220 | | | | |

| DR | RS | % On Time | Sig. |
|---|---|---|---|
| RWK | FBN | 96.019 | |
| FIFO | FBN | 95.504 | |
| RWK | Wait | 93.515 | |
| FIFO | Wait | 91.234 | |
| RWK | RV | 89.556 | |
| FIFO | RV | 85.189 | |

| DR | % On Time | Sig. |
|---|---|---|
| RWK | 93.030 | |
| FIFO | 90.642 | |

| RS | % On Time | Sig. |
|---|---|---|
| FBN | 95.761 | |
| WAIT | 92.374 | |
| RV | 87.373 | |

Figure J.4. ANOVA and Tukey Results for Average WIP

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| Fab | 1 | 298790.000 | 298790.000 | 298790.000 | 210000.000 | 0.000 |
| DR | 1 | 131.000 | 131.000 | 131.000 | 92.490 | 0.000 |
| Fab*DR | 1 | 0.000 | 0.000 | 0.000 | 0.030 | 0.864 |
| RS | 2 | 1279.000 | 1279.000 | 640.000 | 450.190 | 0.000 |
| Fab*RS | 2 | 25.000 | 25.000 | 13.000 | 8.870 | 0.000 |
| DR*RS | 2 | 9.000 | 9.000 | 4.000 | 3.120 | 0.045 |
| RL | 2 | 16005.000 | 16005.000 | 8002.000 | 5632.100 | 0.000 |
| DR*RL | 2 | 152.000 | 152.000 | 76.000 | 53.330 | 0.000 |
| RS*RL | 4 | 1005.000 | 1005.000 | 251.000 | 176.870 | 0.000 |
| Fab*RL | 2 | 26.000 | 26.000 | 13.000 | 9.200 | 0.000 |
| Error | 340 | 483.000 | 483.000 | 1.000 | | |
| Total | 359 | 317906.000 | | | | |

| DR | RS | Avg. WIP | Sig. |
|---|---|---|---|
| RWK | FBN | 157.021 | |
| FIFO | FBN | 157.790 | |
| RWK | Wait | 160.007 | |
| RWK | RV | 161.115 | |
| FIFO | Wait | 161.378 | |
| FIFO | RV | 162.600 | |

| DR | Avg. WIP | Sig. |
|---|---|---|
| RWK | 159.381 | |
| FIFO | 160.590 | |

| RS | Avg. WIP | Sig. |
|---|---|---|
| FBN | 157.406 | |
| WAIT | 160.693 | |
| RV | 161.858 | |

Figure J.5. ANOVA and Tukey Results for Average XT

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| Fab | 1 | 0.085 | 0.085 | 0.085 | 614.870 | 0.000 |
| DR | 1 | 0.013 | 0.013 | 0.013 | 95.210 | 0.000 |
| Fab*DR | 1 | 0.000 | 0.000 | 0.000 | 2.600 | 0.108 |
| RS | 2 | 0.075 | 0.075 | 0.037 | 270.350 | 0.000 |
| Fab*RS | 2 | 0.001 | 0.001 | 0.000 | 2.960 | 0.053 |
| DR*RS | 2 | 0.001 | 0.001 | 0.000 | 3.040 | 0.049 |
| RL | 2 | 1.607 | 1.607 | 0.804 | 5795.810 | 0.000 |
| DR*RL | 2 | 0.013 | 0.013 | 0.006 | 46.020 | 0.000 |
| RS*RL | 4 | 0.072 | 0.072 | 0.018 | 130.120 | 0.000 |
| Fab*RL | 2 | 0.034 | 0.034 | 0.017 | 123.720 | 0.000 |
| Error | 340 | 0.047 | 0.047 | 0.000 | | |
| Total | 359 | 1.949 | | | | |

| DR | RS | Avg. XT | Sig. |
|---|---|---|---|
| RWK | FBN | 1.494 | I |
| FIFO | FBN | 1.502 | I |
| RWK | Wait | 1.515 | I |
| RWK | RV | 1.525 | I |
| FIFO | Wait | 1.529 | I |
| FIFO | RV | 1.540 | I |

| DR | Avg. XT | Sig. |
|---|---|---|
| RWK | 1.512 | I |
| FIFO | 1.524 | I |

| RS | Avg. XT | Sig. |
|---|---|---|
| FBN | 1.498 | I |
| WAIT | 1.522 | I |
| RV | 1.533 | I |

## Appendix K. Fab Description

This appendix contains a description of the dataset used in this research. The dataset is publicly available on the Arizona State University website (Test Beds 2003). There are seven datasets in this test bed, and the dataset used in this research is dataset 3. There are eleven products in this dataset, and the routing for product 9 is on the following pages. The rest of the dataset is in an Excel workbook on a CD is attached to the back cover of the bound thesis. This workbook contains all of the data necessary to build the model used in this research. The database is divided into 14 worksheets. Below is a description of the contents of each worksheet.

**Products:** Contains arrival information for each of the eleven products. The C(?) at the top of the column headings indicates that the distribution used is constant.

**Tools:** Contains information about each of the tools, including the number of quantity of the tool, and the batching information,

**Downtimes & Setups:** Contains downtime data for each of the tool groups, including the mean time to failure and the mean time to repair. This also contains the necessary setup information for each tool. The E(?) at the top of the column headings indicates that the distribution used in exponential.

**1-11:** Contains the routing for each of the eleven products. This includes the load, unload, and processing time. The setup needed at the step is also given, and setups are only done when needed. This means that the setup time will not be incurred if the tool currently has the setup of the lot to be processed. Scrap and rework data is also given. The scrap and rework percentage refers to the percentage of wafers that will be scrapped from each lot. Throughout the data there are lines highlighted in black. These refer to steps that only wafers needing rework go through (rework loop). Wafers not needing rework skip these steps. After wafers needing rework have gone through all of the highlighted steps, they return to the step previous to the highlighting for inspection. It is possible for a reworked wafer to need rework multiple times. Once again, the C(?) in the column headings refers to the constant distribution.

It is important to note that there are some slight changes are made to this dataset. All of the routing information is the same for the MTO and MTS fabs, but the quantity of some of the tools are slightly changed (see table K.1). Also, only products one and five are used in the MTS fab and their changed from 20.81 to 4.16 hours and 17.47 to 10.48 hours, respectively.

Table K.1. Tool Quantity Changes between Fabs

| | Initial Fab | MTO Fab | MTS Fab |
|---|---|---|---|
| Stepper | 13 | 13 | 9 |
| Furnace 3 | 8 | 12 | 8 |
| Furnace 4 | 2 | 2 | 1 |
| Furnace 5 | 2 | 4 | 2 |
| High Implant | 3 | 3 | 2 |
| Med. Implant | 4 | 4 | 3 |

Table K.2. Product 9 Routing

| Step Num | Tool Group Used by Step | Load Time (Hours) C(?) | Processing Time Per-Unit (Hours) C(?) | Processing Time Per-Lot (Hours) C(?) | Processing Time Per-Batch (Hours) C(?) | Batch ID | Unload Time (Hours) C(?) | Setup ID | % of Units Scrapped | % of Units Reworked |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 2 | LIS_Laser_Scribe | 0.0333 | | 0.5000 | | | 0.0333 | | | |
| 3 | PIRH1_Strip | 0.0500 | | 0.1167 | | | | | | |
| 4 | RINS1_Rinse | | | 0.0833 | | | | | | |
| 5 | STI5_Dry_Rinse | 0.0333 | | 0.1333 | | | | | | |
| 6 | FURN5_Furnace_Tube | 0.5833 | | | 4.4667 | 31 | 0.5833 | | | |
| 7 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 8 | CVD5_CVD | 0.0583 | | | 0.2333 | 2 | 0.0583 | | | |
| 9 | AERO_Metrology | 0.0167 | | 0.2500 | | | 0.0167 | | | |
| 10 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 11 | COAT3_Coater | 0.0333 | 0.0250 | | 0.0667 | | 0.0333 | | | |
| 12 | PAL_Photo_Aligner | 0.0667 | 0.0182 | | 0.4667 | | 0.0667 | gpsetup1 | | |
| 13 | DEV_Develop | 0.0167 | 0.0250 | | 0.0333 | | 0.0167 | | | |
| 14 | SCOP2_Metrology | 0.0667 | 0.0020 | | 0.1333 | | 0.0667 | | | 10 |
| 15 | COAT3_Coater | 0.0333 | 0.0250 | | | | 0.0333 | | | |
| 16 | PAL_Photo_Aligner | 0.0667 | 0.0182 | | | | 0.0667 | gpsetup1 | | |
| 17 | DEV_Develop | 0.0167 | 0.0250 | | | | 0.0167 | | | |
| 18 | SCOP2_Metrology | 0.0667 | 0.0020 | | | | 0.0667 | | | |
| 19 | SCOP2_Metrology | 0.0667 | 0.0033 | | | | 0.0667 | | | |
| 20 | ITP_Metrology | 0.0167 | 0.0017 | | | | 0.0167 | | | |
| 21 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 22 | TEG_Dry_Etch | | 0.0287 | | | | 0.1667 | | | |
| 23 | SCOP2_Metrology | 0.0333 | 0.0017 | | | | 0 0333 | | | |
| 24 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 25 | MED_Med_Current_Implant | 0.0333 | 0.0100 | | | | 0.0333 | jtsetup98 | | |
| 26 | | | | | | | | gpsetup4 | | |
| 27 | STI2_Dry_Rinse | 0.0833 | | 0.1333 | | | 0 0833 | | | |
| 28 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 29 | LFE_Asher | 0.0333 | 0.0105 | | | | 0.0833 | | | |
| 30 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 31 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 32 | RINS2_Rinse | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 33 | ESTI_Dryer | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 34 | SCOP2_Metrology | 0.0667 | 0.0033 | | | | 0.0667 | | | |
| 35 | SCOP2_Metrology | 0.0667 | | 0.1667 | | | 0.0667 | | | |
| 36 | VICK_Metrology | 0.0167 | | 0.1250 | | | 0.0167 | | | |
| 37 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 38 | PIRH1_Strip | 0.0500 | | 0.1167 | | | | | | |
| 39 | RINS1_Rinse | | | 0.0833 | | | | | | |
| 40 | STI5_Dry_Rinse | 0.0333 | | 0.1333 | | | | | | |
| 41 | PRPH_Wet_Etch | | | 0.1000 | | | | | | |
| 42 | PRPH_Wet_Etch | | | 0.1000 | | | | | | |
| 43 | STI5_Dry_Rinse | 0.0333 | | 0.1333 | | | | | | |
| 44 | FURN3_Furnace_Tube | 0.5833 | | | 7.4667 | 7 | 0.5833 | | | |
| 45 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 46 | OXIH_Wet_Etch | 0.0333 | | 0.0667 | | | 0.0333 | | | |
| 47 | STI2_Dry_Rinse | 0.0833 | | 0.1333 | | | 0.0833 | | | |
| 48 | NITH_Wet_Etch | 0.0333 | | 0.9167 | | | 0.0333 | | | |
| 49 | NANO_Metrology | 0.0167 | | 0.0833 | | | 0 0333 | | | |
| 50 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0 0333 | | | |
| 51 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0 0333 | | | |
| 52 | RINS2_Rinse | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 53 | ESTI_Dryer | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 54 | SCOP2_Metrology | 0.0333 | | 0.0833 | | | 0.0333 | | | |
| 55 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 56 | MED_Med_Current_Implant | 0.0333 | 0.0100 | | | | 0 0333 | jtsetup99 | | |
| 57 | | | | | | | | gpsetup4 | | |
| 58 | STI2_Dry_Rinse | 0.0833 | | 0.1333 | | | 0.0833 | | | |
| 59 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 60 | COAT3_Coater | 0.0333 | 0.0217 | | 0.0667 | | 0.0333 | | | |

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|---|---|---|---|---|---|---|---|---|---|---|
| 61 | PERK_Photo_Aligner | 0.0167 | 0.0125 | | 0.1000 | | 0.0833 | gpsetup18 | | |
| 62 | DEV_Develop | 0.0167 | 0.0333 | | 0.0333 | | 0.0167 | | | |
| 63 | SCOP2_Metrology | 0.0667 | 0.0030 | | 0.1333 | | 0.0667 | | | 5.3 |
| 64 | COAT3_Coater | 0.0333 | 0.0217 | | | | 0.0333 | | | |
| 65 | PERK_Photo_Aligner | 0.0167 | 0.0125 | | | | 0.0833 | gpsetup18 | | |
| 66 | DEV_Develop | 0.0167 | 0.0333 | | | | 0.0167 | | | |
| 67 | SCOP2_Metrology | 0.0667 | 0.0030 | | | | 0.0667 | | | |
| 68 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 69 | MTRX_Descum | 0.0333 | 0.0208 | | | | 0.0333 | | | |
| 70 | OXIH_Wet_Etch | 0.0333 | | 0.0667 | | | 0.3333 | | | |
| 71 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 72 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 73 | RINS2_Rinse | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 74 | ESTI_Dryer | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 75 | SCOP2_Metrology | 0.0333 | | 0.1667 | | | 0.0333 | | | |
| 76 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 77 | PIRH1_Strip | 0.0500 | | 0.1167 | | | | | | |
| 78 | RINS1_Rinse | | | 0.0833 | | | | | | |
| 79 | STI5_Dry_Rinse | 0.0333 | | 0.1333 | | | | | | |
| 80 | PRPH_Wet_Etch | | | 0.1000 | | | | | | |
| 81 | PRPH_Wet_Etch | | | 0.1000 | | | | | | |
| 82 | STI5_Dry_Rinse | 0.0333 | | 0.2000 | | | | | | |
| 83 | CVD4_CVD | 0.0417 | | | 0.3333 | 32 | 0.0417 | | | |
| 84 | SCOP1_Metrology | | | 0.0083 | | | | | | |
| 85 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 86 | PHOS_Furnace_Tube | 0.4167 | | | 2.8000 | 33 | 0.4167 | | | |
| 87 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 88 | STI5_Dry_Rinse | 0.0333 | | 0.1333 | | | | | | |
| 89 | PIRH1_Strip | 0.0500 | | 0.1167 | | | | | | |
| 90 | RINS1_Rinse | | | 0.0833 | | | | | | |
| 91 | STI5_Dry_Rinse | 0.0333 | | 0.1333 | | | | | | |
| 92 | CVD1_CVD | 0.0417 | | | 0.3167 | 34 | 0.0417 | | | |
| 93 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 94 | COAT3_Coater | 0.0333 | 0.0217 | | 0.0667 | | 0.0333 | | | |
| 95 | PAL_Photo_Aligner | 0.0167 | 0.0333 | | 0.4333 | | 0.0833 | gpsetup8 | | |
| 96 | DEV_Develop | 0.0167 | 0.0250 | | 0.0333 | | 0.0167 | | | |
| 97 | SCOP2_Metrology | 0.0667 | 0.0012 | | 0.1333 | | 0.0667 | | | 6.8 |
| 98 | COAT3_Coater | 0.0333 | 0.0217 | | | | 0.0333 | | | |
| 99 | PAL_Photo_Aligner | 0.0167 | 0.0333 | | | | 0.0833 | gpsetup8 | | |
| 100 | DEV_Develop | 0.0167 | 0.0250 | | | | 0.0167 | | | |
| 101 | SCOP2_Metrology | 0.0667 | 0.0012 | | | | 0.0667 | | | |
| 102 | ITP_Metrology | 0.0167 | 0.0083 | | | | 0.0167 | | | |
| 103 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 104 | OLAM_Dry_Etch | | 0.0350 | | | | 0.7500 | | | |
| 105 | SCOP2_Metrology | 0.0667 | 0.0033 | | | | 0.0667 | | | |
| 106 | LFE_Asher | 0.0167 | 0.0070 | | | | 0.0167 | | | |
| 107 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 108 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 109 | RINS2_Rinse | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 110 | ESTI_Dryer | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 111 | VICK_Metrology | 0.0167 | | 0.0833 | | | 0.0167 | | | |
| 112 | SCOP2_Metrology | 0.0333 | | 0.1667 | | | 0.0333 | | | |
| 113 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 114 | XLAM_Dry_Etch | | 0.0333 | | | | 0.1667 | | 0.4 | |
| 115 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 116 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 117 | RINS2_Rinse | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 118 | ESTI_Dryer | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 119 | SCOP2_Metrology | 0.0333 | | 0.1667 | | | 0.0333 | | | |
| 120 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 121 | MED_Med_Current_Implant | 0.0333 | 0.0100 | | | | 0.0333 | jtsetup100 | | |
| 122 | | | | | | | | gpsetup4 | | |
| 123 | STI2_Dry_Rinse | 0.0833 | | 0.1333 | | | 0.0833 | | | |
| 124 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 125 | PIRH1_Strip | 0.0500 | | 0.1167 | | | | | | |

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|---|---|---|---|---|---|---|---|---|---|---|
| 126 | RINS1_Rinse | | | 0.0833 | | | | | | |
| 127 | STI5_Dry_Rinse | 0.0333 | | 0.1333 | | | | | | |
| 128 | PRPH_Wet_Etch | | | 0.1000 | | | | | | |
| 129 | PRPH_Wet_Etch | | | 0.1000 | | | | | | |
| 130 | STI5_Dry_Rinse | 0.0333 | | 0.1333 | | | | | | |
| 131 | FURN3_Furnace_Tube | 0.5833 | | | 3.7417 | 26 | 0.5833 | | | |
| 132 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 133 | MED_Med_Current_Implant | 0.0333 | 0.0100 | | | | 0.0333 | jtsetup101 | | |
| 134 | | | | | | | | gpsetup2 | | |
| 135 | STI2_Dry_Rinse | 0.0833 | | 0.1333 | | | 0.0833 | | | |
| 136 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 137 | PIRH1_Strip | 0.0500 | | 0.1167 | | | | | | |
| 138 | RINS1_Rinse | | | 0.0833 | | | | | | |
| 139 | STI5_Dry_Rinse | 0.0333 | | 0.1333 | | | | | | |
| 140 | CVD1_CVD | 0.0333 | | | 0.2917 | 35 | 0.0333 | | | |
| 141 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 142 | FURN3_Furnace_Tube | 0.5833 | | | 4.0833 | 13 | 0.5833 | | | |
| 143 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 144 | OLAM_Dry_Etch | | 0.0283 | | | | 0.2500 | | | |
| 145 | LFE_Asher | 0.0167 | 0.0053 | | | | 0.0167 | | | |
| 146 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 147 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 148 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 149 | RINS2_Rinse | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 150 | ESTI_Dryer | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 151 | OXIH_Wet_Etch | 0.0333 | | 0.0667 | | | 0.0333 | | | |
| 152 | ESTI_Dryer | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 153 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 154 | HIGH_High_Current_Implant | 0.0667 | 0.0533 | | | | 0.0667 | jtsetup102 | | |
| 155 | | | | | | | | gpsetup3 | | |
| 156 | TERM_Computer_terminal | | 0.0125 | | | | | | | |
| 157 | PIRH1_Strip | 0.0500 | | 0.1167 | | | | | | |
| 158 | RINS1_Rinse | | | 0.0833 | | | | | | |
| 159 | STI5_Dry_Rinse | 0.0333 | | 0.1333 | | | | | | |
| 160 | PRPH_Wet_Etch | | | 0.1000 | | | | | | |
| 161 | PRPH_Wet_Etch | | | 0.1000 | | | | | | |
| 162 | STI5_Dry_Rinse | 0.0333 | | 0.1333 | | | | | | |
| 163 | CVD5_CVD | 0.0583 | | | 0.1950 | 36 | 0.0583 | | | |
| 164 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 165 | FURN3_Furnace_Tube | 0.5833 | | | 3.0833 | 37 | 0.5833 | | | |
| 166 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 167 | CVD4_CVD | 0.0583 | | | 0.2783 | 16 | 0.0583 | | | |
| 168 | SCOP1_Metrology | | | 0.0117 | | | | | | |
| 169 | TERM_Computer_terminal | | | 0.0125 | | | | | 0.2 | |
| 170 | PHOS_Furnace_Tube | 0.4167 | | | 3.3067 | 17 | 0.4167 | | | |
| 171 | FSI_Clean | 0.0333 | | 0.5833 | | | 0.0333 | | | |
| 172 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 173 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 174 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 175 | RINS2_Rinse | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 176 | ESTI_Dryer | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 177 | COAT3_Coater | 0.0167 | 0.0375 | | 0.0333 | | 0.0167 | | | |
| 178 | PERK_Photo_Aligner | 0.0167 | 0.0292 | | 0.4333 | | 0.0833 | gpsetup10 | | |
| 179 | DEV_Develop | 0.0167 | 0.0417 | | 0.0333 | | 0.0167 | | | |
| 180 | SCOP2_Metrology | 0.0667 | 0.0020 | | 0.1333 | | 0.0667 | | | 4.5 |
| 181 | COAT3_Coater | 0.0167 | 0.0375 | | | | 0.0167 | | | |
| 182 | PERK_Photo_Aligner | 0.0167 | 0.0292 | | | | 0.0833 | gpsetup10 | | |
| 183 | DEV_Develop | 0.0167 | 0.0417 | | | | 0.0167 | | | |
| 184 | SCOP2_Metrology | 0.0667 | 0.0020 | | | | 0.0667 | | | |
| 185 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 186 | MTRX_Descum | 0.0333 | 0.0208 | | | | 0.0333 | | | |
| 187 | POLH_Wet_Etch | 0.0167 | | 0.2500 | | | 0.3333 | | | |
| 188 | SCOP2_Metrology | 0.0333 | 0.0017 | | | | 0.0333 | | | |
| 189 | OXIH_Wet_Etch | 0.0333 | | 0.0667 | | | 0.0333 | | | |
| 190 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |

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|---|---|---|---|---|---|---|---|---|---|---|
| 191 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 192 | RINS2_Rinse | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 193 | ESTI_Dryer | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 194 | NITH_Wet_Etch | 0.0333 | | 0.4167 | | | 0.0333 | | | |
| 195 | SCOP2_Metrology | 0.0667 | 0.0067 | | | | 0.0667 | | | |
| 196 | SCOP2_Metrology | 0.0333 | | 0.1667 | | | 0.0333 | | | |
| 197 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 198 | PIRH1_Strip | 0.0500 | | 0.1167 | | | | | | |
| 199 | RINS1_Rinse | | | 0.0833 | | | | | | |
| 200 | STI5_Dry_Rinse | 0.0333 | | 0.1333 | | | | | | |
| 201 | CVD1_CVD | 0.0333 | | | 0.2217 | 18 | 0.0333 | | | |
| 202 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 203 | WATJ_Metal_Dep | | | 1.6667 | | | | | | |
| 204 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 205 | DEGH_Deglaze | 0.0333 | | 0.2700 | | | 0.0333 | | | |
| 206 | DEGH_Deglaze | | | 0.0833 | | | | | | |
| 207 | PIRH1_Strip | 0.0500 | | 0.1167 | | | | | | |
| 208 | RINS1_Rinse | | | 0.0833 | | | | | | |
| 209 | STI5_Dry_Rinse | 0.0333 | | 0.1333 | | | | | | |
| 210 | FURN4_Furnace_Tube | 0.5833 | | | 3.7667 | 38 | 0.5833 | | | |
| 211 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 212 | COAT5_Coater | 0.0333 | 0.0305 | | | | 0.0333 | | | |
| 213 | OLAM_Dry_Etch | 0.0833 | 0.0383 | | | | 0.2833 | | | |
| 214 | NANO_Metrology | 0.0083 | 0.0250 | | | | 0.0083 | | | |
| 215 | SCOP2_Metrology | 0.0333 | 0.0017 | | | | 0.0333 | | | |
| 216 | LFE_Asher | 0.0167 | 0.0053 | | | | 0.0167 | | | |
| 217 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 218 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 219 | RINS2_Rinse | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 220 | ESTI_Dryer | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 221 | SCOP2_Metrology | 0.0333 | | 0.0500 | | | 0.0333 | | | |
| 222 | TERM_Computer_terminal | | | 0.0125 | | | | | 0.2 | |
| 223 | COAT3_Coater | 0.0167 | 0.0250 | | 0.0333 | | 0.0167 | | | |
| 224 | PERK_Photo_Aligner | 0.0333 | 0.0333 | | 0.4500 | | 0.0833 | gpsetup25 | | |
| 225 | DEV_Develop | 0.0083 | 0.0333 | | 0.0167 | | 0.0083 | | | |
| 226 | SCOP2_Metrology | 0.0667 | 0.0020 | | 0.1333 | | 0.0667 | | | 8.3 |
| 227 | COAT3_Coater | 0.0167 | 0.0250 | | | | 0.0167 | | | |
| 228 | PERK_Photo_Aligner | 0.0333 | 0.0333 | | | | 0.0833 | gpsetup25 | | |
| 229 | DEV_Develop | 0.0083 | 0.0333 | | | | 0.0083 | | | |
| 230 | SCOP2_Metrology | 0.0667 | 0.0020 | | | | 0.0667 | | | |
| 231 | ITP_Metrology | 0.0167 | 0.0083 | | | | 0.0167 | | | |
| 232 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 233 | MTRX_Descum | 0.0500 | 0.0192 | | | | 0.0333 | | | |
| 234 | OXIH_Wet_Etch | 0.0333 | | 0.0667 | | | 0.3333 | | | |
| 235 | OLAM_Dry_Etch | | 0.0650 | | | | 0.1667 | | | |
| 236 | SCOP2_Metrology | 0.0333 | 0.0017 | | | | 0.0333 | | | |
| 237 | LFE_Asher | 0.0167 | 0.0053 | | | | 0.0167 | | | |
| 238 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 239 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 240 | RINS2_Rinse | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 241 | ESTI_Dryer | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 242 | VICK_Metrology | 0.0167 | | 0.0833 | | | 0.0167 | | | |
| 243 | SCOP2_Metrology | 0.0667 | | 0.1667 | | | 0.0667 | | | |
| 244 | SCOP2_Metrology | 0.0333 | | 0.0500 | | | 0.0333 | | | |
| 245 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 246 | MED_Med_Current_Implant | 0.0333 | 0.0100 | | | | 0.0333 | jtsetup103 | | |
| 247 | | | | | | | | gpsetup2 | | |
| 248 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 249 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 250 | PIRH2_Strip | 0.0333 | | 0.1167 | | | 0.0333 | | | |
| 251 | RINS2_Rinse | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 252 | ESTI_Dryer | 0.0333 | | 0.1333 | | | 0.0333 | | | |
| 253 | PRMH_Rinse | 0.0833 | | 0.1667 | | | 0.0833 | | | |
| 254 | STI6_Dry_Rinse | 0.0833 | | 0.1667 | | | 0.0833 | | | |
| 255 | METL_Metal_Dep | 0.0167 | 0.0200 | | | | 0.0167 | | | |

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|---|---|---|---|---|---|---|---|---|---|---|
| 256 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 257 | COAT3_Coater | 0.0333 | 0.0350 | | 0.0667 | | 0.0333 | | | |
| 258 | PERK_Photo_Aligner | 0.0167 | 0.0417 | | 0.4000 | | 0.0500 | gpsetup26 | | |
| 259 | DEV_Develop | 0.0042 | 0.0525 | | 0.0083 | | 0.0042 | | | |
| 260 | SCOP2_Metrology | 0.0833 | 0.0180 | | 0.1667 | | 0.0833 | | | 16 |
| 261 | COAT3_Coater | 0.0333 | 0.0350 | | | | 0.0333 | | | |
| 262 | PERK_Photo_Aligner | 0.0167 | 0.0417 | | | | 0.0500 | gpsetup26 | | |
| 263 | DEV_Develop | 0.0042 | 0.0525 | | | | 0.0042 | | | |
| 264 | SCOP2_Metrology | 0.0833 | 0.0180 | | | | 0.0833 | | | |
| 265 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 266 | MLAM_Dry_Etch | | 0.0867 | | | | 0.2500 | | | |
| 267 | SCOP2_Metrology | 0.0333 | 0.0017 | | | | 0.0333 | | 1 | |
| 268 | STRP_Strip | | | 0.5833 | | | | | | |
| 269 | LFE_Asher | 0.0167 | 0.0122 | | | | 0.0167 | | | |
| 270 | SCOP2_Metrology | 0.0833 | | 0.1667 | | | 0.0833 | | | |
| 271 | VICK_Metrology | 0.0167 | | 0.1250 | | | 0.0167 | | | |
| 272 | SCOP2_Metrology | 0.0333 | | 0.0500 | | | 0.0333 | | | |
| 273 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 274 | STI4_Dry_Rinse | | | 0.1667 | | | | | | |
| 275 | FURN2_Furnace_Tube | 0.3333 | | | 2.3333 | 39 | 0.3333 | | | |
| 276 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 277 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 278 | STI4_Dry_Rinse | | | 0.1667 | | | | | | |
| 279 | CVD2_CVD | 0.3333 | | 1.1833 | | | 0.3333 | | | |
| 280 | CVD2_CVD | 0.3333 | | 1.2333 | | | 0.3333 | | | |
| 281 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 282 | COAT2_Coater | 0.0333 | 0.0350 | | 0.0667 | | 0.0333 | | | |
| 283 | PERK_Photo_Aligner | 0.0167 | 0.0188 | | 0.3667 | | 0.0167 | gpsetup15 | | |
| 284 | DEV_Develop | 0.0167 | 0.0220 | | 0.0333 | | 0.0167 | | | |
| 285 | SCOP2_Metrology | 0.0667 | 0.0013 | | 0.1333 | | 0.0667 | | | 0.8 |
| 286 | COAT2_Coater | 0.0333 | 0.0350 | | | | 0.0333 | | | |
| 287 | PERK_Photo_Aligner | 0.0167 | 0.0188 | | | | 0.0167 | gpsetup15 | | |
| 288 | DEV_Develop | 0.0167 | 0.0220 | | | | 0.0167 | | | |
| 289 | SCOP2_Metrology | 0.0667 | 0.0013 | | | | 0.0667 | | | |
| 290 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 291 | OLAM_Dry_Etch | | 0.0667 | | | | 0.1667 | | | |
| 292 | SCOP2_Metrology | 0.0333 | 0.0017 | | | | 0.0333 | | | |
| 293 | LFE_Asher | 0.0167 | 0.0070 | | | | 0.0167 | | | |
| 294 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 295 | COAT1_Coater | 0.0333 | 0.0217 | | | | 0.0333 | | | |
| 296 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 297 | BAGR_Backgrind | 0.0333 | | 0.5333 | | | 0.0333 | | | |
| 298 | HOOD_Rinse | 0.0167 | | 0.2500 | | | 0.0167 | | | |
| 299 | HOOD_Rinse | | | 0.3000 | | | | | | |
| 300 | STI3_Dry_Rinse | 0.0833 | | 0.2500 | | | 0.0833 | | | |
| 301 | TUBE_Alloy | 0.0167 | | | 0.8250 | 21 | 0.0167 | | | |
| 302 | TERM_Computer_terminal | | | 0.0125 | | | | | | |
| 303 | PR1_Probe | 0.1167 | 0.1667 | | | | 0.1167 | | | |
| 304 | PR1_Probe | 0.0833 | | 0.6000 | | | 0.0833 | | | |


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CD-R
80Min 700MB