Investigations on thin film polysilicon MOSFETs with Si-Ge ion implanted channels

Luigi Ternullo

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Investigations on Thin Film Polysilicon MOSFETs with Si-Ge Ion Implanted Channels

by

Luigi Ternullo, Jr.
Investigations on Thin Film Polysilicon
MOSFETs with Si-Ge Ion Implanted Channels

by

Luigi Ternullo Jr.

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DEPARTMENT OF ELECTRICAL ENGINEERING

COLLEGE OF ENGINEERING

ROCHESTER INSTITUTE OF TECHNOLOGY

ROCHESTER, NEW YORK

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Investigations on Thin Film Polysilicon MOSFETs with Si-Ge Ion Implanted Channels

by

Luigi Ternullo, Jr.

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Luigi Ternullo, Jr.

November 15, 1992
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Preface

Polysilicon Thin Film Transistors (TFT) technology has received much attention lately in applications requiring electronic devices to be fabricated over large areas, namely active matrix liquid crystal displays, image sensors, and silicon on insulator (SOI). Poly-Si TFTs also have applications for building vertical structures for 3-D integration. If the poly-Si devices can be successfully fabricated with channel dimensions comparable to or smaller than the grain size, they can be a possible alternative to conventional silicon MOSFETs.

For these applications the performance of poly TFTs needs to be considerably enhanced. Various techniques can be employed to improve the electrical properties of poly-Si and are outlined in this thesis. In the present study, novel method of forming a heterostructure channel in poly-Si has been attempted and investigated. Si-Ge heterostructure MOSFETs have been fabricated in single crystal silicon employing epitaxial techniques, which have resulted in faster devices through increase in carrier mobility. No such work has been reported in poly-Si to the best of the authors knowledge. Further more, the technique for the formation of Si-Ge channel in poly-Si TFTs developed and studied in this thesis is simple and compatible with IC Processes using implantation.

Both NMOS and PMOS devices have been investigated in thin poly-Si films with and without Si-Ge channels. The electrical results obtained have been interpreted in terms of the film structure and substrate.

The thesis has been organized into six chapters. The first chapter outlines the purpose, objective and relevant literature review. Chapter 2 gives a brief established theory of the important concepts in the work. Chapter 3 describes the fabrication process and design in detail. Chapter 4 displays the relevant results obtained. Chapter 5 gives a detailed discussion of the results, using relevant theory to establish outcome and chapter 6 briefly presents the major conclusions of this work.
Abstract

Thin Film Transistors have been fabricated in 0.2 um thick polycrystalline silicon. NMOS and PMOS devices were fabricated on four groups of substrates. One group was processed with as deposited polysilicon and three of the substrates received high dose implants of Si and/or Ge prior to anneal. The Si implants were designed to amorphize the film by a process known as Seed Selection through Ion Channeling (SSIC), and the Ge was implanted just below the surface to enhance transistor characteristics. Two of the groups, one which received Ge implanted just below the surface and the other no implant at all, did not show much of any improvements in either the NMOS or the PMOS devices. Wafers that received double Si implants prior to substrate anneal, allowed the NMOS devices to exhibit better transistor qualities than any of the other implants, while the PMOS devices exhibited very poor qualities. Substrates that received a high energy high dose Si implant and Ge implanted just below the surface at a high dose to create a Si-Ge channel, demonstrated a 100% increase in hole mobility on 2 um channel length devices over the double Si implanted substrates. The drain current of the Si-Ge PMOS devices was -260 uA as compared to -16 uA for the double Si implanted substrates for $V_{gs}$=-7 V at $V_{ds}$=3.0 V. The subthreshold swing was much larger at 2.1 V/dec for the Si-Ge channel PMOS devices as compared to and average of about 0.5 V/dec for all the other PMOS devices. The undesirable leakage observed in the subthreshold swing can be attributed to the grain structure of the Si-Ge layer in the channel. These effects can be minimized by further enhancement of grain sizes and passivation of the grain boundaries.
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Chapter 1 Introduction

Thin Film polysilicon Transistors (TFT's), on an insulating substrate have become more attractive for use in many applications. A few of the many are active-matrix liquid crystal displays, image sensors [1], SOI, and stacked CMOS technology [2]. Polysilicon can be easily deposited on many materials, such as glass substrates and some deposited films including silicon dioxide (SiO₂) and silicon nitride (Si₃N₄). The low deposition temperature capability of polysilicon gives it the versatility for deposition on many types of substrates including those that are limited to low temperature processing.

Commonly, the polysilicon layers are deposited by Low Pressure Chemical Vapor Deposition (LPCVD) at temperatures around 600°C - 650°C. The grain size obtained in such films is around 300 - 1000 Angstroms in diameter. In polysilicon MOSFETs, grain boundaries are responsible for low channel mobility and high threshold voltage. It is necessary to bring the properties of polysilicon close enough to those of single crystal silicon to build reasonably good field effect devices. This can be achieved by increasing the grain size through recrystallization techniques. Some of the techniques performed to achieve increased grain size are, Zone Melting Recrystallization (ZMR) [3], Annealing by use of an ArF (193 nm) excimer laser [4], and black body radiation.
Rafael Reif, et. al. have employed a technique known as Seed Selection through Ion Channeling (SSIC) as a possible low temperature alternative to recrystallize polysilicon [5]. This process utilizes a high dose Si self implantation followed by a long low temperature anneal at 600°C in N₂. The Si self implant results in a selective amorphization of the poly-Si film preserving few grains of predominate crystallographic orientation. These remaining grains grow by solid phase epitaxy at the expense of the amorphous Si around them during the low temperature anneal.

In a recent paper, the SSIC technique of a single Si implant at the Si/SiO₂ interface was replaced by a double Si implant [6]. This technique includes an extra Si implant just below the surface to maximize amorphization through out the film.

Another technique to increase TFT performance is the passivation of the grain boundaries with atomic hydrogen. The hydrogen atoms attach to the loose Si bonds in the grain boundaries to minimize carrier trapping, and decreases threshold voltage as well as subthreshold swing. Hydrogen works well because it easily diffuses into the substrate and is small enough not to create any strain in the film, but another option could be lithium [7]. Three methods that have been used to passivate grain boundaries are subjecting the substrate to a hydrogen plasma [8], implanting H⁺ ions into the channel [9], and the use of Plasma Enhanced Chemical Vapor Deposition (PECVD) of nitride [10]. The hydrogen
atom penetrates through most materials very easily at even low temperatures. Therefore, the passivation must be performed at the end of the process and without exceeding temperatures of 400°C. Silicon nitride is one of the materials that limits the effusion of hydrogen, so a PECVD nitride to prevent H out diffusion will be used in future work for passivation.

Even with enlarged grains and passivated grain boundaries, the performance of both NMOS and PMOS devices are not inferior to single crystal devices. Some of the grain boundary effects can not be eliminated. The next step for device quality improvement is to enhance the characteristics of the Si grains themselves. Device performance can be enhanced by increasing field effect mobility in the channel.

In crystalline silicon, heterostructure Si-Ge MOSFETs have been fabricated and have shown a remarkable improvement in device performance. SiGe channel NMOSFETs were created by selectively implanting germanium in the channel. These devices exhibited better mobilities and higher currents than NMOS devices fabricated in single crystal Si with no channel enhancement [11]. (See Figure 1.1 for $I_{DS}$ vs. $V_{DS}$ and $I_{DS}$ vs. $V_{GS}$ curves from this article). An increase in subthreshold swing can also be observed from the log($I_{DS}$) vs. $V_{GS}$ curve. PMOS devices were fabricated in polycrystalline silicon-germanium films and received grain boundary passivation through H$^+$ implantation to improved device characteristics. These devices required a gate voltage of -25 volts to obtain a current of -50 uA [12].
(See Figure 1.2 for \( I_{ds} \) vs. \( V_{ds} \) curve before and after passivation). PMOS devices with single crystal silicon-germanium channels were also fabricated and discovered to perform with a higher field effect mobility and current driving capabilities than standard PMOS devices in single crystal Silicon [13,14].

In the present study a technique combining double implantation with Si-Ge channel incorporation has been attempted for the first time. MOSFETS were fabricated in four types of polysilicon films. Three out of the four groups received selective Si and Ge implants. Two of the three groups received two implants. Both received a deep Si implant first and one a second Si implant just below the surface and the other a Ge implant placed just below the surface. The third group received a single Ge implant just below the surface while the fourth group was untreated with implants. All the substrate underwent the exact same processing steps after the selective substrate implants were performed. Values of threshold voltage, subthreshold swing, and field effect mobility has been extracted from devices in each group and compared. The results have been correlated with the film structure and composition.
Figure 1.1: Ge implanted channel NMOS characteristics [11].

Figure 1.2: Electrical curves of PMOS TFT fabricated in LPCVD Poly-Si-Ge [12].
Chapter 2  Theory

2.1 Field Effect in Polysilicon

The concept of placing the conducting channel of a MOS transistor within a thin layer of polysilicon has been extensively explored. Polysilicon TFTs show similar characteristics as compared to transistors made in crystalline silicon except the transconductance is low and the threshold voltage is high. As the gate voltage is applied, the energy band must be bent to induce a conducting inversion layer near the Si surface. Polycrystalline silicon contains high concentration of deep traps located near the grain boundaries. Much of the applied voltage is used to charge or discharge traps, rather than inducing free carriers in an inversion layer. This requires extensively high gate voltages to be applied before a conducting channel can form between the source and drain as shown in Figure 2.1. The poly-Si transistor can therefore be visualized as several transistors in series [15]. The grain regions have a threshold voltage determined by the normal transistor equation for single crystal silicon, but the transistors over grain boundaries have much higher threshold voltages. Consequently, the observed threshold voltage is much higher than expected for the dopant concentration in the polysilicon grains.

The low channel transconductance is due to the combined effects of grain boundaries lowering mobility and the surface scattering of carriers from the poly-Si/SiO₂ interface.
Figure 2.1: (a) Bulk Si in inversion; (b) Bulk Si in accumulation; (c) Poly-Si in inversion; (d) Poly-Si in accumulation. After D.J. Bartelink [15]

Because of the dominating effect of grain boundaries, poly-Si films with larger grains are desired to produce transistors with the best properties.

2.2 CMOS Performance

The PMOS transistors fabricated in silicon substrates have displayed poorer performance as compared to the NMOS devices. The minority carrier electrons in the channel of the NMOS devices have a higher mobility than the holes in the channel of the PMOS devices. This has been the case since integrated circuits were first fabricated. The hole mobility of the PMOS devices was noted to be approximately two times time less than that of the electrons in the NMOS devices. This was taken into account in static CMOS circuits by designing the PMOS transistors twice as wide as the NMOS transistors. This would allow for a larger area under the gate for carriers to be generated and therefore current would
be more comparable to that of the NMOS device. This would allow for virtually equal Beta\textsubscript{n} and Beta\textsubscript{p} values which in turn would allow for equal rise and fall times. See equations below.

\[ \beta_n = \frac{\mu_n e_{ox} W}{t_{ox} L} \quad \ldots (2.1) \]
\[ \beta_p = \frac{\mu_p e_{ox} 2 W}{t_{ox} L} \quad \ldots (2.2) \]

\[ t_{fall} \approx \frac{3C_L}{\beta_n (V_{DD} - V_{Th})} \quad \ldots (2.3) \]
\[ t_{rise} \approx \frac{3C_L}{\beta_n (V_{DD} + V_{Th})} \quad \ldots (2.4) \]

### 2.3 Field Effect Mobility

The performance difference between the NMOS and PMOS devices is primarily attributed to the decreased mobility of holes in silicon as comparable to electrons. The mobility of carriers can be defined as the drift velocity per unit field. The mobility is controlled by lattice scattering and ionized impurities in the bulk semiconductor.

In MOSFETs, carriers flow in the inversion layer close to the Si/SiO\textsubscript{2} interface. The mobility is therefore strongly affected by surface scattering. The increased gate voltage creates a stronger transverse field which attracts the carriers to the interface. The current is flowing by drift current from the field created by the source and drain bias differential. The transverse field prevents the carriers from flowing strictly in a lateral direction to optimize current flow and thus
mobility. The transverse field pulls the carriers toward the Si/SiO₂ interface while the lateral field pulls them toward the drain. This creates a zig-zag motion of the carriers from source to drain. Figure 2.2 shows a pictorial view of the result of surface scattering. This accounts for larger field effect mobilities of carriers as compared to their bulk values. In polycrystalline silicon, the mobility of the carriers is further degraded by the presence of thermionic barriers resulting from the grain boundary charge.

2.4 Buried Channel

The performance of MOS devices in single crystal Si are found to be enhanced with the incorporation of a SiGe channel. The way this has been performed is by using Ge to create a Si-Ge alloy in the channel region of the device to alter the band gap of the semiconductor. The Ge must be introduced as a SiGe alloy in order to minimize the interface states at the Si/Ge interface.

A quantum well is created by depositing a 100Å layer of single crystal Si₀.₆Ge₀.₄ and depositing a single crystal Si layer 75Å thick on top of it [14,16]. The presence of the quantum well allows an inversion layer of holes to first occur in the SiGe alloy channel thus minimizing surface scattering effects on mobility and current. The inversion takes place in the channel first because the smaller band gap in the SiGe creates a lower potential for holes. The smaller band gap allows the valence band in the channel to rise above the fermi level before the valence band at the semiconductor/oxide interface which in turn allows for the threshold
Figure 2.2: An illustration that represents surface scattering in the inversion layer.

Figure 2.3: (a) Energy band of SiGe at flat band. (b) Energy band under forward bias close to inversion. (c) Energy band under strong inversion, showing hole confinement and the existence of a quantum well [14]
voltage to be lowered. The abrupt Si/SiGe interface causes an abrupt change in band gap which causes the quantum well to form for the holes to float into. The inversion layer is first created in the buried channel region resulting in hole confinement. The confinement of the holes in the channel minimizes the effects of surface scattering immensely. Surface scattering does effect the mobility at larger gate voltages because an inversion layer begins to form at the Si-SiO₂ interface. Figure 2.3 illustrates a quantum well in the valence band, bringing the valance band closer to the Fermi level and allowing hole confinement to occur for a negative gate bias.

The Si spacer not only allows for a buried channel to be formed, but also for the gate capacitance to be decreased. The gate oxide capacitance is now in series with the Si spacer capacitance, thus lowering the total effective gate capacitance. This causes the field effect mobility to increase slightly more. See equation (2.5).

\[
\mu = \frac{\Delta I_{DS}}{\Delta V_{GS}} \frac{L (C_{s1} + C'_{ox})}{W (C'_{ox}) (C_{s1}) (V_{DS})} \quad \ldots \quad (2.5)
\]
Chapter 3 Fabrication

3.1 Substrate Preparation

Nineteen P-type <100> oriented wafers were obtained to be scribed. There were four primary categories labeled A, B, C, and D. Wafers scribed A1-A5 did receive deep Si as well as shallow Si implants. Those scribed B1-B5 did receive a deep Si and shallow Ge implant. Those scribed C1-C5 did only receive a shallow Ge implant and wafers D1-D4 received no implant.

After scribing they were put through a standard RCA clean and placed in a furnace tube for an isolation oxide growth. The wafers were pushed in at a rate of 12 inches per minute at a temperature of 800°C with oxygen flowing through the bubbler at 4 lpm. The oxygen was bubbled through de-ionized water at a temperature of 98°C. The furnace temperature was ramped up from 800°C to 1100°C at a rate of 20°C/minute. The wafers soaked at 1100°C for 75 minutes and were then ramped down to 850°C in a wet oxygen environment. The ramp down took approximately 40 minutes and the process grew about 6500 Å of isolation oxide. A few thickness measurements were taken on a good distribution of wafers, and they were immediately place in the Low Pressure Chemical Vapor Deposition (LPCVD) for polysilicon deposition. Control wafers had to be made prior to deposition with 1000 Å of SiO₂ on them so as to be able to measure the polysilicon thickness on the nano spec. These wafers were placed in a furnace
tube and ramped up to 1100°C and soaked for 50 to 60 minutes in a dry oxygen environment with a flow of 5 lpm. Five of these wafers were placed in front as well as in back of all the device wafers to insure uniform flow of the silane (SiH₄) gas across the center of the boat during the polysilicon deposition. Two more controls were inserted in between the device wafers for thickness measurement purposes. All the wafers, in any of the diffusion processes, were placed flats facing up with the polished side oriented away from the flow of the gasses.

The wafers were placed in the LPCVD after the tube was profiled for two hours to allow the temperature to stabilize. The following were the settings and temperatures of the tube. The front setting was 303 with the temperature at 608°C, the center setting was 212 with a temperature of 611°C, and the back or pump end of the tube was set at 361 with a temperature of 611°C. The base pressure was determined to be 52 mtorr and the deposition pressure was 273 mtorr. The SiH₄ flowed at 90 sccm during the 22 minutes of deposition. The polysilicon was deposited at a rate of about 90 A/minute to give approximately 2000 A of polysilicon.

The samples were sent out to Ion Beam Technology in Tustin, CA to be implanted with Si and Ge. The implants were to amorphize the polysilicon substrate to promote SSIC. All of the implants were performed with the incident ion beam 7° off angle to the normal of the wafer. The chuck was cooled with freon and the beam current kept under 3 uA/cm². These restrictions for the implant
allowed the polysilicon to remain amorphous and not to begin recrystallizing before being annealed under the proper conditions [17].

The samples were divided into groups A through D and the implant conditions are shown in Table 3.1.

<table>
<thead>
<tr>
<th>Group</th>
<th>Implant # 1</th>
<th>Implant # 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Si 150keV, 1X10^{15} ions/cm^2</td>
<td>Si 40keV, 1X10^{15} ions/cm^2</td>
</tr>
<tr>
<td>B</td>
<td>Si 150keV, 1X10^{15} ions/cm^2</td>
<td>Ge 85keV, 1X10^{16} ions/cm^2</td>
</tr>
<tr>
<td>C</td>
<td>NONE</td>
<td>Ge 85keV, 1X10^{16} ions/cm^2</td>
</tr>
<tr>
<td>D</td>
<td>NONE</td>
<td>NONE</td>
</tr>
</tbody>
</table>

The implant concentration and damage profiles were simulated using the TRIM software (Transport of Ions in Matter, version 92.3). Figure 3.1 shows the concentration and damage profile obtained in the Si-Si and Si-Ge implanted samples.

The isolation islands and alignment marks were all patterned with the MESA mask which was also the WELL layer for the CMOS MOSIS design levels. The polysilicon islands provide isolation for the devices as well as stress relief for the film during the grain size enhancement anneal. The islands were etched in the reactive ion etcher one wafer at a time at a power of 75 watts and a pressure of 75 mtorr. The gases used were SF₆ at 30 sccm and O₂ at 3 sccm. The etch took about 40 seconds with consideration to the bullseye effect and over etch.
Figure 3.1: (a) TRIM plot showing the location of the Ge and Si from the Si and Ge implants; (b) TRIM plot showing the location of the double Si implant; (c) TRIM damage calculation for the SiGE implants; (d) TRIM damage calculation for the double Si implant.
positive photoresist was then striped off in a $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$, 3:1 mixture called piranha. An asher was not used because energy generated from the deep UV light in the plasma might have caused some unwanted recrystallization in the polysilicon.

The top 50 A or so of polysilicon had to be removed because of the number of seeded crystals that remained after implant. If they were not removed they would start growing during anneal and limit the final grain size [6]. In order to accomplish this, the oxidation capabilities of the APM bath in the standard RCA clean was used to our advantage. Silicon forms a very thin oxide film on the order of ten to twenty angstroms when placed in the APM for five minutes. The surface polysilicon was removed by repeated the cycles of an APM dip to oxidize the film, followed by an HF dip to remove the oxide.

The substrate grain enhancement anneal was performed at 625°C in a furnace for 30 hours with 2.5 lpm flow of $\text{N}_2$. Low temperature anneals have been demonstrated to promote grain growth in amorphous polysilicon films [18-20]. SPE, the process by which the grains increase in size during a thermal step by consuming the amorphous Si around it, occurred in all the films.

### 3.2 Substrate Analysis Procedure

For analysis of the Si/Ge implanted substrates, cross sectional TEM and surface TEM samples were prepared to study the film grain structure. The TEM sample was made by cutting a 2 X 2 mm$^2$ grid in the sample substrate. In this
case, the cuts were made with a die saw about 20 microns deep. They were just deep enough to allow the concentrated HF to undercut the 6500 Å of isolation oxide under the polysilicon substrate. The undercutting took about 48 hours of soaking in 48.0 % HF solution, to float the samples to the surface. The HF was diluted and then the samples were carefully placed on a TEM copper grid. The cross sectional TEM sample were made using the cross sectional sample preparation technique discussed in Appendix A.

### 3.3 Device Design

The physical layout was performed on Chipgraph, which is software supported by Mentor Graphics. There were seven design levels used in the layout of the chip. The levels in order of processing were as follows; MESA for transistor isolation, POLY for the gate electrode, P⁺ and N⁻ for the PMOS and NMOS source and drain implants respectively, CC for the contact cuts and METAL for the metal interconnects. The seventh level is for a contact cut to the metal pads through a PECVD nitride that is deposited for grain boundary passivation. This level was designed for future work and was not used in the processing.

Individual transistors were designed with gate lengths and widths ranging from 2 µm to 50 µm. The largest transistor gate designed was 50 X 50 µm² and the smallest 2 X 2 µm². The design rules used in the layout were scaled MOSIS CMOS design rules. In the MOSIS CMOS design rules lambda is scalable and a 3 µm lambda was chosen for this work. For example, the contact cuts were 6 X
6 \text{um}^2 \text{ and the minimum metal line width was 12 \text{um}. (See Appendix B for scalable MOSIS CMOS design rules).}

The NMOS and PMOS transistors were designed with virtually all possible combinations of gate widths and lengths with the following numbers in micrometers: 50, 25, 15, 10, 6, 4, 3, and 2. See Figure 3.2 for the layout schematic of an NMOS transistors with all the layers labeled. The figure demonstrates how the MESA mask isolated each individual transistor on a 300 X 300 \text{um}^2 \text{ poly island. The metal pads were all 100 X 100 \text{um}^2 \text{ and separated by 100 \text{um} on all sides. Each transistor was designed as a four terminal devices with connections to source, drain, gate, and substrate. The substrate contact was a schottky contact unlike the source, drain and gate which were ohmic. A direct contact to the substrate was made with the assumption that the schottky diode voltage drop would be negligible as compared to the substrate/drain diode voltage drop.}

In addition to various sized TFT's, other test structures were also included to assist in characterization. Static CMOS inverters with varied size transistors were designed to observe switching characteristics. Keeping the lengths of both transistors equal, the ratio of the pull-up to pull-down in the inverter was kept equal to two in all cases. This took into consideration the differences in hole and electron mobility to allow for some what equal currents and rise and fall time. Electrons are generally twice as mobile as holes in single crystal Si. This was not the case that was observed for these fabricated TFT's. Figure 3.3 shows a layout
**Figure 3.2:** Layout schematic of an NMOS transistor design for a TFT fabrication process with samples of the layer patterns.

**Figure 3.3:** Layout schematic of an Inverter design for a TFT fabrication process with samples of the layer patterns.
schematic of a TFT CMOS inverter with L = 2 \, \text{um}.

Other designs in the layout to supply more electrical information were Van der Pauw structures, Kelvin contact resistance structures, capacitors and diodes. The diodes were designed to be able to test if the source/drain to substrate paths were leaky and, if so, to what extent for each of the different polycrystalline substrates.

Some structures were included for lithographic purposes such as line and square resolution patterns ranging from 1.0 \, \text{um} to 10.0 \, \text{um}. Verniers were also included in the layout to assist in setting up the shift for the different mask levels in order to align properly. Verniers were a necessity on most of the mask levels. See Figure 3.4 for schematic of layout on hierarchical level to see where everything was placed.

### 3.4 Device Fabrication

The details of the entire fabrication process is given in Appendix C. Some important specific details are given below.

#### 3.4.1 Gate Oxide

After substrate preparation describe in section 3.1, a gate oxide was grown according to the process in reference [21]. The high temperature growth was chosen to maximize the quality of the oxide grown on the polysilicon. At lower temperatures the surface grain boundaries grow oxide much faster than grains which give a very rough SiO\textsubscript{2} to polysilicon interface. This would allow for the
potential of more interface traps. Low temperature gate oxide processes are to be experimented with in future work primarily for the application of stacked CMOS SRAMS.

Furnace tube #12 underwent a TCA clean for 15 minutes prior to the gate oxide growth. TCA was bubbled into the tube at 189 sccm with the tube at 900°C. The wafers were then pushed into the furnace at 900°C after a 90/10 N\textsubscript{2}/O\textsubscript{2} flow ratio (0.5 lpm/4.5) was established. This flow mixture was to slowly introduce oxygen to the polysilicon surface to form a thin oxide layer to minimize interface traps and stress at the oxide polysilicon interface. After ramping up for 16 minutes, 1100°C was reached and 5 lpm dry oxygen was flowed into the furnace for four minutes. TCA was then bubbled in at 189 sccm with oxygen for 4 minutes followed by 5 lpm dry oxygen only for the last four minutes. After a total time of 12 minutes at 1100°C, the temperature was ramped down to 900°C in an argon environment at a flow of 5 lpm. The argon was used to help minimize surface states and fixed charges in the gate oxide.

3.4.2 Formation of Gate Electrode

The wafers were immediately placed into the LPCVD for polysilicon gate deposition after removal from the furnace with the exception of D3 and D4. Five control wafers were placed in front as well as in back of the device wafers and two in between for thickness measurements. The LPCVD furnace was previously profiled to give temperatures of 608°C, 610°C and 609°C for front, center and
pump thermocouple respectively. The base pressure was measured to be 53.7 mtorr and the deposition pressure was 278 mtorr. SiH₄ was flowed in at 90 sccm for 60 minutes of deposition.

The poly gate was doped using Emulsatone N-250 spin on dopant. The wafers were put through an APM dip for 30 seconds prior to spinning on the N-250 to help promote adhesion of the glass. The N-250 was then spun on at 3k RPM for 30 seconds and baked at 180°C in a convection oven for 15 minutes. The wafers were then placed into furnace tube #13 at 900°C with a 10/90 O₂/N₂ flow ratio for 20 minutes. After removal and cooling, the wafers were de-glazed in BOE. The sheet resistance determined from the four point probe method was much higher than was expected, so another soak was decided to be performed. The wafers were prepared the same way and they were kept in the furnace for 8 minutes. Any longer might cause the phosphorous to be driven into the channel from the remaining thermal steps in the process.

The gate patterning step was the most crucial step. From previous experience, large areas of exposed resist would not remove completely after developing with the existing develop program. To take care of this problem, a new program was written to include a double puddle develop followed by a 140°C hard bake. See Appendix D for program. All of the resist lines were flowed by the post development bake to accommodate for the undercut that would occur from the gate etch in the RIE. All geometries down to 2 um were resolved well enough to
Figure 3.4: Shows location of all designs on chip through hierarchy.

Final Boron Concentration in PMOS S/D

Figure 3.5: Final concentration profile of P⁺ Source/Drain region from TMA SUPREM 3 simulation.
withstand the gate etch in the RIE.

The wafers were all etched individually and with the same gasses and conditions as for the mesa etch. The etch was followed by a resist strip in piranha, \( H_2SO_4/H_2O_2 \) in a 3:1 mixture.

### 3.4.3 Formation of Source and Drain

The wafers were then patterned for the \( P^+ \) self aligned source and drain implants. The implants were performed using \( B^{11} \) at an energy of 35 keV and a dose of \( 1 \times 10^{15} \) ions/cm\(^2\), which were determined by the use of TMA Supreme 3 (See Figure 3.5 for annealed boron profile in the source and drain region and Appendix E for SUPREM 3 input file). The energy was chosen to place the maximum amount of boron into the source and drain region without being too high as to cause an increased risk of boron diffusion into the channel through the gate after final processing. The implanter was only able to produce a 6 μA beam current at 35 kev. This caused the implants to take upwards around 40 minutes a wafer. Wafer number D3 was used as the control wafer for the \( B^{11} \) implant and D4 for the phosphorous implant. Implanting these substrates with this large dose caused the resist to burn onto the wafers. The only way the resist was able to be removed was by performing a heated piranha for 30 to 40 minutes.

After removing the resist, The \( N^+ \) source and drain regions were patterned with mask level four and the implant was performed with an energy of 60 keV and a dose of \( 1 \times 10^{15} \) ions/cm\(^2\). This energy was increased from a previously chosen
energy of 55 keV to insure the implant peak was placed within the polysilicon substrate. The oxide thickness loss from the polysilicon gate etch was assumed to be minimal and was therefore, not taken into account.

A RCA clean was performed following the resist strip in piranha. Then an anneal was performed in tube #13 for 35 minutes at 900°C with an oxygen flow of 5 lpm. An oxide of about 200 A was grown on the gate polysilicon during the P+ and N+ source and drain region anneal. The time of anneal was originally 45 minutes, but after a LTO test run, it was determined that a densification step had to be performed. Ten minutes was subtracted from the original anneal time and a densification step after LTO deposition of ten minutes at 900°C in 5 lpm oxygen was added. The anneal time for the implants were gauged by the diffusion of boron under the gate, using TMA SUPREM 4 to display lateral diffusion and through the gate using TMA SUPREM 3. (See Figures 3.6A for cross section lateral diffusion simulation from SUPREM 4 and 3.6B for the vertical diffusion of boron in the gate. Appendix F has a SUPREM 4 input file that was used to create lateral diffusion plot).

3.4.4 Passivation

The LTO was performed on the four inch wafers using a polysilicon boat at a temperature of about 400°C. A previous run allowed us to ascertain that there was a problem with the uniformity of the deposition across the boat. At least ten dummy wafers had to be placed in front of the device wafers, and a minimal of six
Figure 3.6: (a) TMA SUPREM 4 simulation shows lateral diffusion of boron under the self aligned gate in the PMOS; (b) TMA SUPREM 3 simulation of boron diffusion through the gate.
behind them, to obtain a reasonable uniformity of LTO on the device wafers. The LTO was deposited satisfactorily on the central portion of the wafer, but left an undesirable ring around the edge. After 80 minutes of deposition, the LTO on the central portion of the device wafers ranged from 1600 A to 2500 A.

The deposition process for LTO was slightly different than the polysilicon deposition. The gasses used were SiH₄ and O₂. The SiH₄ and O₂ couldn’t just be turned on at there respective flows of 40 sccm and 24 sccm. The pressure increased dramatically and caused the program to abort. This occurred because the gasses did not immediately react with one another causing the pressure to increase. To prevent this, the gasses were ramped up to their respective flows one at a time starting with O₂. If the pressure exceeded 400 mtorr during the ramping, or any time during the deposition, the program would abort. The base pressure was 58.3 mtorr stabilized at 220 mtorr during deposition.

The LPVCD tube was calibrated for 400°C, but was very difficult to stabilize. The settings and temperatures for the three thermocouple were as follows: front setting at 305 with a temperature of 406°C, center setting at 10 with a temperature of 404°C, and the pump setting at 426 with a temperature of 404°C.

The LTO densification followed directly after the deposition so another RCA clean would not have to be performed. The densification was performed to decrease the etch rate of the LTO in BOE so as to be more comparable with the etch rate of thermally growth oxide. The densification would have best been

30
performed by rapid thermal annealing but that was not an option at this time. The densification step dropped the etch rate of the LTO from 4000 A/minute to 1600 A/minute allowing for a more uniform contact cut etch with the thermally grown oxide under the LTO.

### 3.4.5 Contact Cut and Metallization

The photoresist from the contact cut patterning was removed in the asher instead of the piranha to help save time and money. This was followed by an RCA clean with a 20 second HF dip to clean out the native oxide in the contacts before metal deposition. The wafers were dried in the spin dryer and placed into the sputterer with three dummy wafers for measurement and lithography purposes. Normally, the wafers would undergo a dehydration bake prior to being pumped down in the sputterer. In this case the wafers were left in with the sputterer pumping down over night so a dehydration bake was not as necessary.

The base pressure just before sputtering was $2 \times 10^{-6}$ torr. The desired thickness of Al 1% Si was about 0.8 um. From previous sputtering results, a deposition time of 19 minutes at around 3000 watts was chosen. The voltage was at 340 V and the current at 9 Amps to give a power of 3060 watts. The pre-sputter time was calculated by using 2 minutes for every 1000 watts of power to give a pre-sputter time of 6 minutes.

The wafers were sintered for 20 minutes in forming gas, which was flowing at 5 lpm, between 425°C and 450°C. This procedure was performed after the
metal deposition. Tube #14 was used for the sinter and the temperature was very
difficult to stabilize. The lithography was performed after the sinter and the Al was
etched in an Al etch at 50°C. The wafers were etched in the bath until cleared,
plus an additional minute for over-etch to make it a total of four minutes. The
wafers were then rinsed, dried, ashed, an finally tested.

3.5 Results of Processing

The isolation oxide did not turn out to be very uniform across the wafer. The thicknesses varied from 6900 A at the top (flat) to 6200 at the bottom. This was not felt to be of great importance because it was just to serve as isolation for the TFTs. The polysilicon was deposited on the isolation oxide was very uniform. The thickness was measured from the control wafers placed in between the device wafers during deposition. The nano spec measured an average thickness of 1956A for the boat of wafers. This thickness of polysilicon created a rosy pink color. The rosy pink turned to silver after implanting the substrates with Si and/or Ge. The color change signified that an amorphous film was created.

The implanted regions changed color slightly after anneal. The color after anneal was slightly rosy pink with a hint of silver. The remains of the silvery color might have indicated that film might still have been slightly amorphous.

The gate oxide growth caused the pinkish silver color on the polysilicon substrates to changed to a florescent green after the gate oxide was grown on the substrates. The color of the oxide on the single crystal wafers was a shade of
brown.

A few P-type 5-15 ohm-cm <100> silicon wafers were used to try to characterize the oxide growth. A couple of dummy runs were performed to play with the soak time. An initial soak time of 16 minutes was determined by SUPREM 3 to obtain approximately 700 A of oxide on single crystal Si. After experimenting, a soak time of 12 minutes gave an oxide thickness of 720 A on single crystal silicon. The multi wavelength light from the nano spec could not read the oxide thicknesses on the polysilicon because thin polysilicon does not absorb higher wavelengths of light. Therefore, the thin polysilicon could not be considered a substrate to the nano spec. Only an ultra violet nano spec could be used to measure oxide thicknesses on thin film polysilicon substrates. Doug Hunt sent out some of his wafers to have the oxide thickness on thin film polysilicon measure by UV nano spec. The results determined the SiO₂ to grow approximately 15 % thicker on polysilicon than on single crystal silicon. This allowed the thickness estimation of the gate oxide grown on the polysilicon to be approximately 800 A. Oxide growth on polysilicon and poly-SiGe was proven to be very similar for high temperature oxide growths in dry oxygen. It was also determined that the Ge implanted in the polysilicon near the surface would not incorporate itself into the oxide. The Ge piles up at the Si-Ge oxide interface to create a smoother interface that is believe to help minimize interface traps [22].

Some experiments were run depositing up to 1.3 um of polysilicon on oxide
and bare silicon wafers to see if a thicker polysilicon layer could act as a substrate to measure oxide thicknesses with the ellipsometer. A thick polysilicon film should have absorbed the green light from the ellipsometer allowing it to function as a substrate and allow the measurement of oxide grown. Had this worked, it would have enabled us to measure oxide thicknesses on polysilicon substrates. This was assuming that the growth of the oxide did not depend on the thickness of the polysilicon. The findings were determined to be inconclusive with the measured thicknesses received from the ellipsometer ranging from 600 A to 800 A. In light of these results the gate oxide thicknesses could only be assumed to be 800 A.

The polysilicon gate was deposited on the wafers in the LPVCD gave an average thickness of 4950 A. The gate was doped with Emulsitone N-250 spin on glass to give an N⁺ polysilicon gate. The first bake was for 20 minutes at 900°C and only gave a sheet resistance of 470 ohm/sqr. After the second bake for 8 minutes at 900°C, the gate sheet resistance was only decrease to about 165 ohm/sqr.

A sectioned portion of wafer D3 was implanted with boron at 35 keV with a dose of $1 \times 10^{15}$ ions/cm² to perform a control run for the P⁺ source and drain regions. D3 was then placed in furnace tube 13 to under go a 45 minute anneal at 900°C in oxygen. The sheet resistance determined after four point probe was 264 ohm/sqr. This was satisfactory for the time being, but annealing conditions to lower the sheet resistance should be determined for future work.
The rest of the wafers, including D3 and D4, were implanted with B\textsuperscript{11} for P\textsuperscript{+} and Phosphorous for N\textsuperscript{+}. After the final processing, four point probe readings were taken for both implants and the values of the sheet resistances calculated were very high. Sheet resistance values were determined to be 352 ohm/sqr for the P\textsuperscript{+} and 776 ohm/sqr for the N\textsuperscript{+}. It was first though that the simulation in SUPREM 3 was incorrect for not taking into account the thickness loss in the oxide after the gate etch. It was believed that the implants went to deep and therefore beyond the substrate into the isolation oxide. Further simulations in SUPREM 3 for the N\textsuperscript{+} implant showed that the sheet resistance should be 90 ohm/sqr for a 500 A oxide and 117 ohm/sqr for a 775 A gate oxide. These numbers obviously did not compare with the results obtained on the device wafers. It is highly recommended that the anneal times be experimented with in future work.
Chapter 4   Results

4.1 Film Structure

To study the film structure, grain size was observed using TEM analysis and film composition using Rutherford Back Scattering (RBS).

4.1.1 Film Morphology

Figure 4.1A and 4.1B give the TEM micrographs of as deposited polysilicon and Si-Ge implanted and annealed films respectively. It is observed that the recrystallized Si-Ge implanted polysilicon is composed of large grains, some of them 0.5 um in diameter, in a matrix of a fine grain structure. To study this structure further, the films were viewed in cross sectional mode. Figure 4.1C and 4.1D give XTEM micrographs of the implanted films after anneal. A distinct fine grain structure surface layer (~ 40 nm) was observed on a layer of larger grain polysilicon film.

4.1.2 Film Composition

The Si-Ge implanted polysilicon films were studied using RBS analysis. Figure 4.2 shows the RBS spectrum showing a Ge rich surface layer with a peak just below the surface. The peak concentration was estimated to be 2.7% corresponding to a dose of 1.08 X 10^{16} ions/cm^2 which is very close to the intended implant dose of 1.00 X 10^{16} ions/cm^2.
Figure 4.1: (a) Surface TEM micrograph of as deposited poly-Si 49k mag.; (b) Surface TEM micrograph of Si-Ge implanted poly-Si 12k mag. (c) XTEM Si-Ge implanted film 300k mag.; (d) XTEM Si-Ge implanted film 750k mag.
4.2 Transistor Characteristics

The transistor electrical results include drain current, threshold voltage, mobility, subthreshold currents and inverter characteristics.

4.2.1 $I_{DS} - V_{DS}$ Curves

Figure 4.3A shows typical $I_{DS} - V_{DS}$ curves for group A and group B PMOS transistors for gate voltages ranging from 0 to -7 volts.

Figure 4.3B shows typical $I_{DS} - V_{DS}$ curves for group A and group B NMOS transistors for gate voltages ranging from 0 to +7 volts.

Similar curves were plotted for groups C and D TFTs and are shown in Appendix G.
Figure 4.3:  (a) Comparison of drain currents for 2/25 PMOS devices from a double Si implanted wafer and a SiGe implanted wafer; (b) Comparison of drain currents for 2/25 NMOS devices from a double Si implanted wafer and a SiGe implanted wafer.
Significant difference in drain current is observed.

4.2.2 $I_{DS} - V_{GS}$ Curves

$I_{DS} - V_{GS}$ curves were plotted to study the variations in threshold voltage.

Figure 4.4A shows typical $I_{DS} - V_{GS}$ curves for group A and B PMOS transistors with $V_{sb} = 0$ V.

Figure 4.4B shows typical $I_{DS} - V_{GS}$ curves for group A and B NMOS transistors with $V_{sb} = 0$ V.

Similar curves were plotted for groups C and D TFTs and are shown in Appendix H. These characteristics were also studied under a varying substrate bias from 0 to -3 V for NMOS and 0 to +3 V for PMOS.

Threshold voltage and mobility

The values of threshold voltages and field effect mobilities were extracted from the curves in Figure 4.4, which were plotted in the linear regime. The threshold voltages were extracted from the X intercept of the line and the mobility was calculated from the following equation.

$$
\mu = \frac{\Delta I_{DS}}{\Delta V_{GS} V_{DS} C'_{ox} W} \ldots . . . (4.1)
$$

Table 4.1 lists typical values of $V_T$ and field effect mobility extracted from these curves.
**Figure 4.4:** (a) Shows drain current and log drain current Vs. gate voltage of 2/25 PMOS device for the double Si implant and the SiGe implant; (b) Shows drain current and log drain current Vs. gate voltage of 2/25 NMOS device for the double Si implant and the SiGe implant.
TABLE 4.1: Threshold voltages and field effect mobilities of NMOS and PMOS devices.

<table>
<thead>
<tr>
<th>GRP/SIZE</th>
<th>NMOS DEVICES</th>
<th>PMOS DEVICES</th>
</tr>
</thead>
<tbody>
<tr>
<td>L/W (um)</td>
<td>N Vt (V)</td>
<td>FE cm²/V-s</td>
</tr>
<tr>
<td>A 2/25</td>
<td>1.21</td>
<td>25.42</td>
</tr>
<tr>
<td>A 6/25</td>
<td>2.214</td>
<td>38.94</td>
</tr>
<tr>
<td>A 15/25</td>
<td>2.68</td>
<td>55.58</td>
</tr>
<tr>
<td>B 2/25</td>
<td>3.9</td>
<td>22.03</td>
</tr>
<tr>
<td>B 6/25</td>
<td>4.76</td>
<td>31.43</td>
</tr>
<tr>
<td>B 15/25</td>
<td>5.14</td>
<td>43.38</td>
</tr>
<tr>
<td>C 2/25</td>
<td>1.25</td>
<td>17.69</td>
</tr>
<tr>
<td>C 6/25</td>
<td>1.63</td>
<td>21.52</td>
</tr>
<tr>
<td>C 15/25</td>
<td>1.76</td>
<td>27.38</td>
</tr>
<tr>
<td>D 2/25</td>
<td>1.2</td>
<td>13.1</td>
</tr>
<tr>
<td>D 6/25</td>
<td>1.85</td>
<td>15.23</td>
</tr>
<tr>
<td>D 15/25</td>
<td>2.23</td>
<td>18.42</td>
</tr>
</tbody>
</table>

The following features are observed from this table.

The threshold voltage is increased with gate length.

- Significantly higher threshold voltages from NMOS devices in group B [Si-Ge] were observed.

- Significantly lower threshold voltages from PMOS devices in group B [Si-Ge] were observed.

The threshold voltages in all of these devices were not effected by substrate bias variation.
- The carrier mobility was observed to increase with gate length.
- NMOS transistors on group A [Si-Si] samples show the highest electron mobility.

PMOS transistors on group B [Si-Ge] samples show the highest hole mobility.

**Subthreshold current**

The drain current for $V_{gs}$ below the threshold value is called the subthreshold current. In the subthreshold regime the transistor is under weak inversion. The carrier drift is therefore not important and the current is dominated by diffusion [23]. From the variation of subthreshold current as a function of gate bias a parameter called subthreshold swing ($S/S$) is defined as the $V_{gs}$ difference per decade of current. The increase in $S/S$ reflects higher leakage current in the off state of the device.

The magnitude of $S/S$ is related to the interface trap density and therefore the interface trap capacitance according equation:

$$n = \frac{S/S}{\log(10) \Phi_b} \ldots \ldots (4.2)$$

$$n = 1 + \frac{C_b' + C_{it}'}{C_{ox}'} \ldots \ldots (4.3)$$
\[ D_{it} = \frac{C_{it}'}{q} \ldots (4.4) \]

\( O_b = 0.0259 \) V. \( C_b' \) is the substrate bulk capacitance per unit area. \( C_{it}' \) is the interface trap capacitance per unit area. \( C_{ox}' \) is the gate capacitance per unit area. \( D_{it} \) is the interface trap density, and \( q \) is the charge of an electron.

The interface trap density \( (D_{it}) \) is related to the nature of the Si/SiO\(_2\) interface in terms of the structure and defects present in the interface.

Table 4.2A gives the S/S and calculated values of \( C_{it}' \) and \( D_{it} \) for the NMOS devices with channel dimensions \( (L/W) \) 2/25.

Table 4.2B gives the S/S and calculated values of \( C_{it}' \) and \( D_{it} \) for the PMOS devices with channel dimensions \( (L/W) \) 2/25.

The following observations are made from these tables:

- Group D [non-implanted wafers] gave the lowest S/S in both types of transistors.
- The S/S for the PMOS devices in groups A, C, and D were less than those of the NMOS devices on the same substrate.
- In group B [Si-Ge] an exceptionally high S/S was observed.
Table 4.2A: results table for subthreshold swing and calculations for NMOS devices.

<table>
<thead>
<tr>
<th>IMPLANT</th>
<th>n</th>
<th>S/S V/dec</th>
<th>C_r F/cm²</th>
<th>D_r/cm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si/Si</td>
<td>11.365</td>
<td>0.677</td>
<td>3.84 x 10⁻⁷</td>
<td>2.4 x 10¹²</td>
</tr>
<tr>
<td>Si/Ge</td>
<td>8.83</td>
<td>0.526</td>
<td>2.75 x 10⁻⁷</td>
<td>1.7 x 10¹²</td>
</tr>
<tr>
<td>Ge</td>
<td>10.0</td>
<td>0.596</td>
<td>3.25 x 10⁻⁷</td>
<td>2.0 x 10¹²</td>
</tr>
<tr>
<td>None</td>
<td>8.56</td>
<td>0.510</td>
<td>2.63 x 10⁻⁷</td>
<td>1.65 x 10¹²</td>
</tr>
</tbody>
</table>

Table 4.2B: results table for subthreshold swing and calculations for PMOS devices.

<table>
<thead>
<tr>
<th>IMPLANT</th>
<th>n</th>
<th>S/S V/dec</th>
<th>C_r F/cm²</th>
<th>D_r/cm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si/Si</td>
<td>8.56</td>
<td>-0.510</td>
<td>2.63 x 10⁻⁷</td>
<td>1.65 x 10¹²</td>
</tr>
<tr>
<td>Si/Ge</td>
<td>35.25</td>
<td>-2.1</td>
<td>1.41 x 10⁻⁶</td>
<td>8.84 x 10¹²</td>
</tr>
<tr>
<td>Ge</td>
<td>8.73</td>
<td>-0.52</td>
<td>2.70 x 10⁻⁷</td>
<td>1.68 x 10¹²</td>
</tr>
<tr>
<td>None</td>
<td>7.81</td>
<td>-0.465</td>
<td>2.31 x 10⁻⁷</td>
<td>1.44 x 10¹²</td>
</tr>
</tbody>
</table>

4.3 Inverter Characteristics

The inverter transfer curves were plotted with V_DD = 10 V and Vin varied from 0 to 10 V. The inverter current was super imposed with the voltage transfer curve so they could be plotted at the same time.

Figure 4.5A shows the inverter plot for group A inverter with channel length equal to 2 and PMOS and NMOS widths equal to 24 μm and 12 μm respectively.

Figure 4.5B shows the inverter plot for group A inverter with channel length equal to 10 and PMOS and NMOS widths equal to 24 μm and 12 μm respectively.

- Groups A, C and D exhibited fairly comparable voltage
Figure 4.5: (a) Inverter plot of 2 um channel lengths showing a dip in the current peak (b) Inverter plot of 10 um channel length.
characteristics.
The current plots for groups A, C and D were also fairly comparable.
The output current increased for all the working transistors as the
gate length of the transistors in the inverter decreased.
Figure 4.5A showed a double peak in the inverter current plot.
The effect of the double peak diminished as the gate length of the
transistors in the inverter increased.
A change of gain was observed in the voltage transfer plot of figure
4.5A.
Group B did not have any working inverters.
The output voltage remained constant at 0.5 V with varying input
temperature.
Chapter 5 Discussion

5.1 Film Structure

The results show an improved electrical performance of devices which received double implants, in general. This can be attributed to the increase in grain size of the poly-Si film by solid phase epitaxy, especially in the Si-Si case.

The solid phase epitaxial grain growth is obtained by recrystallization of amorphous film with a few grains (nuclei) acting as seeds. Single Si implants at the poly-Si/SiO₂ interface have been largely employed for this purpose [5]. The use of double implants, (one near the surface and one at the Si/SiO₂ interface) enable amorphization throughout the film as is shown in the TRIM simulations in Figure 3.1. Emoto, et. al. have reported grain sizes up to a few microns in 0.2 um thick poly-Si using a double Si implant technique [6]. They employed anneals of 600°C for 100 hours in N₂. In the present study, annealing was performed at 625°C for 30 hours in N₂. However, with subsequent high temperature steps, (e.g. gate oxide growth, source and drain anneal, etc.), the grain size is expected to increase further.

Hunt [21] employed a single Si implant at the Si/SiO₂ interface with a similar anneal of 625°C for 30 hours in N₂ and did not show much change in the electrical performance as compared to those of the as deposited poly-Si devices. From these observations it is inferred that a double Si implant technique might have
resulted into better grain sizes and size distributions. No TEM could be performed on these samples because of the limited availability of a TEM.

The TEM structure of Si-Ge implanted and annealed samples show a distinct increase in grain size of the polysilicon film with an amorphous like top surface layer. It is obvious that the anneals this film underwent were insufficient to crystallize the top Ge implanted film layer. The RBS analysis confirms the dominant presence of Ge in this layer. King et al have reported that poly-Si-Ge films remained amorphous after a recrystallization anneal of 600°C for 24 hours in N₂ [12].

The annealing of continuous amorphous layers that extend to the Si surface has been found to occur by solid phase epitaxy at temperatures between 500 600°C [24]. That is, a recrystallization process occurs on the underlying crystalline substrate, and regrowth proceeds toward the surface. Impurities present may enhance or retard this regrowth. Apparently the presence of Ge in the polysilicon film is causing the retardation.

The TRIM simulations do not take into account the crystalline structure of the substrate. In the case of a single Ge implant in as deposited polysilicon films, Ge is expected to channel into the grain boundaries. These conditions may not result into the formation of a continuous amorphous layer [17]. At the same time Ge at the grain boundaries may prevent grain growth.

These studies show that it is necessary to preamorphize polysilicon films
prior to Ge implant to form a Si-Ge type of channel.

An insufficient grain growth in as deposited polysilicon might be the reason for high sheet resistance of the source and drain regions. The sheet resistance was calculated from four point probe measurements on wafers that received no substrate implants and was found to be much higher than simulated. The sheet resistance value may be increased in future processing by increasing grain sizes. This might occur because the number of grain boundaries would be less and therefore, the number of dopant ions to be trapped would be less. A SiGe alloy, on the other hand, requires lower dopant activation energy than Si. It therefore follows that the sheet resistance of a Ge implanted wafer might have be lower than those measured [12]. The ionization energies for donor and acceptor centers are lower for Ge than Si. The ionization energies for Phosphorous in Ge and Si are 0.012 ev and 0.045 ev respectively and the ionization energies for Boron in Ge and Si are 0.0104 ev and 0.045 ev respectively [25]. This information brings about a positive aspect in the application of TFTs in stacked CMOS, where low temperature processing is necessary.

5.2 Electrical Properties

5.2.1 Threshold Voltage

Threshold voltages of devices are affected by a number of non-idealities present. Most of these bring variation in the flat band voltage, Vfb, given by equation 5.1.
$V_{fb}=\Phi_{MS}+\frac{Q_g}{C_{ox}} \ldots \ldots \ldots (5.1)$

Where $\Phi_{MS}$ is the work function difference between the gate and the substrate. The work function difference will change with the type of substrate and the concentration of the dopant for the same gate electrode. For example an N-type substrates will have a smaller $\Phi_{MS}$ than a P-type substrate for an N$^+$ gate. In the present study, an intrinsic polysilicon substrate and an N$^+$ polysilicon gate is used. The $\Phi_{MS}$ is therefore around 0.56 ev for both PMOS and NMOS devices.

The number of grains in the gate region has a large effect on threshold voltage as can be seen by the increase in $V_T$ for increase in channel lengths. This has been explained under the discussion on field effect in polysilicon in section 2.1.

Virtually all of the devices did not show a change in threshold voltage with a change in the substrate bias. This acknowledges the fact that the bulk substrate is totally depleted. One could also look at the swing of the threshold voltage and come to the conclusion that the traps had to be donor traps because it required a larger threshold voltage to turn on the PMOS devices. Therefore more holes than electrons had to be generated to fill the traps before the inversion layer could form for the PMOS TFT. This larger negative shift for groups A, C and D could insinuate that the interface traps played a large role a well. The calculated density of interface traps and interface capacitance per unit area can be seen in Table 2.
The values of interface trap densities calculated for all the groups except for B seemed to be slightly larger for the NMOS devices than the PMOS devices. The threshold voltages of the NMOS devices were slightly lower in group C than in A and the PMOS threshold voltage were slightly larger indicating a slight difference in the possible oxide fixed charges. The slight negative trend might be able to be attributed to a larger number of positive charges in the oxide. The Germanium present in the polysilicon of group C might have an effect on the gate oxide fixed as well as the interface charges.

Group B, on the other hand, behaved oppositely of all the other groups. The PMOS threshold voltages were actually less in magnitude than the NMOS threshold voltages for group B. An explanation for this might be because germanium grain boundaries are strongly P-type so barriers form only for electrons [26]. The explanation was for a pure Ge semiconductor, but maybe the Si-Ge alloy retains some of the Ge qualities. From the increased magnitude of $V_T$ for the NMOS devices it follows that the interface traps behaved as acceptor like and require more electrons to invert for the NMOS device. The PMOS devices from group B had the largest subthreshold swing and thus the largest interface trap density and interface capacitance. The large number of interphase traps brought about a very leaky device. Figure 5.1 shows an I-V curve of the source and substrate junction in the PMOS device. An excessive reverse leakage current can be observed, which can be directly related to the corresponding increase in carrier
mobility and trap density.

5.2.2 Mobility

The field effect mobilities extracted from the devices are found to increase with the channel. This increase in mobility with gate length can be attributed to the velocity saturation effects. As the channel gets smaller, the field from drain to source increases. Once the field becomes greater than the critical field ($\varepsilon_c$), the effective channel is no longer equal to $L$ drawn. It becomes smaller and the mobility decreases as the field increases above $\varepsilon_c$. According to the following equation.

$$\mu_{\text{eff}} = \frac{\mu_0}{1 + \frac{1}{V_{gs} - V_t} \times \frac{V_{ds}}{\varepsilon_c}}$$

Where $\mu_0$ is the mobility extracted from a long channel device in the linear region and $\mu_{\text{eff}}$ is the effective mobility.

Figure 5.2 shows the plot of electric field Vs. velocity of carriers. From the plot and equation 5.3, one can observe the mobility decrease with increasing field.

$$\varepsilon_c = \frac{1}{\mu} \frac{V_{ds}}{V_{ds}} \times V_{max}$$

The mobility for the group B wafers increased from 38 cm$^2$/V-s for $L$ equal to 2 um to 66 cm$^2$/V-s for $L$ equal to 15 um. The mobility of the group A wafers
Figure 5.1: The plot shows the reverse substrate/drain diode leakage of a 2/25 PMOS device in a SiGe implanted wafer.

Figure 5.2: Plot illustrating velocity saturation effects with increased field.[23]
increased from 18 cm²/V-s to 44 cm²/V-s for the same gate lengths respectively. The increase was approximately 26 cm²/V-s for both groups of wafers. The percentage increase in mobility for the small channel length device for different implant conditions was larger. There was over a 100 % increase from group A to B for L equal to 2 um and only 66% increase in mobility for L equal to 15 um. From this it can be concluded that the SiGe channel has a greater benefit in mobility for the smaller channel devices, indicating mobility enhancement in the grains.

The mobilities for groups A, C and D were smaller, for the PMOS devices than the NMOS devices. The mobilities of the NMOS devices were not as close as was expected to being twice that of the PMOS devices. Again one must assume the traps in the polycrystalline structure cause this effect. As a matter of fact, the PMOS mobilities were about 20% less than those of the NMOS devices in group A and 30% less in group C.

The mobilities for the PMOS and NMOS devices in group B did not exhibit the same trend as the other groups. In this group, the mobilities of the holes in the PMOS devices were much larger than the mobilities of the NMOS devices. Even though the hole mobility was greater than electron mobility in group B, the electron mobility was greater than all the other groups except for group A. This indicated that the Si-Ge implant increased the hole mobility to a greater extent than
the electron mobility.

The increase in hole mobility can partially be explained by the theory of hole confinement, and partially by the fact that a Si-Ge alloy is favorable to carrier transport. Assuming a Si-Ge channel below the polysilicon surface, (which is actually detected), a schematic band diagram can be constructed base on theoretical considerations described in section 2.4. As shown in Figure 5.3 and inversion layer can be anticipated in the region A-B before the surface under goes inversion. This forms a buried channel for the holes to collect which do not encounter surface scattering effects, increasing the overall mobility. Figure 5.4 show hole mobility plotted against $V_{GS}$ for Si-Ge and Si-Si implanted samples. A decrease in mobility with increased field indicates the presence of surface scattering effects.

Another factor has to be presented in order to explain the large decrease in mobilities of both hole and electrons in group C. Group C received only a surface Ge implant. As discussed earlier, this group of samples did not recrystallize giving essentially similar electrical properties as those obtained in as deposited films.

5.2.3 Subthreshold Current

The grain size and structure of the substrate is expected to influence the subthreshold current since the current is dominated by diffusion in this regime. Group D displays the smallest subthreshold swing for both NMOS and PMOS
Figure 5.3: (a) Poly-Si-Ge implanted film at flat band; (b) Poly-Si-Ge film with channel under inversion to show hole confinement
devices. This indicates a smaller interface trap density in these samples. The thin film polysilicon used assisted in reducing the leakage. The side wall area of the drain is the only region for possible leakage to the substrate since the source/drain regions extended throughout the film. The decrease in substrate thickness increases the bulk capacitance and thus the theoretical subthreshold swing as well. The theoretical subthreshold swing is calculated assuming the substrate to be completely depleted during operation neglecting the interface trap capacitance. Then using equations (4.2) and (4.3), a S/S of 0.146 V/decade was calculated assuming Si as the substrate in all cases. The drastic increase in leakage in Si-Ge samples can be attributed to the presence of crystalline damage in the channel and the increase in mobility. The large S/S gave a large calculated value of density of interface traps. Studies have shown that Ge implanted Si oxidizes at the same rate as Si when outside the linear regime of growth [22,27]. The solid solubility of Ge in SiO₂ and Si were small. Therefore, during oxidation the Ge piles up at the SiO₂/Si interface, creating a smoother interface. That may explain lesser leakage observed in NMOS devices in Si-Ge samples.

5.2.4 Drain Currents

A direct correspondence between mobility and drain current is not observed. Out of all the NMOS devices, group B had the second largest of mobilities and had the lowest current output of all the NMOS devices. Group D had the worst NMOS mobility and found itself next in line for current output. Then came group C
followed by group A.

Even though some of the currents extracted from the NMOS plots are low, they are still greater than their PMOS counterparts. This indicates that electron transport is facilitated over the hole transport in these substrates. However, the group B PMOS characteristic curve exhibited much higher currents than the NMOS curve from the same substrate. These PMOS devices had the highest mobilities of all the PMOS and even NMOS devices. The currents of these PMOS devices were larger than any of the currents exhibited from the NMOS devices for equal magnitudes of \( V_{GS} \), including those from group A. The increase in current was attributed to hole confinement in the Si-Ge buried channel. This current was obtained from a device where the substrate had poor grain structure and no passivated grain boundaries. With enhanced grain sizes and passivated grain boundaries, the currents and mobilities could be increased even higher while decreasing the subthreshold swing.

As was mentioned earlier, the increased current outputs of the devices didn’t always correspond to increase in mobility. For the PMOS devices, the mobility of group A is the second highest, but the current output is the lowest. Groups D and C which have much lower mobilities have greater current output. This occurrence is attributed to the selectivity of the traps in the grain structure to allow certain carriers to flow. Group D allows hole to flow more freely than group A, which we assume have different grain structures.
There seems to be a switching of roles. Group A exhibits good currents for the NMOS devices and really low currents for the PMOS device. Group B on the other hand exhibits the exact opposite favoring hole current over electron current. Both of these exhibit conditions that would provide satisfactory qualities for one type or the other, but not both. Selectively implanting Ge in PMOS channels might be performed to increase the current output to a fairly equal level as the NMOS devices of group A. This could also provide an application in stacked CMOS SRAM technology for a PMOS TFT pull-up stacked on top of a NMOS device in the silicon substrate.

5.2.5 Inverter Analysis

As is expected the behavior of the individual transistors effected the transfer characteristics of the inverters. All of the inverters had to be tested with a 10.0 volt supply and Vin from 0 to 10 volts. The reason 10 volts had to be used was because some of the devices didn’t turn on until 4 or 5 volts. Most of the devices with the smaller channel lengths are found to break down between $V_{DS}$ of 5 and 10 volts. The breakdown occurs at lower voltages for smaller gate lengths, so the transfer plots of the 2 um and 4 um channel lengths are rather interesting. The output voltage displays a kink half way through the transition from high to low. There was a change in slope at this kink, which displayed a change in gain. The lengths of the pull-up and pull down transistor were kept constant while changing the width keeping a two to one ratio of pull-up to pull-down. As the length of the
devices increased so did the gain and the kink seems to disappear for lengths of 10 um or greater. Figure 4.5A shows a double current peak output from a group A inverter with channel length of 2 um.

The double peak is analyzed much more in depth by isolating gate voltages and overlaying PMOS and NMOS characteristic curves to track the current of the inverter given by the two devices. Figure 5.5 shows the overlay plot of the NMOS and PMOS current/voltage characteristic curves with the current dip. The current dip is caused by the intersection of the breakdown portions of the curves. The narrower transistors began to break down long before $V_{DS}$ of 10.0 volts was reached. The longer devices didn’t break down at lower voltages and the inverters behaves normally with larger gains. The increase in gain is also attributed to the device operating in breakdown. The smaller devices going into break down didn’t allow for the smooth transition. A $V_{DS}$ of 10 volts is to high for such small channel lengths, but the threshold voltage of the PMOS device is larger than 4.0 volts. For example, group A has low NMOS $V_T$s but high PMOS $V_T$s. Both devices must turn on in the operation of the inverter. The NMOS device turns on at low values of $V_{GS}$, but the PMOS device needs a larger supply voltage to get the higher $V_{GS}$ needed to turn on.

The maximum current generated by the inverters in group A is around 40 uA. This can only be increased by increasing the current output of the worst working device on the substrate, or by designing the pull-up and pull-down devices
to drive comparable amounts of current. Combining the PMOS device of group B, minus the leakage problem, and the NMOS device of group A would allow for a much improved inverter.

The inverters on the substrates from group B did not function as inverters. The output voltage remained constant around 0.5 volts with the changing input voltage. The pull-up and pull-down devices were a very bad match as far as current output was concerned. The pull-up was designed to drive twice as much as the NMOS pull-down. The PMOS device was already showing 16 times more current with the same size device. Now imagine the size ratio doubles the current to give 32 times more current from the pull-up as the pull-down. The overlay plot illustrates a relatively constant low current value. The low current is not enough to turn off or turn on either of the transistors totally creating a voltage divider and, thus giving a constant voltage at the output.
Chapter 6 Conclusion

The fabrication of the first Si-Ge channel MOSFETs in thin film polysilicon was accomplished. A Si-Ge channel was formed by a long low temperature anneal after the Si and Ge implants. The buried channel only occurred when Ge was implanted following a high energy, high dose Si implant to amorphize the film so as not to allow channeling of the Ge ions. The Si-Ge channel brought about a remarkable improvement in hole mobility, but no such increase in electron mobility. The Si-Ge buried channel accomplished hole mobility increase by allowing hole confinement to take place as was described for single crystalline devices in section 2.4. The dramatic increase in drain current brought about an increase in leakage current which may be due to the presence of a damaged surface layer. The leakage current can be minimized with further grain size enhancement and passivation techniques.

The method of implanting Ge to form a buried Si-Ge channel is simple and compatible with existing integrated circuit technologies. This work is a step in the right direction for the improvement of PMOS TFTs to be implemented in Stacked CMOS designs. This work opens new areas of channel engineering in Polysilicon Thin Film Transistors.
References


Bibliography


APPENDIX A

XTEM SAMPLE PREPARATION

Apparatus and materials needed for XTEM sample preparation:

- Silicon and GaAs (GaAs with surface of interest)
- heat gun (Master Appliance Corporation model # HG1301U)
- Methanol and Acetone
- Ultrasonic Disc Cutter (Gatan model # 601)
- Minimet Polisher (Buehler)
- Dimpler (VCR Group model #D500)
- Light table
- high power light source (Bausch and Lomb cat. no. 31-35-28)
- Bransonic 12 Ultrasonic Bath
- Ion Miller (VCR Group)
- fine point tweezers
- Epo-Tek H20E epoxy
- cross section sandwich jig
- small vice clamps
- razor blades, glass slides, glass discs, Scotch Brite pads
- glycol phthalate or white wax (#7036, J. H. Young Co., Inc.)

Introduction

In order to prepare a sample with the intent to examine its morphology in cross-section by transmission electron microscopy, a many step sample thinning procedure is used. As there are few, if any, analytical techniques capable of examining microstructural features at the nanometer level, the labor required is intensive based on the need to prepare suitably thin sample is currently justifiable.
Sandwich Gluing

The sandwich structure is glued from six 1x3 mm pieces five of which are silicon and one that is GaAs. First, this procedure is started with a large piece of thin film substrate deposited on a GaAs substrate wafer, several 1x3 mm slices (each about 0.5 mm thick), are cut by a wafer dicing saw (see FIG. 1-1). Second, the GaAs should be cleaned before it is glued, so to do so put the GaAs along with methanol in a small peatry dish. The dish should then be placed in an ultrasonic bath for about 10 sec. The Si used in the sandwich should also be cleaned in the same way as the GaAs. Both the Si and the GaAs should be dry before using them in the sandwich. In the next step Epo-Tek H20E epoxy is mixed from two parts of equal amounts and must be made with care to be ensured of a solid bond. Place a small amount (about 5 mm in diameter x 2 mm) of the epoxy resin (part 'A') and an equal amount of hardener (part 'B') on a glass slide. These two parts should be mixed together thoroughly in circular motions (both clockwise 50 times and counter-clockwise 50 times, about two minutes) to make sure that both parts are completely and evenly concentrated throughout the epoxy mixture. [If the glue is not mixed properly it might result in the sample breaking when it becomes stressed during the procedure that follows.] Using this special electrically conductive epoxy, one slice of the GaAs is glued together with a pure silicon piece with the surface of interest facing this first Si piece. [The surface of interest on the GaAs should not be touched by a finepoint tweezer because of the damage it might cause but is handled by grabbing it by the other sides of this slice.] (see FIG 1-2) At this point the geometry of the sandwich is 1x1x3 mm. (see FIG 1-2B) Then on each side of this two piece structure is glued two extra pure Si 1x3 mm slices so that a total of 6 slices is used to make this sandwich. In this six-slice structure, that has an approximate dimension of 1x3x3 mm, the GaAs surface of interest is positioned in the middle. The good surface of the GaAs piece is facing the side of the sample with the three Si pieces. As in most semiconductor materials (Si or GaAs) it is important to know consistently where the surface of interest is located at, from the beginning and this is why the GaAs is positioned in this fashion. The sample is then placed in the cross section sandwich jig and put in an oven. [The sandwich jig should be cleaned of all excess dust and debris to allow for the best bond possible.] The jig should be cleaned using Scotch Brite pads and the dust remaining then needs to be wiped off. The mold should also be lightly oiled (Pam non-stick oil) to prevent
sample from sticking. The sandwich jig should then be placed in an oven and heated for 1 hour at 150° C.

First Thinning

After the epoxy has been thermally set by heating in an oven for approximately 1 hour (at about 150° C), the sandwich jig is allowed to cool and the sandwich is removed so that it can be mechanically sanded down. The sandwich structure is then rigidly set in glycol phthalate or white wax (#7036, J. H. Young Co., Inc.) on a glass disc. This is done by heating the surface of the glass disc with a heat gun and melting the glycol phthalate on to it. The sample is then placed in the molten liquid and pushed down with a moistened finger to minimize the amount of wax under the sample. The wax is then molded around the edges to increase its mechanical strength so the sample does not become freed in the polisher. [If the sample should fall into the polisher it would be lost.] One of the 3x3 mm faces is mechanically sanded down, using a 30 micron diamond studded polishing disc, until the dimension of the block is about 0.8x3x3 mm. A 15 micron diamond studded polishing disc is then used until the dimension of the block is about 0.7x3x3 mm. Both polishing discs must be cleaned after each use by ultrasonically buzzing them in acetone and methonal.

Sample Cutting/ First Dimpling

This structure is then set onto a dimpling platen using the same wax as before so the sample can be cut and dimpled. The sample should be placed on the platen so the interface of the first silicon piece and the second silicon piece on the good side is on the center line (see Fig 2-1). The sample is ultrasonically cut into a 3 mm diameter x 0.7 mm thick disc (see FIG 3-1) and the sanded 3x3 mm face is dimpled with a round metal tool. (polishing wheel number 4 of the VCR Dimpler) A 3.0 micron diamond slurry is used to dimple about 20 to 30 microns of of this mechanically sanded surface. (see FIG 4-1) A different polishing tool (polishing tool number 2 ,with polishing pad, of the VCR Dimpler) and the same 3.0 micron diamond slurry are used to polish the sample. After 15 minutes the sample should have a "mirror-like shine" to its surface. The small grinding particles used in the second polishing step removes much of the mechanically damaged surface area introduced in the first mechanical thinning step. The dimpling process produces a crater-like depression on that surface in order to produce a thin inner
portion and a thick outer region. In order to mechanically strengthen this sandwich structure, the sandwich is first freed from the acetone soluble glycol phthalate by placing the platen in a small beaker filled with acetone. This beaker is placed in an ultrasonic bath until all the visible wax is gone. At this point remove the beaker from the ultrasonic bath and allow the rest of the wax to dissolve. [The sample should be removed from the ultrasonic bath after all the visible wax is gone because any further exposure to this stress might cause the sample to break] Once the sample is free of the wax then remove it with a fine point tweezer.

Griding

The acetone will dull the shine on the sample so it is rinsed in methanol until the shine returns and then a 2.0x1.5 mm slotted copper grid (No. 29150, Ernest F. Fullam, Inc.) is epoxied onto this dimpled polished face. The same epoxy is used as before and should be made using the same procedure. The grids have a shiney and dull side but the dull side is the one that makes a better bonding surface. The dull side is placed in the glue and great care is taken to ensure that no epoxy is accidentally left in the region of interest or the shiney side of the grid. This is because the epoxy does not thin easily in the ion miller. The sample is put in a small vice or clamp so that the grid is held in place while heating. The sample is then placed in an oven and heated for one hour (at about 150° C). With this copper grid in place, the sandwich disc becomes less prone to fracturing especially during the subsequent polishing steps (see FIG 5-1). [If the grid hangs over the edge of the sample after it comes out of the oven then it must be removed with a very sharp razor blade because it may not fit in the TEM if it is larger than the 3 mm diameter required.]

Second Thinning

This disc is now turned upside down, and re-set in white wax (glycol phthalate) for mechanical thinning. The sample will be very thin and if the sample is not firmly in the wax it will cause the
sample to become free in the following steps and once free, it can be easily damaged. The wax should be completely molten and the sample should be firmly pushed down with a moistened finger to produce good adhesion. The reverse 3 mm diameter face is now mechanically sanded until the sandwich is about 300 microns thick with the 30 micron diamond polishing disc. Then the sample is thinned to about 120 or 130 microns using the 15 micron diamond polishing disc. Again the polishing discs need to be cleaned in acetone/methanol routinely.

Second Dimpling

This second 3 mm diameter face is also dimple polished to produce a second crater-like depression. First, the sample is dimpled 20 microns down using the mirometer indicator. Next, the depth is very carefully dimpled down in 5 micron steps until one can observe transmitted red light when placed on top of a powerful light source. The thickness at the bottom of this cavity is estimated to be approximately 10 microns. This surface is then polished with a number two wheel, with a velvet pad, using a 3.0 micron diamond slurry, at 10 minute intervals, until this surface turns out to be orange on the high powered light source. (the orange area should be located on the first Si piece next to the surface of interest see Fig. 6-1a) If the red or orange area is over toward the first and second silicon interface (see Fig 6-1b) the sample should be further polished until the interface of the first silicon and GaAs is orange (red on the light table) even if there is a visible hole in the sample at the first and second silicon interface (area labeled 'Red Area' in Fig. 6-1b.). Alternatively it may also be checked by placing the platen on a light table, a low powered light source, to see if the first silicon and the GaAs interface is red by this source. It is very important that the sample be thin enough so that the time required for ion milling is short. This is done because it seems the less time the sample is milled the better the quality of the specimen. At this time there is also mirror shine to this surface. At this point the thin disc is careful removed from the glycol phthalate using acetone. [Do not use the ultrasonic bath at this stage it could cause the sample to break.] The sample is again rinsed in methanol to get rid of the dull residue left from the acetone and placed in the ion mill.
Ion Milling

The sample needs to be ion milled, which is the finest part of the thinning procedure, and produces the thin areas needed for TEM work. When removing the sample it is important to grab the sample by the edge where the grid is located and not in the middle so the sample doesn't get damaged or broken. The final thinning step is carried out in an ion milling instrument in which both faces of the dimpled disc are simultaneously bombarded by several KV of collimated Ar+ ions. The sample is first placed in the ion milling instrument at a 90° angle to the guides or scratch lines. (see Fig. 7-1) The initial ion milling condition is set at 5.0 KV and 25°. At this angle, the thinning rate is fairly rapid, although somewhat uneven, as fragments of the material are bombarded off by the relatively heavy Ar+ ion, and this condition is used until the central dimple polished area is punctured through (hole diameter ~ 0.05 mm). The final ion thinning step is carried out at 5 KV and 13° to 15° until a larger hole (diameter ~ 0.5 mm) appears in the middle of the disc. This final condition is used because the lower glancing angle of the ions have a polishing effect resulting in a relatively large and smooth area around this hole and this region is thin enough (<3000Å) for TEM observations. Although this procedure is quite involved, it produces large thin areas that reveals much about the structure and phases that are present, as a function of depth, in many systems, including the GaAs structure.

Incidental Maintenance

When the polishing pad on the dimpling tool (tool number 2 VCR Dimpler) has become worn down it must be replaced. The old pad should be removed by pealing it off. The tool should then be placed in acetone and ultrasonically buzzed (about 15 seconds) to remove the old glue residue. The tool should then be rinsed off with methanol and allowed to dry, this will create a good bonding surface for the new polishing pad. A new strip of polishing pad (Buehler Polishing Cloth catalog no. 40-7738) should be cut off and the backing removed from it. The pad is placed on the tool and firmly pressed into place with thumb. The excess at the end and on the sides are cut off using a sharp razor blade.
FIG 1-2

GaAs should be handled by these sides.

Surface of interest

GaAs

GaAs

GaAs surface of interest

Gluing

Dicing

Wafer-saw

1 mm x 3 mm slices

0.5 mm

FIG 1-2B

Si (dull side)

GaAs surface of interest

FIG 1-1

SAMPLE PREPARATION FOR CROSS-SECTION TEM OBSERVATION

A-7
Mechanical support
copper disk

Glue on support disk

Disc-cutter

Dimpled 20 μ
and polished
15 minutes

0.7 mm thick

Surface of
interest

TOP VIEW OF SAMPLE

0.7 mm thick

Fig 2-1

Fig 3-1

Fig 4-1

A-8
Glass Disc

Si

Centering Lines

copper grid
Mechanical support

GaAs

FIG. 4-1

FIG. 5-1
Sample Hole

Scratch Lines (parallel to 2 of the screws)

Screw Holes

Sample Stage

Si

Sample Stage Cover

Fig 7-1

Fig 7-2

Fig 7-3

A-12
MOSIS
SCALABLE & GENERIC
CMOS
DESIGN RULES

February 1988
Revision 6
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<td></td>
</tr>
<tr>
<td>CONT to POLY</td>
<td>CCP</td>
<td>47</td>
<td></td>
</tr>
<tr>
<td>CONT to ACT</td>
<td>CCA</td>
<td>48</td>
<td></td>
</tr>
<tr>
<td>METAL1</td>
<td>CMF</td>
<td>49</td>
<td></td>
</tr>
<tr>
<td>VIA</td>
<td>CVA</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>METAL2</td>
<td>CMS</td>
<td>51</td>
<td></td>
</tr>
<tr>
<td>CONT to ELEC</td>
<td>CCE</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td>ELECTRODE</td>
<td>CEL</td>
<td>56</td>
<td></td>
</tr>
<tr>
<td>OVERGLASS</td>
<td>COG</td>
<td>52</td>
<td></td>
</tr>
</tbody>
</table>

B-3
TECHNOLOGIES AND REQUIRED LAYERS

<table>
<thead>
<tr>
<th>PROCESS TECHNOLOGY</th>
<th>REQUIRED LAYERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWELL AND</td>
<td></td>
</tr>
<tr>
<td>N SUBS THIN TUB</td>
<td>SCP</td>
</tr>
<tr>
<td></td>
<td>CWP</td>
</tr>
<tr>
<td></td>
<td>CSN, CSP</td>
</tr>
<tr>
<td>N WELL AND</td>
<td></td>
</tr>
<tr>
<td>P SUBS THIN TUB</td>
<td>SCN</td>
</tr>
<tr>
<td></td>
<td>CWN, CSN, CSP</td>
</tr>
<tr>
<td>ALL *</td>
<td>SCG</td>
</tr>
<tr>
<td></td>
<td>CWG, CSG</td>
</tr>
<tr>
<td>ALL **</td>
<td>SCE</td>
</tr>
<tr>
<td></td>
<td>CWP, CWN</td>
</tr>
<tr>
<td></td>
<td>CSP, CSN</td>
</tr>
</tbody>
</table>

* For a P well or N subs thin tub process, MOSIS sets CHP=CHG and CSP=CSG

For an NWELL or P SUBS THIN TUB PROCESS, MOSIS sets CWN=CHG and CSN=CSG

** For a P well or N subs thin tub process, MOSIS ignores CWN

For an NWELL or P SUBS THIN TUB PROCESS, MOSIS ignores CWP
1. WELL
(NWELL,PWELL)

1.1 WIDTH 10

1.2 SPACE DIFF. POT. 9

1.3 SPACE SAME POT. 0 or 0

SAME POT. DIFF. POT.

Note: If both p and n wells submitted, they may not overlap but they may be coincident.
2. ACTIVE

2.1 Width
2.2 Space
2.3 Source/Drain Active to Well Edge
2.4 Subs./Well Contact, Active to Well Edge

Lambdas

3
3
5
3
4. SELECT (PSELECT, NSELECT)

4.1 Select space (overlap) to (of) channel to ensure adequate source/drain width

4.2 Select space (overlap) to (of) active

4.3 Select space (overlap) to (of) contact to well or substrate

4.4 Min width and space

Select for XTOR

Note: If both PSELECT and NSELECT submitted, they may be coincident but must not overlap.
5B. DENSER CONTACT TO POLY

5B.1 Contact size: exactly 2x2
5B.2 Poly overlap of contact 1
5B.3 Spacing on same poly 2
5B.4 Spacing on diff poly 5
5B.5 Space to other poly 4
5B.6 Space to act: one contact 2
5B.7 Space to act: many contacts 3

Note: Your associating contacts with poly or active allows MOSIS to independently float the layer and the layer overlap of the contact.
6B. DENSER CONTACT TO ACTIVE LAMBDA

6B.1 Contact size, exactly 2x2
6B.2 Active Overlap 1
6B.3 Spacing on Same Active 2
6B.4 Spacing on Diff Active 6
6B.5 Space to Diff Active 5
6B.6 Space to Gate 2
6B.7 Space to Field Poly, One Cont. 2
6B.8 Space to Field Poly, Many Cont. 3
6B.9 Space to Contact to Poly 4

[Diagram showing contact and spacing configurations]
7. METAL1

7.1 Width 3

7.2 Space to Metal1 3

7.3 Overlap of Contact to Poly 1

7.4 Overlap of Contact to Active 1
8. VIA

8.1 Size, exactly 2x2

8.2 Separation to Via 3

8.3 Overlap by Metal1 1

8.4 Space to Poly or Active Edge 2

8.5 Space to Contact 2

NOTE: Objective Is Via on a Flat Surface. Via Stacked Over Contact NOT Allowed.
9. METAL2

9.1 Width

9.2 Space to METAL2

9.3 Overlap of VIA

LAMDBAS
APPENDIX C

Scribe P-type, 5-15 ohm-cm, <100> wafers and RCA clean

Grow ~0.65 um SiO₂

Deposit ~0.2 um Poly
610°C, 22 min.

5 wafers A1-A5
Si implant dose=1X10¹⁵ @150 kev =1X10¹⁵ @40 kev

and
5 wafers B1-B5
Si implant dose=1X10¹⁵ @150 kev
Ge implant dose=1X10¹⁶ @85 kev

and
5 wafers C1-C5
Ge implant dose=1X10¹⁶ @85 kev

and

2 wafers non implanted Poly

Poly Substrate 200 nm ISOLATION SiO2 650 nm

<100> P-type Silicon

Pattern into islands
RIE 75 watts 75 mtorr.
SF₆/O₂ 30:3 sccm
A1-A4, B1-B4, C1-C4, E1, E2
* use poly dummy with pattern to find etch rate.
* worsts case 4352 A/min (etched for 45 sec)

Strip resist
piranha 3:1 $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$ 15 min.

Special RCA Clean to remove few nanometers of poly
HF dip/rinse/APM/rinse continue 4 times
HPM dip/rinse

Poly grain enlargement (on wafers A1-A4, B1-B4, C1-C4,
D1-D3, E1, E2) anneal tube 16, 625°C 30 hr. 2.5 lpm $\text{N}_2$

**Take some samples for TEM
**(one of each different implant)

Gate oxide Growth
$\text{O}_2$ with TCA bubbler (25°C)
$\text{O}_2$ 4.0 lpm, TCA $\text{N}_2$ source 189 sccm
tube clean for 15 min. @ 900°C

Insert wafers 12 in/min.
Ramp 900-1100°C 10/90 $\text{O}_2/\text{N}_2$ (0.5/4.5 lpm) 15 min.
Soak 1100°C 4.0 lpm dry $\text{O}_2$ 13 min.
Ramp down 1100-900°C 4.5 lpm $\text{N}_2$ 30 min.

Immediate poly-si deposition of
gate electrode $\approx$0.5 um
610°C, 60 min.

Dope gate electrode, Spin on dopant
(Emulsitone N-250) spin @ 3 krpm 10 sec.
**Perform APM prior to spin-on.
Bake @ 180-190°C 15 min.
diffusion @ 900°C 20 min 10/90 O₂/N₂ (0.5/4.5 lpm)
deglaze recoat N-250 bake @ 180-190°C 15 min.
Diffusion @ 900°C 8 min.

Etch Glass (degaze) BOE

Pattern mask #2 and gate Etch in
RIE (same as isolation etch Param)

Resist Ash
N⁺ Poly Gate

<100> P-Type Silicon

P⁺ boron source/drain implant Mask #3
1x10¹⁵ atm/cm³ 35 kev

Resist Ash

N⁺ source/drain implant Mask #4
1x10¹⁵ Atm/cm³ 60 kev

Resist Ash
P+ Implant

N+ Implant

<100> P-Type Silicon

Implant anneal
Grow ~200 A Oxide over gate poly
Soak 900°C 35 min. 5 lpm dry O₂

LTO deposition for passivation oxide
use a lot of baffles to attempt to get
more uniform deposition.
400°C ~0.2 um
deposit time 80 min.

densification of LTO
900°C, dry O₂ 51pm, 10.0 min

LTO Passivation Layer
200 nm

<100> P-Type Silicon

Perform LTO oxide etch test
Pattern Contact Mask #5
Etch contact oxide in BOE
Ash Resist and STD. RCA Clean

LTO Passivation Layer 200 nm

Contact Cuts

<100> P-Type Silicon

Pre-sputter Dehydration bake

Sputter Al ~0.8um

Mask #6 pattern Al and Etch in Al etch

Ash Resist.

Test
### APPENDIX D

<table>
<thead>
<tr>
<th>Time (sec)</th>
<th>Event Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>10, 9</td>
<td>Ramp rate</td>
<td>10000 RPM/sec</td>
</tr>
<tr>
<td>20, 10</td>
<td>Spin speed</td>
<td>500 RPM</td>
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<tr>
<td>30, 11</td>
<td>Time</td>
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<tr>
<td>40, 2</td>
<td>Dispense</td>
<td>1 on DI water</td>
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<tr>
<td>50, 11</td>
<td>Time</td>
<td>10 tenthsec</td>
</tr>
<tr>
<td>60, 2</td>
<td>Dispense</td>
<td>0 off DI water</td>
</tr>
<tr>
<td>70, 11</td>
<td>Time</td>
<td>10 tenthsec</td>
</tr>
<tr>
<td>80, 1</td>
<td>Dispense</td>
<td>1 on developer</td>
</tr>
<tr>
<td>90, 11</td>
<td>Time</td>
<td>40 tenthsec</td>
</tr>
<tr>
<td>100, 10</td>
<td>Spin speed</td>
<td>0 RPM</td>
</tr>
<tr>
<td>110, 11</td>
<td>Time</td>
<td>20 tenthsec</td>
</tr>
<tr>
<td>120, 1</td>
<td>Dispense</td>
<td>0 off developer</td>
</tr>
<tr>
<td>130, 11</td>
<td>Time</td>
<td>200 tenthsec</td>
</tr>
<tr>
<td>140, 10</td>
<td>Spin speed</td>
<td>500 RPM</td>
</tr>
<tr>
<td>150, 11</td>
<td>Time</td>
<td>10 tenthsec</td>
</tr>
<tr>
<td>160, 1</td>
<td>Dispense</td>
<td>1 on developer</td>
</tr>
<tr>
<td>170, 11</td>
<td>Time</td>
<td>30 tenthsec</td>
</tr>
<tr>
<td>180, 10</td>
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<tr>
<td>190, 11</td>
<td>Time</td>
<td>20 tenthsec</td>
</tr>
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<td>200, 1</td>
<td>Dispense</td>
<td>0 off developer</td>
</tr>
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<td>210, 11</td>
<td>Time</td>
<td>250 tenthsec</td>
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<tr>
<td>220, 10</td>
<td>Spin speed</td>
<td>500 RPM</td>
</tr>
<tr>
<td>230, 5</td>
<td>Dispense</td>
<td>1 on DI water</td>
</tr>
<tr>
<td>240, 11</td>
<td>Time</td>
<td>200 tenthsec</td>
</tr>
<tr>
<td>250, 11</td>
<td>Time</td>
<td>100 tenthsec</td>
</tr>
<tr>
<td>260, 5</td>
<td>Dispense</td>
<td>0 off DI water</td>
</tr>
<tr>
<td>270, 10</td>
<td>Spin speed</td>
<td>5000 RPM</td>
</tr>
<tr>
<td>280, 11</td>
<td>Time</td>
<td>200 tenthsec</td>
</tr>
<tr>
<td>290, 10</td>
<td>Spin speed</td>
<td>0 RPM</td>
</tr>
<tr>
<td>300, 11</td>
<td>Time</td>
<td>20 tenthsec</td>
</tr>
</tbody>
</table>
APPENDIX E

Title Suprem-3 SiGe implanted channels P+ S/D region
com simulated by Luigi Ternullo Jr.
com Thesis work 9/23/92 (revision)
Initialize silicon <100> resistiv boron=8 thickness=2.0 dx=0.02
diffusion time=15 temperature=800 weto2 T.rate=20
diffusion time=50 temperature=1100 weto2
diffusion time=30 temperature=1100 weto2 T.rate=-10

Com Setting the grain size to 1.0 microns since Suprem can not simulate
Com low temperature grain growth.
deposit polysilicon temperat=610 grain.si=1.0 thickness=0.195

com Using loop to find optimum ox time for
Comm 1000 A oxide
COM $ Loop steps=50 optimize
$ assign name=tm n.value=20 lower=5 upper=30 optimize

  diffusion time=16 temperature=900 T.final=1100 F.O2=0.5 F.N2=4.5
diffusion time=6 temperature=1100 F.O2=4.0
diffusion time=3 temperature=1100 F.O2=4.0 HCL%=4.7
diffusion time=3 temperature=1100 F.O2=4.0
$  Argon used in place of N2 for Ramp down
diffusion time=34 temperature=1100 T.final=900 F.N2=4.5
$ extract name=xox thickness layer=4 target=.075
COM assign name=xox1 n.value=@xox target=1000
$ l.end

deposit polysilicon temperat=610 pressure=3.5e-4 thickness=0.5
diffusion time=20 temperature=900 ss.phosp
Com Etching gate polysilicon for S/D region
Etch polysili

print layers
implant boron dose=1E15 energy=35
Extract name=xox1 thickness layer=2
Extract name=xox2 thickness layer=4
Extract name=poly1 thickness layer=3
plot net active Title="B Implant before oxide S/D Region"
+ bottom=1e13 top=1e20 device="regis" plot.out="sdbimp.plt"
plot active phosphorous line=2 color=2 ADD
plot chemical boron line=3 color=3 ADD
label label="Gate Oxide in S/D=@xox2"um" x=1.0 y=1e19
label label="Poly Substrate Thickness=@poly1"um"
label label="Thick Isolation Oxide=@xox1"um"
label label=""
Com Oxide growth and S/D anneal at the same time
$ Loop steps=50 optimize
$ assign name=tm n.value=20 lower=5 upper=50 optimize
$ diffusion time=10 temperature=800 t.final=900 F.O2=0.5 F.N2=4.5
$ diffusion time=35 temperature=900 F.O2=5.0
$ diffusion time=20 temperature=900 t.final=850 F.O2=5.0
$ electrical steps=1
$ end.electrical
$ Extract h.resist layer=3 name=rs target=140
$ extract name=xox thickness layer=6 target=.04
COM assign name=xox1 n.value=@xox target=1000
$ l.end
electrical steps=1
bias layer=3
end.electrical
Extract h.resist layer=3 name=rsbd1
Extract name=xox1 thickness layer=2
Extract name=xox3 thickness layer=4
Extract name=poly1 thickness layer=3
print layers active phosphorous boron concentr x.max=1.0
print net active concentr x.max=1.0
plot net active Title="B Concen, S/D Region"
+ bottom=1e13 top=1e20 device="regis" plot.out="sdbcon.plt"
plot active phosphorous line=2 color=2 ADD
plot active boron line=3 color=3 ADD
label label="Gate Oxide Thick. Aft. Drive=@xox3"um" x=1.0 y=1e19
label label="Poly Substrate Thickness=@poly1"um"
label label="B S/D Sheet Res.=@rsbd1"ohm/sqr."
label label="Thick Isolation Oxide=@xox1"um"
label label=""
deposition oxide thickness=0.2 dx=0.02
$ Argon used in place of N2
diffusion time=10 temperature=900 F.O2=5.0
electrical steps=1
bias layer=3
end.electrical
Extract h.resist layer=3 name=rsbd2
Extract name=xox1 thickness layer=2
Extract name=xox4 thickness layer=4
Extract name=poly1 thickness layer=3
print layers active phosphorous boron concentr x.max=1.0
print net active concentr x.max=1.0
plot net active Title="Final Boron Concentration in PMOS S/D"
+ bottom=1e13 top=1e20 device="l/postscript" plot.out="sdblto.plt"
plot active phosphorous line=2 color=2 ADD
plot active boron line=3 color=3 ADD
label label="Gate + Passivation Oxide Thick."@xox4"um" x=1.0 y=1e19
label label="Poly Substrate Thickness=@@poly1"um"
label label="B S/D Sheet Res.="@rsbd2"ohm/sqr."
label label="Thick Isolation Oxide=@xox1"um"
label label=""
label label=""
label label="Boron Concentration Profile"
Stop
$ TMA TSUPREM4 CMOS TFT enhancement transistor simulation
COMMENT DATE 9/23/92
COMMENT FILENAME LATDIFFP.IN
COMMENT FILES CREATED LATDIFFP.STR - SUPREM IV structure file
COMMENT FILES USED NONE
COMMENT CREATED BY LUIGI TERNULLO JR.
COMMENT PURPOSE PMOS device of CMOS TFT
COMMENT
$
$ MASK LEVELS xxxx - opaque ---- clear
$
$ x axis - um 0---1---2---3---4
$
$ POY 1 xxxxxxxxxxxxxxxxxxx (WELL - MESA)
$
$ POLY 2 gate -----------xxxxx
$ P+ S/D --------------- (P select)
$
$ Contact xxxx-----xxxxxxx
$ metal1 --xxxxxxx------
$ passivation not simulated
$
$ Define the grid
$
$ Note: The following "DEFINE" statement sets the grid density for the simulation. A larger value of "GDENS" gives a denser grid. A value of 1 is used for setting up the simulation; 2 is used for most of the simulation work, while values of 3 or greater are used to get the final answers.

DEFINE GDENS 1
$
$ Specify the horizontal grid spacings at various x values
LINE X LOCATION=0.0 SPACING=(0.2/ GDENS )
LINE X LOCATION=3.0 SPACING=(0.2/ GDENS )
LINE X LOCATION=4.0 SPACING=(0.5/ GDENS )
$ LINE X LOCATION=6.0 SPACING=(0.5/ GDENS )
$ LINE X LOCATION=11.0 SPACING=(0.2/ GDENS )
$ LINE X LOCATION=14.0 SPACING=(0.2/ GDENS )
$
$ Specify the vertical grid spacings at various y values

F-1
Tailor the grid to the device being simulated

Eliminate horizontal grid lines below the active device

Initialize the structure


Initialize <100> BORON=1E15

OPTION DEVICE=REGIS

$ ISOLATION OXIDE
METHOD COMPRESS
DIFFUSION TIME=15 TEMP=800 T.final=1100 F.H2O=4.0
DIFFUSION TIME=75 TEMP=1100 F.H2O=4.0
DIFFUSION TIME=30 TEMP=1100 T.final=875 F.H2O=4.0

$ ENLARGED GRAIN POLY (temp at 625. to low for suprem 4 to simulate.
$ & GATE OXIDE
DEPOSIT POLYSILI THICKNESS=0.195 SPACES=GDENS
DIFFUSION TIME=15 TEMP=900 T.FINAL=1100 F.O2=0.5 F.N2=4.5
DIFFUSION TIME=4 TEMP=1100 F.O2=5.0
DIFFUSION TIME=4 TEMP=1100 F.O2=5.0 HCL=4.7
DIFFUSION TIME=4 TEMP=1100 F.O2=5.0
DIFFUSION TIME=35 TEMP=1100 T.FINAL=900 F.N2=4.0

SELECT Z=BORON-8E13
PRINT.1D LAYERS X.VALUE=2.0

NOT SIMULATING SPIN ON DOPING.  ASSUMING DOPING IS INSITU.

ACTUAL SPIN ON DOPING WILL BE PERFORMED AT 900C FOR 20 MIN.

DEPOSIT POLYSILI PHOSPHOR=1E20 THICKNESS=0.5 SPACES=GDENS
ETCH POLYSILI LEFT P1.X=3.0

SELECT Z=BORON-8E13
PRINT.1D LAYERS X.VALUE=3.5
PRINT.1D LAYERS X.VALUE=2.0
SELECT Z=LOG10(PHOSPHOR) TITLE="GATE REGION AFTER PREDEP. AND OXIDE"
OPTION PLOT.OUT=GPREDEP.PLT
PLOT.1D X.V=3.5 Y.MIN=15 Y.MAX=20 LINE.TYP=2

IMPLEMENT BORON DOSE=1.0E15 ENERGY=30
SELECT Z=LOG10(BORON) TITLE="CONCEN. PROFILE P+TFT S/D REGION"
OPTION PLOT.OUT=BIMP.PLT
PLOT.1D X.V=2.0 Y.MIN=15 Y.MAX=20 LINE.TYP=2

DIFFUSION TIME=35 TEMP=900 F.O2=5.0
DEPOSIT OXIDE THICKNESS=0.2 SPACES=GDENS
DIFFUSION TIME=10 TEMP=900 F.O2=5.0

SELECT Z=BORON-8E13
PRINT.1D LAYERS X.VALUE=2.0
PRINT.1D LAYERS X.VALUE=3.5
SELECT Z=LOG10(BORON) TITLE="CONCEN. PROFILE P+TFT S/D REGION"
OPTION PLOT.OUT=BCON.PLT
PLOT.1D X.V=2.0 Y.MIN=15 Y.MAX=20 LINE.TYP=2

SELECT Z=LOG10(PHOSPHOR) TITLE="CONCEN. PROFILE N+ POLY GATE W/P+
OPTION PLOT.OUT=GATEB.PLT
PLOT.1D X.V=3.5 Y.MIN=13 Y.MAX=20 LINE.TYP=2
SELECT Z=LOG10(BORON)
PLOT.1D X.V=3.5 LINE.TYP=1 ^AXIS ^CLEAR
SELECT Z=LOG10(DOPING)
PLOT.1D X.V=3.5 LINE.TYP=3 ^AXIS ^CLEAR
$
$ Plot the lateral diffusion profile
SELECT Z=LOG10(BORON) TITLE="CMOS TFT, PMOS LATERAL DIFFUSION"
OPTION DEVICE="PS-L"
PLOT.2D X.MIN=2.5 X.MAX=4.0 Y.MIN=-1.0 Y.MAX=1.0
FOREACH X (15 TO 20 STEP 1.0)
  CONTOUR VALUE=X LINE.TYP=2
END
$ Plot the con profiles in P+ S/D regions
SELECT Z=LOG10(BORON) TITLE="CMOS TFT, PMOS S/D DIFFUSION"
OPTION PLOT.OUT=PSD.PLT
PLOT.2D X.MIN=1.0 X.MAX=2.0 Y.MIN=-1.0 Y.MAX=1.0
FOREACH X (15 TO 20 STEP 1.0)
  CONTOUR VALUE=X LINE.TYP=2
END
PAUSE
$ This structure file can be used for SCN NMOS enh.
STRUCTURE OUTFILE=LATDIFFP.STR
STOP

F-3
APPENDIX G

POLY VS. GE PMOS 2/25

ID (µA)

-40.00

4.000 /div

0.0000

VDS .5000/div ( V ) -5.000

Vgs = 7V

Vgs = 6V

Vgs = 5V

Vgs = 4V

Vgs = 3V

POLY VS. GE NMOS 2/25

ID (µA)

300.0

30.00 /div

0.0000

VDS .5000/div ( V ) 5.000

Vgs = 7V

Vgs = 6V

Vgs = 5V

Vgs = 4V

Vgs = 3V

G-1