5-22-2012

Exploring Si/SiGe quantum-well thin-film thermoelectric devices using TCAD simulation

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EXPLORING Si/SiGe QUANTUM-WELL THIN-FILM THERMOELECTRIC DEVICES USING TCAD SIMULATION

By

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A Thesis Submitted In Partial Fulfillment of the Requirements for the Degree of

Master of Science in Microelectronic Engineering

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ROCHESTER, NEW YORK

MAY 22, 2012

ABSTRACT

There is an increasing demand for energy as a result of industrial development and rapid growth in global population. To date, most energy supply comes from traditional sources like coal and gas, which are nonrenewable energy sources. The combustion of fossil fuels produces greenhouse gases and pollution, which deteriorates our ecosystem. Extensive attention and research has been given to the development of renewable energy sources, including solar, wind, tides, geothermal heat, hydroelectricity, thermoelectricity and *et al*.

Thermoelectric (TE) applications can be categorized mainly into power generation and cooling operation utilizing Seebeck and Peltier effects, respectively. The further development of TE devices is limited by the low TEG efficiency and the low cooling coefficient of performance due to the limitation of the material figure of merit (*ZT*). In the 1990s, the advent of low dimensional (quantum well and quantum wire) thermoelectric systems triggered the breakthrough of improved *ZT* via two basic mechanisms: 1) increased density of states near Fermi level, and 2) deceased thermal conductivity by increased phonon scattering at material boundaries [1], [2]. Despite theoretical and experimental success using low dimensional TE systems reported by different universities or laboratories, the efficiency and coefficient of performance of commercially available bulk thermoelectric devices remain at a mere 5%-10%.

The Silvaco Inc. device simulator (ATLAS) is used to explore the physics and evaluate the performance of quantum well TE devices on single crystalline silicon-on-glass (SiOG). Owing to the distinguish features of SiOG substrate, including lower

thermal conductivity, microfabrication compatibility, good template for QW layers epitaxially grown atop, Corning Incorporated are especially interested in Si/SiGe quantum well thermoelectrical devices for automobile waste heat recovery application.

In this thesis, model adjustments were implemented to calibrate bulk Si & SiGe parameters, and capture the electrical and thermal effects from quantum-sized dimensions. Design parameters, which optimize the thermal power and *ZT* for *n*- and *p*-type Si/SiGe QW structures were established. The electrical and thermal parasitic effects from SOI and SiOG to QW layers were studied. Moreover, equivalent circuit model was developed which demonstrates the performance advantage of SiOG as a low-loss substrate.

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LIST OF SYMBOLS

η_{max} – the maximum efficiency of thermoelectric generator (TEG) under optimized load condition

T_{cold} – cold side temperature

T_{hot} – hot side temperature

ZT – figure of merit of a material

κ_e – electronic thermal conductivity

κ_l – lattice thermal conductivity

μ –electron mobility

m^* – effective mass

S_d – diffusive Seebeck coefficient component

S_{PD} – phonon drag Seebeck coefficient

S_{CS} – carrier scattering Seebeck coefficient

t_W – quantum well thickness

t_B – barrier thickness

t_{QW} – thickness of entire Si/SiGe film stacks

t_S – thickness of substrate

$\tilde{p}$ – effective hole concentration across the entire Si/SiGe QW film stacks

$\tilde{n}$ – effective electron concentration across the entire Si/SiGe QW film stacks

$\tilde{p}'$ – effective hole concentration inside the center quantum well layer

$\tilde{S}$ – effective Seebeck coefficient across the entire Si/SiGe QW film stacks

$\tilde{\sigma}$ – effective electrical conductivity across the entire Si/SiGe QW film stacks

R_{INT} – internal resistance of TEG consisting of *N*-pair alternating *n*-and *p*-type thermal elements on SiOG substrate in equivalent circuit model

S_T – total Seebeck coefficient of TEG consisting of *N*-pair alternating *n*-and *p*-type thermal elements on SiOG substrate in equivalent circuit model

V_{OCT} – total thermal voltage generated by TEG consisting of *N*-pair alternating *n*-and *p*-type thermal elements on SiOG substrate in equivalent circuit model

V_{OCP} – thermal voltage generated by one pair of *n*-and *p*-type thermal elements on SiOG substrate in equivalent circuit model

w–width of thermoelectric devices in equivalent circuit model

L– length of thermoelectric devices in equivalent circuit model

S_T' – total Seebeck coefficient of QW films stacks and underlying substrate in parallel conductor model

σ_T' – total electrical conductivity of QW films stacks and underlying substrate in parallel conductor model

ACKNOWLEDGMENTS

I would like to acknowledge all those who helped in some way to complete this study. First and foremost I would like to thank my advisor, Dr. Karl Hirschman, for all his support throughout this project. I would also like to thank my committee members, Dr. Robert Pearson and Dr. Robert Stevens for guidance and support. I especially acknowledge Corning Inc., particularly Dr. Greg Couillard. Without their support this project would not be possible. The opportunity given has greatly shaped me and my future career in research.

CHAPTER 1

INTRODUCTION

1.1 Motivation for TE Advancement

Thermoelectric application for energy harvesting is based on the Seebeck effect, where heat is converted directly into usable electricity. The Seebeck effect is widely utilized in two main applications: radioisotope thermoelectric generators (RTG) as power sources in remote space missions and automotive thermoelectric generators (ATEG) for engine waste heat recovery [3].

In general, TE devices possess high sustainability and longer lifetime offer solid-state cooling and heating and are environmental-friendly; however, the low efficiency in conventional TE bulk devices has inhibited further advancement of thermoelectric performance. The figure of merit (*ZT*), the indicator of thermoelectric performance, of bulk materials hovered around one at room temperature before the breakthrough of *ZT* utilizing quantum well structured TE in the early 1990s [4-5]. Since then, intensive research interest was aroused for experiments and modeling on low dimensional TE materials.

1.2 Potential Applications for Silicon-on Glass

Over the past several years, Corning Incorporated has collaborated with Rochester Institute of Technology on modeling, process development and characterization of a low temperature thin film transistor on SiOG substrate. Those research activities have led to great successful and promising outcomes [6-8].

Corning Incorporated invented SiOG substrate technology where single crystal silicon thin film is transferred from a bulk wafer onto a glass [8]. First, the Si wafer is implanted hydrogen ions followed by clean and prebonded of both Si wafer and glass. Next silicon wafer and glass are bonded by simultaneous applications of voltage and heat. During the bonding process, the silicon thin film exfoliates at a depth controlled by the energy of hydrogen ion implantation [8], which results in thin film silicon bonded onto glass, and the remaining bulk Si wafer. With expertise on the manufacture of SiOG for flat panel display application, Corning Incorporated is still seeking potential applications for SiOG and is especially interested in exploring thin-film quantum wells (QW) on SiOG for automobile waste heat recovery applications. The potential advantages of low-dimensional thermoelectricity are attributed to the realization that: 1) size quantization effects can increase Seebeck Coefficient while not degrading density of state (DOS) and as a result electrical conductivity [1]; 2) thermal conductivity decreases due to increased scattering at material boundaries. In contrast, bulk thermoelectric materials face the dilemma of the compromised relationship between Seebeck coefficient and electrical conductivity as well as high bulk thermal conductivity.

1.3 Goals and Objectives of Study

To better understand the physics of thermoelectric devices and to provide the direction for thin-film QW thermoelectric structures grown on SiOG (or SOI) substrates, the following objectives will be accomplished in this work:

- Simulate and optimize QW TE structures
  - Investigate strain effects on QW TE layers
  - Simulate various barrier/well thickness, barrier concentration and Si/Ge ratio
  - Investigate temperature dependent thermoelectric behavior
- Investigate both electrical and thermal parasitic effects that are substrate dependent (e.g. SOI or glass).
- Develop a RC distributed model for thermoelectric modules for interpretation of experimental TE measurements.

1.4 Arrangement of document

In Chapter 2, the physics behind thermoelectricity and the basic TE parameters will be introduced including Seebeck coefficient (S), power factor ($S^2\sigma$), efficiency (η) and figure of merit (ZT) of TEG. While analyzing each component of ZT, the advantages of low-dimensional TE materials as well as the dilemma of bulk counterpart will be revealed.

In Chapter 3, the methodology and physical models involved in ATLAS device simulator will be presented. Then Si/SiGe energy band structure with the strain effect taken into account will be discussed, followed by the description of simulation structure and parameter extraction strategies.

In chapter 4, Seebeck coefficients at room temperature were simulated on both bulk *n*- and *p*-type Si and SiGe alloy and simulation results will be compared to the experimental counterparts. Based on the comparison, input model parameters will be corrected and implemented on QW simulations at 300K using the methodology discussed in chapter 3. QW thermoelectric parameters (S, σ, $S^2\sigma$ and ZT) as a function of well thickness (t_W), barrier thickness (t_B), barrier doping concentration and Ge ratio will be simulated and parameters optimization was discussed based on the simulation results.

In Chapter 5, thermoelectric behaviors over the temperature range from 300 to 900K will be presented and discussed. In Chapter 6, the equivalent circuit of TEG was introduced followed by the discussion of system requirements from electrical and thermal aspects. Then, the electrical and thermal parasitic effects from SOI and SiOG substrate will be characterized using parallel conductor models. Chapter 7 contains summary and extension of this study.

CHAPTER 2

THEORY OF THERMOELECTRIC PHENOMENA

In Chapter 2, the basic principles of thermoelectrics will be introduced including Seebeck effect, efficiency (η) and figure of merit (*ZT*) of TEG. For waste heat recovery application, heat from vehicle engine and exhaust is used as heat source while the cooling source is usually the engine coolant and vehicle radiator. With about 350 °C temperature differential, TEG's efficiency greater than 10% is desired which requires *ZT* about 1.25 to increase mileage up to 10% [10]. However, when attempting to optimize *ZT* using conventional bulk materials, *ZT* hovers ~1. The inherit compromise of bulk material will be presented followed by the electronic transport of different dimensional thermoelectrics, from the comparison of which the advantages of using low-dimensional systems (2D-quantum well and1D-quantum wire) will be revealed.

2.1 SEEBECK EFFECT

The Seebeck effect was first discovered by the German physicist Thomas Johann Seebeck in 1821 and describes the thermoelectric phenomena that when a temperature difference is maintained between two dissimilar metals or semiconductors at open circuit condition, there will be a steady-state electrostatic potential difference between the high- and low- temperature region. The basic thermoelectric circuit is demonstrated in figure 1

where two different materials A and B, with Seebeck coefficient of S_a and S_b, are connected so that one junction is at temperature T_1 and the other junction is at temperature $T_2 \neq T_1$.

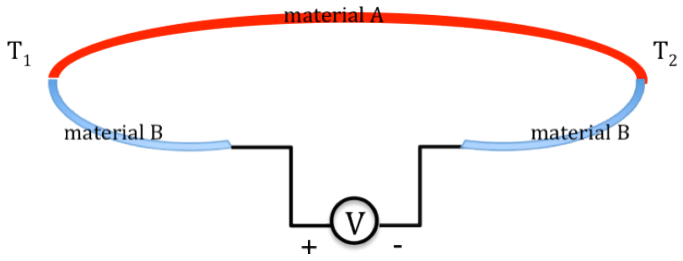

Figure 1. Basic thermoelectric circuit of Seebeck effect

The TE voltage can be derived from:

$$V = \int_{T_1}^{T_2} (S_a(T) - S_b(T))\, dT \tag{2.1}$$

In case of small temperature difference so that S_a, S_b can be treated as temperature independent, the measured TE voltage under open circuit condition can be approximated to [9]:

$$\Delta V = (S_a - S_b) \cdot (T_1 - T_2) = S_{ab} \Delta T \tag{2.2}$$

where the Seebeck coefficient S of the material is positive for p-type and negative for n-type semiconductors and (S_a - S_b) is the differential Seebeck coefficient between material A and B. Note that for a single material, the absolute value of S is relative to a superconductor for which S=0. The corresponding thermoelectric field is written as [9]:

$$\mathbf{E} = S_{ab} \cdot \nabla T \tag{2.3}$$

When a temperature difference is applied, charge carriers either holes in p-type or electrons in n-type semiconductor, migrate from the hot to cold side, leaving the

immobile ionic charge behind. The charge separation creates a Seebeck electromotive force (EMF) and will eventually cease when both thermal and electrical equilibrium are achieved. The configuration of typical *pn* Seebeck thermal couples were demonstrated in figure 2, where *n*- and *p*- type semiconductor thermal pellets were connected by conductors with one side fixed to heat source and the other side attached to heat sink and the open circuit voltage is the Seebeck voltage.

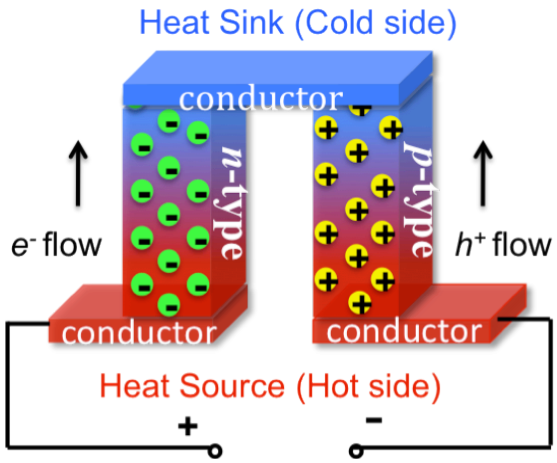

Figure 2. The configuration of typical *pn* Seebeck thermal couples where *n*- and *p*- type semiconductor thermal pellets were connected by conductors with one side fixed to heat source and the other side attached to heat sink and the open circuit voltage is the Seebeck voltage.

2.2 TEG EFFICIENCY

Utilizing Seebeck effects, TE elements can be configured into thermoelectric generators. For practical power generation applications, usually numerous alternative *p*- and *n*-type semiconductor pellets are connected electrically in series and thermally in parallel for the purpose of obtaining high voltage output and large heat flow as illustrated in figure 3 [10]. High thermal but low electrical conductivity ceramic materials are used

as encapsulation of TEG to improve the heat sink efficiency and relieve mechanical stress.

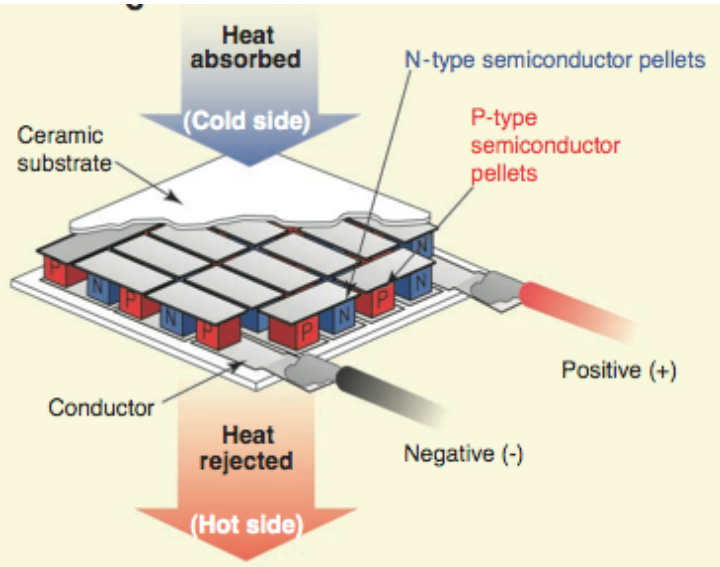

Figure 3. The configuration of thermoelectric generators where a large number of alternative *p*- and *n*-type semiconductor pellets are connected electrically in series and thermally in parallel for the purpose of obtaining high voltage output and large heat flow [10].

TEG efficiency is used to characterize and evaluate the performance of power generation devices, and is defined as the ratio of power provided to the external load over the heat energy absorbed at the hot junction. Under optimized load conditions, the maximum efficiency can be expressed as [1]:

$$\eta_{\max} = \frac{\Delta T}{T_{\text{hot}}} \frac{\sqrt{1+ZT}-1}{\sqrt{1+ZT}+\frac{T_{\text{cold}}}{T_{\text{hot}}}} \tag{2.5}$$

where T_{hot}, T_{cold}, ΔT and ZT are the temperature of hot and cold side, temperature differences between these two sides and material figure of merit which will be discussed more in section 2.3. Figure 4 plots TEG efficiency versus temperature differences at various values of ZT with T_C fixed at 300K. Larger temperature difference gives rise to higher device efficiency. For a given temperature difference, the larger ZT the higher the efficiency. As ZT goes to infinity, efficiency approaches to the ideal Carnot efficiency limit. For vehicle waste heat recovery applications, the temperature differential is usually about 350°C; therefore, improved efficiency can be realized by increased ZT.

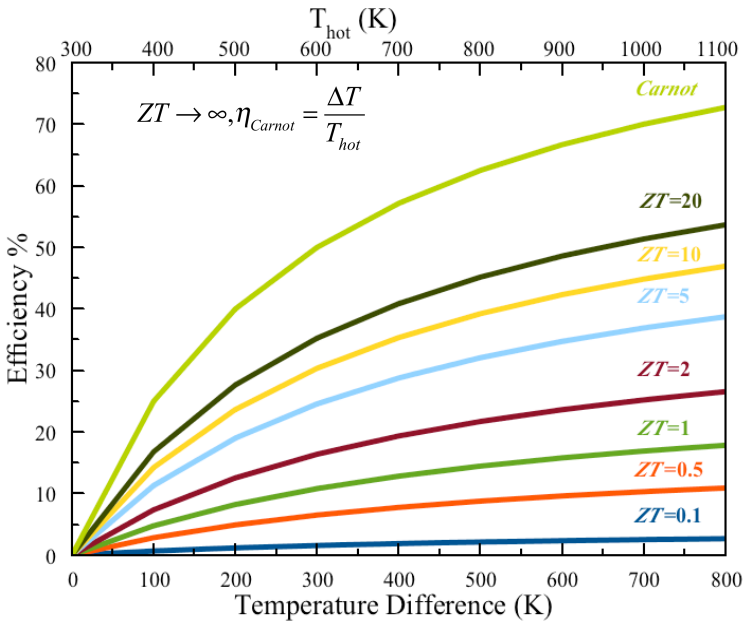

Figure 4. Calculated TEG efficiency versus temperature differences at various ZT values

The maximum TEG efficiency of commercial available TEG is only around 5-10% [10], limited by ZT of the material. Consequently, ZT greater than 1.25 is demanded in order to achieve high efficiency and better device performance.

2.3 FIGURE OF MERIT (*ZT*)

The efficiency of power generation and performance of thermoelectric cooling depend on the dimensionless thermoelectric figure of merit (*ZT*) which is described as:

$$ZT = \frac{S^2\sigma}{\kappa}T \tag{2.6}$$

where S is Seebeck coefficient or thermal power, σ is electric conductivity, κ is thermal conductivity and T is the absolute average temperature. It is obviously observed from equation (2.6) that large S and σ along with small κ give rise to high ZT.

Figure 5 demonstrates the material compromise when attempting to optimize the carrier concentration for the maximum ZT in bulk materials. As the carrier concentration increases, both electrical conductivity and electronic thermal conductivity increase since there are more carriers to transport electron charges and heat energy; whereas Seebeck coefficient decreases because as the materials become too electrically and thermally conductive, less temperature gradient can be maintained to create potential difference. Usually, the maximum ZT of bulk material is achieved in the range of 10^{19} to 10^{20} cm^{-3} doping level. Currently, bulk materials with the highest ZT are Bi_2Te_3 alloy with ZT≈1 at 300K [11].

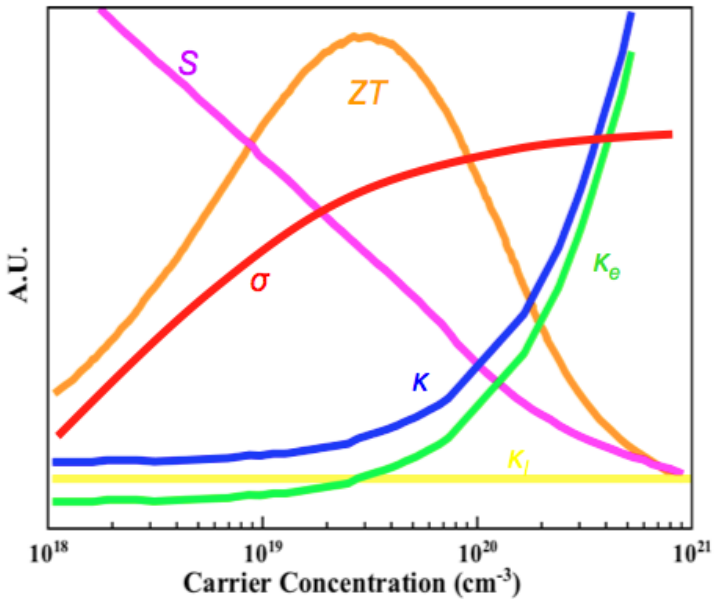

Figure 5. Thermal and electrical parameters as functions of carrier concentration in bulk materials

2.3.1 Electrical Conductivity (σ)

For semiconductors with both electron and holes as carries, the electrical conductivity is given as:

$$\sigma = nq\mu_n + pq\mu_p \tag{2.7}$$

where n, p, μ_n, μ_p and q are electron and hole concentration, electron and hole mobility and electron charge respectively. If $n>>p$ or $p>>n$, σ can be approximate as $nq\mu_n$ or $pq\mu_p$.

Mobility is determined by carrier effective mass and scattering mechanisms and can be expressed using the simple case as [12]:

$$\mu = \frac{q\tau}{m^*} = \frac{q\lambda_e}{m^* v} \tag{2.8}$$

where m^*, τ, λ_e and υ are the effective mass, carrier mean free time, mean free path and group velocity taking different scattering processes into account. As n increases, even though μ decreases as τ and λ_m decrease, the σ increases since the influence of n

dominates over μ in equation (2.7). Also smaller m^* gives rise to larger μ. Based on equation (2.7) and (2.8), material of high carrier concentration and small effective mass materials results in larger σ.

2.3.2 THERMAL CONDUCTIVITY (κ)

Thermal conduction is carried out by both charge carriers and phonon vibrations. Thermal conductivity includes contributions from both electronic thermal conductivity (κ_e) and lattice thermal conductivity (κ_l) [1, 2, 13]:

$$\kappa = \kappa_e + \kappa_l \tag{2.9}$$

Electronic thermal conductivity (κ_e) originates from heat transfer by electrons and holes and is related to electrical conductivity (σ) through the Wiedemann-Franz law [1, 2, 13]:

$$\kappa_e = L_0 \sigma T = L_0 ne\mu T \tag{2.10}$$

where the Lorenz number L_0 is 2.4×10^{-8} ($J^2\ K^{-2}C^{-2}$) for free electrons in vacuum and in solids where electrons undergo only elastic collisions. An increase in carrier concentration results in an increase of electrical conductivity as well as electronic thermal conductivity.

On the other hand, lattice thermal conductivity (κ_l) stems from phonon transferring heat and can be expressed as the product of the specific heat C_p, the phonon velocity υ_ϕ and the phonon mean free path λ_ϕ [1, 2, 13]:

$$\kappa_l = \frac{1}{2} C_p \upsilon_\phi \lambda_\phi \tag{2.11}$$

Equation (2.11) is quite complicated to solve since it needs to calculate a spectrum of phonon with a large variety of frequency and mean free path as well as different scattering mechanisms [13]. As the carrier concentration increases, κ_e will exceed κ_l and become dominating component of κ.

2.3.3 SEEBECK COEFFICIENT (*S*)

For metals and degenerate semiconductors, the relationship between Seebeck coefficient and carrier concentration can be described by simple electron transport model (parabolic band, energy-independent scattering approximation) as [13]:

$$S = \frac{2k_B^2}{3q\hbar^2} m^* T \left(\frac{\pi}{3n}\right)^{2/3} \tag{2.12}$$

where k_B is Boltzmann constant and $\hbar$ is the reduced Plank constant. For material with certain m^*, S is inversely proportional to n.

2.3.4 DESIGN TRADEOFF OF *ZT* IN BULK THERMOELECTRICS

The dilemma of increasing *ZT* results from the fact that an increase of Seebeck coefficient leads to simultaneous decrease of electrical conductivity (σ) and an increase in electrical conductivity (σ) causes an increase in electronic thermal conductivity (κ_e). Thus one cannot obtain maximized *ZT* from increased *S*, σ and decreased κ_e simultaneously by simply tuning the carrier concentration.

Another inherent material conflict stems from effective mass (m^*) since large *S* requires materials to have large m^*, which nevertheless yields to low mobility and therefore small electrical conductivity (σ). Therefore, there is a compromise between large effective mass and high mobility.

The significant enhancement of ZT is realized by the introduction of low-dimensional TE with the benefit of two basic mechanisms [1-2]: (1) an increase in power factor ($S^2\sigma$) owing to increased density of states (DOS) in low-dimensional systems; (2) a reduction of lattice thermal conductivity due to increased phonon scattering at the material boundaries.

2.4 Electronic Transport For Thermoelectrics

2.4.1 Electron Dispersion Relation

For 3D bulk material, carriers are free to move in all directions. Assuming parabolic dispersion relationship between electron energy and its momentum, thus we have [1-2]:

$$E_{3D}(k) = \frac{\hbar^2 k_x^2}{2m_x^*} + \frac{\hbar^2 k_y^2}{2m_y^*} + \frac{\hbar^2 k_z^2}{2m_z^*} \tag{2.13}$$

where m_x^*, m_y^*, m_z^* and k_x, k_y, k_z are the carrier effective mass and wave vectors in x, y and z directions. The wavevector k is inversely proportional to the electron wavelength. $E_{3D}(k)$ describes a series of equal-energy ellipsoid surfaces labeled as $\Sigma(E)$ in (k_x, k_y, k_z) space.

Consider 2D quantum wells (QW) with thickness or well width d, same magnitude of electron wavelength, carriers are free to move in two dimensions (xy plane) but confined in z direction. Carrier confinement in wells is realized by adjacent barrier layers, which have sufficient energy offset to confine carriers in the lower energy states. In the confinement direction, the 3D continuum energy levels are quantized into discrete subbands E_i, where i (=1,2,3…) is the quantum number or subband index. Assuming infinite potential barrier, 2D energy dispersion relation can be defined as [1-2]:

$$E_{2D,i}(k) = \frac{\hbar^2 k_x^2}{2m_x^*} + \frac{\hbar^2 k_y^2}{2m_y^*} + \frac{\hbar^2 \pi^2 i^2}{2m_z d^2}, \quad i = 1,2,3... \tag{2.14}$$

The corresponding equal energy surfaces $\Sigma(E)$ are ellipse in (k_x, k_y) momentum space.

Likewise, in 1D quantum wires with wire diameter of d, carriers are free to move only in one dimension (x direction) and confined in y and z directions. The 1D energy dispersion relation is given as:

$$E_{1D,i,j}(k) = \frac{\hbar^2 k_x^2}{2m_x^*} + \frac{\hbar^2 \pi^2 i^2}{2m_y^* d^2} + \frac{\hbar^2 \pi^2 j^2}{2m_z^* d^2}, \; i, j = 1,2,3... \tag{2.15}$$

The corresponding equal-energy surfaces $\Sigma(E)$ are tubes along the k_x direction.

2.4.2 DENSITY OF STATES (DOS)

DOS, the number of states available states per unit volume of energy at each energy level, is derived rigorously as [1]:

$$g(E) = \int_{\Sigma(E)} \frac{d\Sigma}{4\pi^3} \frac{1}{|\nabla E(k)|} \tag{2.16}$$

where $\Sigma(E)$ is the equal-energetic surfaces and $\nabla E(\boldsymbol{k})$ is the gradient of energy with respect to k. Substituting dispersion relationships of different dimensional systems, equations (2.13–2.15), into equation (2.26), DOS of different dimensions are given as:

$$g_{3D}(E) = \frac{\sqrt{m_x^* m_y^* m_z^*}}{\hbar^3 \pi^2} \sqrt{2E}, \quad E \geq 0 \tag{2.17}$$

$$\begin{aligned} g_{2D,i}(E) &= \sum_i g_i(E), \\ g_i(E) &= \frac{\sqrt{m_x^* m_y^*}}{\pi\hbar^2} \frac{1}{d}, \text{ if } E > E_i \\ g_i(E) &= 0, \quad \text{if } E \leq E_i \end{aligned} \tag{2.18}$$

$$g_{1D,i,j}(E)=\sum_{i,j} g_{i,j}(E),$$

$$g_i(E)=\frac{\sqrt{m_x^*}}{\pi\hbar}\frac{1}{d^2}\frac{1}{\sqrt{E-E_{ij}}},\quad \text{if } E>E_{ij} \tag{2.19}$$

$$g_i(E)=0,\quad \text{if } E\le E_i$$

It can be seen from equation (2.14) and (2.18) that for 2D quantum well, as the well thickness decreases, the spacing among subbands enlarges and correspondingly the magnitude of DOS at each subband increases. Similarly, for 1D quantum dot, the smaller the dot diameter, the more quantization of energy subbands and the better carrier confinement will be.

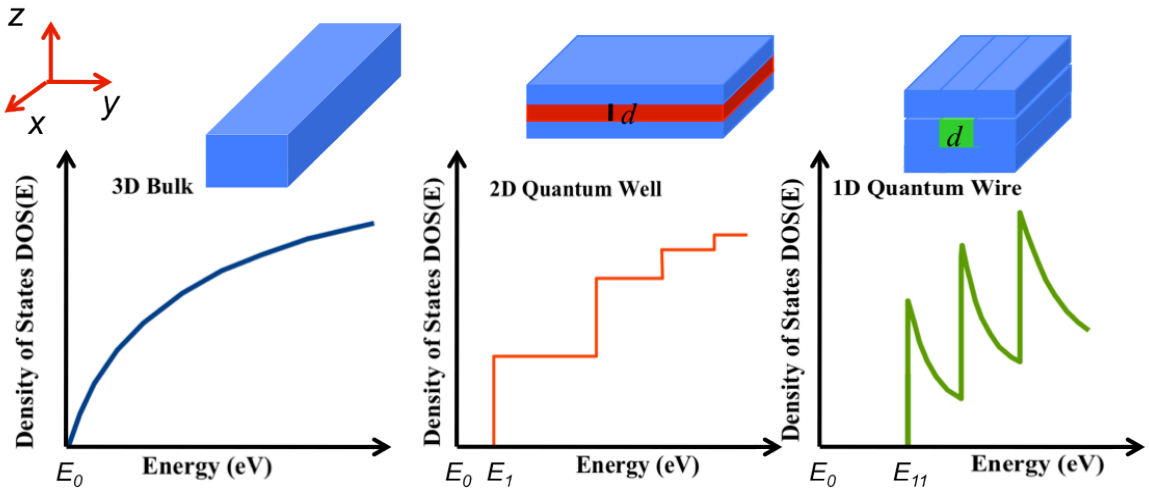

Figure 6. Density of States (DOS) as a function of energy for different dimensional systems where due to quantum confinement, the 3D continuum energy levels are quantized into discrete subbands and the ground state energy level of different low dimensional systems moves up to their first subband

DOS as a function of electron energy for different dimensions is illustrated in figure 6. For low dimensional systems, due to quantum confinement, the 3D continuum energy levels are quantized into discrete subbands. Also the ground state energy level of different

low dimensional systems moves up to their first subband ($\frac{\hbar^2\pi^2}{2m_z^*d^2}$ and $\frac{\hbar^2\pi^2}{2m_y^*d^2}+\frac{\hbar^2\pi^2}{2m_z^*d^2}$ for quantum well and quantum wire respectively) relative to the same band in 3D bulk material. In fact, the upward (or downward) shift of first subband in conduction (or valence) band equivalents to an effective bandgap broadening in low dimensional structures.

2.4.2 MOTT RELATION FOR SEEBECK COEFFICIENT

The distribution of electrons in semiconductor obeys Fermi-Dirac statistics. Occupancy factor $f(E)$ is the probability that a energy state is occupied by an electron and (1- $f(E)$) is the probability that hole reside at a energy state, in other word, unoccupied by an electron. The Fermi-Dirac distribution function is given as:

$$f(E)=\frac{1}{1+\exp\left(\frac{E-E_F}{k_BT}\right)} \tag{2.20}$$

The total number of electrons is calculated by the conduction band density of states $g_C(E)$ multiplied by $f(E)$, integrated from conduction band edge to infinite, and likewise the number of holes is given by the valence band density of states $g_v(E)$ multiplied by (1- $f(E)$), integrated from infinite to valence band edge:

$$n=\int_{E_c}^{\infty} g_c(E)f(E)dE \tag{2.21}$$

$$p=\int_{\infty}^{E_v} g_v(E)(1-f(E))dE \tag{2.22}$$

Similarly, energy dependent electrical conductivity $\sigma(E)$ can be associated to electrons that fill the energy levels between E and E+dE. The total electrical conductivity

σ can be calculated using the integral of $\sigma(E)$ over the entire energy range, moderated by the Fermi distribution function, as expressed [1]:

$$\sigma = \int_0^\infty \sigma(E)\left(-\frac{\partial f(E)}{\partial E}\right)dE \tag{2.23}$$

Culter and Mott [1] derived the Seebeck coefficient that is expressed only using DOS and Fermi distribution irrespective of the dominant transport mechanism. The differential form of Mott relation is expressed as:

$$S = \frac{k_B}{q}\frac{1}{\sigma}\int_0^\infty \sigma\left(E\right)\left(\frac{E-E_F}{k_BT}\right)\left(\frac{\partial f\left(E\right)}{\partial E}\right)dE \tag{2.24}$$

For metal and degenerately doped semiconductors, equation (2.24) can be simplified as the better-known Mott relation [1]:

$$S = \frac{\pi^2}{3}\frac{k_B}{q}k_BT\left(\frac{d\left\{\ln\left[\sigma\left(E\right)\right]\right\}}{dE}\right)_{E=E_F} \tag{2.25}$$

According to Mott relation, for degenerate semiconductor, the Seebeck Coefficient is proportional to energy derivative of conductivity or in other words the DOS near the Fermi level. The sharp features of density of states in low dimensional systems (as shown in figure 6) is the hallmark of increased Seebeck coefficient for a given carrier concentration and electrical conductivity.

In this chapter, the definition of Seebeck effect, the applications of Seebeck effect for power generation and the evaluation of device performance were presented. The difficulties of increasing *ZT* when attempting to optimize carrier concentration for a bulk material due to inherit material tradeoff were described followed by the introductions of low-dimensional TE materials, which has been demonstrated theoretically and experimentally to enhance *ZT* significantly [1-2]. Electronic transports for different-

dimensional materials were discussed next aimed at better explaining the origins of improved *ZT* from increased density of states (DOS) in low-dimensional systems.

CHAPTER 3

TCAD SIMULATOR AND SIMULATION STRUCTURES

In this chapter, the methodology involved in Silvaco ATLAS device simulator [15] will be presented followed by the explanation of how ATLAS takes Seebeck effect and quantum mechanisms into consideration. Then Si/SiGe energy band structure with the strain effect taken into account will be discussed, followed by the description of simulation structure and parameter extraction strategies.

3.1 PHYSICAL MODELS IN ATLAS

In this work, 2D ATLAS device simulation was implemented, which is based on solving a set of coupled mathematical equations derived from device physics. The basic equations can be categorized into: (1) Poisson's equation, (2) current continuity equations and (3) current density equations [15].

Poisson's equation links variations of electrostatic potential to local charge densities taking account contributions from all mobile and fixed charges including electrons, holes and ionized impurities.

$$\nabla^2\psi = -\nabla E = -\frac{\rho}{\varepsilon} = \frac{q\left(n - p + N_A - N_D\right)}{\varepsilon} \tag{3.1}$$

The charge continuity describes the way that the electron and hole densities evolve as a result of carrier generation recombination processes and the net current flow in and out of the region of interest.

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \mathbf{J}_p + G_p - R_p \tag{3.2}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \mathbf{J}_n + G_n - R_n \tag{3.3}$$

where G and R are generation and recommbination rate, and the subscript n and p denote the electron and hole components, respectively.

The current density **J** in the continuity equations can be approximated by drift and diffusion model. When temperature gradient exists, the current densities are modified to account for spactially varying lattice temperature:

$$\mathbf{J}_n = qD_n\nabla n - qn\mu_n\left(\nabla\psi + S_n\nabla T\right) - \mu_n n\left(k_B T\nabla\left(\ln n_{ie}\right)\right) \tag{3.4}$$

$$\mathbf{J}_p = qD_p\nabla p - qp\mu_p\left(\nabla\psi + S_p\nabla T\right) - \mu_p p\left(k_B T\nabla\left(\ln n_{ie}\right)\right) \tag{3.5}$$

where S_n and S_p are the Seebeck coefficient of electrons and holes.

When temperature gradient exists, additional heat transport equation is solved taking into account the effects of Joule heating, heating and cooling from both generation and recombination and Peltier and Thomson effects [15]. In ATLAS, The heat flow equation is given as:

$$\rho C_p\frac{\partial T_L}{\partial t} = \nabla\left(\kappa\nabla T_L\right) + H \tag{3.6}$$

where ρ, C_p, κ and H are the density of the material, specific heat capacitance, thermal conductivity and heat generation term. The heat generation term consists of: (1) Joule heating term, (2) generation and recombination heating and cooling term, and (3) Peltier and Thomson term.

Regarding quantum well TE simulation, a self-consistent coupled Schrodinger Poisson Model was implemented. This model self-consistently solves Poisson's equation for potential, and Schrodinger's equation for bound state energies and carrier wavefunctions. The solution of Schrodinger's equation provides quantized description of DOS in the presence of quantum confining potential variations. In 2D simulation, both electrical and heat current is parallel to QW layers and, quantum confinement is along the *y* direction. The 1D Schrodinger's equation at each slice along y direction for each electron valley (or hole band) *v* is given as follows:

$$-\frac{\hbar^2}{2}\frac{\partial}{\partial y}\left(\frac{1}{m_y^v(x,y)}\frac{\partial \psi_{iv}}{\partial y}\right)+E_C(x,y)\psi_{iv}=E_{iv}\psi_{iv} \tag{3.7}$$

$$-\frac{\hbar^2}{2}\frac{\partial}{\partial y}\left(\frac{1}{m_y^v(x,y)}\frac{\partial \psi_{iv}}{\partial y}\right)-E_V(x,y)\psi_{iv}=E_{iv}\psi_{iv} \tag{3.8}$$

where $m_y^v(x,y)$ is a spatially dependent effective mass in *y* direction for the *v*-th valley and $E_C(x,y)$ and $E_V(x,y)$ are conduction and valence band edge.

Once the eigen energies and wavefuntions are calculated, the electron concentration for 1D confinement, under Fermi statistics, is expressed as:

$$n(x,y)=\frac{2k_BT}{\pi\hbar^2}\sum\sqrt{m_x^v(x,y)m_z^v(x,y)}\sum_{i=0}^{\infty}\left|\psi_{iv}(x,y)\right|^2\ln\left[1+\exp\left(-\frac{E_{iv}-E_F}{k_BT}\right)\right] \tag{3.9}$$

The carrier concentration is then substituted into the charge part of Poisson's equation. The potential derived from the solution of Poisson's equation is substituted back into the Schrodinger's equation. This solution process (alternating between Schrodinger's and Poisson's equations) continues until convergence and a self-consistent solution of Schrodinger and Poisson's equation is reached.

3.2 SIMULATION OF SEEBECK EFFECT

The Seebeck coefficient for electrons and holes at temperature (T) is analytically modeled in ATLAS as follows:

$$S_n(T) = -\frac{k_B}{q}\left(\frac{5}{2} + \ln\frac{N_C}{n} + r + S_{PD}\right) \tag{3.10}$$

$$S_p(T) = \frac{k_B}{q}\left(\frac{5}{2} + \ln\frac{N_V}{n} + r + S_{PD}\right) \tag{3.11}$$

where the Seebeck Coefficient be considered as having three components:

(1) The diffusive component (S_d) which results from Fermi potential variation with respect to temperature. Under Maxwell-Boltzmann statistics approximation, S_d for electrons (S_{dn}) and holes (S_{dp}) are given as:

$$S_{dn} = -\frac{k_B}{q}\left(\frac{3}{2} + \ln\frac{N_C}{n}\right) \approx -\frac{k_B}{q}\left(\frac{3}{2} + \frac{E_C - E_F}{k_B T_L}\right) \tag{3.12}$$

$$S_{dp} = \frac{k_B}{q}\left(\frac{3}{2} + \ln\frac{N_V}{n}\right) \approx \frac{k_B}{q}\left(\frac{3}{2} + \frac{E_F - E_V}{k_B T_L}\right) \tag{3.13}$$

(2) The phonon drag contribution (S_{PD}) which is due to the momentum transfer from phonon to carriers systems by electron-phonon scattering, and is only significant in

lightly doped material and at low temperature. In ATLAS, the default model of S_{PD} for both electrons and holes is express as:

$$S_{PD} = 0.2 \times \left(\frac{k_B}{q} \right) \left(\frac{T_L}{300} \right)^{-2.5} \tag{3.14}$$

(3) The carrier scattering component (S_{CS}):

$$S_{CS} = -\frac{k_B}{q}(1+r) \tag{3.15}$$

where r is the scattering exponent in the power law relationship between relaxation time (τ) and carrier energy (E):

$$\tau(E) = \tau_0 E^{r-\frac{1}{2}} \tag{3.16}$$

where τ_0 is scattering constant depends both material properties and scattering mechanisms. Scattering exponent r is approximated for different scattering processes as: (1) for scattering of electrons on ionized impurities, $r = 2$; (2) for scattering of electrons on neutral impurities, $r = 1/2$; (3) for scattering of electrons on acoustic phonons, $r = 0$. Due to the inherit complexity and uncertainty of scattering exponent, the default value of -1 was used for both Si and SiGe thermopower simulation, which can be thought as eliminating the carrier scattering contribution to the Seebeck coefficient.

When temperature gradient exists across TE material, Seebeck coefficient varies along the material because it is temperature dependent. Under open circuit condition, the TE voltage generated between two contacts at different temperatures (T_1 and $T_2 > T_1$) is calculated by integrating the Seebeck coefficient as function of temperature from T_1 to T_2.

$$\Delta V = -\int_{T_1}^{T_2} \frac{\mu_n n S_n(T) + \mu_p p S_p(T)}{\mu_n n + \mu_p p} dT \tag{3.17}$$

The apparent Seebeck coefficient of the device is obtained using the open-circuit TE voltage (ΔV) divided by the temperature difference ($T_2 - T_1$).

3.3 SIMULATION STRATEGY

3.3.1 SILICON/ SILICON GERMANIUM ENERGY BAND STRUCTURE

Modulation doped $Si/Si_{1-x}Ge_x$ quantum well thermoelectric structures were investigated in this work using Silvaco ATLAS device simulation. When Si and $Si_{1-x}Ge_x$ are brought together into contact, because of wider bandgap (E_g) and larger electron affinity (χ) of Si compared to $Si_{1-x}Ge_x$ ($x<0.85$), their band offset belongs to staggered alignment (Type II) without strain effect [16]. At 300K, the basic energy band diagrams of $Si/Si_{0.8}Ge_{0.2}$ heterojunction before contact as well as *n*-type $Si_{0.8}Ge_{0.2}/Si/Si_{0.8}Ge_{0.2}$ heterojunction after contact and *p*-type $Si/Si_{0.8}Ge_{0.2}/Si$ heterojunction after contact were sketched in Figure 7 (a), (b) and (c), respectively, where the dash lines represent Fermi level controlled by doping concentration.

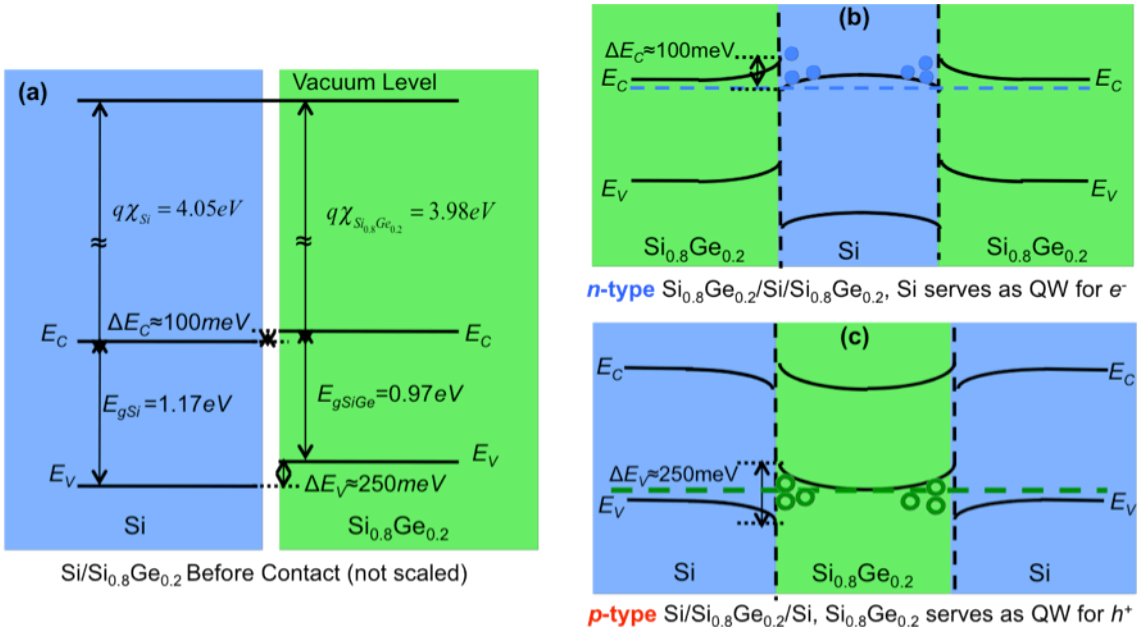

Figure 7. Energy band diagrams of (a) Si/$Si_{0.8}Ge_{0.2}$ heterojunction before contact (not scaled) (b) *n*-type $Si_{0.8}Ge_{0.2}$/Si/$Si_{0.8}Ge_{0.2}$ heterojunction after contact (c) *p*-type Si/$Si_{0.8}Ge_{0.2}$/Si heterojunction after contact

Since carriers tend to stay in the lowest energy states, for *p*-type Si/$Si_{1-x}Ge_x$ quantum well, holes are confined in $Si_{1-x}Ge_x$ wells. For *n*-type Si/$Si_{1-x}Ge_x$ quantum well, Si serves as the quantum well for electrons. However, the conduction band discontinuity between silicon and $Si_{1-x}Ge_x$ (~100meV) is negligible, which results in high probability of thermionic emission and tunneling over the potential barrier, reducing quantum confinement. The strain effect, arising from lattice mismatch of heterostructures, has to be implemented for the band structure engineering to achieve sufficient electron confinement in *n*-type Si/SiGe, which will be discussed in section 3.3.2.

Due to the existence of concentration gradient between undoped quantum wells and heavily doped quantum barriers, upon initial contact, majority carriers in barriers diffuse into the adjacent well layers while minority carriers diffuse opposite, leaving uncovered

nuclei behind, which creates build-in electrical field to suppress the further diffusion of carriers. Upon thermal equilibrium, the drift and diffusion currents balance and there is no net current flow. Carriers are redistributed into wells with enhanced mobility resulting from limited carrier-impurity scattering in the wells.

3.3.2 STRAIN EFFECT ON ENERGY BAND STRUCTURE

$Si_{1-x}Ge_x$ (x<0.85) alloy exhibits Si-like band structure, having six-fold degenerate conduction band minima. Si and Ge have the lattice constant of 5.43Å and 5.66Å, respectively; the lattice constant of $Si_{1-x}Ge_x$ increases with increased Ge context. For strained $Si_{1-x}Ge_x$ layer grown on unstrained $Si_{1-y}Ge_y$ substrate (or layer), if $x > y$, $Si_{1-y}Ge_y$ retains its lattice space and shortens in-plane lattice constant of $Si_{1-x}Ge_x$; as a consequence of Poisson's ratio, the lattice constant perpendicular to the interface stretches. In this case, $Si_{1-x}Ge_x$ is subjected to compressive in-plan strain as shown in Figure 8(a); and in contrast if $y>x$, $Si_{1-x}Ge_x$ layer experiences tensile in-plane strain in order to accommodate the lateral lattice constant of underlying material as shown in Figure 8(b) [17].

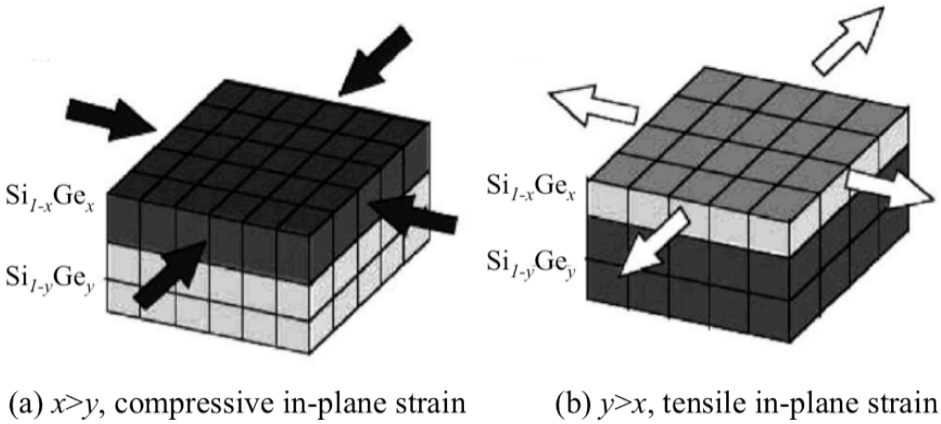

Figure 8. For strained $Si_{1-x}Ge_x$ layer grown on unstrained $Si_{1-y}Ge_y$ substrate (or layer): (a) if $x>y$, $Si_{1-x}Ge_x$ is subjected to compressive in-plan strain; and (b) if $y>x$, $Si_{1-x}Ge_x$ experiences tensile in-plane strain [17]

At initial epitaxial growth, the lattice mismatch is accommodated by elastic distortion but beyond certain critical thickness (h_C), the relaxation of film occurs accompanied with the formation of misfit dislocations, which is detrimental to the devices. Figure 9(b) shows the critical thickness as a function of Ge ratio for MBE $Si_{1-x}Ge_x$ grown on bulk (100) Si at 550°C [17-18]. Using the data from figure 9(b) as a rough estimation, for $Si_{0.8}Ge_{0.2}$ and $Si_{0.6}Ge_{0.4}$ grown on bulk (100) Si substrate the critical thickness is about 10nm and 5nm, respectively, which indicates the maximum stabilized films thickness. Figure 10 (a) illustrated the film structure of *p*-type Si/SiGe/Si QW grown on SOI/SiOG substrate, on top of which strained-SiGe and relaxed-Si layers grow successively. The thickness of strained intrinsic SiGe well layers need to stay below the critical thickness to avoid the occurrence of film relaxation.

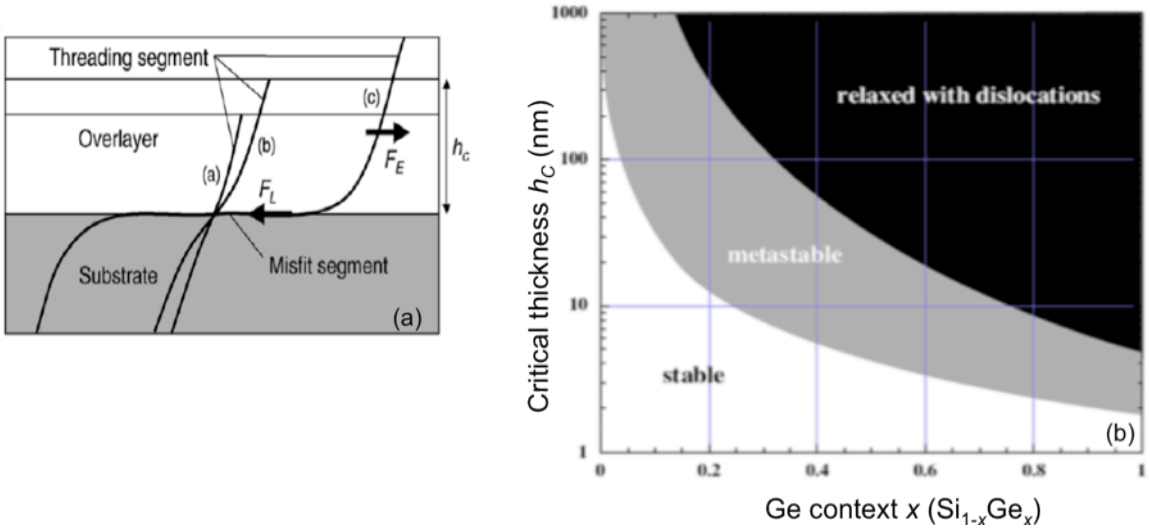

Figure 9. (a) Schematic illustration of the Matthews and Blakeslee model of critical thickness (h_C) and (b) the critical thickness as a function of Ge ratio for growth at 550°C [17-18]

For *n*-type SiGe/Si/SiGe QW structure, sufficient electron quantum confinement in Si layers can be achieved by means of tensile strain induced energy band engineering exerted on Si layers grown on SiGe virtual substrate of larger lattice constant. Figure 10(b) demonstrates the structure of *n*-type SiGe/Si/SiGe QW grown on a graded SiGe buffer layer on top of SOI/SiOG substrate. The dislocation of relaxed $Si_{1-x}Ge_x$ film grown on SiOG (or SOI) substrate can be reduced by linearly or step-wise increasing the Ge ratio from 0 to desired value *x*. The thickness of each strained-Si layer needs to be controlled under the corresponding critical thickness (h_C) to avoid the relaxation of film.

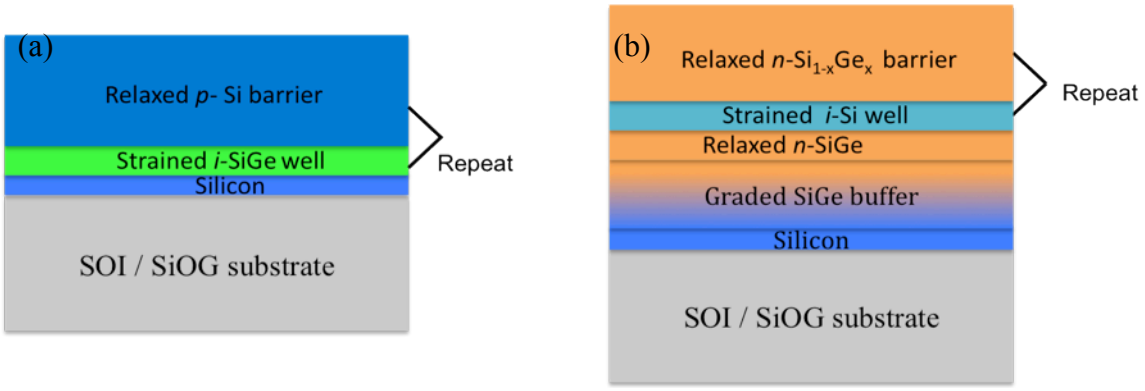

Figure 10. Schematic diagrams of (a) *p*-type Si/SiGe/Si QW structure on SOI/SiOG substrate and (b) *n*-type SiGe/Si/SiGe QW structure on graded SiGe buffer layer on SOI/SiOG substrate

Si/SiGe heterostructure enables band-engineering technology by utilizing the strain effect. Hydrostatic strain, which shifts the energy band edge, and uniaxial strain, which splits the degeneracy of energy bands are the two components of strain. Due the energy band shifting and splitting, important material parameters are affected, including the conduction and valance band energy, bandgap, curvature of bands (or effective mass) and transport properties.

Numerous of papers have calculated the band structure for Si/SiGe heterostructures using pseudopotentials or k.p methods [19]-[22]. However, some of these calculations contradict each other mainly due to the lack of experimental measured data in the strained-SiGe system. The band structure used in this research will be predominantly that calculated by pseudopotential approach in references [18]. Figure (11) and (12), respectively, show the discontinuities of conduction band ($\Delta E_C = E_C(x) - E_C(y)$) and valence band ($\Delta E_V = E_V(x) - E_V(y)$) for strained $Si_{1-x}Ge_x$ active layer on a relaxed $Si_{1-y}Ge_y$ substrate. In figure 10 of ΔE_C, negative value in blue indicates that strained $Si_{1-x}Ge_x$ active layer provides lower energy quantum well for electrons to occupy; and vice verse, in figure 11 of ΔE_V, positive value in red region corresponds to strained $Si_{1-x}Ge_x$ active layer served as quantum well for holes. For electron confinement in strained Si active layer (x=0), ΔE_C versus Ge ratio of relaxed $Si_{1-y}Ge_y$ substrate (or heterolayers) can be found by the contours intersecting with the left axis in figure 11. As substrate Ge ratio (y<0.85) increases, ΔE_C enlarges which yields better electron confinement in QW layers. In similar fashion, for hole confinement in strained $Si_{1-x}Ge_x$ active layer on relaxed Si substrate or heterolayers (y=0), ΔE_V as a function of Ge context can be read from the bottom axis of figure 12. Similarly, ΔE_V increases as Ge ratio increases. The band gap in for strained $Si_{1-x}Ge_x$ grown on $Si_{1-y}Ge_y$ virtual substrates was shown in figure 13.

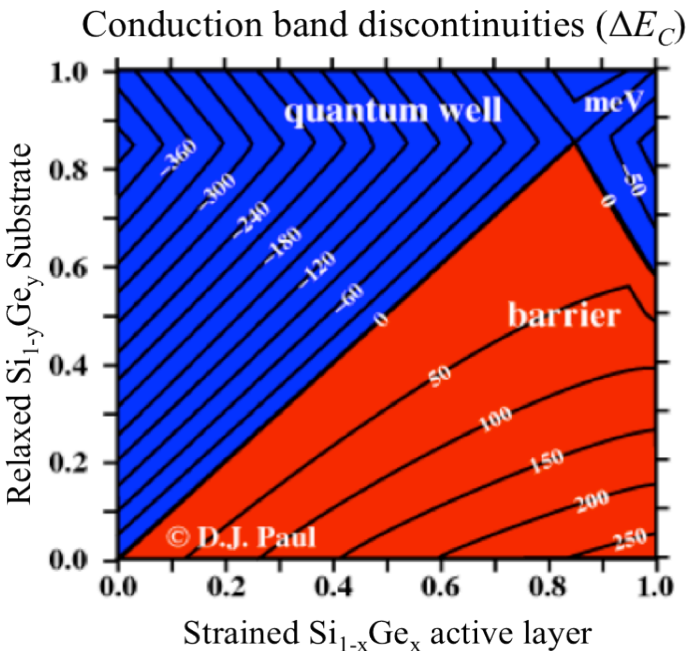

Figure 11. Conduction band discontinuities $E_C(x)$-$E_C(y)$ in meV between strained $Si_{1-x}Ge_x$ active layer on a substrate of relaxed $Si_{1-y}Ge_y$ [18]

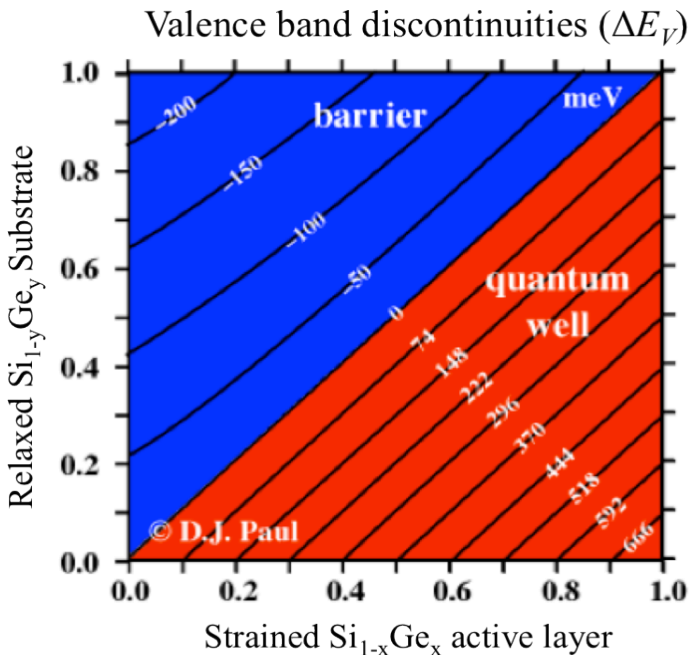

Figure 12. Valence band discontinuities in meV $E_V(x)$-$E_V(y)$ between strained $Si_{1-x}Ge_x$ active layer on a substrate of relaxed $Si_{1-y}Ge_y$ [18]

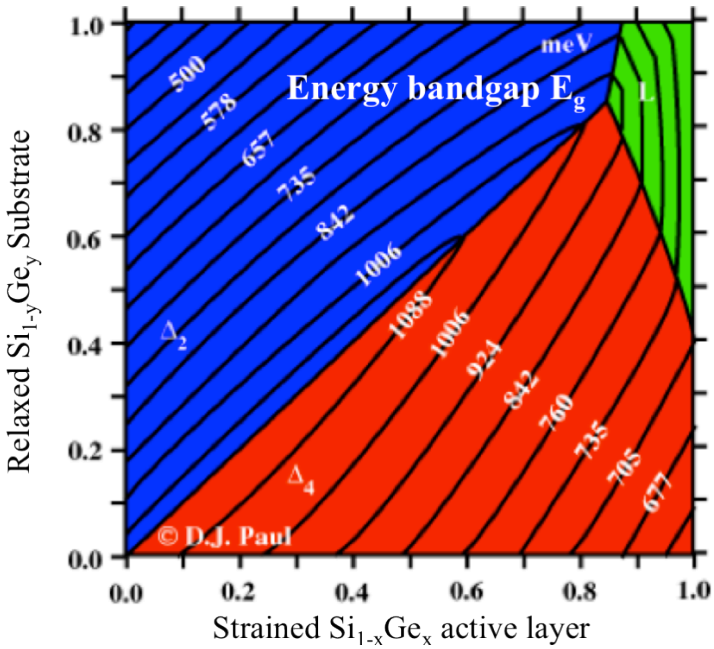

Figure 13. The band gap in meV for strained $Si_{1-x}Ge_x$ grown on $Si_{1-y}Ge_y$ virtual substrates. The data for compressively strained layers is that from pseudopotential theory [18].

Si/SiGe QW band alignment parameters used in ALTAS were taken from figures 11-13. For *n*-type SiGe/Si/SiGe simulation, ΔE_C from figure 11 was used to adjust the electron affinity of $Si_{1-x}Ge_x$ ($\chi_{Si1-xGex}= \chi_{Si}-\Delta E_C$), where electron affinity of Si (χ_{Si}) equals to 4.05*eV*; for *p*-type Si/SiGe/Si simulation, ΔE_V from figure 12 was used. Bandgap energy in figure 13 was used as the bandgap energy of intrinsic strained $Si_{1-x}Ge_x$ at 300K. The bandgap narrowing effect due to elevated temperature as well as heavily doped was taken into account using default BGN model in ATLAS [15].

3.4 Simulation Structures And Parameters Extraction

Only *n*- and *p*-type Si/SiGe QW structures were simulated in ATLAS, excluding the underneath substrate due to limitation of available grid nodes in the simulator. The parasitic effects from the substrate will be considered and discussed later in chapter 6.

To satisfy the maximum grid nodes limitation in ATLAS, the simulation structures were scaled down and the simulation results can be safely applied to different device sizes since Seebeck coefficient is merely temperature and material dependent but size independent.

The 2D ATLAS simulation structure consists of 11 periods of alternating intrinsic well and heavily doped barrier layers; and the simulated *p*-type Si/SiGe/Si QW structure is illustrated in figure 14(a). The total film stack thickness depends on the combined width of well and barrier. Both thermal and electrical contacts (illustrated by the grey bars) are placed simultaneously at the vertical ends of the structure so that both heat and electrical current flow parallel (*x* direction) to the superlattice layers. A thermal condition of 10K temperature gradient is maintained across 3μm-long film stacks. However, a practical TE element can be several centimeters long with hundreds of Kelvin temperature difference.

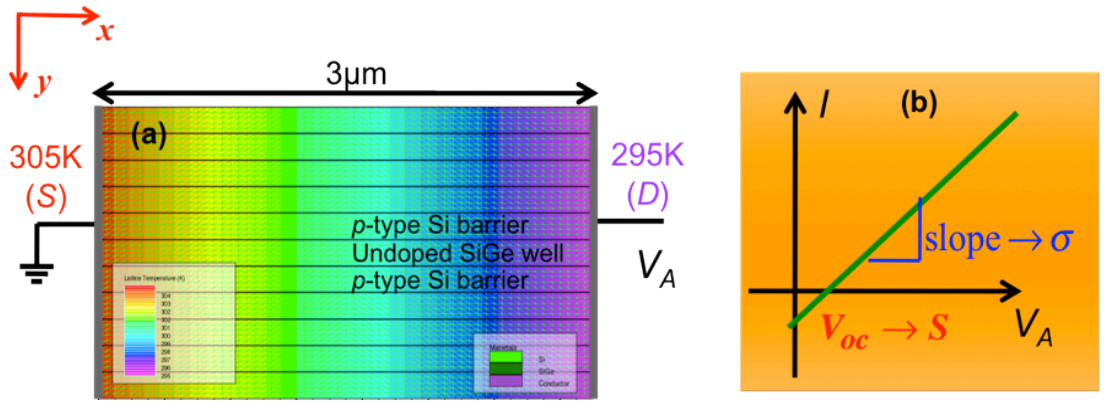

Figure 14. (a) Simulation structure of 3μm-long *p*-type Si/SiGe/Si QW, which consists of 11 periods of alternating intrinsic well and heavily doped barrier layers. The hot-side electrode (source) is grounded while applied voltage (V_A) is swept linearly at cold-side electrode (drain) to counteract the thermal voltage, (b) *I-V* characteristic curve, When the net current flow is zero (open-circuit condition), $\tilde{S}$ is obtained using the open circuit voltage (V_{OC}) divided by the applied temperature difference (ΔT) while $\tilde{\sigma}$ is calculated from the slope of the curve near short-circuit current taking the geometry of the structure into account.

Assuming no heat loss from the top or bottom surfaces, a fixed temperature difference is maintained across the QW structures with ideal ohmic electrical contacts. The hot-side electrode (denoted as source terminal) is grounded while applied voltage (V_A) is swept linearly at cold-side electrode (denoted as drain) to counteract the thermal voltage as illustrated in figure 14(a) and (b). When the net currents flow is zero (open-circuit condition), the effective Seebeck coefficient ($\tilde{S}=V_{OC}/\Delta T$) of the entire film stacks is obtained using the open circuit voltage (V_{OC}) divided by the applied temperature difference (ΔT). From *I-V* characteristic curve, the effective electrical conductivity of the entire QW stack ($\tilde{\sigma}$) is calculated from the slope of the curve near short-circuit condition taking the geometry of the structure into account as shown in figure 14(b). Note that for simplicity tilde mark (~) over symbol is used to denote the weighted average of certain parameter across the entire QW films stack. The effective carrier concentration of the

entire film stacks ($\tilde{n}$ or $\tilde{p}$) was obtained using the integrated doping of the entire film stack divided by the area of the whole stack.

Additionally, to verify the carrier confinement inside the quantum well layers, either effective electron concentration ($\tilde{n}'$) inside Si QW of *n*-type SiGe/Si/SiGe structure or effective hole concentration ($\tilde{p}'$) inside SiGe QW of *p*-type Si/SiGe/Si structure was calculated. The effective carrier concentration inside the quantum well layers ($\tilde{n}'$ or $\tilde{p}'$) was computed using the integrated dose, the concentration integral within the center quantum well over its length and thickness, divided by the area of itself. For convenience, single quote mark denotes the weighted average of parameter inside the center quantum well layer.

In this chapter, the framework of basic physical models incorporated with heat transferring and Seebeck effect in ALTAS were introduced. Next, the energy band structures and alignments of Si/SiGe material taking into account of lattice-mismatch induced strain effect were discussed. The energy band structure parameters from reference [18] were implemented in multi-layer QW simulation correspondingly. Moreover, the QW simulation structures as well the strategies of parameters' extraction have been discussed.

CHAPTER 4

THERMOELECTRIC OPTIMIZATION AT ROOM TEMPERATURE

Seebeck coefficient simulations at room temperature were conducted on both bulk *p*- and *n*-type Si and SiGe alloy, and simulated results were compared to experimental counterparts. The simulated Seebeck coefficient is inversely proportional to the bulk material doping concentration, which agrees with reported data. The magnitude of simulated Seebeck coefficient using default parameters, however, deviates from the experimental data. Based on the analytic model for Seebeck Coefficient implemented in ALTAS, adjustments by modifying the effective density of states N_C (N_V) for *n*-type (*p*-type) material were performed in order to better match experimental results. During this adjustment process, the density of states of minority carriers (N_V for *n*-type or N_C for *p*-type material) was also modified correspondingly to maintain the law of mass action ($n_i^2=np$).

After the verification of bulk Seebeck coefficient, QW simulations at 300K were conducted using the methodology discussed in chapter 3. TE parameters (S, σ, $S^2\sigma$ and ZT) as a function of well thickness (t_W), barrier thickness (t_B), barrier doping concentration and Ge ratio were simulated and parameter optimization based on the simulation results is discussed. To avoid any redundancy only *p*-type Si/SiGe/Si QW

structure are discussed and analyzed thoroughly while the results of *n*-type SiGe/Si/SiGe are briefly mentioned for comparisons.

4.1 SIMULATED SEEBECK COEFFICIENT OF BULK SILICON AND SILICON-GERMANIUM

It is necessary to compare the simulated Seebeck coefficient of bulk Si and SiGe to reported counterparts at 300K before advancing to QW simulation. Initially, default model parameters were employed for simulation, which gave rise to correct relationship between S and carrier concentration (n), S decreases as the n increases; however, the absolute values of S were 50-150% smaller than the experimental data. After evaluating the analytic model of S, equation (3.10-3.11), in ALTAS, it was found that the diffusive component (S_d) has the dominant contribution to total S. S_d is determined mainly by N_V and N_C, which has the default values of 1.04×10^{19} and $2.8\times10^{19}cm^{-3}$, respectively, at 300K. Therefore, in order to obtain better match between simulated and reported S, an increase of S_d resulting from enhanced N_V or N_C is one feasible solution. Specifically, for *p*-type material, N_V is first optimized in order to match experimental value of S; then N_C is adjusted correspondingly to ensure the consistency of mass-action law. In like manner, for *n*-type material, N_C is first determined by reported value of S followed by the calculation of N_V using N_C and n_i. The simulated and reported absolute values of Seebeck coefficient ($|S_{Si}|$) at 300K versus carrier concentration ranging from 10^{14} to 5×10^{20} cm^{-3} for bulk *p*- and *n*-type Si alloy was superimposed in figure 15, where the scattered dots are experimental data extracted from literature [23-25] and the lines represent the results of simulation. Due to limitations of the analytic model for S, the slope of these simulated curves is not adjustable, which results in simulated S to be underestimated in lightly and moderate doped region and overestimated in degenerate region. Furthermore, the

simulated and experimental data [26-27] of $\left|S_{Si_{0.8}Ge_{0.2}}\right|$ at 300K as a function of carrier concentration for bulk *p*- and *n*-type $Si_{0.8}Ge_{0.2}$ is presented in figure 16.

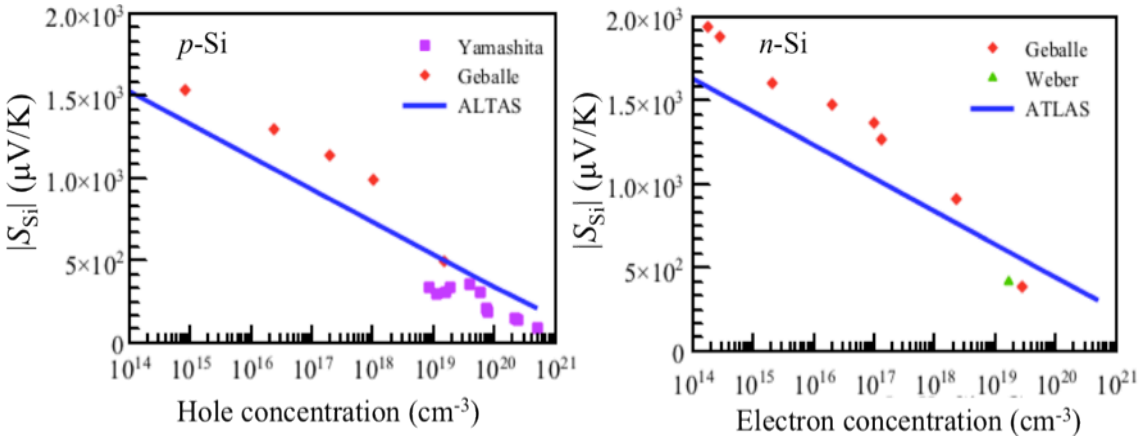

Figure 15. Overlay of simulated and reported Seebeck coefficient of bulk *p*- and *n*-type Si alloy where the scattered dots are experimental data extracted from different literatures [23-25] and the blue lines represent the simulation results.

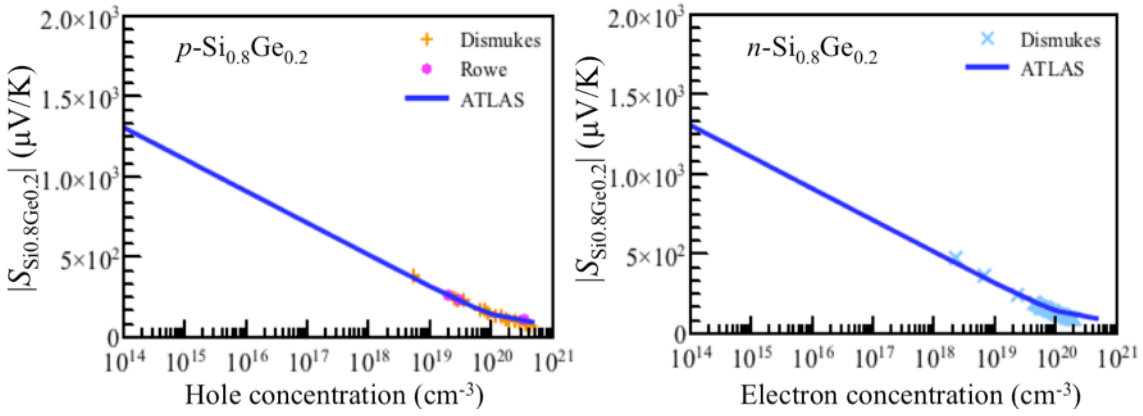

Figure 16. Overlay of simulated and reported Seebeck coefficient of bulk *p*- and *n*-type $Si_{0.8}Ge_{0.2}$ alloy where the scattered dots are experimental data extracted from different literatures [26-27] and the blue lines represent the simulation results.

4.2 Simulation of *P*-Type Silicon/Silicon-Germanium Quantum Well

4.2.1 Influence of Quantum Well Width

As a means to optimize the quantum well thickness to maximize TE performance, *p*-type $Si/Si_{0.8}Ge_{0.2}/Si$ QW structures were simulated with various quantum well thicknesses at fixed barrier thickness. $Si_{0.8}Ge_{0.2}$ quantum wells with thickness (t_W) ranging from 1 to 20 nm are surrounded by *p*-type Si barriers with a fixed thickness of 20nm (t_B=20nm). Moreover, for each quantum well and barrier thickness combination, a set of Si barrier doping concentration at 10^{18} (blue), 5×10^{18} (red), 10^{19} (green), 5×10^{19} (orange) and $10^{20}cm^{-3}$ (pink) were simulated to optimize well thickness over a range of barrier concentration. Each color consistently represents specific barrier doping level throughout this chapter.

Table 1. Simulations of *p*-type $Si/Si_{0.8}Ge_{0.2}/Si$ QW structures at 300K with various barrier doping (p_B) and QW thickness (t_W)

Constant		**Variable**					
Barrier thickness t_B (nm)	QW doping (cm^{-3})	Barrier doping (cm^{-3})	QW thickness t_W (nm)				
20	10^{14}	10^{18}	1	2	3	…	20
		5×10^{18}					
		10^{19}					
		5×10^{19}					
		10^{20}					

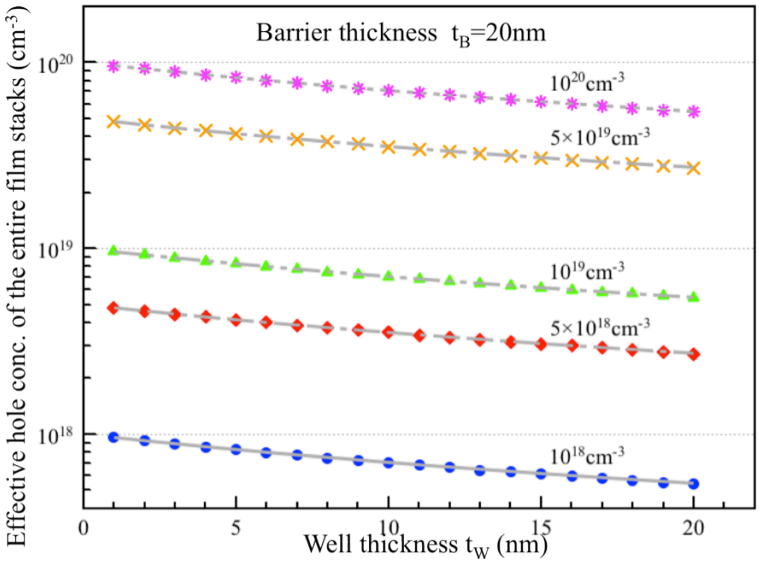

Figure 17. $\tilde{p}$ versus QW thickness (t_W) at different barrier doping levels. The scattered dots were simulation results extracted from ATLAS using integrated dose throughout the entire film stacks divided by the corresponding area. The grey dash lines were calculated using the equation (4.1)

In figure 17, the effective hole concentration of the entire film stacks ($\tilde{p}$) versus QW thickness (t_W) at different barrier doping levels were plotted. The scattered dots were simulated results extracted from ATLAS using the integrated dose throughout the entire film stacks divided by the corresponding area. While the grey dash lines were calculated using the equation (4.1), given as:

$$\tilde{p} = \frac{p_B t_B + p_W t_W}{t_B + t_W} \approx \frac{p_B}{1 + t_W / t_B} \tag{4.1}$$

where p_B, p_W, t_B and t_W are barrier doping, quantum well doping, barrier thickness and quantum well thickness, respectively. It was observed that the calculated $\tilde{p}$ using above-mentioned two methods match exactly, which indicates that $\tilde{p}$ is dependent on neither the doping redistribution between heavily doped barriers and intrinsic quantum wells nor

the quantum confinement effect. If p_B is substantially higher than p_W, $\tilde{p}$ can be simplified to the expression of p_B and t_W/t_B ratio as shown in equation (4.1) where $\tilde{p}$ increases as an increase of p_B and a decrease of t_W/t_B.

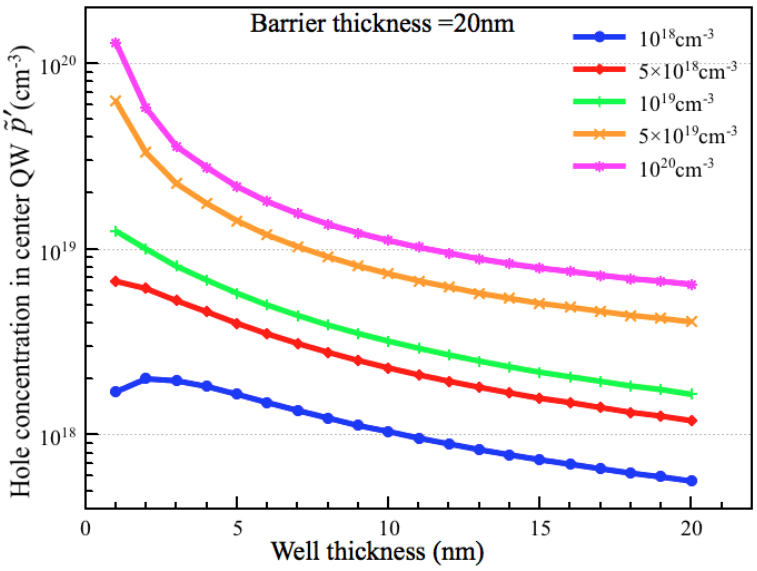

Figure 18. $\tilde{p}'$ versus t_W at different barrier doping p_B and 20nm barrier thickness

The effective hole concentration inside $Si_{0.8}Ge_{0.2}$ quantum well ($\tilde{p}'$) was calculated using the integrated dose in the center QW divided by the corresponding area and was plotted versus QW thickness in figure 18. Compare figure 17 and 18, it was noted that as t_W reduces both $\tilde{p}$ and $\tilde{p}'$ increase. In order to distinguish the increment of $\tilde{p}'$ derived from quantum confinement or increased $\tilde{p}$, $\tilde{p}'$ was normalized by $\tilde{p}'$. The $\tilde{p}'/\tilde{p}$ ratio versus QW thickness at different barrier doping was plotted in figure 19. At specific t_W/t_B ratio, if $\tilde{p}'$ exceeds $\tilde{p}$ ($\tilde{p}'/\tilde{p}>1$), it can be undoubtedly concluded that carrier confinement exists in the quantum well. Quantum confinement is more pronounced in 10^{18} cm^{-3} barrier doping, and diminishes as the barrier doping increases. For 10^{18} cm^{-3} barrier doping, quantum confinement is enhanced as t_W decrease down to 4 nm, arrived

its maximum at t_W of 2-4 nm and then declined at t_W of 1 nm. With the increase of barrier doping, quantum confinement appears significantly in thinner and thinner t_W structures.

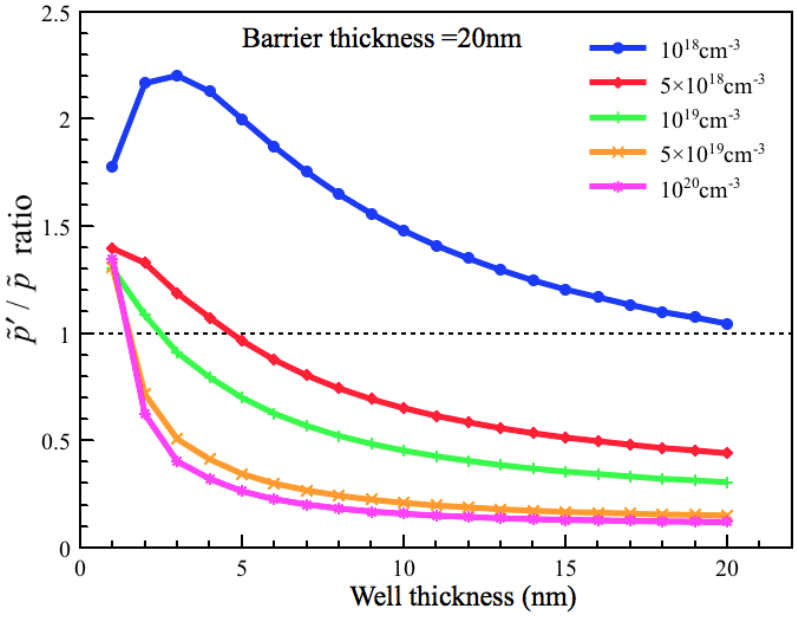

Figure 19. The $\tilde{p}'/\tilde{p}$ ratio versus QW thickness at different barrier doping, which is useful to distinguish the enhanced $\tilde{p}'$ at smaller QW thickness.

In order to better understand the influences of p_B and t_W to quantum confinement, the hole concentration profile of the center barrier/well/barrier film stack (at x=1.5μm) versus the film thickness (as the vertical red lines indicated in the film stacks in figure 20 (a) and (b) for two extreme well thickness (t_W=1 and 20 nm) were plotted in figure 20(c) and (d), correspondingly. The vertical dotted lines in figure 20 (c) and (d) depict boundaries between quantum wells and barriers. It can be found that for t_W=1nm, p_W was greater than p_B at various barrier doping levels, which again proved the existence of quantum confinement. If the barrier concentrations are severely high (≥5×10^{19} cm^{-3}), however, quantum confinement diminishes as seen by the hole concentration dip inside the

$Si_{0.8}Ge_{0.2}$ quantum well. Regarding 20nm well thickness counterparts as shown in figure 20 (d), quantum confinement slightly happens at the barrier concentration of $10^{18}cm^{-3}$ and vanishes at doping levels greater than $10^{18}cm^{-3}$.

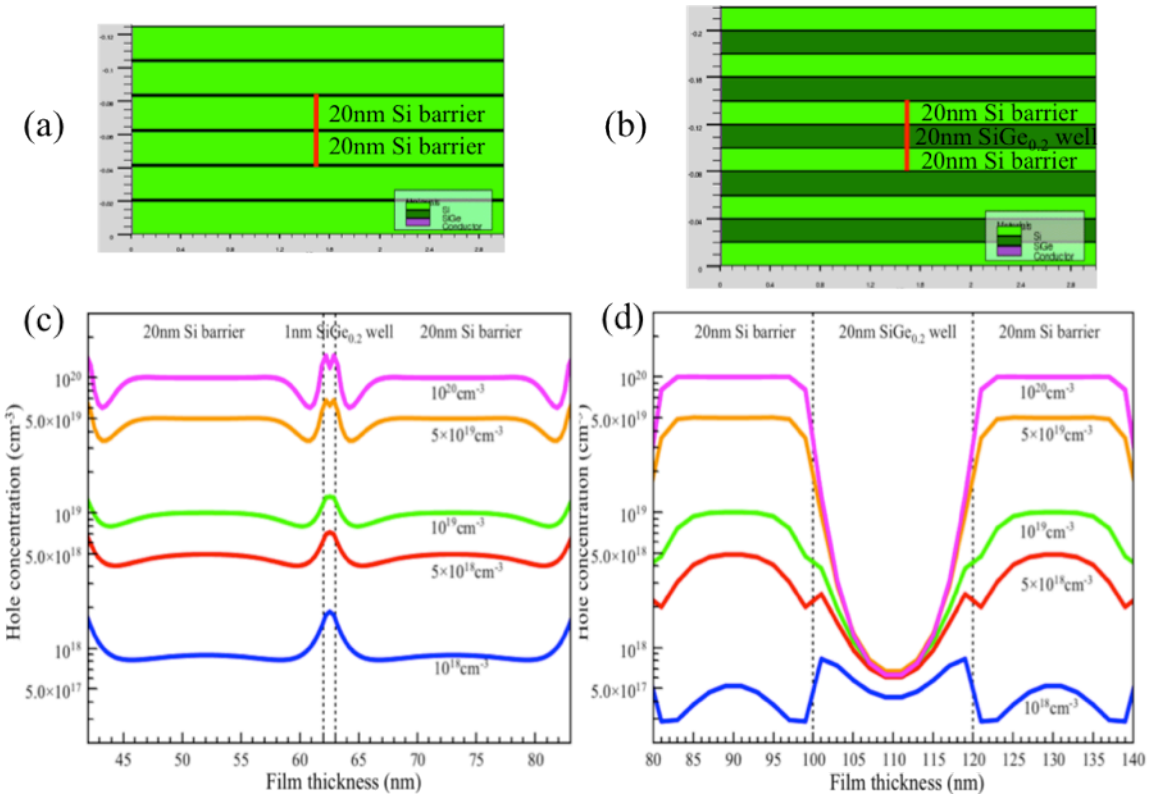

Figure 20. Hole concentration profile of 11 periods *p*-type $Si/Si_{0.8}Ge_{0.2}/Si$ QW film stack with QW thickness of (a) 1nm and (b) 20nm; Hole concentration of the center barrier/well/barrier versus film thickness with QW thickness of (c) 1nm and (d) 20nm

It would be more insightful to further investigate the energy band structures of the center QW film stack. In figure 21, the energy band versus center barrier/well/barrier film thickness was shown for t_W=4nm. The horizontal dotted lines represent hole Fermi level (E_f); a series of curves above E_f are conduction band energy (E_C) and a set of curves below E_f are valence band energy (E_V). As hole doping level increases, E_f moves downward; therefore, the offset of E_f between the intrinsic quantum well and *p*-type barrier increase as an increase of barrier doping, which results in extra band bending between Si/$Si_{0.8}Ge_{0.2}$ heterostructures. Consequently, hole confinement in $Si_{0.8}Ge_{0.2}$ layer diminishes and even ceases as the barrier doping increases; and eventually when the energy difference (E_f-E_V) of $Si_{0.8}Ge_{0.2}$ exceeds that of Si, the original Si barrier becomes the lowest energy states for holes to occupy.

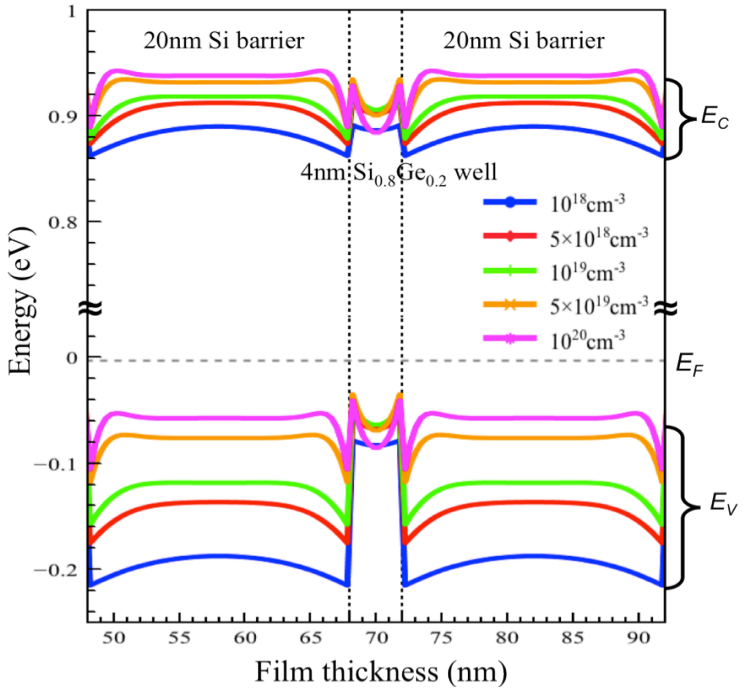

Figure 21. Enlarged conduction and valence band versus center barrier/well/barrier film thickness with t_B of 20nm and t_W of 4nm at different barrier levels.

Compare figure 17 and 20, for 20 nm barrier thickness structures, the thinner the quantum well, the higher $\tilde{p}$. Effective electrical conductivity of the entire film stack ($\tilde{\sigma}$) as a function of quantum well thickness at multiple barrier doping levels with barrier thickness of 20 nm are superimposed, as shown in figure 22. When barrier doping increases from 10^{18} to 10^{20} cm^{-3}, $\tilde{\sigma}$ has an increase of two orders of magnitude and hence was plotted on a logarithmic scale.

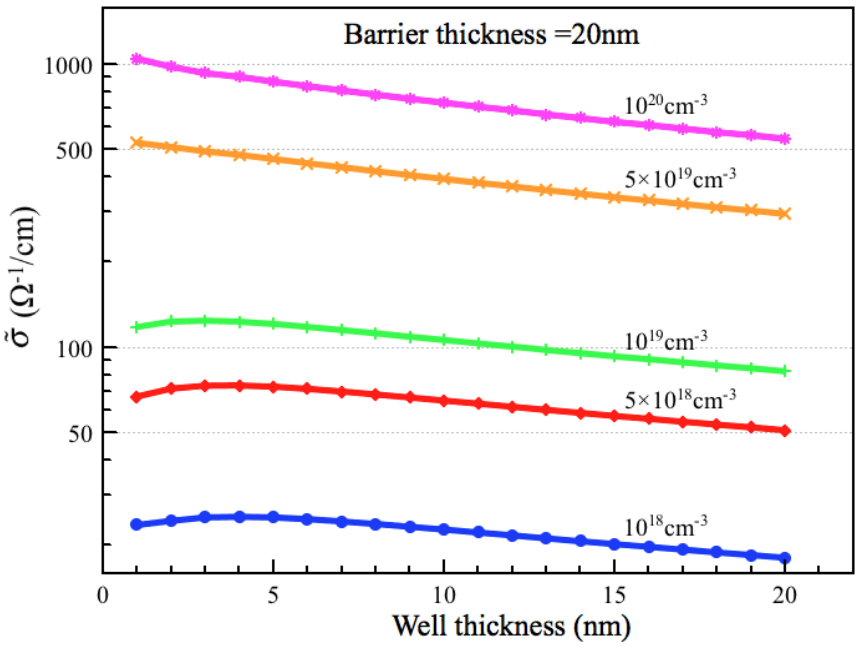

Figure 22. $\tilde{\sigma}$ as a function of quantum well thickness at multiple barrier doping levels with barrier thickness of 20nm

The hole mobility values of Si and $Si_{0.8}Ge_{0.2}$ superlattice films were taken from their bulk counterparts as a function of doping concentration and Ge ratio. Electron and hole mobility (μ_n and μ_p) of bulk Si_xGe_{1-x} versus Ge content (x) at 300K is shown in figure 23 [28]. For lightly doped Si (x=0), at 300K, μ_n and μ_p approximate to be 1400 and

450 $cm^2V^{-1}s^{-1}$, respectively, where both μ_n and μ_p decrease as Ge content (x<0.6) increases.

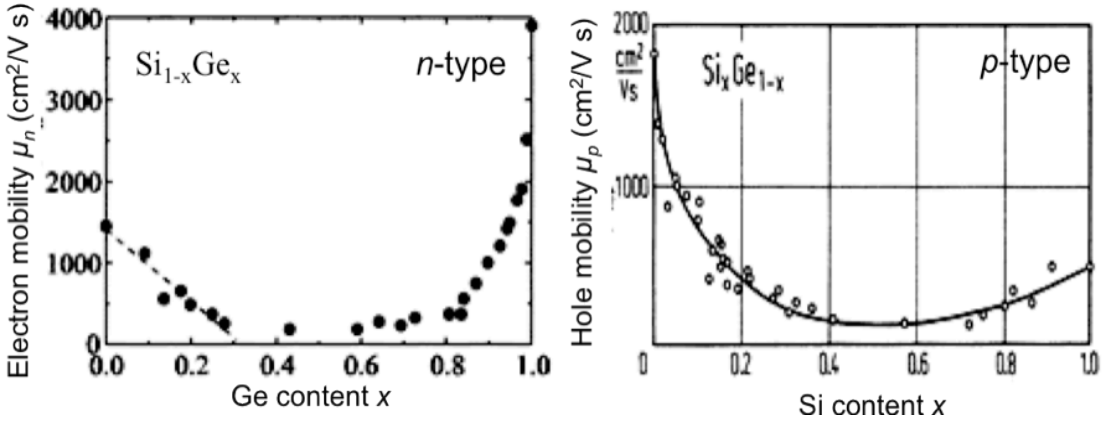

Figure 23. Electron and hole mobility (μ_n and μ_p) of $Si_{1-x}Ge_x$ alloy at 300K [28]

Figure 24 shows the effective Seebeck coefficient of the entire film stacks ($\tilde{S}$) versus well thickness at multiple barrier doping levels with barrier thickness of 20 nm was overlaid. Due to the fact that Seebeck coefficient is inversely proportional to carrier concentration, at fixed barrier to well thickness ratio (t_B/t_W), $\tilde{S}$ reduces as the barrier doping increases. Moreover, for barrier doping less than 5×10^{19} cm^{-3}, $\tilde{S}$ decreases as well thickness (t_W) decreases down to ~5nm. Then as t_W continues to reduce, $\tilde{S}$ becomes to increase; for barrier doping greater than 10^{19} cm^{-3}, $\tilde{S}$ monotonously reduces as t_W decreases. The enhanced $\tilde{S}$ of barrier doping less than 5×10^{19} cm^{-3} with well thickness below 5 nm results from effective quantum confinement existing in that region.

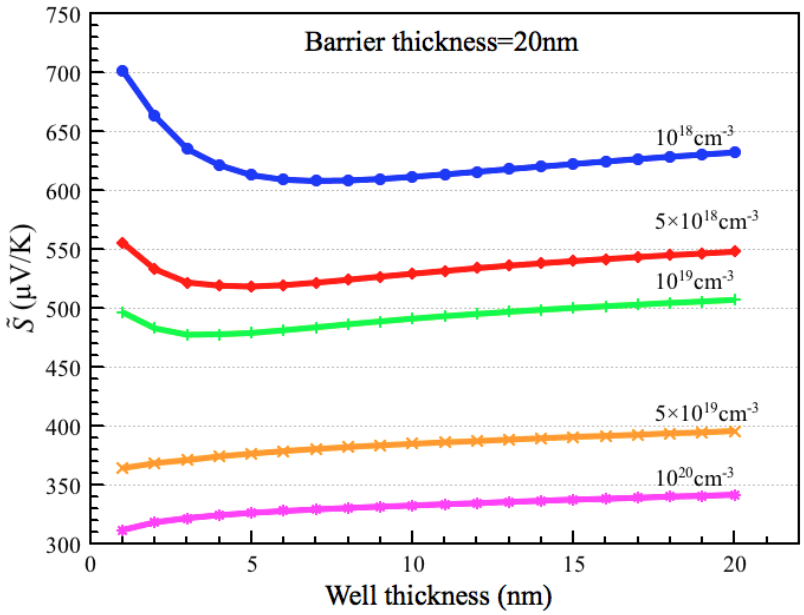

Figure 24. $\tilde{S}$ as a function of t_W at multiple barrier doping levels with t_B of 20nm

Thermal power ($\tilde{S}^2\tilde{\sigma}$), or the numorator in ZT expression, versus t_W at set of barrier doping levels with barrier thickness of 20 nm was overlaid in figure 25. It was found that the heavier the barrier doping and the smaller the t_W, the larger $\tilde{S}^2\tilde{\sigma}$ was.

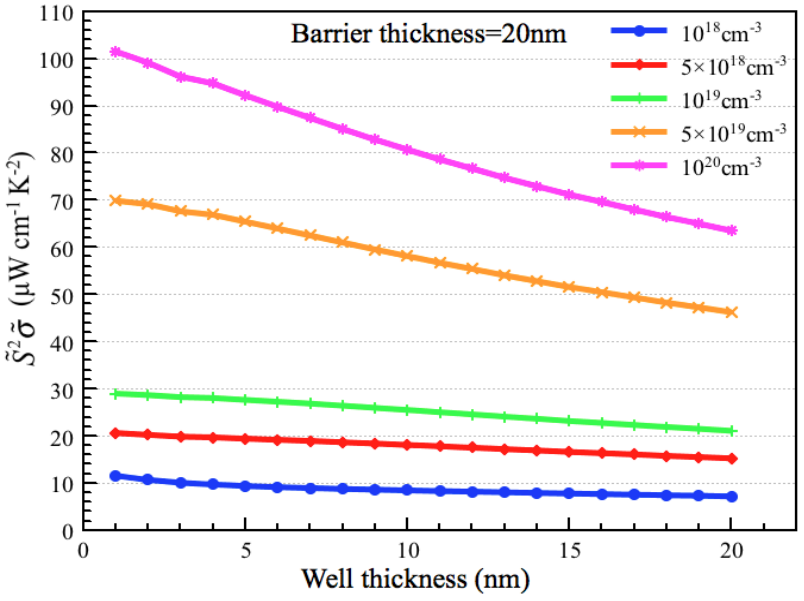

Figure 25. $\tilde{S}^2\tilde{\sigma}$ as a function of t_W at multiple barrier doping levels with t_B of 20nm

At 300K, thermal conductivity (κ) of bulk Si is 148 $Wm^{-1}K^{-1}$. W. Liu and coworkers managed to measure thermal conductivity of ultra-thin single crystal Si on insulator [29]. Their experimental and modeling results were shown in figure 26, which reveals strong size dependence of Si thermal conductivity, where κ of thin film Si is ~22 W $m^{-1}K^{-1}$ at 300K, five times smaller than its bulk counterpart. In contrast, bulk $Si_{0.8}Ge_{0.2}$ has a thermal conductivity about 62.8 $Wm^{-1}K^{-1}$ at 300K, and $Si_{0.8}Ge_{0.2}$ thin film is expected to possess an even smaller value. It is difficult to accurately measure thermal conductivity of Si and SiGe thin films and ALTAS does not provide any size dependent thermal conductivity model. The main effort of this work was attempting to maximize *ZT* via optimizing the thermal power ($\tilde{S}^2\tilde{\sigma}$). Thermal conductivity value of 22 W $m^{-1}K^{-1}$ from reference [25] will be used as a rough estimation for both Si and $Si_{1-x}Ge_x$ QW TE performance calculation.

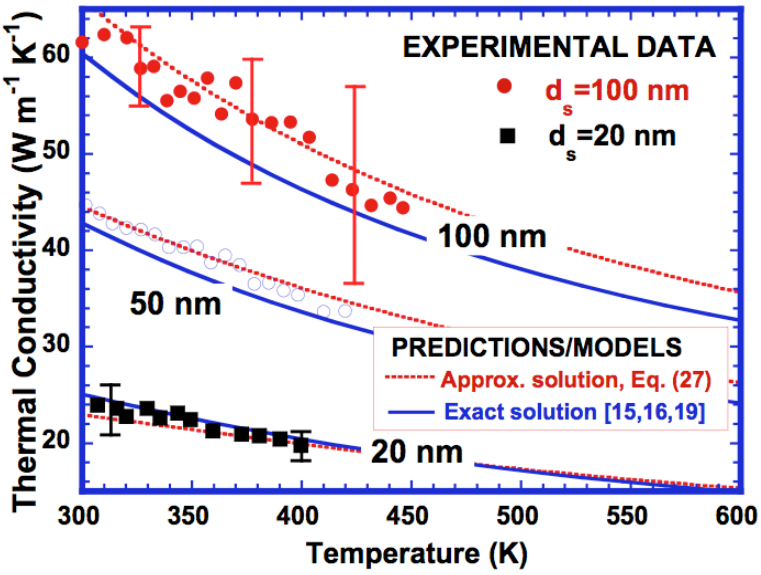

Figure 26. Experimental and modeling thermal conductivity on ultra-thin single crystal Si [29] that reveals strong size dependence of Si thermal conductivity

Based on above simulation results, thinner t_W and heavier n_B give rise to the highest $\tilde{S}^2\tilde{\sigma}$. However, the drawbacks associated with super thin quantum well film stacks are that, first, it is extremely challenging to grow such film with high quality; secondly, there is high probability of tunneling through thin QW reducing the quantum confinement inside. Consequently, a quantum well thickness of 4 nm was chosen as a compromise between above-mentioned tradeoffs and will continue to used for further simulation optimization.

4.2.2 Influence of Barrier Width

At fixed QW thickness, the optimized barrier thickness and doping will be investigated. With 4nm QW thickness (t_W=4nm), barrier thickness (t_B) ranges from 4 to 20nm which corresponds to barrier to well thickness ratio (t_B/t_W) from 1 to 5. Simulations to optimize barrier thickness and doping of *p*-type $Si/Si_{0.8}Ge_{0.2}/Si$ QW structures at room temperature are summarized in table 2.

Table 2. Simulations of *p*-type $Si/Si_{0.8}Ge_{0.2}/Si$ QW structures at 300K with various barrier doping and thickness

Constant		**Variable**					
QW thickness t_W (nm)	QW doping (cm^{-3})	Barrier doping (cm^{-3})	Barrier thickness t_B (nm)				
4	10^{14}	10^{18}	4	5	6	…	20
		5×10^{18}					
		10^{19}					
		5×10^{19}					
		10^{20}					

Figure 27 show the barrier width and doping dependence of $\tilde{p}$ with fixed well thickness of 4nm. As discussed in section 4.2.1, $\tilde{p}$ raises as an increase of p_B and a decrease of t_W/t_B ratio. At a given barrier doping, thicker barrier means that there are more carriers potentially available to spill into the intrinsic quantum wells.

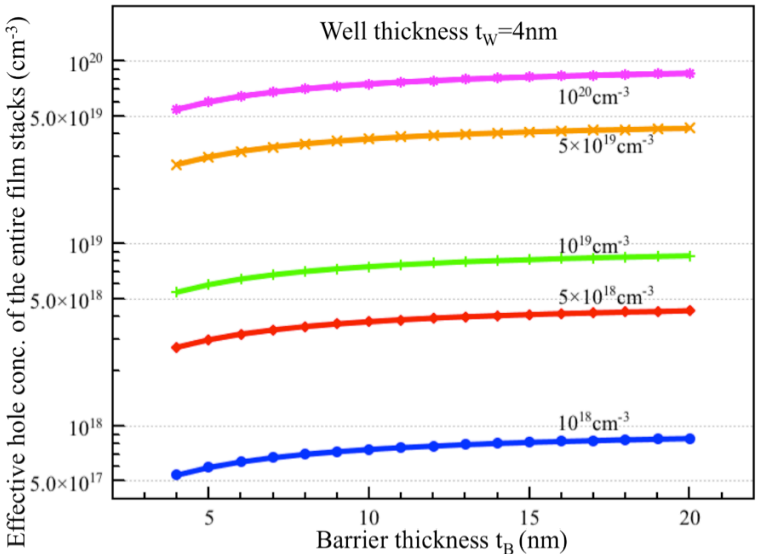

Figure 27. $\tilde{p}$ as a function of barrier witdth (t_B) and doping (p_B) with fixed well thickness of 4nm

Figure 28 shows the barrier witdth (t_B) and doping (p_B) dependence of $\tilde{p}'$ with fixed well thickness of 4nm. For p_B equals to 10^{18}cm^{-3}, $\tilde{p}'$ increases as the t_B increases. For p_B of 5×10^{18} and 10^{19} cm^{-3}, $\tilde{p}'$ increase as t_B increase up to 8 nm, where t_B/t_W equals to 2; as t_B continues to incrase, $\tilde{p}'$ begins to saturate. For p_B of 5×10^{19} and 10^{20} cm^{-3}, $\tilde{p}'$ is insensitive to the change of t_B.

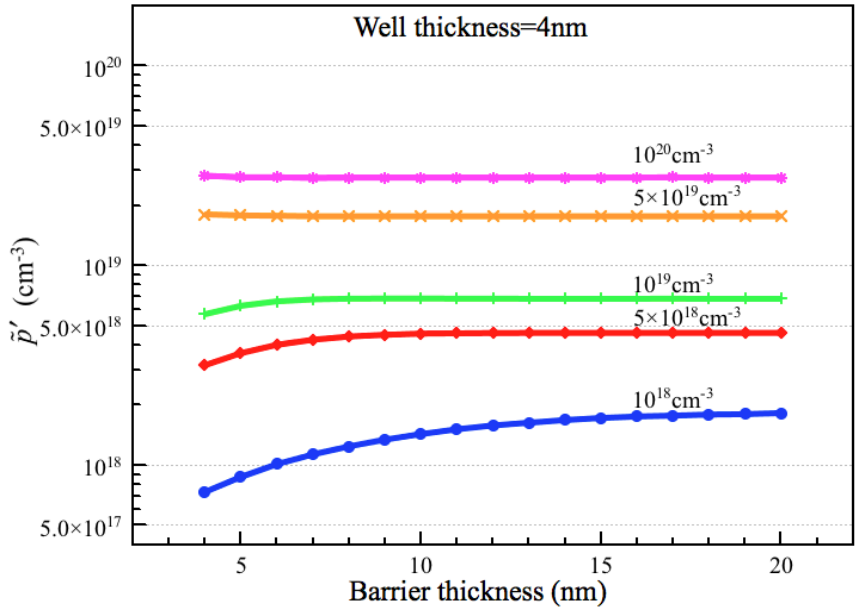

Figure 28. Hole concentration in the center QW ($\tilde{p}'$) as a function of barrier witdth (t_B) and doping (p_B) with fixed well thickness of 4 nm

$\tilde{\sigma}$ and $\tilde{S}$ as functions of barrier thickness (t_B) and doping (p_B) with t_W of 4nm are shown in figure 29 and 30, respectively. To better visualize the trend of $\tilde{\sigma}$ as a function of t_B, $\tilde{\sigma}$ was plotted in logarithmic scale. Comparing these two graphs, it is easy to find the inverse correlation between $\tilde{\sigma}$ and $\tilde{S}$.

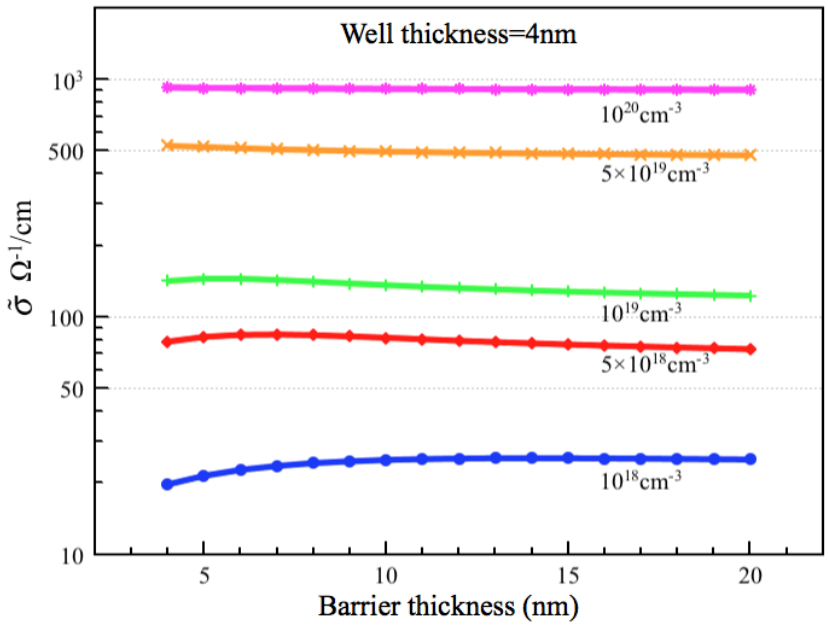

Figure 29. $\tilde{\sigma}$ as a function of barrier witdth (t_B) and doping (p_B) with fixed well thickness of 4 nm

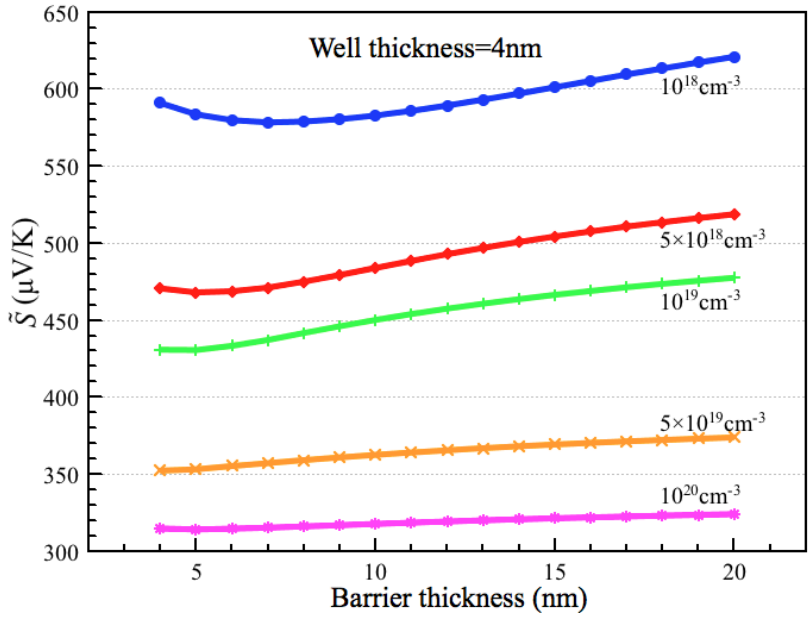

Figure 30. $\tilde{S}$ as a function of barrier witdth (t_B) and doping (p_B) with fixed well thickness of 4 nm

The calculated $\tilde{S}^2\tilde{\sigma}$ was plotted versus barrier thickness (t_B) and doping (p_B) at t_W of 4 nm in figure 31, where demonstrating that heavy barrier doping and thick barrier thickness gives rise to the highest $\tilde{S}^2\tilde{\sigma}$.

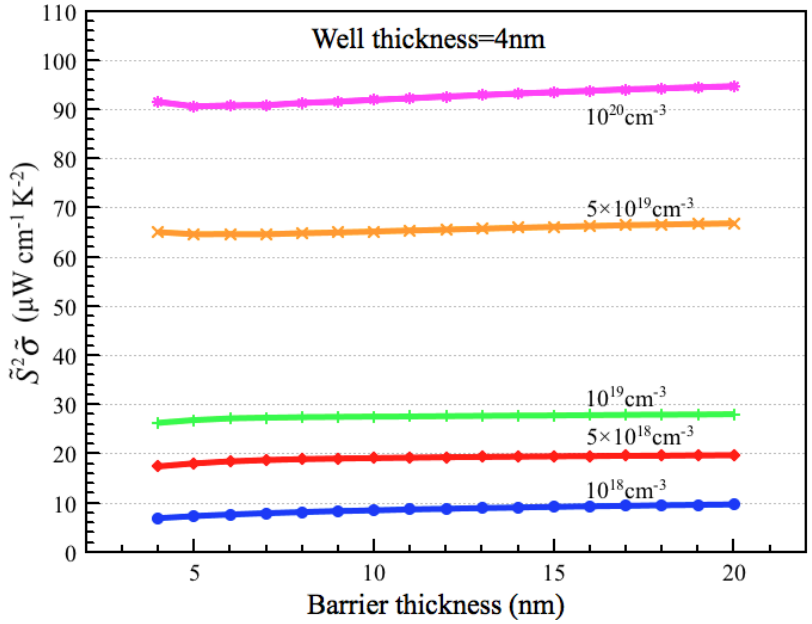

Figure 31. Calculated $\tilde{S}^2\tilde{\sigma}$ as a function of barrier witdth (t_B) and doping (p_B) at QW thickness of 4 nm

4.3 Simulation of Both P- and *N*-Type Silicon/Silicon-Germanium Quantum Well At Different Germanium Ratio

TE modules consist of both *n*- and *p*-type thermal pellets. So far, all the simulation results and analysis were focused on *p*-type Si/$Si_{0.8}Ge_{0.2}$/Si QW structures. The *n*-type $Si_{0.8}Ge_{0.2}$/Si/$Si_{0.8}Ge_{0.2}$ QW simulation structures were took away from the optimized *p*-type counterparts with barrier/well thickness combination (20nm/4nm). In addition to mere 20% Ge ratio investigation, 40% Ge ratio *p*-type Si/$Si_{0.6}Ge_{0.4}$/Si and *n*-type $Si_{0.6}Ge_{0.4}$/Si/$Si_{0.6}Ge_{0.4}$ QW structures were also included, as summarized in table 3.

Table 3. Simulations of *p*- and *n*-type QW (t_W=4nm, t_B=20nm) at room temperature

QW thickness t_W (nm)	QW doping (cm^{-3})	Barrier thickness t_B (nm)	Barrier type	Ge ratio (%)	Barrier doping (cm^{-3})				
4	10^{14}	20	*p*-type	20	10^{18}	5×10^{18}	10^{19}	5×10^{19}	10^{20}
				40					
			n-type	20					
				40					

Figure 32 shows $\tilde{S}$ versus barrier concentration for *n*-type $Si_{0.8}Ge_{0.2}/Si/Si_{0.8}Ge_{0.2}$ (blue), *n*-type $Si_{0.6}Ge_{0.4}/Si/Si_{0.6}Ge_{0.4}$ (red), *p*-type $Si/Si_{0.8}Ge_{0.2}/Si$ (green), *p*-type $Si/Si_{0.6}Ge_{0.4}/Si$ (pink) QW structures with well and barrier thickness of 4 nm and 20 nm, respectively. As we know that $\tilde{S}$ is inversely proportional to doping concentration, $\tilde{S}$ decreases as barrier concentration increases.

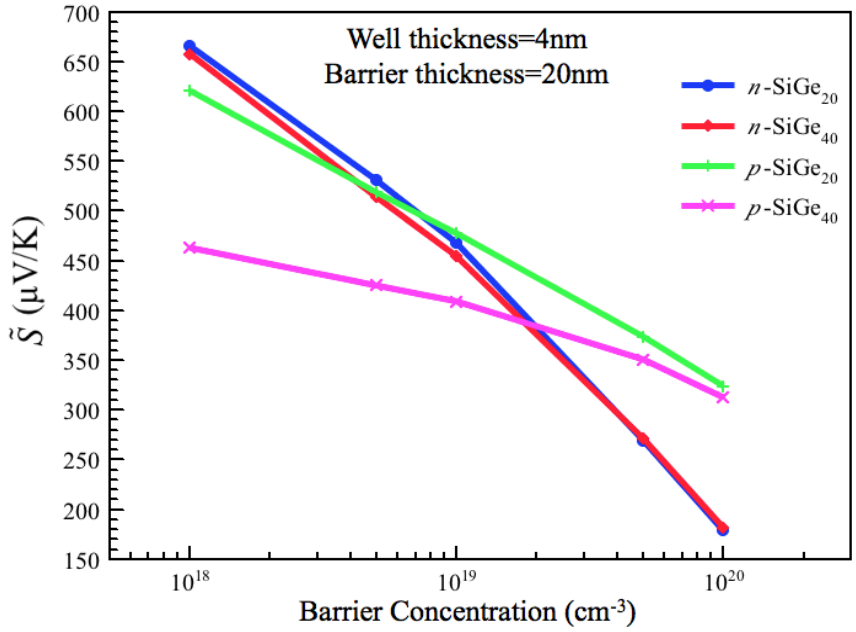

Figure 32. $\tilde{S}$ versus p_B for *n*-type $SiGe_{0.2}/Si/SiGe_{0.2}$ (blue) and $SiGe_{0.4}/Si/SiGe_{0.4}$ (red), *p*-type $Si/SiGe_{0.2}/Si$ (green) and $Si/SiGe_{0.4}/Si$ (pink) QW structures with well and barrier thickness of 4nm and 20nm

In figure 33, $\tilde{\sigma}$ versus barrier concentration for *n*-type $Si_{0.8}Ge_{0.2}$ /Si/$Si_{0.8}Ge_{0.2}$ (blue), *n*-type $SiGe_{0.4}$/Si/$SiGe_{0.4}$ (red), *p*-type Si/$Si_{0.8}Ge_{0.2}$/Si (green), *p*-type Si/$SiGe_{0.4}$/Si (pink) with well and barrier thickness of 4nm and 20nm, were shown respectively. $\tilde{\sigma}$ increases as barrier concentration increase and $\tilde{\sigma}$ of *n*-type QW are larger than *p*-type counterpart due higher electron mobility. If $Si_{0.6}Ge_{0.4}$ was used instead of $Si_{0.8}Ge_{0.2}$, which indicates that *n*-type QW has Ge increase in barrier layers while *p*-type QW has Ge increase in the quantum well, greater electron confinement in *n*-type Si QW and greater hole confinement in the *p*-type $Si_{0.6}Ge_{0.4}$ QW as a result of increased discontinuities of conduction band and valance band according to figure 11 and 12, respectively. For bulk material as Ge ratio increase from 20% to 40%, according to figure 24, both electron and hole mobility decrease slightly.

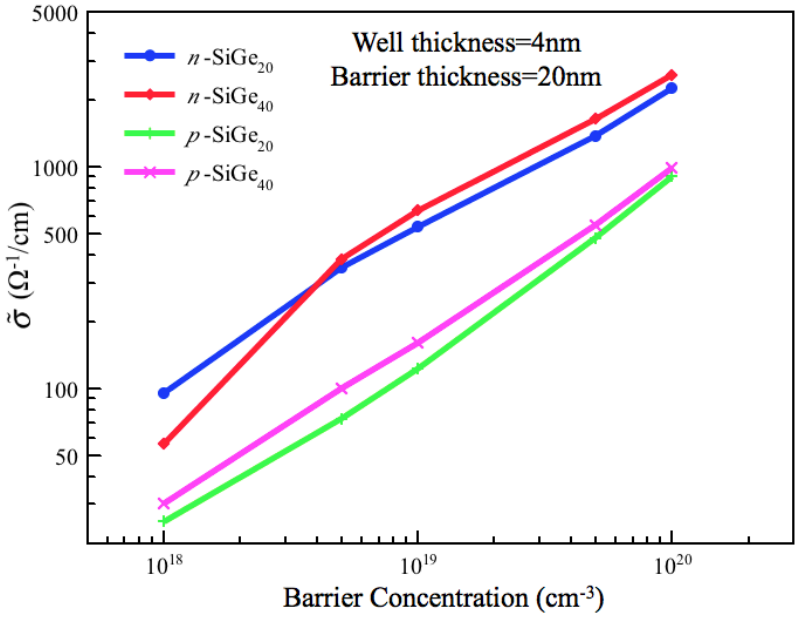

Figure 33. $\tilde{\sigma}$ versus barrier concentration for *n*-type $Si_{0.8}Ge_{0.2}$/Si/$Si_{0.8}Ge_{0.2}$ (blue), *n*-type $Si_{0.6}Ge_{0.4}$/Si/$Si_{0.6}Ge_{0.4}$ (red), *p*-type Si/$Si_{0.8}Ge_{0.2}$/Si (green), *p*-type Si/$Si_{0.6}Ge_{0.4}$/Si (pink) QW structures with well and barrier thickness of 4nm and 20nm

ZT at 300K of different QW structures versus barrier concentration were roughly calculated using thermal conductivity of 20W $m^{-1}K^{-1}$ for Si and SiGe thin films and shown in figure 34. *ZT* of *p*-type bulk Si also shows in figure 34 as the grey dash line at the bottom. For *p*-type $Si/Si_{1-x}Ge_x/Si$ QW, higher Si barrier concentration gives rise to higher *ZT*. At 10^{20} cm^{-3} barrier doping level, it has a *ZT* value 35 times higher than the bulk counterpart. In contrast, for *n*-type $Si_{1-x}Ge_x/Si/Si_{1-x}Ge_x$ QW, maximum *ZT* value is achieved at barrier concentration of 10^{19} cm^{-3}, which leads to *ZT* value 75 times higher than that of bulk Si. For *p*-type QW structure, as Ge ratio of quantum well increase from 20% to 40%, there is no significant influence on *ZT*. However, for *n*-type QW structure, *ZT* was increased as Ge ratio of barrier well increase from 20% to 40% mainly due to the increased $\tilde{\sigma}$ resulting from enhanced electron confinement in the intrinsic high electron mobility quantum well.

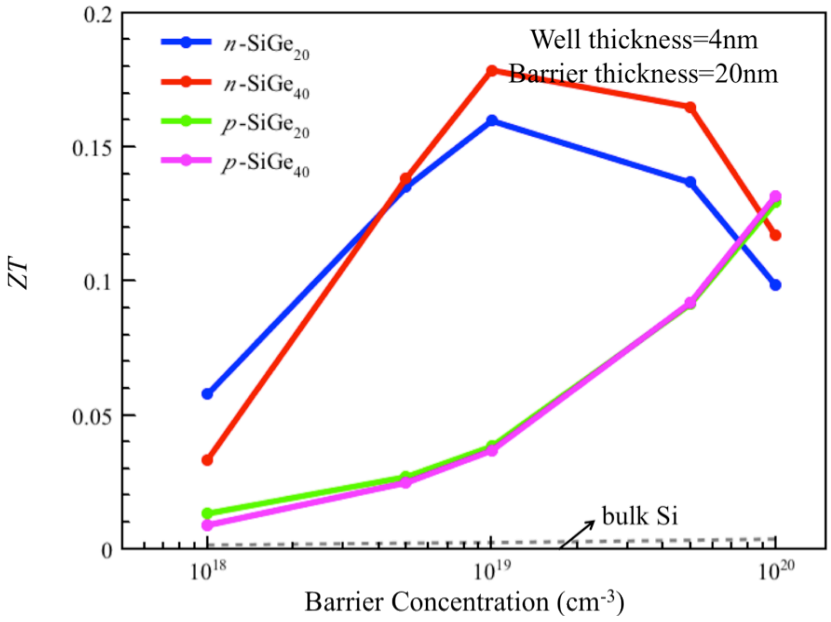

Figure 34. Calculated *ZT* at 300K versus barrier concentration for *n*-type $Si_{0.8}Ge_{0.2}/Si/Si_{0.8}Ge_{0.2}$ (blue), *n*-type $Si_{0.6}Ge_{0.4}/Si/Si_{0.6}Ge_{0.4}$ (red), *p*-type $Si/Si_{0.8}Ge_{0.2}/Si$ (green), *p*-type $Si/Si_{0.6}Ge_{0.4}/Si$ (pink) QW structures with well and barrier thickness of 4nm and 20nm. For better comparison purpose, *ZT* of *p*-type Si alloy was also included as the grey dash line at the bottom

In this chapter, a series of Seebeck simulations at 300K were conducted in the effort to better understand the influence of each variable and then obtain optimized thickness of quantum well and barrier as well as barrier concentration and Ge ratio. *P*-type QW structure simulations were discussed comprehensively and the outcome from *p*-type simulations were transferred to *n*-type counterparts.

Based on *p*-type simulation results, 4 nm quantum well thickness and 20 nm barrier thickness was chosen to be the best combination. Additionally, it was found that for *p*-type Si/ $Si_{1-x}Ge_x$/Si QW, high Si barrier concentration (10^{20} cm^{-3}) gives rise to higher *ZT*; although for *n*-type $Si_{1-x}Ge_x/Si/Si_{1-x}Ge_x$ QW, maximum *ZT* value is achieved at barrier concentration of 10^{19} cm^{-3}. Moreover, increased Ge ratio had less impact on *p*-type than *n*-type quantum well structures.

CHAPTER 5

TEMPERATURE DEPENDENT THERMOELECTRICS

Usually, thermoelectric generators (TEG) operate at elevated temperatures to achieve higher efficiency. In this research, Si/SiGe superlattice films are intended to be grown on SiOG substrate, which has a temperature limit of 900K. Previous simulations and discussions in Chapter 4 considered at room temperature (300K) conditions. In this chapter thermoelectric behavior over the temperature range from 300 to 900K will be presented and discussed. The simulation temperature specifically refers to the average temperature of the thermoelectric material with a 10K temperature difference. Important temperature dependent parameters of semiconductors will be considered first, followed by temperature dependent simulated results of Si/SiGe superlattice.

5.1 TEMPERATURE DEPENDENCE PARAMETERS OF SILICON AND SILICON-GERMANIUM

5.1.1 ENERGY BANDGAP $E_G(T)$

The temperature dependence of the energy bandgap (E_g) of Si is modeled in ATLAS as follows:

$$\begin{aligned} E_g(T)_{Si} &= E_g(300\text{K})_{Si} - 4.73\times10^{-4}\left(\frac{300^2}{300+636}+\frac{T^2}{T+636}\right) \\ &= 1.17 - 4.73\times10^{-4}\frac{T^2}{T+636} \end{aligned} \tag{5.1}$$

Regarding $Si_{1-x}Ge_x$, the temperature dependence of the energy bandgap (E_g) is calculated as a function of Ge fraction (x) as follows:

$$E_g(T)_{Si_{1-x}Ge_x} = E_g(300\text{K})_{Si_{1-x}Ge_x} + (4.73 + 0.04x) \times 10^{-4} \left[\frac{300^2}{300 + (636 - 401x)} + \frac{T^2}{T + (636 - 401x)} \right] \tag{5.2}$$

where E_g(300K) is the energy bandgap at 300K which equals to 1.12eV and 0.97eV for Si and $Si_{0.8}Ge_{0.2}$, respectively.

In the presence of heavy doping greater than $10^{18}cm^{-3}$, a further decrease in the band separation occurs. The bandgap narrowing effect of Si and $Si_{1-x}Ge_x$ at high doping level is modeled as follows:

$$\Delta E_g = 1 \times 10^{17} \left\{ \ln \frac{n}{9 \times 10^{-3}} + \sqrt{\left(\ln \frac{n}{9 \times 10^{-3}} \right)^2 + 0.5} \right\} \tag{5.3}$$

The simulated energy bandgap for Si (dash lines) and $Si_{0.8}Ge_{0.2}$ (solid lines) as a function of temperature at different doping concentration were overlaid in figure 35. It shows that E_g(300K) of moderately doped Si and $Si_{0.8}Ge_{0.2}$ (two blue curves) equal to 1.12eV and 0.97eV, respectively. The energy bandgap narrowing effect occurs as doping concentration extends beyond $10^{18}cm^{-3}$ in addition to E_g dependence on temperature.

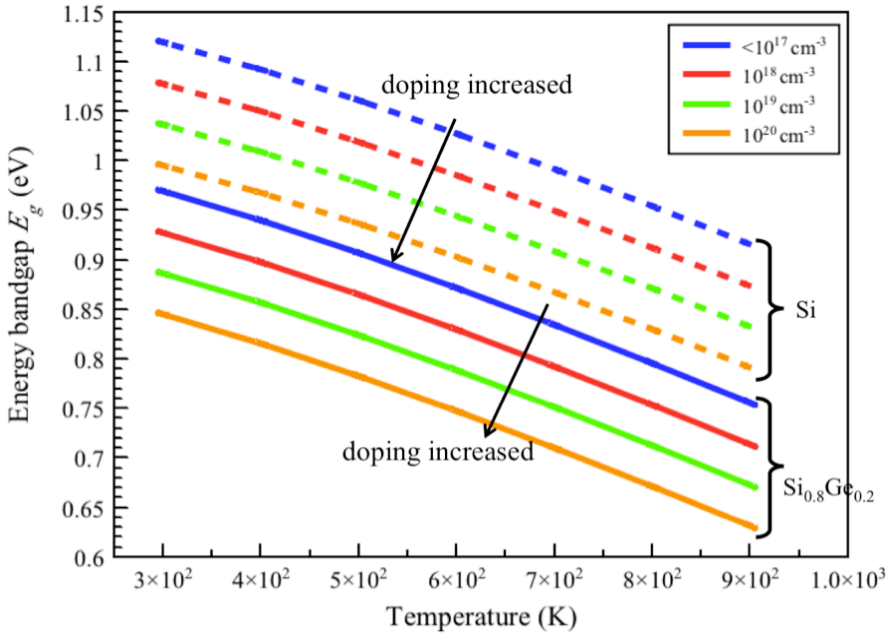

Figure 35. Simulated energy bandgap E_g of Si (dash lines) and $Si_{0.8}Ge_{0.2}$ (solid lines) as a function of temperature at various doping, where bandgap narrows as doping level greater than $10^{18}cm^{-3}$

5.1.2 Intrinsic Carrier Concentration $n_i(T)$

For intrinsic materials, thermal agitation excites electrons into conduction band leaving equal number of holes in valence band, where $n_i=n=p$. For non-degenerate semiconductor at moderate temperature, the product of majority and minority carrier concentration is fixed to be the square of intrinsic carrier concentration, which is best known as the mass-action law as:

$$n_i = \sqrt{np} = \sqrt{N_C N_V}\exp\left(\frac{-E_g}{2k_B T}\right) \tag{5.4}$$

For heavily doped material, the effective intrinsic carrier concentration is calculated taking the bandgap narrowing effect (ΔE_g) into account:

$$n_{ie}^2 = n_i^2 \exp\left(\frac{\Delta E_g}{k_B T}\right) \tag{5.5}$$

In figure 36, the simulated (dash lines) and reported (solid lines) intrinsic carrier concentration (n_i) versus 1000/T for Si and $Si_{1-x}Ge_x$ alloys is superimposed. At 300K, $n_i(Si) = 1.08\times10^{10}$ cm^{-3} and $n_i(Si_{0.8}Ge_{0.2}) \approx 6.8\times10^{10}$ cm^{-3}. Good agreements were obtained between simulated and reported data [28].

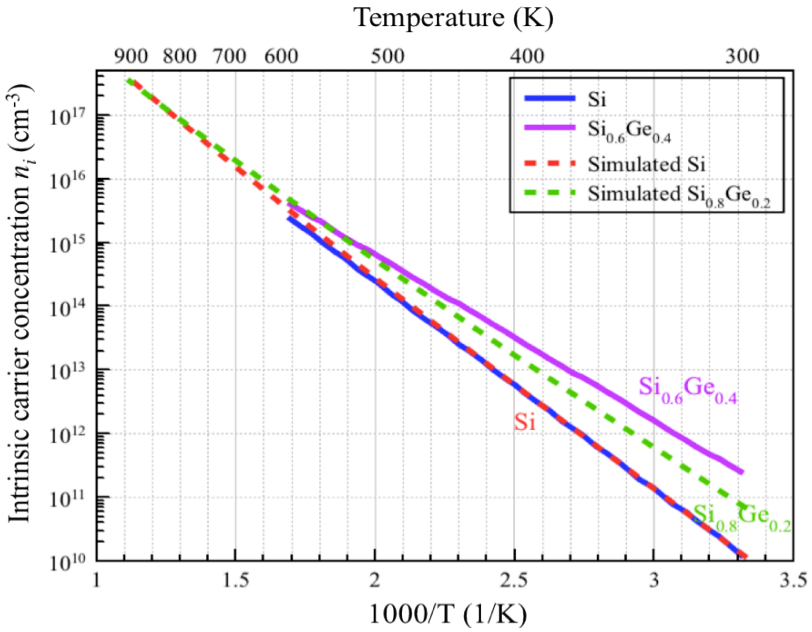

Figure 36. Temperature dependence of n_i(T) for bulk Si and $Si_{1-x}Ge_x$ alloy versus 1000/T. The reported data (solid lines) of Si and $Si_{0.6}Ge_{0.4}$ were taken from [28]

In the intrinsic temperature region, where temperature is high enough such that intrinsic carrier concentration (n_i) outweighs the net impurity concentration (n_i(T)>>|N_A - N_D|), the concentration of both electron and hole is governed by n_i(T) instead of doping concentration, and is given as:

$$n = p = n_i(T) \tag{5.6}$$

At extrinsic temperature range such that temperature is low enough to assure that $n_i(T) << |N_A - N_D|$ but high enough to exceed the carrier freeze-out range, the neutrality condition under complete ionization assumption is expressed as:

For a *p*-type semiconductor where $N_A > N_D$:

$$p_{p0} = (N_A - N_D) + n_{p0} \approx N_A \tag{5.7}$$

$$n_{p0} = \frac{n_i^2}{p_{p0}} \approx \frac{n_i^2}{N_A} \tag{5.8}$$

For a *n*-type semiconductor where $N_D > N_A$:

$$n_{n0} = (N_D - N_A) + p_{n0} \approx N_D \tag{5.9}$$

$$p_{n0} = \frac{n_i^2}{n_{n0}} \approx \frac{n_i^2}{N_D} \tag{5.10}$$

As we can observe from figure 36, n_i has an increase of approximately seven orders of magnitude as temperature increases from 300K to 900K, which in turn has a significant impact on carrier concentration and σ as well. While the effective density of states (N_C, N_V) and E_g are functions of temperature, n_i is much more sensitivity due to the Boltzmann term resulting in an exponential relationship with 1/T.

In semiconductors under extrinsic conditions, the free carrier concentration is not dominated by the temperature; rather it is controlled by the electrically active doping concentration. A temperature gradient does not change the majority concentration unless the intrinsic carrier concentration approaches the doping concentration. Assuming that the temperature remains below this level, a carrier concentration gradient is not established and therefore carrier diffusion is not significant.

A temperature change across a semiconductor slab (hot/cold side) will however create a difference in the energy of associated carriers, and establish a thermal voltage across the sample. Carriers will travel from the hot side to the cold side in order to move toward a state of thermal equilibrium, as illustrated in figure 37. Considering a *p*-type semiconductor; there is a drift current of hole carriers across the device with a continuous supply of hole carriers provided by the thermal energy and vice verse for a *n*-type material. The situation presents a "built-in" voltage that depends upon the temperature difference and the semiconductor type and doping concentration.

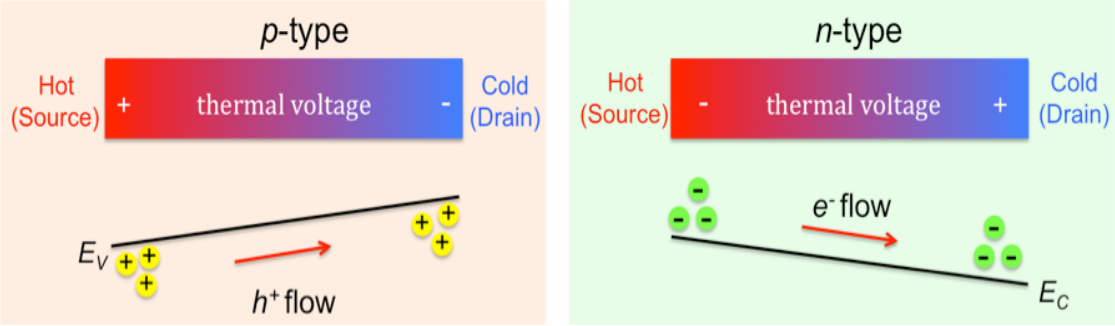

Figure 37. In semiconductors under extrinsic conditions, a temperature change across a semiconductor slab (hot/cold side) will however create a difference in the energy of associated carriers, and establish a thermal voltage across the sample. Carriers will travel from the hot side to the cold side in order to move toward a state of thermal equilibrium

This "built-in" voltage is analogous to a *pn* junction built-in voltage, which is an established potential difference that cannot be directly measured using a voltmeter. However, Silvaco ATLAS can provide a theoretical probe to monitor the potential difference between the hot side (source) and the cold side (drain). This potential difference is the superposition of the thermal voltage and the voltage appearing at the drain terminal in response to the ability to source current through an attached load

resistance. The load resistance can vary from zero (short circuit condition) to infinity (open circuit condition). Under a short circuit condition, the external applied source-drain voltage is zero. An external voltage that works against the thermal voltage is not established, and the net current is maximized as well as the built-in potential difference across the slab. Under an open circuit condition, the external applied (or established) drain-source voltage cancels the thermal voltage, resulting in a net current of zero. This open-circuit voltage (V_{OC}) is referred to as the Seebeck voltage, which is the maximum voltage presented to drive an external load. As the external load resistance changes from zero to a high value, the external voltage changes from zero to a maximum V_{OC}. Figure 38 illustrates *p*-type semiconductor slab is attached with load resistance (R_L) and the valence band energy (E_V) change as a function of R_L from zero (short circuit condition) to infinity (open circuit condition). The Seebeck voltage is this open-circuit voltage, which is consistent with the extraction method discussed in chapter 3.

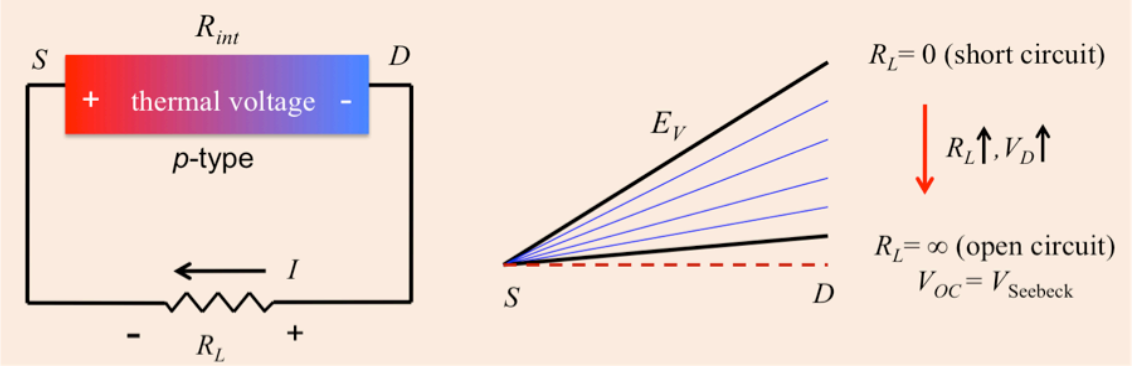

Figure 38. *p*-type semiconductor slab is attached with load resistance (R_L) and the valence band energy (E_V) change as a function of R_L from zero (short circuit condition) to infinity (open circuit condition).

5.1.3 CARRIER MOBILITY $\mu(T)$

The ARORA model for doping and temperature dependent mobility in ATLAS was implemented, which for electrons and holes has the form of:

$$\mu_n = \mu_{1n}\left(\frac{T}{300}\right)^{\alpha_n} + \frac{\mu_{2n}\left(\frac{T}{300}\right)^{\beta_n}}{1+\frac{N}{N_{CRITn}\left(\frac{T}{300}\right)^{\gamma_n}}} \tag{5.11}$$

$$\mu_p = \mu_{1p}\left(\frac{T}{300}\right)^{\alpha_p} + \frac{\mu_{2p}\left(\frac{T}{300}\right)^{\beta_p}}{1+\frac{N}{N_{CRITp}\left(\frac{T}{300}\right)^{\gamma_p}}} \tag{5.12}$$

where N is the total local dopant concentration, and μ_1, μ_2, α, β, γ, N_{CRIT} are user specifiable parameters; the default values of them were used and can be found in ALTAS users manual [15]. These default ARORA parameters are only valid for Si; however, no specific mobility model parameters exist for SiGe. Therefore, the mobility of lightly doped $Si_{1-x}Ge_x$ alloy at 300K was extracted from figure 23, and shares the same temperature and doping concentration dependence model with Si described in equations (5.11) and (5.12). In general, as temperature and doping concentration increase both electron and hole mobility decrease, which results in a reduction of σ.

5.1.4 SEEBECK COEFFICIENT $S(T)$

In the extrinsic temperature range, a rise in temperature causes the Fermi level (E_f) to move closer to intrinsic level (E_i) and the energy differences (E_C -E_f) or (E_f -E_V) enlarges, which gives rise to the increment of diffusive Seebeck coefficient component S_d (T) according to equation (3.12) and (3.13). The total Seebeck coefficient is dominated by diffusive Seebeck coefficient S_d (T) component and consequently improves as the temperature increases. However as temperature increases up to the intrinsic temperature region, electron concentration equates to hole concentration, both of which are governed by intrinsic carrier concentration (n=p=n_i). Therefore, there is equal amount of opposite charge diffusing along the thermal gradient. The electron and hole contributions to thermal current counteract, which result in diminished Seebeck coefficient.

Figure 39 shows the simulated Seebeck coefficient (S) of bulk p- and n-type Si over the temperature range (from 300K to 900K) over a set of doping concentration (from 10^{14} to 10^{20} cm^{-3}). For lightly and moderate doped Si, initially the absolute value of Seebeck coefficient increases as temperature increase and then starts to decrease when $n_i(T)$ outweighs the doping concentration. For pure (10^{14} and $10^{15}cm^{-3}$) p-type Si, S becomes even negative at temperature between 500K and 700K. For heavily doped Si (10^{19} and 10^{20} cm^{-3}), the absolute Seebeck coefficient increases monotonously as temperature elevates up to 900K, where n_i(900k) still remains orders of magnitude smaller than doping concentration according to figure 36. Therefore, heavily doped material is less susceptible to performance degradation at high temperature.

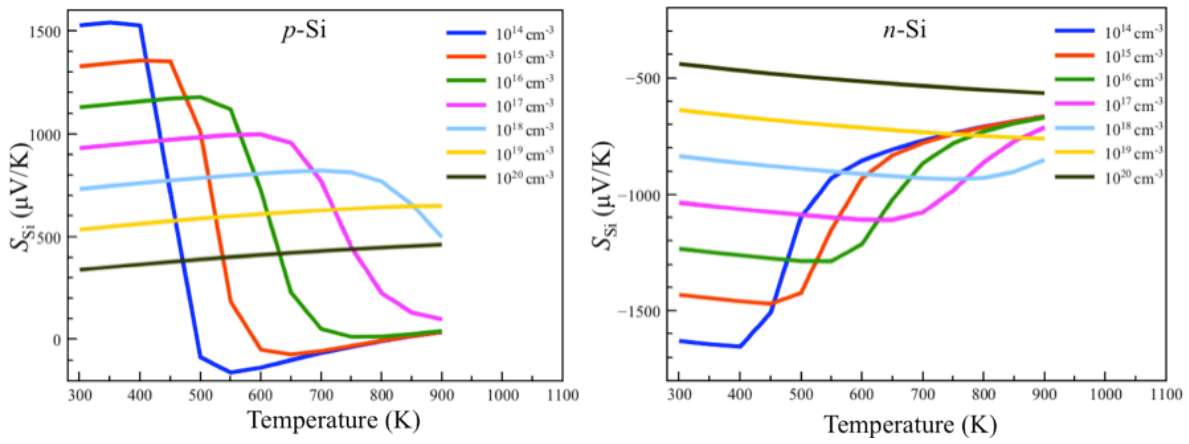

Figure 39. Simulated *S* of bulk *p*- and *n*-type Si versus temperature (from 300K to 900K) at doping level from 10^{14} to 10^{20} cm^{-3}.

The simulated bulk *S* of *p*- and *n*-type $Si_{0.8}Ge_{0.2}$ alloy ranging from 300K to 900K over a set of doping concentration from 10^{14} to 10^{20}cm^{-3} were plotted in figure 40.

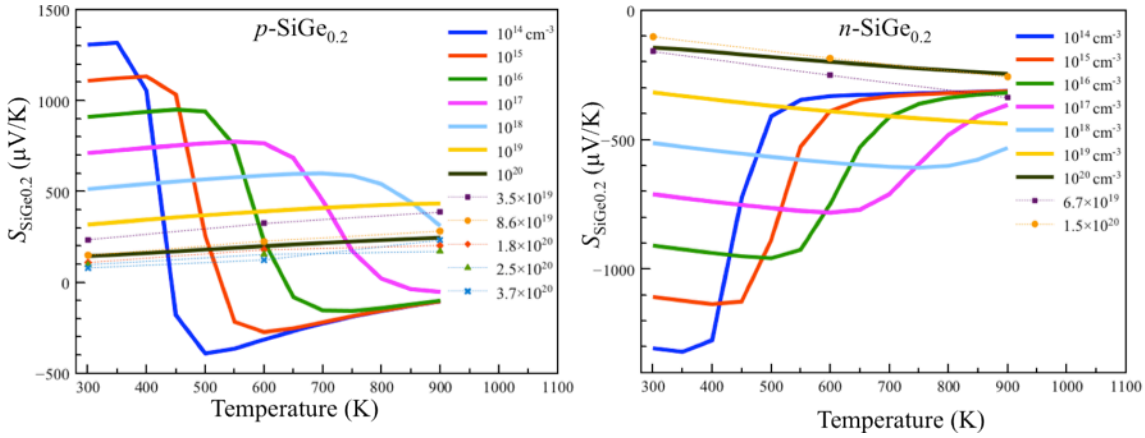

Figure 40. Simulated (solid curves) and experimental (scattered dots) *S* of bulk *p*- and *n*-type $Si_{0.8}Ge_{0.2}$ versus temperature ranging from 300K to 900K at doping level from 10^{14} to 10^{20} cm^{-3} [27].

Experimental *S* data (scattered dots) of heavily doped $Si_{0.8}Ge_{0.2}$ at 300K, 600K and 900K from [27] are overlaid with simulated data in figure 40, where a good match between experimental and simulation results are observed. |*S*| of both bulk *p*-and *n*-type $Si_{0.8}Ge_{0.2}$ follow the same trend with temperature at certain doping level, although, with smaller absolute values than the bulk Si counterparts.

5.2 QW THERMOELECTRICS SIMULATIONS AT ELEVATED TEMPERATURE

Based on the room temperature quantum simulation results from Chapter 4, the investigation on temperature dependence was continued and the simulation plan for *p*-type $Si/Si_{0.8}Ge_{0.2}/Si$ was summarized in table 4. QW thickness was maintained at 4nm thickness and barrier doping ranged from 10^{18} to 10^{20} cm^{-3}. Regarding barrier thickness, both 4nm (dash curves) and 20nm (solid curves) are used and discussed in the temperature range from 300K to 900K in order to better understand the influence of barrier thickness at elevated temperature.

Table 4. Simulations of *p*-type $Si/Si_{0.8}Ge_{0.2}/Si$ QW as temperature ranging from 300K to 900K.

Constant		**Variable**							
QW thickness t_W (nm)	QW doping (cm^{-3})	Barrier doping (cm^{-3})	Barrier thickness t_B (nm)		Temperature (K)				
4	10^{14}	10^{18} 5×10^{18} 10^{19} 5×10^{19} 10^{20}	4	20	300	350	…	850	900

The total integrated hole concentration cross the entire of *p*-type $Si/Si_{0.8}Ge_{0.2}/Si$ film stack ($\tilde{p}$) versus temperature with t_W of 4nm and t_B of 4nm (dash lines) and 20nm (solid lines) at different barrier concentration are shown in figure 41. At temperature near 800K, n_i of silicon starts to exceed $10^{17}\,cm^{-3}$; therefore $\tilde{p}$ of $10^{18}\,cm^{-3}$ Si barrier concentration has an increase which is influenced by n_i(T).

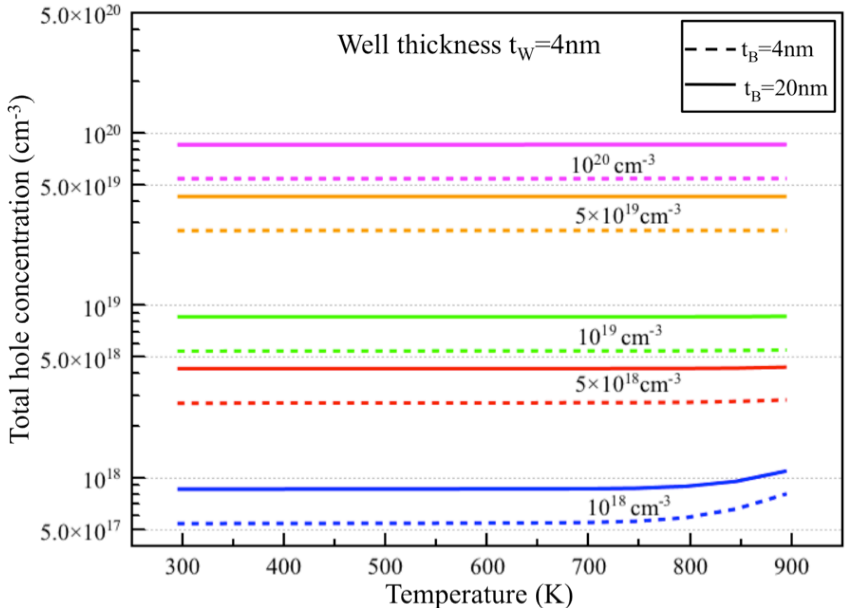

Figure 41. Total integrated hole concentration cross the entire of *p*-type $Si/Si_{0.8}Ge_{0.2}/Si$ film stack ($\tilde{p}$) versus temperature with t_W of 4nm and t_B of 4nm (dash lines) and 20nm (solid lines) at different barrier concentration of 10^{18}, 5×10^{18}, 10^{19}, 5×10^{19} and $10^{20}cm^{-3}$.

The integrated hole concentration inside the center QW ($\tilde{p}'$) of *p*-type $Si/SiGe_{0.2}/Si$ versus temperature with t_W of 4nm and t_B of 4 (dash lines) and 20nm (solid lines) at different barrier concentration were shown in figure 42. At elevated temperature, $\tilde{p}'$ decreases since that the carriers in quantum well gain extra thermal energy to overcome the potential barrier reducing quantum confinement. The increment of $\tilde{p}'$ of

10^{18} cm^{-3} barrier concentration at temperature greater than 800K was due to the increase of $\tilde{p}$ in the intrinsic temperature region.

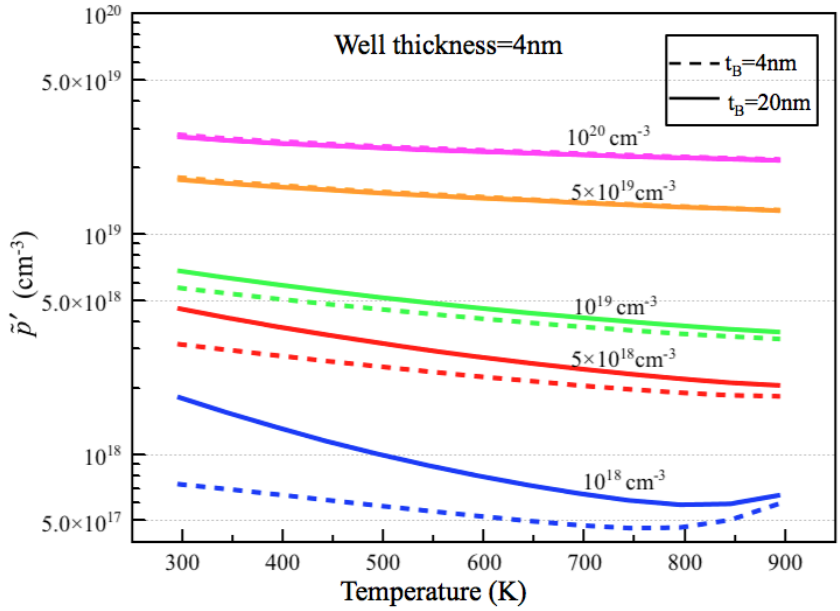

Figure 42. The integrated hole concentration in the center QW ($\tilde{p}'$) of *p*-type Si/ $Si_{0.8}Ge_{0.2}$/Si versus temperature with t_W of 4nm and t_B of 4nm (dash lines) and 20nm (solid lines) at different barrier concentration of 10^{18}, 5×10^{18}, 10^{19}, 5×10^{19} and $10^{20}$$cm^{-3}$.

The effective electrical conductivity ($\tilde{\sigma}$) of the entire *p*-type Si/$Si_{0.8}Ge_{0.2}$/Si film stacks versus temperature with t_W of 4nm and t_B of 4 and 20nm at different barrier concentration are plotted in figure 43. The $\tilde{\sigma}$ decrease stems from the reduced carrier mobility at elevated temperature.

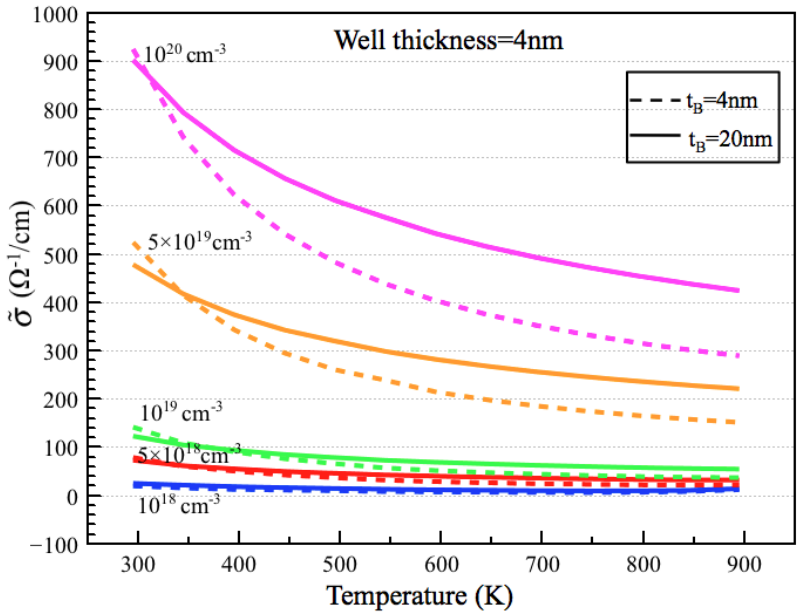

Figure 43. The effective electrical conductivity ($\tilde{\sigma}$) of *p*-type Si/ $Si_{0.8}Ge_{0.2}$/Si versus temperature with t_W of 4nm and t_B of 4 nm (dash lines) and 20nm (solid lines) at different barrier concentration of 10^{18}, 5×10^{18}, 10^{19}, 5×10^{19} and 10^{20} cm^{-3}.

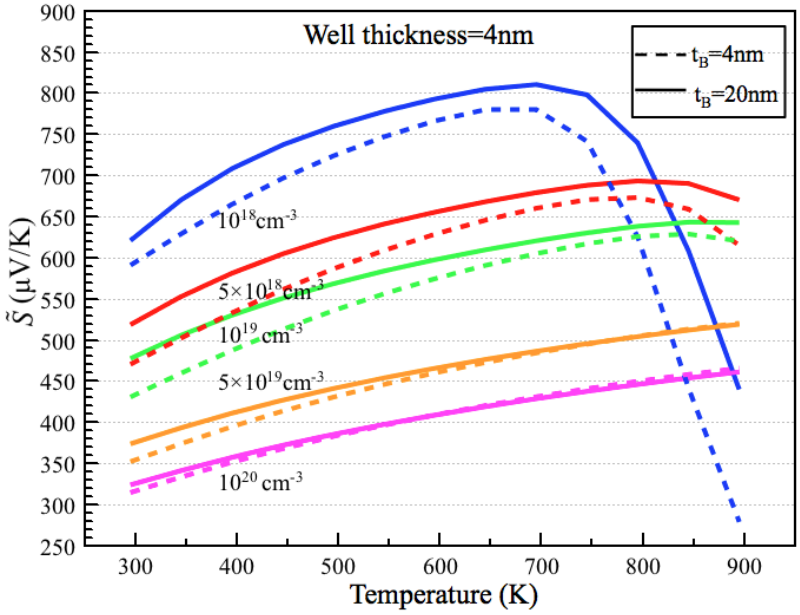

Figure 44. The effective Seebeck coefficient ($\tilde{S}$) of *p*-type Si/$Si_{0.8}Ge_{0.2}$/Si versus temperature with t_W of 4 nm and t_B of 4 nm (dash lines) and 20nm (solid lines) at different barrier concentration of 10^{18}, 5×10^{18}, 10^{19}, 5×10^{19} and 10^{20} cm^{-3}.

The effective Seebeck coefficient of the entire film stacks ($\tilde{S}$) versus temperature with t_W of 4 nm and t_B of 4 and 20 nm at different barrier concentration are plotted in figure 44. As expected from previous bulk simulations, as temperature increases from 300K to 900K, $\tilde{S}$ increases monotonously for heavily doped Si/SiGe material (greater than 10^{19} cm^{-3}); however, for lightly or moderate doping level (<$10^{19}$$cm^{-3}$), $\tilde{S}$ increases initially and then decrease as temperature continues to elevate.

As shown in figure 45, it was concluded that, for *p*-type $Si/Si_{0.8}Ge_{0.2}/Si$ QW structure, 4nm well thickness, 20nm barrier thickness with barrier doping concentration of 10^{20} cm^{-3} gives rise to the maximum $\tilde{S}^2\tilde{\sigma}$ over the entire temperature range of 300K to 900K. Moreover, the 20nm barrier thickness yields higher $\tilde{S}^2\tilde{\sigma}$ consistently compared to 4 nm barrier thickness.

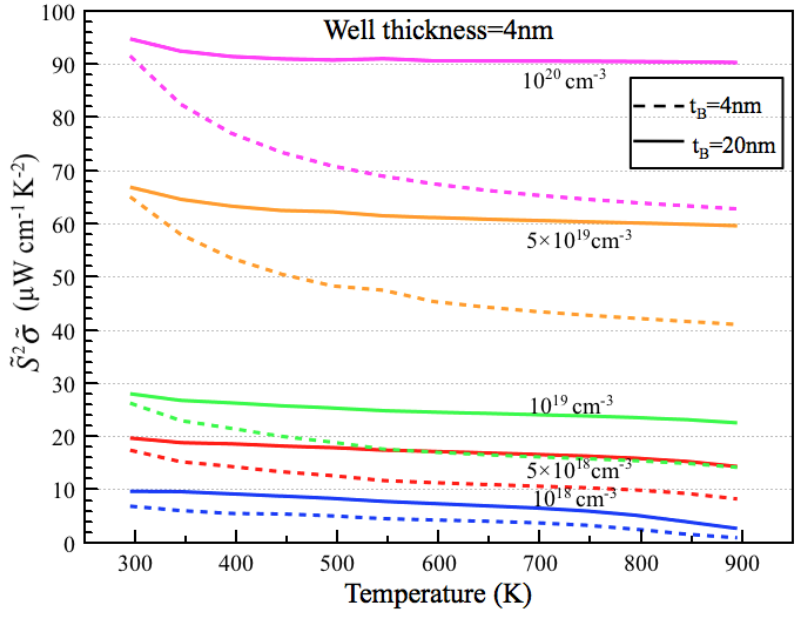

Figure 45. The thermal power ($\tilde{S}^2\tilde{\sigma}$) of *p*-type $Si/Si_{0.8}Ge_{0.2}/Si$ versus temperature with t_W of 4nm and t_B of 4nm (dash lines) and 20nm (solid lines) at different barrier concentration of 10^{18}, 5×10^{18}, 10^{19}, 5×10^{19} and $10^{20}$$cm^{-3}$.

Additionally, *n*-type 20nm $Si_{0.8}Ge_{0.2}$/4nm Si/20nm $Si_{0.8}Ge_{0.2}$ QW structures with barrier thickness from 10^{18} to $10^{20}cm^{-3}$ were simulated at temperature range from 300K to 900K. Corresponding electrical conductivity ($\tilde{\sigma}$), Seebeck coefficient ($\tilde{S}$) and thermal power ($\tilde{S}^2\tilde{\sigma}$) are shown in figure 46, 47 and 48, respectively. Similar to *p*-type 20nm Si/4nm $Si_{0.8}Ge_{0.2}$/20nm Si QW structures, $\tilde{\sigma}$ decrease as temperature increase and barrier concentration decrease; the absolute value of $\tilde{S}$ increase as temperature increase until $n_i(T)$ exceeds the doping level; and heavily doped barrier had less variation of $\tilde{S}^2\tilde{\sigma}$ across 300K to 900K temperature range. The highest overall $\tilde{S}^2\tilde{\sigma}$ was achieved with 5×10^{19} and 10^{20} cm^{-3} barrier concentration in the temperature region from 300K to 900K. Figure 48 shows that for a particular temperature range, different values of barrier doping concentration should be considered.

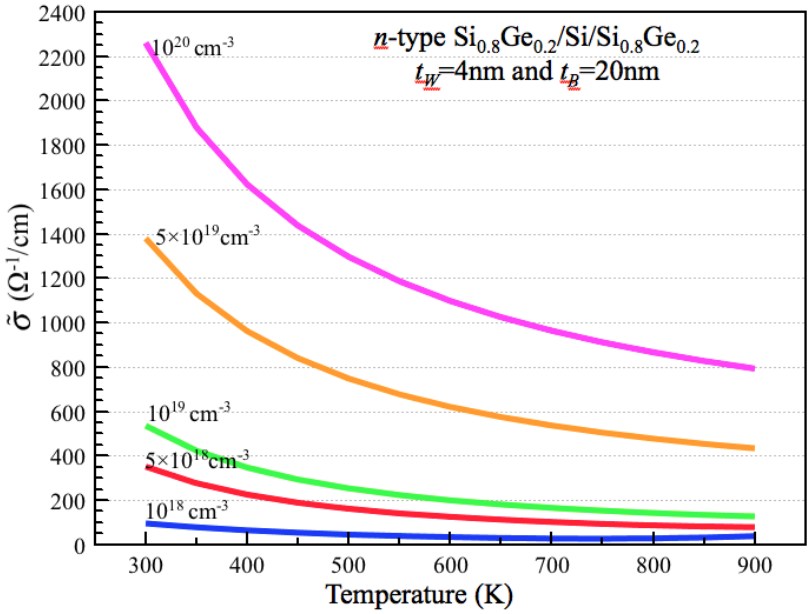

Figure 46. $\tilde{\sigma}$ of *n*-type $Si_{0.8}Ge_{0.2}$/Si/$Si_{0.8}Ge_{0.2}$ versus temperature with t_W of 4nm and t_B of 4nm (dash lines) and 20nm (solid lines) at different barrier concentration of 10^{18}, 5×10^{18}, 10^{19}, 5×10^{19} and $10^{20}cm^{-3}$

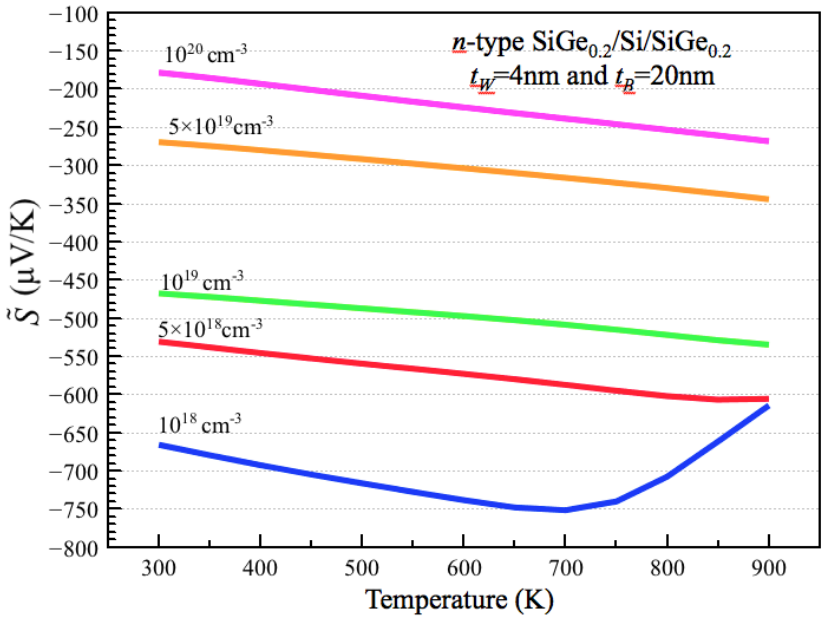

Figure 47. $\tilde{S}$ of *n*-type $Si_{0.8}Ge_{0.2}/Si/Si_{0.8}Ge_{0.2}$ versus temperature with t_W of 4nm and t_B of 4nm (dash lines) and 20 nm (solid lines) at different barrier concentration of 10^{18}, 5×10^{18}, 10^{19}, 5×10^{19} and 10^{20} cm^{-3}

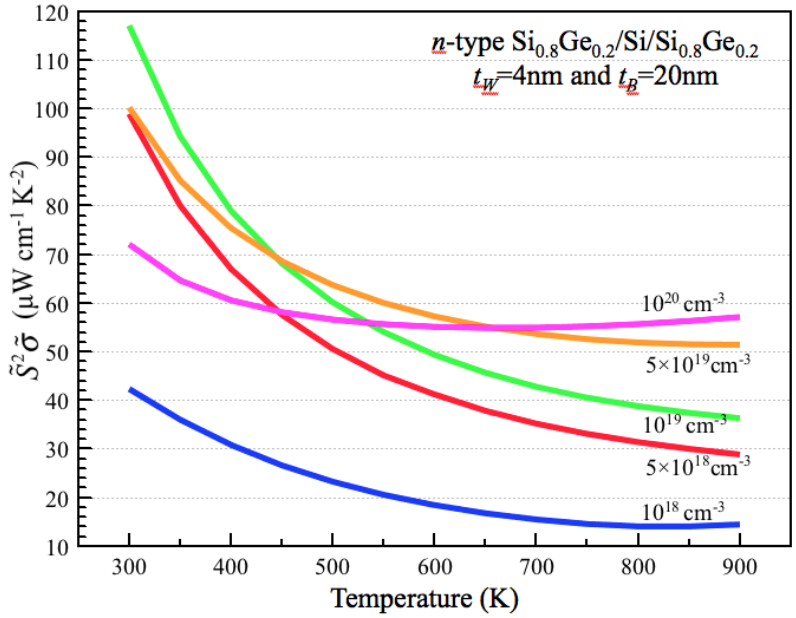

Figure 48. The thermal power ($\tilde{S}^2\tilde{\sigma}$) of *n*-type $Si_{0.8}Ge_{0.2}/Si/Si_{0.8}Ge_{0.2}$ versus temperature with t_W of 4nm and t_B of 4nm (dash lines) and 20nm (solid lines) at different barrier concentration of 10^{18}, 5×10^{18}, 10^{19}, 5×10^{19} and $10^{20}cm^{-3}$

TEG for waste heat recovery application usually operates at elevated temperature with 300-500K temperature differences between cold and hot sides. In this chapter, temperature dependent material parameters of great importance used in simulations were discussed, among which n_i has the strongest temperature dependence. In the intrinsic temperature range, the concentration of $n_i(T)$ instead of dopant determines the carrier concentration ($n_i=n=p$) and consequently $S(T)$ also diminishes due to electrons and holes diffusion current cancellation.

Next, various QW structures at temperature ranging from 300-900K were evaluated and discussed. It was found that for *p*-type 20nm Si/4nm $Si_{0.8}Ge_{0.2}$/20nm Si QW structure, barrier doping concentration of 10^{20} cm^{-3} gives rise to the maximum $\tilde{S}^2\tilde{\sigma}$ over the entire temperature range of 300K to 900K. For *n*-type 20nm $Si_{0.8}Ge_{0.2}$/4nm Si/20nm $Si_{0.8}Ge_{0.2}$ QW structures, the highest overall $\tilde{S}^2\tilde{\sigma}$ is achieved between 5×10^{19} and 10^{20} cm^{-3} barrier concentration with some crossover in the temperature region from 300K to 900K.

CHAPTER 6

THERMOELECTRIC DEVICE PERFORMANCE

The discussion this far has examined the QW films as stand-alone structures. TEG devices consist of a large number of alternate *n*- and *p*-type thermoelectric elements, which are connected electrically in series by conductors and encapsulated by electrically insulated but high thermally conductive materials, such as ceramic material, as shown in figure 3 in chapter 1. In this chapter, the equivalent circuit of TEG will be first introduced followed by the discussion of system requirements from electrical and thermal aspects. Then, the electrical and thermal parasitic effects from SOI and SiOG substrate will be characterized using a parallel conductor model.

6.1 EQUIVALENT CIRCUIT AND SYSTEM REQUIREMENTS OF TEG

TEG devices consist of alternating *n*- and *p*-type thermoelectric elements, which are connected electrically in series but thermally in parallel in order to obtain higher power output and heat flow. As shown in figure 49 (a), for TEG modules made up with N pairs of alternating *p*- and *n*-type thermal pellets with the length of L, the total thickness of QW layers of t_{QW}, the thickness of SiOG substrate t_S, and the width of pellets of w, the total Seebeck coefficient (S_T), serial electrical resistance (R_{INT}) and open-circuit TE voltage (V_{OCT}) of these N pairs of *p*- and *n*-type thermal elements are given as:

$$R_{INT} = N \cdot \left(\tilde{R}_p + \tilde{R}_n \right) = N \cdot \frac{L}{w \cdot t} \left(\rho_P + \rho_N \right) \tag{6.1}$$

$$S_T = N \cdot \left(\tilde{S}_p + \tilde{S}_n \right) \tag{6.2}$$

$$V_{OCT} = S_T \cdot \Delta T = N \cdot V_{OCP} \tag{6.3}$$

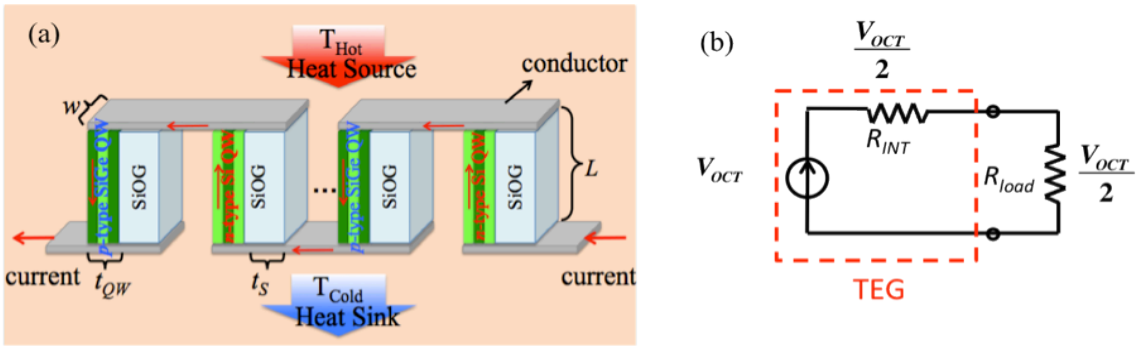

Figure 49. (a) TEG modules made up with N pairs of alternating p- and n-type thermal pellets with the length of L, the total thickness of QW layers of t_{QW}, the thickness of SiOG substrate t_S, and the width of pellets of w (b) equivalent circuit of N pairs of thermal pellets: power source ($N \cdot V'_{OCP}$) with internal resistance (R_{INT}) as shown inside the red box, and maximum power is achieved under resistance matched condition where power source equally divided between internal resistance and load resistance

Assuming negligible thermal resistance at heat sink and ideal ohmic contacts, a TEG of N pairs of thermal elements can be electrically modeled as a power source ($N \cdot V_{OCP} = S_T \cdot \Delta T$, where V_{OCP} denote the open-circuit thermal voltage for one pair of p- and n-type thermal elements) with internal resistance (R_{INT}) as demonstrated inside the red box of figure 49 (b). When the load resistance equals to the internal TEG resistance ($R_{Load} = R_{INT}$), total thermal voltage (V_{OCT}) evenly drops on these resistances and power output

achieves its maximum. The ideal power generation density (p') for N pairs of thermal elements, ignoring the resistance drop of conductors and contact resistance, is given as:

$$P' = \left(\frac{V_{OCT}}{2}\right)^2 \frac{1}{R_{INT} \cdot \left(w \cdot t_{QW}\right)} = \frac{N}{4} \cdot \left(\tilde{S}_p + \tilde{S}_n\right)^2 \cdot \frac{\Delta T^2}{L \cdot \left(\rho_P + \rho_N\right)} \tag{6.4}$$

where $w.t_{QW}$ is the cross-section area of current flow. It is observed from equation (6.4) that power density (p') is enhanced by increased the pair number of *pn* thermal pellets (N) and larger temperature difference between cold and hot sides (ΔT). For quantum structures with fixed quantum well and barrier thickness and doping in the temperature range 300-900K, power generation density (p') can be further improved by optimizing the TE devices length (L) that also determines the maximum contact resistance (R_C) allowed and the minimum heat transfer coefficient (h) needed to assure that the electrical and thermal parasitic losses do not dominate the device performance. Usually less than 10% parasitic losses are desired [30], which means that contact resistance (R_C) and heat transfer coefficient (h) need to satisfy the following constrains:

$$R_C < 0.1\rho L \tag{6.5}$$

$$h > 10\frac{\kappa}{L} \tag{6.6}$$

For fixed well and barrier width, t_{QW} is determined by the number of periods in the superlattice. Based on simulated structures, for 5×10^{19} cm^{-3} barrier doping *n*-type QW, with $\tilde{S}_n$ =-310 μV/K, $\tilde{\sigma}_n$ =575 Ω^{-1}/cm, and for 10^{20} cm^{-3} *p*-type QW $\tilde{S}_p$ =419 μV/K, $\tilde{\sigma}_p$ =516Ω^{-1}/cm. Thin film Si thermal conductivity ($\kappa\approx$20 W $m^{-1}K^{-1}$) [29] was employed for QW film stacks. Assuming cold and hot side temperature at 400K and 900K, power

density, maximum contact resistance (R_C) and minimum heat transfer coefficient (h) for superlattice layers at different device length were calculated and plotted in figure 49 (a) and (b). It can be observed from figure 50 that power density increases as the device becomes shorter, however less contact resistance and more efficient heat sink are demanded. For example, taking a 1cm long device in order to generate 1W/cm^2 power according to criteria in equation (6.5), R_C needs to be less than 10^{-4} Ω-cm^2, which is quite possible; and heat sink needs to have heat transfer coefficient h greater than 3 W/cm^{2}K, otherwise device performance will be significantly degraded. Practically, the requirement on the heat sink is the limiting factor of performance [30].

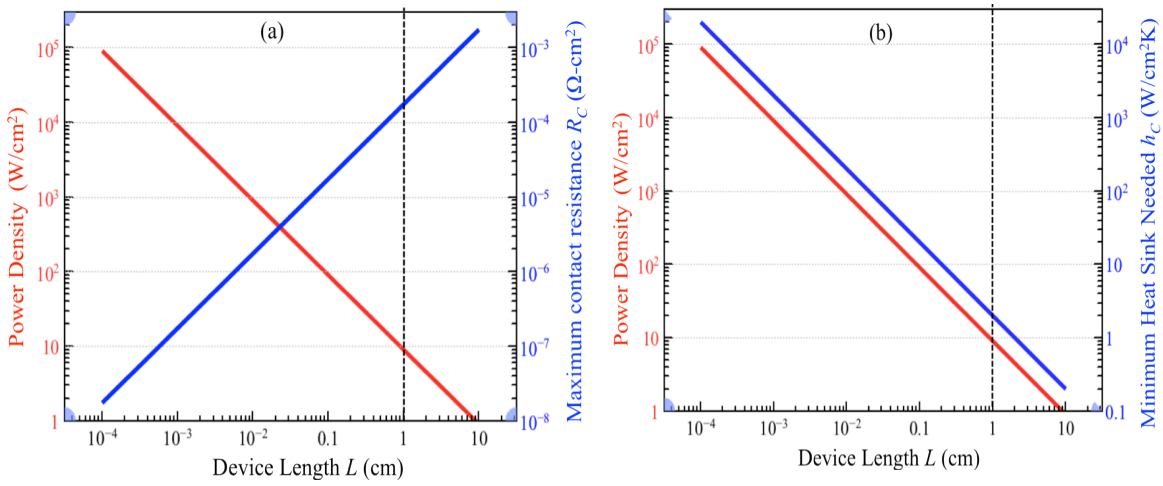

Figure 50. Assuming cold and hot side temperature was at 400K and 900K, the calculated power density, maximum contact resistance (R_C) and minimum heat transfer coefficient (h) using equation (6.4), (6.5) and (6.6) as a function of device length (L) for 5×10^{19} cm^{-3} barrier doping n-type QW with $\tilde{S}_n$=-310μV/K, $\tilde{\sigma}_n$=575Ω^{-1}/cm, and for 10^{20}cm^{-3} p-type QW with $\tilde{S}_p$=419μV/K, $\tilde{\sigma}_p$=516Ω^{-1}/cm and $\kappa\approx$20 W m^{-1}K^{-1}

6.2 PARASITIC EFFECTS FROM SUBSTRATE

6.2.1 ELECTRICAL PARASITIC EFFECT FROM SUBSTRATE

Under DC voltage, no electrical influence was imposed to QW films by SiOG substrate, which has zero S and σ; however, in case of superlattice layers grown on SOI substrate, the total electrical properties are determined by the combination of QW and underlying substrate, which can be considered as a two parallel conductors. Neglecting the interface effects, the total electrical properties taking SOI substrate into account can be modeled as [1]:

$$S_T' = \frac{S_S \sigma_S t_S + \tilde{S}_{QW} \tilde{\sigma}_{QW} t_{QW}}{\sigma_S t_S + \tilde{\sigma}_{QW} t_{QW}} \tag{6.7}$$

$$\sigma_T' = \frac{\sigma_S t_S + \tilde{\sigma}_{QW} t_{QW}}{t_S + t_{QW}} \tag{6.8}$$

$$Z' = \frac{S_T'^2 \sigma_T'}{\kappa_{eT}' + \kappa_{lT}'} \tag{6.9}$$

where the subscripts T, S, QW correspond to the total, substrate and QW film stacks, respectively, and t represents thickness.

The implementation of parallel conductor model requires QW films and underlying substrate to be electrically connected at the edges. Assuming contact metal has negligible S and σ, to better understand the electrical influence from substrate, S_T', σ_T' and Z' were calculated using equations (6.7-6.9) for p-type QW films at room temperature with $\tilde{S}_{QW}$=419 μV/K, $\tilde{\sigma}_{QW}$= 516 Ω^{-1}/cm and $\kappa_{QW} \approx$ 22 W $m^{-1}K^{-1}$. SOI substrate has doping

level ranging from 10^{14} to 10^{20} cm^{-3}. The total electrical conductivity of QW layers and SOI substrate (σ'_T) as a function of substrate to QW electrical conductivity ratio ($\sigma_S/\tilde{\sigma}_{QW}$) at substrate to QW thickness ratio (t_S/t_{QW}) ranging from 1 to 10^4 were plotted in figure 51. The horizontal top and oblique grey dash lines are $\tilde{\sigma}_{QW}$ and σ_S, respectively, and σ'_T is in between $\tilde{\sigma}_{QW}$ and σ_S. It was observed that σ'_T increases as σ_S increases as well as t_S/t_{QW} decreases and reaches the maximum when σ_S equals to $\tilde{\sigma}_{QW}$.

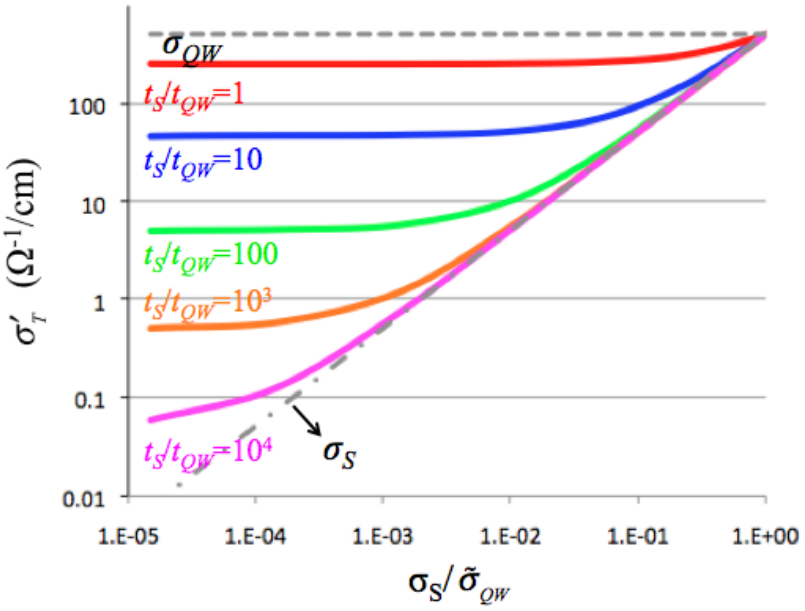

Figure 51. The total electrical conductivity of QW layers and SOI substrate (σ_T) as a function of substrate to QW electrical conductivity ratio ($\sigma_S/\tilde{\sigma}_{QW}$) at substrate to QW thickness ratio (t_S/t_{QW}) ranging from 1 to 10^4 where The horizontal top and oblique grey dash lines are σ_{QW} and σ_S, respectively, and σ_T is in between $\tilde{\sigma}_{QW}$ and σ_S.

The total Seebeck coefficient (S'_T) of QW layers and SOI substrate as a function of electrical conductivity ratio of substrate to QW ($\sigma_S/\tilde{\sigma}_{QW}$) at the thickness ratio of

substrate to QW (t_S/t_{QW}) ranging from 1 to 10^4 was plotted in figure 52. The horizontal bottom and oblique grey dash lines are $\tilde{S}_{QW}$ and S_S, respectively, and S_T' is in between $\tilde{S}_{QW}$ and S_S. As $\sigma_S/\tilde{\sigma}_{QW}$ increases, S_T' increases first and then decrease approaching to S_S; meanwhile, S_T' has an increase as t_S/t_{QW} increases.

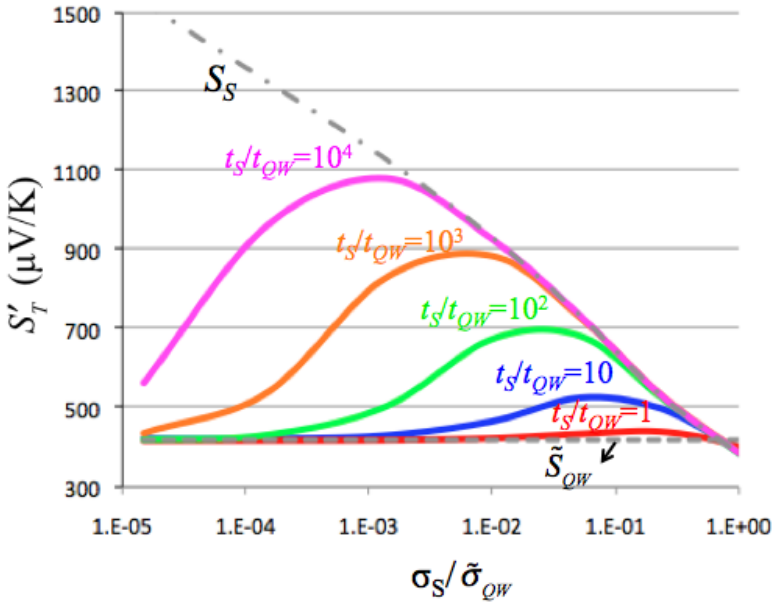

Figure 52. The total Seebeck coefficient (S_T') of QW layers and SOI substrate as a function of electrical conductivity ratio of substrate to QW ($\sigma_S/\tilde{\sigma}_{QW}$) at the thickness ratio of substrate to QW (t_S/t_{QW}) ranging from 1 to 10^4

Moreover, the total thermal power ($S_T'^2\sigma_T'$) of QW layers grown on SOI substrate as a function of electrical conductivity ratio of substrate to QW ($\sigma_S/\tilde{\sigma}_{QW}$) at the thickness ratio of substrate to QW (t_S/t_{QW}) ranging from 1 to 10^4 was plotted in figure 53. The horizontal top dash line is $\tilde{S}_{QW}^2\tilde{\sigma}_{QW}$ (=91μW·cm^{-1}·K^{-2}) of QW structure and oblique grey dash lines is thermal power of substrate ($S_S^2\sigma_S$), and the values of $S_T'^2\sigma_T'$ were shown in

between $\tilde{S}_{QW}^2\tilde{\sigma}_{QW}$ and $S_S{}^2\sigma_S$. The maximum thermal power is obtained at QW films alone or QW films on SiOG structure. The introduction of SOI substrate degrades the device performance, where higher t_S/t_{QW} and lower $\sigma_S/\tilde{\sigma}_{QW}$ give rise to more electrical loss.

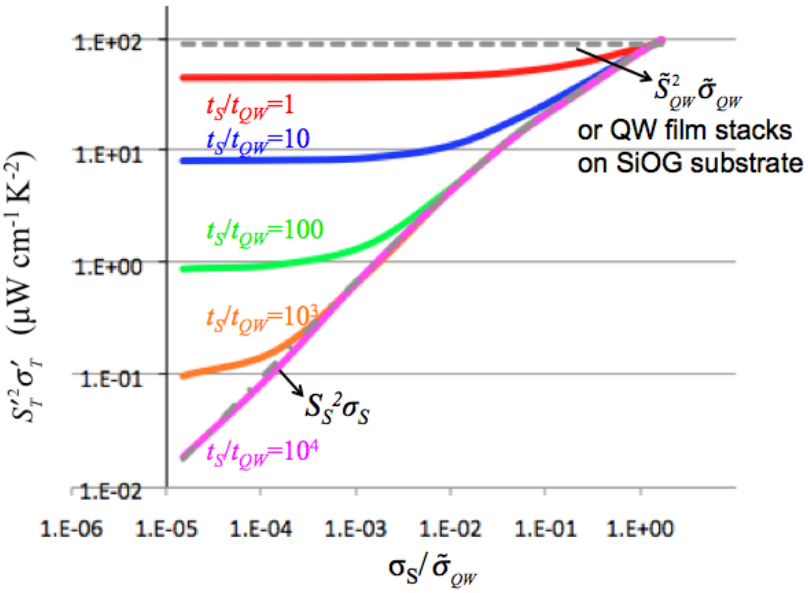

Figure 53. The total thermal power ($S_T'^2\sigma_T'$) of QW layers grown on SOI substrate as a function of electrical conductivity ratio of substrate to QW ($\sigma_S/\tilde{\sigma}_{QW}$) at the thickness ratio of substrate to QW (t_S/t_{QW}) ranging from 1 to 10^4

6.2.2 Thermal Parasitic Effect From Substrate

Besides electrical parasitic loss, the introduction of substrate also has substantial thermal influences on overall device performance. Firstly, thermal conductivity of substrate has a direct impact on the overall *ZT*. At 300K, bulk Si has higher thermal conductivity (κ_{Si}=146 W·m^{-1}·K^{-1}) compared to nanostructured Si and $Si_{1-x}Ge_x$ films (κ_{QW}≈22 W·m^{-1}·K^{-1}), and even higher than glass (κ=1.4 W·m^{-1}·K^{-1}). QW films and the underlying substrates are electrically disconnected therefore substrates exert only thermal

influence to the atop QW films. The same QW film parameters for electrical parasitic influence ($\tilde{S}_{QW}$ =419 μV/K, $\tilde{\sigma}_{QW}$ = 516 Ω^{-1}/cm and $\kappa_{QW} \approx$ 22 W $m^{-1}K^{-1}$) are used for *ZT* calculation. Instead of conductivity, the electrical resistance for QW films alone and the total thermal resistance for the combination of QW films and underlying substrates are calculated to take the geometry of devices into account, and meanwhile assure the non-dimensionality of *ZT*. The total figure of merit ($Z'T$) of QW alone, QW layers grown on SiOG and QW layers grown SOI substrate as a function of $\sigma_S/\tilde{\sigma}_{QW}$ ratio at different t_S/t_{QW} ratio ranging from 1 to 10^4 was plotted in figure 54. It is observed that QW alone gives rise to the highest $Z'T$; QW films stack on SOI has the smallest $Z'T$ value and decreases linearly as t_S/t_{QW} increase: $Z'T$; QW films stack on SiOG has $Z'T$ value lies in between. Due to electrical disconnection between QW films stack and substrates, thermal power ($\tilde{S}^2_{QW}\tilde{\sigma}_{QW}$) is fixed; therefore, the decreased $Z'T$ is derived from high total thermal conductivity. High thermal conductivity of bulk Si results in dramatically *ZT* degradation. Glass has the smallest thermal conductivity, provided that SiOG substrate no more than ten times thicker than QW films stack, $Z'T$ remain intact.

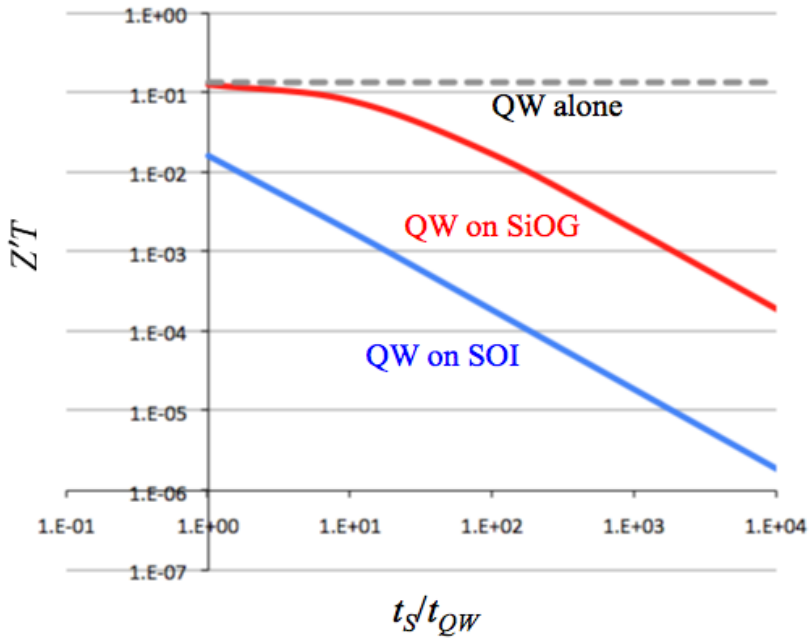

Figure 54. The total figure of merit ($Z'T$) of QW layers grown on SOI substrate, QW grown on SiOG substrate and QW films stack alone as a function of t_S/t_{QW} ratio

In case of electrical short of QW films stack and substates, not only does κ of substrates shift the overall ZT substantially, but also the effective cold side temperature of QW film stack or the thermal voltage of QW films stack will be changed consequently. Due to the high κ of SOI substrate, the effective cold side temperature of QW layers atop the substrate is elevated, which consequently reduces temperature differences and thermal voltage. In contrast, if low thermal conductivity SiOG substrate is employed, cold side temperature will not be dominated by the substrate. Metal contact at the cold side spreads out heat and allows good heat sinking to airflow or cooling water.

CHAPTER 7

CONCLUSION AND EXTENDED WORK

7.1 CONCLUSION OF THIS WORK

Thermoelectrical power generation as an alternative renewable energy generation method has drawn great attention and intensive research interests due to the advantages of high sustainability, longer lifetime, solid-state cooling and heating and environmental-friendly. Despite all the virtues, the relative low efficiency and high manufacturing cost become the main restriction for further development. Nevertheless, the implement of low-dimensional (quantum well and quantum wire) thermoelectric system has experimentally demonstrated the success of achieving high efficiency [33-34].

The objective of this thesis was to design and evaluate high performance Si/SiGe quantum well structures epitaxial grow on SiOG for automobile waste heat recovery application. The main motivations behind this research were driven by the following reasons: (1) Si/SiGe quantum well thermoelectric materials have demonstrated to yield high *ZT* at high temperature [11], [31], (2) Si/SiGe films are able to epitaxial grow on SiOG substrate and (3) the low thermal conductivity of SiOG leads to increased device efficiency.

Silvaco TCAD device simulator -ATLAS- was implemented to model and simulate QW thermoelectric device, the outcomes of which provide directions for future TE

device fabrication. Various device parameters of both *n*- and *p*-type QW were investigated exhaustedly, including quantum well/ barrier thickness, barrier doping concentration and Ge context, at temperature ranging from 300K to 900K at the purpose of optimizing the device performance. It was found that 4nm/20nm quantum well/barrier thickness was a better combination in terms of enhanced quantum confinement and better film quality. Also heavy barrier doping concentration ($\geq 5\times10^{19}cm^{-3}$) was preferred which not only yields to high $S^2\sigma$ at room temperature but also ensures that materials remain in extrinsic temperature region so that Seebeck coefficient was not degraded at high temperature. However, there was no conclusive result by using 20% or 40% Ge ratio, which seems to have less effect on thermoelectric behavior.

TEG can be considered as power source with certain internal resistance. The equivalent circuit of 2N thermal pellets was presented, which provides direction for power density optimization. The electrical and thermal contact requirements for TEG systems as a function of device length were also discussed. Moreover, the electrical and thermal parasitic effects from SOI and SiOG substrate were discussed and compared. It was concluded that SOI substrate brings in both electrical and thermal losses to QW films, and due to the high thermal conductivity of SOI substrate the temperature differences and Seebeck coefficient of QW decreases significantly. On the other hand, the low thermal conductivity of SiOG substrate not only is helpful to dissipate heat from QW films increasing temperature differences and Seebeck coefficient of QW but also decreases *ZT* directly.

7.2 Extended Work

7.2.1 Modeling Optimization Non-Ideal Factors

This thesis work mainly focuses on modeling and simulation based on default models provided by Silvaco and parameters from Silvaco as well as published results. The inaccuracy of quantum well parameters mostly originated from uncertainty of mobility in superlattice layers and strain induced energy band structure. Even though the simulation results from bulk materials were comparable to experimental counterparts, the accuracy of QW simulation was uncertain, which needs to be verified and calibrated upon future fabrication and measurement.

In our simulations, no heat loss from top and bottom surfaces was assumed with negligible heat sink thermal resistance at the cold side, which rarely hold in practical applications. Finite thermal resistance needed to be used in future modeling to take the non-ideal factor into account. For TEG module, the Seebeck coefficient and electrical resistance of conductors connected *n*- and *p*-type thermal pellets were neglected but actually have finite values, which introduce extra parasitic loss. Additional concern and optimization are needed to minimize the parasitic loss from metal connections.

7.2.3 TEG Module Assembly Using Microfabraction Technique

Conventional TEG modules are assembled using mechanical pick-and-place method [31]. A novel assembling method is proposed which takes advantage of microfabrication technology. The major process flows were illustrated in figure 55 and summarized as follows: (a) epitaxial growth of *n*- and *p*-type QW stacks on separate SiOG substrates, (b) patterning and etching QW layers to define the active regions, (c) depositing oxide for

passivation and formation of edge contact regions, (d) *n*- and *p*-type staggered alignment and substrate bonding, (e) patterning and etching oxide, (f) depositing and etching away metal (eg. Mo) to form side metal contacts and slicing glass sheets into individual strips similar concept as the Sliver ® technology used in solar cell industry [32].

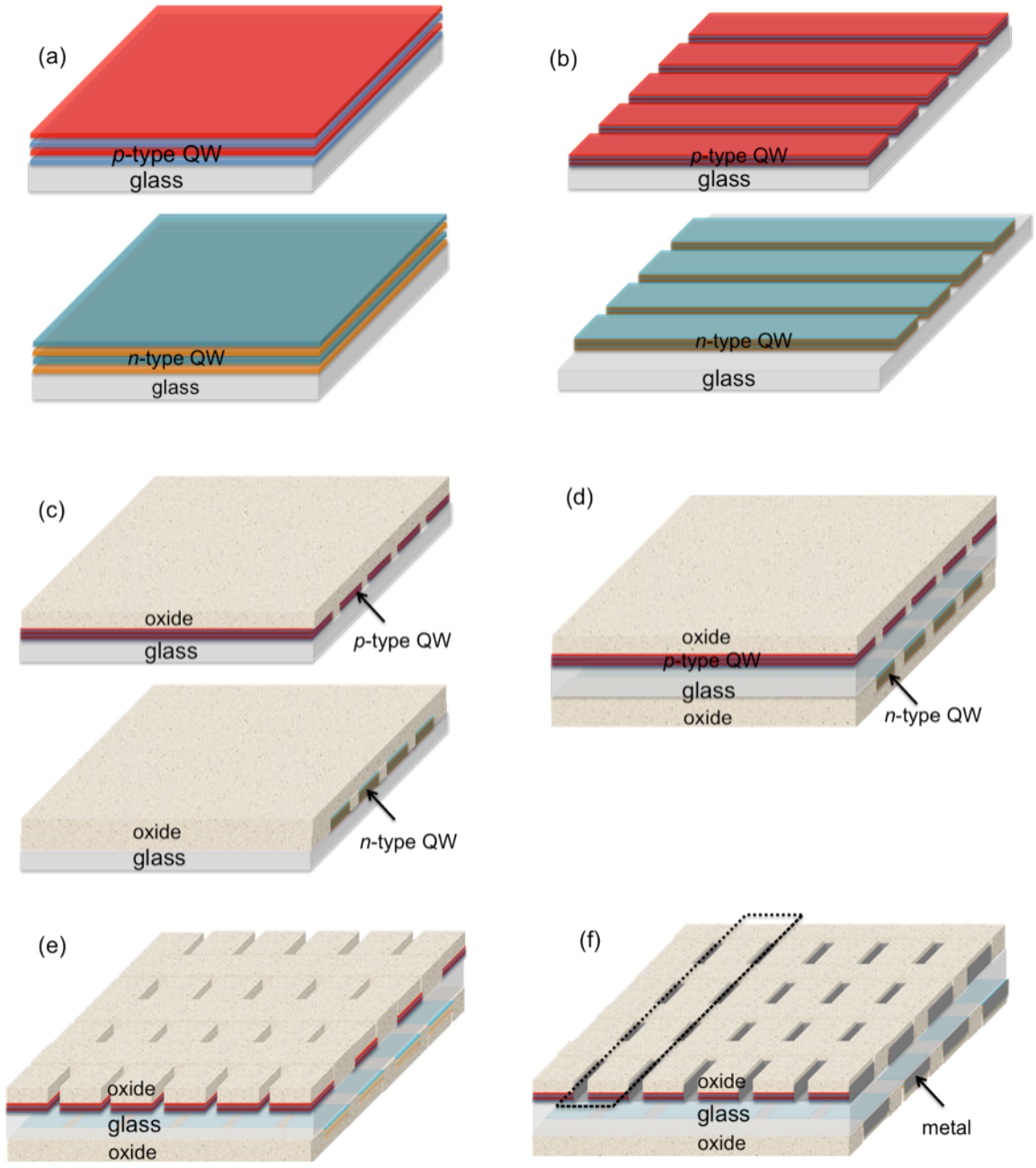

Figure 55. Process flows for QW TEG module assembling using microfabrication techniques.

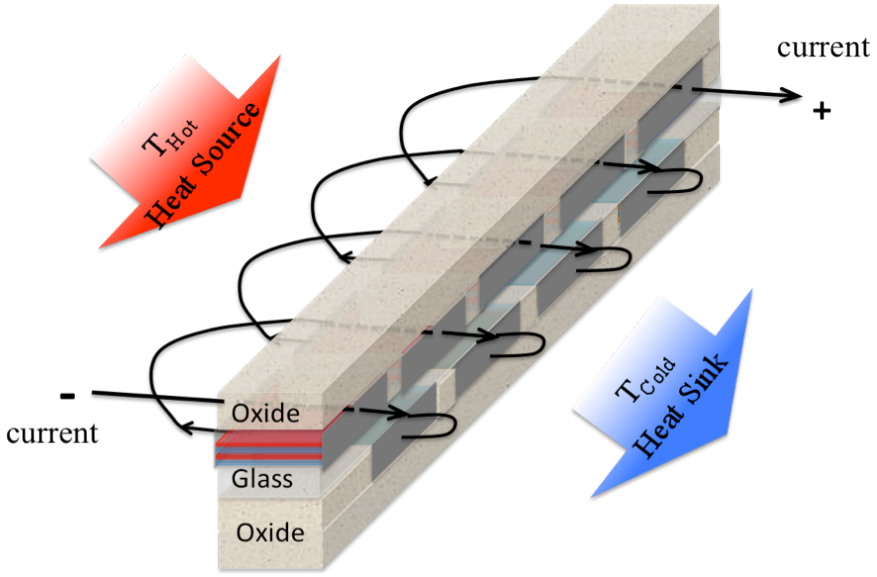

Figure 56. Sketch of one single strip where *n*- and *p*-type QW are staggered and connected using package level bump-bond series connections and the black arrows illustrate the current flow

Figure 56 shows the close-up sketch of one single strip where *n*- and *p*-type QW are staggered and connected using package level bump-bond series connections. If fix one side of the sliver to heat source and the other side to heat sink, and attach a reasonable load, the direction of current flow are illustrated as the black arrows in figure 56. Using external wiring connections, slivers possess the flexibility to assemble into to parallel or series configurations where the total length of slivers in series determines the output voltage while the width of slivers in parallel relies on the circuit drive requirement.

This microfabricated system assembly process flow of course is a concept and detailed process conditions need to be investigated and optimized. But first and foremost, high efficiency QW film stack requires to be realized before advancing to module assembly, which is still a long way to go.

APPENDIX A SILICON/ SILICON GERMANIUM PARAMETERS AT 300K [28]

Parameters (@ 300K)		Silicon	$Si_{1-x}Ge_x$
Lattice constant (Å)		5.431	$5.431+ 0.2x + 0.027x^2$
Number of atoms (cm^{-3})		5×10^{22}	$(5-0.58x)\times10^{22}$
Density (g/cm^3)		2.329	$2.329+ 3.493x-0.499x^2$
Dielectric constant		11.7	$11.7+4.5x$
Effective electron mass (in units of m_0)	Longitudinal mass m_l	0.98	~0.98 for $x<0.85$
	Transversal mass m_t	0.19	
Effective hole mass (in units of m_0)	Heavy hole m_{hh}	0.54	
	Light hole m_{lh}	0.15	
	Spin-orbit m_{so}	0.23	
Energy band gap E_g (eV)		1.12	$1.08-0.55x$ ($x\leq0.245$) $0.78-0.6(x-0.5)$ ($0.35<x\leq0.5$)
Electron affinity χ (eV)		4.05	$4.05-0.05x$
Effective Density of state	Conduction band N_C	3×10^{19}	~3×10^{19} ($x<0.85$)
	Valence band N_V	2×10^{19}	

(cm^{-3})			
Intrinsic carrier concentration n_i (cm^{-3})		1.08×10^{10}	
Specific heat (J/mol/K)		19.6	19.6+2.9x
Thermal conductivity (W/cm/K)		1.48	~0.046+0.084x (0.2<x<0.85)
Thermal diffusivity (cm^2/V)		0.8	
Thermal velocity (cm/s)	Electrons v_n	2.4×10^7	2.4×10^7
	Holes v_h	1.65×10^7	$(1.65+0.25)\times10^7$
Mobility (cm^2/V s)	Electrons μ_n	1396	1396-4315x (0≤x<0.3)
	Holes μ_h	450	450-865x (0≤x<0.3)

APPENDIX B ALTAS DEVICE SIMULATION

```
## Set Variables ------------------------------------------------
set Thot  = 305
set Tcold = 295
set cycle=11
set XSi=0.02
set XSiGe=0.004
set NSi=5E19
set NSiGe=1E14

## Mesh ---------------------------------------------------------

mesh  auto

x.mesh loc=0               spac=0.05
x.mesh loc=3             spac=0.05

## Regions ------------------------------------------------------

DBR half.cyc=$cycle  mat1=Si mat2=SiGe thick1=$XSi thick2=$XSiGe
n1=10 n2=10 Na1=$NSi Na2=$NSiGe Qwell2=true well2.nx=100 well2.ny=10
x2.comp=0.2 top
```

```
## Electrodes -----------------------------------------------------

electrode name=source x.min=0 x.max=0  y.min=-(6*$XSi+5*$XSiGe)
y.max=0 num=1
electrode name=drain  x.min=3 x.max=3  y.min=-(6*$XSi+5*$XSiGe)
y.max=0 num=2

contact     name=source  neutral
contact     name=drain   neutral

material material=SiGe tcon.comp hc.comp  affinity=4.04 Nc300=1.2e18
Nv300=7e19  Nc.F=-1
material material=silicon   affinity=4.05  EG300=1.12  Nv300=9e20
Nc300=9E17 Nc.F=-1

mobility mu2p.arora=233 material=SiGe
## Models -------------------------------------------------------

thermcontact elec.num=1 temp=$Thot
thermcontact elec.num=2 temp=$Tcold

models consrh auger srh.exptemp arora Fermi print lat.temp heat.full
bgn phonondrag schro  p.schro
method  block newton gummel

output band.temp band.param con.band val.band recomb qfn qfp
e.mobility h.mobility j.drift j.diffusion

log outf=$'Xsi'_$'NSi'Si$'XSiGe'_$'NSiGe'SiGe.log
solve vdrain=0 vstep=0.1 vfinal=0.5 name=drain
extract name="$'Xsi'_$'NSi'Si_$'XSiGe'----------------------"
extract name="Voc" 1E5*max(vint."drain")

struct outf=$'Xsi'$'NSi'Si_$'XSiGe'SiGe.str
extract init infile="$'Xsi'$'NSi'Si_$'XSiGe'SiGe.str"

extract name="SiGe_1" 2d.area impurity="Hole Conc" x.step=0.01
x.min=0 x.max=3 y.min=-3*($XSi+$XSiGe) y.max=-3*$XSi-2*$XSiGe
extract name="SiGe_HConc" $SiGe_1/3/$XSiGe*1E12
extract name="Total" 2d.area impurity="Hole Conc" x.step=0.01
x.min=0 x.max=3 y.min=-6*$XSi-5*$XSiGe y.max=0
extract name="HoleTotal" $Total/3/(6*$XSi+5*$XSiGe)*1E12
extract name="End-----------------------------------------"
tonyplot

quit
```

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