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Oxidized porous silicon for localized formation of SOI active regions

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OXIDIZED POROUS SILICON FOR LOCALIZED FORMATION OF SOI ACTIVE REGIONS

By

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A tribute of love to my parents,

Leela and Ramakrishna

for their love, encouragement,

blessings and support.

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ABSTRACT

The oxidation of electrochemically etched porous silicon (Si) has demonstrated success in the formation of device quality Localized Silicon on Insulator (L-SOI) for Complementary Metal Oxide Semiconductor (CMOS) applications [1, 2]. A primary advantage of L-SOI formation is the ability to integrate novel device structures and optoelectronics (i.e. optical switches, waveguides) with bulk silicon CMOS. The formation of porous Si can be selective by controlling the Fermi level in areas to be etched or not etched, which is typically done by adjusting the level of doping [1]. An alternative method is to introduce a reversible donor species such as protons [2] or fluorine (this work) for the selective formation of islands of crystalline silicon surrounded by porous silicon. Implanted fluorine in silicon has demonstrated a donor effect upon annealing at low temperature (600°C), which is reversible as the fluorine out diffuses during higher temperature annealing (1000°C). Crystalline silicon islands that were fabricated with this technique have a thickness of about 150nm and are completely surrounded by oxidized porous silicon. Further study to investigate the device quality of the L-SOI structures for microelectronic applications and optoelectronic applications has been done by building transistors for microelectronic application and waveguides for optoelectronic application.

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Chapter 1: *INTRODUCTION*

1.1 Background

Porous silicon is a combination of silicon and void space and is formed due to anodic dissolution of silicon in hydrofluoric acid electrolyte (HF) in the presence of hole carriers. It was first discovered accidently by Uhlir [3] (Bell Labs, Murray Hill, NJ) in 1956 when they were trying to electropolish silicon wafers. It was considered a nuisance at the time [3]; its potential was not realized until many years later. Turner [4] was the first to study electrochemically prepared porous Si using a subtractive anodization process, as opposed to an electroplating process where silicon typically acts as a cathode. Chemically prepared films were studied by Archer [5] in 1960. Watanabe *et al*, [6, 7] first reported their porous nature and the fast oxidation of thick porous Si films [8–10]. In the 1970, porous Si was utilized for dielectric trench isolation of active Si devices [11–13]. The interest in porous Si has drastically increased after the discovery of high efficient visible light emission properties due to quantum confinement in porous Si [14] by Canham [15] in 1990.

This work explores the properties of electrochemically prepared porous Si for L-SOI applications. The formation process has intricate dependence on many factors [16-18] such as HF concentration, doping type and doping concentration of the Si wafer, etching current density, and illumination intensity.

1.2 Motivation

Porous Silicon is a versatile material; it can be used in many different applications due to its many attributes. Notable features that brought porous Si to the technology forefront is the ability of this form of silicon to emit visible light, first reported by Canham [15], and the invention of Fully-Isolated Porous Oxidized Silicon (FIPOS) structures by NTT for the fabrication of L-SOI regions [2]. These events presented opportunities for application in mainstream device technology. By changing the porosity of the porous Si film, the refractive index can be adjusted between that of air (n ~ 1) and silicon (n ~ 3.5). This property can be used to make optical structures such as antireflective layers, waveguides, etc., giving us the opportunity to integrate optoelectronic devices with Complementary Metal Oxide Semiconductor (CMOS) circuits. Porous Si can be selectively masked based on preferential anodization of p-type Si to n-type [2], which allows bulk and SOI based devices to be fabricated on the same chip. The work that is presented in this thesis also demonstrates the ability to make L-SOI using a technique similar to the reported FIPOS process [2] creating reversible n-type regions using fluorine. The L-SOI process demonstrates the ability to make very thin films of 200 nm or less; thickness comparable to present day partially depleted SOI substrates. The L-SOI process can be easily integrated into a CMOS fabrication process, and realized in any IC fabrication facility.

1.3 Goal & Objectives

This work involves the development of L-SOI regions using the mentioned porous silicon isolation technique. The goal of this study was to develop L-SOI active device regions using fluorine as a reversible donor species, and to characterize the device quality of the silicon surface. This was accomplished through several objectives, which included: Addressing the challenges of process integration of oxidized porous Si with a standard CMOS technology; studying the effects of high-dose fluorine implantation in the active (channel) device regions; and fabricating and testing the optical performance of waveguide structures. This work has provided a thorough understanding of the porous silicon formation and suppression mechanisms discovered using the developed technique, and the influence of the key process factors involved in the fabrication of L-SOI structures.

1.4 Thesis Outline

In order to describe the investigation as defined above, the remaining chapters of this thesis are structured as follows. Chapter 2: describes the fundamental mechanisms involved in the electrochemical formation of porous silicon. Chapter 3: gives an overview on porous silicon technology. Different types of electrochemical cells are described, and the factors influencing the formation of porous silicon are discussed in detail. Chapter 4: provides an overview on SOI substrate technology and introduces a new technique for the formation of L-SOI regions using fluorine implantation. Chapter

5: describes the investigation on input factors that lead towards the development of a process flow for integrated device structures. Chapter 6: describes the results of NMOS transistors and waveguide structures that were built using the described L-SOI technique. Devices are characterized and performance indicates certain modifications for improvements that are summarized in Chapter 7:.

Chapter 2: *FUNDAMENTALS OF ELECTROCHEMISTRY*

Electrical carrier transport is a requirement for the formation of porous Si, where there have been several proposed electrochemical formation models. This chapter gives a basic introduction to electrical carriers in semiconductors and electrolytes and associated interface transport properties. Analogies are drawn between metal-semiconductor Schottky contacts and the semiconductor-electrolyte interface in describing carrier transport under electrical bias.

2.1 Introduction

The energy spectrum of free carriers (electrons & holes available for conduction) in a perfect semiconductor crystal consists of allowable states known as energy bands and the absence of states known as the energy band gap. The allowable energy states associated with electrons are above E_c (conduction band edge) and the allowable energy states associated with holes are below E_v (valence band edge). The magnitude of the energy gap ($E_G = E_c - E_V$) in crystalline silicon is 1.12 eV at room temperature (see Figure 2.1) and can be reduced by increasing temperature [20]. The Fermi Energy (E_F) is a level within the forbidden energy band gap that is used to describe the statistics of free carriers in a semiconductor. The position of E_F defines the equilibrium concentration of free carriers in the material [19].

Conduction in a semiconductor can take place with carriers provided by atoms of the crystal material itself through thermal generation of electron-hole pairs (intrinsic

semiconductor) or through carriers provided by the introduction of external impurities or dopants that bond with the host material. There are two types of dopants in the extrinsic case known as donors and acceptors. Donor impurities are located at energy levels just below the conduction band edge, and give up electrons to the conduction band leading to electron conduction (n-type semiconductor). Acceptor impurities are located just above the valence band edge and capture valence electrons from the bonding sites leading to the availability of hole carriers (p-type semiconductor).

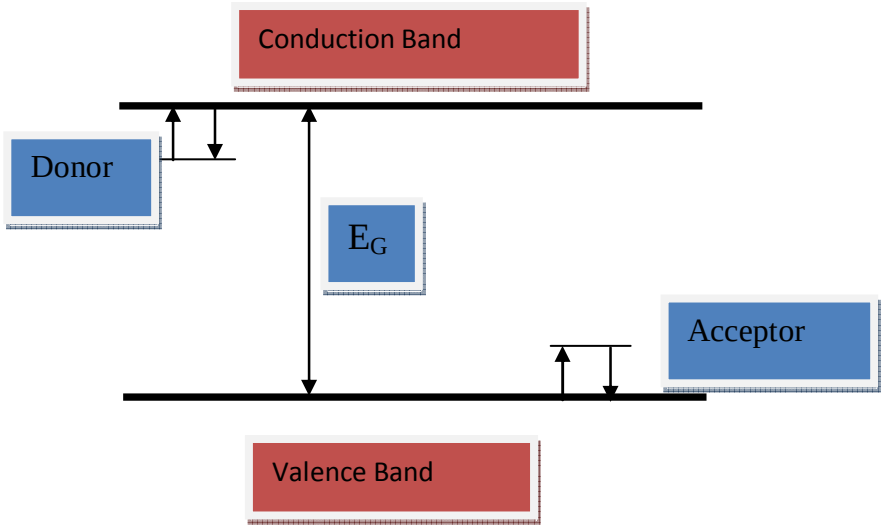


Figure 2.1: The energy band diagram for a semiconductor showing both conduction and valence band edges with donor and acceptor impurities in the forbidden gap region [19].

Analogous to E_F in a semiconductor is the Redox potential in aqueous electrolytes [20], which represents the ability to gain or lose electrons. Likewise, analogous to E_C and E_V are oxidation and reduction potentials, illustrated in Figure 2.2. The oxidation potential of an electrolyte is the ability to lose electrons, and the reduction potential of an electrolyte is the ability to gain electrons.

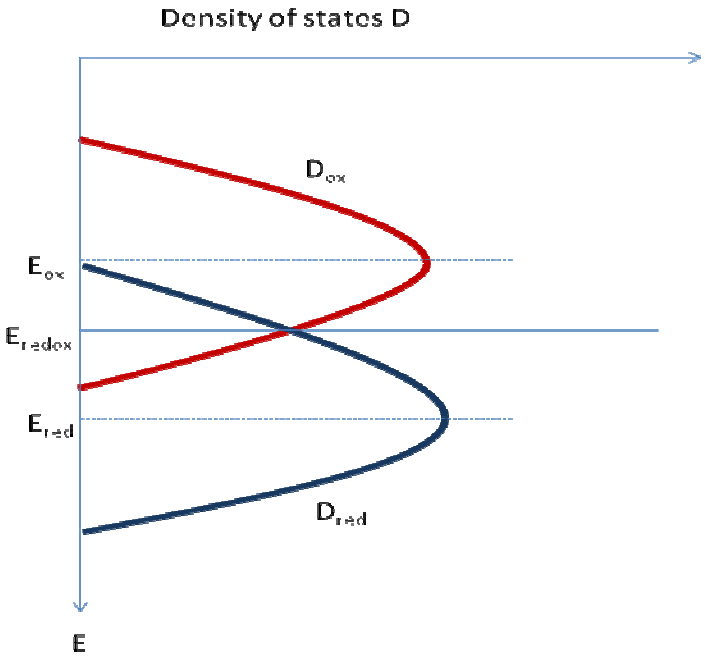


Figure 2.2: The different energy levels and the density of states in the electrolyte. The redox potential $E_{redox} = (E_{ox} + E_{red})/2$ is the mathematical mean of the energy levels E_{ox} of the oxidized species and E_{red} of reduced species. D_{ox} describes the density of empty states and D_{red} describes the density of occupied states [21].

2.2 Metal-Semiconductor Contact

A metal semiconductor (MS) contact is used as a baseline for comparison of semiconductor electrolyte interface. Like in the case of MS contacts, semiconductor-electrolyte has two materials with different bandgap brought into intimate contact with each other. Unlike metals where excess charge resides at the surface, the electrolyte has charge distributed, as in the case of semiconductor depletion region. Hence for understanding semiconductor-electrolyte interface understanding of MS contact behavior is very critical.

Under equilibrium conditions a metal and semiconductor brought into contact with each other must have constant Fermi energy levels. In the case of MS contacts with higher levels of semiconductor Fermi energy than a metal leads to lowering of Fermi

levels of semiconductor by a difference of metal (ϕ_m) and semiconductor work functions (ϕ_s). The work function of a material is defined as the energy difference between the vacuum level and the Fermi level

A p-type semiconductor with $\phi_m<\phi_s$ leads to rectifying behavior; electron transfer takes place from metal into semiconductor side of the junction forming a depletion region on the semiconductor side. Electric field is created due to difference in potentials in the two regions leading to bending of bands as shown in Figure 2.3a.[22] The case where $\phi_m>\phi_s$ leads to ohmic behavior in a p-type semiconductor. Hence the electrons are transferred from the semiconductor into the metal leading to a depletion layer formation on the semiconductor side and eventually leading to bending of bands as seen in Figure 2.3b.

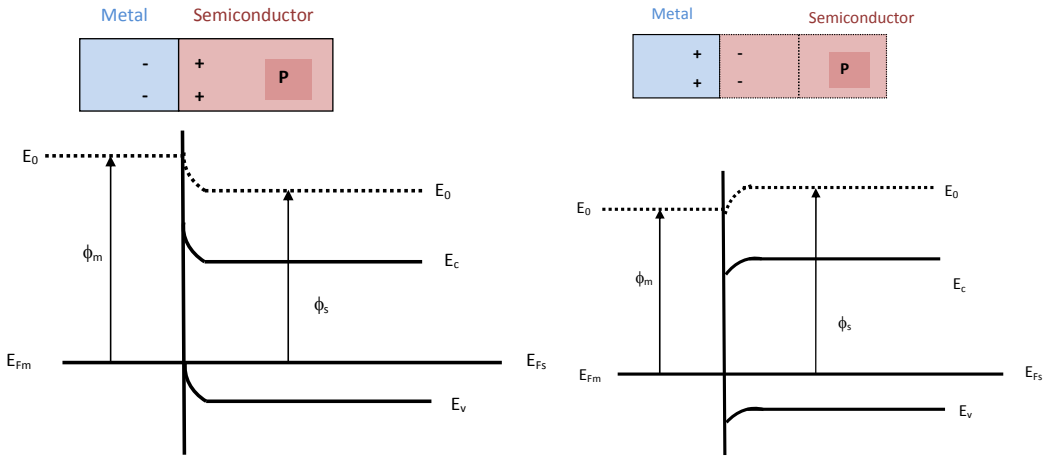


Figure 2.3: Representation of a P-type semiconductor and metal interface. a) Rectifying contact ($\phi_m<\phi_s$) b) ohmic contact ($\phi_m>\phi_s$). Under equilibrium Fermi energy levels attain a constant level for both semiconductor and metal. This leads to band bending of conduction and valence band edges due to potential difference.

2.3 Semiconductor-Electrolyte Contact

This section reviews the properties of semiconductor electrolyte interface [23,24,25,26]. When an electrolyte and semiconductor are brought together under equilibrium condition like in the case of MS contacts, the Fermi level of the semiconductor and E_{redox} potential of the electrolyte should be at the same level, resulting in band bending due to the potential difference in the two levels. At equilibrium the Fermi level of the p-type semiconductor is lower than that of E_{redox} as seen in Figure 2.4, therefore the electron transfer takes place from the electrolyte side towards the semiconductor side resulting in a formation of space charge region on the semiconductor side. The electrolyte contact can behave similar to a metal region or a semiconductor region, depending on the solution ion concentration (molarity). In the electrolyte ions are distributed across a double layer, a sheet charge known as Helmholtz layer, typical thickness of the Helmholtz layer is about 3Å, again Helmholtz layer is distributed into inner and outer Helmholtz layers one containing ions in solution adsorbed at the surface of the solid, the other is due to the ions of opposite sign attracted by adsorbed ions. Another layer referred to as the Gouy layer, an ionic layer extending from the outer Helmholtz to the bulk is formed. This layer has negligible contribution for solution concentration more than 0.1 M. ultimately when the semiconductor and electrolyte are brought in contact the resulting energy band diagram is as depicted in Figure 2.4**.**

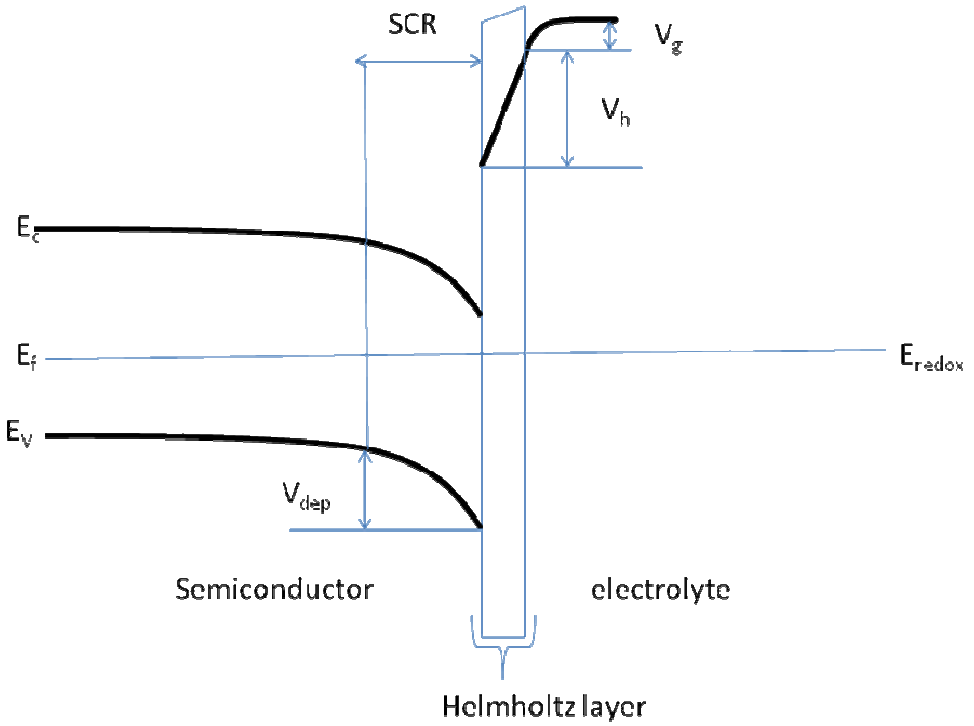


Figure 2.4: Schematic illustration of the double layers in the P-type semiconductor/electrolyte interface at an equilibrium state. And it also represents the electrolyte equivalent of the space charge region (V_{dep}) known as Helmholtz layer (V_h) and Gouy layer (V_g).

In an ideal situation assuming there are no surface states. The electron transfer takes place directly between energy bands of the electrolyte and the electrode assuming the initial and final energy states coincide [21] as depicted in

Figure **2.5**.

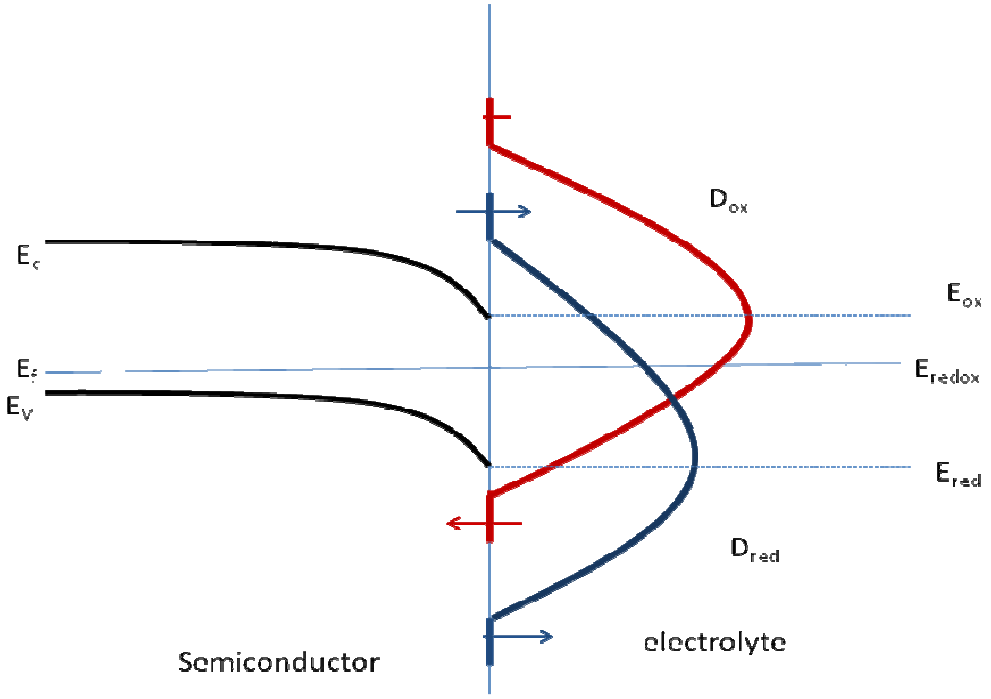


Figure 2.5: Schematic illustration of the electron transfer as anodic and cathodic current via the conduction and valence band edges. The arrows represent the conventional current flow between semiconductor and electrolyte interface. $I_{c,}$ represents the cathodic current and i_a represents anodic currents flowing across both conduction and valence band edges [21].

From

Figure **2.5** it can be observed that the conduction band edge is closer to the oxidation potential edge of the electrolyte side and the valence band edge is closer to the reduction potential of the electrolyte side. Anodic reaction involves transfer of electron from electrolyte molecules to the semiconductor (i_a) and vice-versa for the cathodic current (i_c). The magnitude of the anodic current and cathodic current are represented in (2.1) and (2.2) and they depend on the number of molecules attracted towards the electrode surface during the reaction as:

$$i_a = F.z.c \int_{-\infty}^{+\infty} k(E).Nem(E).Dred(E)dE \quad (2.1)$$

$$i_c = F.z.c \int_{-\infty}^{+\infty} k(E).Noc(E).Dox(E)dE \quad (2.2)$$

where F is the Faraday constant, z·c is the number of molecules that reach electrode surface, k(E) the transition coefficient and strongly depends on the distance of reacting molecules from the surface, and Nem, Noc represent the density of empty state of the electrode and Dred, Dox are filled and empty states in the electrolyte.

In the case of a conduction band process the empty states Noc = Nc and is bias independent. In the case of valance band process the electron transfer is only possible through the presence of holes at the surface therefore density of empty states in the valence band edge is equal to the hole density, Ps, which in turn depends on the band bending at the surface and hence on the doping concentration as well as on the bias voltage. Therefore, the valence band component of the anodic current is doping and bias dependent [21].

In the case of cathodic currents, electrons transfer takes place from the semiconductor to the empty states in the electrolyte, which have a density of Dox. The conduction band component of the cathodic current requires electrons on the surface and hence depends on the electron surface concentration n_s. The valence band component of the cathodic current Ic,v depends on the effective density of states N_V in the valence band [21]. The net current can be written as:

$$i = i_0[1 - \exp(-e\eta/Kt)] \quad (2.3)$$

The form shown in (2.3) represents the standard metal-semiconductor Schottky barrier contact [20] commonly referred to in the literature [21-30].

2.4 Summary

While carrier transport across a semiconductor-electrolyte interface can be well understood, the situation becomes much more complex if there is an associated electrochemical reaction. Thus is the case in the formation of porous silicon, where the reactions were presented at the beginning of this chapter. There have been several electrochemical models proposed to describe the partial dissolution of silicon resulting in a material of various morphologies made up of remaining silicon and void space. Chapter 3: will describe the properties of porous silicon and review these models of formation in detail.

Chapter 3: *PROPERTIES OF POROUS SILICON*

Porous Si forms by electrochemically etching a silicon wafer in an electrolyte containing hydrofluoric acid (HF). This chapter begins with a review of the fundamentals of porous Si. Different models proposed historically to explain the porous Si formation mechanisms, different types of anodization cells, pore morphologies, characterization techniques and, most importantly, factors which influence porous Si formation and the resulting material properties are discussed.

3.1 Introduction

Porous silicon is a combination of silicon and void space and is formed by a subtractive etch process through electrochemical etching using an HF solution as the electrolyte. Under most conditions, a silicon surface is virtually inert to HF. However by the application of anodic bias, silicon is dissolved in HF in the presence of hole carriers. This dissolution, based on the etching conditions, can lead to two phenomena; one being electropolishing [32] which is an indirect method based on formation of anodic oxide and dissolution in HF solution. The other results in a sponge like partially dissolved silicon material known as porous silicon shown in Figure 3.1a. Both of the operating regions are represented in the current-voltage characteristics as shown in Figure 3.1b. The J_{crit} point on the curve is a small spike as shown in Figure 3.1b, and differentiates the two regions. Porous Si formation is obtained in the region below the J_{crit} point and the electropolishing region starts above the J_{crit} point.

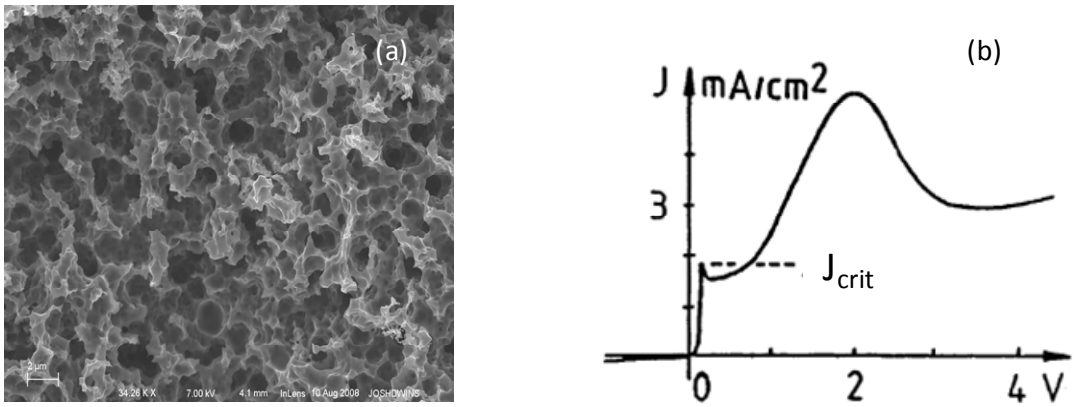


Figure 3.1: (a)SEM top down view of a porous Si film etched on p-type substrates, showing silicon and void spaces. (b) Representation of a typical anodic current-voltage characteristic of a p-type substrate. It also represents critical current density J_{crit} which is a differentiating point between porous Si and electropolishing regimes [33].

3.2 Porous silicon formation mechanism

A silicon surface is virtually inert against hydrofluoric acid (HF) because the electron affinity of hydrogen is close to that of silicon. Under anodic bias holes in the silicon electrode reach the surface making it prone to neucleophillic attack of electron rich atoms in the solution; in this case fluorine atoms as shown in Figure 3.2-1. Fluorine replaces the hydrogen atom that is bonded to silicon as shown in Figure 3.2-2. But the fluorine atom that is bonded to silicon causes polarization making it prone to another fluorine attack replacing the remaining hydrogen bond as shown in Figure 3.2-3 and resulting in the evolution of hydrogen. Eventually the silicon atom is separated as shown Figure 3.2-5, also leading to a byproduct of silicon hexafluoride and the evolution of hydrogen gas.

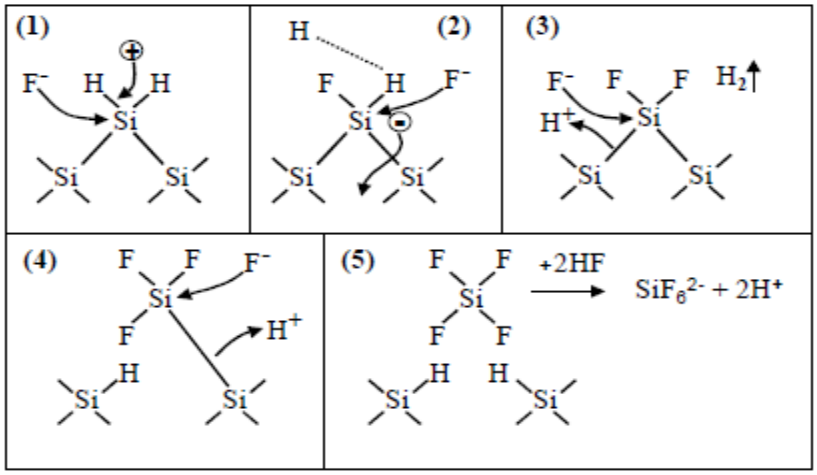


Figure 3.2: Etching mechanism involved in the porous Si formation proposed by Lehmann and Gosele. After ref [34].

3.3 Porous silicon formation model

There have been several models proposed to explain the formation of porous silicon. The connection between the semiconductor-electrolyte transport theory described in Chapter 2: can be somewhat obscure due to the complexities involved with the transport and resulting electrochemical reaction.

3.4 Depletion layer and field intensification model

Beale *et al.* were the first group to present a model that explains the porous Si formation process [35-37]. The model proposed states that during anodization the porous silicon surface is always depleted of hole carriers. The spacing between the pores is always less than width of the depletion region width W_{DEP}, which is formed at the Si/HF interface, and the depletion region is responsible for current localization at the pore tips, where the field is intensified. The field intensification is attributed to the large curvature at the pore tips. Hence, the current flows only at the pore tips and not across the pore walls. For lightly doped p-type Si, the hole transfer from the bulk of Si to the

Si/electrolyte interface is described by thermionic emission. The small radius of curvature at the pore tips reduces the Schottky barrier height and thus increases the current density at the pore tips. For heavily doped materials, the current flows by tunneling, this depends on the barrier width W_{dep}. The large curvature at the pore tips reduces the barrier width W_{dep} and hence increases the current density. The model provides a deeper understanding level of the current localization required for porous Si formation on different Si substrates and explains the correlation between the relative pore dimensions and the space charge region. Even though the model does a good job explaining all the physical aspects based on semiconductor physics but doesn't explain the chemical interaction during the anodization process, and also lacks in explaining the micropore formation in n-type semiconductor substrates.

3.5 Carrier diffusion model

Smith *et al.* [38,39] at the end of 1980's proposed a computer simulation model based on the diffusion of holes in the semiconductor. This model is based on a concept called as random walk of hole carriers. They assumed that the pore structure is determined by the random availability of hole carriers from the bulk of the semiconductor towards the growing pore tips. The model explains the dependence of pore density, diameter, shape and layer porosity as well as the transition from porous Si formation to the electropolishing on the etching parameters.

Although the Carrier diffusion model simulated some morphological features of porous Si, it was too general to account for the different current conduction mechanisms for different types of Si substrates. The mechanism of formation of porous silicon on

heavily doped n-type substrate through injection of electrons in the dark cannot be explained using this model and it also doesn't take into account the properties of semiconductor electrolyte interface.

3.6 Quantum confinement model

The most generally accepted model for the formation mechanisms of porous Si was proposed by Lehmann and Gösele in 1990 [34]. They postulated the quantum confinement model to account for the nanometer size features in the remaining crystalline silicon [34]. Quantum confinement occurs due to an increase in the energy band gap caused by the quantum size porous structure. The confinement prevents the charge carriers from entering the wall region of porous Si, and hence the anodization process only takes place at the pore tips [16] which establishes the etch front.

Frohnhoff *et al.* [40] extended the quantum confinement model to account for the wide distribution of pore diameters of porous Si formed on p-type Si. The model proposes the tunneling of holes in the crystal to be responsible for nanometer size pore formation. The model has been also adopted by many groups to explain observed luminescence from porous Si [41,42]. The model successfully explains the formation of crystallites of a few nanometers. However, it doesn't account for effect of doping and HF concentration on anodization and also it doesn't account for highly doped n-type silicon anodization in the dark.

3.7 Different types of anodization cell design

A standard electrochemical cell with a single tank and two electrodes can be used for anodization process as shown in Figure 3.3. A silicon wafer acts as an anode and an inert and HF resistant metal such as platinum can act as a cathode. A major advantage of this cell is its ability to etch SOI or SOG wafers. The major drawback being the anodization occurs only in regions in contact with chemistry. In addition the lateral current flow across the sample maintains a potential difference between points A and B shown in Figure 3.3, leading to non-uniform anodization.

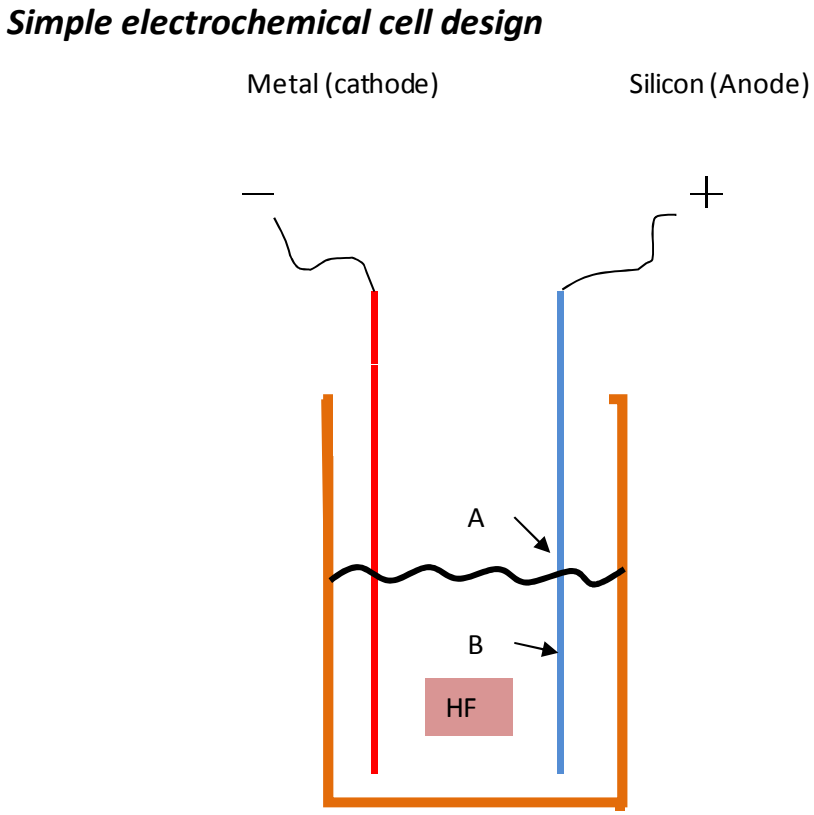


Figure 3.3: Representation of a simple electrochemical anodization cell with HF as electrolyte and a HF compatible inert electrode as a cathode and silicon wafer to be etched acts as an anode.

The cell represented in

Figure **3.4** is widely used in porous silicon applications. It has a platinum electrode at the top forming a cathode and aluminum puck as a wafer backside contact and a reservoir of HF on top in contact with only the front part of the silicon wafer. The uniformity of anodization in this cell is very good except for about 2mm at the edge where the O-ring seal makes contact. The major drawback of this cell is the need for backside metallization to form an ohmic backside contact.

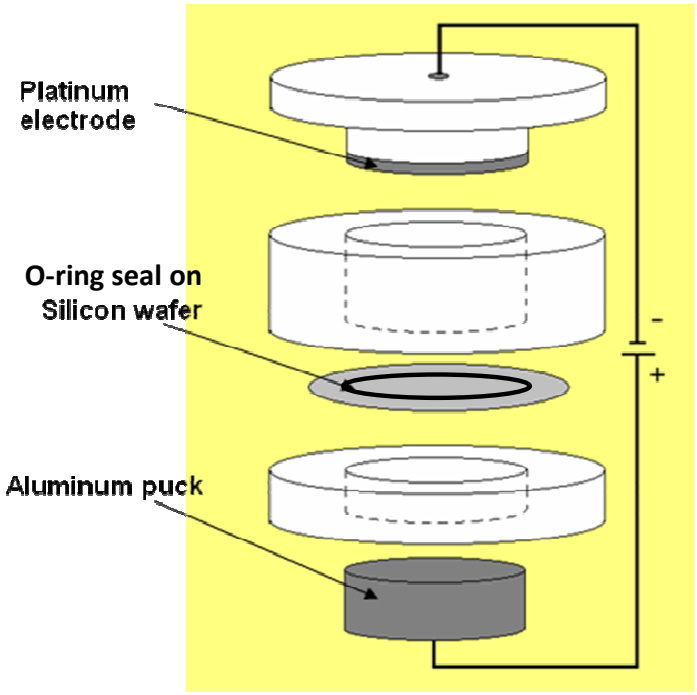


Figure 3.4: Illustration of anodization cell used for most of this work. It has a platinum electrode as a cathode, and the silicon wafer acts as the anode. An aluminum puck serves as the backside contact to the wafer.

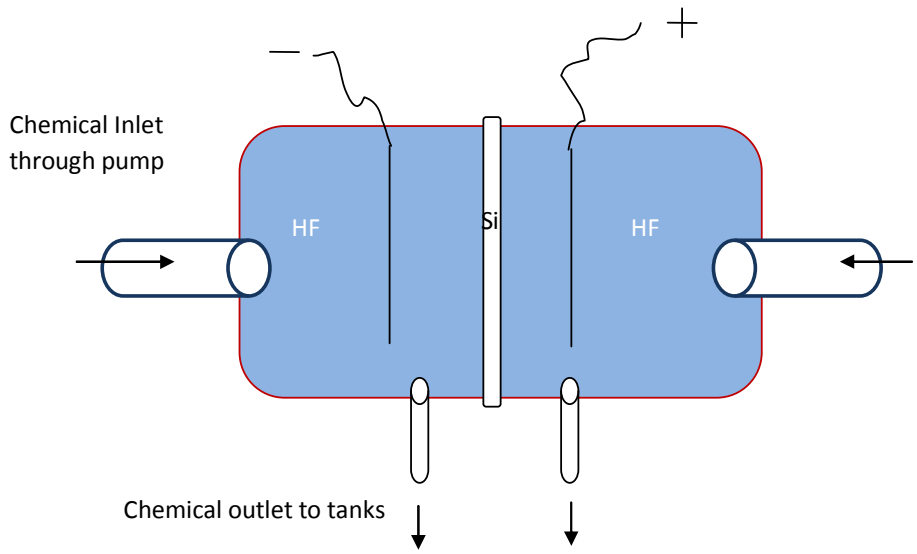


Figure 3.5: Representation of anodization double cell model used for porous Si etching. It has HF as electrolyte forming the backside contact in place of aluminum puck used in previous design. It uses a pumped chemical inlet and gravity fed chemical outlet to the tanks.

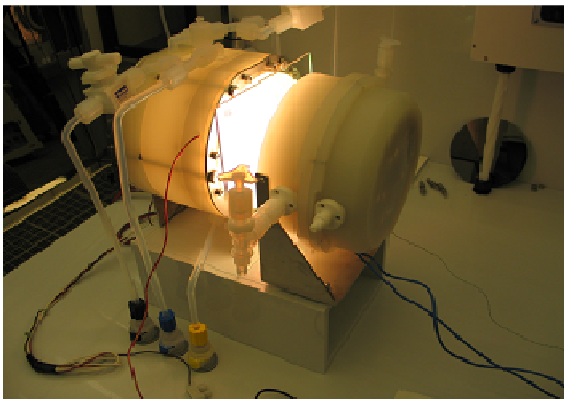


Figure 3.6: Picture taken of a double cell model with illuminated backside at work. The cell is a prototype built by Semitool, Inc., which led to a fully-automated commercial model.

Double cell design shown in

Figure **3.5** has two cells with lines plumbed into HF tanks through a pump and a gravity drain to drain back into HF tanks. This cell has two platinum electrodes in both halves of the cell and HF in both tanks form a front and backside contact to the wafer. The major advantage of the cell is its ability to continuously pump liquid in and out of the system so that there are always fresh chemistries in the cell, due to the continuous flow;

the hydrogen bubbles formed at the platinum electrode are effectively removed with the flow. Therefore a very uniform film without the need of backside metallization can be realized.

Figure **3.6** shows a prototype of the first commercially built anodization cell by Semitool Inc. with a backside illumination capability.

3.8 Types of Porous Silicon

Porous silicon can be broadly classified into three types known as microporous silicon as shown in

Figure **3.7**(a), mesoporous silicon shown in

Figure **3.7**(b), and macroporous silicon shown in

Figure **3.7**(c). According to the International Union of Pure and Applied Chemistry (IUPAC) convention, microporous silicon has a pore size less than 2nm, mesoporous silicon has a pore size between 2nm to 50nm, and macroporous silicon has a pore size greater than a micron [43]. These different morphologies are obtained by changing HF concentration, current density, time, light assistance, and substrate type and resistivity.

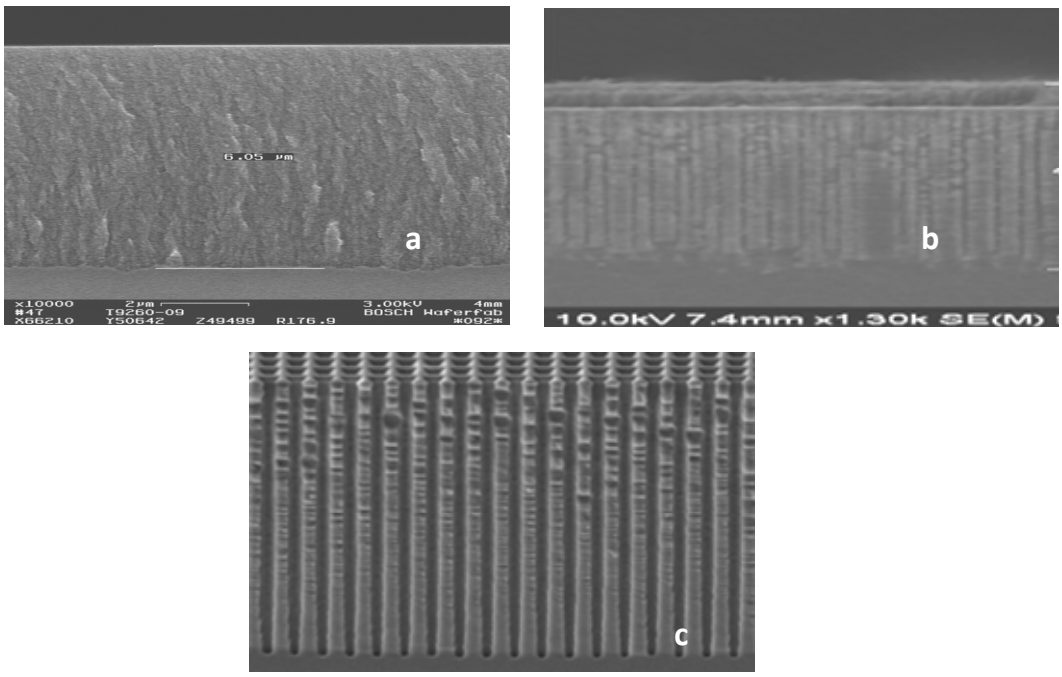


Figure 3.7: SEM cross-sectional representation of different porous silicon morphologies. a) Microporous silicon film b) Mesoporous silicon film c) Macroporous silicon film

Porosity is the primary metric used for porous silicon layer characterization. It is defined as the percentage of void space to silicon, and can be characterized on a blanket porous silicon film. In order to determine the porosity, the thickness of the film must be established; therefore a high resolution Scanning Electron Microscope (SEM) is used. However due to depth of focus limitations, SEM cannot resolve porosity of a film. Hence a conventional and simple method is used where weights of the wafers are taken, before and after the electrochemical etching. Then thickness measurements are made with the SEM. Equation (3.1) is then used to determine the porosity. This equation gives an average value of porosity and is known as the gravimetric method [43].

$$P = \frac{W1 - W2}{T \times S \times d} \qquad (3.1)$$

where W_1 is the initial weight of the substrate, W_2 is the weight after the anodization, T is the thickness of porous Si film, S is the area of the cell and d is the density of silicon.

3.9 Factors Influencing Porous Silicon Properties

The primary input factors that determine the properties of the porous silicon material that results from the anodization process are substrate type and doping concentration, current density and electrolyte composition, and the illumination condition.

Substrate doping

The inter-pore spacing and the pore diameter are expected to be on the same order as the space charge region width W_{dep} [44]. The space charge region W_{dep} in the semiconductor decreases by increasing the doping concentration of the Si substrate, and vice versa. For heavily doped wafers, the small space charge region results in a small pore size. For lightly doped wafers the space charge region width is large, hence the resulting pore size and porosity are high. Figure 13 shows that the porosity of material formed on p-type silicon decreases as the doping concentration increases up to $\sim 10^{19}$ cm^{-3}, while the porosity of material formed on n-type silicon appears to follow an opposite trend. It is somewhat difficult to quantify the effects of doping in general because of the change in morphology at different doping levels.

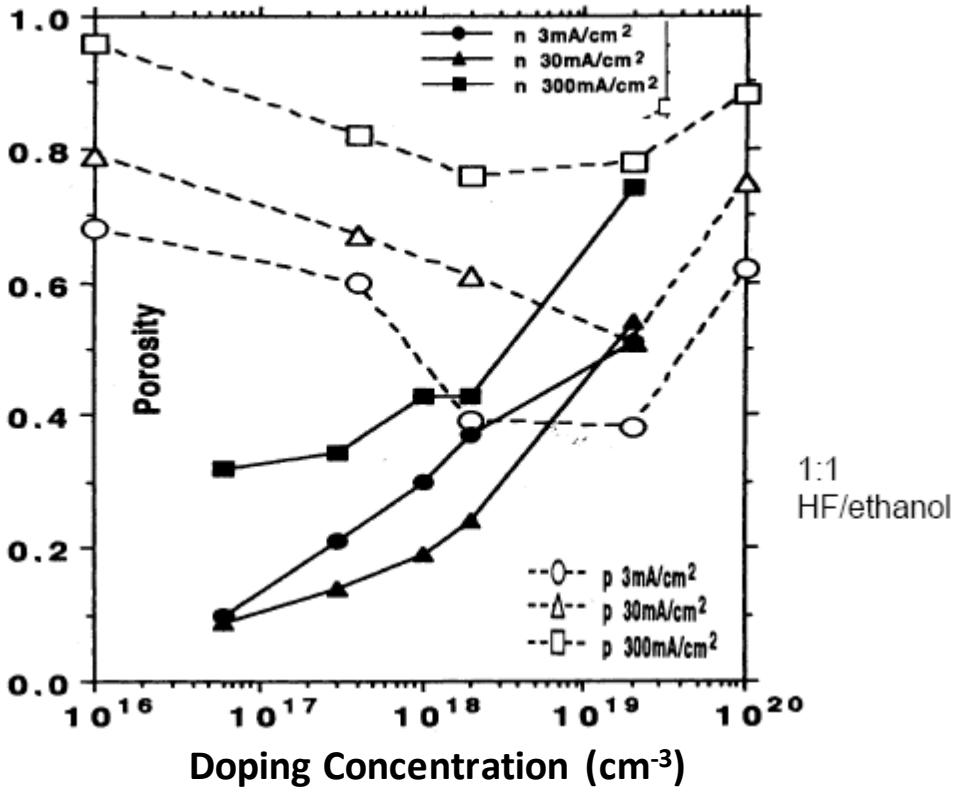


Figure 3.8: Graphical representation of relationship between porosity and doping concentration over variations in current density [45].

Current Density & HF Concentration

It is well understood from the porous Si formation mechanisms that holes are an integral part of silicon dissolution. Hence higher current density leads to higher flux of holes which in turn leads to increased rate and amount of dissolution. With an increase in current density at a given HF concentration and substrate resistivity, there is a corresponding increase in the porosity as shown in the graph in Figure 3.9. An increase in current density also increases the diameter of the pores. Note that this trend is relatively consistent in the formation of porous silicon on p-type material; the graph in Figure 3.8 shows n-type formation results that do not follow this relationship.

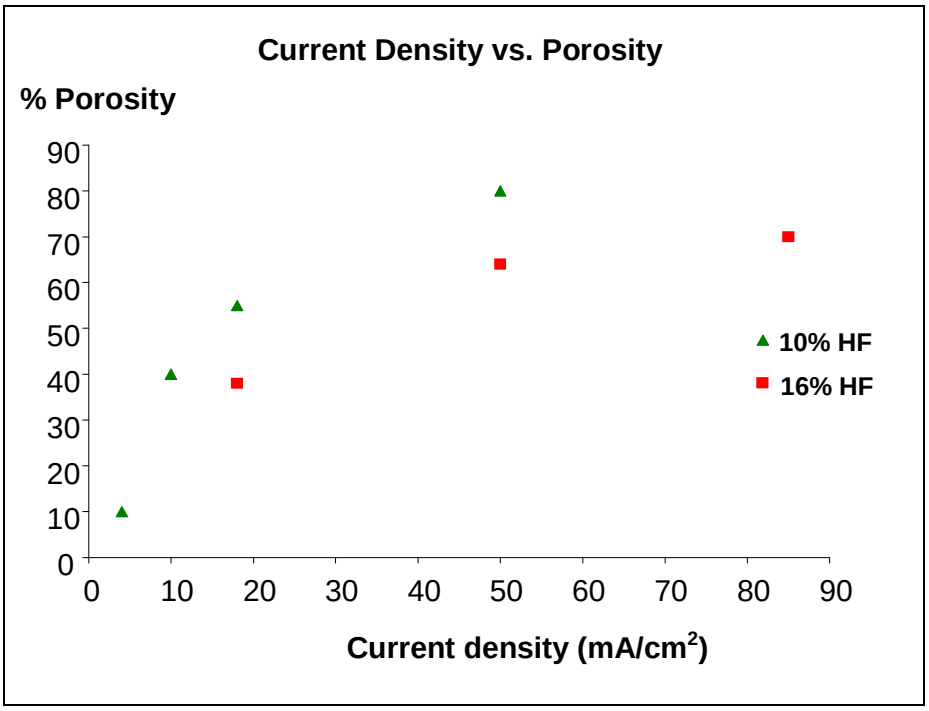


Figure 3.9: A scatter plot representation of porous Si etching data with current density on x-axis and gravimetric porosity on y-axis at different levels of HF concentrations.

Figure 3.9 also shows an inverse relationship between HF concentration and the resulting porosity of the anodized film. The critical current density, J_{crit}, is a function of HF concentration; as the HF concentration increases, J_{crit} decreases leading to faster dissolution reaction. While this trend is clearly not intuitive, the increase in dissolution results in both increasing pore size and pore spacing, and ultimately results in a lower porosity material.

Table 3.1 summarizes the influence an increase in the doping concentration (N_A), the HF concentration, and the current density (J) on the porosity (p) following the anodization of p-type silicon.

Table 3.1: Factors and their effects on porous silicon properties with formation on p-type material without illumination.

Factor	Porosity	Comments
Doping Conc. N_A ↑	↓	Complex relationship due to change in morphology with doping concentration.
Current Density J ↑	↑	Higher current density leads to mesopore formation.
HF Conc. ↑	↓	High HF conc. with low doping leads to macropore formation.

Illumination Condition

Illumination is a major factor in many electrochemical reactions. Illumination generates electron-hole pairs in the semiconductor, which are generally distributed across the substrate. The electron-hole pairs within the bulk undergo recombination; however the electron-hole pairs may be separated by an electric field that is either built-in (as in a p-n junction) or applied. If the minority carrier lifetime is high (microseconds) then the carriers can travel large distances in the semiconductor before recombination. The graphs in

Figure **3.10** and Figure 3.11 show representative current-voltage (I-V) characteristics recorded during the anodization process both with and without backside illumination on n-type and p-type silicon, respectively. Illumination is required for porous silicon formation on lightly doped n-type material, and

Figure **3.10** shows a significant increase in current density at low bias conditions with the assistance of backside illumination. While not required for the formation of porous silicon on p-type material, backside illumination can be used to facilitate a low-resistance backside contact without the use of degenerate doping or metallization. A

decrease in the voltage drop during the anodization of a lightly doped p-type substrate using a liquid electrolyte backside contact is shown in Figure 3.11.

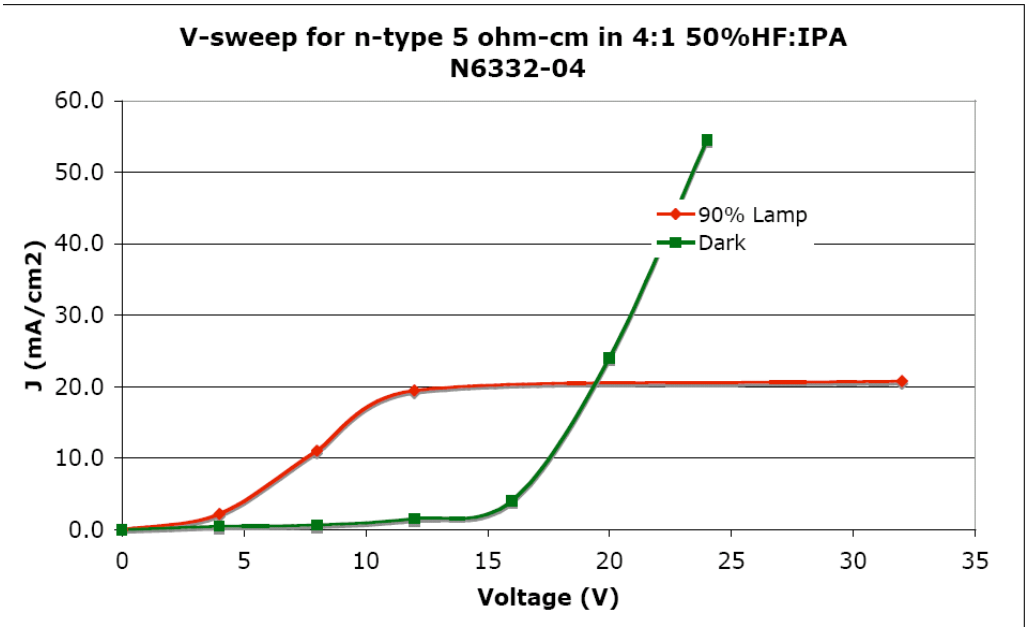


Figure 3.10: Representation of current-voltage characteristics on an n-type substrate collected during anodization, both in dark (square markers) and with backside illumination.

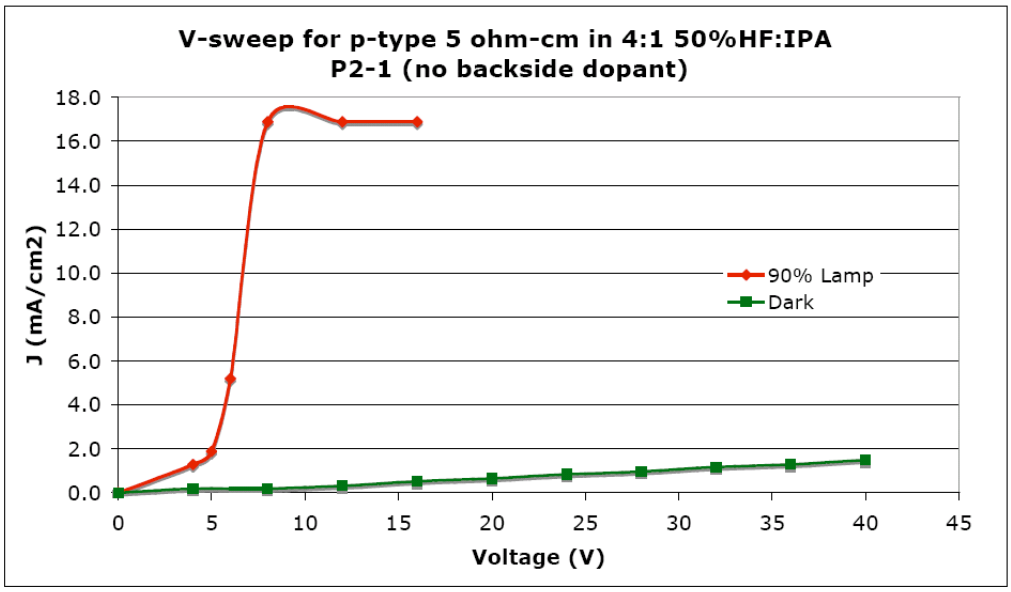


Figure 3.11: Representation of current-voltage characteristics on a p-type substrate collected during anodization, both in dark (square markers) and with backside illumination.

Chapter 4: *SILICON ON INSULATOR TECHNOLOGY*

This chapter reviews the basics of various Silicon-on-Insulator (SOI) technologies along with their merits and demerits. A localized SOI (L-SOI) technology known as FIPOS is also discussed. This chapter will describe a new technique based on this L-SOI technology, which is the focus of this study.

4.1 Conventional Bulk MOSFET vs. SOI based MOSFET

In bulk silicon based devices, subsurface leakage currents are an inherent problem. There is significant current flow below the surface during the off state of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) leading to power loss. However, an SOI wafer has a thick Buried Oxide (BOX) layer formed in the silicon substrate that can eliminate the leakage path underneath the devices. If the silicon layer in an SOI substrate is thick, devices fabricated on the substrate behave like bulk MOSFET's. The thinner the silicon is, the less the sub-surface leakage [47, 48]. Subsurface leakage currents in the case of SOI can be reduced without sacrificing on-current characteristics of the transistors by optimizing the silicon thickness.

SOI can be broadly classified into three types: partially depleted, fully depleted and ultra thin body. A partially depleted SOI device has a depletion region that does not come in contact with the buried oxide [49] as shown in

Figure **4.1**a. Even though this partially depleted SOI is similar to the bulk in terms of leakage, the junction capacitance is lower as it is in series with the buried oxide

capacitance. Therefore, the partially depleted SOI is very beneficial for high performance applications. This type of SOI has been used in the integrated circuit industry for many years. However, recent trends have been moving toward fully depleted SOI.

A fully depleted SOI [48] occurs when the depletion region reaches the buried oxide region as shown in

Figure **4.1**b. This greatly reduces the leakage as discussed above, and leads to very good control over subthreshold swing, approaching the 60 mV/decade limit. An ultra thin body SOI [49] has a body that is so thin that there is hardly any depletion region, only an inversion region, thus ultimate control over leakage can be obtained. Even doping in the channel is not needed, which can reduce statistical fluctuations on threshold voltage (V_T) and improve mobility in the channel.

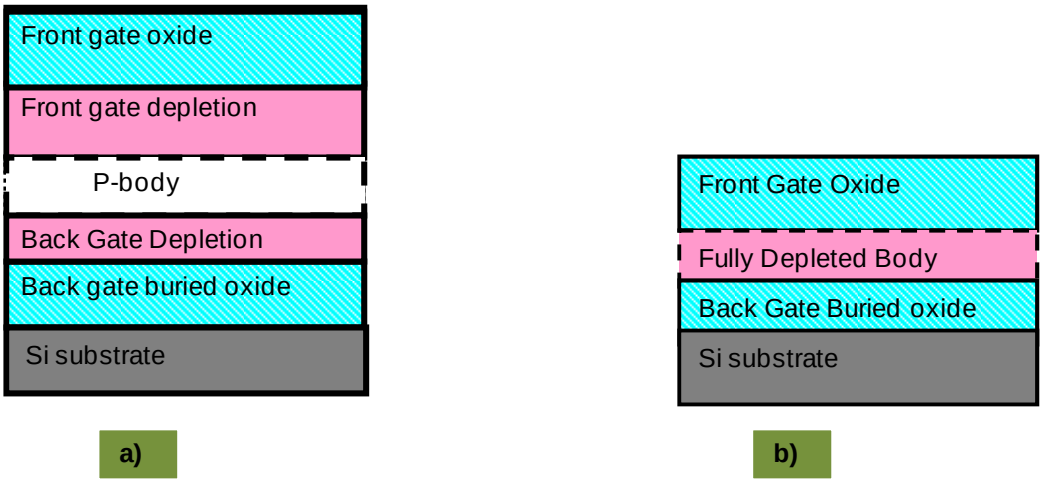


Figure 4.1: A block diagram of a Partially depleted and fully depleted SOI substrate a) Represents partially depleted SOI substrate with gate oxide and back gate buried oxide regions leading to front and back gate depletion regions b) Represents fully depleted SOI substrate with a front and buried oxide regions and a fully depleted body.

4.2 Development of SOI Based Substrates

SIMOX (Separation by Implantation of Oxygen)

Separation by Implantation of Oxygen (SIMOX) [52] is one of the very first techniques that was used for SOI formation. The main goal of the SIMOX approach is to have a thin silicon layer about 0.1 to 0.2 microns and a SiO_2 layer thick enough to withstand leakage as shown in

Figure **4.2**. A high dose of oxygen ions is implanted into a heated silicon substrate to avoid amorphization of the surface. The substrate is annealed at temperatures close to 1300^{o}C so that oxygen in the interstitial sites reacts with silicon and form nearly stoichiometric SiO_2. This results in the formation of a BOX layer as shown in

Figure **4.2**.

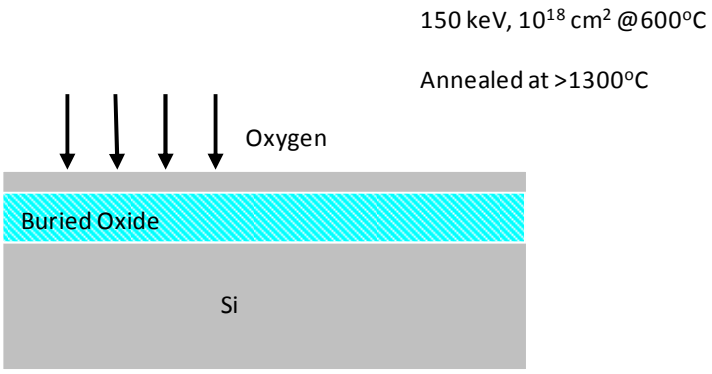


Figure 4.2: Block diagram representation of a SOI substrate manufactured using SIMOX technology. It shows a buried oxide region formed through implantation of oxygen at high concentration and annealing at temperatures greater than 1300^{o}C.

Smart Cut (SOITEC), Unibond

The principle behind wafer bonding is that two silicon wafers (a handle wafer and a donor wafer) can be oxidized and bonded together under high temperature [51] as shown in Figure 4.3a. A strong covalent bond is formed between the oxidized wafers, and the donor wafer is removed using a lapping and etch process shown in Figure 4.3b. The problem with this approach is that it is difficult to obtain a thin Si layer due to the lack of an etch stop.

The key innovation from SOITECH [51, 52] in using this bonding technique is the implantation of the donor wafer with a very high dose of hydrogen as shown in Figure 4.4a. As the handle wafer and donor wafer are bonded at a high temperature, a strong covalent bond is formed between both of the SiO_2 layers. All the hydrogen agglomerates to form a distinct layer as shown in the Figure 4.4b, and the wafers separate due to the induced stress, as shown in Figure 4.4c. The advantage of this process is that by optimizing the hydrogen implant profiles a very thin silicon layer can be realized, and the donor wafer can be used multiple times for a cost savings. This has become the industry standard for SOI because the quality of the interface is excellent, and the silicon thickness can be controlled.

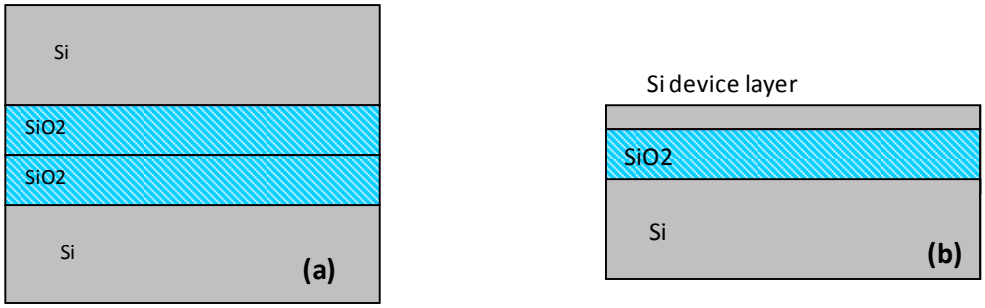


Figure 4.3: Representations of the basic principles of UNIBOND process. a) Two oxidized silicon wafers attached together for bonding. b) High temperature bonding and donor wafer removal leaving behind a layer of silicon.

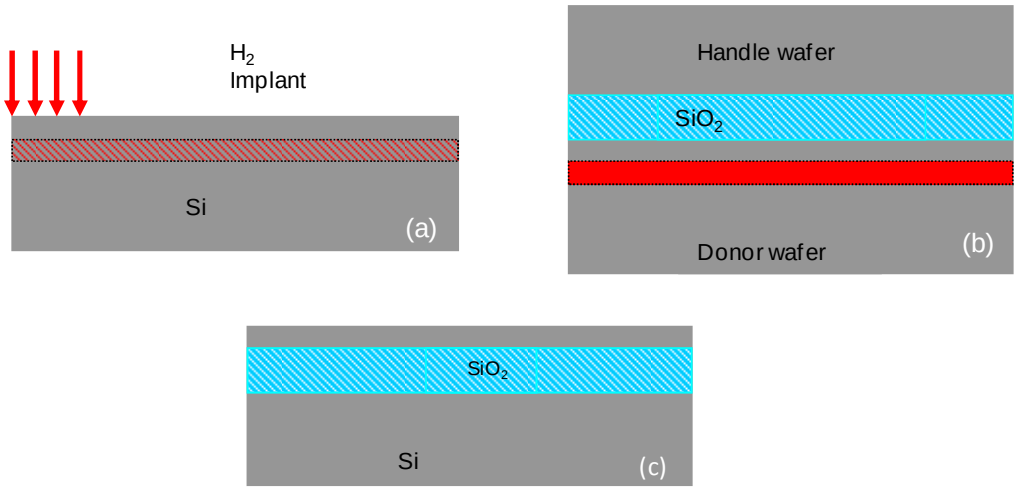


Figure 4.4: Representation of basic principles of the Soitec process. a) Silicon wafer implanted with hydrogen species. b) Wafer implanted with hydrogen and with oxide grown on the substrate is covalently bonded to another wafer with oxide in the front. c) SOI substrates after covalent bonding and exfoliation layer transfer.

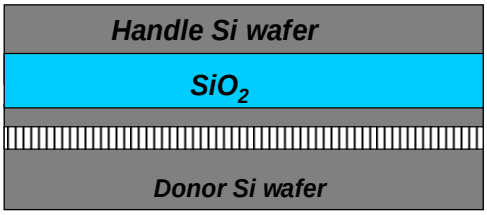
4.3 SOI Substrates using Porous Silicon (Canon ELTRAN)

For SOI substrate fabrication, a commercial process was developed by Canon, known as ELTRAN [53] as shown in Figure 4.5. This process is similar to the SOITEC smart cut process, except that the donor wafer utilizes a high quality epitaxial silicon layer grown on a porous silicon bilayer consisting of a low porosity surface layer and a

high porosity bottom layer. The epitaxial silicon layer is bonded to the oxidized handle wafer, and the layer transfer is performed using a water jet to fracture the high porosity layer. Similar to the smart cut process, the donor wafer can be used repeatedly to lower production costs. Although this technique demonstrated high quality SOI substrates, it is no longer in manufacturing due to the inability to compete with the smart cut process.

(A) Epitaxial silicon transfer layer grown on porous silicon

(B) Bonding of epitaxial layer to oxidized handle wafer



(C) Water-Jet Exfoliation and Surface Polish

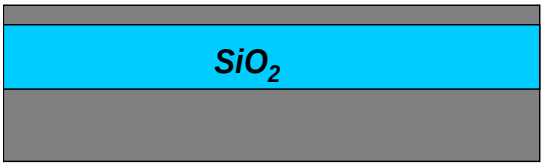


Figure 4.5: Block diagram representation of basic principles of Eltran process which uses a porous silicon release layer used for wafer-jet separation.

4.4 Development of Localized SOI Technology

A localized SOI technology may have advantages in applications which use both the bulk wafer and SOI regions for electrical and optoelectronic devices. Doping concentration can be used to enhance or suppress the formation of porous silicon, as shown in Figure 4.6. However the addition of dopants may present process integration challenges or unwanted effects. The use of proton implantation into p-type silicon was shown to behave as a reversible donor species and was successful in forming localized SOI structures for CMOS devices that demonstrated superior performance compared to their bulk silicon counterparts [2]. The proton implanted regions exhibited n-type behavior upon annealing at low temperature (T = 450 °C), and effectively suppressed the formation of porous silicon which requires hole carriers. The donor properties were subsequently removed upon annealing at temperatures above 700 °C, with the resistivity of the isolated silicon regions consistent with the low boron concentration starting p-type wafer. However, limitations with this technique include the lack of availability of a low-energy H^+ implant capability, and the difficulty in obtaining a proton distribution needed to support the formation of a thin (<0.5 μm) isolated silicon layer. In addition, an artifact of this technique is the formation of a silicon anchor beneath the SOI layer, shown in Figure 4.7.

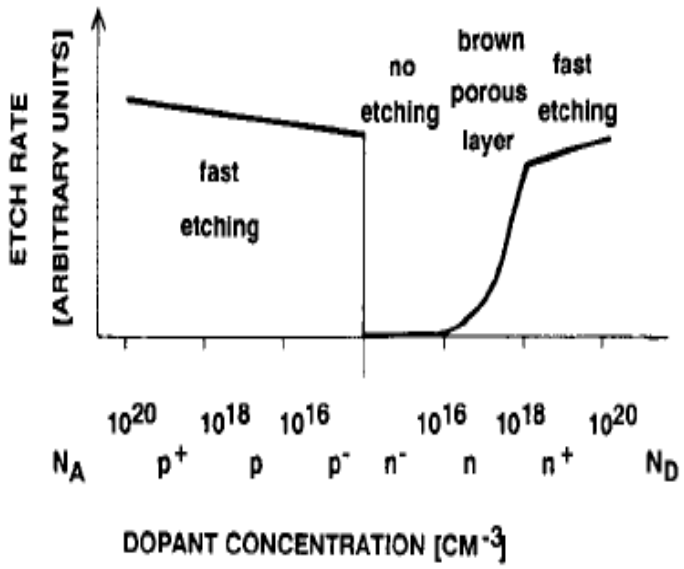


Figure 4.6: Selective etching representation at different doping concentration on x-axis and etch rate on the y-axis. Ref Eijkel et al [54]

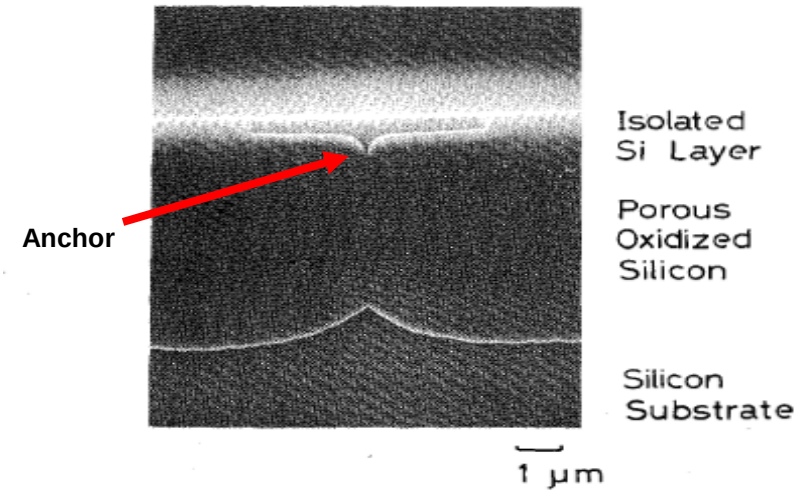


Figure 4.7: The formation of a FIPOS isolated silicon region, with an anchor formed as the porous silicon regions merge beneath the structure. Ref: Kazuo Imai [55].

It was recently discovered that a high dose fluorine implantation also demonstrates donor-like behavior when annealed at 600 °C. This study investigates the use of implanting fluorine to create a reversible donor species for the selective

suppression of porous silicon formation. This effect is represented by the spreading resistance profile data shown in Figure 4.8. The spreading resistance profile was done on a p-type substrate with high dose fluorine ($^{19}F^{+}$) implant, and annealed at 600 °C for 2hrs. The hole-depleted surface region is related to the presence of fluorine and/or fluorine-related defects that are stable at the annealing temperature. Once discovered, it was thought that this technique might addresses certain limitations of the proton strategy; F^{+} ions are produced in standard implant systems for boron that use BF_3 as the source gas, and the higher mass (19 amu) enables a shallow implanted distribution for thin SOI layer formation.

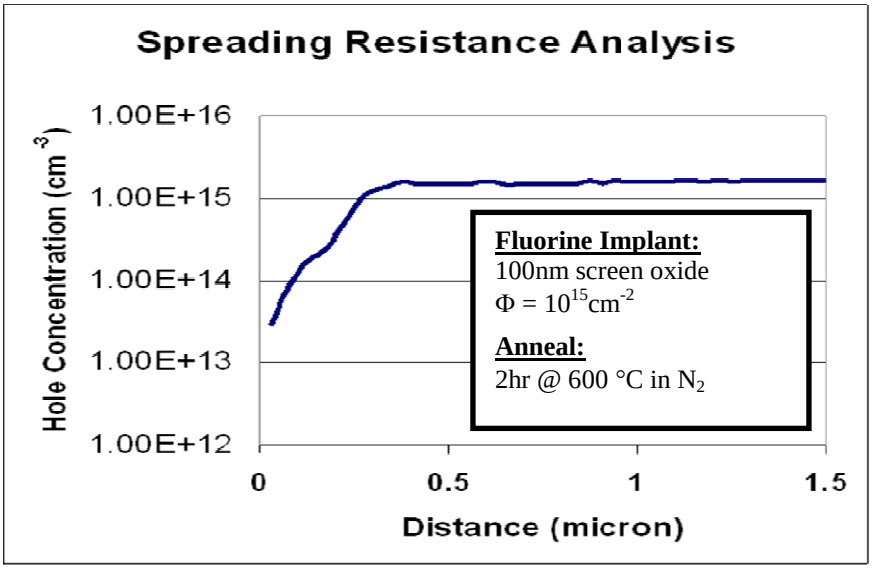


Figure 4.8: Spreading resistance profile of a fluorine implanted and annealed sample, showing the hole depletion effect in the surface region that is related to the presence of fluorine and/or fluorine related defects.

4.5 Feasibility Investigation

An experiment was planned to test the effect of fluorine on the anodization process. A p-type substrate was implanted with a very high dose of fluorine ($\Phi = 3x10^{15}cm^{-2}$). Half of the wafer was then blocked with photoresist, and a boron implant was done to compensate for this donor effect and replenish the surface region with hole carriers. The wafer was subjected to a low temperature anneal (2 hours at 600 °C in N_2) followed by an anodization process for porous silicon formation on both halves of the sample. Figure 27 shows SEM images of each half of the sample, with uniform formation of porous silicon in regions without the fluorine implant, and periodic porous silicon formation in regions with the fluorine implant. Note that there was no masking layer (e.g. Si_3N_4) for the anodization process, allowing the formation of porous silicon on top of the crystalline silicon areas (

Figure **4.9**a). This periodic formation is a result of forced current that becomes self-localized, with injected holes available for porous silicon formation at a regular spacing.

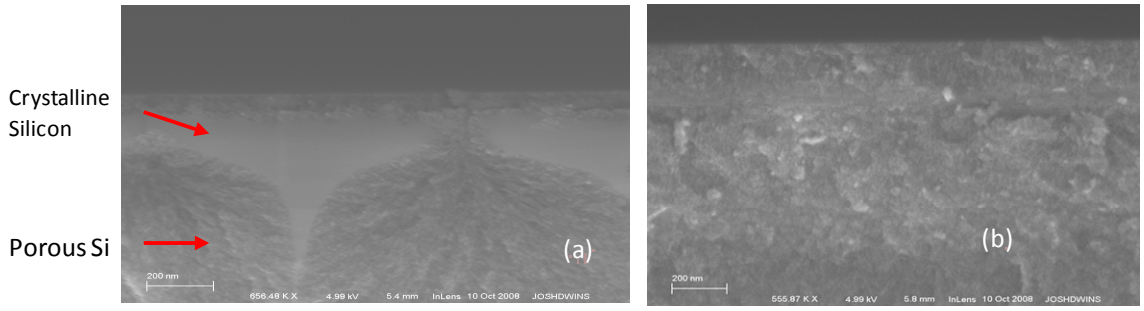


Figure 4.9: Representation of the SEM cross-sectional view of the substrate taken after anodization process. a) P-type substrate with high dose fluorine implant leading to isolated silicon regions formed in a periodic fashion. b) P-type substrate with both fluorine and boron implants leading to porous Si formation.

The anchor feature that was observed in

Figure **4.9**a is similar to that previously reported in the FIPOS process [39], and is the result of hole carrier depletion as the porous silicon regions become close.

Figure **4.9**b represents the part of the wafer where both fluorine and boron were implanted. Due to fluorine preamorphization, boron is activated very effectively at 600 °C [59]. As a result, a continuous porous silicon layer is formed. These results have lead towards the L-SOI integration scheme, where the fluorine-only implanted areas represent the active device regions, and the regions that were implanted with both fluorine and boron represent the field isolation regions. This will be described in Chapter 5: following the discussion on screening experiments.

4.6 Localized SOI Screening Experiments

Several screening experiments (i.e. one factor at a time, large factor setting increments) were designed in order to determine an appropriate strategy for L-SOI regions using fluorine as the primary mechanism for selective suppression of porous silicon. As part of the survey, fluorine was implanted at different energies and dose into silicon substrate with 1000 Å SiO_2 as a screening layer to suppress implant channeling and adjust the peak of the implanted profile. The implant distributions were modeled using SRIM (Stopping and Range of Ions in Matter) simulation software [60]. SRIM is a vital tool to model implant damage and ion range as a function of the energy of the implant, as shown in Figure 4.10**.** Initial treatment combination results shown in

Figure **4.9** suggested that the fluorine implant must provide a dose in excess of $10^{15}cm^{-2}$, at an energy of around 100 keV or higher for the suppression effect to be successful.

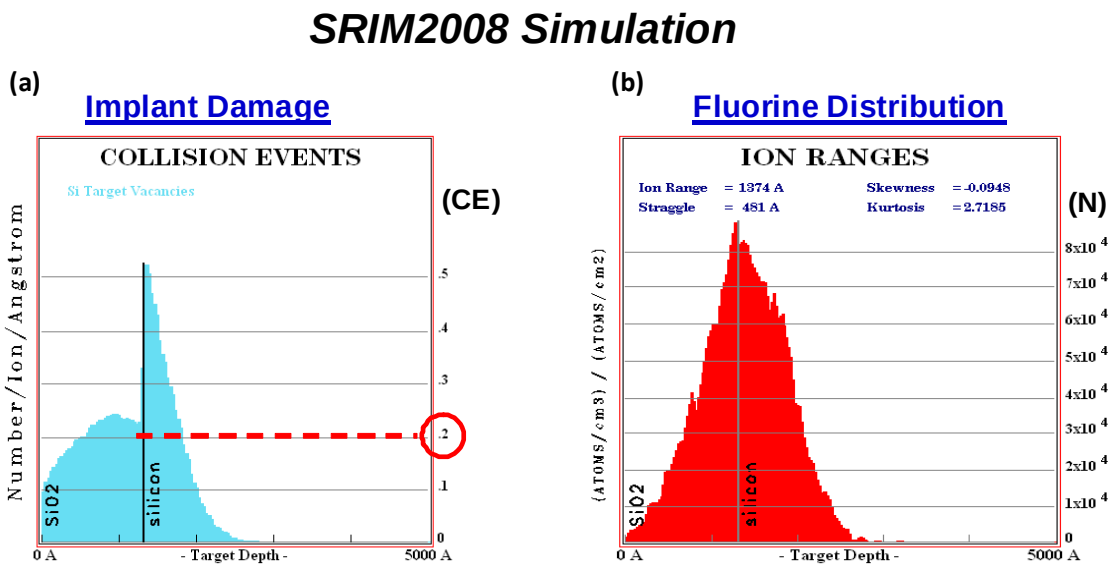


Figure 4.10: SRIM simulation done on a fluorine implant at 100keV. a) Implant damage events showing high damage near the silicon surface, ensuring continuous amorphization. A collision event level of 0.2 corresponds to a displacement concentration required for amorphization, assuming a dose of ~ $10^{15}cm^{-2}$. b) Fluorine ion distribution (linear scale).

The experimental results show a lack of suppression using a fluorine dose below the dose required to amorphize, as well as an energy that would prevent a significant portion of the dose from entering the silicon through the screen oxide. This confirms the dependence of suppression on the fluorine dose, and suggests that the operative mechanism is due to the formation of specific fluorine-silicon defects that arise from a solid-phase epitaxy regrowth process, are stable at 600 °C, and have donor-like behavior (hole depletion).

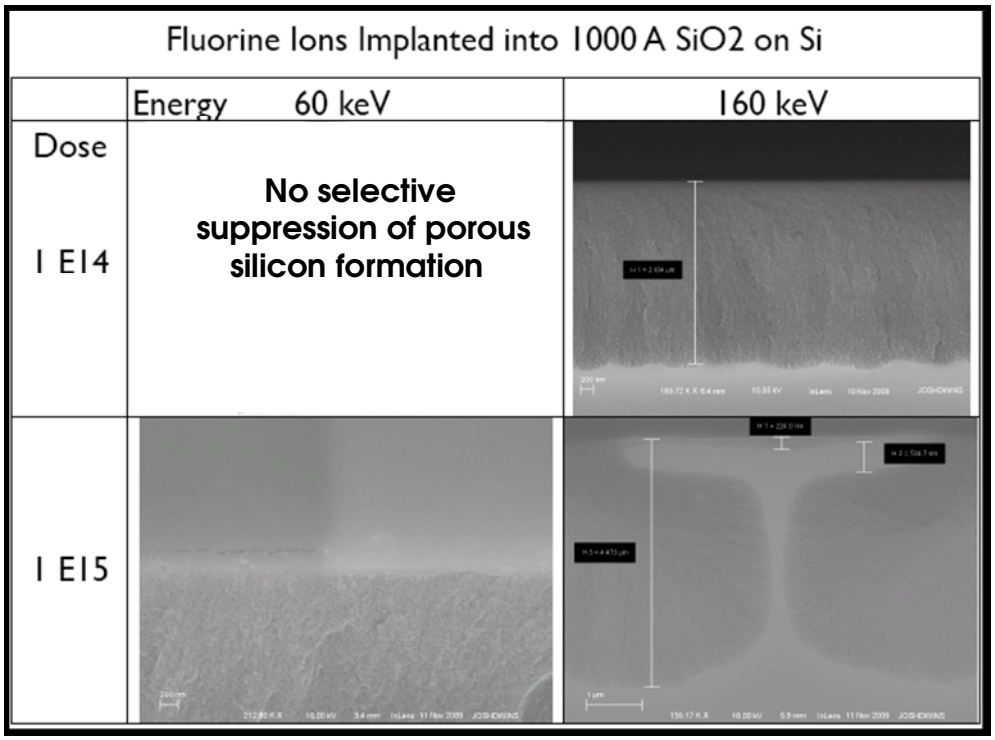


Figure 4.11: Cross sectional view of anodized substrates implanted with fluorine through a 100 nm SiO_2 layer at different energy-dose combinations prior to anodization. Only the high dose / high energy combination result in the selective suppression needed for localized SOI. Note the anchor feature which connects the silicon surface region to the bulk.

These preliminary results led to a more focused set of experiments for an integrated L-SOI process. Chapter 5: describes these experiments which explore the significance of several input parameters, and which lead towards a practical integration scheme for device applications.

Chapter 5: PROCESS INTEGRATION FOR LOCALIZED SOI

Several details were considered in the development of a process sequence for integrated device applications. The basic sequence that was employed involved field and active region preparation, electrochemical formation of porous silicon, and oxidation of porous silicon for isolation regions. Each of these process areas contained input variables that were further explored in a series of experiments. Results from these experiments were then used for the fabrication of integrated device structures discussed in Chapter 6:.

5.1 Localized SOI Process Sequence

Initial Substrate Preparation

Figure 5.1 shows the step-by-step procedure in forming localized SOI structures. The starting substrate is a p-type silicon wafer with a resistivity of 5-15 Ω-cm. A 50 nm screen oxide is grown, and a blanket (non-patterned) low-dose high-energy boron implant is done to produce a buried layer (Figure 5.1a) which is activated at high temperature (1000 °C). This p-type buried layer serves three purposes; to promote lateral formation of porous silicon beneath active regions, to provide SOI thickness control and uniformity, and to avoid the anchor structure observed because of fully depleted silicon in between the porous silicon formation fronts as seen in Error! Reference source not found.Error! Reference source not found.. The screen oxide is then replaced with a silicon nitride layer deposited via LPCVD, which will eventually serve as a masking layer for the active regions during the porous silicon formation process. A blanket high-dose / high-energy fluorine implant is then done through this nitride layer (Figure 5.1b), which effectively amorphizes the surface region.

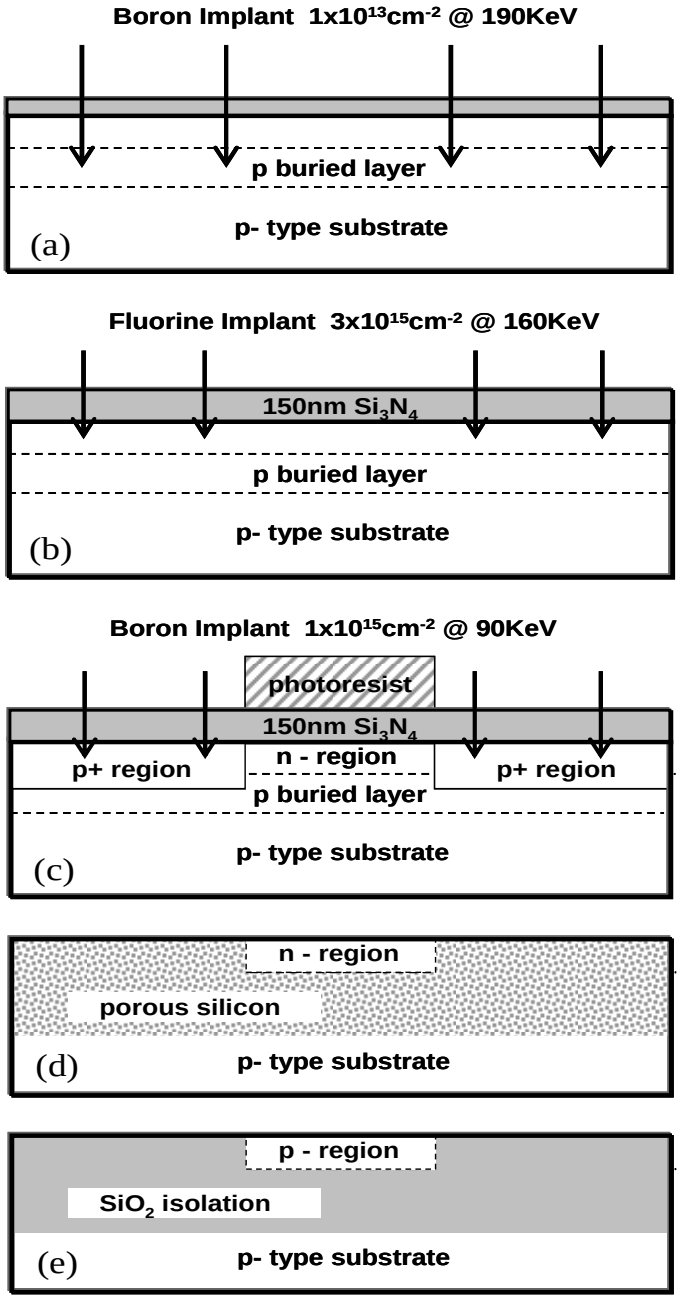


Figure 5.1: Process sequence for the fabrication of fully isolated crystalline silicon regions, using fluorine for suppression of electrochemical formation of PSi. See text for description.

Active lithography (clear-field) is then done to pattern the nitride layer, and a high dose boron field implant is done in the isolation regions (Figure 5.1c) prior to the nitride etch. The nitride is etched via RIE, leaving some remaining nitride to avoid etching into

the silicon substrate in order to ensure planar topology. Note that this remaining nitride is removed in the electrolyte immediately prior to the formation of porous silicon. Photoresist is then removed, followed by substrate cleaning and annealing at 600 °C in N_2 for 2 hrs. This provides partial restoration of the silicon lattice, resulting in fluorine-induced n-type regions in the active areas, and nearly full activation of the boron in the p+ isolation regions due to the solid phase epitaxy regrowth process [59]. An aluminum layer was sputter deposited on the backside of the wafers, and sintered at 450 °C to ensure an ohmic backside contact for the electrochemical process.

Formation of Porous Silicon

A specially designed electrochemical etching cell was used for full-wafer substrates. The apparatus is shown in

Figure **3.4**. The cell uses an aluminum disk for contact to the aluminum coated backside of the wafer, a platinum foil for the working cathode, and o-ring seals to ensure chemical (and electrical) isolation between each side of the wafer. The cell is completely closed during etching, except for a small port that allows for H_2 to escape, and anodization takes place in complete darkness. The exposed area of the wafer surface is 38.5cm².

The initial porous silicon layer must be able to provide a stable film that can withstand stress induced by thermal oxidation due to volume expansion of the oxide. A silicon layer with a porosity of 56% (void space) will essentially have no volume expansion when subjected to oxidation. A film porosity between 45% and 55% was initially targeted to allow for a small amount of volume expansion in order to avoid oxide

voids, which would also compensates for some field isolation loss during oxide removal over the active regions.

Electrochemical etching is then done to form porous Si throughout the interconnected p-type regions using an appropriate HF/IPA mixture at a constant voltage (Figure 5.1d). LabView™ was used to interface a computer with a Keithley power supply used for the anodization process, allowing for precise process control and real time data collection. Using a constant voltage process, a current vs. time plot was used as an endpoint detection technique. As the porous silicon etch front reaches the underlying bulk region below the p-type buried region, the current level decreases and eventually stabilize as shown in the Figure 5.2.

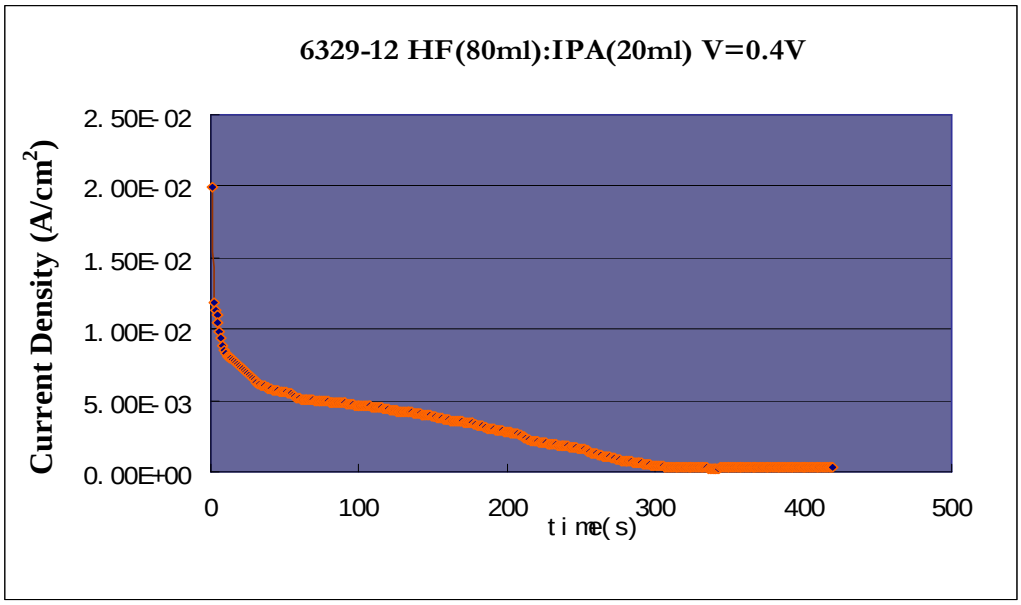


Figure 5.2: Current Density vs. Time plot collected real time during constant-voltage anodization at 0.4V, where the endpoint at around 300 sec corresponds to the point at which the porous silicon etch front has surpassed the p-buried region.

Oxidation of Porous Silicon

Prior to oxidation, the aluminum film on the backside was removed using a chlorine plasma, and a decontamination clean in a heated $HCl/H_2O_2/H_2O$ mixture was done to remove any metal contaminants. The oxidation involved a multistep thermal process [56, 57], which included 300°C for 1 hr in dry O_2 for pore stabilization (prevents pore collapse), 1000 °C for 1 hr in O_2 for full oxidation of the field isolation regions, and an inert anneal at 1100 °C for 4 hours in N_2. This process completely oxidizes the porous Si regions, removes fluorine, restores the crystalline silicon islands back to the original p-type resistivity (see Figure 5.1e), and promotes high quality oxide/silicon interfaces. The described process produces isolated silicon regions that are approximately 150 nm thick and are surrounded by a thick SiO_2 isolation region as shown in

Figure **5.3**.

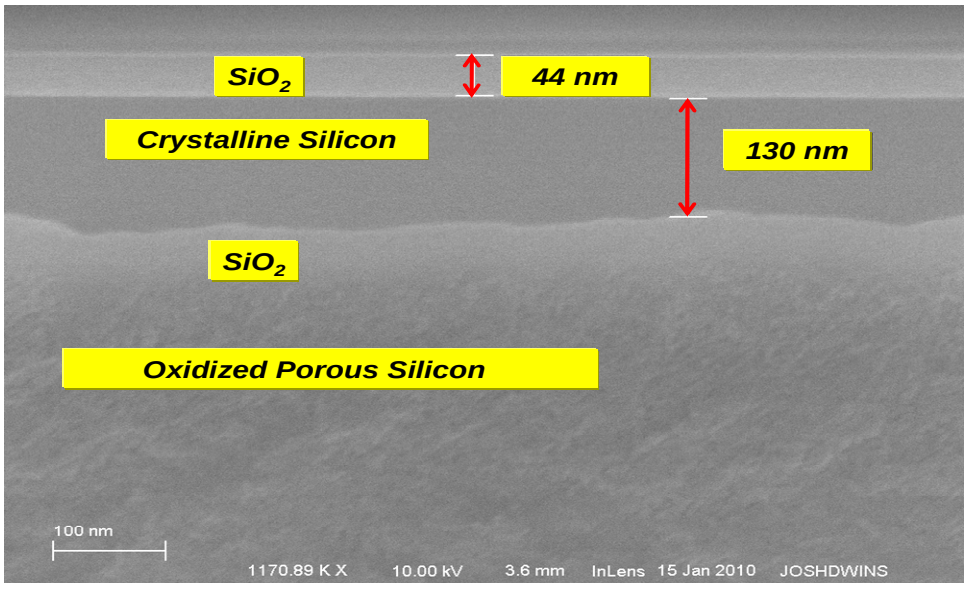


Figure 5.3: SEM cross-section view of an L-SOI structure following oxidation. The silicon layer is approximately 130 nm thick above a thick oxidized porous silicon layer. The image also shows void-free thermally oxidized SiO_2 layers both above and beneath the silicon layer.

5.2 Process Integration Experiments

The initial set of experiments demonstrated that localized SOI structures could be fabricated using the integrated process sequence. A second set of experiments was used to further refine the process for integrated device applications. Treatment combinations identified in Table 5.1 were prepared using the described process sequence, with specific parameter setting adjustments or alterations in the process to further investigate the effects or importance of input factors. This set of experiments was focused on process integration prior to the oxidation of the isolation regions.

Table 5.1: Treatment combinations for a focused investigation on process integration prior to oxidation of the isolation regions. The sample identification used during the actual experiment has been maintained.

Sample	***F^+ implant***	***P+ implant***	***Nitride RIE***	***Pre-Anneal***
A	YES	YES	underetch	600°C 2hr
C	YES	NO	overetch	600°C 2hr
D	NO	YES	underetch	800°C 1hr
E	YES	YES	underetch	800°C 1hr
F	LAST	YES	underetch	NONE
G	NO	NO	overetch	NONE

The factors investigated were the F^+ implant, the p+ field implant, the nitride RIE process, and the pre-anneal process immediately prior to anodization. All samples were processed with a high-energy boron implanted buried layer, which was activated at high temperature. Silicon nitride was deposited as an etch mask against porous silicon formation. The blanket F^+ implant ($\Phi = 3x10^{15}cm^{-2}$) was done through the nitride mask before patterning on samples A, C and E. Samples D and G did not receive the F^+

implant. Sample F (LAST) received the F^+ implant after the nitride pattern and etch processes, immediately prior to anodization without any subsequent anneal.

The boron p+ implant was done following the active region lithography on all samples except C and G. This implant was then activated during the "pre-anneal" process, which was kept at or below 800 °C to ensure stability of the fluorine-induced donor effect. Note that sample F was annealed at a higher temperature (1000 °C) due to the fact that there was no fluorine introduced into this sample until after this activation process. The "pre-anneal" condition for sample F is listed as NONE, meaning that there was no anneal following the F+ implant prior to the anodization process.

The influence of the nitride RIE process for the nitride masking layer was investigated, with the "underetch" representing the case where there was remaining nitride over the silicon, avoiding etching into the silicon surface and maintaining a planar topology. The "overetch" condition allowed the RIE to extend some distance into the silicon surface. This factor was investigated in order to determine the influence of surface topology on the resulting L-SOI structure.

All samples were prepared with boron p+ backside implants (done at the start) and a sintered aluminum backside contact. Anodization was done using a 4:1 49%HF:IPA mixture at a constant voltage of ~0.9V, raising the current density to approximately $10mA/cm^2$ to target a porosity closer to 60%. This was due to global sample deformation observed from wafer bow measurements taken on the initial screening experiments, indicating that the amount of volume expansion of the isolation regions during oxidation was too high. Scanning electron micrographs were then taken on each sample, with results and observations now discussed. Note that the sample order

in which the results are presented was chosen to maintain continuity and consistency in the discussion.

Sample G

The treatment combination for sample G was as follows: Without F^+ implant, no p+ field implant, nitride RIE overetch, and no pre-anneal. The SEM image is shown in Figure **5.4**.

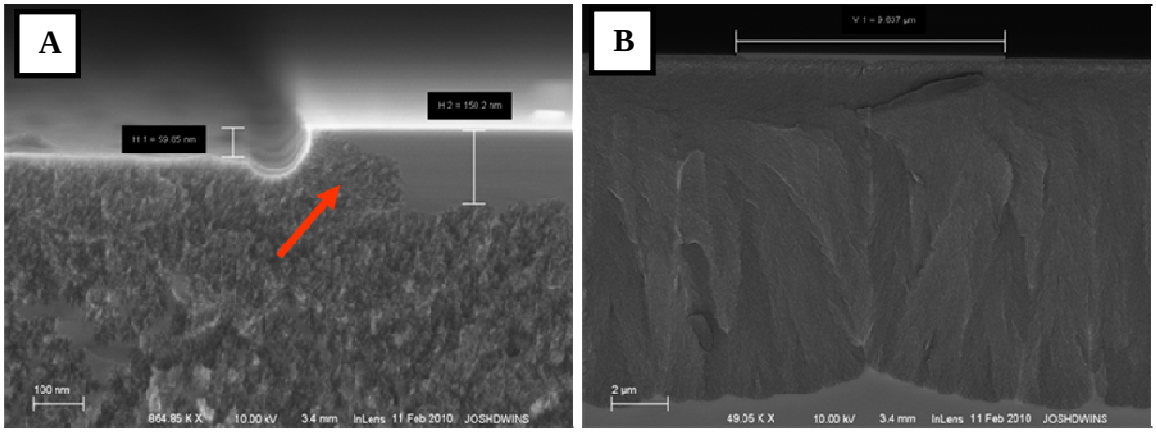


Figure 5.4: SEM cross-sections of sample G at high magnification (A) and low magnification (B). The arrow points to the lateral encroachment of porous silicon into the active region, initiating from the non-planar edge feature created from the nitride overetch into the silicon surface. The isolation region extends approximately 13 microns deep, with etch fronts that meet in the middle beneath the active region, shown in (B).

The result shown in Figure **5.4** is quite interesting, due to the fact that Sample G does indeed demonstrate selectivity in porous silicon formation without the use of fluorine, and results in the formation of isolated silicon regions. The formation of porous silicon begins in an isotropic fashion, as evidenced by the active region encroachment of ~ 200

nm. However once the porous silicon reaches the p-buried region there is formation selectivity which is driven by the higher boron (hole) concentration in the p-buried region and the tendency for a thin lightly doped p-type region to become fully depleted of hole carriers due to surface charge at the etch front. The recessed field region due to the nitride overetch allows this condition to occur sooner, and helps to suppress the flux of hole carriers towards the surface of the active regions near the edge of the L-SOI structure. Thus lateral encroachment is suppressed; however the non-planar topology is not desirable. The thickness of the active region is only about 150 nm which is thinner than the other treatment combinations which had the F+ implant.

Sample D

The treatment combination for sample D was as follows: Without F^+ implant, with the p+ field implant, nitride RIE underetch, and a 800 °C pre-anneal. The SEM image is shown in Figure 5.5.

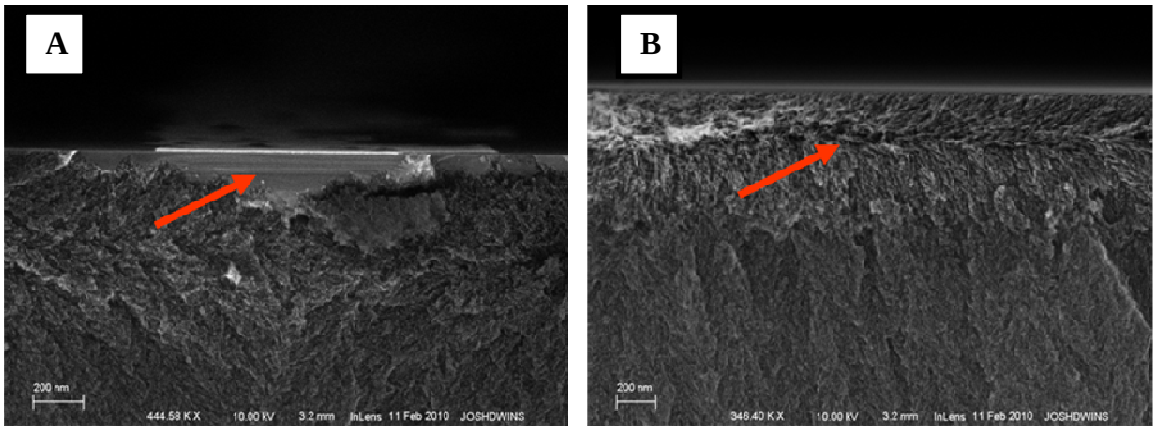


Figure 5.5: SEM cross-sections of sample D. There is relatively poor selectivity with irregularity in the isolated silicon regions (A). Porous silicon under the mask edge (above the p-buried region) appears different than in the underlying area (B).

Sample D did not have the fluorine implant, therefore the pre-anneal was done at 800 °C to ensure activation of the boron p+ field implant. Figure 5.5a shows that the structure is planar (no nitride overetch), however the selectivity is poor. Crystalline silicon regions remain, undercut by porous silicon forming preferentially in the p-buried region, however the isolated silicon structure is quite irregular. Lateral formation of porous silicon under the masked regions (Figure 5.5b) is not suppressed. Porous silicon formed under the mask edge (above the p-buried region) appears different than in the underlying area, presumably due to the behavior of current vectors near the mask edge.

Sample C

The treatment combination for sample C was as follows: With F^+ implant, without the p+ field implant, nitride RIE overetch, and a 600 °C pre-anneal. The SEM image is shown in

Figure **5.6.**

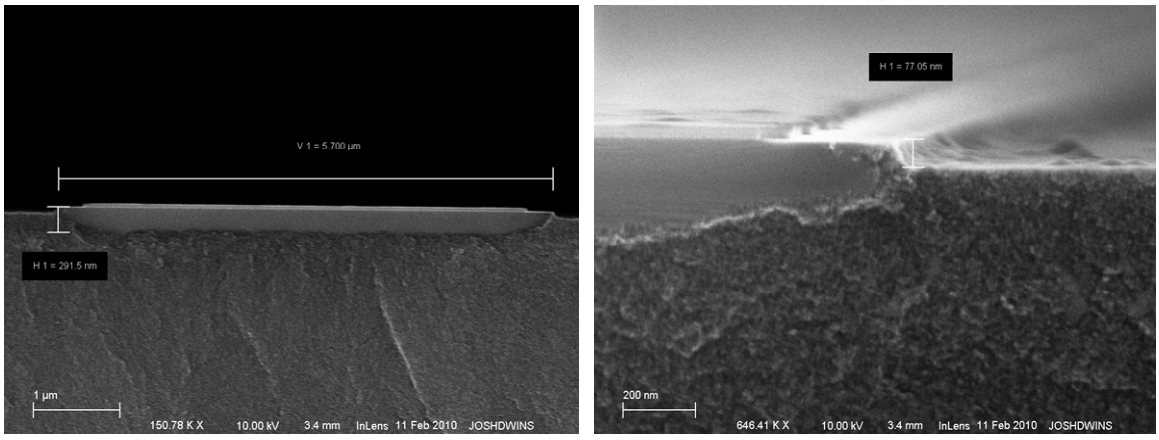


Figure 5.6: SEM cross-sections of sample C. The cross-section on the right shows erosion at the edge and surface of the isolated structure due to the lack of selectivity at the start of porous silicon formation.

While sample C has a non-planar surface topology due to the nitride mask overetch, the isolated silicon layer shows a uniform thickness of ~ 290 nm, and essentially no evidence of an anchor. There is no p+ field implant, and porous silicon appears to form on the surface and encroaches into the active region as the nitride mask erodes. The lack of selectivity at the active/field border is presumably due to the absence of the p+ field implant and the nitride overetch not reaching the p-buried layer prior to the anodization process.

Sample A

The treatment combination for sample A was as follows: With F^+ implant, with the p+ field implant, nitride RIE underetch, and a 600 °C pre-anneal. The SEM image is shown in Figure 5.7.

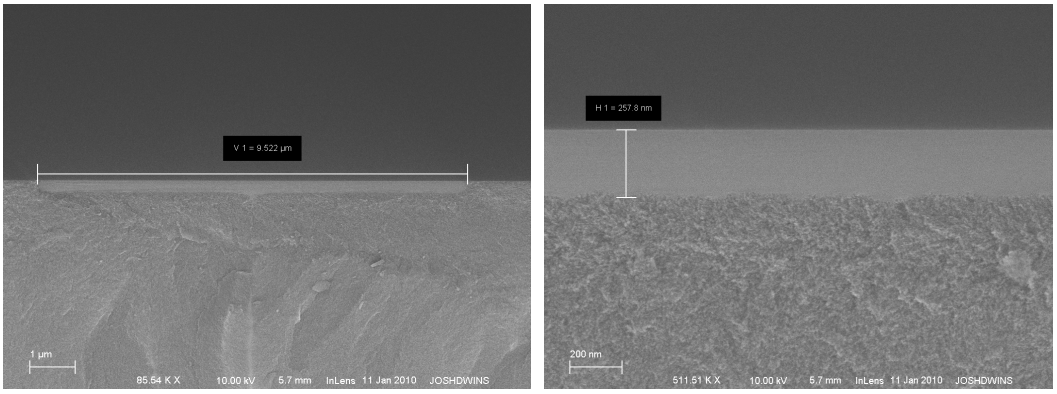


Figure 5.7: SEM cross-sections of sample A. The surface topology is planar, and the isolated silicon layer thickness is uniform with a relatively smooth interface.

Sample A appears to overcome the shortcomings of sample C. The nitride underetch promotes a planar surface topography, and the p+ field implant promotes

etching selectivity and allows the formation of porous silicon to quickly reach the p-buried layer and continue laterally. This treatment combination leads to a very uniform etch with silicon thickness of about 260 nm and the suppression of anchor formation.

Sample E

The treatment combination for sample E was as follows: With F^+ implant, with the p+ field implant, nitride RIE underetch, and a 800 °C pre-anneal. The SEM image is shown in Figure 5.8.

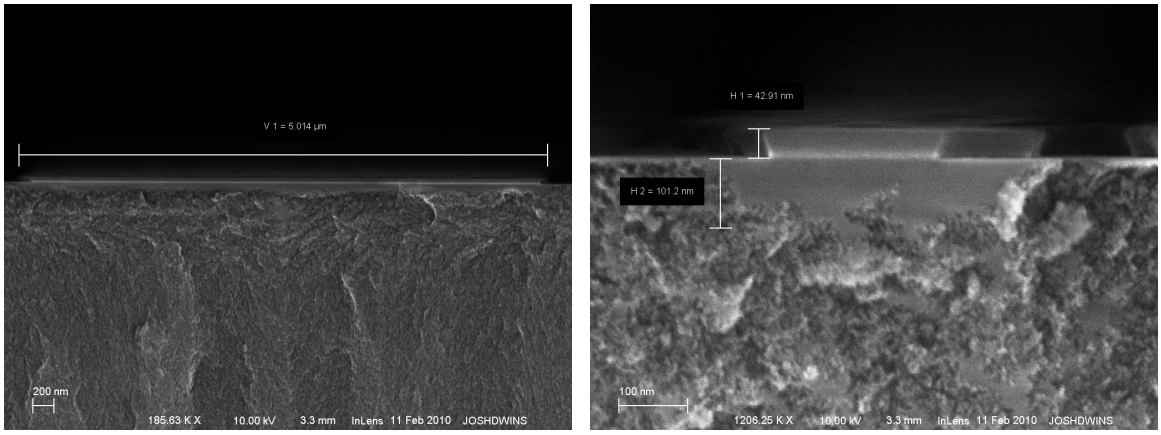


Figure 5.8: SEM cross-sections of sample E. The anneal temperature at 800 °C results in a thinner isolated silicon region with significant thickness variation.

The result of sample E reinforces the role of fluorine and/or fluorine related defects that promote selectivity of porous silicon formation. The anneal done at 800 °C reduces the donor-like effect that is stable at 600 °C, and results in a thinner silicon layer (~ 100 nm) with enhanced interface roughness. Note that the thickness of this isolated silicon layer is less than that formed in sample G which did not have any fluorine introduced. This result may be related to crystal defects remaining at 800 °C which ends up enhancing, rather than suppressing, the formation of porous silicon.

Sample F

The treatment combination for sample F was as follows: With F^+ implant, with the p+ field implant (and activation anneal), nitride RIE underetch, and without a pre-anneal. The SEM image is shown in Figure 5.9.

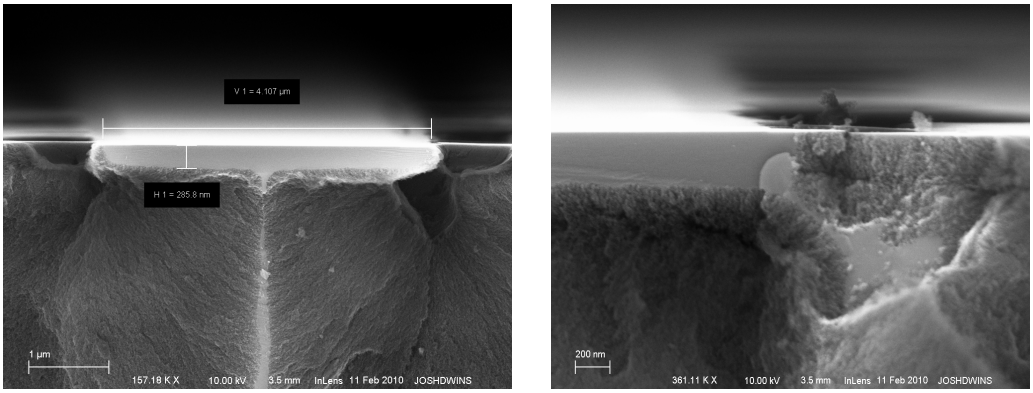


Figure 5.9: SEM cross-sections of sample F. The lack of a pre-anneal whatsoever still results in selective formation of porous silicon, however there appears to be large voids, presumably due to electropolishing in localized areas.

Sample F results in a selective etch with a silicon thickness of about 290nm. In this case since there is no pre-anneal done following the fluorine implant, therefore selectivity may be driven by the high level of disorder. It is likely that the remaining silicon region is amorphous, not crystalline; this remains in question. Large voiding at the edge regions, most likely due to localized current crowding leads to electropolishing. Note that the F+ implant was done in the p+ areas with no subsequent anneal.

Summary

The results of the process integration experiments provided significant insight on the importance of the factors investigated. While the nitride RIE overetch can promote etching selectivity without the use of fluorine (sample G), this technique should not be

used to maintain a planar surface topology. The fluorine implant in combination with the boron p+ field implant provides selectivity with minimal edge encroachment into the active region. A pre-anneal temperature of 600 °C provided recrystallization of the isolated silicon layer while maintaining the selectivity induced by the fluorine, which was compromised at 800 °C. Sample *A* demonstrated, comparatively, the best suited factor settings for an integrated process flow, and was used for the fabrication of electronic and optical devices which will be described in Chapter 6:.

Chapter 6: *INTEGRATED DEVICE FABRICATION AND TESTING*

The developed L-SOI process based on the original FIPOS work looked promising for device applications; however the integrity of the crystalline silicon active regions was still in question. While the integrated process offered high etching selectivity and excellent silicon layer thickness control and uniformity, residual effects of the high-dose fluorine implant following the oxidation and annealing processes had not yet been explored. Both active electronic devices (transistors) and passive optical devices (waveguides) were fabricated on the L-SOI structures to investigate the quality of the silicon and isolation oxide material and associated interface for device applications. This chapter will describe the fabrication and testing results of nMOS transistors and waveguides (λ = 1550 nm) fabricated on L-SOI structures.

6.1 nMOS Fabrication and Testing

Enhancement mode nMOS transistors were fabricated using a six level masking process. The process used was originally designed for the fabrication of thin-film transistors on glass substrates performed at low temperature (T < 600°C) [61]; however thermal processes could be done at higher temperatures consistent with standard silicon technology. These devices were fabricated on L-SOI structures prepared using the integrated process sequence presented in Chapter 5: (see Figure 5.1). The treatment combination of sample A was used as follows: With F^+ implant, with the p+ field implant, nitride RIE underetch, and a 600 °C pre-anneal.

Following sample preparation, electrochemical formation of porous silicon was performed over the interconnected p-type regions, using a 4:1 HF:IPA mixture and a constant current density of 7.5-10mA/cm^2 for 10-15 minutes. Leaving the wafers in the HF-electrolyte for an additional 2-4 minutes ensured complete removal of the nitride masking layer. The multi-step thermal process was then performed: 300 °C for 1 hr in O_2; 1000 °C for 1 hr in O_2; and 1100 °C for 4 hr in N_2. During the thermal oxidation of porous silicon the silicon active regions (top-side and bottom-side) were also oxidized resulting in a high quality SiO_2 for interface passivation (see

Figure **5.3**). The surface oxide layer served as the gate dielectric for an nMOS process developed to establish the electronic performance of devices fabricated using this localized SOI technique.

A molybdenum film was then deposited via DC magnetron sputtering and patterned to form the gate electrode. Molybdenum was used as the gate material; both for thermal stability which enables a self-aligned gate structure, and work function (Φ_M = 4.53 eV) for threshold voltage tuning. The n+ source/drain regions were self-aligned to the molybdenum gate, using a phosphorus dose of 4×10^{15} cm^{-2}. A SiO_2 inter-level dielectric (ILD) was deposited using low pressure chemical vapor deposition, followed by an anneal at 900 °C for two hours in a N_2 ambient. Contact openings were then patterned and etched, followed by aluminum sputter deposition and patterning. A sinter at 425 °C in forming gas (5% H_2 in N_2) was performed for 15 minutes to complete the fabrication process.

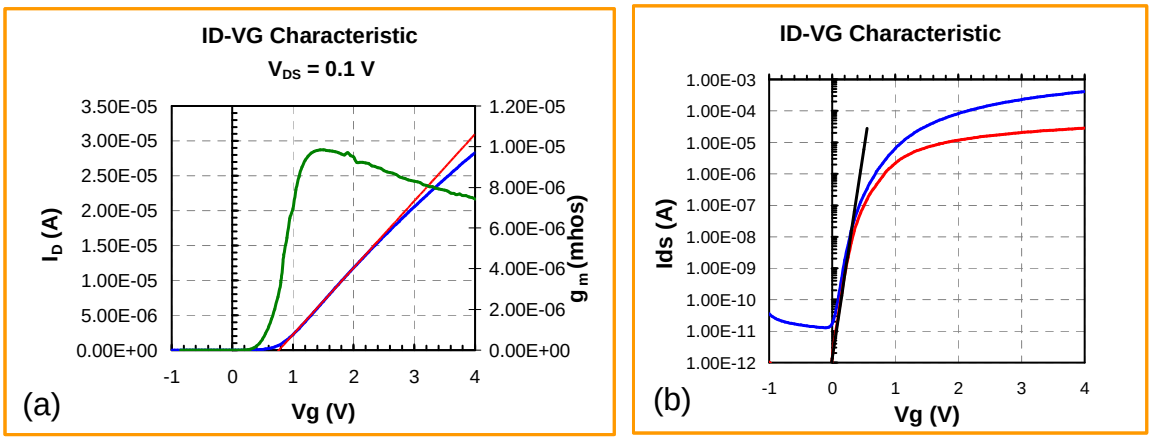


Figure 6.1: Linear-scale (a) and log-scale (b) I_D-V_G transfer characteristics of an nMOS transistor fabricated on a localized SOI active region. The gate length is 12 µm and the active region width is 24 µm. (a) The linear extrapolated threshold voltage is V_T = 0.77 V and the field-effect electron mobility taken at the maximum transconductance is 630 cm^2/V-sec. (b) The subthreshold swing is 87 mV/dec at V_{DS} = 5 V.

I-V characteristics from nMOS transistors fabricated on localized SOI active regions are shown in Figure 6.1. Testing was done using a HP-4145 semiconductor parameter analyzer. The device characteristics are typical of devices fabricated on bulk silicon control wafers. This result confirms that the active channel regions which received the high-dose fluorine implant were completely restored to device quality p-type crystalline silicon. The threshold voltage (V_T = 0.77 V) is consistent with the starting boron doping concentration and a low level of interface charge. The high transconductance and extracted field-effect electron mobility (μ_n = 630 cm^2/V-sec) demonstrates that the silicon surface has not been degraded from the process. The steep subthreshold characteristic (S = 87 mV/dec) demonstrates a low level of interface traps (frontside and backside) as well as a low level of bulk trap states in the silicon body. These results clearly indicate that the strategy used for L-SOI formation yields material suited for electronic device applications.

6.2 Waveguide Fabrication and Testing

The large interest in silicon photonic devices, such as optical interconnects, switches, detectors, amplifiers and modulators, has led to the study of multiple porous silicon waveguide structures. Waveguides are optical devices which are used to transport light from one point to another. They consist of a high refractive index core layer surrounded with a low refractive index cladding layer(s), where light is confined due to the difference in refractive index according to Snell's law. Multilayer planar waveguides [62,63], strip-rib waveguides [63], buried waveguides [64], or silicon-on-oxidized-porous-silicon (SOPS) waveguides [58] are all promising methods of guiding light. With the SOPS method, H^+ implantation [58], or in this case F^+ implantation, creates temporary regions of higher resistivity used to suppress porous silicon formation. A simple waveguide structure has been demonstrated by forming L-SOI regions capable of functioning as an optical waveguide near 1550 nm.

The fabrication of L-SOI for waveguide structures was done using the same integration strategy as the transistor process (sample A, described in Chapter 5:), excluding the low-dose boron implant for the p-buried layer. The process sequence is shown in Figure 6.2. Process variables that were investigated were the pre-anneal temperature and the anodization current density. The pre-anneal temperature will influence the effects of fluorine active region, as well as the level of implanted boron activation in the p+ field regions. Variations in the anodization current density influenced the porosity of the isolation regions, and thus the refractive index of the underlying cladding of the strip waveguide structure.

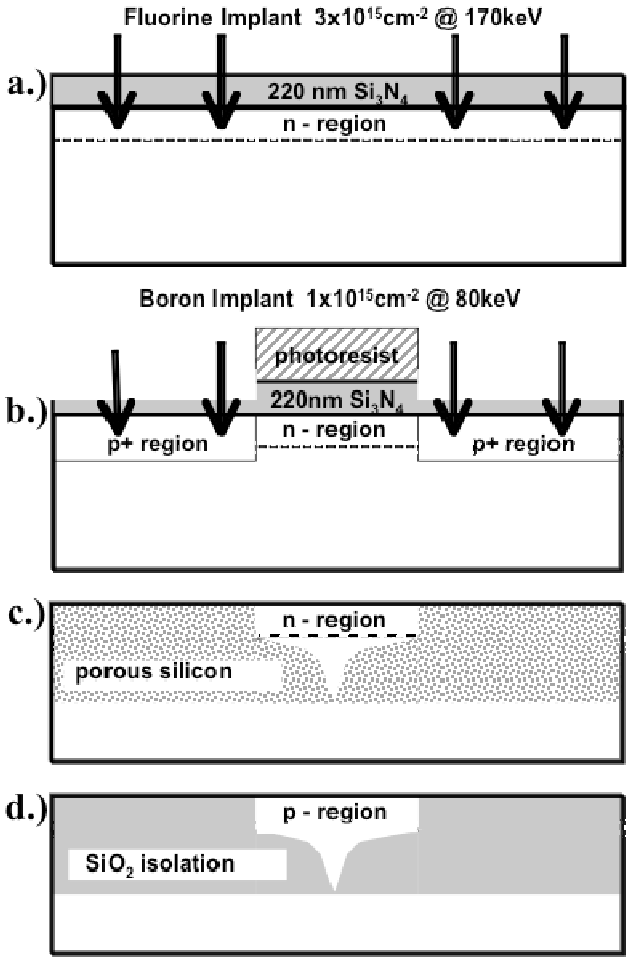


Figure 6.2: Process flow for formation of isolated silicon waveguides inside an oxidized porous silicon film. The use of a p-buried region was not implemented, and thus resulting in an anchor structure tying the isolated region to the bulk substrate.

The investigation on the 2hr pre-anneal temperature demonstrated that as the temperature was increased from 500 °C to 700 °C, the thickness of the crystalline silicon region decreased from 800 nm to 50 nm, respectively. A sample without a pre-anneal was also investigated, however the results demonstrated a degradation of the optical appearance of the sample indicating a surface roughening effect that would translate to significant waveguide loss. Images of fabricated strip waveguides using a 600°C pre-anneal (same as the "standard" L-SOI process) are shown in Figure 6.3 and Figure 6.4.

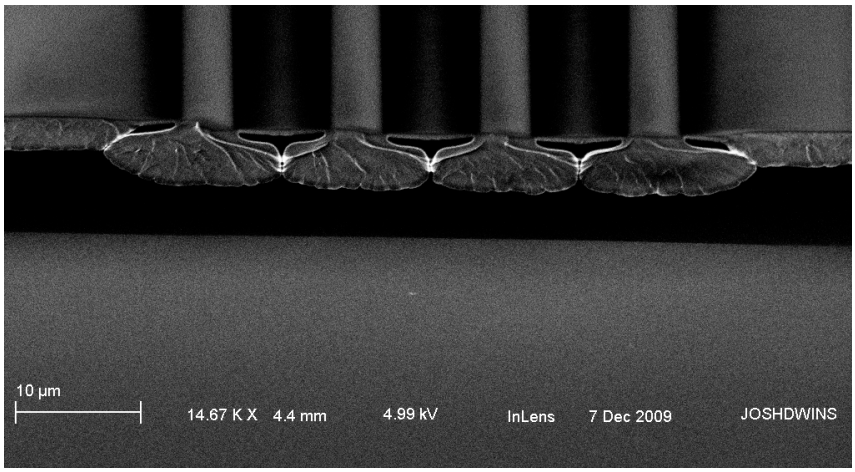


Figure 6.3: SEM image of strip waveguide structures fabricated using the L-SOI process

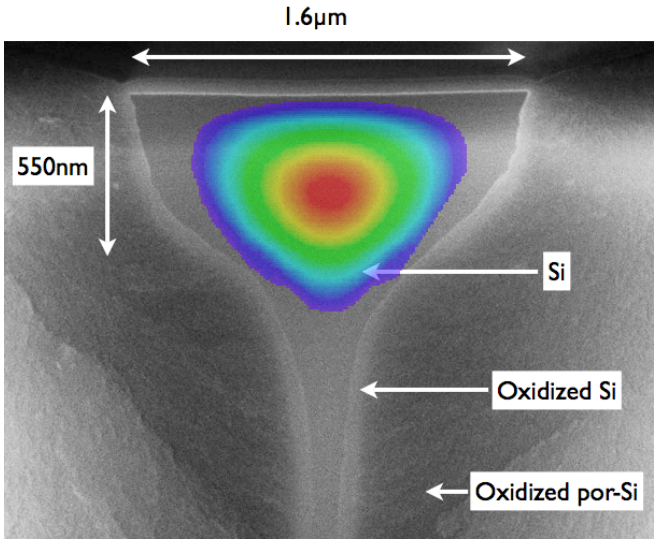


Figure 6.4: The cross section of a typical waveguide created with this process and an overlay of the TE fundamental E-field mode profile for 1550 nm wavelength light source simulated with RSoft FemSim ®.

Without the use of the p-buried layer, the isolated waveguides did have an anchor tie to the underlying substrate. However simulation of the TE fundamental E-field mode profile (Figure 6.4) indicates that the waveguides should demonstrate low loss despite this feature. The estimated refractive indices used for this calculation are n1=1.2, n2=1.45, n3=3.45 for the porous oxide, thermal oxide at the silicon-porous oxide

interface, and silicon core, respectively. The mode profile has an effective index of n_{eff} = 3.3 indicating a high degree of confinement.

The structures were tested using a semiconductor tunable laser set at 1550nm wavelength. TE polarized light was coupled into the waveguide using a lensed fiber. To measure loss, an IR camera captured the light scattered from the top surface of the waveguide as shown in Figure 6.5 and ImageJ® image analysis software was used to calculate the decrease in intensity over a given length.

The measured losses were found to be ~40 dB/cm, which is higher than comparable devices being reported [65]. The greatest source of loss for this waveguide comes from the roughness at the boundary between the silicon core and the porous oxide. It is well reported that the roughness at the edges of a waveguide will play a dominant role in losses, especially as the dimensions of the waveguide become less than the wavelength of the light [58,66]. The estimated roughness at our interface by visual inspection of the SEM cross section is 50 nm. This may be reduced by modifying the anodization and/or oxidation processes.

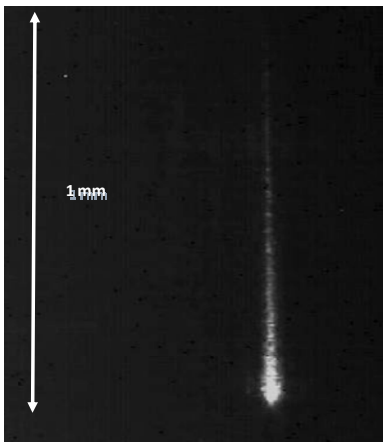


Figure 6.5: IR camera capturing the light scattered from the top surface of the waveguide representing optical loss.

Chapter 7: *SUMMARY AND CONCLUSION*

Initially stated, the goal of this study was to develop L-SOI active device regions using fluorine as a reversible donor species, and to characterize the device quality of the silicon surface. This goal was accomplished through the analysis of various experiments performed, and the characterization of fabricated electronic and optical devices on L-SOI structures.

7.1 Investigation Summary

The initial experiments resulted in a "standard" L-SOI process suitable for integrated device structures. The investigation demonstrated that the choice of integration procedures was just as important as the primary factors under investigation. A key finding which proved to be a significant enhancement to the resulting silicon layer thickness control and uniformity was the introduction of the p-buried implant. This was also shown to enhance the lateral formation of porous silicon, and to avoid the formation of the "anchor" structure which may introduce electrical and optical losses. Implementation of the p-buried layer would also be expected to enhance the performance of the strip waveguides. The "standard" process produces isolated silicon regions that are less than 200 nm thick, with the ability to form large mesa islands as well as resolve structures down to one micron in size.

Electrical characterization of NMOS transistors fabricated on L-SOI regions demonstrated that the modified FIPOS technique using fluorine for selective suppression of porous silicon formation could be a viable candidate for an integrated process. The

implementation of a high-dose implant into the active silicon layer for device fabrication is not unprecedented; the SIMOX method of SOI formation uses exceedingly high doses of implanted oxygen for the formation of a buried oxide. The developed technique uses a F^+ dose that is comparable to standard doping levels, and does not appear to have a permanent effect on the active regions once annealed at high temperature.

7.2 Future Work

While this FIPOS strategy demonstrated success, there are areas which are in need of improvement. The chosen parameters for the "standard" process needs optimization, with further refinement on the range of factor settings. In addition, modifications are required in process integration. Because of the combination of high-dose boron and fluorine implants in the field isolation regions, these areas demonstrate pronounced light scattering and a high density of topographical defect features that are easily observed by optical microscopy. It is expected that these defects contribute to the optical edge losses demonstrated by the strip waveguides tested. These defects are not apparent on blanket field isolation regions, and an integration strategy which does not require implants in the field region is currently under investigation.

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