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# Design for manufacturing: Performance characterization of digital VLSI systems using a statistical analysis/inference methodology

J. Ignacio Espinosa de los Monteros

# DESIGN FOR MANUFACTURING:

## Performance Characterization of Digital VLSI Systems Using a Statistical Analysis/Inference Methodology

by

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## Performance Characterization of Digital VLSI Systems Using a Statistical Analysis/Inference Methodology.

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_____ Date: July 27 1993

*This M.S. Thesis is dedicated to those most special people in my life:*

*Dr. María Antonieta Espinosa de los Monteros*

*(my mother)*

*Mr. J. Antonio Gutierrez T. E. M.*

*(my brother)*

*Ms. Maria Helena Pulkkinen*

*(my girlfriend)*

*for their love, understanding, support and belief in me.*

*J. Ignacio G. T. E. M.*

# ABSTRACT

Design For Manufacturing (DFM) is a TQM methodology by which inherently producible products can be manufactured with high yields, short turnaround time and great flexibility. The key to the success of any DFM program lies in increased accuracy in the modeling of the process and product designs, product simulations and effective manufacturing feedback of key parametric data. That is, properly modeling and simulating designs with data which reflects current fabrication capabilities has the most lasting influence in the performance of products. It is this area that is tackled in the methodology developed hereafter; a method by which to feedback and feedforward parametric data critical to the performance of Digital VLSI systems for performance prediction purposes. In this method, integrated circuit and applied statistics concepts are used jointly to perform analyses and inferences on response variables as a function of key processing and design variables that can be statistically controlled. Furthermore, an experimental design procedure utilizing electrical simulation is proposed to efficiently collect data and test previously proposed hypotheses. Conclusions are finally made with regard to the usefulness and outreach of this method, as well as those areas affected by the behavior of the performance predictors, both in the design and manufacturing stages of VLSI engineering.

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# Section 1

## *Thesis Principles*

# 1

# INTRODUCTION

## 1.1 Introduction

Design for Manufacturing (DFM) is a methodology by which inherently producible products can be manufactured with high yields, short turnaround time and great flexibility. There are several ways to achieve these objectives. One such way is by reducing variability levels in fabrication processes and thus increase capabilities on the individual process steps, as well as whole processes for mass production. Another way to attain this is by realistic characterization of processes, leading to models which can be used at the circuit design level in order to prevent violations of physical and electrical rules that could hinder performance of the overall system.

The key to the success of any DFM program lies in increased accuracy in the modeling of the process and product designs, product simulations and effective manufacturing feedback of key parametric data. It is this area which proves most effective when dealing with the interactions between manufacturing and design. That is, properly modeling and simulating designs with data which reflects current fabrication capabilities has the most lasting influence in the performance of products.

This has been the motivation behind geometric (drawn) rule generation and electrical parameter extraction for very large scale integrated (VLSI) systems. Even though correctly drawn structures are necessary for integrated (semiconductor) circuits to attain the desired topology, electrical characterization and device parameter extraction are indispensable to predict actual performance of the product.

The Simulation Program for Integrated Circuit Engineering (SPICE) has long been regarded as essential in the simulation of digital and analog circuits of any sort, both academically and industrially. This program has the flexibility to choose between different models and fill out as many parameters as necessary for the desired accuracy level. Moreover, it will take into consideration the interconnection structure of the system and will interrelate the inherent device physics that underlie the elements which compose it.

Other tools which have recently become available to those in the area of DFM includes statistical analysis. Statistics has successfully been used in various disciplines. This has allowed the use of more stringent control and specifications, making processes and products more reliable and reproducible than ever before. Nevertheless, techniques like those of descriptive statistics, capability analyses, design of experiments and statistical process control (SPC) are very new to those working in the semiconductor industry.

## 1.2 Problem Statement, Objectives and Hypothesis

Variability is inherent to any manufacturing process. Quality is a feature that is hard to attain, and even harder to maintain. Rochester Institute of Technology has made it one of their goals to "make students more aware of high-quality engineering and manufacturing" so as "to make the companies graduates work for more competitive in the world market."[4] With this five-year goal in mind, the student-run integrated circuit (IC) factory should undergo a current-capability analysis in order to assess what specific objectives will allow the achievement of the goal stated above. This subsection will consider the general problem being faced by design and manufacturing efforts, as well as the desired objectives and hypotheses that must be provided.

### 1.2.1 Problem Statement

Precision, accuracy, quality and reliability and high performance are goals that both VLSI designers and IC manufacturers have in common. The metrics for these goals can be in the form of high-yield, low turnaround time lowest cost objectives, as well as in the form of high-performance, low-power, short time delay. Whatever they may be called, they are genuine concerns that affect the relationships between both sides of the overall process which results in semiconductor electronic systems. Nevertheless, the way to achieve these objectives is not well understood.

To begin with, designers need proper characterization of devices and well-defined parameters in order to design according to realistic constraints and specification limits within which the systems will work

properly. On the other hand, manufacturers have the everlasting nuisance of dealing with the idealistic and highly controlled conditions in which designers simulate, verify and test systems to be manufactured; this is a set of circumstances that rarely occurs in reality. There is obviously a lack of detailed and timely communication between the two parts that make up the entire process.

A comparison between design-side and manufacturing-side results is necessary. These results are to be thoroughly analyzed. Furthermore, characterizations of the performance that is supposed to be attainable and that is actually obtained should be compared. Finally, recommendations will be made to close the gap between the ideal design and the actual product in future efforts. A means to visualize the method that needs to be used to solve this problem will be provided through the detailed application of this procedure to a product (design) at the R.I.T. Fab.

### 1.2.2 Objectives

This study intends to concentrate on the feedback path existing from the manufacturing stage to the design stage. A method will be developed by which tools such as SPICE will provide realistic indicators of the attainable performances from the target manufacturing conditions under which the VLSI systems will be fabricated. This will include a detailed analysis of the interactions between each of the different factors that affect this feedback, as well as techniques for obtaining the most significant results out of the information available for characterization of the fabrication processes that affect designs running through them.

Moreover, recommendations for future work will be drawn from the results obtained out of this methodology.

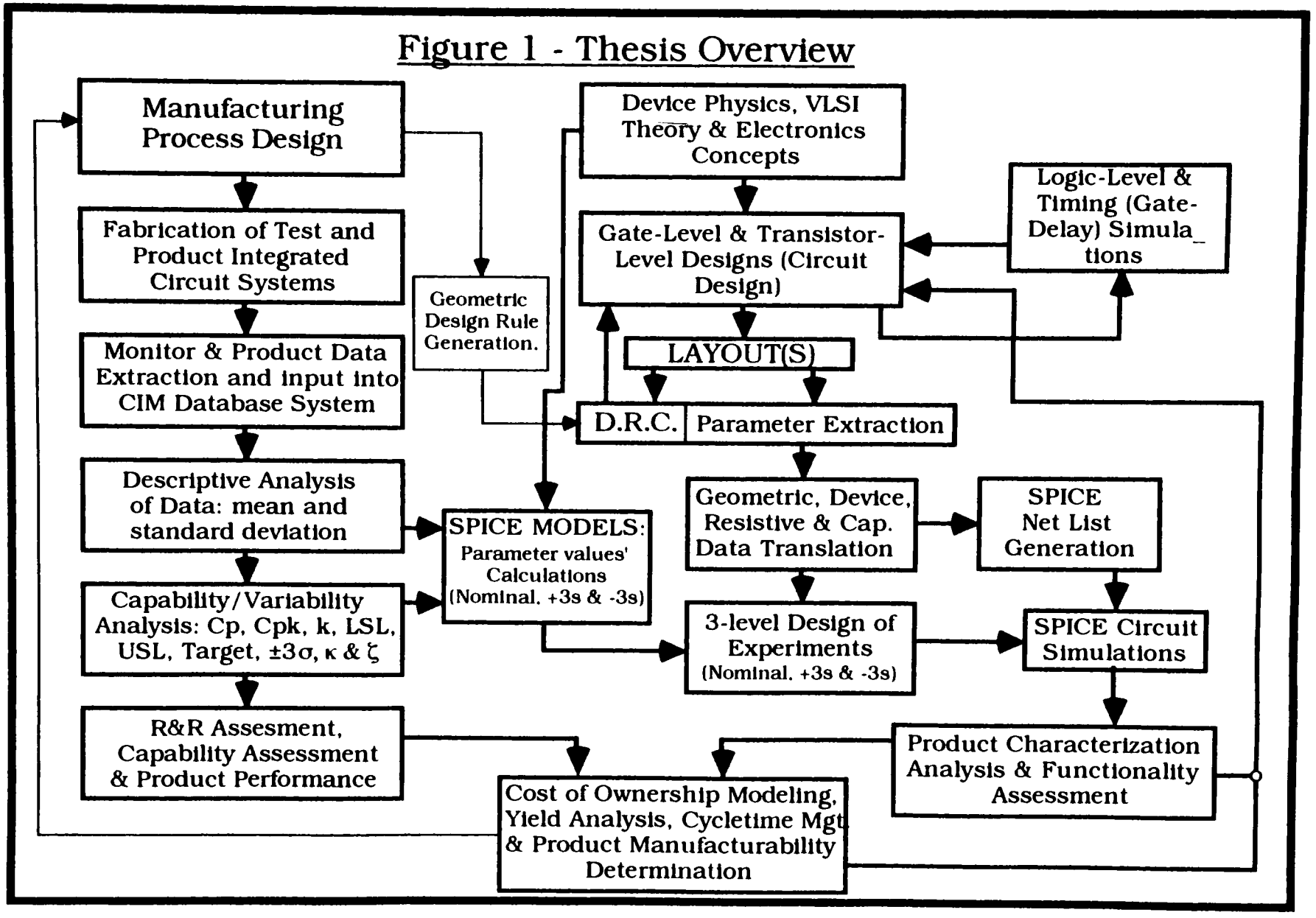
Because of the large span of variables that affect the feedback from fabrication to design, there needs to be some kind of control in order to better understand the most important ones. Theoretical background from both stages of the production process will be used to reduce the total set of variables to the maximum extent possible, by understanding the relationships between all of them. Statistical tools of analysis and inference will be used to define the subset of interactions which can currently be studied and which will produce the largest results among those variables available for study.

Finally, there is a need for examples of the usefulness of this method is noticed. Therefore, a simple application of this method to the nMOS inverter will be considered, results will be outlined and conclusions stated in order to foresee practical uses of this method and possible expansion of it into other areas that affect the relationships between manufacturing and design.

### 1.2.3 Hypothesis

With all the tools, techniques and theory available, a solution is proposed. This solution specifies a set of steps by which manufacturing data can influence design work, as well as factors such as cost and yield. This is shown in figure 1 (page 7 above). It can be seen that the nature of the interactions between manufacturing and design is complex, no matter how simplified the model may be. The methodology to follow

# Figure 1 - Thesis Overview



involves analysis and manipulation of data in both manufacturing and design. It is important to notice that the major emphasis of this model is in circuit performance characterization. This is why there is only a weak link between manufacturing and design involving layout design rules.

It is most important to notice the series of steps required rather than the work involved in each of them. This is because one of the goals of this study is to be able to expand this reasoning into more detailed research as well as into other areas that affect the relationships between fabrication and design work. The hypothesis is that this method works and can be used to simulate realistically any effects of manufacturing variability at the design stage, therefore reducing the probability of product failure once fabrication has begun. Moreover, it is hypothesized that the effects of machine and process capabilities can be accounted for at design level in order to reduce the aftermath of problems that may occur otherwise.

## 1.3 General Assumptions and Justifications

The material and method here presented are largely simplified due to the real size of the problem being dealt with here. The true size and quantity of relationships that exist between design and manufacturing are too many to handle in a single effort of the size of this one. Thus, some assumptions and justifications are given in order to better understand the problem space that will be covered by the solution being

proposed hereafter.

The first assumption is that the layout design rules that provide geometric data (which defines areas of capacitive and resistive importance) are held true. That is, their effects on performance will not be tested and their validity will not be questioned for the purposes of this research. The justification behind this is that the number of variables that can therefore be held constant will increase and the problem space will converge into a more manageable one. Otherwise, interactions that occur due to the geometry of structures as far as performance and device parametrics are concerned would make the problem far too complex. This implies a need to investigate what effects geometry considerations will have on performance when variations in sizes come to play after the manufacturing process. This is beyond the reach of this research.

Another assumption that is made refers to the sole use of SPICE as a characterization tool. There are many more tools that can be used to characterize circuits. Nevertheless, SPICE has been regarded as a standard throughout academic and industrial environment. The models contained in this package are thorough enough for the purposes of this project. Even though there are many models, the treatment will only be made at an empirical level. Certainly there are other more involved and thorough models to consider, but due to the simplifications that are sure to exist in this study the need for such models is somewhat irrelevant.

A third assumption considered here is that capability studies, as important as they are to the factory environment, come into play to determine the variability that is relevant to those causes which affect

performance in any way. Certainly, complete studies of this sort would prove more insightful and could show how to improve accuracy and precision in mass production. Nevertheless, the broad nature of this research cannot concentrate on this matter alone and must consider only those results which are of importance to the overall circuit performance assessment as related to the variables under study.

Another assumption that is being used here is that of the limited extent of knowledge that can be used as far as Statistics and Design of Experiments is concerned. This will certainly have the effect of simplifying matters more than if more thorough knowledge regarding such disciplines was available. Nevertheless, the analysis, inferences and results obtained from the use of this disciplines will be robust in their nature and should not mislead future efforts in this area of research.

Finally, even though there are many tools available for the circuits being studied, only those which are mostly encountered at Rochester Institute of Technology's Computer Engineering and Microelectronic Engineering departments will be considered. The reason for this is that the lack of technical support could result in serious setbacks, an impossibility to complete the study and could even make the conclusions become unreliable due to the inability to prove the usefulness of the methodology developed in theory.

# 2

# THEORETICAL BACKGROUND

Parameter extraction is a very important part of any successful DFM effort. It is recognized that without accurate models used by designers of VLSI structures, faulty products result and variation remains out of control throughout the process. It is of particular interest for designers to have reliable measures of quality from the manufacturing side, especially in a quantitative form usable within the models available.

It is because of this reasoning that tools such as SPICE, were made available. SPICE was first developed at the University of California at Berkeley with the goal of analyzing integrated circuits by simulating models containing parameters which demonstrate the effects of manufacturing process changes on circuit performance. Furthermore, it became a standard which has played a central role in the development of proprietary and commercial tools of similar, but enhanced features. Tools such as the Mentor Graphics' Accusim, Meta-Software's HSPICE and others have become more common nowadays. Some tools have become more accepted than others, making it difficult to chose among them. Due to its similarity to the original SPICE, its compatibility to CAD tools currently used, and its straight forward operation HSPICE is a good example of integrated circuit modeling software tools that has been well accepted in the engineering world.

Selection by designers of the correct model within the program is essential for validation of the work done prior to manufacturing procedures. Several models exist within each of the tools that can be chosen for particular applications. Most frequently, corporations will have their own circuit models for use in simulators and validation tools. In the academic world, on the other hand, models inherent to the program are accepted as such, unless research has been conducted to find more accurate ones.

In this particular study, due to its focus, as well as its approach, a simple model will prove very helpful in simplifying the methodology being developed. Problems associated with more complex models, as well as the inclusion of large numbers of parameters within a particular model will be left for future research efforts to solve. Therefore, an empirical model has been chosen for use in the methodology that will be discussed in the following chapter.

Integrated circuits are quite complex in their behavior and the ways to understand them. Most of the design world looks at VLSI structures as sets of switches with a number of resistances and capacitances which hinder their performance. Nevertheless, the individual "switches" are dealt with in a very simplistic manner. On the other hand, the manufacturing world regards these structures as complex electromagnetic "machines" which are composed of elements rather complex themselves. This discrepancy between the two worlds has made a large impact in the development of feedback lines from manufacturing to design in order to reduce variation in the

characteristics of circuits, increase yield, turnaround time, etc. Obviously, there is a need for a middle ground between both views.

In this chapter it is intended to provide a broad enough set of concepts to provide for a basis from which to extract the necessary tools for method-building and analysis essential thereafter. A knowledge base is drawn from a very diverse number of places, centering around SPICE modeling. These include software modeling, such as that used in SPICE, MOSFET theory, inverter circuit theory, Statistics (Descriptive and Analytical), Design of Experiments, manufacturing issues such as yield, cost of ownership and others which are impacted by the performance and manufacturability of the circuits processed in the VLSI industry. All of the concepts that are necessary in order to understand the methodology developed and explained in subsequent chapters is discussed below.

## 2.1 SPICE MOSFET Modeling

Transistors, whether pMOS or nMOS, have a number of characteristics which are becoming more and more important to consider in order to achieve the speeds and densities which are currently sought after. Their modeling is essential in order to properly predict behaviors of small and large structures as well as be able to assess the speed and power dissipation desired for the VLSI product being designed. SPICE contains models that are accurate and thorough enough to fulfill the needs of both design and fabrication. Also, it can fully characterize the elements which are so essential to performance in IC circuits. Moreover,

it provides the tools to simulate larger basic elements, such as inverters, which define the essential structure which all digital circuits in integrated circuit design can be reduced to in the end. SPICE's empirical model (level 3) contains a number of parameters which have both design and fabrication theory behind them. Because of this reason, a general discussion of each of those parameters and their theory are essential to the better understanding of the method discussed subsequently.

For VLSI applications of programs like HSPICE, circuit models are defined by the MOSFET model and element parameters, and two submodels selected by the CAPOP (MOSFET gate capacitances' model) and ACM (Area Calculation Method for bulk diode model determination) parameters [1]. The selection of the MOSFET model type depends on the electrical parameters critical to the application. In this case, the number of parameters is to be reduced substantially to try out the method of interest to the minimum few required for meaningfulness.

The MOS transistor is described by use of an element and a .MODEL statement (just as in SPICE). The element statement defines the connectivity of the transistor, as well as referencing the .MODEL statement. The .MODEL statement defines the transistor operation as that of an n- or p-channel device, its level and other model parameters of interest. The CAPOP parameter is associated with the MOS model. Depending on its value, different capacitor models are used to model the MOS gate capacitance. Modeling of the bulk-to-source and bulk-to-drain diodes are selected by the ACM parameter, which controls the geometry of the source and drain diffusions, resistance, capacitance and DC

characteristics [1]. There are intricate details concerning the correct use of each of this modeling options and submodels, which are left to the manuals to explain in a more thorough manner. The CAPOP and ACM parameters will specify the set of equations to use in the calculation of capacitances, resistances and areas of importance. This feature is of importance in the methodology explained in chapter 3, since some of these parameters need to be held constant somehow and this provides a simple method for doing so.

Certainly, different processes will have different emphases on different variables available for modeling. Nevertheless, having an empirical (level 3) model there are certain parameters that because of their importance, need a brief explanation. These are shown in table 1 along with a short definition, default value and units used for each of them.

Table 1
Empirical Model HSPICE Parameters

| **Name (Alias)** | **Units** | **Default** | **Description** |
|---|---|---|---|
| *Basic Model Parameters* | | | |
| *LEVEL* | | 1.0 | DC model selector. 3 is for Empirical Model. |
| *COX* | $F/m^2$ | 3.453E-4 | Oxide capacitance per unit gate area. |
| *KAPPA* | $1/V$ | 0.2 | Saturation field factor, for $\lambda$ calculation. |
| *KP (BETA)* | $A/V^2$ | 2.0E-5 | Intrinsic Transconductance parameter. |
| *TOX* | m | 1E-7 | Gate oxide thickness. |
| *VMAX* | m/s | 0.0 | Maximum drift velocity of carriers. |
| *Effective Width and Length Parameters* | | | |
| *DEL* | m | 0.0 | Channel length reduction on each side. |
| *LD (LATD)* | m | none | Lateral source & drain diff. into channel. |
| *LREF* | m | 0.0 | Channel length reference. |
| *WD* | m | 0.0 | Lat. diff. into chan. from bulk along width. |
| *WMLT* | | 1.0 | Diffusion layer and width shrink factor. |

table 1 (continued)

| Name (Alias) | Units | Default | Description |
|---|---|---|---|
| *WREF* | m | 0.0 | Channel width reference. |
| *LMLT* | | 1.0 | Length shrink factor. |
| *XJ* | m | 0.0 | Metallurgical junction depth. |
| *XL (LDEL)* | m | 0.0 | Masking/Etching effect contribution factor. |
| *XW (WDEL)* | m | 0.0 | Masking/Etching effect contribution factor. |
| *Threshold Voltage Parameters* | | | |
| *DELTA* | | 0.0 | Narrow width threshold adjust factor. |
| *ETA* | | 0.0 | Static feedback threshold adjust factor. |
| *GAMMA* | $V^{1/2}$ | none | Body effect factor. |
| *LND* | $\mu$m/V | 0.0 | ND length sensitivity. |
| *LN0* | $\mu$m | 0.0 | N0 length sensitivity. |
| *ND* | 1/V | 0.0 | Drain subthreshold factor. Typical value=1. |
| *N0* | | 0.0 | Gate subthreshold factor. Typical value=1. |
| *NFS* | $cm^{-2}V^{-1}$ | 0.0 | Fast surface state density. |
| *NSUB* | $cm^{-3}$ | 1E15 | Bulk surface doping. |
| *PHI* | V | 0.576 | Surface inversion potential. |
| *VTO* | V | none | Zero-bias threshold voltage. |
| *WIC* | | 0.0 | Subthreshold model selector. |
| *WND* | $\mu$m/V | 0.0 | ND width sensitivity. |
| *WN0* | $\mu$m | 0.0 | N0 width sensitivity. |
| *Mobility Parameters* | | | |
| *THETA* | 1/V | 0.0 | Mobility degradation factor. |
| *UO (UBO)* | $cm^2/(V \cdot s)$ | 600 (N)<br>250 (P) | Low field bulk mobility. |
| *DC Model Parameters* | | | |
| *ACM* | | 0 | Area Calculation Method selector. |
| *JS* | $A/m^2$ | 0 | Bulk junction sat. current per unit area. |
| *JSW* | A/m | 0 | Sidewall bulk junction sat. current |
| *IS* | A | 1E-14 | Bulk junction saturation current. |
| *N* | | 1 | Emission coefficient. |
| *NDS* | | 1 | Reverse bias slope coefficient. |
| *VNDS* | V | -1 | Reverse diode current transition point. |
| *Capacitance Model Parameters* | | | |
| *CBD* | F | 0 | Zero-bias bulk-drain junction capacitance. |
| *CBS* | F | 0 | Zero-bias bulk-source junction capacitance. |
| *CJ (CSB)* | $F/m^2$ | 0 | Zero-bias bulk junction capacitance. |
| *CJSW (CJP)* | F/m | 0 | Zero-bias sidewall bulk junction cap. |

table 1 (continued)

| Name (Alias) | Units | Default | Description |
|---|---|---|---|
| *CJGATE* | F/m | 0 | Zero-bias gate-edge sidewall bulk junct. cap. |
| *FC* | | 0.5 | Forward-bias depletion cap. coeff. (not used) |
| *MJ (EXJ)* | | 0.5 | Bulk junction grading coefficient. |
| *MJSW (EXP)* | | 0.33 | Bulk sidewall junction grading coefficient. |
| *NSUB** | $cm^{-3}$ | 1E15 | Substrate doping. |
| *PB (PHS)* | V | 0.8 | Bulk junction contact potential. |
| *PHP* | V | PB | Bulk sidewall junction contact potential. |
| *TT* | s | 0 | Transit time. |
| *Drain and Source Resistance Model Parameters* | | | |
| *RD* | Ω | 0.0 | Drain ohmic resistance. |
| *RDC* | Ω | 0.0 | Additional drain resistance due to contact. |
| *RS* | Ω | 0.0 | Source ohmic resistance. |
| *RSC* | Ω | 0.0 | Additional source resistance due to contact. |
| *RSH* | Ω/sq. | 0.0 | Drain and source diffusion sheet resistance. |
| *MOS Geometry Model Parameters* | | | |
| *LD (LATD)** | m | none | Lateral diffusion into channel from S & D. |
| *LDIF* | m | 0 | Length of lightly doped diff. adjacent to gate. |
| *HDIF* | m | 0 | Length of heavily doped diff., from contact. |
| *WMLT** | | 1 | Width diff. layer shrink reduction factor. |
| *XJ** | m | 0 | Metallurgical junction depth. |
| *XW (WDEL)** | m | 0 | Masking/etching effects contribution factor. |
| *Common Threshold Voltage Parameters* | | | |
| *DELVTO* | V | 0.0 | Zero-bias threshold voltage shift. |
| *GAMMA** | $V^{1/2}$ | 0.527625 | Body effect factor. |
| *NGATE* | $cm^3$ | none | Polysilicon gate doping, used in anal. model. |
| *NSS* | $cm^{-2}$ | 1.0 | Surface state density. |
| *NSUB** | $cm^3$ | 1E15 | Substrate doping. |
| *PHI** | V | 0.576036 | Surface potential. |
| *TPG (TPS)* | | 1.0 | Type of gate material, used in anal. model. |
| *VTO** | V | none | Zero-bias threshold voltage. |
| *Impact Ionization Model Parameters* | | | |
| *ALPHA* | $V^{-1}$ | 0.0 | Impact ionization current coefficient. |
| *LALPHA* | μm/V | 0.0 | ALPHA length sensitivity. |
| *WALPHA* | μm/V | 0.0 | ALPHA width sensitivity. |
| *VCR* | V | 0.0 | Critical voltage. |
| *LVCR* | μm·V | 0.0 | VCR length sensitivity. |
| *WVCR* | μm·V | 0.0 | VCR width sensitivity. |
| *IIRAT* | 1 | 1.0 | Part of ALPHA that goes to bulk. |

table 1 (continued)

| Name (Alias) | Units | Default | Description |
|---|---|---|---|
| *Basic Gate Capacitance Parameters* | | | |
| *CAPOP* | | 2 | Capacitance model selector. |
| *COX (CO)** | $F/m^2$ | 3.453E-4 | Oxide capacitance per unit area. |
| *TOX** | m | 1E-7 | Thin oxide thickness. |
| *Gate Overlap Capacitance Model Parameters* | | | |
| *CGBO (CGB)* | F/m | 0.0 | Gate-bulk overlap cap./meter chan. length. |
| *CGDO (C2)* | F/m | 0.0 | Gate-drain overlap cap./meter chan. width. |
| *CGSO (C1)* | F/m | 0.0 | Gate-source overlap cap./meter chan. width |
| *LD (LATD)** | m | none | Lateral diffusion into channel from S & D. |
| *METO* | m | 0.0 | Fringing field factor for G-to-S & G-to-D cap |
| *WD** | m | 0.0 | Lat. diff. into chan. from bulk along width. |
| *Meyer Capacitance Parameters, CAPOP = 0,1,2* | | | |
| *CF1* | V | 0.0 | Modif. MEYER cntrl. for cgs transition from depletion to weak inversion for CGSO. |
| *CF2* | V | 0.1 | Modif. MEYER cntrl. for cgs transition from weak to strong inversion region. |
| *CF3* | | 1.0 | Modif. MEYER cntrl. for cgs and cgd from saturation to linear reg. as funct. of vds. |
| *CF4* | | 50.0 | Mod. MEYER cntrl. for contour of cgb & cgs smoothing factors. |
| *CF5* | | 0.667 | Modif. MEYER cntrl. capacitance multiplier for cgs in saturation region. |
| *CF6* | | 500.0 | Modif. MEYER cntrl. for contour of cgd smoothing factor. |
| *CGBEX* | | 0.5 | cgb exponent, only for CAPOP = 1. |
| *Charge Conservation Parameter, CAPOP = 4* | | | |
| *XQC* | | 0.5 | Coeff. of chan. charge share due to drain. |
| *Noise Parameters* | | | |
| *AF* | | 1.0 | Flicker noise exponent. |
| *KF* | | 0.0 | Flicker noise coefficient. |
| *NLEV* | | 2.0 | Noise equation selector. |
| *GDSNOI* | | 1.0 | Shot noise coefficient. |
| *Temperature Effects Parameters* | | | |
| *BEX* | | -1.5 | Low field mobility temperature exponent. |
| *CTA* | $°K^{-1}$ | 0.0 | Junction cap. CJ temperature coefficient. |
| *CTP* | $°K^{-1}$ | 0.0 | Junction sidewall cap. CJSW temp. coeff. |
| *EG* | eV | 1.11 (TLEV=0,1)<br>1.16 (TLEV=2) | Energy gap for pn junction diode. |

table 1 (continued)

| Name (Alias) | Units | Default | Description |
|---|---|---|---|
| *F1EX* | | 0 | Temp. exponent for mobility degrad. param. |
| *GAP1* | eV/°K | 7.02E-4 | First bandgap correction factor. |
| *GAP2* | °K | 1108 | Second bandgap correction factor. |
| *LAMEX* | $°K^{-1}$ | 0 | λ temperature coefficient. |
| *N** | | 1.0 | Emission coefficient. |
| *MJ** | | 0.5 | Bulk junction bottom grading coefficient. |
| *MJSW** | | 0.33 | Bulk junction sidewall grading coeff. |
| *PTA* | V/°K | 0.0 | Junction potential PB temp. coeff. |
| *PTC* | V/°K | 0.0 | Fermi potential PH :mp. coefficient. |
| *PTP* | V/°K | 0.0 | Junction potential PHP temp. coefficient. |
| *TCV* | V/°K | 0.0 | Threshold voltage temp. coefficient. |
| *TLEV* | | 0.0 | Temperature equation level selector. |
| *TLEVC* | | 0.0 | Temp. eq. level select. for caps. & potentials. |
| *TRD* | $°K^{-1}$ | 0.0 | Temperature coeff. for drain resistor. |
| *TRS* | $°K^{-1}$ | 0.0 | Temperature coefficient for source resistor. |
| *XTI* | | 0.0 | Saturation current temperature exponent. |

* Repeated parameters in different categories.

Having so many parameters to consider, a brief discussion of the most important (and well-known) ones is in order. For this matter, we will turn to MOSFET and inverter theories. This will allow for a definite reduction of the set of parameters that is necessary for manageable simulation purposes. Considerations about what all the submodels and parameters are about are left for the reader to study in the appropriate bibliography. An emphasis will be given to tying variables and parameters together in order to justify as many reductions as possible. On the other hand, it should be noted that some of the parameters are only useful in certain models or submodels. Also, some others can be calculated from several parameters if not specified (such as VTO). This is

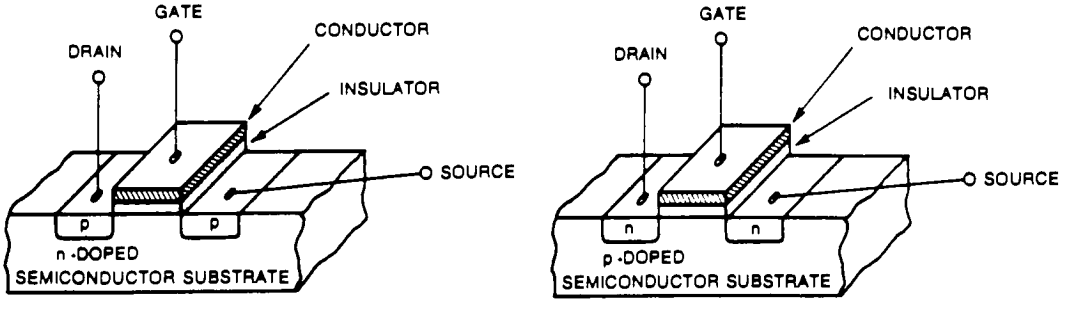
the main reason why there is a need for discussing some important transistor theory concepts.

## 2.2 MOSFET & Circuit Theory

### 2.2.1 MOSFETs

An MOS (Metal-Oxide-Silicon) structure is created by superimposing several layers of conducting, insulating, and transistor forming materials (LOCOS technology).[5] nMOS technology provides two types of transistors (or devices), an enhancement-mode n-type transistor and a depletion-mode n-type transistor. On the other hand, CMOS technology only uses enhancement transistors, one n-type and the other p-type. Typical physical structures of the two types of transistors are shown in Fig. 2 as follows.

Figure 2 - MOSFET Physical Structures

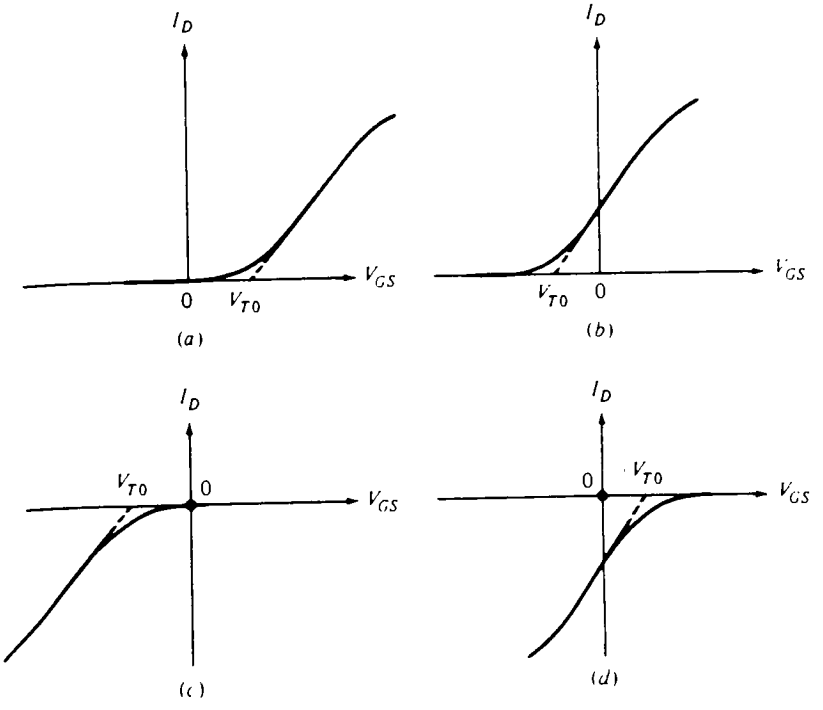



MOSFETs (or transistors) have certain I-V characteristics that

result from the physics of the MOS system when coupled to the drain and source n+ (or p+) regions. Current flow from drain to source is controlled by the gate-source voltage $V_{GS}$, the drain-source voltage $V_{DS}$, and the source-bulk voltage $V_{SB}$.[6] Depending on the sign of the threshold voltage ($V_{TO}$), MOS transistors are separated into two categories. The n-type transistors with positive $V_{TO}$ are called enhancement mode (or "normally off") devices, whereas n-type transistors with negative $V_{TO}$ are said to be depletion mode (or "normally on") devices. The reverse of this situation is the case for p-type transistors.[7] This is shown in Fig. 3 for the four types of devices and a very small absolute value of $V_{DS}$.

## Figure 3 - Enhancement versus Depletion Mode MOSFETs

$I_{DS}$ vs. $V_{GS}$ for $V_{SB}$=0 and very small ABS($V_{DS}$). (a) n-type enhancement device; (b) n-type depletion device; (c) p-type enhancement device; (d) p-type depletion device.




A MOS transistor is termed a majority-carrier device, in which the

current in a conducting channel between the source and drain is modulated by a voltage applied to the gate. In the n-type MOSFET, the majority carriers are electrons. A positive voltage applied on the gate with respect to the substrate *enhances* the number of electrons in the channel (the region directly under the gate oxide) and hence increases the conductivity of the channel. For gate voltages less than $V_{TO}$ the channel is cut-off, thus causing a very low drain-to-source current. The operation of a p-type MOSFET is analogous, with the exception that the majority carriers are holes and the voltages are negative with respect to the substrate. In the case of depletion devices, increasing the voltage will reduce the number of electrons (or holes) under the gate oxide and will eventually cause the flow to cut-off.

Several parameters are used to characterize the operation of MOSFETs. Among them are the threshold voltage, $V_{TO}$, the body bias, $\gamma$, the device transconductance, $\beta$, the channel length modulation, $\lambda$, etc. Also, a set of current-voltage characteristics can be extracted by modeling the electron inversion (or hole inversion) layer created when the gate voltage exceeds (or is less than) $V_{TO}$. A brief discussion of these figures and equations is shown below for it is necessary to further understand the operation of larger systems, such as the inverter, discussed later on. The approach taken is by observing the operation of the n-channel transistor in certain amount of detail and then extracting the p-channel device from this.

**$C_{ox}$:** This is the oxide capacitance per unit area. It is calculated from $t_{ox}$, as follows:

$$C_{ox} = \varepsilon_{ox}/t_{ox}\ [F/m^2],$$

such that $\varepsilon_{ox} \approx 3.9\varepsilon_o$ F/m for silicon dioxide and $\varepsilon_o$ = 8.854E-12 F/m [2].

**$V_{TO}$:** The value of the threshold voltage is set by the electrical properties of the MOS system. Internal device parameters such as doping densities, oxide thickness, and ion implant dose are established during the processing, and set the basic value this variable will take. The "O" subscript is used to denote zero body-bias ($V_{SB}$=0). The threshold voltage may be calculated from:

$$V_{TOn} = V_{FB} + \phi_S + C_{OX}^{-1}(2q\varepsilon_{Si}N_a\,\phi_S)^{1/2} \pm (qD_I/C_{OX})\ [V],$$

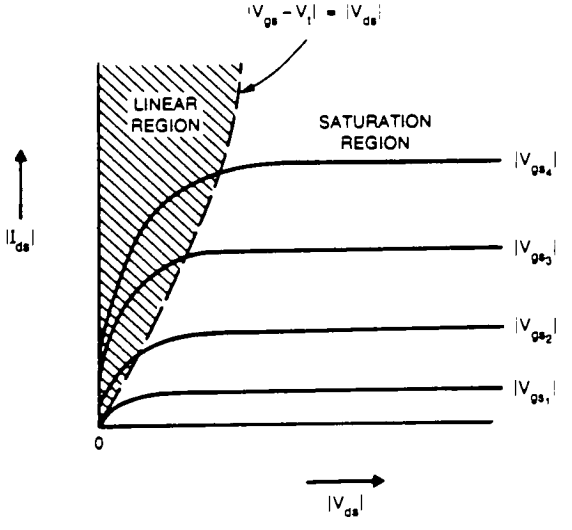
where $V_{FB}$ is the flatband voltage, $\phi_S$ the surface potential, $\varepsilon_{Si} \approx 11.8\varepsilon_0$ is the silicon permittivity, $N_a$ is the acceptor doping concentration in the substrate and $D_I$ is the dose of the threshold adjustment ion implant.
In addition, the absolute value of the threshold voltage decreases with an increase in temperature. This variation is approximately -4 mV/°C for high substrate doping level, and -2 mV/°C for low doping level.

**$\gamma$:** The threshold voltage of a MOSFET is altered when a source-bulk voltage $V_{SB}$ is applied. The body-bias (or body effect), $\gamma$, increases $V_{Tn}$ because $V_{SB}$ adds reverse-bias across the n-channel/p-substrate boundary which increases the bulk depletion charge. This is especially common when arranging of devices is needed to form gating functions in series.

Applying body effect increases the third term of the $V_{TOn}$ equation to $C_{OX}^{-1}(2q\varepsilon_{Si}N_a(\phi_S+V_{SB}))^{1/2}$. Thus, there is a $\Delta V_{Tn}$ increase given by $\gamma_n((\phi_S+V_{SB})^{1/2} - (\phi_S)^{1/2})$. Therefore, $V_{Tn}=V_{TOn}+\gamma_n((2\cdot ABS(\phi_F) + V_{SB})^{1/2} - (2\cdot ABS(\phi_F))^{1/2})$, where $\gamma_n = C_{OX}^{-1}(2q\varepsilon_{Si}N_a)^{1/2}\ [V^{1/2}]$, and ABS is the absolute value of the term in parentheses.[7],[8]

MOSFETs have three regions of operation: cut-off, linear and saturation. The terminal characteristics of the device are given by a plot of $I_{DS}$ against $V_{DS}$ for different values of $V_{GS}$. All voltages are referenced with respect to the source voltage, which is assumed to be at ground potential in this case. The source and substrate are assumed to be connected together. The characteristic curves are shown in Fig. 4.

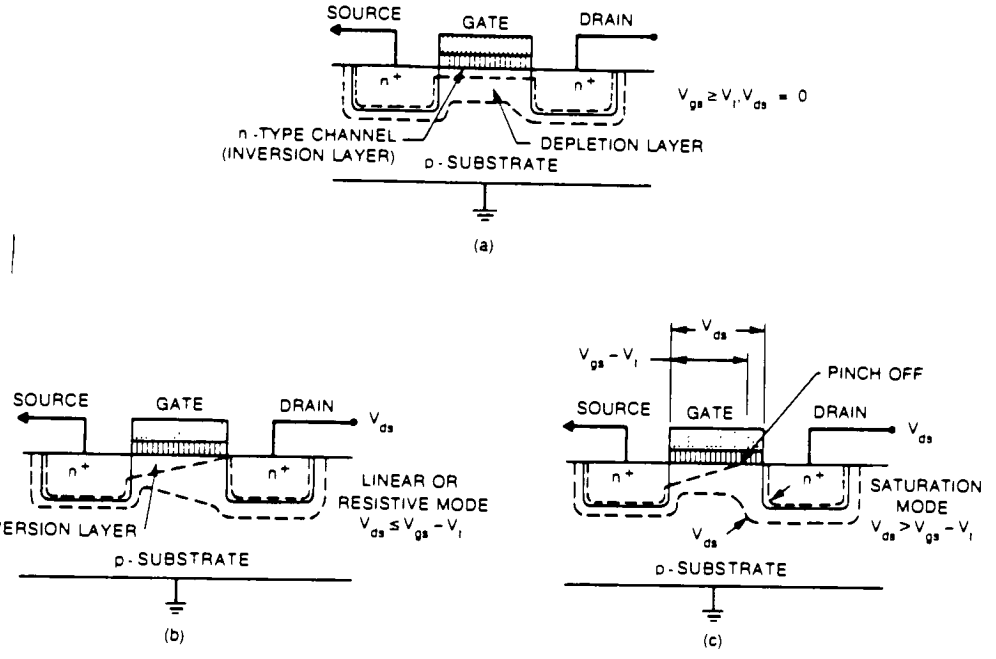
Figure 4 - I-V Characteristics for n- & p-transistors




These characteristics, as mentioned earlier, are extracted from the electron (or hole) inversion layer under the gate which forms the

conduction channel from drain to source. Modeling can be performed at various levels with the general tradeoff being complexity versus accuracy. The basic analytic models are obtained using charge control arguments within the gradual-channel approximation. Consider the crossection shown in Figure 5 below.

Figure 5 - nMOS Device Conducting Channel Behavior




To induce current flow, two conditions are necessary. First, $V_{GS}>V_{Tn}$ is required to create a channel. Second, $V_{DS}$ must be applied to produce the channel electric field **E**. This field forces electrons from the source to the drain, thereby giving current flow $I_D$ in the opposite direction.[8] After a rather complex set of derivations and integrations, several variables of interest are obtained. The first of these is the process transconductance $K_P$ (or process gain factor), which equals $\mu_n C_{OX}$

$[A/V^2]$. The device geometry plays a very important role, which is completely specified by the designer. This role forms the aspect ratio (W/L), which in turn determines the current. Since the aspect ratio is set by the device layout, it is the easiest parameter to control for circuit design. From this set of values, the device transconductance (or β) can be obtained from the equation $\beta = K_p(W/L)\ [A/V^2]$, and is used to characterize a specific device. From this set of equations and the gradual-channel analysis, the basic device equations are obtained as follows.

There are, as mentioned before, several models that can be considered. Among them are the square-law model, the bulk-charge model and the simplified bulk-charge model. The square-law model assumes that $V_{Tn}$ is a constant in the channel. This model is usually chosen for circuit analysis due to the simplicity it shows. Since this approach ignores some fundamental device physics, errors are automatically introduced into the analysis. This should not be a problem as long as only general calculations are made with these equations.

A more accurate equation set is obtained by noting that the channel voltage V is underneath the oxide and increases the effective bias on the MOS system. On the other hand, the increased complexity can offset the desire for precision, particularly when performing calculator-based estimates. This is the main reason the square-law model is more commonly used for manual computations.

A simpler model which retains some of the accuracy of the bulk-charge analysis can be obtained by performing a Taylor series expansion on the voltage terms in the bulk-charge equation.[8] Including the body-bias factor and considering only first order terms gives

$$C_{OX}^{-1}(2q\varepsilon_{Si}N_a(2\cdot ABS(\phi_F)+V+V_{SB}))^{1/2} \approx \gamma(2\cdot ABS(\phi_F)+V_{SB})^{1/2} - \partial V,$$

where $\partial = \gamma/[2(2\cdot ABS(\phi_F)+V_{SB})^{1/2}]$ is the slope.

Thus, with the use of the current integral equation (see device physics bibliographical reference) and the above equations gives

$$I_{Dn} = (\beta_n/2)[2(V_{GS} - V_{Tn})V_{DS} - (1+\partial)V^2_{DS}].$$

The presence of the $(1+\partial)$ term reduces the current to a more correct value. The threshold voltage is interpreted as the value needed to invert the surface at the source end of the channel. The saturation voltage is given by $V_{DS,sat} = (V_{GS} - V_{Tn})/(1+\partial)$, which in turn give

$$I_{Dn} = [\beta_n/(2(1+\partial))](V_{GS} - V_{Tn})^2[1 + \lambda(V_{DS} - V_{DS,sat})].$$

The accuracy of these analytical models is limited by the fact that the gradual-channel approximation is a 1-dimensional approximation to the 3-dimensional MOSFET structure. Computer simulations provide the key to understanding the details of the transistor operational modes. Now, the effective channel length is a factor to consider when scaling is present in the design of structures for VLSI systems. This channel length can be approximated by: $L_{eff} = L - [2\varepsilon_0(\varepsilon_{Si}/qN)(V_{DS} - (V_{GS} - V_{Tn}))]^{1/2}$. This

is a simple way to approximate the effects of the channel length modulation factor $\lambda$, which is ever present in the current-voltage relationships in MOSFETs. In the case of pMOS transistors, the same equations apply, only changing some signs to make up for the differences in threshold voltage effects, as well as other intricacies of the device physics of holes as majority carriers. Moreover, there have to be factors to make up for the fact that the drift and maximum velocity of the carriers in n-type devices is about 2.5 times that of p-type devices.

Continued discussion of the details of MOSFETs could lead to a long discussion of facts and equations that are hard to visualize and too complex for the scope of this thesis. Therefore, the relevant equations to consider, as well as others that relate them to others are shown in table 2 as follows. It is left to the reader to study the theoretical concepts behind those equations and parameters of interest in this table.

Table 2

MOSFET Characteristic Equations of Relevance

| **Equation (Relationship)** | **Description** |
|---|---|
| *Threshold Voltage Related* | |
| $V_{FB} = \Phi_{GS} - (Q_f/C_{OX}) - C_{OX}^{-1}\int_0^{x_{OX}} (x'/x_{OX})\rho_{OX}(x')dx'$ | Flatband Voltage |
| $\Phi_{GS} = \Phi_M - \Phi_S$ (metal gate) | Work function difference between Gate & Substrate. |
| $\Phi_{GS} \approx -(kT/q)\ln((N_a N_{d,poly})/n_i^2)$ (polysilicon gate) | " " |
| $kT/q$ | Thermal Voltage |
| $q = 1.602E\text{-}19$ Coulombs | Electronic Charge Constant |
| $k = 8.62E\text{-}5$ eV/°K | Boltzmann Constant |
| $\phi_S \approx 2 \cdot ABS(\phi_F)$ | Surface Potential |
| $ABS(\phi_F) \approx (kT/q)\ln(N_a/n_i)$ | Bulk Fermi Potential (p-type) |

table 2 (continued)

| Equation (Relationship) | Description |
|---|---|
| *MOS-Based Capacitance Related* | |
| $C_g = C_{OX}WL$ | Gate (G) capacitance |
| $C_{ol} = C_{OX}L_0$ | Overlap cap. per unit G width |
| $C_0 = C_{ol}W$ | Total overlap capacitance |
| $C_{0,GB} = C_{FOX}(L + 2L_0)w_0$ | Gate Overhang capacitance |
| $C_{FOX} = \varepsilon_{OX}/X_{FOX}$ | Field Oxide cap. per unit area |
| $C_{j0} = \varepsilon_{Si}/x_d$ | zero-bias cap. per unit area |
| $C_{jsw} = C_{j0sw}x_j$ | Sidewall cap./unit perimeter |
| $C_{sw} = C_{jsw} \cdot l$ | Total sidewall capacitance |
| $x_j$ | Junction depth |
| $l$ | Tot. perimeter length |
| *Channel Capacitances* | |
| $C_{gs} = nC_g$ | Gate-source channel cap. |
| $C_{gd} = nC_g$ | Gate-drain channel cap. |
| $C_{gb} = nC_g$ | Gate-bulk channel cap. |
| n = 0.5 (linear) or 0.667 (saturation) | Avg. Multiplicative Constant |
| $C_{GS} = C_0 + 0.667C_g$ (worst-case) | Non-linear Gate-Source cap. |
| $C_{GD} = C_0 + 0.5C_g$ (worst-case) | " " Gate-Drain cap. |
| *Parasitic Resistances* | |
| $R_{c(lin)} = (\beta(V_{GS} - V_T))^{-1}$ | Output resistance w/cnst. $\mu$ |
| $g_{m(linear)} = \beta V_{DS}$ | Transconductance |
| $g_{m(sat)} = \beta(V_{GS} - V_T)$ | " " |
| $R_{TOTAL} = R_C/N$ | Total contacts' resistance |

Note: This table is based upon equations and values found in [8]. For more info., please read Device Physics and VLSI Design theory bibliographical references.

### 2.2.2 Inverters

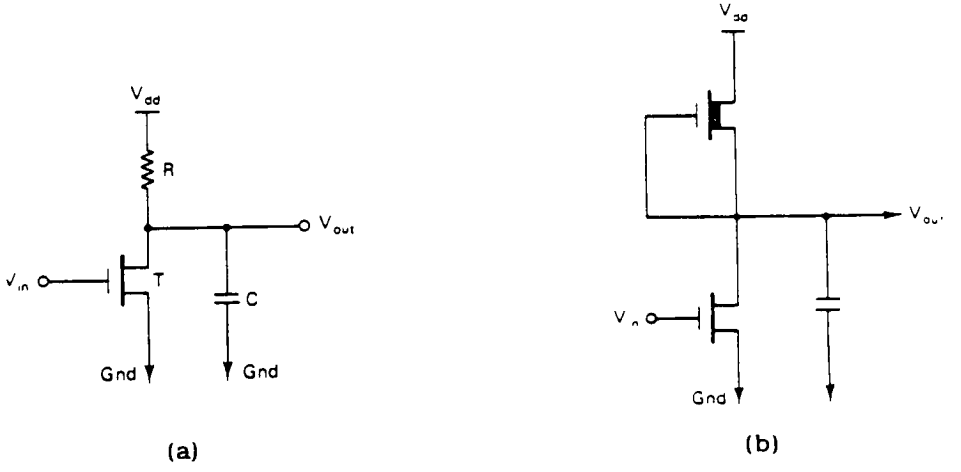
The simplest, and yet most fundamental logic structure beyond that of the MOSFET is the inverter. The reason for this is that any structure, whether nMOS, pMOS or CMOS can be reduced to an inverter equivalent which can hold the timing, capacitance and resistance characteristics of the larger structure. There exist two main types of

MOS inverters which are being used today. These are: the nMOS inverter consisting of two nMOS transistors, one depletion mode and one enhancement mode; and the CMOS inverter consisting of two enhancement devices, one nMOS and one pMOS. In order to understand the function and electrical differences between these two kinds of inverters, a discussion follows for each of them.

*2.2.2.1 The nMOS Inverter*

It consists of a "load" resistance R called the pull-up resistor, and a pull-down transistor T connected in series between supply voltage $V_{dd}$ and ground GND. The resistor is sized to limit the pull-up current to some fraction of maximum pull-down current provided by the transistor.[9] This is shown in Fig. 6 below.

Figure 6 - nMOS Inverter Basic Structure




As can be seen above, the input voltage $V_{in}$ is applied to the gate of T, which provides a very high input impedance via the gate capacitance $C_g$. This, in turn, will drive a similar output capacitance C. If $V_{in}$ is less

than the threshold voltage of T, the load capacitance C will be charged to $V_{dd}$. Although $V_{out}$ will never be equal to $V_{dd}$ due to a small leakage current flowing through T, but it will approach it. If $V_{in}$ is raised beyond threshold, T will initially conduct in saturation, C will start discharging (pulling down $V_{out}$) and $I_{ds}$ will increase due to the large value of $V_{gs}$ ($V_{in}$) until T moves into the linear region of operation. When $V_{in}=V_{dd}$ the output voltage will be given by $V_{dd}(R_{ch}/(R_{ch}+R))$, such that $R_{ch}$ is the channel resistance at this point and R is the resistance due to the pull-up resistor. In order to have $V_{out}$ less than threshold $R \geq 4\ R_{ch}$ must hold.

In order to be able to achieve high speeds of operation, the value of R must be very small, but not smaller than 4 $R_{ch}$. There are two ways to achieve this. The first is using an integrated circuit resistor, which takes too much silicon area. The other is by using a depletion mode transistor as pull-up load (shown in Fig. 6b). Having this particular structure, after some mathematical derivations, yields the pull-down & pull-up equations and characteristics shown below.

Table 3

nMOS Inverter Characteristic Equations

*Pull-down Current Equations*

| | | |
|---|---|---|
| $I_{pd} = 0$ | when | $V_{in}-V_{th} < 0$ (off) |
| $I_{pd} = (\beta_d/2)(V_{in}-V_{th})^2$ | when | $0 \leq V_{in}-V_{th} \leq V_{out}$ (saturation) |
| $I_{pd} = \beta_d(V_{in}-V_{th} -0.5V_{out})V_{out}$ | when | $V_{in}-V_{th} > V_{out}$ (linear) |

such that $\beta_d = (\mu\varepsilon/T_{ox})(W/L)$

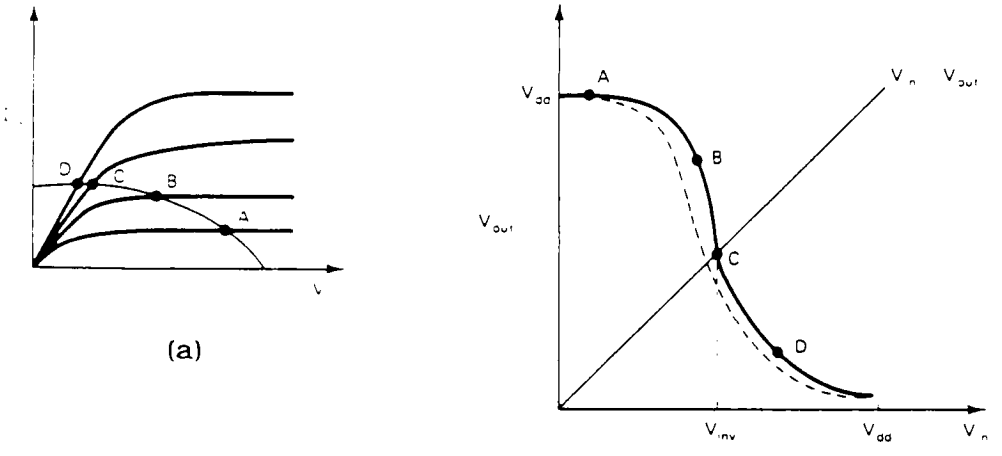
*Pull-up Current Equations (Depletion T always conducts since $V_{gs}-V_{dep} > 0$ holds)*

| | | |
|---|---|---|
| $I_{pu} = 0.5\beta_u(ABS(V_{dep}))^2$ | when | $ABS(V_{dep}) \leq Vdd- V_{out}$ (saturation) |
| $I_{pu} = \beta_u[\ (ABS(V_{dep}))-0.5(V_{dd}- V_{out})\ ](V_{dd}- V_{out})$. | | $ABS(V_{dep}) > V_{dd}-V_{out}$ (linear) |

such that $\beta_u = (\mu\varepsilon/T_{ox})(W/L)$

Superimposing the operating curves of both transistors, we obtain the characteristic curves for the nMOS inverter. This is possible since $I_{ds}$ flows in both pull-up and pull-down transistors. Thus, the voltage transfer curve is as shown in Fig. 7b below along with the $I_{ds}$ versus $V_{out}$ curve (Fig. 7a).

Figure 7 - nMOS Inverter Characteristic Curves




Point A in these curves above corresponds to pull-down off, pull-up linear; point B represents pull-down saturated, pull-up linear; point C shows because both are saturated and D because pull-down becomes linear and pull-up remains saturated. When the pull-down is turned off, the circuit will provide faster charge and discharge times for the load capacitance. The most important relationship of this circuit is that which shows the switching point, that is, the relationship where $V_{out}=V_{in}=V_{inv}$. Equating pull-up and pull-down currents, and after several other considerations and derivations yields

$$V_{inv} = V_{tpd} + ((V_{dd} - V_{out})/(\beta_{inv})^{1/2})$$

where $\beta_{inv} = \beta_{pd}/\beta_{pu} = (W/L)_{pd}/(W/L)_{pu}$

Finally, the time delay (or propagation delay) of the inverter is always a parameter of interest. The reason for this is that it will determine the frequency of operation of larger structures and cycle times of complete systems. The derivation being rather complicated will be left to the reader to study in the bibliography presented at the end of this document. The only thing presented here is the end result which is

$$t_d = (C_{g\cdot sq.}/C_g)\tau_d$$

where $\tau_d = 2(V_{dd}-V_{lo})/[\ (\mu/L^2)(V_{inv}-V_{lo})(V_{dd}-V_{th}-0.5(V_{inv}+V_{lo}))\ ]$

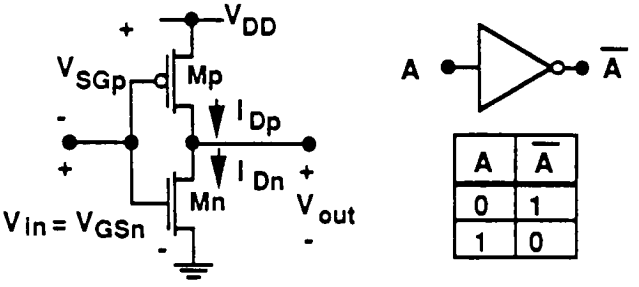
*2.2.2.2 The CMOS Inverter*

Much theory exists regarding this logic structure. Nevertheless, the emphasis not being the study of this gate, only a very short overview will be shown in this subsection. It is assumed that the reader is fairly familiar with the CMOS inverter. Moreover, it is also assumed that any further study necessary for the understanding of the methodology of Chapter 3 will be pursued by the reader. With this in mind let us review the characteristics and DC operation of the CMOS inverter.

The CMOS inverter is quite simple and is built using two opposite-polarity MOSFETs in a complementary manner. The circuit gives a large output voltage swing and only dissipates significant power when the input is switched; these are two important properties of CMOS logic

circuits.[10] The inverter is realized by the series connection of a p- and n-device, as shown in Fig. 8 below.

Figure 8 - CMOS Inverter




| A | $\overline{A}$ |
|---|---|
| 0 | 1 |
| 1 | 0 |

In order to derive the DC transfer characteristics for the inverter,one must first consider the regions of operation for the devices that make it up. These are shown below.

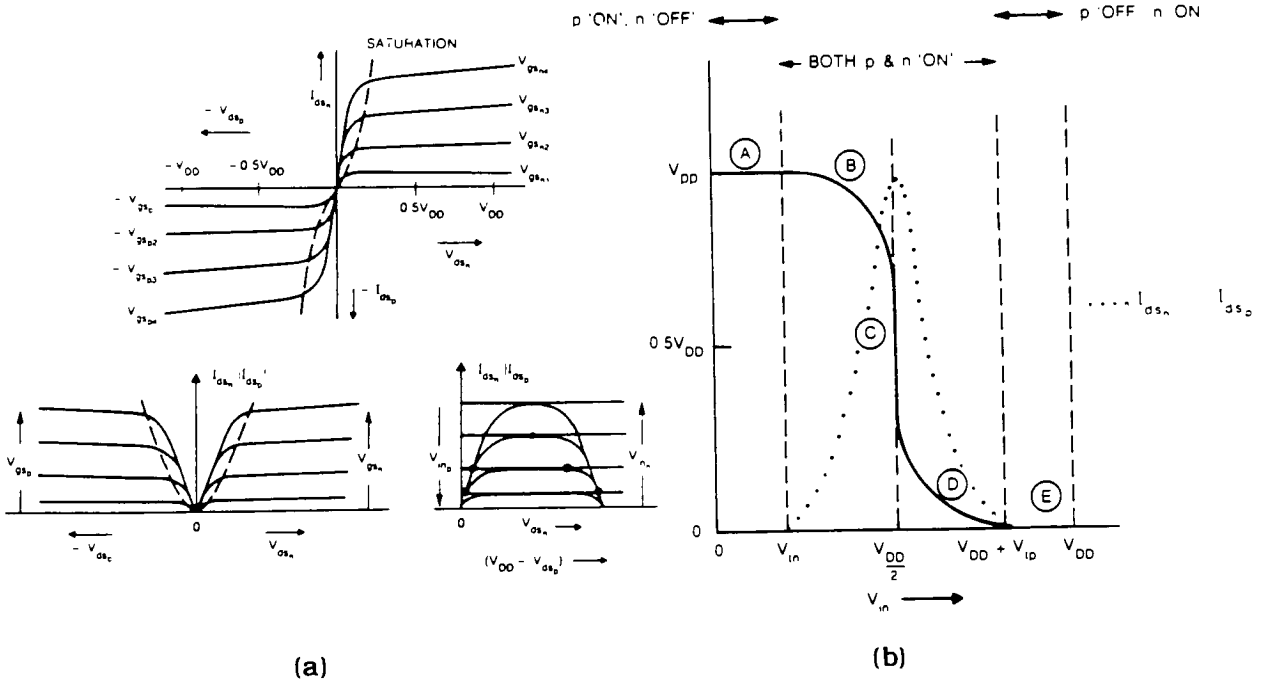
Table 4

Voltage Relationships for the CMOS Inverter's Regions of Operation

| Device | Cutoff | Linear | Saturation |
|---|---|---|---|
| p-device | $V_{gsp} > V_{tp}$; $V_{in} > V_{tp} + V_{DD}$ | $V_{gsp} < V_{tp}$; $V_{in} < V_{tp} + V_{DD}$<br>$V_{gdp} < V_{tp}$; $V_{in} - V_O < V_{tp}$ | $V_{gsp} < V_{tp}$; $V_{in} < V_{tp} + V_{DD}$<br>$V_{gdp} > V_{tp}$; $V_{in} - V_O > V_{tp}$ |
| n-device | $V_{gsn} < V_{tn}$; $V_{in} < V_{tn}$ | $V_{gsn} > V_{tn}$; $V_{in} > V_{tn}$<br>$V_{gdn} > V_{tn}$; $V_{in} - V_O > V_{tn}$ | $V_{gsn} > V_{tn}$; $V_{in} > V_{tn}$<br>$V_{gdn} < V_{tn}$; $V_{in} - V_O < V_{tn}$ |

This table, along with the current-voltage relationships of the MOSFET (see section 2.2.1) allow for the graphical derivation of the DC transfer curve and characteristic family of curves that defines the CMOS inverter. This is shown in Fig. 9 below.[11] As can be seen in Fig. 9a there are five points where the families of both n- and p-devices cross. These are the five points that define the five regions of operation shown in Fig. 9b and explained starting on pg. 35. This curve is found by solving for $V_{inn} = V_{inp}$ and $I_{dsn} = I_{dsp}$ in the equations that define the operation of n- and p-devices. During transition, both transistors in the CMOS inverter are momentarily 'on'; resulting in a short pulse of current drawn from the power supply (shown as a dotted line in Fig. 9b).

Figure 9 - Graphical Derivation of CMOS Inverter DC Transfer Curve & Operating Regions




(See reference [11])

**Region A:** n-device cutoff, p-device in linear region ($I_{dsn} = -I_{dsp} = 0$). Since $V_{dsp} = V_O - V_{DD} = 0$ then $V_O = V_{DD}$.

**Region B:** p-device in linear region, n-device saturated. At this point, $I_{dsn} = 0.5\beta_n(V_{in} - V_{tn})^2$, $V_{gsp} = V_{in} - V_{DD}$, $V_{dsp} = V_O - V_{DD}$ and $I_{dsp} = -\beta_p[(V_{in} - V_{DD} - V_{tp})(V_O - V_{DD}) - 0.5(V_O - V_{DD})^2]$. Thus,
$V_O = (V_{in} - V_{tp}) + [(V_{in} - V_{tp})^2 - 2(V_{in} - 0.5\,V_{DD} - V_{tp})V_{DD} - (\beta_n/\beta_p)(V_{in} - V_{tn})^2]^{1/2}$

**Region C:** In this region both the n- and p-device are in saturation. $I_{dsp} = 0.5\,\beta_p(V_{in} - V_{DD} - V_{tp})^2$ and $I_{dsn} = 0.5\,\beta_n(V_{in} - V_{tn})^2$. Thus, $V_{in} = [V_{DD} + V_{tp} + V_{tn}(\beta_n/\beta_p)^{1/2}]/(1 + (\beta_n/\beta_p)^{1/2})$
It is the relationship above that provides the basis for defining the gate threshold $V_{inv}$, which corresponds to the state where $V_{in} = V_O$.

**Region D:** Here the p-device is saturated and the n-device lies in the linear region. The equations defining this state are $I_{dsp} = \beta_p(V_{in} - V_{DD} - V_{tp})^2$ & $I_{dsn} = \beta_n[(V_{in} - V_{tn})V_O - 0.5\,V_O{}^2]$
Thus, $V_O = (V_{in}-V_{tn}) - [(V_{in}-V_{tn})^2 - (\beta_p/\beta_n)(V_{in} - V_{DD} - V_{tp})^2]^{1/2}$

**Region E:** p-device is cutoff and n-device is linear. Thus, $V_O = 0$.

It is often desired to have a very steep transition between the two states of operation. The reason for this is the noise immunity maximization that occurs because of this steepness, as well as the voltage separation existing between the low noise-margin and the high noise-margin (as explained in section 2.3.2 of bibliography reference 4). On the other hand, there is some influence that is exerted by the $\beta_n/\beta_p$ ratio. This influence causes the transfer curve to shift either left ($\beta_n > \beta_p$) or right ($\beta_n < \beta_p$). Nevertheless, the output voltage transition remains sharp and the switching performance is not affected. This should be contrasted with the behavior of the nMOS inverter, where the

transition gain depends critically on the ß ratio of the pull-up and pull-sown transistors. Also, the ratio is rather independent of temperature, since both $ß_n$ and $ß_p$ are related to temperature in a similar manner and thus, the overall effect approximately cancels in the ratio. Nevertheless, the mobility of electrons and holes is affected and can cause shifts accordingly (see Section 2.2.1).

A point should be made about the noise margins being highly dependent on the threshold voltage values of both transistors. Thus, care should be taken when designing the inverter and when designing the process by which it can be obtained. One final point should be made with regard to the time delay of the CMOS inverter. Assuming that the length and width of both devices is the same, there will be a charging time ($t_c$ - or rise time from 10% to 90%) and a discharging time ($t_d$ - or fall time from 90% to 10%). The equations that define these times are

$$t_d = 8L^2V_{DD}/[\mu_n(V_{DD} - Vtn)^2] \quad \& \quad t_c = 8L^2V_{DD}/[\mu_p(-V_{DD} + ABS(V_{tp}))^2]$$

## 2.3 Statistical Theory (General Discussion)

Just as important as circuit and transistor theory are those concepts which are used to analyze the results obtained from manufacturing and design procedures. This is because it makes them reliable, precise, repeatable and robust. Concepts such as tests of means, analysis of variance (ANOVA), Nonparametric tests, capability analysis, reliability and repeatability (R&R) analysis, chi-square tests,

designs of experiments, etc. are of great importance for their analysis, inference and hypotheses testing outreach. Thus, descriptions of the general theory behind basic concepts which are important to this thesis will be presented very briefly.

The origin of modern statistics can be traced to two areas of interest, which, on the surface, have very little in common: government and games of chance. These methods, which at first consisted primarily of presenting data in the form of tables and charts, make up what we now call descriptive statistics. This includes anything done to data which is designed to summarize, or describe, without going any further; without to infer anything that goes beyond the data, themselves.

Although descriptive statistics is an important branch of statistics and it continues to be widely used, statistical information usually arises from samples, and this means that its analysis requires generalizations which go beyond the data. As a result, the most important feature of the recent growth of statistics has been a shift in emphasis from methods which merely describe to methods which serve to make generalizations; that is, a shift in emphasis from descriptive statistics to the methods of statistical inference. In these cases there are uncertainties because there is only partial, incomplete, or indirect information, therefore, the methods of statistical inference are needed to judge the merits of our results, to choose the "most promising" prediction, or to select a "most reasonable" course of action. This is the field of probability theory. Nevertheless, it has been suggested that the emphasis has swung too far from descriptive statistics to statistical inference, and that more

attention should be paid to the treatments of problems requiring only descriptive techniques. To accommodate these needs, some new descriptive methods have recently been developed under the heading of exploratory data analysis. Two of these which have quite a powerful outreach are the use of the histogram for graphical representations of data and Pearsonian coefficient of skewness for understanding the symmetry of the histogram and measure the skewness (tailing towards one way or the other). There are many others that should only be considered when necessary in order to analyze and understand samples and possibly infer generalizations out of them.

One concept which is well known is that of the tendency of data to group in a bell-shaped form called Gaussian, even though this might not be always the case in semiconductor manufacturing. This curve can be defined by the relationship $f(x) = \sigma^{1}(2\pi)^{-1/2}exp(-0.5(x - \mu / \sigma)^{2})$, such that *exp* is the exponential function ($e^{x}$). The normal curve that is expressed by the function above has an area under it which can be standardized by centering it around zero. Since the curve is symmetrical any area of interest will be determined by the equation $z = (x - \mu)/\sigma$ where x is the point of interest (usually the sample mean, $\mu$ is the actual mean (thus, standardized) and $\sigma$ is the sample standard deviation (roughly the standard deviation of the infinite population, thus standardized as well).

Now, having this very basic information about a particular sample, or set of samples from several populations many one can undergo large quantities of test that can determine information necessary for inferences. For example, having the means and standard deviations of

two samples, tests of equality of means against the assumed population mean can be performed. Others include: differences between means, paired data tests of means, tests concerning standard deviations, estimation of proportions, tests concerning proportions, r X c table analysis, goodness of fit, ANOVA (one-way, two-way, replications, Latin squares, curve fitting, regression analysis, Design of Experiments and if nothing else Nonparametric tests are available. Unfortunately it is not possible to discuss all of these topics in detail. Whatever techniques and/or tests are used for the methodology and its application have to be identified by the investigator and studied in detail to make the best use of them. If more information is desired about any of these topics, please read the bibliography presented at the end of this document. The only topics that will be discussed in this document will be those necessary to prove the usefulness of the method shown here and exemplified in Chapter 4.

It has to be pointed out that the theory discussed in this thesis is relevant to the development of the method discussed in Chapter 3. The reason for this relevance is that it has to be shown that it works for the simplest cases if it is to be extended over to more complex areas of investigation. More importantly, one of the major requirements for efficient experimentation is a solid prior knowledge of the process under investigation. Therefore, the need to understand the manufacturing process of integrated circuits, the design process of VLSI systems and the analysis techniques of statistical inference is vital to the proper application of this (or any other) methodology . With this in mind, let us turn to the explanation of the methodology being proposed here.

# Section 2

## *Methodology*

# 3

# MANUFACTURING CONSIDERATIONS

DFM can take many approaches to fulfill TQM goals that may be pending in any environment of interest. The approach taken in this thesis may or may not be the best applicable to the problem of integrated circuit performance prediction, but it certainly outlines a simple set of steps to follow in order to determine values of interest needed for improvement recommendations in both Design and Processing stages of VLSI systems. The reader is reminded that in order for any problem to be feasible there needs to be certain number of constraints and limits put on the problem. Otherwise, the problem can quickly become unmanageable and impossible to tackle methodically and in an orderly manner.

Therefore, a set of steps is shown and explained in as much detail as necessary to be able to apply it to a reasonable range of systems within the realm of IC design and manufacturing. For example, systems which are simple in design and of moderate size (less than a few tens of thousands of devices) can be characterized with this method. Also, systems of more complexity and larger number of devices can surely be partitioned to accommodate for the constraints put forth by this method in order to be a manageable problem.

## 3.1 Theory-based Problem Size Reduction

The objective here is to reduce the set of independent variables available for investigation to a manageable number. For example, in the case of MOSFET modeling, there are literally hundreds of variables that could have a wide range of values within their definitional ranges. It is impossible to investigate the effects of all of these variables and their interactions, as well as their effects on MOSFET and MOSFET-based systems performances simultaneously. This is an unfeasible problem that could not even be tackled in reasonable length of time by any currently available supercomputer. It is therefore impossible to be tackled in a manual or semi-automated fashion.

Even though the task of problem-size limiting may be an obvious one to the experienced researcher, it is not a trivial one. This is exactly why its importance is pointed out. Moreover, this task must be properly considered to achieve any goals set out in advance of the research effort.

There are some techniques available to aid the investigator. Most importantly, knowledge and experience will be the irreplaceable basis from where to begin. This will allow one to identify the most influential (performance-hindering) independent variables and the dependent variables which respond to the relationships of the earlier ones. Moreover, these dependent variables will be used for measuring the performance of the system (or any other characteristics) that may interest the investigator. Nevertheless, a brief explanation of some techniques that will ease the completion of this first step will be

discussed below.

### 3.1.1 Basic Tools & Techniques

*3.1.1.1 Pareto Principle*

A concept established by Vilfredo Pareto, an economist and sociologist who tried to prove that the distribution of wealth followed a consistent pattern in all societies and throughout history. Although the principle of the vital few and trivial many has been observed by numerous authors to apply to many activities, it was not generalized until studies made by J. M. Juran. The Pareto principle is predicated on the assumption that approximately 80% of the condition of a system is due to 20% of the variables affecting the system. There are two ways to apply this principle. The first is by graphically showing nothing more than a bar-and-line chart that plots two things. The first one is of course the condition one wishes to represent in bar form and the many categories or components that define this condition. The categories of the condition are charted in descending order of magnitude to segregate easily the vital few from the trivial many items. The second, and most important component, of the Pareto chart is the relative importance of each category of the condition to the overall total. This is shown by superimposing a cumulative line and % scale on the right of the chart.[12] *The applicability of the Pareto principle is to concentrate the problem-solving efforts on the vital few causes (20% or less) that account for the majority (80% or more) of the effects observed, instead of wasting efforts on the trivial many causes.*

The second way to apply the Pareto principle is by examining the

problem given and understanding the mathematical relationships that constitute it. From these mathematical relationships point out which of them are the most common and most influential variables. That is, understand the influential pattern that each of the constituents of the system (in this case VLSI system), has and count the number of instances in which a particular variable affects the mathematical relationships that exist. Thus, from these counts one can determine which of the variables are those which are most common and which are most fundamental to the system. These are most possibly the vital few variables and the rest (not so common or recurrent) are the trivial many.

*3.1.1.2 Cause and Effect Diagrams*

A C-and-E diagram is a method of identifying, in a systematic or orderly way, all possible causes that may be attributed to an effect or specific problem. The C-and-E diagram is sometimes called a "Fishbone" graph, or an "Ishikawa" diagram. The goal of using a C-and-E diagram is to outline the many causes that impact a problem or effect, and to promote brainstorming at each level of the diagram until the possible causes for a particular problem are exhausted. There are several steps for making a C-and-E diagram.[13] These are:

1.) Decide on the problem or effect to be analyzed. For example, the process gain, $\beta$.

2.) Draw a horizontal arrow from the left to right, and place the problem statement (or name) in a box on the right.

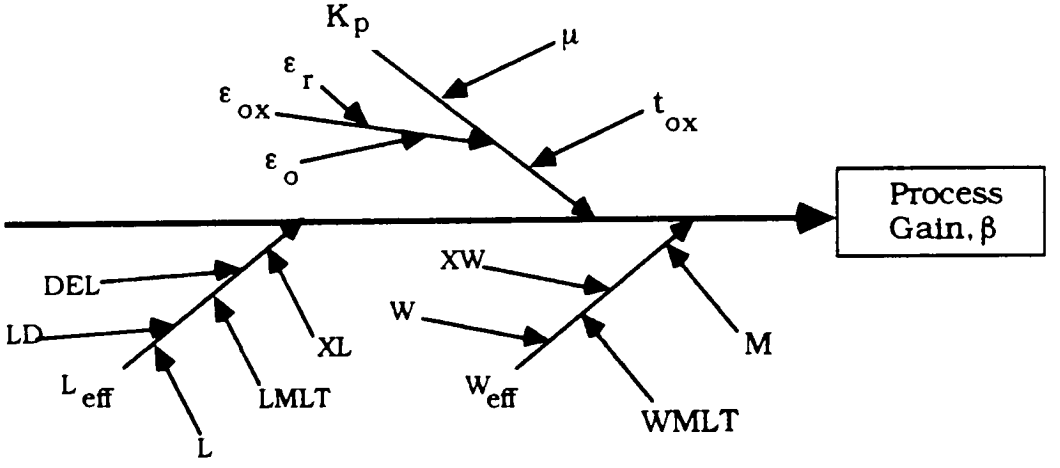
3.) Write the traditional major factor categories, or the main factors that may be causing the specific problem or effect. In the case of $\beta$ they are $K_p$, $W_{eff}$ and $L_{eff}$.

4.) Within each of these category items, list in the detailed factors that may be the causes for those categories and indirectly, the overall effect. This process is repeated until all possible causes to the problem have been covered for the category being considered.

5.) Finally, make sure that all the items that cause (or may cause) the effect be included in the diagram.

The final diagram with respect to the process gain is shown below on Figure 10.

Figure 10 - C-and-E Diagram for Process Gain, β




*3.1.1.3 Machine/System Definition*

This technique is necessary in order to systematically determine what is under study and what is to be observed, as well as what affects the observed responses. There are a few steps to follow in this technique. They are:

*(a)* Describe all the functional characteristics of the machine or

system under study.

*(b)* List the distinguishing features or qualitative peculiarities added to the input (product or independent variables) by the machine/system (response or dependent variables)

*(c)* List the independent variables internal to the machine/system not to the process (exclude environment, manpower, etc.)

*(d)* Form a Cause-and-Effect Cross-reference between the independent variables (causes) and the dependent or response variable(s) (effect(s)) for each functional category characteristic defined. Then mark with an 'X' the independent variables that are theorized to influence the variability of the response variable. Finally, rank order the independent variables. A C-and-E diagram might prove useful in organizing the inputs in order to identify the independent variables in each Functional Characteristic of the machine or system under study. The Cause-and-Effect Cross-reference table helps to identify the independent variables that are:

*1)* Most important for the machine or system, and
*2)* Most important for each dependent (response) variable.

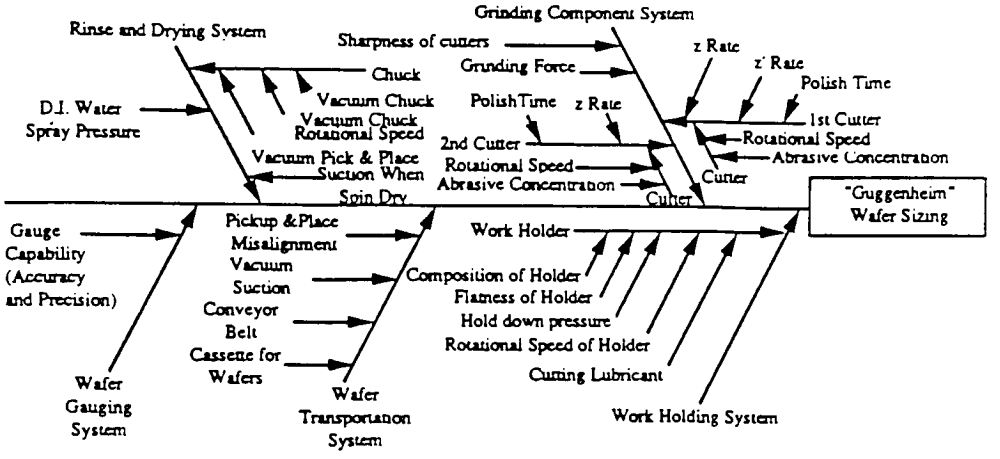
The independent variables are in:

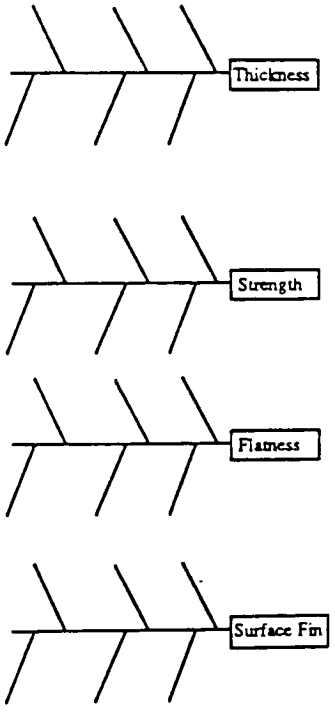
*1)* Rank-order of importance, or
*2)* Rank-order of influence to variability (Pareto principle) to the dependent variable.[13]

An example (important in IC industry, yet unrelated to this thesis) is shown in Fig. 11 (pg. 48). With these techniques in mind, as well as the basic (and indispensable) requirement of a solid knowledge of the subject under investigation, we now turn to applying these concepts to the nMOS inverter.

# Figure 11 - Machine/System Definition Summary

Includes C-and-E diagram, C-and-E Cross-reference table and sub-C-and-E diagrams for each dependent variable to be filled out. More details found in Appendix A.




Program — MACHINE/PROCESS CAPABILITY STUDY — Study #
Responsible Person — C&E Cross-reference Table — Date
Operation
Equip #
Machine/Process — Page of
RANK-ORDER: ☐ Yes ☐ No

| DEPENDENT → / INDEPENDENT ↓ | Thickness | Strength | Flatness | Surface Finish | | | | TOTAL | LEVEL OF INDEPENDENT |
|---|---|---|---|---|---|---|---|---|---|
| 1st Cutter z Rate | X | X | X | X | | | | 4 | |
| 1st Cutter Abrasive Conc | X | X | X | X | | | | 4 | |
| 1st Cutter z' Rate | X | X | X | X | | | | 4 | |
| 2nd Cutter Polish Time | X | X | X | X | | | | 4 | |
| 2nd Cutter z Rate | X | X | X | X | | | | 4 | |
| 2nd Cutter Abrasive Conc | X | X | X | X | | | | 4 | |
| 1st Cutter Spin Speed | X | X | | X | | | | 3 | |
| 1st Cutter Polish Time | X | X | | X | | | | 3 | |
| 2nd Cutter Spin Speed | X | X | | X | | | | 3 | |
| Rotational Speed of Holder | X | X | | X | | | | 3 | |
| Grinding Force | | | X | X | | | | 2 | |
| Flatness of Holder | | X | X | | | | | 2 | |
| Cutting Lubricant | | | X | | | | | 1 | |
| DI Water Pressure Spray | | X | | | | | | 1 | |
| Gauge Capability | | | X | | | | | 1 | |
| Pick & Place Misalign | | | | | | | | | |
| Vacuum Suction | | | | | | | | | |
| Conveyor Belt | | | | | | | | | |
| Cassette for Wafers | | | | | | | | | |
| Composition of Holder | | | | | | | | | |
| Hold Down Pressure | | | | | | | | | |
| Sharpness of Cutters | | | | | | | | | |
| Vacuum Chuck Dry & Rinse | | | | | | | | | |
| Vacuum Chuck Spindle | | | | | | | | | |
| Vacuum Pick & Place | | | | | | | | | |
| Suction when Spin Dry | | | | | | | | | |

### 3.1.2 Application to the nMOS Inverter System

In order to visualize the application range of the method outlined in this second section of the thesis, one would have to dedicate large amounts of efforts and time into exemplifying all the types and all the sizes of systems that could be analyzed, modeled and have their performances predicted using it. Nevertheless, in order to prove the point of its intended use, a fundamental case will be studied in simple terms as follows, any weaknesses of the method will be noted and a set of results will be tabulated and/or plotted.

nMOS technology is an old one, which has now been almost discarded and carefully replaced by both CMOS and BiCMOS technologies. Nevertheless, it was very important in the development of integrated circuits as a whole. It provided higher integration densities, faster speeds of operation and more structural complexity than that achieved in metal-gate pMOS technologies.

But, these are not the main reasons why this particular structure (or system) was chosen. The main two reasons are: first, it is the basic structure for digital integrated circuit systems in this (or any other) technology. The second reason is that the nMOS processing technology at Rochester Institute of Technology is mature enough to be studied thoroughly and it is capable of providing the database needed for this particular research methodology; something which, at this point, the CMOS process cannot.

In chapter 2 the theory behind nMOS transistors and the nMOS

inverter were explained in some detail. It was nevertheless a short description and was assumed that the reader would be fairly familiar with this system. Also, as was seen in chapter 2, for each of the transistors that form the inverter, there are more than one hundred variables that could affect the modeled performance of the circuit (in HSPICE and approximately 48 in SPICE). Nevertheless, in most cases, there are many variables that are not necessary or that can simply be regarded as constants throughout the analysis.

More importantly, there are particular standard measures of performance for the inverter. They are: inversion voltage ($V_{inv}$), propagation delay time ($t_d$), Gain and the $I_{ds}$-$V_{ds}$ curves. Out of these four metrics, device physics theory and software modeling techniques (such as HSPICE), one can obtain all kinds of parameters that affect each of them, as shown in table 1 (pg. 14). Certainly all parameters could be taken into consideration, but most of them only produce negligible effects that will not commonly be important until submicron feature sizes or high-frequency (RF) applications. Since this is only a basic system, certainly more than a few of the parameters will be either discarded or made constant for all cases. A more detailed analysis of this procedure is shown in Appendix B at the end of this document for all of the metrics above. Only the results are shown in Table 5 (pg. 51).

In reality, there are many variables affecting the performance of the inverter. For example, ohmic resistances are not constant, but vary depending on the diffusions made. Nevertheless, they are not considered here since the most fundamental causes that, repeated times, appear

Table 5
nMOS Inverter Performance: The Vital Few Causes

| Name | Symbol | Influencing Causes |
|---|---|---|
| Inverter Voltage | $V_{inv}$ | $x_j$ & $t_{ox}$ |
| Gain | k | $x_j$ |
| Time delay | $t_d$ | $R_{sh}$, $t_{ox}$, $x_j$, $f$ (freq.) |
| Current-Voltage Relationships | $I_{ds}$ vs. $V_{ds}$ -$V_{gs}$ curves | $x_j$ & $t_{ox}$ |

throughout the mathematical models of the inverter are those shown above. Maybe in more detailed studies that could be pursued, the importance of those variables could be addressed and their impacts analyzed in detail.

It should be noted that the techniques outlined in section 3.1.1 were not used as outlined. They were, nevertheless, used in principle. If one reviews Appendix B, one will notice that both a description (or definition) of each of the metrics was made there and a definition of the entire system was made in chapter 2. The important parameters were sorted out according to their relative importance and recurrence (according to the Pareto principle) and they were summarized on a table (in a modified C-and-E table) above. It should also be noted that, even though $V_t$ is dominated by $V_t$ -adjustment implant steps, due to their uniform distribution, no statistical analysis would be possible.

## 3.2 Influential Processing Steps' Identification

A very important second step is that of identifying those processing

steps which have an impact on the variables of interest. That is, certain semiconductor processing steps (or groups of steps) will give rise to specific values of the independent variables that were identified in step 1 of this method.

It is very important to recognize what steps have an effect on the variability of responses if this method is to succeed in its objectives. The reason for this is that the assessment of performance may very well be an intermediate goal in the process of improving quality of any particular product-process interaction. Without this realization, all the efforts put forth into the development and completion of steps followed here is to a certain point futile, because the goals of DFM are those of higher standards of quality and reliability in the arena of interest.

### 3.2.1 Basic Tools & Techniques

This particular objective may be accomplished in very simple or in very complex ways. It is important to notice again that a solid prior knowledge of the semiconductor manufacturing process is necessary to fulfill this objective. There are two ways to assess the information needed in this step (as mentioned before). The first technique is very simple and should always be backed up by an expert's opinion. This technique will basically look for the predefined process monitor and product parameters that relate directly or indirectly to the independent variables of step 1. Then, a rank ordering of importance (Pareto principle) will be done to determine the vital few processing steps and the trivial many that have an effect on the predetermined variables of table 5. Moreover, this technique will look for the most direct ways for

obtaining the values needed for each of the independent variables. It should be stressed that this technique should always have the technical support of an expert in the subject in order to avoid any subsequent errors that might occur otherwise.

The second technique is a more involved procedure, but will certainly determine each of the determinants of any independent variable being considered since step 1. Expert knowledge of the semiconductor process is very necessary to succeed in this technique. In this case, process characterization is necessary to understand the factors that affect each of the variables that are to be used subsequently. Moreover, each of those factors should be investigated further to understand the impact on the particular value obtained for any variable being affected by them. Furthermore, a sub-process definition (as explained below) should be made, which will determine the steps and all the characteristics associated with each of them. Finally, regression analysis should be done to determine the independent variable-to-process step(s) relationship(s) that exist in order to better predict performance on a particular product that runs through the process under scrutiny.

The sub-process definition consists of the following steps:

*(a)* Identify and describe all the sub-process characteristics external to the machine that may influence the machine or equipment under study (i.e. environment, previous process output, materials, etc.).

*(b)* List the distinguishing features or qualitative peculiarities added to the input (product) by the sub-process (responses). These qualitative features are of two kinds: Dissectible characteristics

which are measurable during the process of manufacture at successive process stages (e.g. wafer thickness); and Nondissectible characteristics which cannot be measured during the progress of fabrication process and do not even exist until a whole series of manufacturing operations have been performed (e.g. hFe (gain)). There are ways to measure nondissectible characteristics. This is done as follows:

*(i)* Convert the nondissectible characteristics to dissectible by measuring related but dissectible characteristics and/or creating a new instrument of measurement.

*(ii)* Correlate independent (process) variables with product results (regression analysis) to better identify and control the dominant ones.

*(c)* List the independent variables of the sub-process (external to the machine) that may influence the output (product). Create FIshbone diagrams for each of them.

(d) Form a Cause-and-Effect Cross-reference between the causes and the response variables for each sub-process category characteristic defined. This is done the same way as explained in the techniques mentioned for step 1 of this thesis' methodology.

### 3.2.2 Application to the nMOS Inverter System

After careful considerations, and knowing that my expertise is limited coming from the design side of the environment, it has been determined that the first and simpler technique will be used. The reasons are well outlined in section 3.2.1 above.

In this technique, there is a need for understanding and being familiar with the process used for manufacturing. Such prior knowledge was made available to the author through courses taken at R.I.T. which dealt in detail with the nMOS technology and which stressed the laboratory experience of fabrication under such predefined processes.

At R.I.T. there is currently a 51 step (6 mask levels) process which results in nMOS analog and digital structures. It is also currently undergoing a revision which will allow for a broader spectrum of metrics and parameters to be obtained both in a monitor and product (after completion) manner. Nevertheless, the non-revised process can be found in Appendix C.

As seen in table 5, there are only three variables of main interest in this problem. These are: $x_j$, the metallurgical junction depth of the diffusion (active) region; $R_{sh}$, the sheet resistance of the diffusion regions; and $t_{ox}$, the gate oxide thickness. From Appendix C, one can realize there are many resistance and junction depth measurements, but only one thin oxide thickness measurement.

One should be careful only picking the correct sheet resistance and junction depth measurements needed for the performance modeling. For example, steps 13 and 14 obtain both a junction depth and a sheet resistance measurements, but these refer only to the field oxide region and its field threshold adjust implant, and thus are unimportant to a point. At Step 19 the depletion transistor's threshold adjust ion implant and at step 22 the enhancement threshold adjust implant are made. At

steps 26 and 27 another set of junction depth and resistance measurements are made. This time they refer to the threshold adjusts of the two devices of the inverter, and thus, yet not definitive since there are still some diffusion steps ahead. Moreover, no clear results can be effectively correlated to the final values of the variables chosen at this point and therefore these steps will not be considered.

At step 25 there is a measurement made for the the thickness of the gate. This occurs after the oxide growth step made in the same step of the process. This is the first definitive variable that should be considered with its value range and variation.

At step 34 the doping of the gate is found by checking the resistivity. That is, using Irving's curves one could find the actual doping, by utilizing thickness of the oxide and the sheet resistance measurement to approximate the $R_{sh} \cdot x_j$ product.[20] Nevertheless, it can be neglected and its influence will not be major. The reason for this is that its influence only shows on the calculation of the work function $\Phi_{ms}$ as a factor within a natural logarithm function and can be approximated by the value of the energy gap.[21]

After the ion implant step which defines the drain and source regions of the transistors, step 39, one can make measurements which will reflect the variables of interest, for these will be final values on those regions. These measurements are made on steps 44 & 45 of this process. Finally, in order to obtain the time delay of the inverter, a ring oscillator should be measured at step 51 (test step of the RIT nMOS 2.0 process).

## 3.3 CIM Database Query for Steps & Variables of Interest

The next step on this methodology is that of obtaining the necessary information as outlined by step 2 for the variables of step 1. In the R.I.T. Factory a Computer Integrated Manufacturing (CIM) system is available for storing monitor (while processing is being done) and product (test data) information in a database system called MESA (previously called WIPTRACK). This database system is responsible for storing of instructions, documentation related to Fab equipment and measurement data. Access to instructions and other features of the system are restricted depending on a predefined hierarchy. Several types of access are unimportant and unrelated to this method. Therefore, the only access considered here is that which is related to measurement data.

Access to measurement data is accomplished either through MESA or through a database accessing system inherent to the IBM AS/400 system called Query. Access through MESA is done via selection of options of the main menu which directs the user to the desired information. Access through Query is more organized in the sense that it can obtain information from different sources by limiting or expanding the search in ways that MESA cannot do by itself. The two techniques are briefly explained below for introductory purposes. Nevertheless, it is expected of the investigator to learn and understand the database system(s) being used to store and retrieve relevant data in order to complete performance research through this methodology.

### 3.3.1 Tools & Techniques

*3.3.1.1 MESA Reports and Control Charts*

As mentioned above, the first technique for obtaining necessary information is by entering MESA in the engineering or faculty modes and selecting the correct menus to obtain certain data of interest (measurement data for independent variables in this case). There are two types of print out to obtain: reports and control charts. The steps to get any of them are as follows:

*(a)* Log on in engineering or faculty modes

*(b)* Select 6 (Plant/Security Menu), then

*(c)* Select 7 (Print Transaction Log Reports),

*(d)* Fill in the requested information at the window

*(e)* To obtain a report select 'N' for batch processing, Opt='2' and <CR>

This will produce a report with the requested information, even though it is limited to a small amount of data. The other print out that can be obtained is the control chart. In order to obtain this, the steps are as follows:

*(a)* Log on in engineering or faculty modes

*(b)* Type 3 (Data Collection Menu), then

*(c)* Select 5 (Control Chart - basic)

*(d)* Define the parameters necessary and limiting filters for the search. Two parameters are necessary: Parameter Group and Operation. Filters such as Product, Process, Revision, Owner code, Product class and Value allow for generation of limited-data control charts.

*(e)* Next, type the period of time in which to chart data, along with the range and scale desired.

(f) Then, the control chart will appear in the next window where data will be plotted against Lot number and date/time.

Unfortunately, there is no way other than print screen to obtain this information on hard copy. Moreover, there is little information to be obtained using this method, unless only a particular variable is of interest. There is no way to filter the search further and this leaves much room for improvements; improvements which Query is capable of giving.

*3.3.1.2 AS/400 Query Utility*

This is an IBM licensed program and a decision support utility that can be used to obtain information from the AS/400 database. It can obtain information from any database files that have been defined on the system using OS/400 data description specifications the OS/400 IDDU or SQL/400. Query is accessed through option 20 of the main menu of MESA. Query can be used to select, arrange, and analyze information stored in one or more database files to produce reports and other data files. Determination of what data query is to retrieve, the format of the report, and whether it should be displayed, printed, or sent to another database is done by the user. There are many details regarding the operation and intricacies of Query. They are beyond the purposes defined in this method. It is left to the reader to investigate these procedures and use them to the best ability needed.[14]

### 3.3.2 Application to the nMOS Inverter System

A database upgrade where the old database (WIPTRACK) was

replaced by the new one (MESA), for which several database redefinitions and storage library renamings, had to be made. This stopped the effort of obtaining a query that could span accross the entire nMOS v. 2.0 process. The reason was the lack of familiarity with the new system and the library redefinitions that pertain to the relevant data.

On the other hand, for the variables that were identified on step 1 of this methodology, because of the urgent need for obtaining updated figures with 50+ data points, a more detailed analysis was made. Due to the fact that the system was upgraded, and that libraries had been redefined, there was no knowledge of where the pertaining data could be found (as mentioned before). To get around this, several control charts were made for all the variables of interest, i.e., the steps of the process where data for these variables is collected. This was done for data starting on January 1, 1990 at 1:00 a.m. and ending July 17, 1993 at 7 p.m.

The MESA control chart results were obtained on hard copy. These are shown on Appendix D. It was found, through the control chart function of MESA, that there is no data available for step 51. That is, data regarding real measurements of threshold voltages (both depletion and enhancement), inversion voltage, ring oscillator frequency, sheet resistances (diffusion layer, metal layer, etc.) etc. was not found at all. This makes it impossible to achieve on the objective of comparing real data with simulation data. Although measurements could have been made, the lots which would produce the test results at step 51 are either non-existent or have been thrown away or given away by this point in

time. An effort is being done to emphasize this step's importance, but it will take some time to correct this lack of relevant data. The only possibility now is to make simulations and expect them to be accurate and precise. This, of course, simplifies the analysis section of this method quite a bit, but it is a simplification that was not desired here and should never be made.

# 4

# PRELIMINARY ANALYSIS

## 4.1 Descriptive Statistical Analysis of Raw Data

Once all the data related to each of the independent variables pointed out by step 1 of this method has been obtained as explained in step 3, certain meaning must be given to it. Descriptive statistics have been established for this particular purpose. Very simple formulas and graphing techniques exist to accomplish this objective.

### 4.1.1 Basic Tools & Techniques

For each independent variable one must find:

*(a)* The mean of the sample: the sum of all the numbers divided by the number there is of them. Mathematically expressed, $\bar{x} = (\Sigma x)/n$.

*(b)* The sample standard deviation: average distance or deviation of each number from the mean or average. Mathematically expressed, $s = \{[\Sigma(x - \bar{x})]^2 / (n-1)\}^{1/2}$

Moreover, control charts showing historical records of variation tendency at different times for the same independent variable and histograms (graphical technique that displays the central tendency of the data and its variability) should be made. The reason for this can be best explained by the famous cliché: "A picture is worth a thousand words." Examples of these descriptive techniques for raw data obtained from

querying the CIM system can be found in Appendix E for the entire measurement set of significance of the RIT nMOS process. In any page of this appendix one can find a number of different fields of interest. The first field is the title where relevant information about what is being portrayed is written. The second field contains the set of predefined nominal, upper specification limit and lower specification limit values. The third field contains the set of descriptive statistical values for the variable of interest. The fourth is a lot-by-lot history of values obtained. The fifth contains the histogram-related data (see bibliographical reference 6). The sixth is the actual histogram. The seventh is the control chart. Finally, the eighth contains all the capability calculations for the sub-process (though this is of no concern until the following step of the methodology).

There are many other descriptive statistics such as the mode, median, range, weighted mean, grand mean, frequency, cumulative frequency, mean of grouped data, etc. Nevertheless, the most important ones are those measures shown above.

With these measures one can understand the basic behavior of any particular independent variable as a function of the semiconductor process where it is found. The rest of the understanding comes from detailed analysis and capability determination that follows in the next step of this methodology. Let us now turn to the application of this section to the nMOS inverter.

### 4.1.2 Application to the nMOS Inverter System

Once all the measurement values have been obtained, a histogram, a historical control chart, the mean of the sample, the total count of values in the sample and the standard deviation should be obtained. These values are all shown in Appendix E for a previously completed job which reflects the data for the entire nMOS v. 2.0 process. The worksheets show a few values of interest (those mentioned above), plus others which are important for section 4.2. It should be noted that not all the worksheets contain upper and lower specification limits, since there was no need to include them when these worksheets were made. This is why the values of capability for steps which do not refer to the variables of interest are absolutely meaningless. Moreover, upper and lower control limits are not defined, since a stage of variability reduction across the entire process should be undergone before setting these control values.

As far as the data which describes the processing steps influencing the independent variables identified in step 1, a more detailed analysis can be noticed. That is, all the specification limits and capability values have meaning and correspond to realistic values. Also, more data points are found, for which the worksheets are longer. Nevertheless, they are of major importance for this section and section 4.2 and thus should be analyzed and statistically described in more detail. They are shown at the beginning of Appendix E.

One more point should be made before turning attention to the capability analysis. Due to the fact that students run the fabrication

facility, there are some errors that are bound to occur in the input of data for measured parameters. This is why certain amount of scrutiny must be made when considering the data from any particular parameter here. Even though this notion goes against the principle of randomization of statistics, the need for ignoring values which are far off those theoretically expected is crucial (as shown in Appendix D). Otherwise, the accuracy and precision of the study could be vastly thrown off by erroneous data that was input. Also, a need for safeguards against this sort of inputs should be established.

## 4.2 Capability Analysis of the Data

Once all the raw descriptions of the data (for each cause) have been obtained by following steps 1 to 4, there is a need to reduce the set of variables to a final number which is responsible for the most influences in the effects that are being studied (according to Pareto principle). This is why a detailed capability analysis should be made for those outstanding processing steps responsible for the raw data described in step 4. Before any of the analysis is explained, some concepts should be introduced in order to aid the completion of this step by anybody using this methodology. It should be noted that there are other techniques that can be used, but these are the ones that the author believes are most appropriate.

### 4.2.1 Basic Tools & Techniques

*4.2.1.1 Metrology Characterization*

This technique deals with the metrology, i.e., gauges, test equipment, and measuring instruments needed for measuring the response variables identified in the previous steps for any particular system being characterized. This technique also deals with tolerances, engineering, design, production, or customer specifications for each response variable under study. Even though it is not necessary to conduct a metrology characterization, it is recommended for it might give some insight into the possible sources of variation for any particular measurement made.

In a machine or sub-process, there may be many response variables. Not all the response variables carry the same importance; some are more critical than others. The response variables classified as being critical, are the ones that should be studied, and optimized.

A measuring instrument has to be identified to measure the response variables to be studied. In turn, the state of conformance of the response variables to specification should be determined, and this implies that a specification is needed. If a specification is not available for a response variable thought to be critical, the objective of this technique should most likely be geared towards determining a realistic tolerance for this response variable.

If a measuring instrument or gauge is not available for the response variable under study, this should not be an obstacle in studying

the response. There are external laboratories that may be able to measure the response variable with very sophisticated equipment. Other departments or productions facilities may have the instruments that are needed. Select the response variables based on their seriousness or importance in impacting the quality of the product turned out by the sub-process and/or machine. This is why one should not worry about the measurement until response variables have been identified. It is beyond the scope of this document to thoroughly explain this point any further. Please refer to appropriate sources for related concepts.[15]

*4.2.1.2 Gauge Capability*

This technique deals with the accuracy and precision of the measuring instruments used to collect data. Again, there is no real need for this technique, but it very well leads to a robust result determining sources of variation and defines the meaningfulness of the data obtained and described in step 4 of the methodology.

Measuring instruments are also subject to variation, therefore, a machine or process capability study cannot be meaningful unless the measuring instrument used to measure the response variables posses accuracy and precision. To increase the confidence in the results that may be obtained from a machine or process capability study, the measuring instruments must undergo a Repeatability and Reproducibility (R&R) study. This R&R study is done to: a) quantify the ability of the measuring instrument to reproduce the same results when different operators measure the same unit, and b) to quantify the ability of the measuring instrument to obtain virtually the same results when a

unit is measured more than once.

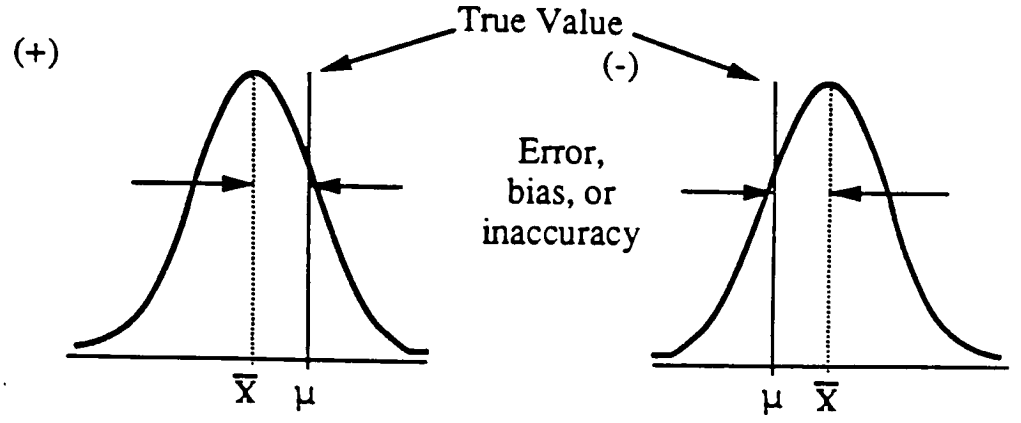
Repeatability is the amount of variation obtained by measuring the same unit (precision) with the measuring equipment. Reproducibility is the variation obtained in the average of measurement made by various operators measuring the same unit. The repeatability and reproducibility are then taken as a percentage of the tolerance of the response variable being measured and this is referred to as %R&R. This index tells, in percentage, the uncertainty of the measurements in comparison to the tolerance. The smaller this percentage the better the measuring instrument. If a measuring instrument has a high %R&R, the study should not continue, but rather the measuring instrument should be studied to reduce its sources of variation. Otherwise, a better measuring instrument or gauge should be recommended and used. This is an extremely powerful and useful technique for very complex and involved investigations that could be used by the method described in this section of the thesis.

There are two tools available at this level that should be explained in some detail. They are:

*(a)* Accuracy: this is the extent to which the average agrees with the 'true' value of the unit. The distance ($\mu$ - $\bar{x}$) is referred to as error, bias, or inaccuracy. This error or inaccuracy is the extent to which the measuring instrument is out of calibration. Bias can be either positive or negative (as shown in Fig. 12). The correction needed to put the measuring instrument in calibration is of the same

magnitude as the bias but opposite in sign.

Figure 12 - Instrument Accuracy Deviations Possible




A measuring instrument is considered accurate if the error is less than the tolerance for that grade of instrument. In some test equipment the tolerance is about 2% of the measurement. The measurement equipment should have the ability to measure to 1/10 of the total product tolerance range.

*(b)* Precision: a measuring instrument will not give identical readings even when making a number of measurements on the same unit. Instead the measurement will be scattered around the average. Precision is the ability of a measuring instrument to reproduce its own measurement, even if the measurement is incorrect. The quantification of precision is expressed in terms of the standard deviation, $\sigma$, of "replicated" measurements. Re-calibration can improve the accuracy of a measuring instrument by reducing bias; but it does not necessarily improve the precision of an instrument.

Precision is an inherent dispersion in a measuring system that can be reproduced and measured; and once known it is predictable. Precision is corrected by systematic, careful investigation with the aim at reducing the sources of variation.

There are some combinations to consider when there might be one of the two, or none of the two, or both accuracy and precision. There are also some ways to solve the problems that arise out of this combinations. This is beyond the scope of this document, as it is to give the investigator the step-by-step procedures for the gauge capability analysis. Please refer to appropriate sources for more detailed information in this regard.[16]

*4.2.1.3 Capability Determination*

The third technique is that of capability determination. The objective of this technique is to determine and quantify the ability of the machine to produce product within the specification limits (tolerance). This is done by determining the capability index, $C_{pk}$, and the process potential, $C_p$, for each response variable of the processing being used as independent variables for the overall method being proposed. Product is physically processed through the machine or sub-process and data is collected using a measuring instrument with an assumed good R&R. Then, the data collected is used to make predictions and inferences about the behavior of the machine or sub-process through time. Descriptive statistics are computed (as in step 4) to understand the central tendency of the data, to quantify the amount of variation, and to understand the shape of the sampling distribution. A goodness of fit test

is done by using the normal probability paper (or known analytical techniques) and validated using the skewness and kurtosis. As a requirement to capability, a stability test is done by charting the data in a control chart, and then analyzing the chart for presence of non-random patterns, or a test to detect out-of-control conditions. If a response variable (independent performance variable) shows a $C_{pk}$ lower than the goal, ($C_{pk}$ > 2.0 or whatever management has determined as a minimum), then one must proceed to optimize the capability, reduce the variability and then control the capability. This particular effort is beyond the scope of this document. Refer to the bibliography for more information in this regard.

In the paragraphs that follow, concepts, tools and techniques to determine the capability will be briefly explained. If any more insight is needed, it is recommended that the investigator following this method finds other sources where these concepts, tools and techniques are thoroughly explained and given explicit meaning.

The concepts, tools and techniques that are found useful in capability determination are:

*(a)* Frequency distributions (or histograms): this is a graphical technique that displays the central tendency of the data and its variability. It is divided into cells such that cell width (CW) is equal to the range divided by the number of cells and the range is the difference between the maximum and minimum values.

*(b)* Measures of Central tendency: they are the sample mean, median, mode, etc.

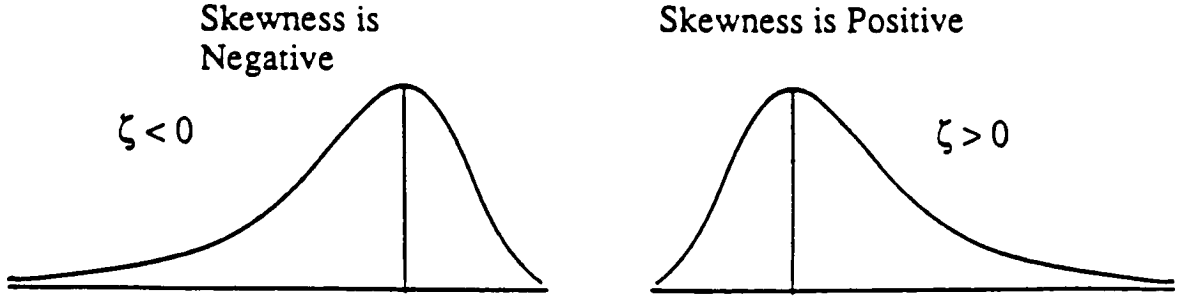
*(c)* Measures of Spread or Variability: range, standard deviation, etc.

*(d)* Measures of Shape: there are two of them:

*(i)* Skewness: a sampling distribution that is not symmetrical has more observations in one side of the tail of the distribution that in the other. A distribution with this characteristic is called a skewed distribution. Skewness is a statistic that quantifies this lack of symmetry in the skewness of the distribution. A positively skewed distribution has more observations in the negative (left) side of the distribution, whereas a negatively skewed has the majority of the observations in the positive side (right). For a perfect symmetric distribution the skewness equals zero. All this is shown in Figure 13 (next page). Normal sampling distributions have their skewness fluctuate around zero, an effect due to sampling variation. The equations that determine this characteristic are shown along in Figure 13 (next page).

*(ii)* Kurtosis: A sampling distribution that is symmetrical and is normally distributed has a kurtosis equal to 3.0 The kurtosis measures the peakedness of a distribution, or the clustering of observations around the mean or central point. It also measures the flatness of the distribution or the lack of clustering of observations around the central point. A distribution with more observations piled up in the center is called a leptokurtic distribution. A leptokurtic distribution is more peaked than a normal distribution, its kurtosis is greater than 3.0, and it tends to have fewer observations in the tails. On the other hand, a distribution with fewer observations around the central point is flat and is called a platykurtic distribution (kurtosis < 3.0). For

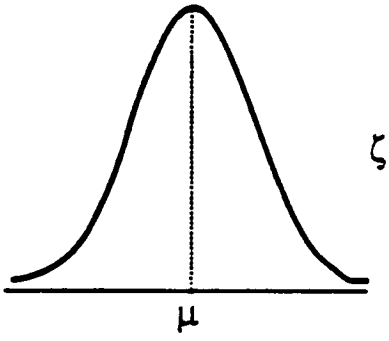
Figure 13 - Skewness




The moment about the mean:

$$\mu_\theta = \frac{\sum_{j=1}^{n} (x_j - \bar{x})^\theta}{n}$$

Normal Distribution




$\zeta = 0$

Skewness:

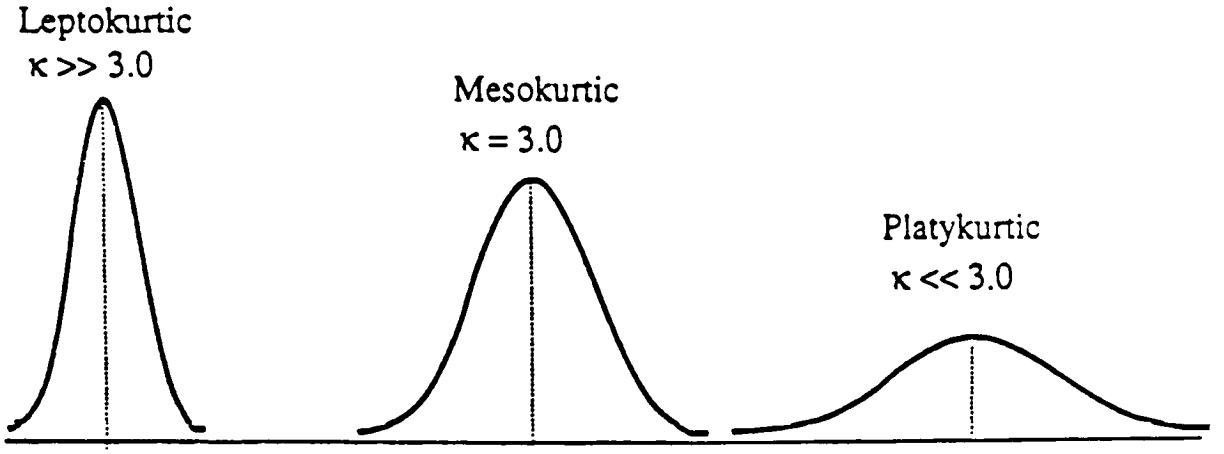
$$\zeta = \frac{\mu_3}{\sqrt{\mu_2^3}} \quad \text{or}$$

$$\zeta = \frac{\sum_{j=1}^{n} [(x_j - \bar{x})/S]^3}{n}$$

samples of normal distributions the kurtosis typically does not equal exactly three, again due to sampling variation. The equation and graphical display of kurtosis are shown in Figure 14 (next pg.).

*(e)* Percentiles (or Centiles): this is the point in a distribution below which a certain percent of the cases fall. The nomenclature for centiles is Cn, where the C stands for centiles and the n for the

Figure 14 - Kurtosis




$$K = \frac{\mu_4}{(\mu_2)^2} \qquad \text{or,} \qquad K = \frac{\sum_{j=1}^{n}[(x_j - \bar{x})/s]^4}{n}$$

Where $\mu_\theta$ is the $\theta$ th moment about the mean.

percentage. The formula and steps in calculating centiles are given below.

**Formula:** $C = ll + \dfrac{N \cdot p - cf}{fi}$

**ll** = lower limit of interpolated interval
**N** = number of cases
**p** = proportion equivalent of desired centile
**cf** = cumulative frequency of cases below the interval in which we are interpolating
**i** = size of the interval
**fi** = frequency of the interval in which we are interpolating

**Steps in calculating the centile:**

1.) Take the percentage of **N** (sample size).
2.) Find the interval in the frequency table with **N·p** points below it. Start counting from the bottom. IF the next interval exceeds the **N·p**, then that interval has to be interpolated.

3.) Obtain the lower limit, **ll**, of the interpolated interval.
4.) Obtain the cumulative frequency, **Cf**, of the cases below the interval in which the interpolation is being done.
5.) Obtain the frequency, **fi**, of the interval in which we are interpolating.
6.) Obtain the size of the interval, **i**.

*(f)* The Ogive curve (or accumulative frequency distribution): it is a curve that results from plotting the cumulative percentages (C%) against their respective centiles. This curve is also known as the S-shaped curve. The Ogive curve is adequate when it is desired to display all the centiles for a set of data. The steps to construct an ogive curve are:

*(i)* Calculate the cumulative frequency, **Cf**, by adding the total number of cases below the top of the intervals.

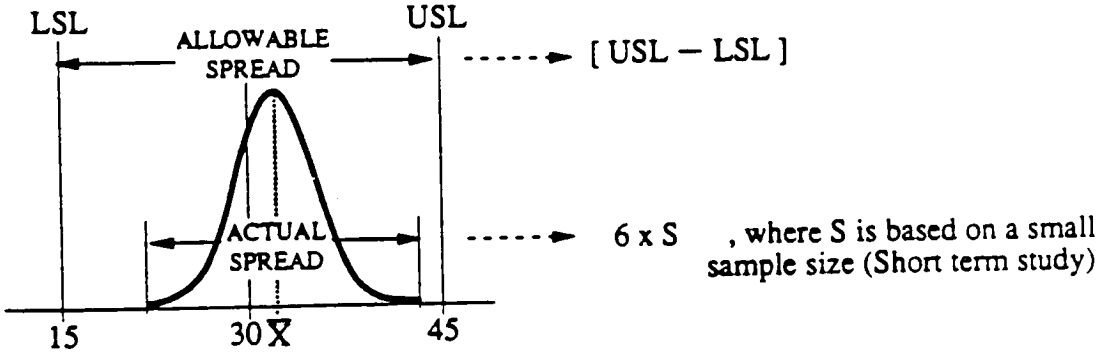
*(ii)* Convert each of the **Cf** into a cumulative proportion by dividing **Cf** by the total number of samples taken.

*(iii)* Obtain the cumulative percentages, **C%**, by multiplying each **Cf** by 100.

*(g)* Machine/Process Potential ($C_p$): The $C_p$ is a process potential index that measures the potential of capability of a machine or process. The $C_p$ is the ratio of the allowable spread over the actual spread. The allowable spread is the range or tolerance of the specification, and its calculated by subtracting the LSL from the USL. The actual spread is the spread from data collected from the machine or process and it is calculated by multiplying 6 times the standard deviation, s, of the data. A high value of $C_p$ does not guarantee that the process is capable producing product within specification. Furthermore, the whole distribution of the process

might not overlap with the specification range. $C_p$ does not measure the location of the average of the actual spread with respect to the target of the allowable spread; it only compares their widths. The capability index, $C_{pk}$, measures the degree of centering of the actual spread versus the allowable spread. The $C_p$ may only be calculated when two sided specifications are available. Numerical properties such as addition and averages, cannot be applied to the $C_p$ because it is a unitless index and would not yield meaningful information other than that which it contains. The equations for it and a graphical description are shown below in Figure 15.

Figure 15 - Machine/Process Potential




$$Cp = \frac{USL - LSL}{8 \times S} \quad \text{(Short Term Study)}$$

$$Cp = \frac{USL - LSL}{6 \times S} \quad \text{(Long Term Study)}$$

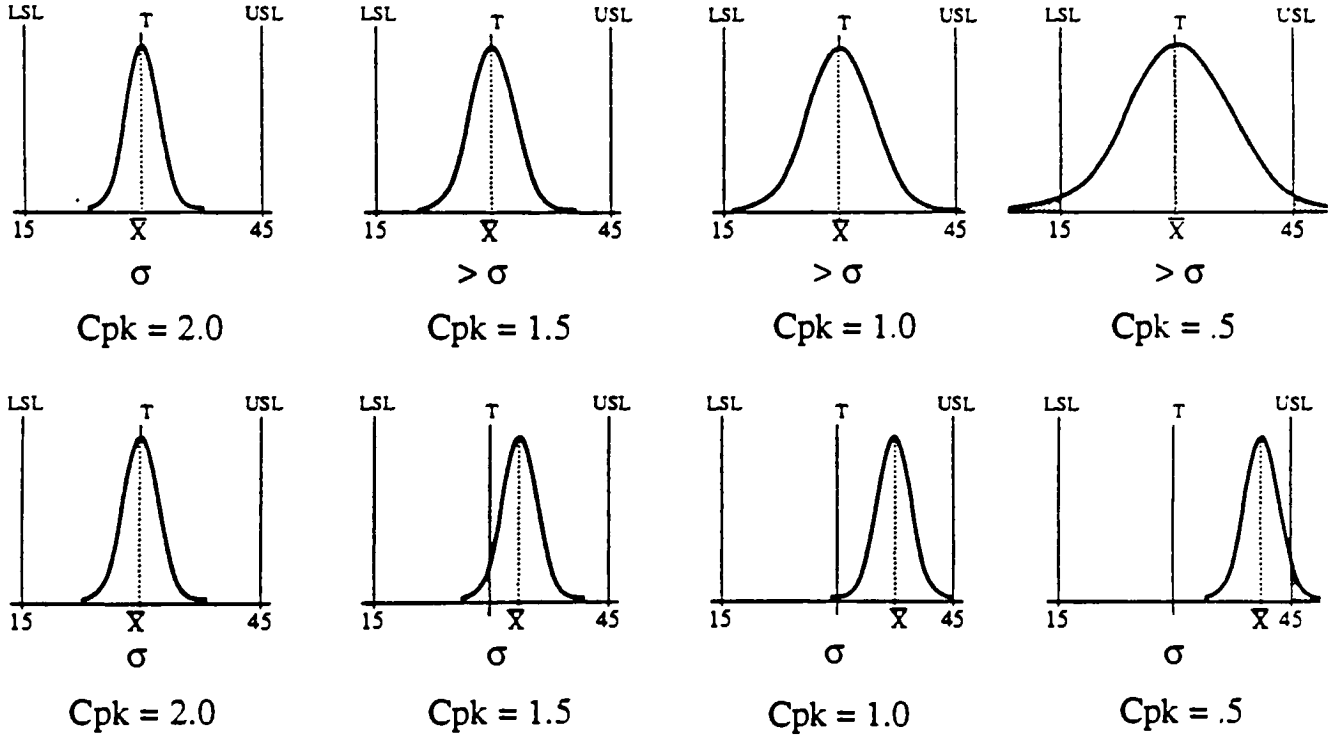
*(h)* Machine/Process Capability ($C_{pk}$): The $C_{pk}$ is a machine/process capability index that measures the ability of a machine or process

to produce product within specification. The $C_{pk}$ is the ratio of the distance between the actual process average and the closest spec. limit over three times the standard deviation of the actual process. The $C_{pk}$ measures the degree of centering of the actual process spread with respect to the allowable spread. Mathematically, and graphically, this concept is shown in Figure 16 below.

## Figure 16 - Machine/Process Capability

**Short Term Study:** $Cpk = \{ \text{Smallest of: } \frac{USL - \bar{X}}{4 \times S} ; \frac{\bar{X} - LSL}{4 \times S} \}$

**Long Term Study:** $Cpk = \{ \text{Smallest of: } \frac{USL - \bar{X}}{3 \times S} ; \frac{\bar{X} - LSL}{3 \times S} \}$




*(i)* Short & Long Term Capability Studies: A short term study is an instant (short time frame) evaluation of a particular characteristic

in a machine or process. This type of study should take a few hours or days at the most, depending on the production rate of the machine or process. A long term study is a prolonged evaluation of a particular characteristic in a machine or process. This type of study should take between 30 and 60 days, where data are taken from the machine or process under study. The intention of a long term study is to account for time-related effects on variability, and to confirm that the machine/process is producing product within specifications. There are recommended sample sizes for each of these types of studies. They are shown in Table 5 below.

Table 6

Recommended Sample Sizes for Short/Long Term Capability Studies

| SAMPLE SIZE | Short Term | | | Long Term | | |
|---|---|---|---|---|---|---|
| Study Number | 1st | 2nd | 3rd | 1st | 2nd | 3rd |
| Normal Distribution | 50 | 30 | 30 | 300 | 250 | 250 |
| Non-Normal Distribution | > 50 | > 30 | > 30 | | | |
| Binomial Distribution | 10K | 10K | 10K | 250* | 250* | 250* |
| Factor | 4 | | | 3 | | |

* 250 random units without a single failure

The sample standard deviation tends to be an underestimation of the parameter (population) standard deviation. It is evident that when small sample sizes are used to predict the population $\sigma$ that this underestimation would be even greater. To compensate for this misprediction a correction should be used (that gives the equations for $C_p$ and $C_{pk}$ found above) as follows:

$$\sigma = 1.33 \cdot s$$

Now that all this concepts, tools and techniques have been briefly discussed, it is necessary to point out the general procedure used to determine capability in a machine or process to use in step 5 of the method being described in this chapter. The procedure is as follows:

1.- Plan the machine/process capability study.
2.- Set up the machine/sub-process to known optimum conditions, and record the levels of the independent variables for that sub-process.
3.- Run the product through the machine/sub-process.
4.- Observe the processing of product and take notes.
5.- Measure and record the response variables (our independent variables).
6.- Determine normality.
7.- Compute Descriptive statistics (as in step 4).
8.- Determine state of statistical control.
9,- Determine the capability indexes.
10.- Reduce variability if not capable.

#### *4.2.1.4 Problems and Solutions Associated with Academic Manufacturing Environments*

In academic environments there are certain problems that are not found in industry. These problems cause the analysis of the results and capability to become difficult and sometimes new statistical techniques and tests must be considered to be able to justify the conclusions made. Among these problems there are three that are most noticeable:

1.- Difficulty for obtaining data: this means that data comes at a great cost and longer time spans than in industry. This tends to reduce the sample sizes significantly and thus any normal distribution statistics become non-applicable. Small sample techniques with Student

distributions and Nonparametric statistics become the only choices available. Unfortunately, there needs to be a more involved learning process for these two types of statistical tools since they require some extensive amount of knowledge of the discipline of statistics.

2.- Student operators: this problem creates a myriad of situations that would definitely only be found rarely in a mass-production industrial environment. Most of the facilities used in academic environments are used as class laboratories predominantly and production tends to vary in specifications and designs that are run simultaneously. Moreover, students are learning about the equipment and the field of microelectronics while using the facilities. This mere fact increases the probability of lack of precision and larger spreads as well as inaccurate results for any variable and measurement of interest. The only possible way to fight this is by close monitoring of the activities in the facility by experts as well as safeguards protecting the input of erroneous data into the database systems used.

3.- Equipment age: most of the equipment in academic facilities is usually donated by industrial partners of the school. Hence, the age of the equipment is such that there may be recurring problems which causes down time. Moreover, technical assistance is provided mostly by in-house staff that needs to be trained in the operation of each of the pieces of equipment. The only way to make this problem completely disappear is obvious, but does not come cheap at all unfortunately.

With these circumstances in mind, the best has to be made out of the challenges posed by academic environments, which, after all are the cribs of engineers which will eventually work in the microelectronic

industries of the future. Therefore, a unique opportunity is available for learning to deal with difficult situations in a smaller scale and prepare for the situations encountered in larger scales in industry.

A serious warning is to be placed at this point as worded by a statistical process control expert in industry, who I am grateful to for his time and help. This is shown in Table 7 below.

Table 7

E-Mail Warnings From Quality Control Expert

From: IN%"RGORDON@INTEL9.intel.com"
To: IN%"JIG7975@ritvax.isc.rit.edu"
Subj: RE: Statistical Process Analysis...

Ignacio,

My apologies for a slow reply to your EMail. I will try to communicate to you a few lessons from analysis of wafer fabrication data that maybe of benefit to you.

1.- There is a need to consider what the basic sampling unit is. In a production fab, sampling plans are often hierarchical or nested (sites within wafers within loads for example). To just consider the site level data to be a homogeneous population is misleading. Thus I typically apply elementary statistical methods to load/batch/lot level statistics. To analyze data from nested sampling plans, technically one should do a mixed GLM analysis. The approximation we usually do is to a nested ANOVA and plot the data in strategic ways to understand systematic effects in the data. Much of what we do can be found in an article by Ron Snee in the JOURNAL OF QUALITY TECHNOLOGY with the words "Process Capability Studies" or something like that in the title.

2.- You used oxide growth data as an example where mean +/- 3 sigma gives misleading information. For our data, where we lack normality or have outliers we often use the pseudospread to estimate standard deviation (the pseudospread is the Interquartile Range (P75-P25) divided by 1.349). If you were using the data to compute control limits and the minimum possible value is 0, I can make a case for either of the following:

LSL = max(0,mean-3*stddev) **OR**
LSL = max(0,median-3*pseudospread)
&
USL = mean+3*stddev **OR**
USL = median+3*pseudospread

For semiconductor processing, basing control limits on within subgroup variability is often misleading.

3.- The comparison of different parameters is a problem for which there is not a satisfactory solution for semiconductor processing. The standard approach is to

use capability indices such as Cp and Cpk as unitless measures for comparing different parameters. Since the distribution of a capability index for a single operation is a function of the specification, the sampling plan, and the intrinsic capability of the process step, comparing parameters with their capability indices is often misleading.

I hope this addresses items you were raising in your E-Mail. If this does not help, we may be able to progress more quickly with a phone discussion ((505) 893-1221). Regards, Rob

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Completing this step of the methodology will allow for increased simplicity in the rest of the investigation. Let us now turn to applying these concepts, techniques and tools to the nMOS inverter.

### 4.2.2 Application to the nMOS Inverter System

This step of the method is crucial in nature for it will guide the investigator towards careful consideration of those parameters which have the highest potentially to cause faulty products to be made. This step is very complex in nature, as was seen above. It involves the overview of all the metrology of the plant and the correct management of the data which the plant produces.

In the case of the RIT Fab, for this particular system, since the number of variables is quite small already, all of them will undergo considerations of capability. Nevertheless, techniques dealing with metrology characterization and gauge capability will be not be dealt with. The reason for this is that there is not enough experience with the systems at the Fab to be able to assess such issues, even though there is an apparent need for it. It is assumed that there are correct, and reliable and repeatable ways to obtain the necessary data and that the data is consistent in the lots of wafers that progress through the plant to create

products.

It is also assumed that the data obtained matches each of the parts of the system (in this case the nMOS inverter) and characterizes all of them thoroughly. For example, in the case of sheet resistance, values for diffusion regions are needed for both the enhancement and depletion transistors. Each of them will have a different range of values and will need to be modeled with those values accordingly. Unfortunately, at the RIT facility there is no such separation of measurements. There might be a reason behind this, thus it will be assumed that the sheet resistance is the same for both devices (from the reasoning above). Future endeavors should strive to correct this.

With regard to the capability of the parameters, a previous study was made which dealt with determining these facts (as mentioned in section 4.1.1). In it, all the current values for which there was sufficient meaningful data were studied and their capability, as linked to the machines and processing steps which they characterized, was assessed. Nevertheless, not all the work was completed due to lack of specification limits in most instructions.

On the other hand, for the case of the variables which are to be used in the application to the nMOS inverter, the specification limits were extrapolated from the data and from knowledge of the process through simulation using SUPREM-3, and double-checked with an expert. SUPREM-3 is a software tools which is used to characterize the effects of processing (both physical and electrical) on a slab of

semiconductor material when designing processes. This knowledge was acquired while taking a course in Manufacturing Science during Fall 1992, Winter 1992-93 and Spring 1993. Thus, as can be seen from the first six pages of Appendix E, frequency distributions, measures of central tendency, measures of spread, measures of shape, machine/process potential ($C_p$) and machine/process capability ($C_{pk}$) are determined in a short term study manner, i.e. with approximately 50 or more data points. Nevertheless, this is actually a long term study spanning years of data collecting. This is the reason why the capability indexes did not change their formula to that which is used for short term studies.

It was found that there is very little capability in all of these measurements and the operations that produce them. Indeed, the capability index Cpk is as low as 0.03 and does not surpass 0.20. Also, there is a lack of centering on the data, which shows that there is quite a lot of inaccuracy within the Fab. Some corrective measures should be taken and some ideas are discussed in chapter 8. Moreover, there is some lack of normality on the distributions of the data. This goes along to show that the warning given in table 7 is true and should be considered in future endeavors. In the case of this study, there is no knowledge of the theory behind the facts shown on table 7 no previous investigation of the actual modeling that should be applied to academic environments with respect to such precautions. Therefore, there was no point in using the equations and data shown in the table. That is, there needs to be a research effort that investigates the industrial standards for capability determination and from there extrapolate methods which

could be applicable to academic environments. Nevertheless, more details regarding the variables of interest are shown in Appendix E, as mentioned in the previous paragraphs.

# 5

# DESIGN CONSIDERATIONS

## 5.1 VLSI Design Evaluation

### 5.1.1 Concepts

In this step the VLSI design is put under scrutiny to understand the underlying concepts behind it, its functionality, its timing considerations (as designed) and its expected performance. There is an assumption that needs to be made: the design should already be readily available since the purpose of this method is not to investigate the design considerations per se, but to understand the design-manufacturing interactions and effects in order to predict real performances and characteristics.

Therefore, it is not a concern of this step to explain the theory behind design of integrated circuits. The justification behind this is that anyone using this methodology should already be familiar with the intricate details of matters such as VLSI design, fabrication, etc. The only concerns and objectives of this step are to thoroughly understand the functionality and architectural considerations of the system being dealt with. Topics such as gate-level (logic) design, expected results, circuit-level (transistor) design, timing simulations, verifications, layout of both subsystems and the overall system, design rule checking (DRC), electrical rule checking (ERC) and layout versus schematic (LVS) checks

should also be studied and understood. This will enable the investigator to get a feel for the designer's point of view as well as not be surprised by results obtained in the end of the research effort following this methodology.

One final point should be made, if a design is not readily available, and there is need for designing a VLSI system, careful considerations should be taken and there should be some level of expertise by the investigator. The necessary time to design the system should be allocated, for this effort alone could take several days, weeks or even months depending on the complexity of the system. Nevertheless, for the purposes of this method, the design effort should be minimal and the understanding of the design should be emphasized to the maximum extent possible.

### 5.1.2 Application to the nMOS Inverter System

The inverter has been theoretically considered in detail in chapter 2. Nevertheless, the actual design that is being produced at the RIT Fab has not been mentioned. It is the objective of this section to introduce the reader to the design considerations that were made by the designer of the system.

The inverter being considered here is part of a cell of a larger test chip designed by H. J. Bijker for the microelectronic engineering department in 1991. This system consists of test structures that are able to ascertain the correctness of a process which was being used in 1991 and is still being used now. The system consists of 64 cells, of which

cells 38 to 45 are inverters and cell 53 a ring oscillator.

Cells 38 through 45 differ both in feature sizes and thus in gain factors. The basic design being considered is shown on figure 17 (next page).

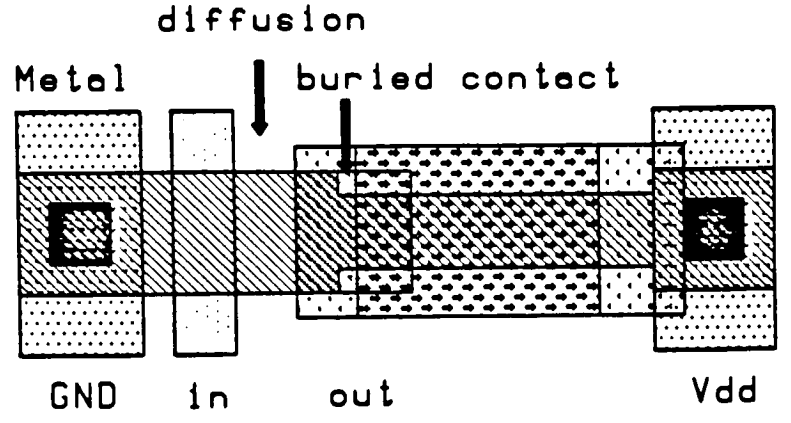
As far as timing simulations are concerned, the work done by H. J. Bijker does poorly in showing specific factors such as timing, inversion, voltage, and others characterizing the inverter at the design level. On the other hand, a good description of test results from an actual fabrication run are provided. Moreover, an analytical method for obtaining the figure of merit, i.e. $t_d$ is provided along with other useful information (such as inverter layouts) which helps understanding the basic design. All the information for the nMOS test chip is available at the department of Microelectronic Engineering at R.I.T. or by directly contacting H. J. Bijker.

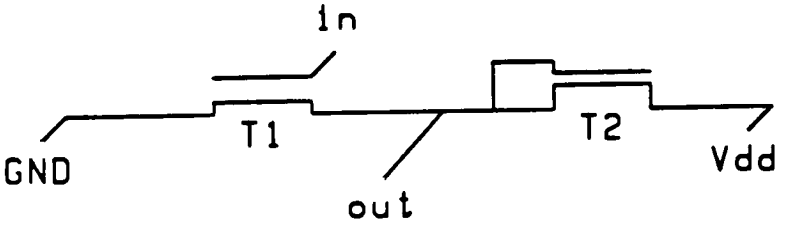
## 5.2 Layout Parameter Extraction (LPE)

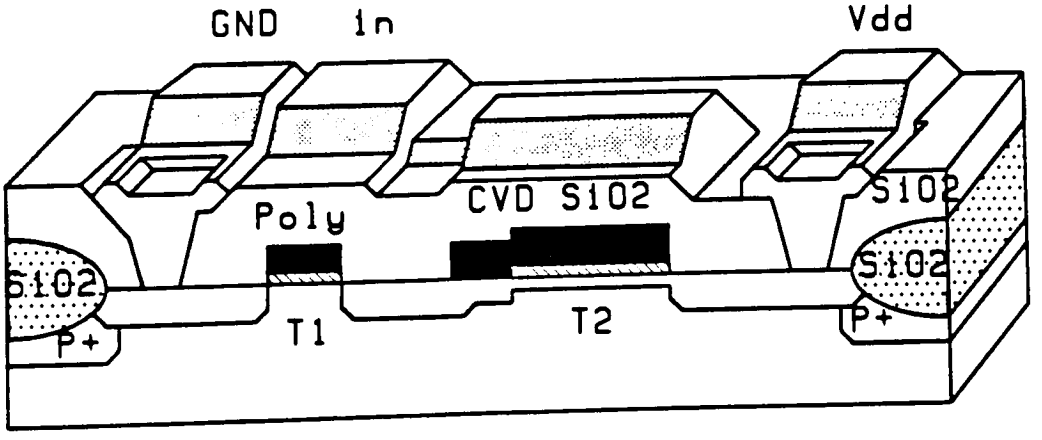
In this step of the method, it is necessary for one to have computer tools that verify the electrical and physical integrity of the IC design. This toolset can be used to insure that the layout is manufacturable, functional and adheres to the electrical performance which can be defined using a schematic design or netlist. The objective here is to obtain a SPICE readable netlist with predetermined values (obtained by extraction from manufacturing data and input into a system script) for

# Figure 17 - E/D Inverter as Depicted by H. J. Bijker

The top figure shows the final topography of an nMOS inverter. The middle figure shows the schematic representation of the nMOS inverter. The lower figure shows a cross-sectional view.



each of the parameters of interest. Nevertheless, the question of actual performance versus simulated performance is still unanswered. Further steps beyond this one are necessary to tackle such a problem and try to resolve it in an efficient manner.

There are many tools to accomplish the objective of this step. Of particular interest is the Mentor Graphics verification toolset (it is one of the several available and used at R. I. T.). This does not imply that there may not be other tools available with more features or powerful handling of layouts. Nevertheless, due to licensing laws and copyrights, these other toolsets are only available for use within specific design environments.

Any way, a brief discussion of the Mentor Graphics toolset shall be given. It is expected that the reader will be familiar with the use of the toolset available for the purposes of this step. It is also assumed that there will be a set of scripts pre-written for use by designers for these purposes and able to handle the specific characteristics of the system being studied. The reason for this is that it is not necessarily the task of any particular designer to set up the system in which these (or any other) CAD/CAM tools are to be used. If this were the case, the design effort would become more costly and time consuming than is needed for the purposes of the methodology being considered in this thesis. For more information on the Mentor Graphics verification tools, please refer to bibliography at the end of this document.

### 5.2.1 Concepts

The Mentor Graphics® IC checking toolset (CheckMate™) consists of two major tools: MaskCheck and Netcheck. A third toolset, the CheckMate Utilities, work on the data created by the two major tools. MaskCheck is the physical layout verification checker. MaskCheck verifies that the IC layout has the proper interlayer and intralayer relationships for the fabrication process. NetCheck verifies that the IC layout design conforms to the schematic design or netlist. The Utilities are additional tools that manipulate information from both the other tools and include: OutNetL and OutNetS which create LSIM or SPICE netlists from the database information of the other two tools; TransNetL and TransNetS to translate external LSIM or SPICE netlists into database information usable by the other two tools; etc.

With MaskCheck one can: define layers, extract new layers, output layers, specify circuit connectivity, detect shorts and opens, detect design rule violations, extract netlists extract devices, extract parasitic devices, calculate device parameters, perform nodal summations, etc. MaskCheck performs verifications and extraction operations according to instructions placed in the control and rules files (scripts). The entries made in the MaskCheck control and rules files determine the input accepted and the output delivered. Release 2.2 has new capabilities to extract and report parasitic capacitances and resistances that occur in the layout. These parasitics affect the timing performance of the circuit. Finding these parasitic values, and attaching them to the netlist generated for simulation, allows for a more accurate circuit performance simulation. CheckMate MaskPE™ is a separately licensed software.

NetCheck identifies differences between two circuit netlist descriptions (usually, one from a layout and one from a schematic) and reports the differences. It needs three input files: an extracted netlist from the layout; a reference netlist from the schematic and a control file. NetCheck outputs signal and device matching errors and allows for interactive querying of output.[18]

Careful completion of this step will allow for a check of the SPICE netlist to be easier. Usually, if the design is readily available, this LPE should also be available (as explained in step 6). Nevertheless, it can be done very easily having the necessary scripts available in the CAD/CAM design system.

### 5.2.2 Application to the nMOS Inverter System

In this step, the design of H. J. Bijker was to be checked to obtain a SPICE (or HSPICE in this case) readable netlist. Nevertheless, after careful considerations of the toolset available at R.I.T. and consultations with experts, it was determined that the system cannot perform layout parameter extraction on nMOS designs, because no Pdf files were written for the purposes of nMOS design verification. It is only useful for CMOS designs and does not provide for ways of checking depletion mode inverters. Moreover, the toolset is not set up to extract parasitic resistances and capacitances that could be obtained in theory by it. This happens because of the need of another software tool (MaskPE™) which is licensed by Texas Instruments Corporation, and it is not available in the R.I.T. design environment.

These facts reduce LPE to a manual task that can only accomplish limited extraction of parameters, such as obtaining geometric data for the generation of an HSPICE netlist. This netlist is to be generated in manual form as well, because of the inadequacy of the toolset with respect to nMOS designs. Thus, the geometric data will be manually obtained from the design reviewed in section 5.1.

From the review of designed cells available in such a chip for the E/D inverter, a $\lambda$=2 $\mu$m cell with a gain=2 was chosen (see Appendix F). The reason for choosing such an inverter is that in pre-manufacturing simulation it gives the best overall output. This being the only way to know whether this system works, and without manufacturing data to confirm any other notions, it was an obvious choice. The geometric data that is associated with the design choice within cell 38 or 39 of the test chip by H. J. Bijker is shown in Table 8 below. All other considerations being minor at this point, for it is very hard to obtain the necessary parasitics from the designed layout, we now turn to the problem of designing a thorough statistical experiment for this study.

Table 8
Geometric Values for E/D Inverter Chosen

| | **Parameter** | **Value** | **Units** |
|---|---|---|---|
| *Ratio (Gain$^2$):* | *k* | *4* | *N/A* |
| **Enhancement:** | M | 1 | N/A |
| | L | 8 | $\mu$m |
| | W | 8 | $\mu$m |
| | AD | 16 | $\mu$m$^2$ |
| | AS | 64 | $\mu$m$^2$ |
| | PD | 20 | $\mu$m |
| | PS | 32 | $\mu$m |
| | NRD | 4 | squares |

table 8 (continued)

| | Parameter | Value | Units |
|---|---|---|---|
| | NRS | 16 | squares |
| **Depletion:** | M | 1 | N/A |
| | L | 32 | $\mu$m |
| | W | 8 | $\mu$m |
| | AD | 64 | $\mu m^2$ |
| | AS | 16 | $\mu m^2$ |
| | PD | 32 | $\mu$m |
| | PS | 20 | $\mu$m |
| | NRD | 16 | squares |
| | NRS | 4 | squares |

# 6

# STATISTICAL EXPERIMENTATION

## 6.1 Design of Experiment(s) (DofE)

The joint objectives of this step are two. First, to maintain focus on the important factors of the research being done on the VLSI system by designing an experiment before any conclusive results are obtained. Second, to set out the hypotheses needed to obtain the desired results and be able to test them and analyze them by statistical methods. One of the most important reasons behind designing an experiment is that of avoiding combinatronic explosion of data. That is, as more independent variables are used and for each variable the number of values to be studied is large, the number of data to accumulate and analyze increases factorially by the equation:

$C(n,r) = n!/[r!\cdot(n-r)!]$ such that
n = number of factors
r = distinct objects chosen at a time

For example, for 7 independent variables, taken 2 at a time (varied two at a time), the total number of data values to be obtained is 21. This means that there would be 21 sets of 7 variations. For a more complete study (full-factorial), which would express every single interaction between the variables one would need a $k^n$ design, such that k is the number of different values taken by each variable. Clearly, this

is not practical as the number of variables increases. One should strive to reduce the set of variables to the minimum required to understand the effects of interest and reduce the number of data to such needed to describe the major interactions between them. A brief discussion of this topic will be presented below in order to define some basic concepts needed with regard to this particular method.

### 6.1.1 Background Information

*6.1.1.1 Introduction to DofE*

The prime application area of DofE is that of process characterization. In this very general use, one studies the result of making purposeful changes in the way the process is operated and watch the way the responses of the process change. This is one of the goals of the method developed in this thesis. Another application utilizes experimental design to troubleshoot a problem by interchanging components. In this way one can induce a failure at will and understand the source of this failure. Routine analytical errors may be accessed by proper experimental designs. Instead of just watching the variation in the data by a so called "random process," one can trace the sources of changes in the numbers so that control may be gained on the overall variance and improve the quality of the product, process or service.

Purposeful changes are the important part of experimental design. Efficiency is the added value provided by a statistical approach to experimentation. An efficient experiment is that which derives the required information at the least expenditure of resources.

Now, there are ways to attain this efficiency. For instance, instead of using the well-known technique of changing one factor while keeping all the others constant to find out the effects of that one variable versus the others, one should look to find out all the possible combinations of importance to the process, i.e., all the interactions between variables per se, and, between variable(s) and the process. For this matter, one needs, as mentioned earlier, prior knowledge and experience with the process, a response or set of response variables and clear goals and objectives. Moreover, the response(s) should be quantitative, precise and must mean something related to the investigation. There are several ways to find the desired results in an experimental manner, but some are more efficient than others, as seen below. One has to be able to assess which method of experimentation, from those presented below or others, is the most efficient for the investigation.

*6.1.1.2 Statistical Experimental Designs*

As mentioned before, we have the so called 1-F.A.T. (one factor at a time) technique, where analysis is performed on each result independently of the other results. This is highly inefficient and may not even obtain the required information. There are others.

The two level factorial design looks at k factors in n observations, with each factor at two levels (two values only). In this study observations are not analyzed separately, but as an experimental unit to provide independent assessments of the effects of each of the factors under study. The number of observations in such an experiment is given by taking the number of levels to the power of the number of factors.[19]

The use of this design stems in the exploratory nature of a process or problem. Whenever there is an initial need to investigate effects caused by certain circumstances that can be experimentally controlled, and there is no previous data, this should be chosen. The reason is that this design will investigate the effects of the limits of the data. Nonetheless, this is seldom useful in engineering applications, where Targets, LSLs and USLs are always (or most always) needed.

In the fractional factorial at two levels design, one looks only for the main interactions of variables on the response variable. That is, in this type we will have a number of observations equal to the number of levels raised to the quantity of number of factors minus the fractionalizing element of the design. The problem with this type of design is that there are several complications that arise as a result from fractionalizing the experiment.

Multi-level designs are another type of experimental designs. These designs assume more levels (more possible values) for the number of factors taken out of the observations. The most common is the 3-level design in which any variable can take on three possible values and all the possible combinations can be analyzed. There are others such as the five-level design, etc. One must be careful with these types of designs since the combinatorial explosion that could arise out of an overseen situation could render the design too expensive and too inefficient to be affordable.

There are many variations within each type of design discussed

above. Nevertheless, the subject of DofE is too broad and thus cannot be thoroughly covered in this subsections of this eighth step. For more information, please refer to the bibliography section for any books dealing with the subject in a more complete manner.

#### *6.1.1.3 Hypotheses Determination*

Hypotheses are important, because they give direction to the study and the tests that are to be run in analyzing the results from the gathering of data. Hypotheses are very important and should be considered very carefully. They should be mathematically precise and logically correct, since these two requirements are very important for any statistics to be performed on them. Moreover, hypotheses should be made for the default and alternative considerations for each response variable of interest and should be plentiful enough to cover the range of responses obtained from experimentation.

Having the above concepts in mind, let us turn to the application of one of them to the characterization of the nMOS Inverter System.

### 6.1.2 Application to the nMOS Inverter System

Due to the characteristics of the data that is to be used as independent variables in this performance analysis, two-level designs are useless. The reason for this is that there are at least three levels of interest for each of the factors in the nMOS system (Target, -3$\sigma$ and +3$\sigma$). On the other hand, three level designs are inherently inefficient due to the volume of information generated at a relatively high cost. There are some modifications of the basic three-level designs that can be

efficient by giving the required information at a low cost. One of such solutions is that of the Central Composite Design (CCD) of 5 levels, or even a modified version of it. Another such solution, which by the way is the most appealing, is that of the "Box-Behnken" (B-B) three-level designs. This class of designs investigates three-levels with a minimum of work required to obtain meaningful results for analysis. This concept makes logical use of the $2^k$ factorial. To build a B-B design, factors are taken and $2^2$ factorials are built for all pairs of them while holding the other factors at a center point. There is a greater expenditure of resources in a B-B design than in a CCD. Nevertheless, the design of a CCD is very complex and requires much work, the same situation being for its analysis. Hence, the B-B design is a tremendous increase in efficiency from the full three-level factorial design that is affordable in this research.

To determine how many "sets" or sub-designs in a B-B are needed, one has to find the number of pairs of factors for the problem at hand. This is the combination of k factors taken 2 at a time, as shown below.

$$C_2{}^k = k!/[(k-2)!\ 2!] = (k(k-1))/2$$

such that k = # of factors

Therefore the number of treatment combinations (#tc) in a B-B design will be equal to the number of pairings of factors times the number of treatments in the sub-design (which will always be 4) plus the zero or center point.

$$\#tc = 4\cdot[(k(k-1))/2] + 1$$

As in any experimental design, the treatment combinations are randomized and run in random order. So, while the B-B designs are not as efficient as the CCD, they fill a gap between the $2^{k-p}$ and the larger, multi-level full factorial design and certainly are far more efficient than the full $3^k$ factorials. From a degree of freedom analysis, one can see that the B-B designs use up fewer df and in turn give up information on higher order interactions that would not likely occur. One does not obtain information on quadratic interactions of subtle nature from a B-B design. However, one does obtain information on main linear and main quadratic effects along with the two factor linear interactions. This is important to consider when one is doing an exploratory analysis such as the one for this example with the inverter. Finally, as related to the inverter case study, the B-B design is shown on Table 9 below.

Table 9
B-B Design for Use in Simulation Framework

| tc | $t_{ox}$ | $x_j$ | $R_s$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | - | - | 0 |
| 2 | + | - | 0 |
| 3 | - | + | 0 |
| 4 | + | + | 0 |
| 5 | - | 0 | - |
| 6 | + | 0 | - |
| 7 | - | 0 | + |
| 8 | + | 0 | + |
| 9 | 0 | | - |
| 10 | 0 | + | - |
| 11 | 0 | - | + |
| 12 | 0 | + | + |

*k = 3  #sets = 3  #tc = 13  - = -2σ-value  + = +2σ-value  0 = μ-value*
*Values of only ±2σ were chosen due to the low capability shown throughout the measurements of the independent variables (factors) being used in this study.*

Notice that this design improves over the full factorial by eliminating 14 cases, that are unlikely to be of significance any way.

As far as hypotheses are concerned, at this point there is only one (or a modified version of it). This study is concerned with proving there is no statistically significant differences between design-simulated performance, $\mu_1$; post-manufacturing performance, $\mu_2$; and manufacturing/design-feedback-simulated performance, $\mu_3$ (i.e., that which takes into account the inherent characteristics of the manufacturing environment). Expressed mathematically, this is as follows:

$H_0$: $\mu_1 = \mu_2 = \mu_3$
$H_A$: The $\mu$'s are not equal
$\alpha = 0.05$ (conservative alpha risk)

Unfortunately, there is no such manufacturing data for the metrics chosen earlier in the database of the RIT Fab. This reduces the analysis to a test of means between $\mu_1$ and $\mu_3$. Matters are complicated even further by the fact that simulation results from 1991 are not averaged or have a standard deviation (two conditions which are necessary for the test of means). Nevertheless, this subject will be dealt with in the analysis section of this methodology for the nMOS inverter case.

## 6.2 SPICE Calculations and Simulation Runs

After all considerations have been made for each and every one of the variables and an efficient experiment has been design, data must be

gathered. All the previous steps of this method have lead to the most important causes. Furthermore, they have lead to the most influencing sources of variation for the responses of interest. It is now time to obtain some realistic simulations in order to be able to compare them with the actual product further on. For this matter there are three points to be taken into account.

### 6.2.1 Associated Tasks

*(a)* Calculation of lower and upper specification limits (LSLs and USLs) for each of the factors ($x_j$, $t_{ox}$ and $R_s$) of the experiment as well as their target value. Maybe there is the need to calculate other values (depending on the design of the experiment) or maybe there is only a need for the LSLs and USLs.

*(b)* Double-check of the netlist generated by LPE step of this method. That is, check that the SPICE net list created as a result of doing the Layout Parameter Extraction agrees with the values set out for models, elements, interconnects, parasitics, etc. This is important, because most of the predefined scripts have certain values associated with each of the parameters for the model and element. One has to be able to ascertain that each and everyone of them agrees with those from the capability analysis step, design step (those specified by the system designer(s)) and those of substep (a) above. Any discrepancies should be thoroughly checked and the source of this error should be determined and cleared before continuing with the study. This could otherwise lead to erroneous results, and therefore, erroneous conclusions as well.

*(c)* SPICE vs. HSPICE use: SPICE is a public software available to

most academic and industrial environments upon request and certain other considerations. HSPICE is a commercially available system (as explained in Chapter 2) with many enhancements over the public version. It offers more capabilities, both analytically and graphically over those of SPICE. Nevertheless, there is a cost associated with the use of HSPICE; that is, there is a monetary price involved and there is a learning curve over SPICE that needs to be covered before efficient use of the tool is possible. One should address the needs of the environment where the study is being executed and select whichever option is more attractive.

*(d)* SPICE-deck runs and result retrieval: once all of the above issues have been addressed properly, one can turn to the task of running the necessary amount of combinations (as set out in step 8) in SPICE (or HSPICE) in order to obtain the set of values for each of the response variables defined earlier in this method.

### 6.2.2 Application to the nMOS Inverter System

At this point, once the B-B design has been laid out, one needs to obtain results from SPICE simulations reflecting such parametric variations. If LPE had been available, a netlist containing all the necessary parameters would be available and there would only be a need for checking it to make sure all the values were correct. Furthermore, only minor changes would have to be made in order to incorporate the variations induced through the experimental design of section 6.1 in order to accommodate for the ranges of values of the three variables that were defined as fundamentally essential to performance and for which an

entire capability analysis was made.

Unfortunately, LPE was not available and thus a netlist must be generated manually. This, in turn, represents a fail-safe procedure in which checking of the values for each of the constants and variables of the model files. Also, this provides for an assurance in which values that were determined to be negligible, are, in fact, neglected.

A point should be made with regard to the variables chosen in this study. Junction depths and sheet resistance values should be done for each transistor of the inverter individually and recorded accordingly. This is not the case in the RIT Fab, for only one junction depth measurement and only one sheet resistance measurement are made for all diffusion purposes of the drain/source region's definition implant (or diffusion). This is correct in principle, but does not take into consideration the electrical characteristics that are affected by previous implants both for threshold adjusts, as well as depletion implant region purposes. Thus, there are variations in values that are going to be found in the two devices' regions and these have effects in the model files made for each of them. For the purposes of this study, the values of each of the two variables will be assumed to be the same for both transistors, even though this might not really be the case.

Also, considering the choice between SPICE and HSPICE, the following must be read. One of the steps of this method had the objective of reducing the number of parameters which are available for modeling. HSPICE, on the other hand, increases the number of

modeling parameters from about 48 to over one hundred. This, at simple sight, is a terrible shortcoming of HSPICE. A more in-depth analysis of the software tool will reveal that most of those parameters are used in calculations that are not available in SPICE. For example, the parameter ACM, and another set of them which follow in table 1 (pg.15), could be viewed as useless. Nevertheless, they are fundamental in the sense that any specification of them will allow for the model to be manipulated to obtain effective areas of devices and regions of each device, which will prove useful in calculating, among others, the actual gain of the system. There are other instances, and they are to be considered carefully. This was done in an arbitrary manner and is shown in Appendix B. By arbitrary it is implied that the user's manual for this tool was studied and the values that would prove most useful in this simple example (nMOS Inverter) were set constant. Also, other values were chosen according to MOSIS models, for it is a possible fact that the designer used these models for his simulations in 1991. Moreover, these MOSIS models provide for some typical values that could not be obtained from the R.I.T. facility and are presently missing in the database.

Therefore, after calculating the $\mu \pm 2\sigma$ values, as well as obtaining the mean value from Appendix E for each of the independent variables, the results are as shown on table 10 (next page).

Having these values calculated, and the rest of those being considered held constant or simply neglected, simulation is performed in HSPICE H9000D for the 13 cases of the B-B design. The results are shown in Appendix F along with a representative HSPICE netlist. Once

Table 10

Values for the Three-levels of the Three-factors Being Considered

| | $t_{ox}$ | $x_j$ | $R_{sh}$ |
|---|---|---|---|
| $\mu - 2\sigma$ value: | 374.3 Å | 0.47 $\mu$m | 0 Ω* |
| $\mu$ value (Mean): | 828.2 Å | 1.89 $\mu$m | 23.31 Ω |
| $\mu + 2\sigma$ value: | 1282.1 Å | 3.31 $\mu$m | 79.01 Ω |

* = value actually goes negative [not possible]

all these results are obtained for the inverter, we turn to the analysis of the results obtained. Another point should be made, regarding the simulations for $t_d$, that is, with respect to the Ring Oscillator simulation needed to produce the results concerning time delay metrics for each of the cases of the designed experiment. The netlist representing such circuit is shown in Appendix F, as well as the diagram from which visualization of the netlist was made.

As much work as was done for the simulation regarding this metric, no results were obtained. There are certain author-related shortcomings regarding the operation of HSPICE which did not allow for proper solutions to be investigated. Moreover, the time constraints put forth stopped this simulations short from producing the easy results which the ring oscillator produces and are otherwise hard to calculate manually. Nevertheless, with some effort the circuit and all the variations needed for it to give the results for time delay depending on $R_s$, $x_j$, and $t_{ox}$ can be obtained. This is, by no means, a weakness in the method. Rather, it is a weakness in the span of knowledge that the author holds regarding the details of HSPICE H9000D. It should, nevertheless, be possible to simulate this circuit by appropriate fixtures

to the netlist that will allow for transient analysis to run smoothly and the frequency to be extrapolated out of this analysis. With regard to the overall results of this case study, it should be noted that the fact that this particular simulations were not run does not constitute disaster. The reason is that there is already some essential data missing that will stop any analysis from being performed. Nevertheless, this is explained better in the section below.

## 6.3 Analysis of Result Set(s)

This is again a controversial step, meaning that there is much material to cover. This material can be found in Statistics and Design of Experiment books where it is explained in a very thorough manner. Nevertheless, depending on the desires of the research being done (in this case the nMOS inverter performance characterization), most analyses will fall in the following categories:

### 6.3.1 Basic Tools & Techniques

*(a)* Simple Analysis: That is, performing hypothesis testing. There are many types of hypothesis testing, but most important of all these that of means (large and small samples for both equality and differences and for both independent and paired data); tests for standard deviations (single and among two standard deviations). The problem with these types of tests is that they tend to increase the alpha risk (risk of hypothesizing erroneously) as the number of tests increases for several associated means and/or standard

deviations.

*(b)* ANOVA: that is, analysis of variance. This remedies the problem regarding the alpha risk and can simplify procedural difficulties quite a bit. The only problem with this analysis technique is that it assumes several things, one of them being the homogeneity of the variances of the means being tested, and the other being normality. Now, as seen from table 6, in VLSI and IC processing normality is an unusual feature. This creates problems that are difficult to solve and beyond the scope of this document to discuss.

*(c)* Nonparametric tests: these are all those methods that do not assume anything about the distributions of the sample(s) taken. They deal with the data as it is and deal with obtaining the information being asked for by unconventional techniques. There are a myriad of Nonparametric tests and techniques and thorough review and study of them will be the only way to discern which one is the most applicable.

*(d)* Regression Analysis: this type of analysis deals with the proportions, curve fitting and the extrapolation of equations that thoroughly describe the behavior of the response as a function of the data provided by the results of the interactions of independent variables. This is more a complement to the analysis performed by those categories shown above, rather than a sole analysis option.

Again, it is up to the investigator to choose such techniques which are to obtain the most meaning out of the results. It is difficult and rather cumbersome to believe that there are simple ways to analyze data for general cases. There is an immense amount of research undergoing

even presently to deal with the difficulties associated with analytical techniques to suit new and more complex problems. It is one of such problems that of IC processing. Thus, it is stressed that detailed study of the techniques, the motivations, the theory and implications behind any attractive analysis procedure, is necessary to achieve the most efficient and robust conclusions. This is a critical step of this thesis' methodology and it is not, by any means, to be taken lightly.

### 6.3.2 Application to the nMOS Inverter System

Before any analysis could be performed, the result set from this methodology's simulations is presented. Results for the metrics defined in step 1 are shown in Table 11 below.

Table 11
Methodology's Simulation Results

| tc | $V_{t_{pd}}$ | Gain | $V_{inv}$ | $t_d$ |
|---|---|---|---|---|
| 0 | 1.2440V | 2.3167 | 2.3395V | N/F* |
| 1 | 1.2923V | 2.3167 | 2.4793V | " " |
| 2 | 1.3553V | 2.3167 | 2.7862V | " " |
| 3 | 1.1851V | " " | 2.3445V | " " |
| 4 | 1.2482V | " " | 2.8224V | " " |
| 5 | 1.2125V | " " | 2.3253V | " " |
| 6 | 1.2755V | " " | 2.8268V | " " |
| 7 | 1.2125V | " " | 2.3253V | " " |
| 8 | 1.2755V | " " | 2.8268V | " " |
| 9 | 1.3238V | " " | 2.4806V | " " |
| 10 | 1.2167V | " " | 2.3502V | " " |
| 11 | 1.3238V | " " | 2.4806V | " " |
| 12 | **DISCARDED, because of impossibility of this situation** | | | |

* = value not found

A representative I-V curve is shown on graphical output (for treatment combination 0) in Appendix F.

Unfortunately, the R.I.T. nMOS 2.0 process does not stress testing of parameters at the end of the fabrication procedures as much as it should. Testing is the step where most of the measurements come to existence and can be validated to be used in modeling and understanding processing-design relationships (as in this thesis) or any number of other modeling efforts that can arise out of characterizations.

Because of the lack of measurements from step 51 of the nMOS process, no sampling can be done, no means or standard deviations of the measurements can be obtained, and thus, no real testing can be done. Also, the designer did a terrible job specifying operating curves and specification limits for any parameter. This mere fact completely blocks any effort intended toward analysis of the results for comparative purposes. On the other hand, just looking at the results from table 11 above, one can ascertain the following:

1.) The greatest effects on inversion and threshold voltages are those caused by $t_{ox}$ and $x_j$. This can be seen from any mathematical derivation of the relationships that exist between the metrics and the two parameters above.
2.) Sheet resistance will only have a significant effect if no influences from contact and diffusion resistances are considered. That is, of course, impossible.
3.) The gain will be constant throughout, unless lateral diffusion and length modulation effects are considered along the channel.
4.) The farthest reaching effects are given by $t_{ox}$. This is clear if

one looks at treatment combinations (t.c.) 1 through 4, and 5 through 8. In the first set, there will be large variations occurring on the voltages. This is because the effects of both junction depth and thin oxide thickness are being considered. On the other hand, in the second set, there is still some variation occurring depending on the values taken by think oxide thickness, and they are larger than those on the third set (9 through 12) where junction depth is the variable and thin oxide the constant.

5.) The combined effect of $x_j$ and $t_{ox}$ is the most influencing cause of variation. Only on large diffusions will sheet resistance become a factor of importance. This also applies to submicron minimum feature sizes (currently being used in industry).

6.) None of the time delays were obtained. This is due to reasons discussed earlier.

7.) The zeroth combination (all average values for parameters) will give a value not far from the desired inversion voltage (2.5 V). A better result will occur on tc#1, tc#9 and tc#10.

8.) There are certain voltages that repeat. This is because the effects of sheet resistance are negligible and they do not affect the values that re-appear on different t.c. for $x_j$ and $t_{ox}$.

9.) A fatal error occurs when junction depth is shallow and thin oxide thick, i.e., treatment combination 2 where inversion voltage shoots up to a high value. Also, when both are in their maximum values, or when thin oxide is larger than average (not target!!!), and junction depth is average the inversion voltage increases. See the inversion voltage curve range plotted in Appendix F (after the output for treatment combination 0).

10.) All I-V curves are similar and smooth in nature. The gain is smaller than the design value (Gain=2). This seems to compensate for the variations of the most influencing parameters by not allowing for large overshoots (or undershoots) to occur.

11.) There is a further need for investigation of variations of other parameters in conjunction with the three parameters investigated in this case study. This is not going to be a feasible experiment, unless there is availability of supercomputing systems and algorithms powerful enough to handle the computational load this will incur.

12.) Measurements are vital, as well as design specifications based on pre-manufacturing simulations.

Regression Analysis could not be done. The reason is that due to the lack of comparative analysis because of a lack of measured and specified data in this system (nMOS inverter) would result in formidably weak and unreliable results. This is left to be done in future efforts after data exists in at least one of the two populations mentioned above (manufacturing data and specification data). With this in mind, let us turn to the question of manufacturability, functionality and repercussions of the system in other areas revolving around it, in particular this one (nMOS inverter).

# 7

# MANUFACTURABILITY ASSESSMENT

## 7.1 Product Functionality, Manufacturability & Other Implications

At this point of the study (following the methodology being described), everything regarding the responses and their relationships to the independent variables should be known. That is, all the results should be available and a good idea of the predicted performance (based on real values) should be clear. The questions then are: so what? what do these results tell us? where do these result lead us? what can these results impact? These are rather involved matters and much thought must be put into them.

### 7.1.1 Concepts to Consider

One area that is definitely identifiable is that of comparison between what the method reports for predicted performance and what real manufacturing gives as a result. There is a need for comparing the two results to understand whether there is accuracy in the methodology and whether any statistically significant differences exist. Logic dictates there should not be any, but logic does not always take many factors into consideration. One should make a point of studying these differences (if existent) and reporting them accordingly. Moreover, these differences would give insight into any overseen details and provides for a feedback path in this methodology. In other words, it provides for its

continuing improvement and search for ultimate accuracy and precision with respect to reality.

Out of the above comparisons one should be able to assess functionality, i.e. the conformance of the predicted (and real) characteristics to the design of the system. It should be readily clear whether this occurs and whether there are any weaknesses in the product with respect to the specifications due to variances of important parameters and their effects on the relevant characteristics of the product.

Another clear fact should be that of manufacturability, or the inherent producibility of the system in the manufacturing process. It is rather difficult to change processes in the semiconductor industry. The reason for this is that it takes much longer to perfect and quantify a process that to characterize a product differently to accommodate for a process. One of the facts of this matter is that a process may be accommodating for many products and if changed it might have a farther reaching effect than if left as such (or only modified very slightly if absolutely necessary) and only modifying the products around its characteristics. There are many other details involved that defend the above notion. The point is that one should be able to assess the need for changes in the product or to pin point areas of conflict between the process and the product and recommend action(s) that could solve this conflicts.

There are more far reaching implications than the two explained

above. Product functionality and performance, as well as manufacturability are cornerstones of issues such as cost of ownership of products and processes, cycletime reduction efforts, etc. These implications are subject to consideration and should be addressed properly in order to quantify the effects of any product's variation in performance in any area that it may touch. This, or course, assumes knowledge of the industrial planning and financial issues that surround any process-product interaction. Moreover, some level of expertise is required due to their rather sensitive nature. With this in mind, as well as the concepts and areas that are to be considered, let us turn to the nMOS inverter's case for a brief explanation relating it to this last step of the methodology.

### 7.1.2 Application to the nMOS Inverter System

With respect to the comparison of results from the Fab, from simulation and from this method, the only comment to be made is that until there is such data to be compared, no testing of the hypothesis of step 8 can be made. That is, the hypothesis set in the design of experiments section for the nMOS inverter cannot be tested until there are enough values for each of the three population to make it a significant and insightful effort.

Nevertheless, from the results obtained following the method set forth in this thesis, one can tell that there is some level of functionality of the inverter. That is, as long as there are no extreme conditions surpassing the $\pm 2\sigma$ limits from the average, the product should give reasonable values for inversion voltage, threshold voltage, gain and

possibly time delay (though this needs to be confirmed in future endeavors). Still, a definite increase of capability indexing on most of the operations done inside the Fab is needed. This will allow for further improvement in precision and accuracy in the processing undergone there. More details regarding functionality and capability of this case study are given in the above corresponding sections that analyze these points.

Manufacturability is an important issue, and it should not be left unattended. According to the methodology undergone, the nMOS inverter is manufacturable in the R.I.T. Fab, but the variations in the process are too large to overlook. Performance is highly hindered by incorrect diffusion operations and insufficient gate oxide growth. There should be a safeguard against erroneous processing of these particular steps as well as others that might influence the performance of the circuit to any extent. Also, a need for metrology characterization and gauge capability is underlined. There is nothing more important than reducing variability in the equipment to be used, in order to determine the influence that student-operators have on the processing effort. This needs to be addressed properly.

A point should be made with respect to the design done for this product. There was no thorough simulation work done, and the fact that the product was allowed to go through the nMOS process may have a lasting effect in the capability of the Fab. This means that a faulty design could induce erroneous data to enter the CIM MESA system, thus confounding the effects of the process per se and those of the product by

itself. Moreover, a blurry overall effect that is highly inseparable would result, unless the design works prior to manufacturing in a simulation environment. Review of the design will reveal the statement which informs of the fact that the inverter does not work in simulation. This is a warning that should never occur and should be taken care of before the design enters the factory. Otherwise, the analysis work could be made as complicated as this case study has shown to be. Thus, thorough verification and data extraction should occur prior to manufacturing endeavors, in order to have a basis where to make comparisons later on.

There are more subtle subjects to talk about, such as that of the effect of the performance of the inverter into cycletime reduction planning, inventory controlling, cost of ownership of the process and product and others. Surely there are effects that are to be addressed in each and everyone of the subjects stated above. Nevertheless, the problems associated with the nMOS inverter per se and the lack of data that exists for it as a product is complex enough that the other topics have to be left for future efforts to address. This should only happen once certain comparative analysis is done and all the functionality of the product (system), is manufacturable.

# Section 3

## *Final Notes*

# 8

# SUMMARY, CONCLUSIONS & RECOMMENDATIONS

## 8.1 Summary

In the preceding section, a method for predicting real performance has been discussed in detail, assuming prior knowledge where necessary and expressing a more detailed explanation where needed. It has been noticed that the complex nature of the problem of properly assessing performance makes any solution equally complex in nature. A point has been made throughout this section (and all the research that goes behind it) to make the solution as simple, flexible and general as possible. The reason for this is that there needs to be room left for the researcher using this methodology to use his or her own judgment about the relative importance of each of the steps outlined here.

Moreover, this method has the inherent assumption that none of the steps are rigid in form, but rather each should be viewed as a possible approach towards the overall solution, which presents a set of tools and techniques currently available to aid the investigator in the efforts of the study. By no means this represents that the tools, techniques and procedures presented here are exhaustive. There may be other, more powerful, sets of tools that could tackle the problems being addressed here in a more efficient manner. Nevertheless, the tools

presented here are geared towards determining direction of the investigation and are simple enough to understand (having had some prior exposure to all the theory behind them).

Some of the steps involved a more detailed discussion due to their sublime nature (to put it somehow). An example is that of step 5, where immense amounts of detail can be found. The reasons for this is that such rather lengthy explanation will enable anyone in the area of IC design and manufacturing to use this method if there is a desire to understand the theory behind this method and there is a willingness to, not only use this method, but investigate the structural intricacies that make it work with such a simple set of steps. This simplicity is not to make up for lack of expertise in any of the disciplines that back this method up. It would be very foolish to assume that no knowledge and exposure to the material is necessary to get the best out of the solution laid out in this second section.

Finally, a summary table is presented outlining the series of steps and the general objective or objectives that each one of the steps fulfills. The table does not cover every aspect in retrospective, and it is hoped that this table (Table 12) will only provide for a reminder of what the previous chapters of this section have covered much more thoroughly. With this in mind, a simple case study was presented along showing the application of this method and the general problems that arise as each of the steps are covered.

Table 12

Methodology Summary

| Step # | Description | Objective(s) |
|---|---|---|
| 1 | Theory-based problem size reduction | Pin point the vital few variables that influence performance of the system. |
| 2 | Influential Processing Steps' Identification | Find those processing stages which have effect on the variables of step 1. Also, identify metrology that will give the values for the above variables. |
| 3 | CIM Database Query for Steps & Var... | Find the values needed for each parameter measured and recorded |
| 4 | Descriptive Statistical Analysis of... | Visualize & describe the central tendency of the samples. |
| 5 | Capability Analysis of the Data | Final reduction of set of variables and determination of variance for each of them and their capabilities. |
| 6 | VLSI Design Evaluation | Understand the motivations and functionality desires put forth at design stage of the system. |
| 7 | Layout Parameter Extraction (LPE) | Obtain SPICE readable netlist(s) that reflect on the system's charac_ teristics. |
| 8 | Design of Experiment(s) (DofE) | Maintain focus on the research by designing an experiment that will only concentrate on the important aspects of it. Also, determine one or more hypotheses to be tested next. |
| 9 | SPICE Calculations and Simulation Runs | Gathering of data and double-check SPICE-deck's LSLs, USLs & Targets. |
| 10 | Analysis of Result Set(s) | Give meaning to results obtained by simulation. |
| 11 | Product Functionality, Manufacturability & Other Implications | Understand the aftermath of effects that system performance causes on any issue of interest to the environ_ ment where the study is undergone. |

## 8.2 Conclusions

### 8.2.1 Regarding The Methodology

Thorough considerations have been provided to methodically characterize any system depending on the vital components that make it up. Brief or extended discussions have been made for each of the steps

of the method, depending on the knowledge base that is required to conduct such studies in the VLSI IC field in order to assess system performance and be able to predict accurately and precisely what characteristics the system will have from prior manufacturing and design considerations. Nevertheless, there is room for improvement and for future research work to provide with more extensive sets of tools to deal with the problems encountered in any particular phase of such an investigation.

This methodology provides simple tools to extract the parameters needed, perform statistical descriptions of their distributions, determine their capability and shape, understand the fundamental concepts behind both the process and the product, design an appropriate experiment that proves affordable and efficient, gather simulation data using tools such as SPICE, analyze the data resulting from the simulations and assess the repercussions that the characteristics of the system will have. This is a simple method, which attacks the problems associated with each of the steps in a complete manner and obtains the information required to further continue the methodology after each step.

It does not, however, provide a set of powerful tools that could attack specific problems that will be encountered in each of the steps. It gives certain basic techniques and tools which will direct the investigator to find more information that could lead to a satisfactory solution. Or, if it cannot provide the path to a solution , it will provide the path to a better understanding of the problem involved at each step for a particular system and will direct towards sources which can deal with the problem

more thoroughly.

It is a general method. As mentioned before, in section 2, it is impossible to provide detailed and specific procedures for solving the challenges of each step without losing the intended flexibility and possible outreach. Moreover, the method assumes certain amount of familiarity and/or expertise in certain areas, because without this familiarity most of the steps will be confusing and too complex to handle properly. If there is no expertise in the subject matter of each of the steps, the methodology assumes that there will be expert support and supervision overlooking the work done to achieve the particular objectives of each step, and therefore, the overall process to characterize a system.

The methodology does not deal with the design of either the semiconductor process or the VLSI system to be studied. These are matters that should be dealt with separately once testing of the process with a test chip has been done thoroughly. On the other hand, it will deal with the progressive improvement of both of the above by pointing out the relationships that exist between processing and product design. One more assumption made by this method is that of being able to obtain the necessary data for each of the considerations it tackles (manufacturing realities and design specifications).

The method does not concentrate on particular software tools, but they are used or mentioned because of the author's familiarity with them. Nevertheless, lacking proper software will hinder the extent in

which the methodology can properly characterize the system of interest in an accurate, precise and reliable manner. Furthermore, the software tools allow for more modeling capacity to be explored and statistically scrutinized.

Finally, the method leads towards the assessment of manufacturability of a product in a particular environment. It points out the shortcomings of either the product or the process to accommodate for smooth interactions to occur. Also, it tends towards a feedback loop where more detailed analysis either concentrating or expanding the number of variables can be undertaken. It will eventually state the repercussions of the characteristics of the process-product interactions and system performance in other areas that surround the engineering environment, such as cost of ownership, cycletime reduction and others of financial and managerial nature.

### 8.2.2 Regarding The Case Study

The nMOS inverter system, even though fundamentally simple, proved to be quite a challenge to the methodology. That is, it proved to be an indicator for those areas that need to be addressed in order for this methodology to be sound and robust.

This represents a dependency of the methodology on certain conditions. These conditions are pointed out in the previous subsection of this chapter. Nevertheless, there are some areas of specific concern that will be discussed in the next section of this chapter.

As far as the characterization of the nMOS inverter, there was a high degree of success from this methodology's standpoint. Analysis of SPICE, HSPICE, the mathematics of MOSFETs and of the nMOS inverter per se gave a good indication of which are the most prevalent variables that influence the good operation of the system.

Thanks to acquired knowledge with respect to the R.I.T. nMOS version 2.0 process, a simple way to determine which processing steps influenced the variables chosen in the first step was outlined. Even though the overall outcome of the heat treatments, chemical treatments and physical conditions in which ICs are manufactured has an effect on the performance of the product, certain operations have a particularly strong influence on particular parameters. These particular steps were identified and the measured data for each of them was gathered using database querying systems available for such purposes.

Simple descriptive statistics were calculated for each of these samples of measurements, as well as determination of the capability under which the operations (and results) exist. Since there were only three variables ($t_{ox}$, $R_s$ and $x_j$), the capability fully concentrated on each of them, without regard towards further reducing the number of causes to manageable levels, because the number is already manageable. It was observed that all these variables had high degrees of variability, means far from target levels (except for $R_s$) and very low capability indexes.

Once the general viewpoint was established for the system of choice, the design was considered, studied and understood from the

designer's viewpoint. It was found that no specifications were set out in this design, which was disappointing, and yet expected. It is rare to see that design considerations of variability are studied when a VLSI system is simulated and verified (at least in the author's experience). This hindered the characterization study since no comparative analysis other than that of specific values would be possible from a statistical standpoint. Moreover, LPE was not possible under the Mentor Graphics IC verification toolset. The reasons for this included the fact that CheckMate™ only allows for CMOS systems to be parametrized. It does not provide for a depletion mode device definition. Also, the parasitics extraction would be impossible, even in CMOS systems, because MaskPE™ is a T. I. Corp. licensed software tool that is not available without a large monetary investment.

To get around this problem, MOSIS nMOS definitions and models were used under a $\lambda$=2 $\mu$m design rule setting, as well as HSPICE's enhanced capability over regular SPICE. Next, a designed experiment was planned and defined. A three-level three-factor design was chosen for reasons applicable to the study of the parameters from lower specifications to upper specifications. It was decided that due to the extensive amount of variability in the process, the lower level and the upper level would be set to only -2$\sigma$ and +2$\sigma$ respectively.

HSPICE H9000D was used to simulate the circumstances designed into the Box-Behnken experiment. Results were obtained for all except the time delay due to problems that were not circumvented in a satisfactory manner. It was found that the Ring Oscillator simulation

would converge to a stable state and after several time consuming attempts, the matter was decided to be inconclusive. In any case, most of the results proved to be good, and variations were noted.

Problems got out of hand in the analysis section of the methodology. Due to the lack of design-stage specifications (LSL, USL, Target), proper variability simulation runs using standard (such as MOSIS) files at design-phase and complete non-existance of test data at manufacturing-stage, comparative analysis was impossible to be made. Therefore, inconclusive statistical results exist. The only possible analysis was a point analysis, i.e., that in which single values are checked against the single values given by the designer.

Finally, assessments of manufacturability were given on a limited basis, as well as with regard to other subjects being affected by performance of the system. The reason for this is that of the inconclusive nature of the analysis. Certainly, it was noted were the methodology lacked robustness, but this robustness is not directly related to the theoretical basis on which the method stand. It is rather dependent on the environment in which the method is used and how favorable the conditions are for its intended objectives. Therefore, a set of recommendations is necessary to address this environmental factors that affect the methodology and without which this method proves cumbersome and inconclusive.

## 8.3 Recommendations

Some subjects need to be addressed and certain amount of work should be done in the future to fill in the gaps which presently exist and were noted as environmental flaws towards the methodology proposed in this document. This is either a flaw on the methodology by not taking these circumstances into account, or there is a real need to solve these challenges to create appropriate conditions for this method to be used. The subjects are:

1.) LPE needs to be expanded to accommodate for systems of various technological configurations, such as CMOS, BJT, BiCMOS and maybe nMOS (even though this is an old technology, but still a good learning tool in academic environments). Also, obtain such software to be able to extract parasitics, which turn out to be very important in the performance modeling of any system.

2.) Design specifications and pre-manufacturing simulations to accommodate for appropriate comparison points for after manufacturing analysis, as well as the use of the method for performance prediction and improvement set forth in this thesis.

3.) Set specification limits for each measurement made across all the fabrication processes currently running at the R.I.T. Fab to ease the strains put forth on the descriptive analyses and capability studies to be performed in future endeavors.

4.) Metrology Characterization and gauge capability should be worked throughout the fabrication facility in order to rule out effects due to poor, inaccurate, imprecise, unreliable and non-repeatable measurements.

5.) Capability analysis shown in the appendixes of this thesis should be analyzed carefully, and variability reduction measures should be taken across the R.I.T. Fab. This includes the protection against erroneous data from entering the MESA system, by properly installing safeguards against such occurrences.

6.) A serious need to obtain product parameter values after completion of the processing is noted. There needs to be test data for each and every one of the parameters that are to be used in modeling (using SPICE, HSPICE, Accusim, or any others). Without these data, comparative statistical analyses are useless.

7.) Non-normal distributions are common in IC processing. They require novel methods and techniques for analysis and use in capability determinations and statistical inferences (as stated in table 7). These are to be studied and appropriate training is to be provided for future endeavors, maybe by the C.Q.A.S. at R.I.T.

8.) More in-depth research efforts will be required for more complex systems. Therefore, favorable conditions are in need if results and robust conclusions are to be obtained from this methodology.

9.) Due to its dependence on threshold voltage, noise margins should be investigated in future efforts. That is, the effects of threshold voltage and indirectly of the fundamental variables studied in this thesis (or others), should be considered having the noise margins as response variables.

# REFERENCES


[1] Meta-Software Inc., HSPICE User's Manual (Chpt. 7). 1990.

[2] J. P. Uyemura, Circuit Design For CMOS VLSI (Chpt. 2). KAP 1992.

[3] N. Weste, K. Eshraghian, Principles of CMOS VLSI Design: A Systems Perspective (Chpt. 3). Addisson-Wesley, 1988.

[4] L. F. Fuller, "Six Sigma Process Capability in Student-Run IC Factory," TQM Talks with IBM Corp. 1992.

[5] N. Weste, K. Eshraghian, Principles of CMOS VLSI Design: A Systems Perspective (Chpt. 1). Addisson-Wesley, 1988.

[6] J.P. Uyemura, Circuit Design For CMOS VLSI (Chpt. 2). KAP, 1992.

[7] Y. P. Tsividis, Operation and Modeling of THE MOS TRANSISTOR (Chpt. 4). McGraw-Hill, 1987.

[8] J.P. Uyemura, Circuit Design For CMOS VLSI (Chpt. 2). KAP, 1992.

[9] A. Mukherjee, Intoduction to nMOS & CMOS VLSI Systems Design (Chpt. 2). Prentice-Hall, 1985.

[10] J.P. Uyemura, Circuit Design For CMOS VLSI (Chpt. 3). KAP, 1992.

[11] N. Weste, K. Eshraghian, Principles of CMOS VLSI Design: A Systems Perspective (Chpt. 2). Addisson-Wesley, 1988.

[12] M. Perez-Wilson, Machine/Process Capability Study (Section 1). Copyright © 1989, by Mario Perez-Wilson.

[13] M. Perez-Wilson, Machine/Process Capability Study (Section 2). Copyright © 1989, by Mario Perez-Wilson.

[14] AS/400 System Utilities Manual, IBM Corporation (Chpt. 3). Copyright © 1988, 1990 by IBM Corp.

[15] M. Perez-Wilson, Machine/Process Capability Study (Section 4).

Copyright © 1989, by Mario Perez-Wilson.

[16] M. Perez-Wilson, Machine/Process Capability Study (Section 5). Copyright © 1989, by Mario Perez-Wilson.

[17] M. Perez-Wilson, Machine/Process Capability Study (Section 6). Copyright © 1989, by Mario Perez-Wilson.

[18] Mentor Graphics® Checkmate™ Release 2.2 User's Manual. Copyright © 1992 by Mentor Graphics Corporation.

[19] T. B. Barker, Quality by Experimental Design (Part 2). Marcel Dekker, 1985.

[20] R. C. Jaeger, Introduction to Microelectronic Fabrication (Chpt. 4). Addison-Wesley, 1988.

[21] Meta-Software Inc., HSPICE User's Manual (Chpt. 7). 1990.

# BIBLIOGRAPHY


1.- Meta-Software Inc., HSPICE User's Manual. Copyright ©1990.

2.- Y. P. Tsividis, Operation and Modeling of The MOS Transistor McGraw-Hill, 1987.

3.- J. P. Uyemura, Circuit Design For CMOS VLSI, KAP, 1992.

4.- N. Weste, K. Eshraghian, Principles of CMOS VLSI Design: A Systems Perspective. Addison-Wesley, 1988.

5.- A. Mukherjee, Introduction to nMOS & CMOS VLSI Systems Design. Prentice Hall, 1986.

6.- J. F. Freund, G. A. Simon, Modern Elementary Statistics, Prentice Hall, 1992.

7.- T. B. Barker, Quality by Experimental Design. Marcel Dekker, 1985.

8.- M. Perez-Wilson, Machine/Process Capability Study. Copyright © 1989, by Mario Perez-Wilson.

9.- Mentor Graphics® Checkmate™ Release 2.2 User's Manual & other MentorGraphics® tools and User's Manuals. Copyright © 1992 by Mentor Graphics Corporation.

10.- D. C. Montgomery, Design and Analysis of Experiments 3rd Edition. Wiley, 1991.

11.- W. R. Dillon, M. Goldstein, Multivariate Analysis: Methods & Applications. Wiley, 1984.

12.- E. R. Ott, E. Schilling, Process Quality Control 2nd Edition. McGraw-Hill, 1990.

13.- T. B. Barker, Engineering Quality by Design: Interpreting the

Taguchi Approach. Marcel Dekker, 1990.

14.- J. A. Cornell, Experiments With Mixtures 2nd Edition. Wiley, 1990.

15.- N. Draper, H. Smith, Applied Regression Analysis. Wiley, 1981.

16.- R. A. Johnson, D. W. Wichern, Applied Multivariate Statistical Analysis. Prentice-Hall, 1992.

# APPENDIX A

## *Guggenheim Wafer Sizing Machine Definition*

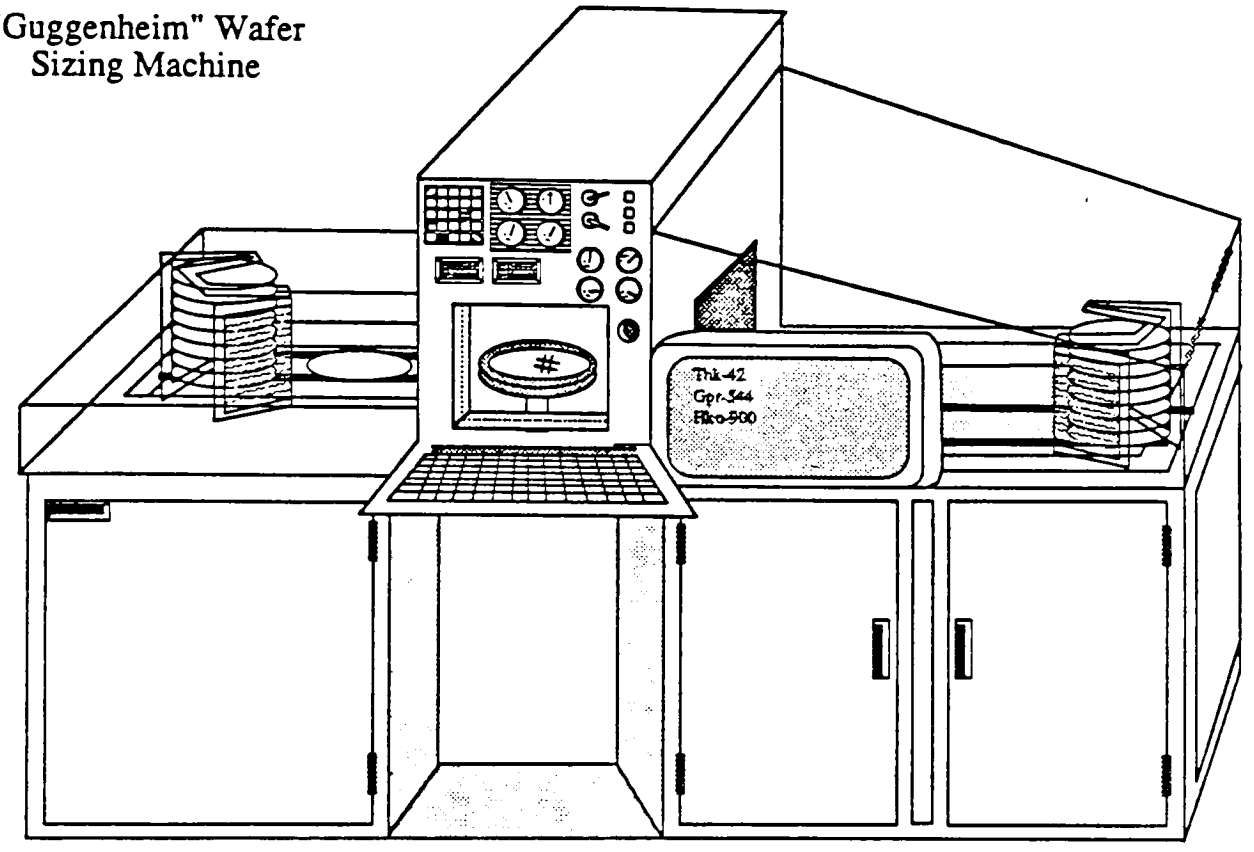
*(From reference [13])*

## Machine Definition

Step 1. Describe the "Functional Characteristics" of the machine under study.

Example:

"Guggenheim" Wafer Sizing Machine




## Functional Characteristics

1. Wafer Transportation System
2. Grinding Component System
3. Work Holding System
4. Rinse and Dry System
5. Thickness Gauging System

## Machine Definition

Step 1. Describe Functional Characteristics of Machine under study

## Description

1. Wafer Transportation System -

   The wafer transportation system automatically unloads wafers from a cassette, transports the wafers from station to station and automatically loads the wafers into a receive cassette when processing is complete.

2. Grinding Component System

   The grinding component system is comprised of a 1st cutter, 2nd cutter which are driven by a programmable motor of variable speed (100-5000 rpm). The z-axis is programmable and is made up of two steps, the z and z'. The z has a variable feed rate of 1-100 microns per second, the z' has a variable feed rate of 1-50 microns per second. Polish time is also programmable, from 0-20 seconds.

3. Work Holding System

   The work holding system is made up of a programmable variable speed vacuum chuck, which operated in the range of 10-500 rpm.

4. Rinse and Drying System

   The rinse station has a vacuum chuck with dual variable speed, 100-5000 rpm. It sprays D.I. water to rinse, and spins dry.

5. Wafer Gauging System

   The wafers are gauged after they are sized using a contact thickness gauge.

## Machine Definition

Step 2. List the distinguishing qualitative features added to the product by the machine. (Response Variables)

## Response (Dependent) Variables

Wafer:

1. Thickness,
2. Strength
3. Flatness
4. Surface Finish

## Questions

What kind of data are available in these Response Variables ?

| | |
|---|---|
| Attributes Data: | Yes/No, 1/0, Good/Bad, Pass/Fail |
| | N - Nominal |
| | O - Ordinal |
| Variable Data: | I - Interval |
| | R - Ratio |

| Response | Type of Data | Property of Data | Measurement Scale |
|---|---|---|---|
| 1. Thickness | Variable | Continuous | Ratio |
| 2. Strength | Variable | Discrete | Ratio |
| 3. Flatness | Variable | Continuous | Ratio |
| 4. Surface Finish | Attribute | Discrete | Ordinal |

Step 3. List the independent variables internal to the machine (Factors).

## Independent Variables (Functional Characteristics)

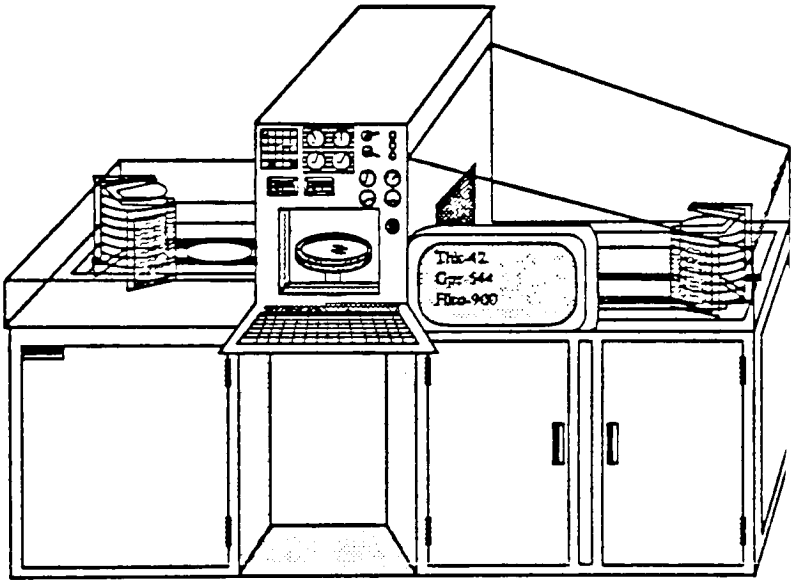
### Wafer Transportation System

Pickup &Place Misalignment
Vacuum Suction
Conveyor Belt
Cassette for Wafers

### Grinding Component System

1st Cutter Spin Speed
1st Cutter Polish Time
1st Cutter z Rate
1st Cutter Abrasive Concentration
1st Cutter z' Rate
2nd Cutter Spin Speed
2nd Cutter Polish Time
2nd Cutter z Rate
2nd Cutter Abrasive Concentration
Grinding Force
Sharpness of Cutters

"Guggenheim" Wafer Sizing



### Work Holding Station

Composition of Holder
Rotational Speed of Holder
Flatness of Holder
Hold down pressure
Cutting Lubricant

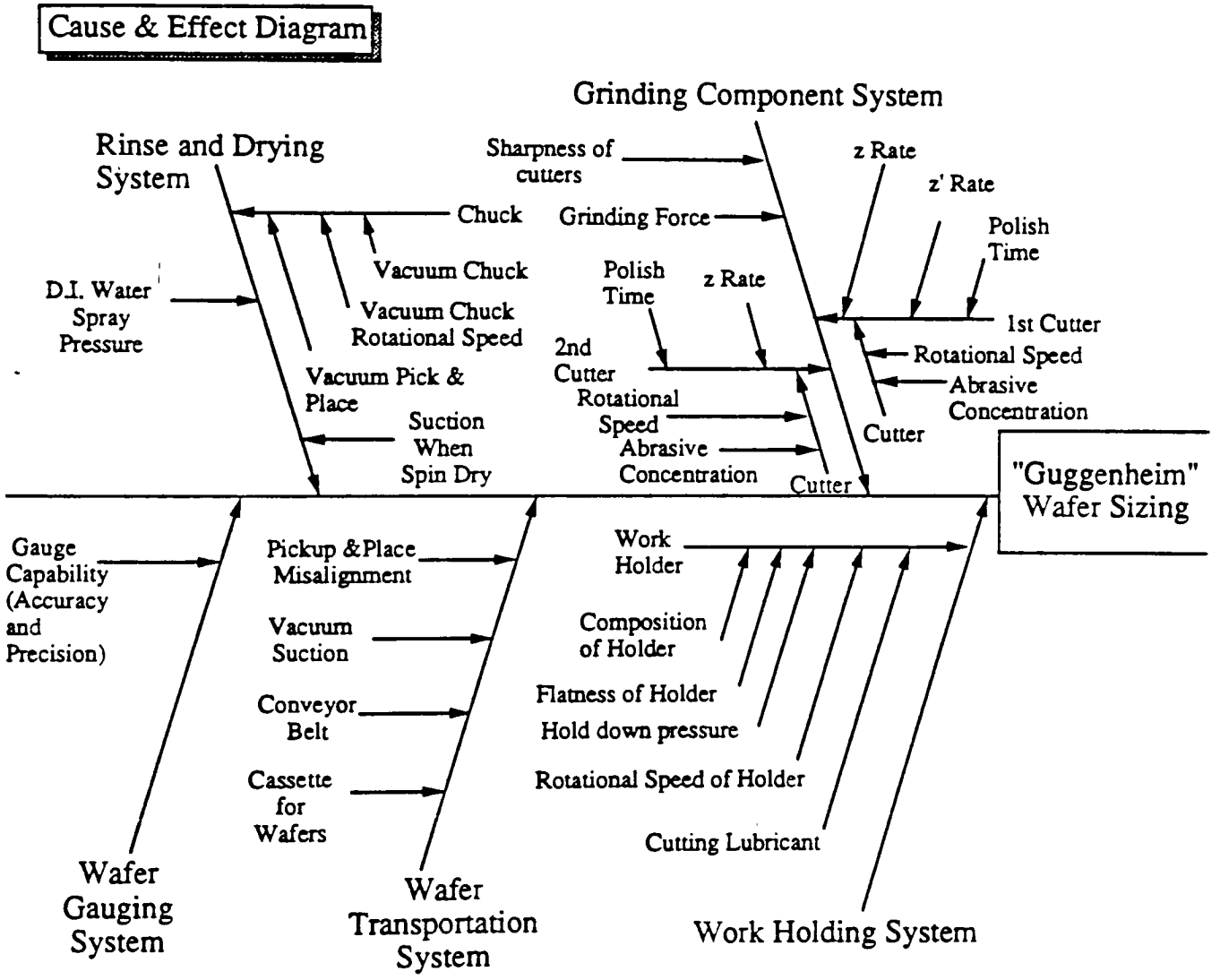
### Rinse and Drying System

Vacuum Chuck
Vacuum Chuck Rotational Speed
Vacuum Pick & Place
D.I. Water Pressure Spray
Suction When Spin Dry

### Wafer Gauging System

Gauge Capability

A modified Cause and Effect diagram, like the one below can help organize the inputs from a brainstorming session to identify the independent variables in each Functional Characteristic of the machine under study.



Step 4. Form a Cause And Effect Cross-reference Table between the independent variables and the dependent (response) variables.

Program _____ MACHINE/PROCESS CAPABILITY STUDY

Responsible Person _____ C&E CROSS-REFERENCE TABLE

| Study # | |
|---|---|
| Date | |
| Operation | |
| Equip # | |
| Page | of |

MACHINE/PROCESS

RANK-ORDER: ☐ Yes ☐ No

INDEPENDENT VARIABLES

| DEPENDENT → / INDEPENDENT | *Thickness* | *Strength* | *Flatness* | *Surface Finish* | | | | TOTAL | LEVEL OF INDEPENDENT |
|---|---|---|---|---|---|---|---|---|---|
| *Pick & Place Misalign* | | | | | | | | | |
| *Vacuum Suction* | | | | | | | | | |
| *Conveyor Belt* | | | | | | | | | |
| *Cassette for Wafers* | | | | | | | | | |
| *1st Cutter Spin Speed* | | | | | | | | | |
| *1st Cutter Polish Time* | | | | | | | | | |
| *1st Cutter z Rate* | | | | | | | | | |
| *1st Cutter Abrasive Concentration* | | | | | | | | | |
| *1st Cutter z' Rate* | | | | | | | | | |
| *2nd Cutter Spin Speed* | | | | | | | | | |
| *2nd Cutter Polish Time* | | | | | | | | | |
| *2nd Cutter z Rate* | | | | | | | | | |
| *2nd Cutter Abrasive Concentration* | | | | | | | | | |
| *Grinding Force* | | | | | | | | | |
| *Composition of Holder* | | | | | | | | | |
| *Rotational Speed of Holder* | | | | | | | | | |
| *Flatness of Holder* | | | | | | | | | |
| *Hold down pressure* | | | | | | | | | |
| *Cutting Lubricant* | | | | | | | | | |
| *Sharpness of Cutters* | | | | | | | | | |
| *Vacuum Chuck Dry & Rinse* | | | | | | | | | |
| *Vacuum Chuck Spindle* | | | | | | | | | |
| *Vacuum Pick & Place* | | | | | | | | | |
| *DI Water Pressure Spray* | | | | | | | | | |
| *Suction when Spin Dry* | | | | | | | | | |
| *Gauge Capability* | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |

Place the Independent Variables in any order or group them by machine functional characteristic

Mark with an 'X' the independent variables that you theorize influence the variability of the response variable.

Program _____

Responsible Person _____

## MACHINE/PROCESS CAPABILITY STUDY

C&E CROSS-REFERENCE TABLE

| | |
|---|---|
| Study # | |
| Date | |
| Operation | |
| Equip # | |
| Page | of |

MACHINE/PROCESS

RANK-ORDER: ☐ Yes ☐ No

| DEPENDENT → / ↓ INDEPENDENT | *Thickness* | *Strength* | *Flatness* | *Surface Finish* | | | | TOTAL | LEVEL OF INDEPENDENT |
|---|---|---|---|---|---|---|---|---|---|
| *Pick & Place Misalign* | | | | | | | | | |
| *Vacuum Suction* | | | | | | | | | |
| *Conveyor Belt* | | | | | | | | | |
| *Cassette for Wafers* | | | | | | | | | |
| *1st Cutter Spin Speed* | X | X | | X | | | | | |
| *1st Cutter Polish Time* | X | X | | X | | | | | |
| *1st Cutter z Rate* | X | X | X | X | | | | | |
| *1st Cutter Abrasive Concentration* | X | X | X | X | | | | | |
| *1st Cutter z' Rate* | X | X | X | X | | | | | |
| *2nd Cutter Spin Speed* | X | X | | X | | | | | |
| *2nd Cutter Polish Time* | X | X | X | X | | | | | |
| *2nd Cutter z Rate* | X | X | X | X | | | | | |
| *2nd Cutter Abrasive Concentration* | X | X | X | X | | | | | |
| *Grinding Force* | | | X | X | | | | | |
| *Composition of Holder* | | | | | | | | | |
| *Rotational Speed of Holder* | X | X | | X | | | | | |
| *Flatness of Holder* | | X | X | | | | | | |
| *Hold down pressure* | | | | | | | | | |
| *Cutting Lubricant* | | | X | | | | | | |
| *Sharpness of Cutters* | | | | | | | | | |
| *Vacuum Chuck Dry & Rinse* | | | | | | | | | |
| *Vacuum Chuck Spindle* | | | | | | | | | |
| *Vacuum Pick & Place* | | | | | | | | | |
| *DI Water Pressure Spray* | | X | | | | | | | |
| *Suction when Spin Dry* | | | | | | | | | |
| *Gauge Capability* | | | X | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |

Rank order the independent variables.

Program

Responsible Person

MACHINE/PROCESS CAPABILITY STUDY

C&E CROSS-REFERENCE TABLE

| Study # | |
|---|---|
| Date | |
| Operation | |
| Equip # | |
| Page | of |

MACHINE/PROCESS

RANK-ORDER: ☐ Yes ☐ No

| DEPENDENT → / INDEPENDENT ↓ | *Thickness* | *Strength* | *Flatness* | *Surface Finish* | | | | TOTAL | LEVEL OF INDEPENDENT |
|---|---|---|---|---|---|---|---|---|---|
| *1st Cutter z Rate* | X | X | X | X | | | | 4 | |
| *1st Cutter Abrasive Concentration* | X | X | X | X | | | | 4 | |
| *1st Cutter z' Rate* | X | X | X | X | | | | 4 | |
| *2nd Cutter Polish Time* | X | X | X | X | | | | 4 | |
| *2nd Cutter z Rate* | X | X | X | X | | | | 4 | |
| *2nd Cutter Abrasive Concentration* | X | X | X | X | | | | 4 | |
| *1st Cutter Spin Speed* | X | X | | X | | | | 3 | |
| *1st Cutter Polish Time* | X | X | | X | | | | 3 | |
| *2nd Cutter Spin Speed* | X | X | | X | | | | 3 | |
| *Rotational Speed of Holder* | X | X | | X | | | | 3 | |
| *Grinding Force* | | | X | X | | | | 2 | |
| *Flatness of Holder* | | X | X | | | | | 2 | |
| *Cutting Lubricant* | | | X | | | | | 1 | |
| *DI Water Pressure Spray* | | X | | | | | | 1 | |
| *Gauge Capability* | | | X | | | | | 1 | |
| *Pick & Place Misalign* | | | | | | | | | |
| *Vacuum Suction* | | | | | | | | | |
| *Conveyor Belt* | | | | | | | | | |
| *Cassette for Wafers* | | | | | | | | | |
| *Composition of Holder* | | | | | | | | | |
| *Hold Down Pressure* | | | | | | | | | |
| *Sharpness of Cutters* | | | | | | | | | |
| *Vacuum Chuck Dry & Rinse* | | | | | | | | | |
| *Vacuum Chuck Spindle* | | | | | | | | | |
| *Vacuum Pick & Place* | | | | | | | | | |
| *Suction when Spin Dry* | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |

The Cause & Effect Cross-reference Table helps to identify the independent variables that are:

- Most important for the machine, and
- Most important for each dependent (response) variable.

The independent variables are in:

- Rank-order of importance, or
- Rank-order of influence to variability to the dependent variable.

Program _____ MACHINE/PROCESS CAPABILITY STUDY — Study # | Date | Operation | Equip # | Page of

Responsible Person _____ C&E Cross-reference Table

Machine/Process _____ RANK-ORDER: ☐ Yes ☐ No

| DEPENDENT → / INDEPENDENT ↓ | Thickness | Strength | Flatness | Surface Finish | | | | TOTAL | LEVEL OF INDEPENDENT |
|---|---|---|---|---|---|---|---|---|---|
| 1st Cutter z Rate | X | X | X | X | | | | 4 | |
| 1st Cutter Abrasive Conc | X | X | X | X | | | | 4 | |
| 1st Cutter z' Rate | X | X | X | X | | | | 4 | |
| 2nd Cutter Polish Time | X | X | X | X | | | | 4 | |
| 2nd Cutter z Rate | X | X | X | X | | | | 4 | |
| 2nd Cutter Abrasive Conc | X | X | X | X | | | | 4 | |
| 1st Cutter Spin Speed | X | X | | X | | | | 3 | |
| 1st Cutter Polish Time | X | X | | X | | | | 3 | |
| 2nd Cutter Spin Speed | X | X | | X | | | | 3 | |
| Rotational Speed of Holder | X | X | | X | | | | 3 | |
| Grinding Force | | | X | X | | | | 2 | |
| Flatness of Holder | | X | X | | | | | 2 | |
| Cutting Lubricant | | | X | | | | | 1 | |
| DI Water Pressure Spray | | X | | | | | | 1 | |
| Gauge Capability | | | X | | | | | 1 | |
| Pick & Place Misalign | | | | | | | | | |
| Vacuum Suction | | | | | | | | | |
| Conveyor Belt | | | | | | | | | |
| Cassette for Wafers | | | | | | | | | |
| Composition of Holder | | | | | | | | | |
| Hold Down Pressure | | | | | | | | | |
| Sharpness of Cutters | | | | | | | | | |
| Vacuum Chuck Dry & Rinse | | | | | | | | | |
| Vacuum Chuck Spindle | | | | | | | | | |
| Vacuum Pick & Place | | | | | | | | | |
| Suction when Spin Dry | | | | | | | | | |

**Vital Few Independent Variables**

**Trivial Many Independent Variables**

# APPENDIX B

*Theory-based Reduction to Vital Few*

*Causes for the nMOS Inverter's Performance*

# 2. Process and Device Parameter Targets

MOSIS insists that all NMOS fabricators meet the following Scalable NMOS Process and Dev Parameter Targets:

| PARAMETER | UNITS | ENHANCEMENT | DEPLETION |
|---|---|---|---|
| 1. $V_{tc}$(large xtor) | volts | 0.7⟷1.0 | -3.5⟷-2.5 |
| 2. K PRIME $\frac{\epsilon_{ox}\mu}{t_{ox}}$ | $\mu a/volt^2$ | 20⟷30 | 20⟷30 |
| 3. GAMMA(large xtor) | $Volts^{1/2}$ | 0.30⟷0.50 | 0.30⟷0.50 |
| 4. $N_{sub}$ | $10^{15}/cm^3$ | 1⟷9 | 0.5⟷1.5 |
| 5. $\mu_c$ (surface) | $cm^2$/volt-sec | 600⟷800 | 600⟷800 |
| 6. $T_{ox}$ | angstroms | 450.⟷600. | 450.⟷600. |
| 7. DEL L (drawn-effective) | microns | 0⟷1.5 | 0⟷1.5 |
| 8. DEL W (drawn-effective) | microns | -0.2⟷0.6 | -0.2⟷0.6 |
| 9. PUNCHTHROUGH | volts | >7 | >7 |
| 10. DRAIN BREAKDOWN | volts | >20 | >20 |
| 11. METAL FIELD THR. | volts | >10 | >10 |
| 12. POLY FIELD THR. | volts | >7 | >7 |

(cont.)

| PARAMETER | UNITS | |
|---|---|---|
| 13. $x_j$ (junction depth) | microns | 0.3⇔0.6 |
| 14. $C_{ox}$(Gate Oxide) | $^{fF}/_{\mu^2}$ | 0.62⇔0.84 |
| 15. $C_{poly/field}$ | $^{fF}/_{\mu^2}$ | .045⇔.064 |
| 16. $C_{metal/field}$ | $^{fF}/_{\mu^2}$ | .020⇔.030 |
| 17. $C_{metal/poly}$ | $^{fF}/_{\mu^2}$ | .035⇔.050 |
| 18. $C_j$ (junct bott.) | $^{fF}/_{\mu^2}$ | .09⇔.15 |
| 19. $C_{jp}$ (junct per.) | $^{fF}/_{\mu^2}$ | .1⇔.35 |
| 20. $R_{poly}$ | ohms/sq. | <40 |
| 21. $R_{n+ diff}$ | ohms/sq. | <30 |
| 22. $R_{metal}$ | ohms/sq. | <.05 |
| 23. JUNCTION LEAKAGE | $^{fA}/_{\mu^2}$ | .1 (typical) |

METAL CURRENT DENSITY LIMIT 1.0 mA/um (of conductor width)

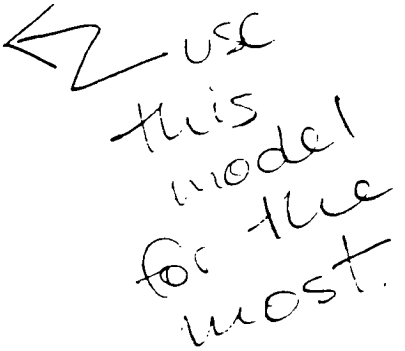
# 3. SPICE Parameters

The following are three sets of SPICE parameters that were extracted from three different MOSIS fabrication runs (M43D, M46L, M48U). These parameters are typical of the current MOSIS fabricator base. The parameters will be revised as we gain further experience with these fabricators. Users should note that the SPICE model parameters are obtained via transistor DC curve fitting using a parameter optimizer. These Level = 2 parameters are treated as empirical parameters allowing the optimizer to change parameters for best curve fit to measured transistor curves without regard for consistency with the parameter targets listed above. The simulated test circuit (inverters and ring oscillator) performance is accurate to within 10% to 20% of measured performance. Because of the empirical nature of the DC parameters, it is possible that there will be larger errors observed in simulating certain kinds of dynamic circuits that depend upon accurate AC capacitor model information. New parameter measurement equipment is being added to the MOSIS test facility along with revised model parameter extractor/optimizer methods which will greatly improve simulation accuracy of dynamic circuits.

Typical SPICE parameters for the MOSIS NMOS process are:

```
SPICE set #1

 MODEL NMOSE NMOS LEVEL=2.00000 LD=0.826296U TOX=544.000E-10
+NSUB=2.09C161E+15 VTO=1.14181 KP=3.730740E-05 GAMMA=0.628861
+PHI=0.600000 UO=300.000 UEXP=1.001000E-03 UCRIT=1.000000E+06
+DELTA=1.15554 VMAX=100000. XJ=1.31233U LAMBDA=3.101167E-02
+NFS=1.902288E-12 NEFF=1.001000E-02 NSS=0.000000E+00 TPG=1.00000
+RSH=25.4 CGSO=1.6E-10 CGDO=1.6E-10 CGBO=1.7E-10 CJ=1.1E-4
+MJ=0.5 CJSW=5E-10 MJSW=0.33
.MODEL NMOSD NMOS LEVEL=2.00000 LD=1.01616U TOX=544.000E-10
+NSUB=1.000000E+16 VTO=-3.78687 KP=3.281897E-05 GAMMA=0.371506
+PHI=0.600000 UO=800.000 UEXP=1.001000E-02 UCRIT=804753.
+DELTA=2.79525 VMAX=674713. XJ=0.600132U LAMBDA=1.000000E-0E
+NFS=4.310000E+12 NEFF=1.001000E-02 NSS=0.000000E+00 TPG=1.00000
+RSH=25.4 CGSO=1.6E-10 CGDO=1.6E-10 CGBO=1.7E-10 CJ=1.1E-4
+MJ=0.5 CJSW=5E-10 MJSW=0.33
```




Nevertheless,
apply to
LEVEL = 3 mode!
(LAMBDA, UEXP, UCRIT, NEF
are non-existent in Level

***MODEL PARAMETERS:***

Level = 3
COX = calculated from TOX
KAPPA = default value
KP = see SPICE set #1 value on previous sheets from MOSIS
TOX = variable!!!
VMAX = see SPICE set #1 value on previous sheets from MOSIS
DEL = neglected
LD = see SPICE set #1 value on previous sheets from MOSIS
LREF = neglected
WD = neglected
WMLT = default value
WREF = neglected
LMLT = default value
XJ = variable!!!
XL = negleced
XW = neglected
DELTA = see SPICE set #1 value on previous sheets from MOSIS
ETA = neglected
GAMMA = see SPICE set #1 value on previous sheets from MOSIS
LND = neglected
LN0 = neglected
ND = neglected
N0 = neglected
NFS = see SPICE set #1 value on previous sheets from MOSIS
NSUB = 3.1E+14 (from average of step 2 $R_{sh}$ and a conversion table)
PHI = calculated from NSUB
VTO = see SPICE set #1 value on previous sheets from MOSIS
WIC = neglected
WND = neglected
WN0 = neglected
THETA = neglected
UO = see SPICE set #1 value on previous sheets from MOSIS
ACM = 3

JS = 1E-04
JSW = 1E-10
IS = default value
N = default value
NDS = default value
VNDS = default value
CBD = calculated from CJ and AD
CBS = " "
CJ = see SPICE set #1 value on previous sheets from MOSIS
CJSW = see SPICE set #1 value on previous sheets from MOSIS
CJGATE = neglected
FC = default value
MJ = see SPICE set #1 value on previous sheets from MOSIS
MJSW =
PB = default value
PHP = default value
TT = neglected
RD = 700 Ω (typical value)
RDC = 1 Ω (typ. val. averaged from all contacts related to source region)
RS = 700 Ω (typical value)
RSC = 1 Ω (typ. val. averaged from all contacts related to drain region)
RSH = variable!!!
LDIF = 1/8 of geometric length drawn (approximated)
HDIF = 7/8 of geometric length drawn (approximated)
XW = neglected
DELVTO = neglected
NGATE = neglected
NSS = from SPICE set #1 on previous sheeets from MOSIS
TPG = +1
ALPHA = neglected
LALPHA = neglected
WALPHA = neglected
VCR = neglected
LVCR = neglected
WVCR = neglected

IIRAT = neglected
CAPOP = 9
CGBO = see SPICE set #1 value on previous sheets from MOSIS
CGDO = see SPICE set #1 value on previous sheets from MOSIS
CGSO = see SPICE set #1 value on previous sheets from MOSIS
METO = neglected
CF1 = default value
CF2 = default value
CF3 = default value
CF4 = default value
CF5 = default value
CF6 = default value
CGBEX = default value
XQC = default value
AF = neglected
KF = neglected
NLEV = neglected
GDSNOI = neglected
BEX = neglected
CTA = neglected
CTP = neglected
EG = neglected
F1EX = neglected
GAP1 = neglected
GAP2 = neglected
LAMEX = neglected
PTA = neglected
PTC = neglected
PTP = neglected
TCV = neglected
TLEV = neglected
TLEVC = neglected
TRD = neglected
TRS = neglected
XTI = neglected

***ELEMENT PARAMETERS:***

AD = from layout
AS = from layout
DTEMP = neglected
GEO = **1** for depletion transistor and **2** for enhancement transistor
L = from layout
mname = one for each transistor
M = 1 (no multiple devices)
Mxxx = one for each transistor in netlist
nd = set for each transistor node
ng = set for each transistor node
ns = set for each transistor node
nb = set for each transistor node
NRD = from layout
NRS = from layout
OFF (for enhancement devices only as a initial condition)
PD = from layout
PS = from layout
IC = vds, vgs, vbs (initial conditions for transistors if necessary)
W = from layout

.OPTIONS SCALE = 1E-6 for microns

Remember that all the above values are to be given in units given in table 1.

Using nMOS inverter theory, scrutiny of the inverter's mathematical description leads to the following standard metrics:

$V_{inv}$

$t_d$

Gain

I-V relationships

---

Starting with $V_{inv}$, let us define it as explained by techniques 2 and 3 and then identify the main "players" with help of the Pareto principle (technique 1).

1.)

$$V_{inv} = V_{tpd} + [(V_{dd} - V_{out})/(\beta_{inv})^{1/2} \text{ such that } \beta_{inv} = (W/L)_{pd}/(W/L)_{pu}$$

$V_{dd}$ is constant

$V_{out}$ is assumed to be $0.5V_{dd}$

W is actually $W_{eff}$ which considers all effects from non-idealities of lithography.

L is also actually $L_{eff}$

from HSPICE Manual pg. 7-84:

$W_{eff}$ = M(Wscaled·WMLT + XWscaled - 2·WDscaled)

$L_{eff}$ = Lscaled·LMLT + XLscaled - 2·(LDscaled + DELscaled)

such that Wscaled = W·SCALE and Lscaled = L·SCALE and W. L and SCALE are specified. W and L come from layout geometry. The rest are parameters that account for the reality of semiconductor diffusion, etching and masking effects as well as shrinking or multiplicity of devices. Everyone of these parameters are constant, except for WDscaled, LDscaled, XWscaled and XLscaled. These four parameters depend on circumstances that occur usually in semiconductor processing. Nevertheless, XW & XL are ignored for their importance is not recognizable without further study. The other two are heavily dependent on the metallurgical junction depth of diffusions, XJ. This parameter tends to vary in a normally distributed manner (if implanted and heat treated or annealed afterwards). Thus, it should be considered

carefully.

$V_{tpd}$ is the threshold voltage of the enhancement (or pull-down) device. The formula for this is found on page 22 (Chapter 2). Another version (for a level=3 model in HSPICE) is found on page 7-84 of the manual.

$V_{th} = V_{bi} - [(8.14E\text{-}22 \cdot ETA)/(COX \cdot L_{eff}^3)] \cdot v_{ds} + GAMMA \cdot fs \cdot (PHI + v_{sb})^{1/2}$
$+ fs \cdot (PHI + v_{sb})$ such that

$V_{bi} = V_{fb} + PHI$
$V_{fb} = \Phi_{ms} - [(q \cdot NSS)/COX] + DELVTO$
$\Phi_{ms} = type \cdot [-TPG \cdot v_t \cdot \ln(NGATE(10^6)/n_i) - 0.5 \cdot PHI]$
type = +1
TPG = +1
NGATE = constant defaulted value
PHI = calculated from NSUB
NSS = constant (as shown in previous pages)
DELVTO = neglected
$COX = \varepsilon_{ox}/TOX$
TOX = thickness of gate
ETA = default value above mentioned
$GAMMA = COX^{-1} \cdot (2q\varepsilon_{si}NSUB)^{1/2}$ and is proportional to TOX
fs is proportional to XJscaled

Thus, for $V_{inv}$ alone, the most recurrent and fundamental (because of the trace of equations back to them) variables are XJ and TOX.

---

Gain: it is defined as the square root of the ratio of the pull-down MOSFET process gain factor to the pull-up MOSFET gain factor. That is,

$$Gain = [(W/L)_{pd}/(W/L)_{pu}]^{1/2}$$

As seen in the discussion for inversion voltage, both W and L are actually the effective width and length of each device. Thus, they are

dependent on geometrical design and actual processing non-idealities. It was found there is a proportional relationship to XJ. Thus, other than this relationship, none other than the channel modulation $\lambda$ influences this metric. Nevertheless, $\lambda$ is not considered at all in the level=3 model.

---

Propagation delay ($t_d$): it is limited by the speed at which the load or parasitic capacitances in the circuit can be charged or discharged during a transition between states. All the device capacitances are voltage dependent and most of the time all capacitive effects can be summed up to form a single load capacitance. Also, the time delay can be viewed as either the charge or the discharge time for the inverter.

The discharge delay, $t_{phl}$ (high-to-low) is given by:

$$t_{phl} = [C_{TOT}/(2 \cdot ABS(I_{avg}))] \cdot (V_h - V_l)$$

The charge delay, $t_{plh}$ (low-to-high) is given by:

$$t_{plh} = [C_{TOT}/(2 \cdot ABS(I_{avg}))] \cdot (V_h - V_l)$$

In both instances the average current through the inverter varies.

On the other hand, resistances play a more sublime role in this metric. Resistances are more apparent when considering interconnect layers, one at a time, as well as the depleted channel under the gate. For each transistor, the channel resistance is given by $R_{chan} = (\beta(v_{gs} - v_{th}))^{-1}$ This quantity varies considerably during the transitions that occur in an inverter for each of the devices that form it. It is heavily dependent on XJ, $\mu$ (mobility of the majority carriers), TOX, and every variable the threshold voltage is dependent on. Therefore, TOX and XJ are again the most recurrent variables in this analysis.

Considering each layer of the structure, sheet resistance, contact resistance, current crowding resistance and ohmic resistance of the layer play important roles. Here, sheet resistance tends to be a value between 20 and 100 ohms. It is important to notice that contact resistances and ohmic resistances will also be in ranges of 1 $\Omega$ to several hundred ohms.

Nevertheless, it is easier to just consider the sheet resistance to vary as it does in the nMOS process and extract the propagation delay from a ring oscillator structure by the relationship

$$t_d = (2 \cdot f \cdot N)^{-1}$$

such that f is the operational frequency of the structure and N is the odd number of inverters that constitute the structure.

---

As far as the I-V relationships are concerned, a more detailed discussion can be found in Chapter 2.

---

With these concepts, a summary table can be found in the body of the thesis (table 5).

# APPENDIX C

*RIT nMOS Process v. 2.0 Instructions Listing*

| Step | Operation | Work Center | Spec ID/rev<br>Spec Description |
|---|---|---|---|
| 1.00 | ID01 SCRIBE | TEST | NMOS-ID01<br>NMOS ID01 |
| 2.00 | DE01 4PT PROBE | METAL | NMOS-DE01-START<br>NMOS DE01 4PT PROBE |
| 3.00 | CL01 RCA CLEAN | CLEAN | NMOS-CL01-PAD<br>NMOS CL01 PAD |
| 4.00 | OX05 DRY OXIDE | DIFF | NMOS-OX05-PAD<br>NMOS OX05 PAD |
| 5.00 | CV02 CVD NITRID | CVD | NMOS-CV02<br>NMOS CV02 NITRIDE |
| 6.00 | PH03 PHOTOLITH | PHOT2 | NMOS-PH03-DIFF<br>NMOS PH03 DIFF |
| 7.00 | ET09 NITRIDE | PLASM | NMOS-ET09-PRE-FIELD<br>NMOS ET09 NITRIDE |
| 8.00 | ET06 OXIDE ETCH | WET2 | NMOS-ET06-PRE-FIELD<br>NMOS ET06 PRE-FIELD |
| 9.00 | IM01 IMPLANT | IMPL | NMOS-IM01-FIELD<br>NMOS IM01 FIELD |
| 10.00 | ET07 STRIP | PLASM | NMOS-ET07<br>NMOS ET07 ASH RESIST |
| 11.00 | CL01 RCA CLEAN | CLEAN | NMOS-CL01-FIELD<br>NMOS CL01 FIELD |
| 12.00 | OX04 WET OXIDE | DIFF | NMOS-OX04-FIELD<br>NMOS OX04 FIELD OX |
| 13.00 | GR01 GROOVE | METAL | NMOS-GR01-FIELD<br>NMOS GR01 GROOVE |
| 14.00 | DE01 4PT PROBE | METAL | NMOS-DE01-FIELD<br>NMOS DE01 4PT PROBE |
| 15.00 | ET09 NITRIDE | PLASM | NMOS-ET09-POST-FIELD<br>NMOS ET09 POST-FIELD |
| 16.00 | ET06 OXIDE ETCH | WET2 | NMOS-ET06-POST-FIELD<br>NMOS ET06 POST-FIELD |

Process/rev . . . . : NMOS 2.0 RIT NMOS PROCE

| Step | Operation | Work Center | Spec ID/rev<br>Spec Description |
|---|---|---|---|
| 17.00 | CL01 RCA CLEAN | CLEAN | NMOS-CL01-K001<br>NMOS CL01 CLEAN K001 |
| 18.00 | OX04 WET OXIDE | DIFF | NMOS-OX04-K001<br>NMOS OX04 K001 |
| 19.00 | PH03 PHOTOLITH | PHOT2 | NMOS-PH03-IMPLANT<br>NMOS PH03 IMPLANT |
| 20.00 | IM01 IMPLANT | IMPL | NMOS-IM01-DEP-VT<br>NMOS IM01 VT ADJUST |
| 21.00 | ET07 STRIP | PLASM | NMOS-ET07-FIELD-IMP<br>NMOS ET07 ASH RESIST |
| 22.00 | IM01 IMPLANT | IMPL | NMOS-IM01-ENH-VT<br>NMOS IM01 ENH VT ADJ |
| 23.00 | ET06 OXIDE ETCH | WET2 | NMOS-ET06-K001<br>NMOS ET06 K001 ETCH |
| 24.00 | CL01 RCA CLEAN | CLEAN | NMOS-CL01-GATE<br>NMOS CL01 RCA CLEAN |
| 25.00 | OX06 DRY OXIDE | DIFF | NMOS-OX06-GATE<br>NMOS OX06 GATE |
| 26.00 | GR01 GROOVE | METAL | NMOS-GR01-GATE<br>NMOS GR01 GROOVE |
| 27.00 | DE01 4PT PROBE | METAL | NMOS-DE01-GATE<br>NMOS DE01 4PT PROBE |
| 28.00 | PH03 PHOTOLITH | PHOT2 | NMOS-PH03-BURIED<br>NMOS PH03 BURIED |
| 29.00 | ET06 OXIDE ETCH | WET2 | NMOS-ET06-BURIED<br>NMOS ET06 BURIED |
| 30.00 | ET07 STRIP | PLASM | NMOS-ET07-BURIED<br>NMOS ET07 ASH RESIST |
| 31.00 | CL01 RCA CLEAN | CLEAN | NMOS-CL01-POLY<br>NMOS CL01 POLY |
| 32.00 | CV01 CVD POLY | CVD | NMOS-CV01<br>NMOS CV01 POLY-DEP |
| 33.00 | DI04 N-TYPE DIF | DIFF | NMOS-DI04-POLY<br>NMOS DI04 POLY DOPE |
| 34.00 | DE01 4PT PROBE | METAL | NMOS-DE01-POLY<br>NMOS DE01 4PT PROBE |
| 35.00 | ET06 OXIDE ETCH | WET2 | NMOS-ET06-P-GLASS<br>NMOS ET06 P-GLASS |
| 36.00 | PH03 PHOTOLITH | PHOT2 | NMOS-PH03-POLY<br>NMOS PH03 POLY |
| 37.00 | ET08 POLY ETCH | PLASM | NMOS-ET08<br>NMOS ET08 POLY ETCH |
| 38.00 | ET07 STRIP | PLASM | NMOS-ET07<br>NMOS ET07 ASH RESIST |

Process/rev . . . . : NMOS 2.0 RIT NMOS PROCE

| Step | Operation | Work Center | Spec ID/rev<br>Spec Description |
|---|---|---|---|
| 39.00 | IM01 IMPLANT | IMPL | NMOS-IM01-DS<br>NMOS IM01 DS |
| 40.00 | CV03 CVD SPINON | CVD | NMOS-CV03<br>NMOS CV03 GLASS |
| 41.00 | PH03 PHOTOLITH | PHOT2 | NMOS-PH03-CC<br>NMOS PH03 CC |
| 42.00 | ET01 STEP ETCH | WET2 | NMOS-ET01-CC<br>NMOS ET01 ETCH CC |
| 43.00 | ET07 STRIP | PLASM | NMOS-ET07<br>NMOS ET07 ASH RESIST |
| 44.00 | GR01 GROOVE | METAL | NMOS-GR01-BPSG<br>NMOS GR01 GROOVE |
| 45.00 | DE01 4PT PROBE | METAL | NMOS-DE01-BPSG<br>NMOS DE01 4PT PROBE |
| 46.00 | ME01 AL DEPOSIT | METAL | NMOS-ME01<br>NMOS ME01 ALUMINUM |
| 47.00 | PH03 PHOTOLITH | PHOT2 | NMOS-PH03-METAL<br>NMOS PH03 METAL |
| 48.00 | ET05 AL ETCH | WET2 | NMOS-ET05<br>NMOS ET05 METAL ETCH |
| 49.00 | ET07 STRIP | PLASM | NMOS-ET07<br>NMOS ET07 ASH RESIST |
| 50.00 | SI01 SINTER | DIFF | NMOS-SI01<br>MSOS SI01 SINTER |
| 51.00 | TE01 TEST | TEST | NMOS-TE01<br>NMOS TE01 |

* * * * End of Report * * * *

# APPENDIX D

*nMOS 2.0 MESA Database Control Charts*

## *Instruction 25 data*

7-17-98
19:33:27

NMOS-OX06-GATE

| Lot number | Value |
|---|---|
| L930712 | 763 |
| L921205 | 1200 |
| L930322 | 911 |
| L921204 | 932 |
| L920605 | 552 |
| [redacted] | |
| L930222 | 1028 |
| L920703 | 1042 |
| [redacted] | |
| L920416 | 750 |
| L930401 | 635 |
| [redacted] | |

NMOS-OX06-GATE

| Lot number | Value |
|---|---|
| L920324 | 830 |
| L920123 | 1246 |
| L911207 | 1143 |
| L911209 | 1050 |
| L911203 | 1384 |
| L911207 | 854 |
| L911210 | 566 |
| [redacted] | |
| L911205 | 584 |
| L911206 | 508 |
| [redacted] | |
| L910917 | 424 |
| [redacted] | |
| L910912 | 487 |

NMOS-OX06-GATE

| Lot number | Value |
|---|---|
| L901211 | 880 |
| L901208 | 865 |
| L900919 | 780 |
| [redacted] | |
| L901211 | 1150 |

NMOS-OX06-GATE

| Lot number | Value |
|---|---|
| L921208 | 901 |
| L921006 | 517 |
| L920625 | 854 |
| L921019 | 717 |
| L920913 | 661 |
| [redacted] | |
| [redacted] | |
| L920907 | 844 |
| L920601 | 463 |
| [redacted] | |
| L920718 | 590 |
| L920602 | 566 |
| L920318 | 760 |
| [redacted] | |
| [redacted] | |
| [redacted] | |

NMOS-OX06-GATE

| Lot number | Value |
|---|---|
| L910924 | 612 |
| L910905 | 660 |
| L910621 | 900 |
| L910723 | 828 |
| L910709 | 703 |
| L910715 | 620 |
| [redacted] | |
| L910624 | 845 |
| L910430 | 845 |
| L910125 | 590 |
| L910125 | 1220 |
| L910121 | 700 |
| L910109 | 832 |
| L910121 | 1083 |
| L910105 | 1076 |
| L901210 | 930 |
| L901210 | 1150 |
| L901205 | 1141 |
| L900905 | 860 |
| L901208 | 878 |
| L900820 | 700 |
| [redacted] | |
| L900919 | 1130 |

**Any values equal to zero or >1500Å were discarded.**

## *Instruction 44 data*

NMOS-GR01-BPSG

| Lot number | Value |
|---|---|
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| L930822 | .890 |
| L920416 | 1.106 |
| [redacted] | [redacted] |
| L930222 | 2.880 |
| L930222 | 2.500 |
| L930222 | .750 |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| L930115 | 2.120 |
| L921202 | 1.330 |
| L920605 | 2.597 |
| L930702 | .808 |
| L921204 | 2.700 |
| L930115 | 1.090 |

NMOS-GR01-BPSG

| Lot number | Value |
|---|---|
| [redacted] | [redacted] |
| L921208 | 2.310 |
| L921208 | 1.120 |
| [redacted] | [redacted] |
| L921019 | 2.450 |
| L921006 | 2.300 |
| [redacted] | [redacted] |
| L921006 | 2.100 |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| L921007 | 1.276 |
| L921012 | 2.000 |
| L921019 | 1.750 |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| L920620 | 2.980 |

NMOS-GR01-BPSG

| Lot number | Value |
|---|---|
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| L920915 | 2.58 |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| [redacted]07 | 2.70 |
| L920907 | 2.90 |
| L920907 | .80 |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| L920422 | 2.40 |
| L920401 | 2.40 |
| L920713 | 2.68 |
| L920713 | 2.20 |
| L920713 | .80 |

NMOS-GR01-BPSG

| Lot number | Value |
|---|---|
| L930712 | 3.000 |
| L930712 | 2.230 |
| L930712 | 1.290 |
| L930706 | 2.020 |
| [redacted] | [redacted] |
| [redacted]10 | .030 |
| [redacted] | [redacted] |
| L921205 | .830 |
| [redacted] | [redacted] |
| L930107 | 1.400 |
| L930923 | 2.582 |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| L930822 | 2.400 |
| L921204 | .825 |
| L921202 | 1.470 |

NMOS-GR01-BPSG

| Lot number | Value |
|---|---|
| [redacted] | [redacted] |
| L920602 | 1.680 |
| L920602 | 2.700 |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| L920416 | 2.400 |
| L920410 | 2.900 |
| [redacted] | [redacted] |
| L930813 | 2.100 |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| L911220 | .200 |
| L911210 | 1.880 |
| [redacted] | [redacted] |
| L920224 | 2.780 |

NMOS-GR01-BPSG

| Lot number | Value |
|---|---|
| L920224 | 2.250 |
| L920224 | 1.100 |
| L911204 | 1.500 |
| L911202 | 1.350 |

NMOS-GR01-BPSG

| Lot number | Value |
|---|---|
| [redacted] | [redacted] |
| L930115 | 2.21 |
| L930116 | 2.19 |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| L921202 | 2.04 |
| L921202 | 1.52 |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| [redacted]921202 | .80 |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| [redacted] | [redacted] |
| L921208 | 2.80 |

Any values < .75 $\mu$m and > 3.0 $\mu$m were discarded.

NMOS-DE01-BPSG

| Lot number | Value |
|---|---|
| L930712 | 91.000 |
| L930712 | 75.000 |
| [redacted] | |
| L930706 | 94.720 |
| L930712 | 4.790 |
| [redacted] | |
| L930706 | 7.612 |
| L930610 | 8.193 |
| [redacted] | |
| L920610 | 5.930 |
| [redacted] | |
| L921204 | 5.803 |
| [redacted] | |

NMOS-DE01-BPSG

| Lot number | Value |
|---|---|
| [redacted] | |
| L920922 | 19.450 |
| [redacted] | |
| L930322 | 9.400 |
| L930323 | 8.800 |
| L930313 | 12.900 |
| L920415 | 99.270 |
| [redacted] | |
| L930222 | 6.462 |
| L920401 | 84.210 |
| [redacted] | |

NMOS-DE01-BPSG

| Lot number | Value |
|---|---|
| L930115 | 5.270 |
| L921202 | 6.604 |
| [redacted] | |
| [redacted] | 8.330 |
| [redacted] | |

NMOS-DE01-BPSG

| Lot number | Value |
|---|---|
| [redacted] | |
| L930121 | 7.170 |
| [redacted] | |
| L921202 | 43.600 |
| L930116 | 5.740 |
| L930115 | 5.740 |
| L930416 | 22.600 |
| [redacted] | |
| L930107 | 11.470 |
| [redacted] | |
| L921208 | 42.900 |
| L920923 | 94.700 |
| L921208 | 1.970 |

NMOS-DE01-BPSG

| Lot number | Value |
|---|---|
| L920915 | 10.000 |
| [redacted] | |
| L920907 | 6.190 |
| L920313 | 84.000 |

NMOS-DE01-BPSG

| Lot number | Value |
|---|---|
| [redacted] | |
| L921208 | 6.320 |
| L921205 | 5.630 |
| L921204 | 6.730 |
| L921203 | 5.458 |
| L921202 | 7.189 |
| L921201 | 6.130 |
| [redacted] | |
| L921019 | 9.064 |
| [redacted] | |
| L921006 | 98.000 |
| [redacted] | |
| L921007 | 10.960 |
| [redacted] | |

NMOS-DE01-BPSG

| Lot number | Value |
|---|---|
| [redacted] | |
| 921019 | 6.820 |
| [redacted] | |
| L921006 | 12.110 |
| L921007 | 62.900 |
| L921019 | 8.790 |
| [redacted] | |
| L921019 | 7.022 |
| L920915 | 98.100 |
| [redacted] | |
| L921012 | 8.160 |
| L921007 | 7.392 |
| L920601 | 60.860 |
| [redacted] | |

**Any values > 100 Ω/sq. and < 1 Ω/sq. were discarded.**

# APPENDIX E

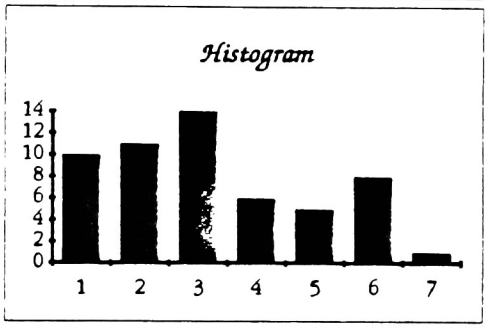
*Statistical Description & Capability Analysis of nMOS v. 2.0 Process Measurements*

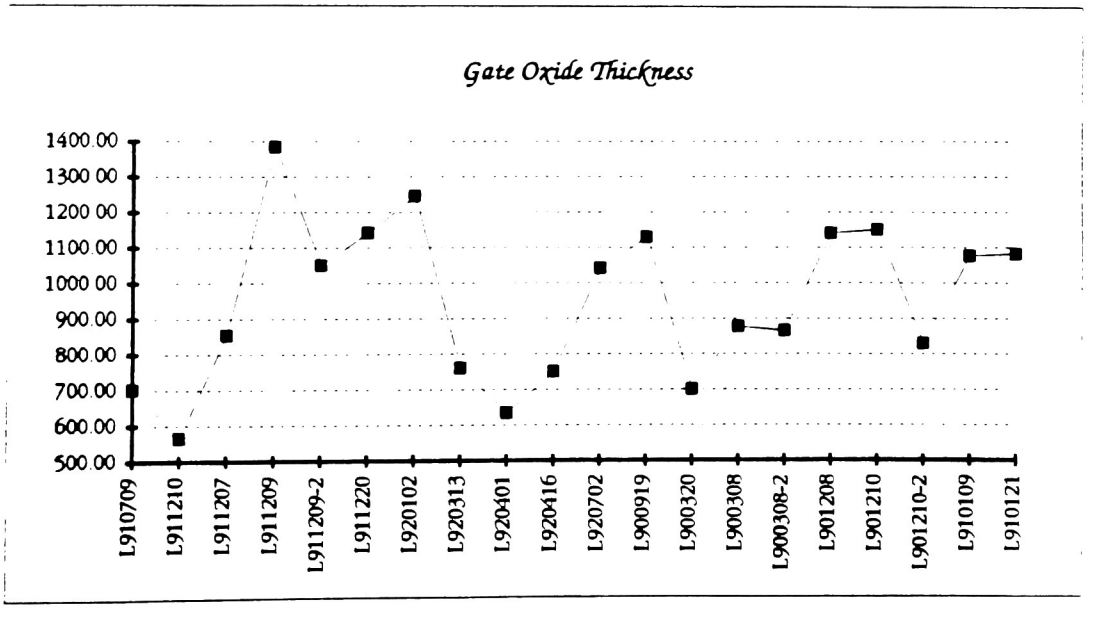
*Rochester Institute of Technology*
*Microelectronic Engineering*
*Capability Analysis (nMOS 2.0 process)*
*Step 25 - Gate Oxide Growth*

| DEFINED | |
|---|---|
| Target | 700.00 |
| USL | 850.00 |
| LSL | 550.00 |
| **STATISTICAL** | |
| Mean | 828.20 |
| Std. Dev | 226.95 |
| Count | 55 |
| Max. Val | 1384.00 |
| Min. Val | 463.00 |
| Range | 921.00 |
| **CAPABILITY** | |
| ζ | 0.39 |
| κ | 2.33 |
| Cp | 0.22 |
| k | 0.85 |
| Cpk | 0.03 |

| Lot Number | tox (Ang.) |
|---|---|
| L910709 | 703.00 |
| L911210 | 566.00 |
| L911207 | 854.00 |
| L911209 | 1384.00 |
| L911209-2 | 1050.00 |
| L911220 | 1142.00 |
| L920102 | 1246.00 |
| L920313 | 760.00 |
| L920401 | 635.00 |
| L920416 | 750.00 |
| L920702 | 1042.00 |
| L900919 | 1130.00 |
| L900320 | 700.00 |
| L900308 | 878.00 |
| L900308-2 | 865.00 |
| L901208 | 1141.00 |
| L901210 | 1150.00 |
| L901210-2 | 830.00 |
| L910109 | 1076.00 |
| L910121 | 1083.00 |

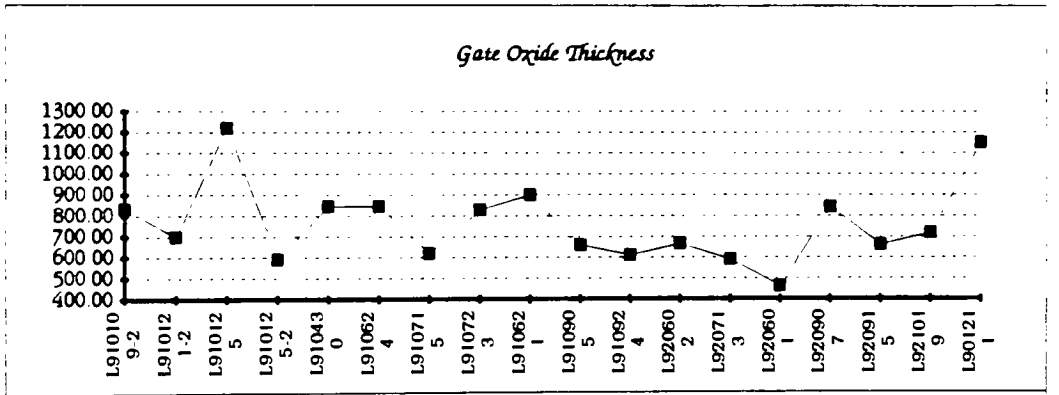
| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 10 | 463.00 | 594.57 |
| 2 | 11 | 595.57 | 726.14 |
| 3 | 14 | 727.14 | 857.71 |
| 4 | 6 | 858.71 | 989.29 |
| 5 | 5 | 990.29 | 1120.86 |
| 6 | 8 | 1121.86 | 1252.43 |
| 7 | 1 | 1253.43 | 1385.00 |

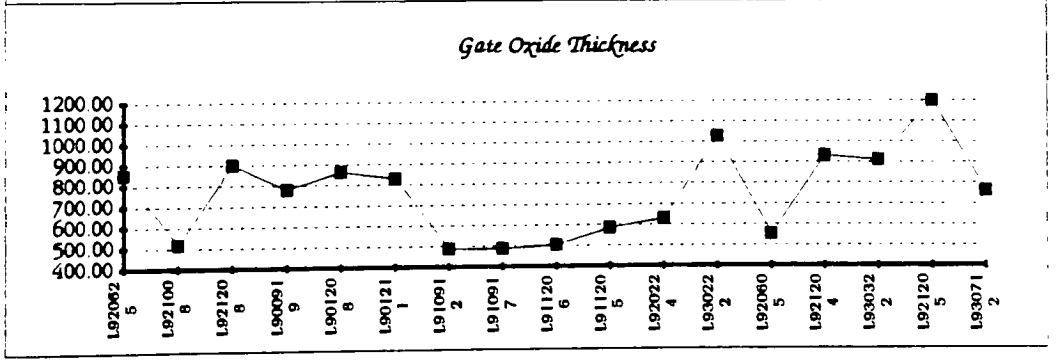


| | Lot Number | tox (Ang.) |
|---|---|---|
| | L910109-2 | 832.00 |
| | L910121-2 | 700.00 |
| | L910125 | 1220.00 |
| | L910125-2 | 590.00 |
| 55 | L910430 | 845.00 |
| 131.57 | L910624 | 845.00 |
| | L910715 | 620.00 |
| | L910723 | 828.00 |
| | L910621 | 900.00 |
| | L910905 | 660.00 |
| | L910924 | 612.00 |
| | L920602 | 666.00 |
| | L920713 | 590.00 |
| | L920601 | 463.00 |
| | L920907 | 844.00 |
| | L920915 | 661.00 |
| | L921019 | 717.00 |
| | L901211 | 1150.00 |

| Lot Number | tox (Ang.) |
|---|---|
| L920625 | 854.00 |
| L921006 | 517.00 |
| L921208 | 901.00 |
| L900919 | 780.00 |
| L901208 | 865.00 |
| L901211 | 830.00 |
| L910912 | 487.00 |
| L910917 | 486.00 |
| L911206 | 503.00 |
| L911205 | 584.00 |
| L920224 | 630.00 |
| L930222 | 1028.00 |
| L920605 | 552.00 |
| L921204 | 932.00 |
| L930322 | 911.00 |
| L921205 | 1200.00 |
| L930712 | 763.00 |

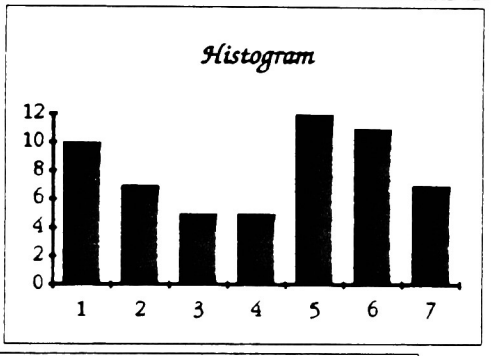


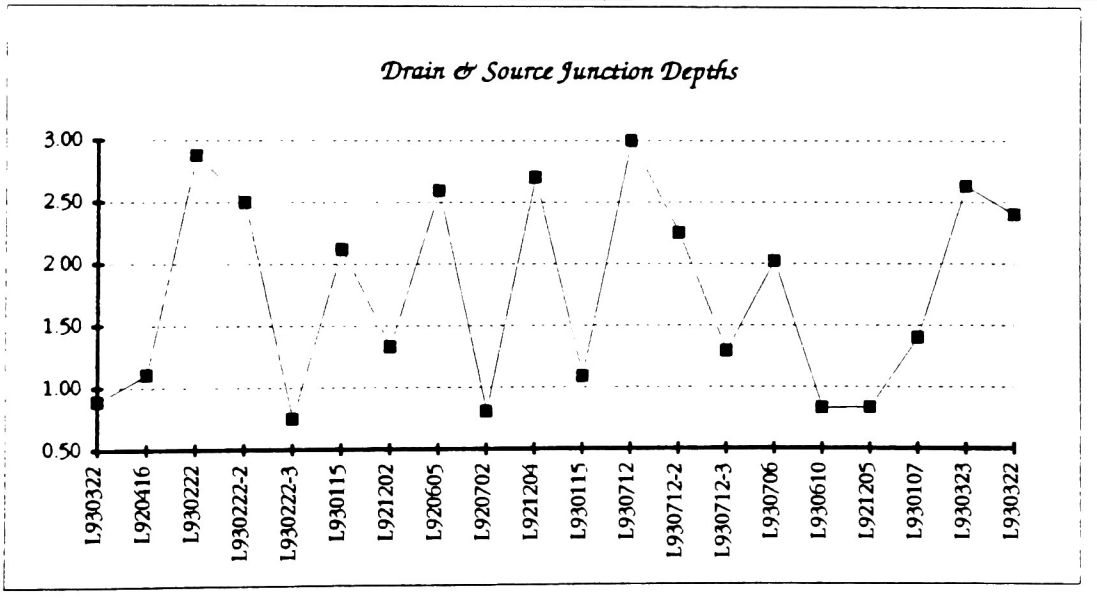



| DEFINED | |
|---|---|
| *Target* | 1.80 |
| *USL* | 2.30 |
| *LSL* | 1.30 |
| **STATISTICAL** | |
| *Mean* | 1.89 |
| *Std. Dev.* | 0.71 |
| *Count* | 57 |
| *Max. Val.* | 3.00 |
| *Min. Val.* | 0.75 |
| *Range* | 2.25 |
| **CAPABILITY** | |
| ζ | -0.27 |
| κ | 1.71 |
| *Cp* | 0.23 |
| *k* | 0.18 |
| *Cpk* | 0.19 |

| Lot Number | xj (μm) |
|---|---|
| L930322 | 0.89 |
| L920416 | 1.11 |
| L930222 | 2.88 |
| L930222-2 | 2.50 |
| L930222-3 | 0.75 |
| L930115 | 2.12 |
| L921202 | 1.33 |
| L920605 | 2.60 |
| L920702 | 0.81 |
| L921204 | 2.70 |
| L930115 | 1.09 |
| L930712 | 3.00 |
| L930712-2 | 2.25 |
| L930712-3 | 1.29 |
| L930706 | 2.02 |
| L930610 | 0.83 |
| L921205 | 0.84 |
| L930107 | 1.40 |
| L930323 | 2.63 |
| L930322 | 2.40 |

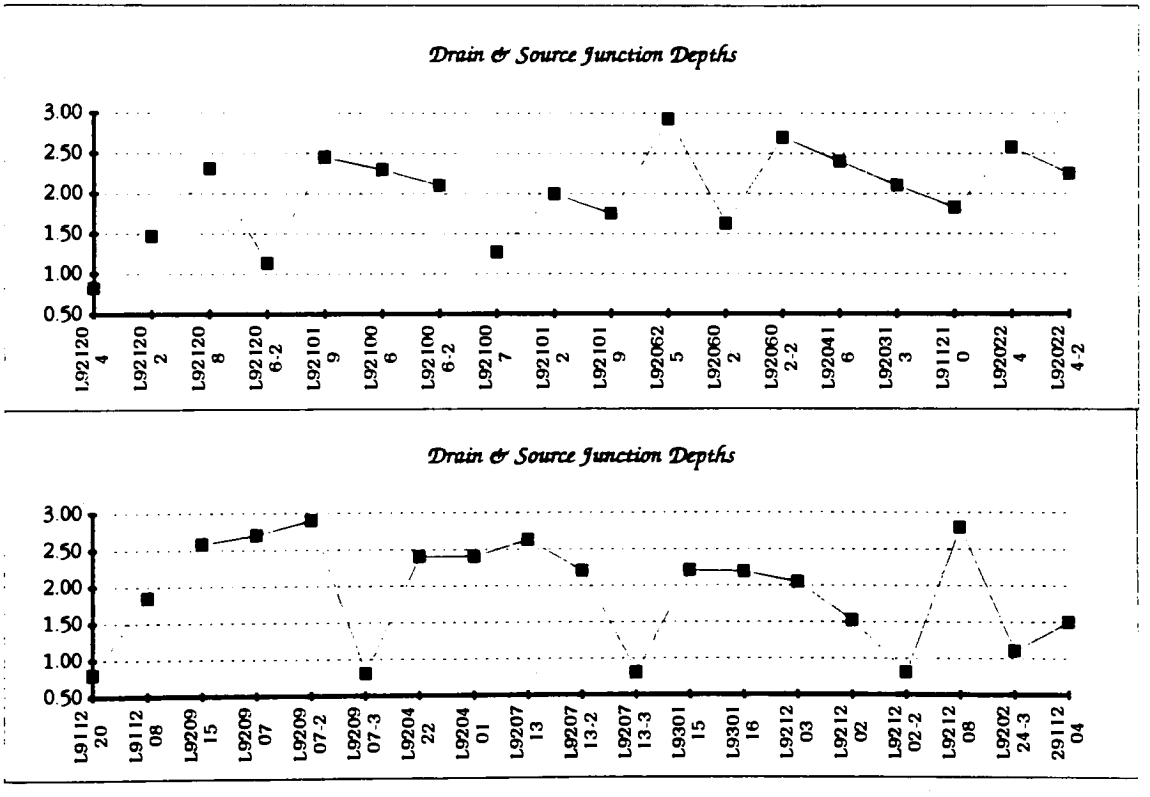
| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 10 | 0.75 | 1.07 |
| 2 | 7 | 1.08 | 1.39 |
| 3 | 5 | 1.40 | 1.71 |
| 4 | 5 | 1.72 | 2.04 |
| 5 | 12 | 2.05 | 2.36 |
| 6 | 11 | 2.37 | 2.68 |
| 7 | 7 | 2.69 | 3.01 |



| Lot Number | xj (µm) |
|---|---|
| L921204 | 0.83 |
| L921202 | 1.47 |
| L921208 | 2.31 |
| L921208-2 | 1.13 |
| L921019 | 2.45 |
| L921006 | 2.30 |
| L921006-2 | 2.10 |
| 57 L921007 | 1.28 |
| 0.32 L921012 | 2.00 |
| L921019 | 1.75 |
| L920625 | 2.93 |
| L920602 | 1.63 |
| L920602-2 | 2.70 |
| L920416 | 2.40 |
| L920313 | 2.10 |
| L911210 | 1.83 |
| L920224 | 2.58 |
| L920224-2 | 2.25 |

| Lot Number | xj (µm) |
|---|---|
| L911220 | 0.80 |
| L911208 | 1.85 |
| L920915 | 2.58 |
| L920907 | 2.70 |
| L920907-2 | 2.90 |
| L920907-3 | 0.80 |
| L920422 | 2.40 |
| L920401 | 2.40 |
| L920713 | 2.63 |
| L920713-2 | 2.20 |
| L920713-3 | 0.81 |
| L930115 | 2.21 |
| L930116 | 2.19 |
| L921203 | 2.05 |
| L921202 | 1.52 |
| L921202-2 | 0.81 |
| L921208 | 2.80 |
| L920224-3 | 1.10 |
| 2911204 | 1.50 |



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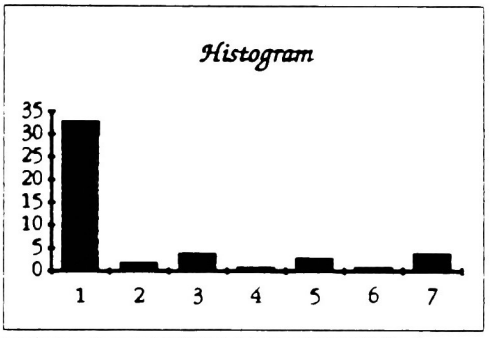
*Capability Analysis (nMOS 2.0 process)*
*Step 45 - Diffusion Sheet Resistance*

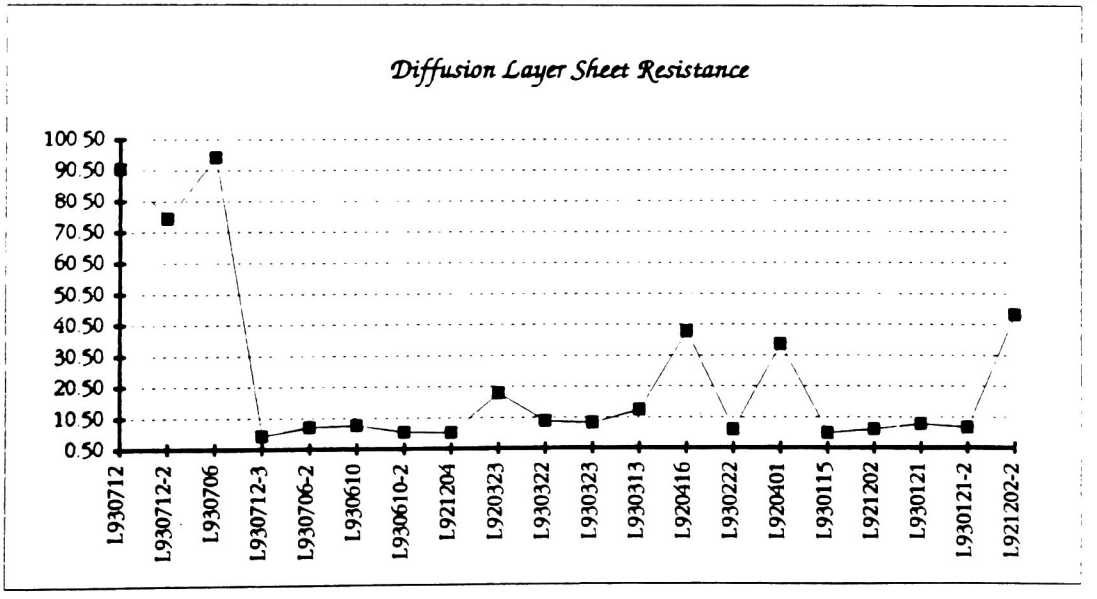
| DEFINED | |
|---|---|
| *Target* | 50.00 |
| *USL* | 90.00 |
| *LSL* | 10.00 |
| **STATISTICAL** | |
| *Mean* | 23.31 |
| *Std. Dev* | 27.85 |
| *Count* | 48 |
| *Max. Val.* | 98.10 |
| *Min. Val.* | 1.97 |
| *Range* | 96.13 |
| **CAPABILITY** | |
| $\zeta$ | 1.56 |
| $\kappa$ | 4.08 |
| *Cp* | 0.48 |
| *k* | 0.67 |
| *Cpk* | 0.16 |

| Lot Number | Rs (Ω) |
|---|---|
| L930712 | 91.00 |
| L930712-2 | 75.00 |
| L930706 | 94.72 |
| L930712-3 | 4.78 |
| L930706-2 | 7.61 |
| L930610 | 8.19 |
| L930610-2 | 5.93 |
| L921204 | 5.80 |
| L920323 | 18.46 |
| L930322 | 9.40 |
| L930323 | 8.80 |
| L930313 | 12.90 |
| L920416 | 38.27 |
| L930222 | 6.46 |
| L920401 | 34.21 |
| L930115 | 5.37 |
| L921202 | 6.60 |
| L930121 | 8.33 |
| L930121-2 | 7.17 |
| L921202-2 | 43.60 |

Histogram

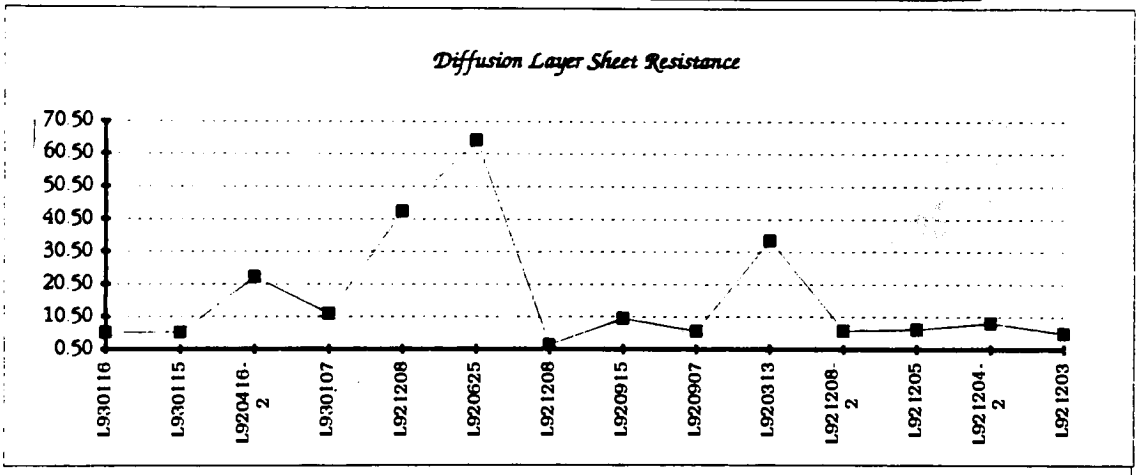
| Group | Count | MIN | MAX |
|---|---|---|---|
| 1 | 33 | 1.97 | 15.70 |
| 2 | 2 | 16.70 | 29.44 |
| 3 | 4 | 30.44 | 43.17 |
| 4 | 1 | 44.17 | 56.90 |
| 5 | 3 | 57.90 | 70.63 |
| 6 | 1 | 71.63 | 84.37 |
| 7 | 4 | 85.37 | 99.10 |

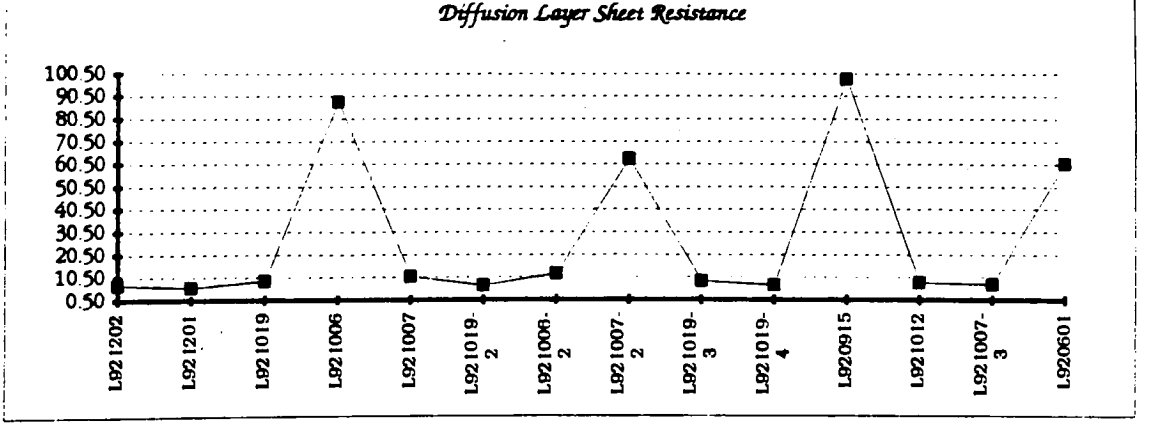


| Lot Number | Rs (Ω) |
|---|---|
| L930116 | 5.74 |
| L930115 | 5.74 |
| L920416-2 | 22.80 |
| L930107 | 11.47 |
| L921208 | 42.90 |
| L920625 | 64.70 |
| L921208 | 1.97 |
| L920915 | 10.00 |
| L920907 | 6.19 |
| L920313 | 34.00 |
| L921208-2 | 6.32 |
| L921205 | 6.63 |
| L921204-2 | 8.73 |
| L921203 | 5.46 |

| Lot Number | Rs (Ω) |
|---|---|
| L921202 | 7.19 |
| L921201 | 6.13 |
| L921019 | 9.06 |
| L921006 | 88.00 |
| L921007 | 10.96 |
| L921019-2 | 6.82 |
| L921006-2 | 12.11 |
| L921007-2 | 62.90 |
| L921019-3 | 8.79 |
| L921019-4 | 7.02 |
| L920915 | 98.10 |
| L921012 | 8.16 |
| L921007-3 | 7.39 |
| L920601 | 60.86 |



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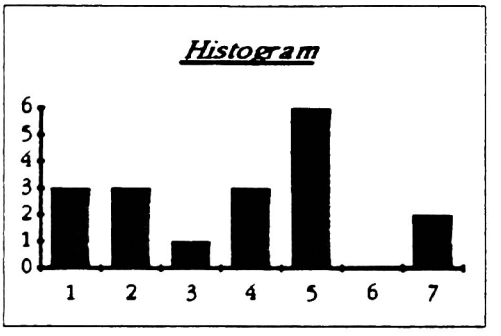
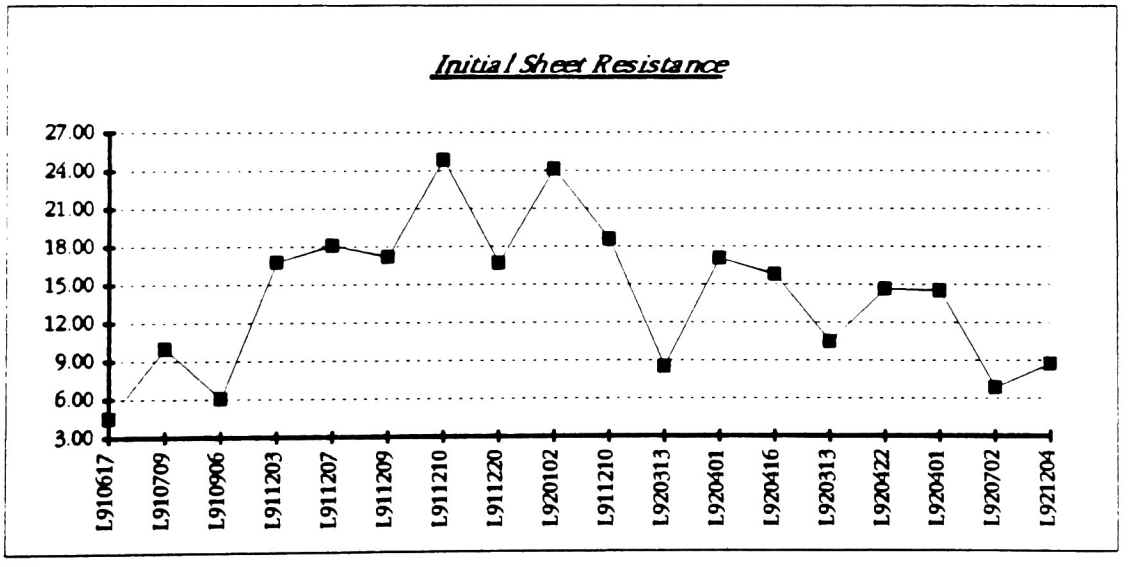
*Capability Analysis (nMOS 2.0 process)*
*Step 2 - Starting Sheet Resistance*

| DEFINED | |
|---|---|
| *Target* | |
| *USL* | |
| *LSL* | |
| *UCL* | |
| *LCL* | |
| **STATISTICAL** | |
| *Mean* | 14.08 |
| *Std. Dev.* | 5.87 |
| *Count* | 18 |
| *Max. Val* | 24.86 |
| *Min. Val* | 4.52 |
| *Range* | 20.34 |
| **CAPABILITY** | |
| *Cp* | 0.00 |
| *k* | #DIV/0! |
| *Cpk* | 0.80 |

| Lot Number | Rs (Ω/sq.) |
|---|---|
| L910617 | 4.52 |
| L910709 | 10.00 |
| L910906 | 6.06 |
| L911203 | 16.78 |
| L911207 | 18.08 |
| L911209 | 17.20 |
| L911210 | 24.86 |
| L911220 | 16.67 |
| L920102 | 24.12 |
| L911210 | 18.56 |
| L920313 | 8.50 |
| L920401 | 17.05 |
| L920416 | 15.80 |
| L920313 | 10.49 |
| L920422 | 14.64 |
| L920401 | 14.50 |
| L920702 | 6.87 |
| L921204 | 8.73 |

| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 3 | 4.52 | 7.43 |
| 2 | 3 | 7.44 | 10.33 |
| 3 | 1 | 10.34 | 13.24 |
| 4 | 3 | 13.25 | 16.14 |
| 5 | 6 | 16.15 | 19.05 |
| 6 | 0 | 19.06 | 21.95 |
| 7 | 2 | 21.96 | 25.86 |



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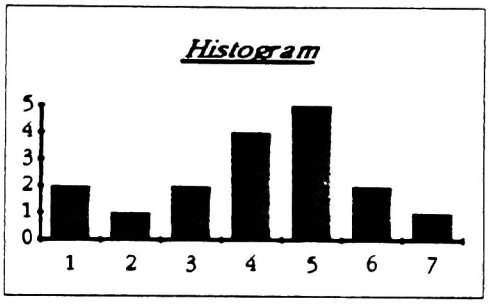
*Capability Analysis (nMOS 2.0 process)*
*Step 4 - Pad Oxide Thickness*

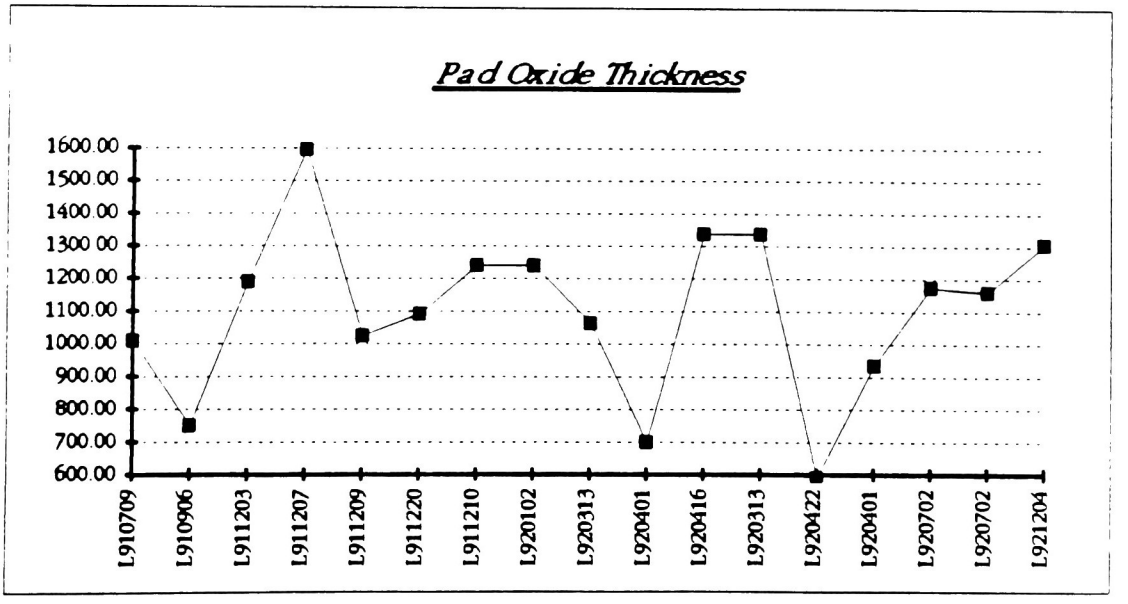
| DEFINED | |
|---|---|
| *Target* | 1000.00 |
| *USL* | 1200.00 |
| *LSL* | 800.00 |
| *UCL* | |
| *LCL* | |
| **STATISTICAL** | |
| *Mean* | 1102.94 |
| *Std. Dev.* | 255.32 |
| *Count* | 17 |
| *Max. Val.* | 1596.00 |
| *Min. Val.* | 590.00 |
| *Range* | 1006.00 |
| **CAPABILITY** | |
| *Cp* | 0.26 |
| *k* | 0.51 |
| *Cpk* | 0.13 |

| Lot Number | Pox (Ang) |
|---|---|
| L910709 | 1010.00 |
| L910906 | 750.00 |
| L911203 | 1190.00 |
| L911207 | 1596.00 |
| L911209 | 1025.00 |
| L911220 | 1092.00 |
| L911210 | 1241.00 |
| L920102 | 1241.00 |
| L920313 | 1064.00 |
| L920401 | 700.00 |
| L920416 | 1337.00 |
| L920313 | 1337.00 |
| L920422 | 590.00 |
| L920401 | 935.00 |
| L920702 | 1175.00 |
| L920702 | 1160.00 |
| L921204 | 1307.00 |

**Histogram**

| Group | Count | MIN | MAX |
|---|---|---|---|
| 1 | 2 | 590.00 | 733.71 |
| 2 | 1 | 734.71 | 877.43 |
| 3 | 2 | 878.43 | 1021.14 |
| 4 | 4 | 1022.14 | 1164.86 |
| 5 | 5 | 1165.86 | 1308.57 |
| 6 | 2 | 1309.57 | 1452.29 |
| 7 | 1 | 1453.29 | 1597.00 |



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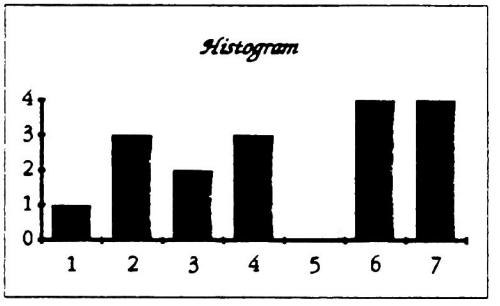
*Capability Analysis (nMOS 2.0 process)*
*Step 5 - CVD Nitride*

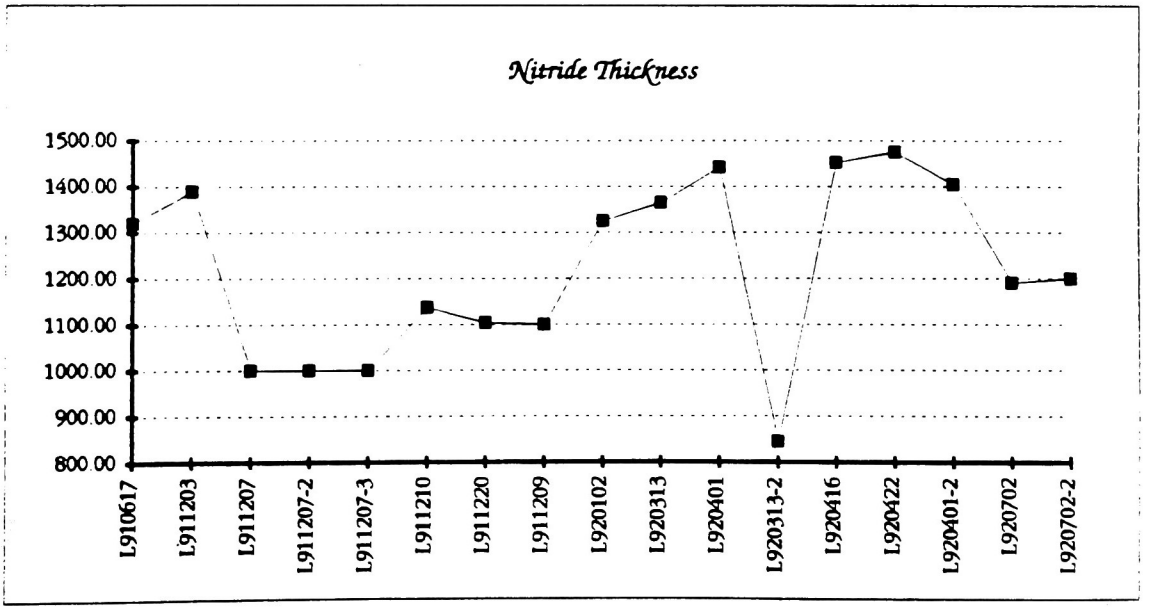
| DEFINED | |
|---|---|
| Target | |
| USL | |
| LSL | |
| UCL | |
| LCL | |
| **STATISTICAL** | |
| Mean | 1220.59 |
| Std. Dev. | 192.98 |
| Count | 17 |
| Max. Val. | 1475.00 |
| Min. Val. | 845.00 |
| Range | 630.00 |
| **CAPABILITY** | |
| Cp | 0.00 |
| k | #DIV/0! |
| Cpk | 2.11 |

| Lot Number | Xnt (Ang) |
|---|---|
| L910617 | 1320.00 |
| L911203 | 1390.00 |
| L911207 | 1000.00 |
| L911207-2 | 1000.00 |
| L911207-3 | 1000.00 |
| L911210 | 1137.00 |
| L911220 | 1103.00 |
| L911209 | 1100.00 |
| L920102 | 1325.00 |
| L920313 | 1365.00 |
| L920401 | 1442.00 |
| L920313-2 | 845.00 |
| L920416 | 1453.00 |
| L920422 | 1475.00 |
| L920401-2 | 1405.00 |
| L920702 | 1190.00 |
| L920702-2 | 1200.00 |

**Histogram**

| Group | Count | MIN | MAX |
|---|---|---|---|
| 1 | 1 | 845.00 | 935.00 |
| 2 | 3 | 936.00 | 1025.00 |
| 3 | 2 | 1026.00 | 1115.00 |
| 4 | 3 | 1116.00 | 1205.00 |
| 5 | 0 | 1206.00 | 1295.00 |
| 6 | 4 | 1296.00 | 1385.00 |
| 7 | 4 | 1386.00 | 1476.00 |



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*Microelectronic Engineering*
*Capability Analysis (nMOS 2.0 process)*
*Step 7 - Nitride Etch Rate*

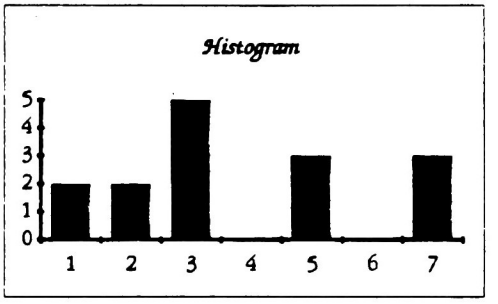
| DEFINED | |
|---|---|
| *Target* | |
| *USL* | |
| *LSL* | |
| *UCL* | |
| *LCL* | |

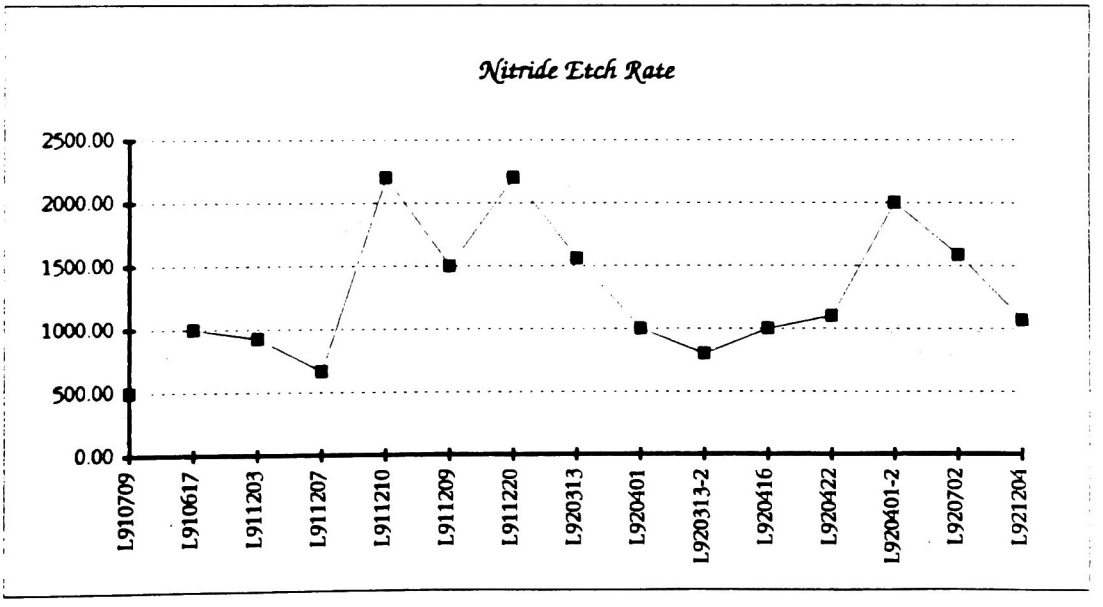
| STATISTICAL | |
|---|---|
| *Mean* | 1273.80 |
| *Std. Dev.* | 540.07 |
| *Count* | 15 |
| *Max. Val.* | 2200.00 |
| *Min. Val.* | 500.00 |
| *Range* | 1700.00 |

| CAPABILITY | |
|---|---|
| *Cp* | 0.00 |
| *k* | #DIV/0! |
| *Cpk* | 0.79 |

| Lot Number | Rate (Ang/min) |
|---|---|
| L910709 | 500.00 |
| L910617 | 1000.00 |
| L911203 | 926.00 |
| L911207 | 667.00 |
| L911210 | 2200.00 |
| L911209 | 1500.00 |
| L911220 | 2200.00 |
| L920313 | 1560.00 |
| L920401 | 1000.00 |
| L920313-2 | 800.00 |
| L920416 | 1000.00 |
| L920422 | 1100.00 |
| L920401-2 | 2000.00 |
| L920702 | 1586.00 |
| L921204 | 1068.00 |

| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 2 | 500.00 | 742.86 |
| 2 | 2 | 743.86 | 985.71 |
| 3 | 5 | 986.71 | 1228.57 |
| 4 | 0 | 1229.57 | 1471.43 |
| 5 | 3 | 1472.43 | 1714.29 |
| 6 | 0 | 1715.29 | 1957.14 |
| 7 | 3 | 1958.14 | 2201.00 |



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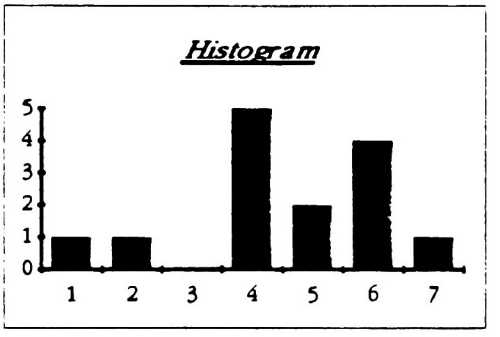
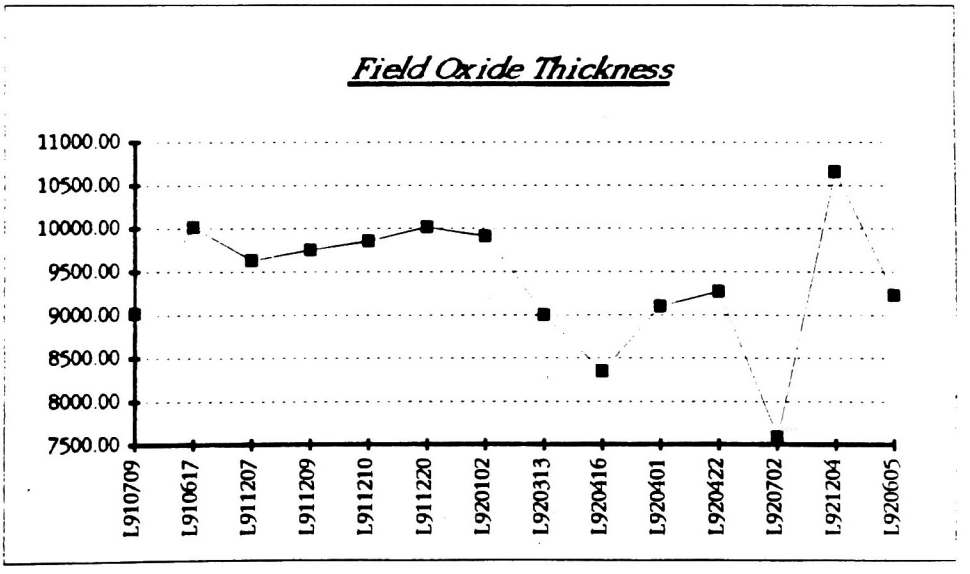
*Capability Analysis (nMOS 2.0 process)*
*Step 12 - Field Oxide Thickness*

| DEFINED | |
|---|---|
| Target | 10500.00 |
| USL | 12000.00 |
| LSL | 9000.00 |
| UCL | |
| LCL | |
| **STATISTICAL** | |
| Mean | 9386.14 |
| Std. Dev. | 776.02 |
| Count | 14 |
| Max. Val. | 10660.00 |
| Min. Val. | 7587.00 |
| Range | 3073.00 |
| **CAPABILITY** | |
| Cp | 0.64 |
| k | 0.74 |
| Cpk | 0.17 |

| Lot Number | Xox (Ang) |
|---|---|
| L910709 | 9020.00 |
| L910617 | 10020.00 |
| L911207 | 9630.00 |
| L911209 | 9754.00 |
| L911210 | 9855.00 |
| L911220 | 10020.00 |
| L920102 | 9910.00 |
| L920313 | 9000.00 |
| L920416 | 8350.00 |
| L920401 | 9100.00 |
| L920422 | 9270.00 |
| L920702 | 7587.00 |
| L921204 | 10660.00 |
| L920605 | 9230.00 |

| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 1 | 7587.00 | 8026.00 |
| 2 | 1 | 8027.00 | 8465.00 |
| 3 | 0 | 8466.00 | 8904.00 |
| 4 | 5 | 8905.00 | 9343.00 |
| 5 | 2 | 9344.00 | 9782.00 |
| 6 | 4 | 9783.00 | 10221.00 |
| 7 | 1 | 10222.00 | 10661.00 |



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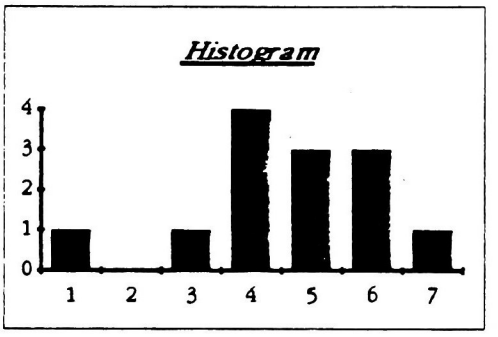
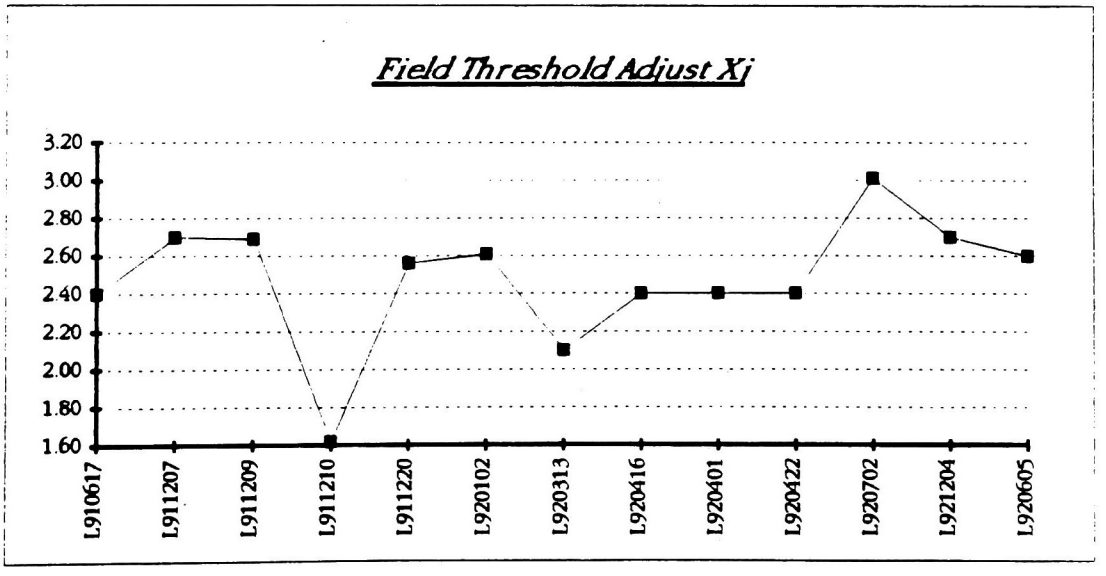
*Capability Analysis (nMOS 2.0 process)*
*Step 13 - Field Threshold Adjust Junction Depth*

| DEFINED | |
|---|---|
| *Target* | |
| *USL* | |
| *LSL* | |
| *UCL* | |
| *LCL* | |
| **STATISTICAL** | |
| *Mean* | 2.48 |
| *Std. Dev.* | 0.34 |
| *Count* | 13 |
| *Max. Val.* | 3.01 |
| *Min. Val.* | 1.62 |
| *Range* | 1.39 |
| **CAPABILITY** | |
| *Cp* | 0.00 |
| *k* | #DIV/0! |
| *Cpk* | 2.44 |

| Lot Number | FTA Xj (µm) |
|---|---|
| L910617 | 2.40 |
| L911207 | 2.70 |
| L911209 | 2.69 |
| L911210 | 1.62 |
| L911220 | 2.56 |
| L920102 | 2.61 |
| L920313 | 2.10 |
| L920416 | 2.40 |
| L920401 | 2.40 |
| L920422 | 2.40 |
| L920702 | 3.01 |
| L921204 | 2.70 |
| L920605 | 2.60 |

| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 1 | 1.62 | 1.82 |
| 2 | 0 | 1.92 | 2.02 |
| 3 | 1 | 2.12 | 2.22 |
| 4 | 4 | 2.32 | 2.41 |
| 5 | 3 | 2.51 | 2.61 |
| 6 | 3 | 2.71 | 2.81 |
| 7 | 1 | 2.91 | 3.11 |



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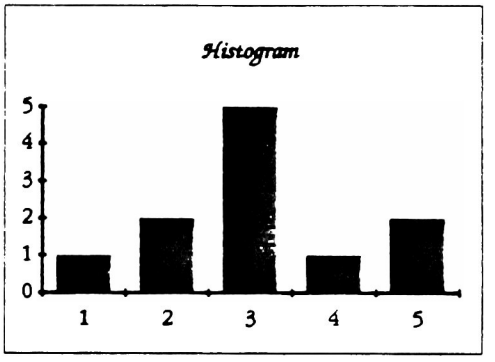
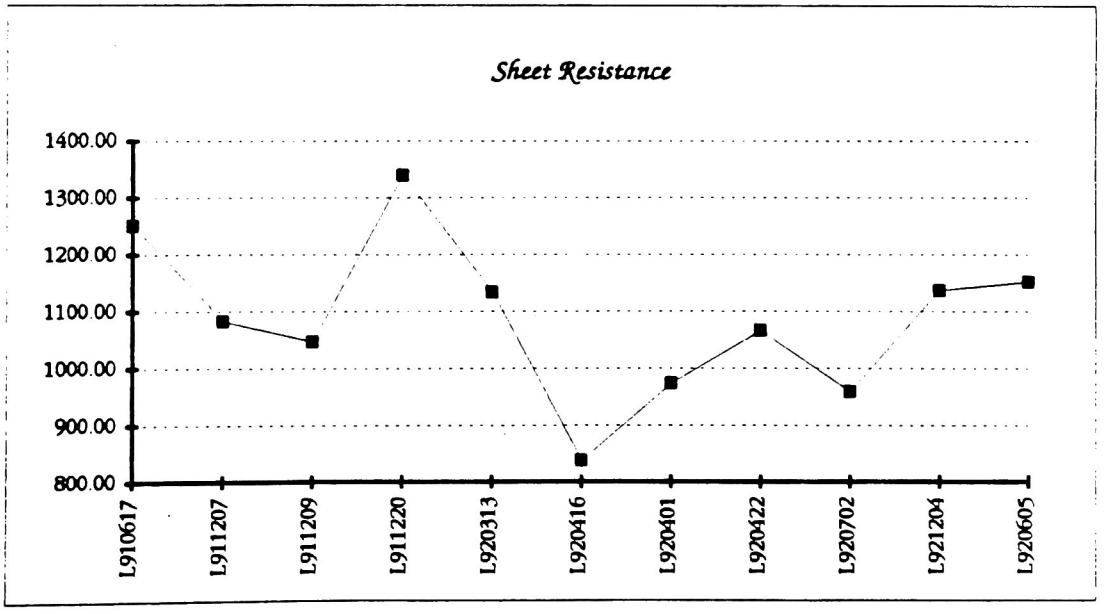
*Capability Analysis (nMOS 2.0 process)*
*Step 14 - Sheet Resistance*

| Lot Number | Rs (Ω/sq.) |
|---|---|
| L910617 | 1252.00 |
| L911207 | 1083.00 |
| L911209 | 1047.00 |
| L911220 | 1340.00 |
| L920313 | 1134.00 |
| L920416 | 838.00 |
| L920401 | 974.00 |
| L920422 | 1066.00 |
| L920702 | 959.00 |
| L921204 | 1137.00 |
| L920605 | 1152.00 |

| DEFINED | |
|---|---|
| *Target* | |
| *USL* | |
| *LSL* | |
| *UCL* | |
| *LCL* | |
| **STATISTICAL** | |
| *Mean* | 1089.27 |
| *Std. Dev.* | 139.04 |
| *Count* | 11 |
| *Max. Val.* | 1340.00 |
| *Min. Val.* | 838.00 |
| *Range* | 502.00 |
| **CAPABILITY** | |
| *Cp* | 0.00 |
| *k* | #DIV/0! |
| *Cpk* | 2.61 |

| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 1 | 838.00 | 938.40 |
| 2 | 2 | 939.40 | 1038.80 |
| 3 | 5 | 1039.80 | 1139.20 |
| 4 | 1 | 1140.20 | 1239.60 |
| 5 | 2 | 1240.60 | 1341.00 |

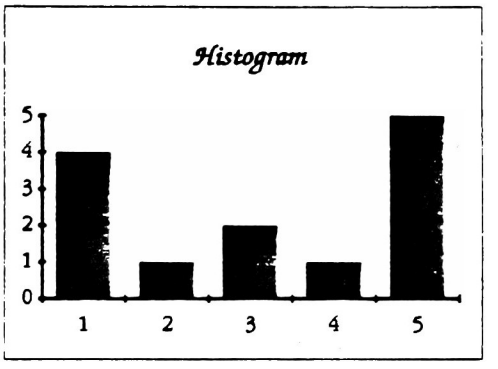


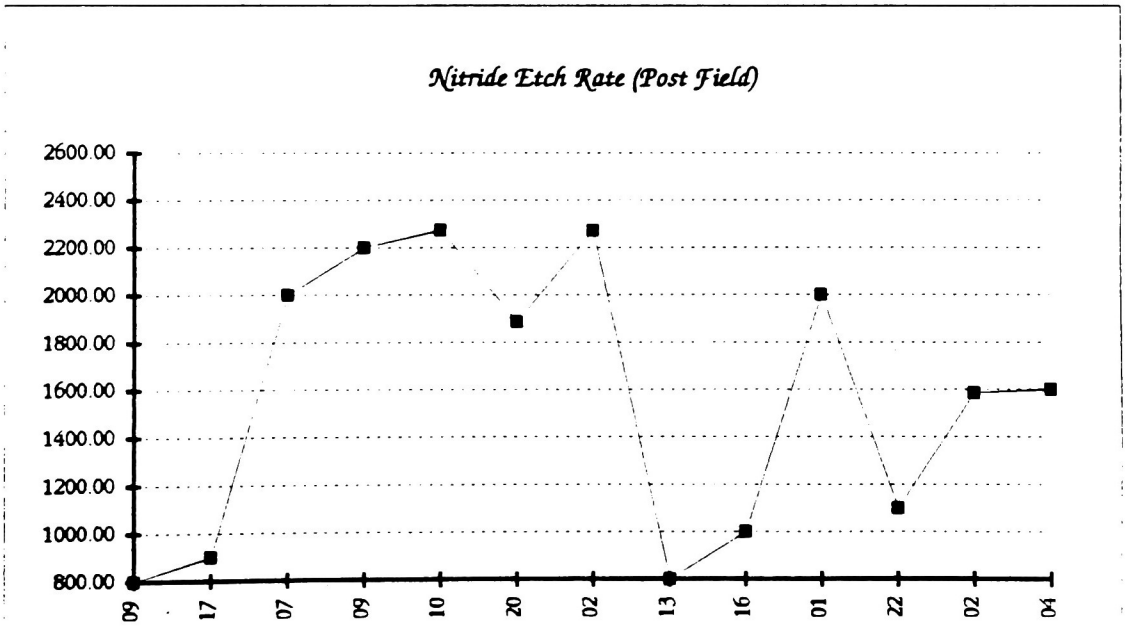



| DEFINED | |
|---|---|
| *Target* | |
| *USL* | |
| *LSL* | |
| *UCL* | |
| *LCL* | |
| **STATISTICAL** | |
| *Mean* | 1570.46 |
| *Std. Dev.* | 579.84 |
| *Count* | 13 |
| *Max. Val.* | 2274.00 |
| *Min. Val.* | 800.00 |
| *Range* | 1474.00 |
| **CAPABILITY** | |
| *Cp* | 0.00 |
| *k* | #DIV/0! |
| *Cpk* | 0.90 |

| Lot Number | Rate (A/min.) |
|---|---|
| L910709 | 800.00 |
| L910617 | 900.00 |
| L911207 | 2000.00 |
| L911209 | 2200.00 |
| L911210 | 2274.00 |
| L911220 | 1885.00 |
| L920102 | 2271.00 |
| L920313 | 800.00 |
| L920416 | 1000.00 |
| L920401 | 2000.00 |
| L920422 | 1100.00 |
| L920702 | 1586.00 |
| L921204 | 1600.00 |

| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 4 | 800.00 | 1094.80 |
| 2 | 1 | 1095.80 | 1389.60 |
| 3 | 2 | 1390.60 | 1684.40 |
| 4 | 1 | 1685.40 | 1979.20 |
| 5 | 5 | 1980.20 | 2275.00 |



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*Microelectronic Engineering*
*Capability Analysis (nMOS 2.0 process)*
*Step 18 - Kooi Oxide Growth*

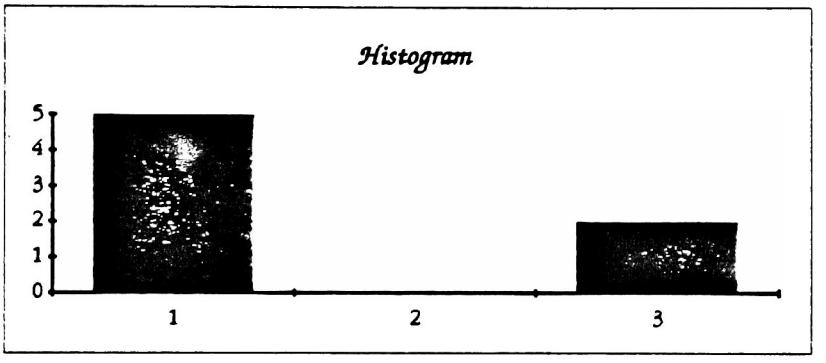
| DEFINED | |
|---|---|
| *Target* | |
| *USL* | |
| *LSL* | |
| *UCL* | |
| *LCL* | |

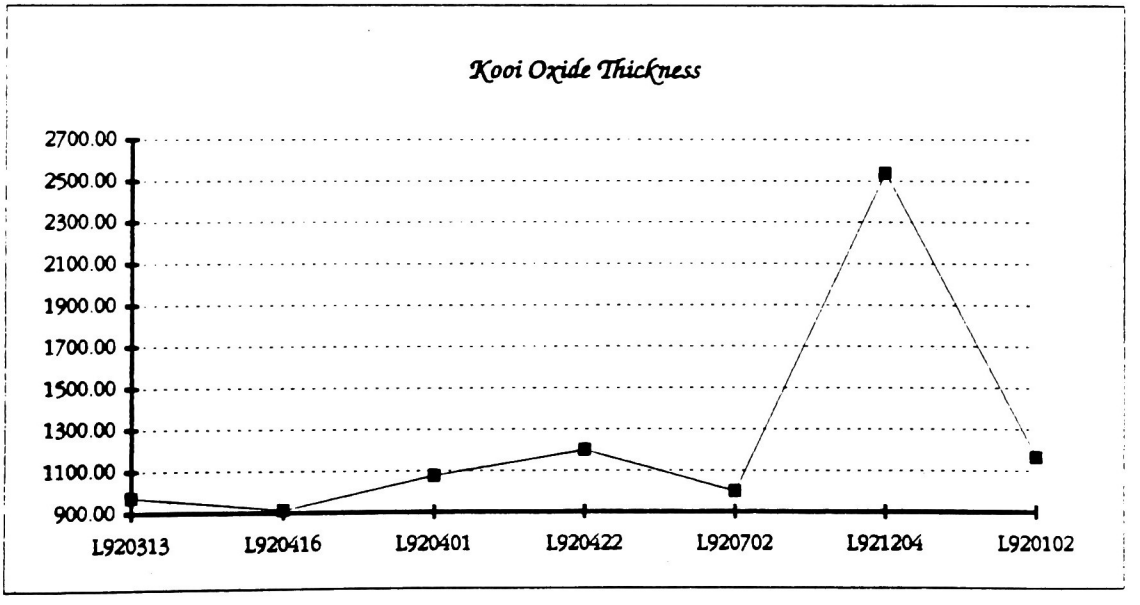
| STATISTICAL | |
|---|---|
| *Mean* | 1267.00 |
| *Std. Dev.* | 569.33 |
| *Count* | 7 |
| *Max. Val.* | 2537.00 |
| *Min. Val.* | 914.00 |
| *Range* | 1623.00 |

| CAPABILITY | |
|---|---|
| *Cp* | 0.00 |
| *k* | #DIV/0! |
| *Cpk* | 0.74 |

| Lot Number | Kox (Ang.) |
|---|---|
| L920313 | 975.00 |
| L920416 | 914.00 |
| L920401 | 1077.00 |
| L920422 | 1200.00 |
| L920702 | 1000.00 |
| L921204 | 2537.00 |
| L920102 | 1166.00 |

| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 5 | 914.00 | 1455.00 |
| 2 | 0 | 1456.00 | 1996.00 |
| 3 | 2 | 1997.00 | 2538.00 |



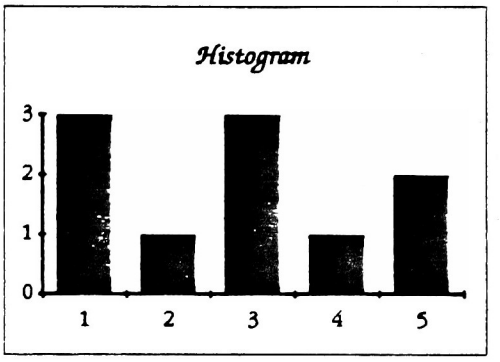



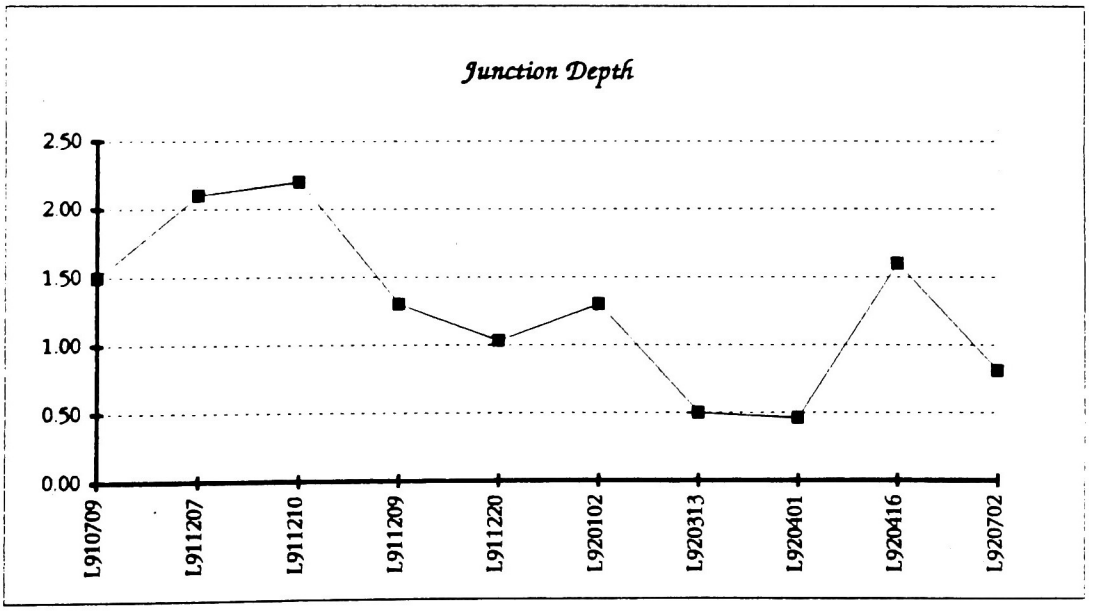
*Rochester Institute of Technology*
*Microelectronic Engineering*
*Capability Analysis (nMOS 2.0 process)*
*Step 26 - Junction Depth*

| DEFINED | |
|---|---|
| *Target* | |
| *USL* | |
| *LSL* | |
| *UCL* | |
| *LCL* | |
| **STATISTICAL** | |
| *Mean* | 1.28 |
| *Std. Dev.* | 0.60 |
| *Count* | 10 |
| *Max. Val.* | 2.20 |
| *Min. Val.* | 0.46 |
| *Range* | 1.74 |
| **CAPABILITY** | |
| *Cp* | 0.00 |
| *k* | #DIV/0! |
| *Cpk* | 0.71 |

| Lot Number | Xj (microns) |
|---|---|
| L910709 | 1.50 |
| L911207 | 2.10 |
| L911210 | 2.20 |
| L911209 | 1.30 |
| L911220 | 1.03 |
| L920102 | 1.30 |
| L920313 | 0.50 |
| L920401 | 0.46 |
| L920416 | 1.60 |
| L920702 | 0.81 |

| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 3 | 0.46 | 0.81 |
| 2 | 1 | 0.91 | 1.16 |
| 3 | 3 | 1.26 | 1.50 |
| 4 | 1 | 1.60 | 1.85 |
| 5 | 2 | 1.95 | 2.30 |



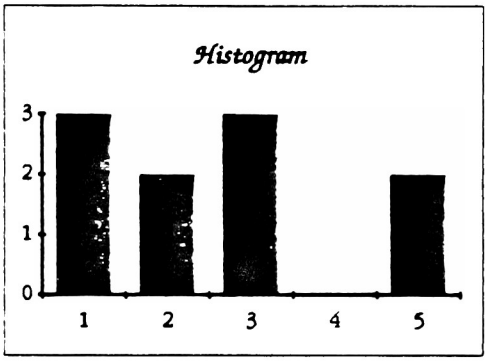



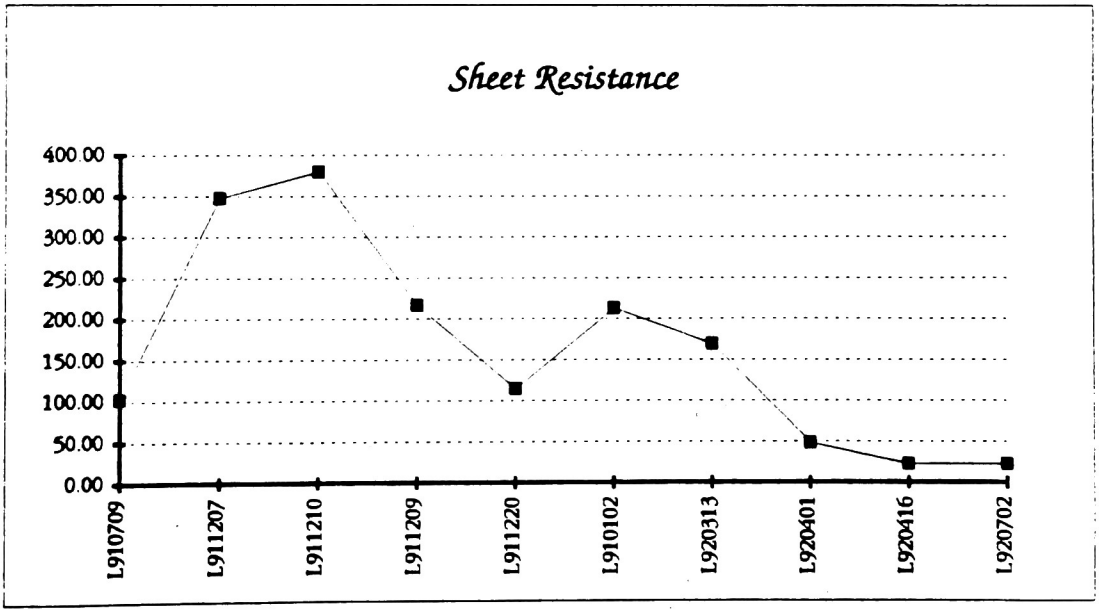
*Rochester Institute of Technology*
*Microelectronic Engineering*
*Capability Analysis (nMOS 2.0 process)*
*Step 27 - Gate Sheet Resistance*

| DEFINED | |
|---|---|
| *Target* | |
| *USL* | |
| *LSL* | |
| *UCL* | |
| *LCL* | |
| **STATISTICAL** | |
| *Mean* | 163.85 |
| *Std. Dev.* | 127.04 |
| *Count* | 10 |
| *Max. Val.* | 380.20 |
| *Min. Val.* | 22.47 |
| *Range* | 357.73 |
| **CAPABILITY** | |
| *Cp* | 0.00 |
| *k* | #DIV/0! |
| *Cpk* | 0.43 |

| Lot Number | Rs (Ω/sq.) |
|---|---|
| L910709 | 103.00 |
| L911207 | 348.00 |
| L911210 | 380.20 |
| L911209 | 216.60 |
| L911220 | 114.50 |
| L910102 | 212.90 |
| L920313 | 169.40 |
| L920401 | 48.60 |
| L920416 | 22.80 |
| L920702 | 22.47 |

| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 3 | 22.47 | 94.02 |
| 2 | 2 | 95.02 | 165.56 |
| 3 | 3 | 166.56 | 237.11 |
| 4 | 0 | 238.11 | 308.65 |
| 5 | 2 | 309.65 | 381.20 |



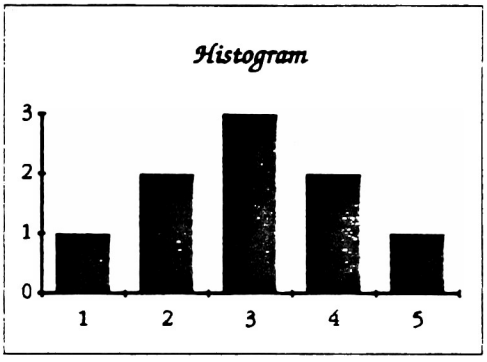



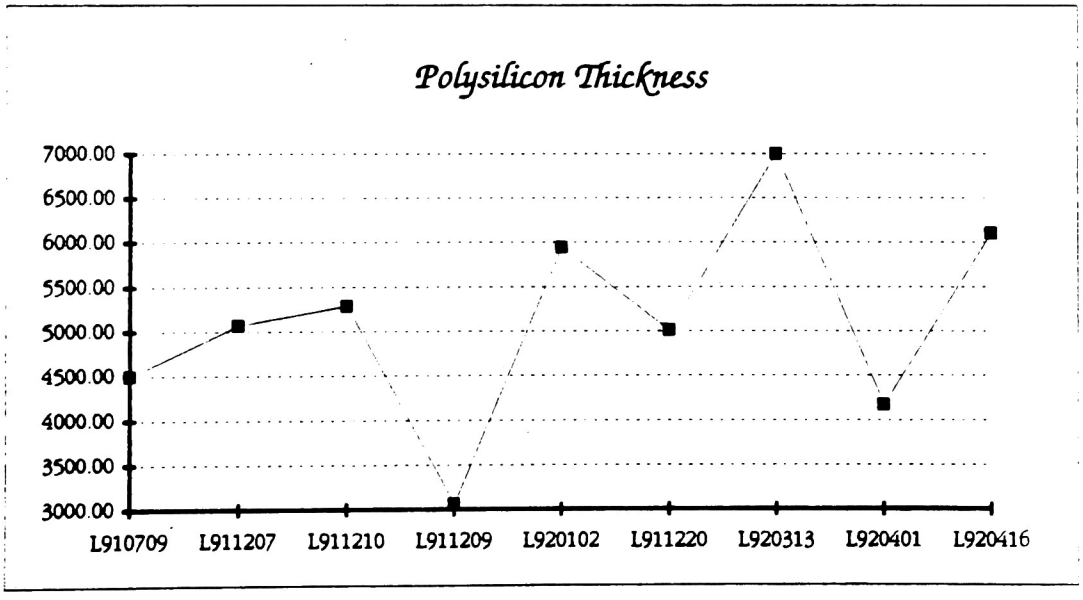
*Rochester Institute of Technology*
*Microelectronic Engineering*
*Capability Analysis (nMOS 2.0 process)*
*Step 32 - Polysilicon CVD*

| DEFINED | |
|---|---|
| *Target* | |
| *USL* | |
| *LSL* | |
| *UCL* | |
| *LCL* | |
| **STATISTICAL** | |
| *Mean* | 5127.00 |
| *Std. Dev.* | 1158.55 |
| *Count* | 9 |
| *Max. Val.* | 7000.00 |
| *Min. Val.* | 3060.00 |
| *Range* | 3940.00 |
| **CAPABILITY** | |
| *Cp* | 0.00 |
| *k* | #DIV/0! |
| *Cpk* | 1.48 |

| Lot Number | Poly (Ang.) |
|---|---|
| L910709 | 4500.00 |
| L911207 | 5070.00 |
| L911210 | 5285.00 |
| L911209 | 3060.00 |
| L920102 | 5943.00 |
| L911220 | 5012.00 |
| L920313 | 7000.00 |
| L920401 | 4173.00 |
| L920416 | 6100.00 |

| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 1 | 3060.00 | 3848.00 |
| 2 | 2 | 3849.00 | 4636.00 |
| 3 | 3 | 4637.00 | 5424.00 |
| 4 | 2 | 5425.00 | 6212.00 |
| 5 | 1 | 6213.00 | 7001.00 |



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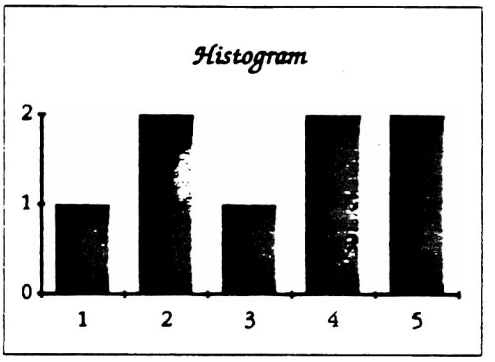
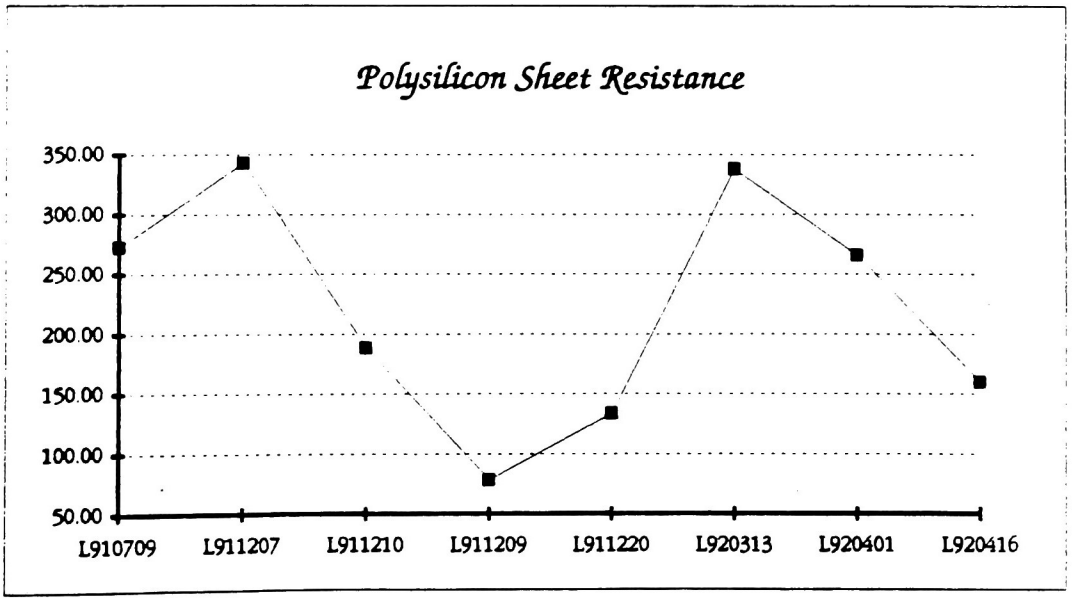
*Microelectronic Engineering*
*Capability Analysis (nMOS 2.0 process)*
*Step 34 - Poly Sheet Resistance*

| DEFINED | |
|---|---|
| *Target* | |
| *USL* | |
| *LSL* | |
| *UCL* | |
| *LCL* | |
| **STATISTICAL** | |
| *Mean* | 222.61 |
| *Std. Dev.* | 97.17 |
| *Count* | 8 |
| *Max. Val.* | 343.30 |
| *Min. Val.* | 78.50 |
| *Range* | 264.80 |
| **CAPABILITY** | |
| *Cp* | 0.00 |
| *k* | #DIV/0! |
| *Cpk* | 0.76 |

| Lot Number | Rs (Ω/sq.) |
|---|---|
| L910709 | 273.00 |
| L911207 | 343.30 |
| L911210 | 188.60 |
| L911209 | 78.50 |
| L911220 | 133.50 |
| L920313 | 338.00 |
| L920401 | 266.00 |
| L920416 | 160.00 |

| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 1 | 78.50 | 131.46 |
| 2 | 2 | 132.46 | 184.42 |
| 3 | 1 | 185.42 | 237.38 |
| 4 | 2 | 238.38 | 290.34 |
| 5 | 2 | 291.34 | 344.30 |



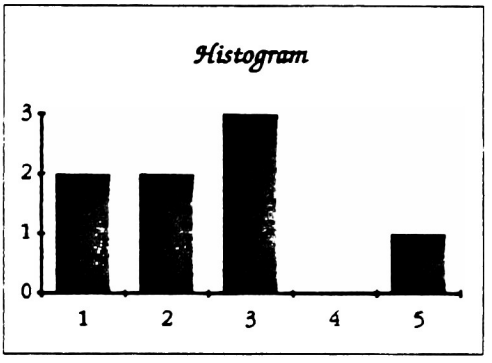



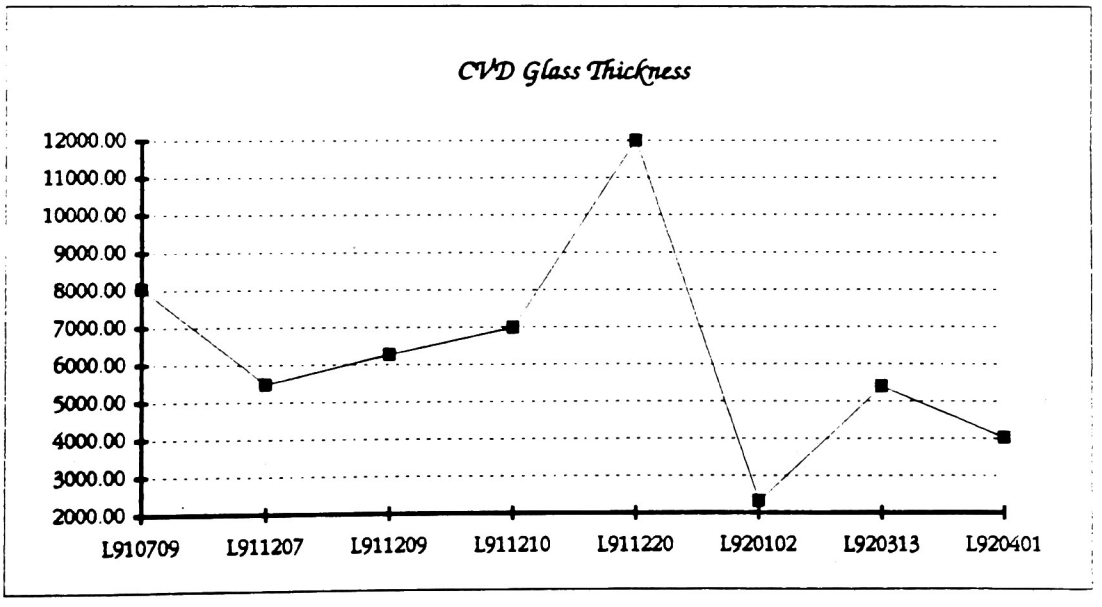
*Rochester Institute of Technology*
*Microelectronic Engineering*
*Capability Analysis (nMOS 2.0 process)*
*Step 40 - CVD Oxide Glass*

| DEFINED | |
|---|---|
| *Target* | |
| *USL* | |
| *LSL* | |
| *UCL* | |
| *LCL* | |
| **STATISTICAL** | |
| *Mean* | 6316.30 |
| *Std. Dev.* | 2889.96 |
| *Count* | 8 |
| *Max. Val.* | 12000.00 |
| *Min. Val.* | 2325.40 |
| *Range* | 9674.60 |
| **CAPABILITY** | |
| *Cp* | 0.00 |
| *k* | #DIV/0! |
| *Cpk* | 0.73 |

| Lot Number | GLASSox (Ang) |
|---|---|
| L910709 | 8045.00 |
| L911207 | 5479.00 |
| L911209 | 6273.00 |
| L911210 | 6984.00 |
| L911220 | 12000.00 |
| L920102 | 2325.40 |
| L920313 | 5400.00 |
| L920401 | 4024.00 |

| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 2 | 2325.40 | 4260.32 |
| 2 | 2 | 4261.32 | 6195.24 |
| 3 | 3 | 6196.24 | 8130.16 |
| 4 | 0 | 8131.16 | 10065.08 |
| 5 | 1 | 10066.08 | 12001.00 |



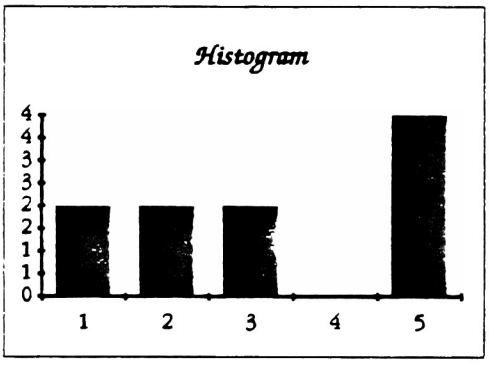



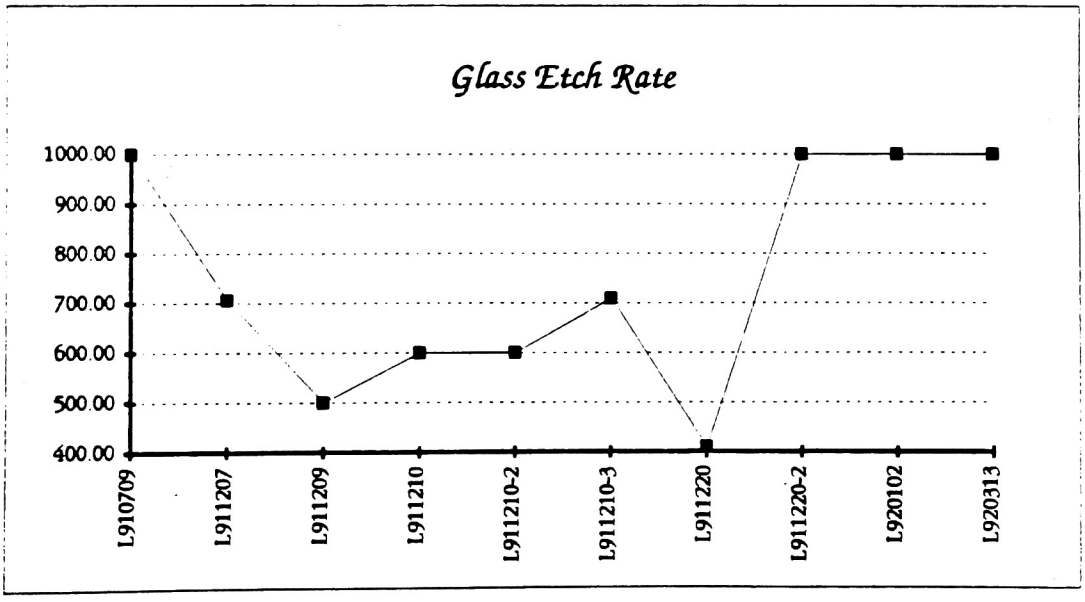
*Rochester Institute of Technology*
*Microelectronic Engineering*
*Capability Analysis (nMOS 2.0 process)*
*Step 42 - Glass Etch Rate*

| DEFINED | |
|---|---|
| Target | |
| USL | |
| LSL | |
| UCL | |
| LCL | |
| **STATISTICAL** | |
| Mean | 752.60 |
| Std. Dev. | 230.11 |
| Count | 10 |
| Max. Val. | 1000.00 |
| Min. Val. | 410.00 |
| Range | 590.00 |
| **CAPABILITY** | |
| Cp | 0.00 |
| k | #DIV/0! |
| Cpk | 1.09 |

| Lot Number | Rate (Ang/min) |
|---|---|
| L910709 | 1000.00 |
| L911207 | 706.00 |
| L911209 | 500.00 |
| L911210 | 600.00 |
| L911210-2 | 600.00 |
| L911210-3 | 710.00 |
| L911220 | 410.00 |
| L911220-2 | 1000.00 |
| L920102 | 1000.00 |
| L920313 | 1000.00 |

| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 2 | 410.00 | 528.00 |
| 2 | 2 | 529.00 | 646.00 |
| 3 | 2 | 647.00 | 764.00 |
| 4 | 0 | 765.00 | 882.00 |
| 5 | 4 | 883.00 | 1001.00 |



*Rochester Institute of Technology*
*Microelectronic Engineering*
*Capability Analysis (nMOS 2.0 process)*
*Step 42 - Metal Deposition*

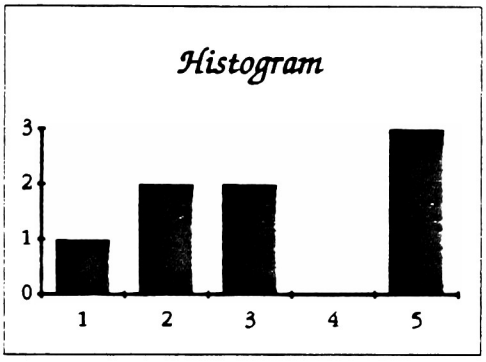
| DEFINED | |
|---|---|
| Target | |
| USL | |
| LSL | |
| UCL | |
| LCL | |

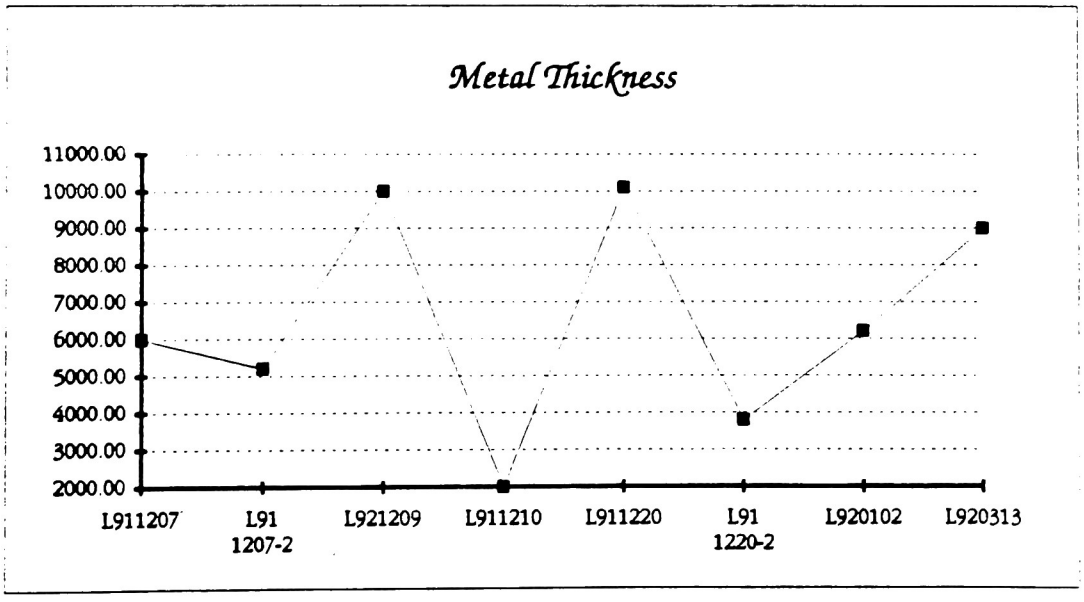
| STATISTICAL | |
|---|---|
| Mean | 6537.50 |
| Std. Dev. | 2952.45 |
| Count | 8 |
| Max. Val. | 10100.00 |
| Min. Val. | 2000.00 |
| Range | 8100.00 |

| CAPABILITY | |
|---|---|
| Cp | 0.00 |
| k | #DIV/0! |
| Cpk | 0.74 |

| Lot Number | Mtckn. (Ang.) |
|---|---|
| L911207 | 6000.00 |
| L911207-2 | 5200.00 |
| L921209 | 10000.00 |
| L911210 | 2000.00 |
| L911220 | 10100.00 |
| L911220-2 | 3800.00 |
| L920102 | 6200.00 |
| L920313 | 9000.00 |

| Histogram | | | |
|---|---|---|---|
| Group | Count | MIN | MAX |
| 1 | 1 | 2000.00 | 3620.00 |
| 2 | 2 | 3621.00 | 5240.00 |
| 3 | 2 | 5241.00 | 6860.00 |
| 4 | 0 | 6861.00 | 8480.00 |
| 5 | 3 | 8481.00 | 10101.00 |



# APPENDIX F

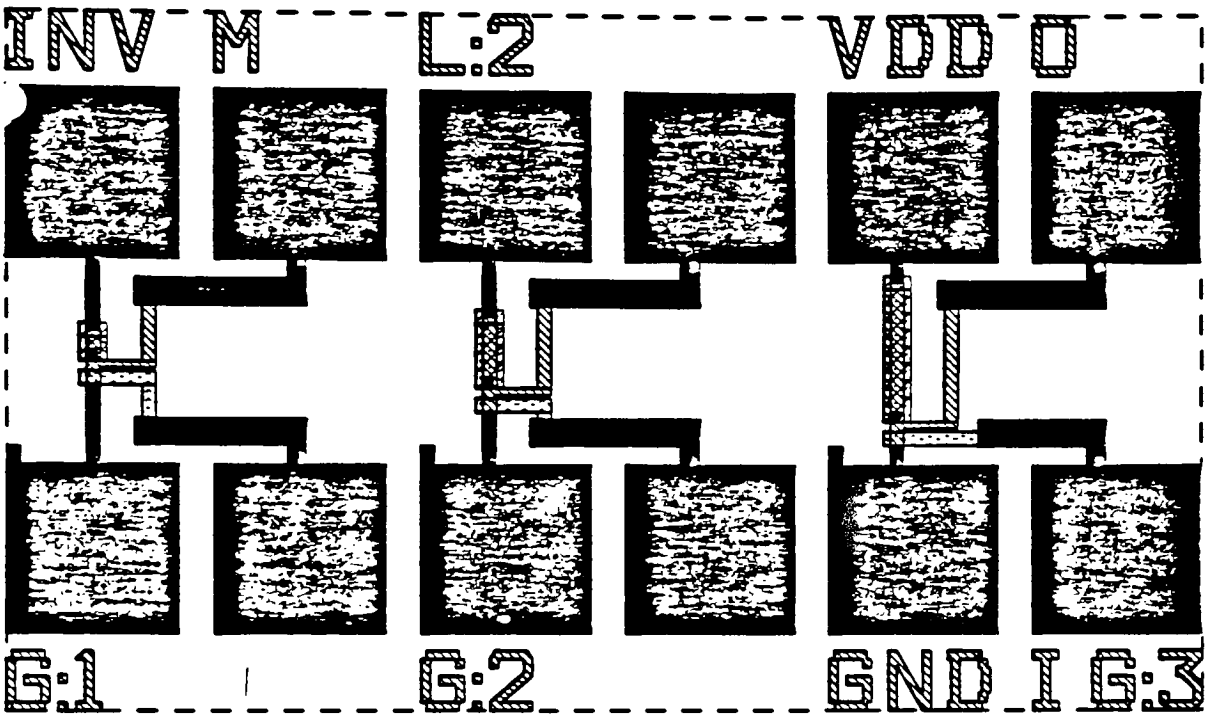
*VLSI Layouts, Circuit Diagrams, HSPICE Netlists and Simulation Results*

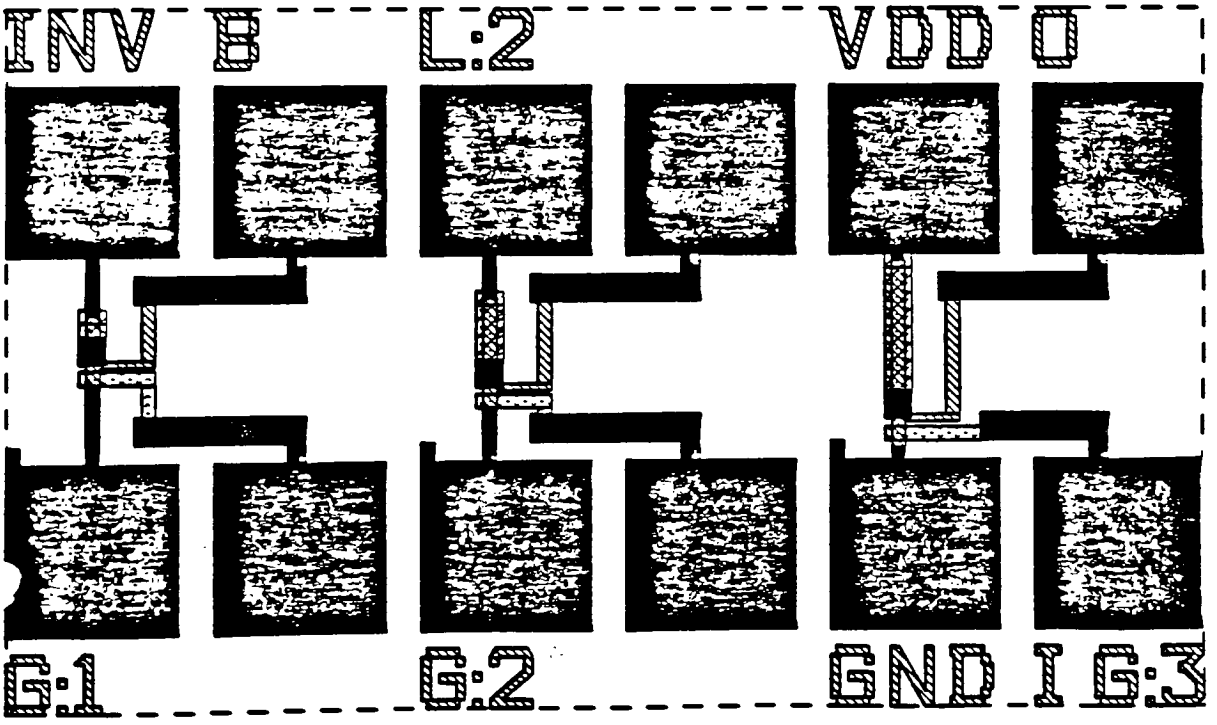
| | |
|---|---|
| CELL | : 38 and 39 (continued) |
| CONTENTS | : D/E mode inverter |
| PAD CONFIGURATION | : small 12 pad |
| STRUCTURE | : NMOS inverter with gains of 1, 2 and 3 designed with $\lambda = 2$ µm |
| TOTAL AREA | : 700 x 400 µm |

Cell 39

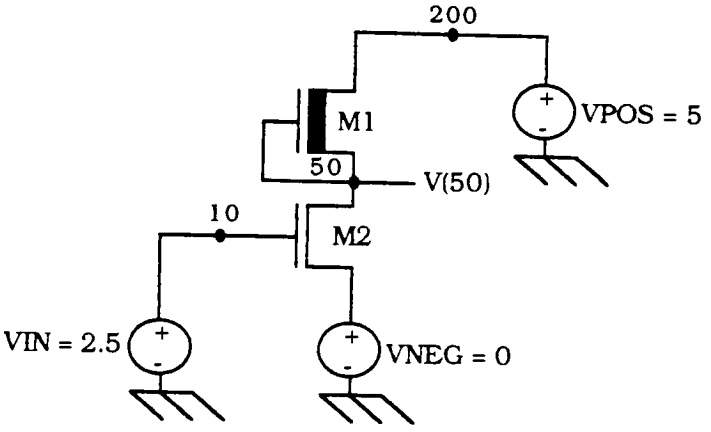
Cell 39 contains three D/E inverters, with gains of 1, 2 and 3. The designed inverters use minimum sized enhancement transistors. The depletion mode transistors have the same dimensions as the depletion mode transistors in cell 38. These particular inverters use buried contacts, to connect the gate of the depletion mode transistor to its source.
The output of these inverters should be equivalent to the simulation results for the inverters in cell 38.

REMARK :
The simulations are performed without alteration of parameters in the spice model.


INV M
L:2
VDD O
G:1
G:2
GND I G:3


INV B
L:2
VDD O
G:1
G:2
GND I G:3

# Single nMOS Inverter



```
 ******    h s p i c e      h92b.02          10:56:21  27-JUL93   vax
* file: experimental design simulation #1
****** copyright 1990 meta-software,inc. *****site:rochester tech
******  input listing                     evaluation expires 931213
******
* lib$disk:[acclib.meta.h92b]:hspice.ini
* july 1993
* submitted as an appendix for the m.s. degree thesis of
* J. Ignacio Gutierrez Topete Espinosa de los Monteros
* nmos inverter with theoretical gain=2 and lambda=2 micron design rules.
* treatment combination 0
*
*
.option scale=1u scalm=1.0
.op
vneg 100 0 dc 0
vpos 200 0 dc 5
vin 10 0 dc 2.5
m1 200 50 50 50 depmod l=32 w=8 ad=64 as=16 pd=32 ps=20 nrd=16 nrs=4
+ m=1 geo=2
m2 50 10 100 0 enhmod l=8 w=8 ad=16 as=64 pd=20 ps=32 nrd=4 nrs=16
+ off m=1 geo=1
*
*
.model depmod nmos level=3 kp=3.281897e-05 tox=828.2e-10 vmax=674713
+ ld=1.01616u xj=1.89u delta=2.79525 gamma=0.371508 nfs=4.310e+12
+ nsub=3.1e+14 vto=-3.78687 uo=900.00 acm=3 js=1e-04 jsw=1e-10 cj=1.1e-04
+ cjsw=5e-10 mj=0.5 mjsw=0.33 rd=700 rdc=1 rs=700 rsc=1 rsh=23.31 ldif=4
+ hdif=28 nss=3.6e+11 tpg=1.0 capop=9 cgbo=1.7e-10 cgdo=1.6e-10 cgso=1.6e-10
*
.model enhmod nmos level=3 kp=3.730740e-05 tox=828.2e-10 vmax=100000
+ ld=0.826296u xj=1.89u delta=1.15554 gamma=0.628861 nfs=1.902288e+12
+ nsub=3.1e+14 vto=1.14181 uo=300.00 acm=3 js=1e-04 jsw=1e-10 cj=1.1e-04
+ cjsw=5e-10 mj=0.5 mjsw=0.33 rd=700 rdc=1 rs=700 rsc=1 rsh=23.31 ldif=1
+ hdif=7 nss=3.6e+11 tpg=1.0 capop=9 cgbo=1.7e-10 cgdo=1.6-10 cgso=1.6e-10
*
.dc vin 0 5 .1
.print dc i(vneg), v(50)
.plot dc v(50) (0,5), i(vneg)
.width out=80
.end
```

```
******    h s p i c e      h92b.02          10:56:21  27-JUL93   vax
* file: experimental design simulation #1
****** copyright 1990 meta-software,inc. *****site:rochester_tech
******  mos   model parameters           tnom=  25.000 temp=  25.000
******
********************************************************************************
*** common model parameters  model name:   0:depmod   model type:nmos   ***
********************************************************************************
    names  values   units     names  values   units     names  values   units
    -----  ------   -----     -----  ------   -----     -----  ------   -----

  1*** geometry parameters ***
      ld=   1.02u meters       lmlt=   1.00                wd=   0.     meters
    wmlt=   1.00                 xl=   0.     meters      xw=   0.     meters
    lref=   0.     meters      wref=   0.     meters    lref=   0.     meters
    wref=   0.     meters     xlref=   0.     meters   xwref=   0.     meters
    lmin=   0.     meters      wmin=   0.     meters    lmax=   0.     meters
    wmax=   0.     meters

  2*** threshold voltage parameters ***
     vto=  -3.79  volts         nss= 360.00g 1/cm**2     tpg=   1.00
     phi= 519.66m volts       gamma= 371.51m v**0.5     bulk=  gnd
   ngate=   0.    cm**3        nsub= 3.1e+14 1/cm**3  delvto=   0.     volts

  3*** gate overlap capacitance parameters ***
    cgbo= 170.00p f/meter     cgdo= 160.00p f/meter     cgso= 160.00p f/meter
    meto=   0.    meters

  4*** gate capacitance parameters ***
   capop=   9.00                cf1=   0.     volts      cf2= 100.00m volts
     cf3=   1.00  volts         cf4=  50.00              cf5= 666.67m
     cf6= 500.00                xqc= 500.00m             tox=  82.82n meters
     cox= 416.95u f/m**2

  5*** diffusion parasitic parameters ***
     acm=   3.00                 is=  10.00f amps         js= 100.00u a/m**2
     jsw= 100.00p amp/m         nds=   1.00              cbd=   0.     farad
     cbs=   0.    farad          cj= 110.00u f/m**2     cjsw= 500.00p f/m
  cjgate= 500.00p f/m            mj= 500.00m            mjsw= 330.00m
      pb= 800.00m volts         php= 800.00m volts        tt=   0.     secs
    hdif=  28.00  meters       ldif=   4.00  meters       rd= 700.00  ohms
      rs= 700.00  ohms          rsh=  23.31  ohms/sq      fc=   0.
   alpha=   0.                  vcr=   0.    volts     iirat=   0.
     rdc=   1.00  ohms          rsc=   1.00  ohms          n=   1.00
    vnds=  -1.00  volts

  6*** temperature effect parameters ***
    tlev=   0.                tlevc=   0.                 eg=   1.11  ev
    gap1= 702.00u ev/deg       gap2=   1.11k deg        xti=   0.
     bex=  -1.50                tcv=   0.    v/deg k     trd=   0.     /deg
     trs=   0.    /deg          cta=   0.    /deg        ctp=   0.     /deg

  7*** noise parameters ***
      kf=   0.                   af=   1.00             nlev=   2.00
  gdsnoi=   1.00

  *** level  3  model parameters  ***

   delta=   2.80                 eta=   0.             kappa= 200.00m /v
     nfs= 4.3e+12 1/cm**2      theta=   0.     /v        vmax= 674.71k m/sec
```

```
      xj=   1.89u meters          uo= 900.00 cm**2/vs        kp=  32.82u a/v**2
   deriv=   1.00
********************************************************************************
*** common model parameters  model name:   0:enhmod   model type:nmos   ***
********************************************************************************
    names  values   units     names  values   units     names  values   units
    -----  ------   -----     -----  ------   -----     -----  ------   -----

  1*** geometry parameters ***
      ld= 826.30n meters       lmlt=   1.00               wd=   0.     meters
    wmlt=   1.00                 xl=   0.     meters      xw=   0.     meters
    lref=   0.     meters       wref=   0.     meters    lref=   0.     meters
    wref=   0.     meters      xlref=   0.     meters   xwref=   0.     meters
    lmin=   0.     meters       wmin=   0.     meters    lmax=   0.     meters
    wmax=   0.     meters

  2*** threshold voltage parameters ***
     vto=   1.14  volts          nss= 360.00g 1/cm**2     tpg=   1.00
     phi= 519.66m volts        gamma= 628.86m v**0.5      bulk=  gnd
   ngate=   0.    cm**3         nsub= 3.1e+14 1/cm**3   delvto=   0.     volts

  3*** gate overlap capacitance parameters ***
    cgbo= 170.00p f/meter      cgdo=   1.60  f/meter     cgso= 160.00p f/meter
    meto=   0.    meters

  4*** gate capacitance parameters ***
   capop=   9.00                cf1=   0.     volts       cf2= 100.00m volts
     cf3=   1.00  volts         cf4=  50.00               cf5= 666.67m
     cf6= 500.00                xqc= 500.00m              tox=  82.82n meters
     cox= 416.95u f/m**2

  5*** diffusion parasitic parameters ***
     acm=   3.00                 is=  10.00f amps          js= 100.00u a/m**2
     jsw= 100.00p amp/m         nds=   1.00               cbd=   0.     farad
     cbs=   0.    farad          cj= 110.00u f/m**2      cjsw= 500.00p f/m
  cjgate= 500.00p f/m            mj= 500.00m             mjsw= 330.00m
      pb= 800.00m volts         php= 800.00m volts         tt=   0.     secs
    hdif=   7.00  meters       ldif=   1.00  meters       rd= 700.00  ohms
      rs= 700.00  ohms          rsh=  23.31  ohms/sq      fc=   0.
   alpha=   0.                  vcr=   0.    volts      iirat=   0.
     rdc=   1.00  ohms          rsc=   1.00  ohms          n=   1.00
    vnds=  -1.00  volts

  6*** temperature effect parameters ***
    tlev=   0.                tlevc=   0.                 eg=   1.11  ev
    gap1= 702.00u ev/deg       gap2=   1.11k deg         xti=   0.
     bex=  -1.50                tcv=   0.    v/deg k      trd=   0.     /deg
     trs=   0.    /deg          cta=   0.    /deg         ctp=   0.     /deg

  7*** noise parameters ***
      kf=   0.                   af=   1.00              nlev=   2.00
  gdsnoi=   1.00

  *** level 3 model parameters ***

   delta=   1.16                 eta=   0.               kappa= 200.00m /v
     nfs= 1.9e+12 1/cm**2      theta=   0.     /v         vmax= 100.00k m/sec
      xj=   1.89u meters          uo= 300.00 cm**2/vs       kp=  37.31u a/v**2
   deriv=   1.00
```

```
******    h s p i c e      h92b.02          10:56:21  27-JUL93   vax
* file: experimental design simulation #1
****** copyright 1990 meta-software,inc. *****site:rochester_tech
******  dc transfer curves                tnom=  25.000 temp=  25.000
******
```

| volt | current vneg | voltage 50 |
|---|---|---|
| 0. | 1.2914n | 4.0934 |
| 100.00000m | 1.6614n | 3.8347 |
| 200.00000m | 2.0839n | 3.5392 |
| 300.00000m | 2.5550n | 3.2098 |
| 400.00000m | 3.0700n | 2.8496 |
| 500.00000m | 3.6245n | 2.4618 |
| 600.00000m | 4.2143n | 2.0493 |
| 700.00000m | 4.8356n | 1.6148 |
| 800.00000m | 5.4849n | 1.1606 |
| 900.00000m | 5.6190n | 1.0668 |
| 1.00000 | 5.6588n | 1.0389 |
| 1.10000 | 5.6806n | 1.0237 |
| 1.20000 | 5.6934n | 1.0148 |
| 1.30000 | 5.7012n | 1.0093 |
| 1.40000 | 5.7061n | 1.0059 |
| 1.50000 | 5.7091n | 1.0038 |
| 1.60000 | 5.7110n | 1.0024 |
| 1.70000 | 5.7122n | 1.0016 |
| 1.80000 | 5.7130n | 1.0010 |
| 1.90000 | 5.7135n | 1.0007 |
| 2.00000 | 5.7138n | 1.0005 |
| 2.10000 | 5.7139n | 1.0004 |
| 2.20000 | 5.7140n | 1.0003 |
| 2.30000 | 5.7141n | 1.0003 |
| 2.40000 | 5.7141n | 1.0002 |
| 2.50000 | 5.7142n | 1.0002 |
| 2.60000 | 5.7142n | 1.0002 |
| 2.70000 | 5.7142n | 1.0002 |
| 2.80000 | 5.7142n | 1.0002 |
| 2.90000 | 5.7142n | 1.0002 |
| 3.00000 | 5.7142n | 1.0002 |
| 3.10000 | 5.7142n | 1.0002 |
| 3.20000 | 5.7142n | 1.0002 |
| 3.30000 | 5.7142n | 1.0002 |
| 3.40000 | 5.7143n | 1.0002 |
| 3.50000 | 5.7143n | 1.0002 |
| 3.60000 | 5.7143n | 1.0002 |
| 3.70000 | 5.7143n | 1.0002 |
| 3.80000 | 5.7143n | 1.0001 |
| 3.90000 | 5.7143n | 1.0001 |
| 4.00000 | 5.7143n | 1.0001 |
| 4.10000 | 5.7143n | 1.0001 |
| 4.20000 | 5.7143n | 1.0001 |
| 4.30000 | 5.7143n | 1.0001 |
| 4.40000 | 5.7143n | 1.0001 |
| 4.50000 | 5.7143n | 1.0001 |
| 4.60000 | 5.7143n | 1.0001 |
| 4.70000 | 5.7143n | 1.0001 |
| 4.80000 | 5.7143n | 1.0001 |
| 4.90000 | 5.7143n | 1.0001 |
| 5.00000 | 5.7143n | 1.0001 |

**legend:**

a: v(50)
b: i(vneg)

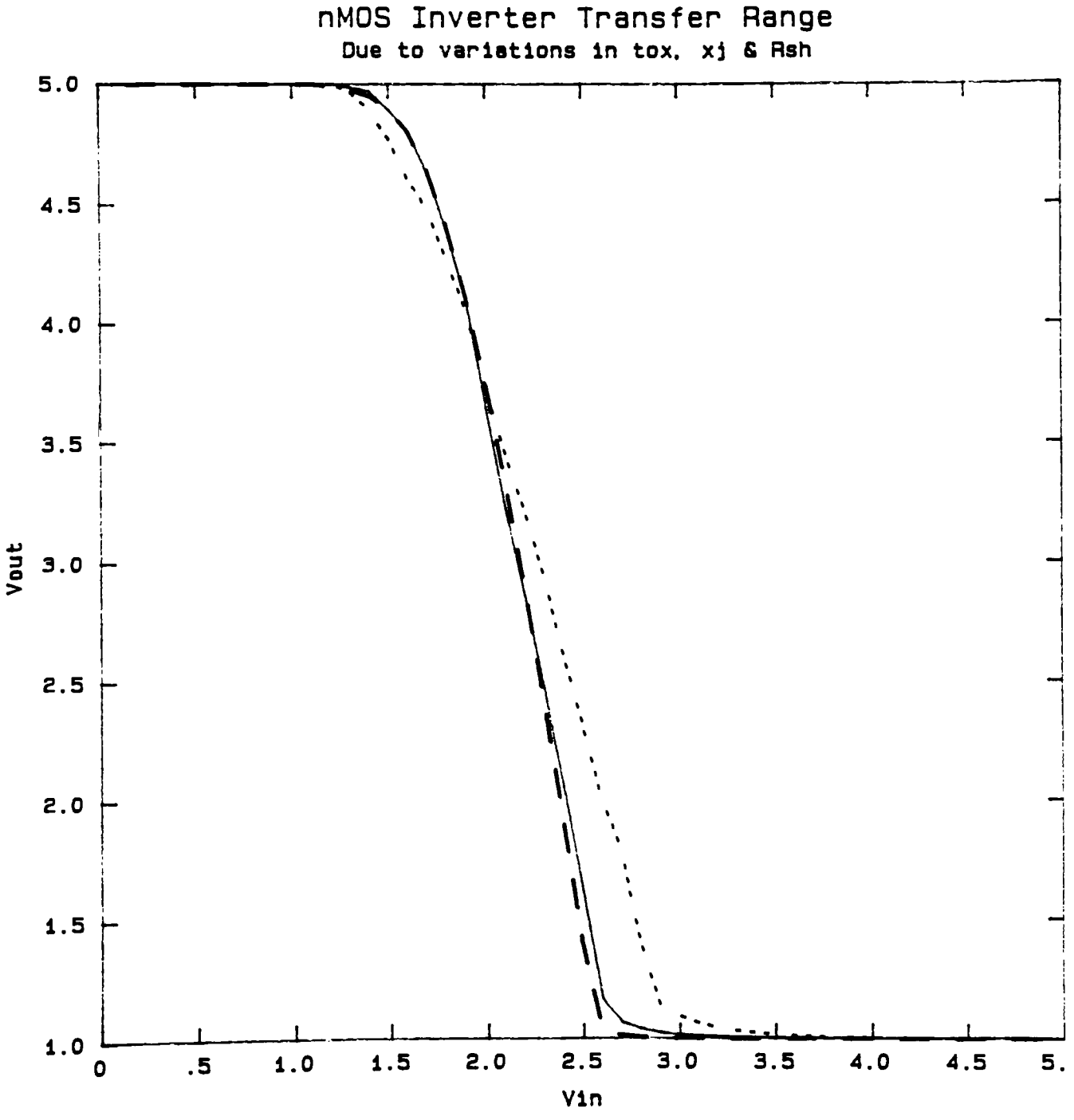
```
     volt        v(50)
(a         )      0.          1.2500          2.5000          3.7500          5.0000
(b         )      0.          2.0000n         4.0000n         6.0000n         8.0000n
                +              +               +               +               +
   0.          4.093 -+-------+-b-----+-------+-------+-------+-------+---a---+-------+-
 100.0000m     3.835  +       +    b  +       +       +       +       +  a    +       +
 200.0000m     3.539  +       +      +b       +       +       +    a  +       +       +
 300.0000m     3.210  +       +       +   b   +       +       +a      +       +       +
 400.0000m     2.850  +       +       +       b       +    a  +       +       +       +
 500.0000m     2.462  +       +       +         b  a  +       +       +       +       +
 600.0000m     2.049  +       +       +  a    + b     +       +       +       +       +
 700.0000m     1.615  +       +       +   a   +       +     b+       +       +       +
 800.0000m     1.161  +       +      a+       +       +       +  b    +       +       +
 900.0000m     1.067  +       +    a  +       +       +       +   b   +       +       +
   1.0000      1.039 -+-------+----a--+-------+-------+-------+-------b-+-------+-------+-
   1.1000      1.024  +       +  a    +       +       +       +       b +       +       +
   1.2000      1.015  +       +  a    +       +       +       +       b +       +       +
   1.3000      1.009  +       +  a    +       +       +       +       b +       +       +
   1.4000      1.006  +       +  a    +       +       +       +       b +       +       +
   1.5000      1.004  +       +  a    +       +       +       +       b +       +       +
   1.6000      1.002  +       +  a    +       +       +       +       b +       +       +
   1.7000      1.002  +       +  a    +       +       +       +       b +       +       +
   1.8000      1.001  +       +  a    +       +       +       +       b +       +       +
   1.9000      1.001  +       +  a    +       +       +       +       b +       +       +
   2.0000      1.000 -+-------+--a----+-------+-------+-------+-------b-+-------+-------+-
   2.1000      1.000  +       +  a    +       +       +       +       b +       +       +
   2.2000      1.000  +       +  a    +       +       +       +       b +       +       +
   2.3000      1.000  +       +  a    +       +       +       +       b +       +       +
   2.4000      1.000  +       +  a    +       +       +       +       b +       +       +
   2.5000      1.000  +       +  a    +       +       +       +       b +       +       +
   2.6000      1.000  +       +  a    +       +       +       +       b +       +       +
   2.7000      1.000  +       +  a    +       +       +       +       b +       +       +
   2.8000      1.000  +       +  a    +       +       +       +       b +       +       +
   2.9000      1.000  +       +  a    +       +       +       +       b +       +       +
   3.0000      1.000 -+-------+--a----+-------+-------+-------+-------b-+-------+-------+-
   3.1000      1.000  +       +  a    +       +       +       +       b +       +       +
   3.2000      1.000  +       +  a    +       +       +       +       b +       +       +
   3.3000      1.000  +       +  a    +       +       +       +       b +       +       +
   3.4000      1.000  +       +  a    +       +       +       +       b +       +       +
   3.5000      1.000  +       +  a    +       +       +       +       b +       +       +
   3.6000      1.000  +       +  a    +       +       +       +       b +       +       +
   3.7000      1.000  +       +  a    +       +       +       +       b +       +       +
   3.8000      1.000  +       +  a    +       +       +       +       b +       +       +
   3.9000      1.000  +       +  a    +       +       +       +       b +       +       +
   4.0000      1.000 -+-------+--a----+-------+-------+-------+-------b-+-------+-------+-
   4.1000      1.000  +       +  a    +       +       +       +       b +       +       +
   4.2000      1.000  +       +  a    +       +       +       +       b +       +       +
   4.3000      1.000  +       +  a    +       +       +       +       b +       +       +
   4.4000      1.000  +       +  a    +       +       +       +       b +       +       +
   4.5000      1.000  +       +  a    +       +       +       +       b +       +       +
   4.6000      1.000  +       +  a    +       +       +       +       b +       +       +
   4.7000      1.000  +       +  a    +       +       +       +       b +       +       +
   4.8000      1.000  +       +  a    +       +       +       +       b +       +       +
```

```
 ******    h s p i c e      h92b.02          10:56:21  27-JUL93   vax
* file: experimental design simulation #1
****** copyright 1990 meta-software,inc. *****site:rochester_tech
******  operating point information      tnom=  25.000 temp=  25.000
******
***** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:10      =   2.5000  0:50      =   1.0002  0:100     =   0.
+0:200     =   5.0000


**** voltage sources

subckt
element  0:vneg      0:vpos      0:vin
 volts      0.          5.0000      2.5000
 current    5.7142n    -5.7152n     0.
 power      0.         28.5758n     0.


    total voltage source power dissipation=   28.5758n       watts

**** mosfets

subckt
element  0:m1        0:m2
model    0:depmod    0:enhmod
 id         5.7131n     5.7150n
 ibs       -7.1960f    -4.7999f
 ibd      -19.1948f    -1.8005f
 vgs        0.          2.5000
 vds        3.9998      1.0002
 vbs        0.          0.
 vth       -3.1577      1.2440
 vdsat    970.5602m   631.7628m
 beta       8.7611u    47.0203u
 gam eff  348.8240m   493.2419m
 gm         4.9319n     7.5607n
 gds       10.1408u    35.5080u
 gmb        1.1911n     1.9118n
 cdtot     49.4097f    12.8000u
 cgtot    107.6137f    12.8000u
 cstot     42.6315f    30.7266f
 cbtot     56.9042f    43.3127f
 cgs       51.2697f    11.8671f
 cgd       51.2495f    12.8000u
```

—— **Nominal**

- - - **Upper Limit**

— — **Lower Limit**



| | | |
|---|---|---|
| CELL | : | 53 |
| CONTENTS | : | ring-oscillators |
| PAD CONFIGURATION | : | large 12 pad |
| STRUCTURE | : | 11-stage ringoscillators, designed with λ=2, 4 and 10 μm |
| TOTAL AREA | : | 700 x 1896 μm |

The ringoscillators provide the delay in inverters, by way of relating the generated frequency to the total delay time. The ouputs of the ringoscillators, designed with λ=4 and 10 μm are not buffered using a special buffer configuration. These ringoscillators have an extra inverter configuration between the actual output and the output pad.. The ouputs are labelled O. The 2 μm based ringoscillator has as well as an unbuffered (it does have that extra inverter between the actual ouput and the output pad) as a buffered output, using the super-buffer, designed with λ= 4 μm. It has the same dimensions as the super-buffer in cell 54. The super-buffer needs a separate power rail. The inverters in each ringoscillator have a k-ration of k=4.
Simulation of a series of four inverters show (A is input, Q is output) :

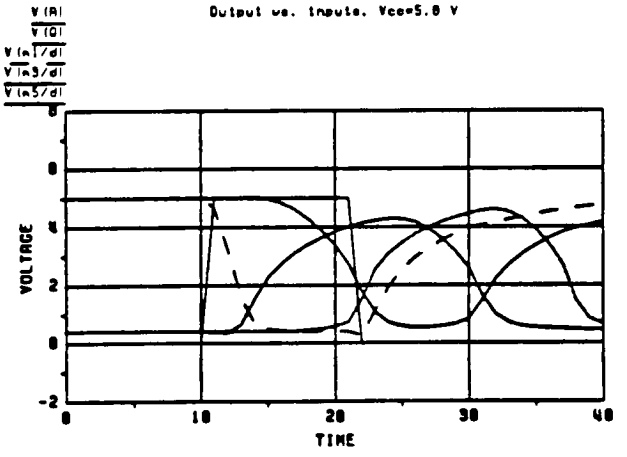
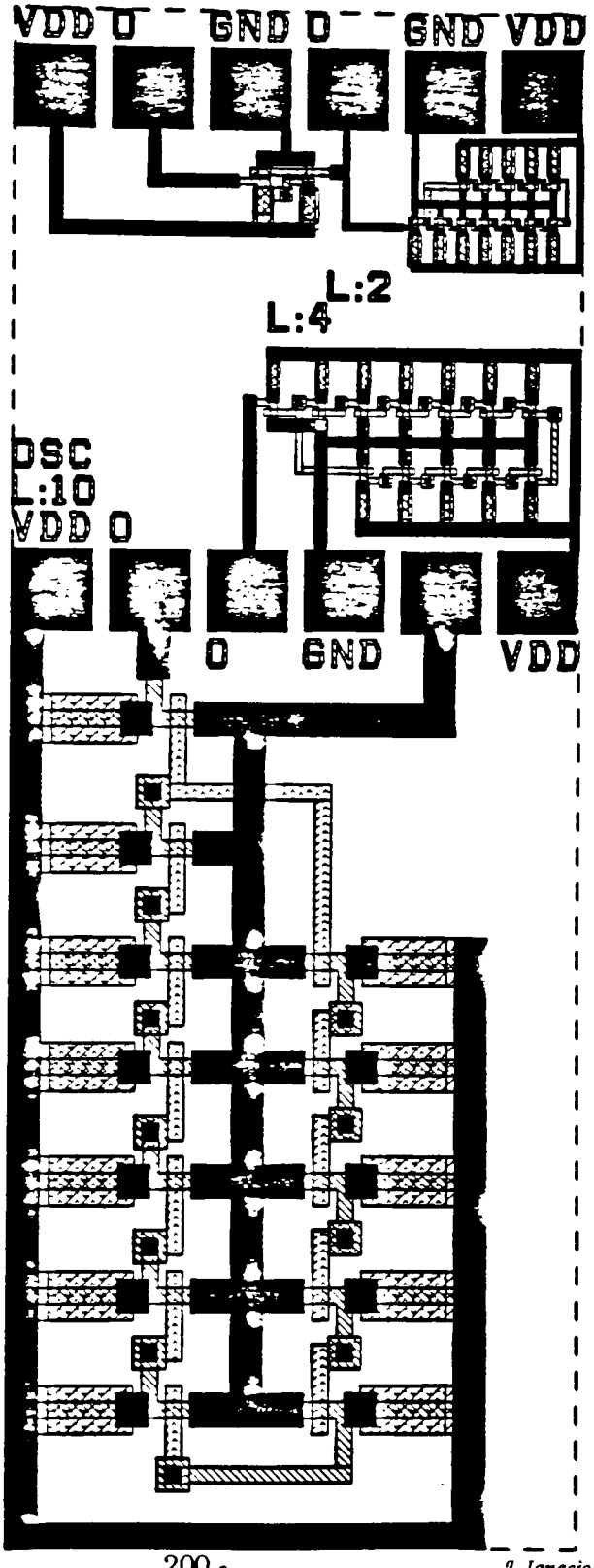
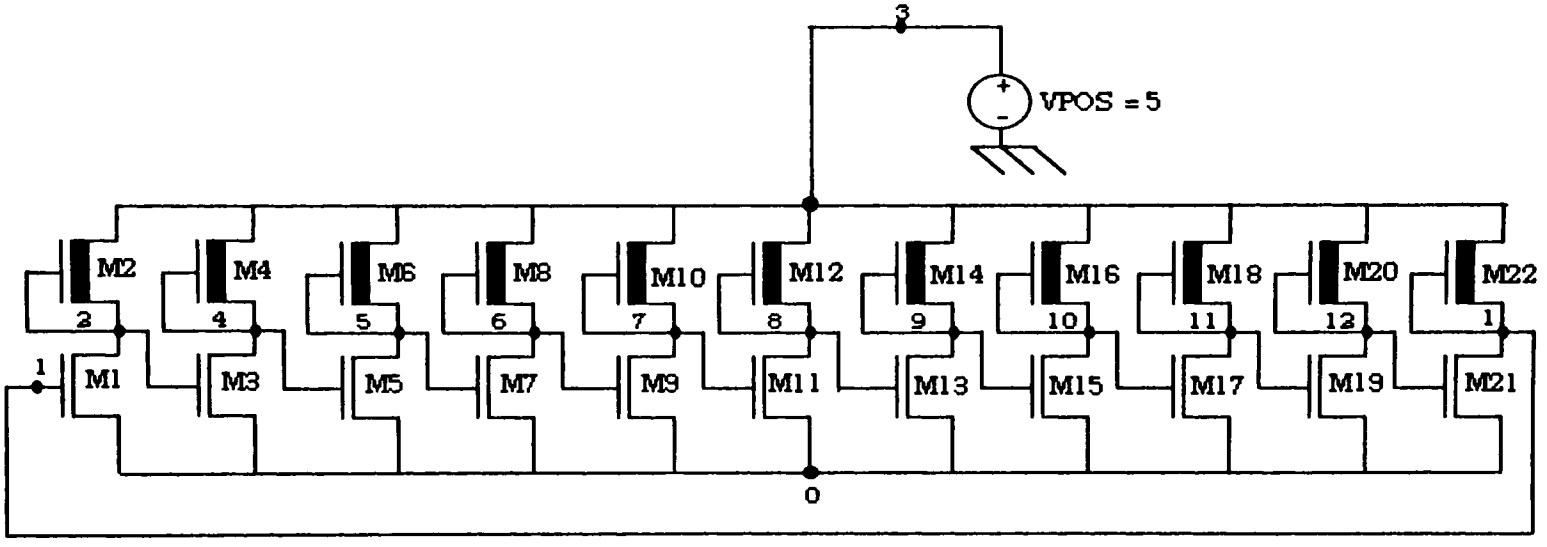



Figure 14

REMARK :


VDD
O
GND
O
GND
VDD
L:2
L:4
DSC
L:10
VDD
O
O
GND
VDD

# 11-Stage nMOS Ring Oscillator



```
 ******    h s p i c e      h92b.02          11:00:35  27-JUL93   vax
* file: experimental design simulation #2
****** copyright 1990 meta-software,inc. *****site:rochester_tech
******  input listing                     evaluation expires 931213
******
* lib$disk:[acclib.meta.h92b]:hspice.ini
* july 1993
* submitted as an appendix for the m.s. degree thesis of
* j. ignacio gutierrez topete espinosa de los monteros
* 11 stage ring oscillator made out of 11 nmos inverters all
* with theoretical gain=2 and lambda=2 micron design rules.
*
*
.option scale=1u scalm=1.0
vpos 3 0 dc 5
*  d   g   s   sub   -   order of node connections!!!
m1 2 1 0 0 enhmod l=8 w=8 ad=16 as=64 pd=20 ps=32 nrd=4 nrs=16
+ off m=1 geo=1
m2 3 2 2 2 depmod l=32 w=8 ad=64 as=16 pd=32 ps=20 nrd=16 nrs=4
+ m=1 geo=2
m3 4 2 0 0 enhmod l=8 w=8 ad=16 as=64 pd=20 ps=32 nrd=4 nrs=16
+ off m=1 geo=1
m4 3 4 4 4 depmod l=32 w=8 ad=64 as=16 pd=32 ps=20 nrd=16 nrs=4
+ m=1 geo=2
m5 5 4 0 0 enhmod l=8 w=8 ad=16 as=64 pd=20 ps=32 nrd=4 nrs=16
+ off m=1 geo=1
m6 3 5 5 5 depmod l=32 w=8 ad=64 as=16 pd=32 ps=20 nrd=16 nrs=4
+ m=1 geo=2
m7 6 5 0 0 enhmod l=8 w=8 ad=16 as=64 pd=20 ps=32 nrd=4 nrs=16
+ off m=1 geo=1
m8 3 6 6 6 depmod l=32 w=8 ad=64 as=16 pd=32 ps=20 nrd=16 nrs=4
+ m=1 geo=2
m9 7 6 0 0 enhmod l=8 w=8 ad=16 as=64 pd=20 ps=32 nrd=4 nrs=16
+ off m=1 geo=1
m10 3 7 7 7 depmod l=32 w=8 ad=64 as=16 pd=32 ps=20 nrd=16 nrs=4
+ m=1 geo=2
m11 8 7 0 0 enhmod l=8 w=8 ad=16 as=64 pd=20 ps=32 nrd=4 nrs=16
+ off m=1 geo=1
m12 3 8 8 8 depmod l=32 w=8 ad=64 as=16 pd=32 ps=20 nrd=16 nrs=4
+ m=1 geo=2
m13 9 8 0 0 enhmod l=8 w=8 ad=16 as=64 pd=20 ps=32 nrd=4 nrs=16
+ off m=1 geo=1
m14 3 9 9 9 depmod l=32 w=8 ad=64 as=16 pd=32 ps=20 nrd=16 nrs=4
+ m=1 geo=2
m15 10 9 0 0 enhmod l=8 w=8 ad=16 as=64 pd=20 ps=32 nrd=4 nrs=16
+ off m=1 geo=1
m16 3 10 10 10 depmod l=32 w=8 ad=64 as=16 pd=32 ps=20 nrd=16 nrs=4
+ m=1 geo=2
m17 11 10 0 0 enhmod l=8 w=8 ad=16 as=64 pd=20 ps=32 nrd=4 nrs=16
+ off m=1 geo=1
m18 3 11 11 11 depmod l=32 w=8 ad=64 as=16 pd=32 ps=20 nrd=16 nrs=4
+ m=1 geo=2
m19 12 11 0 0 enhmod l=8 w=8 ad=16 as=64 pd=20 ps=32 nrd=4 nrs=16
+ off m=1 geo=1
m20 3 12 12 12 depmod l=32 w=8 ad=64 as=16 pd=32 ps=20 nrd=16 nrs=4
+ m=1 geo=2
m21 1 12 0 0 enhmod l=8 w=8 ad=16 as=64 pd=20 ps=32 nrd=4 nrs=16
+ off m=1 geo=1
m22 3 1 1 1 depmod l=32 w=8 ad=64 as=16 pd=32 ps=20 nrd=16 nrs=4
+ m=1 geo=2
```

```
*
*
.model depmod nmos level=3 kp=3.281897e-05 tox=828.2e-10 vmax=674713
+ ld=1.01616u xj=1.89u delta=2.79525 gamma=0.371508 nfs=4.310e+12
+ nsub=3.1e+14 vto=-3.78687 uo=900.00 acm=3 js=1e-04 jsw=1e-10 cj=1.1e-04
+ cjsw=5e-10 mj=0.5 mjsw=0.33 rd=700 rdc=1 rs=700 rsc=1 rsh=23.31 ldif=4
+ hdif=28 nss=3.6e+11 tpg=1.0 capop=9 cgbo=1.7e-10 cgdo=1.6e-10 cgso=1.6e-10
*
.model enhmod nmos level=3 kp=3.730740e-05 tox=828.2e-10 vmax=100000
+ ld=0.826296u xj=1.89u delta=1.15554 gamma=0.628861 nfs=1.902288e+12
+ nsub=3.1e+14 vto=1.14181 uo=300.00 acm=3 js=1e-04 jsw=1e-10 cj=1.1e-04
+ cjsw=5e-10 mj=0.5 mjsw=0.33 rd=700 rdc=1 rs=700 rsc=1 rsh=23.31 ldif=1
+ hdif=7 nss=3.6e+11 tpg=1.0 capop=9 cgbo=1.7e-10 cgdo=1.6-10 cgso=1.6e-10
*
.ic v(1)=0 v(2)=5
.op
.tran 1us 100us uic
.plot tran v(1)
.width out=80
.end
```

```
******    h s p i c e      h92b.02          11:00:35  27-JUL93   vax
* file: experimental design simulation #2
****** copyright 1990 meta-software,inc. *****site:rochester_tech
******  mos   model parameters           tnom=  25.000 temp=  25.000
******
********************************************************************************
*** common model parameters  model name:   0:depmod   model type:nmos   ***
********************************************************************************
    names  values   units     names  values   units     names  values   units
    -----  ------   -----     -----  ------   -----     -----  ------   -----

  1*** geometry parameters ***
      ld=   1.02u meters      lmlt=   1.00               wd=   0.     meters
    wmlt=   1.00                xl=   0.     meters      xw=   0.     meters
    lref=   0.    meters      wref=   0.     meters    lref=   0.     meters
    wref=   0.    meters     xlref=   0.     meters   xwref=   0.     meters
    lmin=   0.    meters      wmin=   0.     meters    lmax=   0.     meters
    wmax=   0.    meters

  2*** threshold voltage parameters ***
     vto=  -3.79  volts        nss= 360.00g 1/cm**2     tpg=   1.00
     phi= 519.66m volts      gamma= 371.51m v**0.5     bulk=  gnd
   ngate=   0.    cm**3       nsub= 3.1e+14 1/cm**3  delvto=   0.     volts

  3*** gate overlap capacitance parameters ***
    cgbo= 170.00p f/meter     cgdo= 160.00p f/meter     cgso= 160.00p f/meter
    meto=   0.    meters

  4*** gate capacitance parameters ***
   capop=   9.00               cf1=   0.     volts       cf2= 100.00m volts
     cf3=   1.00  volts        cf4=  50.00               cf5= 666.67m
     cf6= 500.00               xqc= 500.00m              tox=  82.82n meters
     cox= 416.95u f/m**2

  5*** diffusion parasitic parameters ***
     acm=   3.00                 is=  10.00f amps          js= 100.00u a/m**2
     jsw= 100.00p amp/m         nds=   1.00              cbd=   0.     farad
     cbs=   0.    farad          cj= 110.00u f/m**2      cjsw= 500.00p f/m
  cjgate= 500.00p f/m            mj= 500.00m             mjsw= 330.00m
      pb= 800.00m volts         php= 800.00m volts         tt=   0.     secs
    hdif=  28.00  meters      ldif=   4.00  meters        rd= 700.00  ohms
      rs= 700.00  ohms          rsh=  23.31  ohms/sq      fc=   0.
   alpha=   0.                  vcr=   0.    volts     iirat=   0.
     rdc=   1.00  ohms          rsc=   1.00  ohms          n=   1.00
    vnds=  -1.00  volts

  6*** temperature effect parameters ***
    tlev=   0.                tlevc=   0.                 eg=   1.11  ev
    gap1= 702.00u ev/deg       gap2=   1.11k deg         xti=   0.
     bex=  -1.50                tcv=   0.    v/deg k      trd=   0.     /deg
     trs=   0.    /deg          cta=   0.    /deg         ctp=   0.     /deg

  7*** noise parameters ***
      kf=   0.                   af=   1.00              nlev=   2.00
  gdsnoi=   1.00

  ***  level  3  model parameters  ***

   delta=   2.80                 eta=   0.              kappa= 200.00m /v
     nfs= 4.3e+12 1/cm**2      theta=   0.     /v         vmax= 674.71k m/sec
```

```
     xj=   1.89u meters        uo= 900.00 cm**2/vs       kp=  32.82u a/v**2
  deriv=   1.00
********************************************************************************
*** common model parameters  model name:   0:enhmod   model type:nmos   ***
********************************************************************************
    names  values   units     names  values   units     names  values   units
    -----  ------   -----     -----  ------   -----     -----  ------   -----

  1*** geometry parameters ***
     ld= 826.30n meters      lmlt=   1.00               wd=   0.     meters
   wmlt=   1.00               xl=   0.     meters       xw=   0.     meters
   lref=   0.     meters     wref=   0.     meters     lref=   0.     meters
   wref=   0.     meters    xlref=   0.     meters    xwref=   0.     meters
   lmin=   0.     meters     wmin=   0.     meters     lmax=   0.     meters
   wmax=   0.     meters

  2*** threshold voltage parameters ***
    vto=   1.14  volts        nss= 360.00g 1/cm**2      tpg=   1.00
    phi= 519.66m volts      gamma= 628.86m v**0.5      bulk=  gnd
  ngate=   0.    cm**3       nsub= 3.1e+14 1/cm**3   delvto=   0.     volts

  3*** gate overlap capacitance parameters ***
   cgbo= 170.00p f/meter     cgdo=   1.60  f/meter     cgso= 160.00p f/meter
   meto=   0.    meters

  4*** gate capacitance parameters ***
  capop=   9.00               cf1=   0.     volts       cf2= 100.00m volts
    cf3=   1.00  volts        cf4=  50.00               cf5= 666.67m
    cf6= 500.00               xqc= 500.00m              tox=  82.82n meters
    cox= 416.95u f/m**2

  5*** diffusion parasitic parameters ***
    acm=   3.00                is=  10.00f amps          js= 100.00u a/m**2
    jsw= 100.00p amp/m        nds=   1.00               cbd=   0.     farad
    cbs=   0.    farad         cj= 110.00u f/m**2       cjsw= 500.00p f/m
 cjgate= 500.00p f/m           mj= 500.00m              mjsw= 330.00m
     pb= 800.00m volts        php= 800.00m volts         tt=   0.     secs
   hdif=   7.00  meters      ldif=   1.00  meters        rd= 700.00  ohms
     rs= 700.00  ohms          rsh=  23.31  ohms/sq      fc=   0.
  alpha=   0.                  vcr=   0.    volts     iirat=   0.
    rdc=   1.00  ohms          rsc=   1.00  ohms          n=   1.00
   vnds=  -1.00  volts

  6*** temperature effect parameters ***
   tlev=   0.                tlevc=   0.                 eg=   1.11  ev
   gap1= 702.00u ev/deg       gap2=   1.11k deg         xti=   0.
    bex=  -1.50                tcv=   0.    v/deg k      trd=   0.     /deg
    trs=   0.    /deg          cta=   0.    /deg         ctp=   0.     /deg

  7*** noise parameters ***
     kf=   0.                   af=   1.00              nlev=   2.00
 gdsnoi=   1.00

  ***  level  3  model parameters  ***

  delta=   1.16                eta=   0.               kappa= 200.00m /v
    nfs= 1.9e+12 1/cm**2     theta=   0.     /v         vmax= 100.00k m/sec
     xj=   1.89u meters         uo= 300.00 cm**2/vs       kp=  37.31u a/v**2
  deriv=   1.00
```

```
******    h s p i c e      h92b.02          11:00:35  27-JUL93   vax
* file: experimental design simulation #2
****** copyright 1990 meta-software,inc. *****site:rochester_tech
******  transient analysis                tnom=  25.000 temp=  25.000
******
```

| time | v(1) | 0. | 200.0000m | 400.0000m | 600.0000m | 800.0000m |
|---|---|---|---|---|---|---|
| (a ) | | + | + | + | + | + |
| 0. | 0. | -a | | | | |
| 1.0000u | 198.990m | | a | | | |
| 2.0000u | 355.171m | | | a | | |
| 3.0000u | 472.605m | | | a | | |
| 4.0000u | 560.044m | | | a | | |
| 5.0000u | 628.346m | | | a | | |
| 6.0000u | 677.783m | | | a | | |
| 7.0000u | 715.184m | | | a | | |
| 8.0000u | 740.529m | | | a | | |
| 9.0000u | 758.182m | | | a | | |
| 10.0000u | 769.808m | | | | | a |
| 11.0000u | 777.588m | | | | | a |
| 12.0000u | 781.801m | | | | | a |
| 13.0000u | 783.736m | | | | | a |
| 14.0000u | 784.078m | | | | | a |
| 15.0000u | 783.402m | | | | | a |
| 16.0000u | 781.863m | | | | | a |
| 17.0000u | 779.774m | | | | | a |
| 18.0000u | 777.383m | | | | | a |
| 19.0000u | 774.799m | | | | | a |
| 20.0000u | 772.084m | | | | | a |
| 21.0000u | 769.283m | | | | | a |
| 22.0000u | 766.495m | | | | | a |
| 23.0000u | 763.715m | | | | a | |
| 24.0000u | 760.978m | | | | a | |
| 25.0000u | 758.268m | | | | a | |
| 26.0000u | 755.637m | | | | a | |
| 27.0000u | 753.055m | | | | a | |
| 28.0000u | 750.552m | | | | a | |
| 29.0000u | 748.099m | | | | a | |
| 30.0000u | 745.731m | | | | a | |
| 31.0000u | 743.417m | | | | a | |
| 32.0000u | 741.184m | | | | a | |
| 33.0000u | 739.002m | | | | a | |
| 34.0000u | 736.898m | | | | a | |
| 35.0000u | 734.844m | | | | a | |
| 36.0000u | 732.865m | | | | a | |
| 37.0000u | 730.932m | | | | a | |
| 38.0000u | 729.070m | | | | a | |
| 39.0000u | 727.253m | | | | a | |
| 40.0000u | 725.503m | | | | a | |
| 41.0000u | 723.794m | | | | a | |
| 42.0000u | 722.149m | | | | a | |
| 43.0000u | 720.543m | | | | a | |
| 44.0000u | 718.996m | | | | a | |
| 45.0000u | 717.487m | | | | a | |
| 46.0000u | 716.034m | | | | a | |
| 47.0000u | 714.615m | | | | a | |
| 48.0000u | 713.249m | | | | a | |
| 49.0000u | 711.917m | | | | a | |
| 50.0000u | 710.634m | | | | a | |

```
 51.0000u  709.381m +      +      +      +      +      +      +     +a     +
 52.0000u  708.176m +      +      +      +      +      +      +     +a     +
 53.0000u  706.999m +      +      +      +      +      +      +     a      +
 54.0000u  705.867m +      +      +      +      +      +      +     a      +
 55.0000u  704.761m +      +      +      +      +      +      +     a      +
 56.0000u  703.697m +      +      +      +      +      +      +     a      +
 57.0000u  702.659m +      +      +      +      +      +      +     a      +
 58.0000u  701.659m +      +      +      +      +      +      +     a      +
 59.0000u  700.684m +      +      +      +      +      +      +     a      +
 60.0000u  699.745m-+------+------+------+------+------+------+-----a------+-
 61.0000u  698.829m +      +      +      +      +      +      +     a      +
 62.0000u  697.947m +      +      +      +      +      +      +     a      +
 63.0000u  697.086m +      +      +      +      +      +      +     a      +
 64.0000u  696.258m +      +      +      +      +      +      +     a      +
 65.0000u  695.450m +      +      +      +      +      +      +     a      +
 66.0000u  694.671m +      +      +      +      +      +      +     a      +
 67.0000u  693.912m +      +      +      +      +      +      +     a      +
 68.0000u  693.181m +      +      +      +      +      +      +     a      +
 69.0000u  692.468m +      +      +      +      +      +      +    a+      +
 70.0000u  691.782m-+------+------+------+------+------+------+-----a+------+-
 71.0000u  691.112m +      +      +      +      +      +      +     a+     +
 72.0000u  690.467m +      +      +      +      +      +      +     a+     +
 73.0000u  689.839m +      +      +      +      +      +      +     a+     +
 74.0000u  689.233m +      +      +      +      +      +      +     a+     +
 75.0000u  688.642m +      +      +      +      +      +      +     a+     +
 76.0000u  688.074m +      +      +      +      +      +      +     a+     +
 77.0000u  687.519m +      +      +      +      +      +      +     a+     +
 78.0000u  686.985m +      +      +      +      +      +      +     a+     +
 79.0000u  686.464m +      +      +      +      +      +      +     a+     +
 80.0000u  685.962m-+------+------+------+------+------+------+-----a+------+-
 81.0000u  685.473m +      +      +      +      +      +      +     a+     +
 82.0000u  685.002m +      +      +      +      +      +      +     a+     +
 83.0000u  684.542m +      +      +      +      +      +      +     a+     +
 84.0000u  684.100m +      +      +      +      +      +      +     a+     +
 85.0000u  683.668m +      +      +      +      +      +      +     a+     +
 86.0000u  683.253m +      +      +      +      +      +      +     a+     +
 87.0000u  682.848m +      +      +      +      +      +      +     a+     +
 88.0000u  682.458m +      +      +      +      +      +      +     a+     +
 89.0000u  682.077m +      +      +      +      +      +      +     a+     +
 90.0000u  681.711m-+------+------+------+------+------+------+-----a+------+-
 91.0000u  681.353m +      +      +      +      +      +      +     a+     +
 92.0000u  681.009m +      +      +      +      +      +      +     a+     +
 93.0000u  680.674m +      +      +      +      +      +      +     a+     +
 94.0000u  680.351m +      +      +      +      +      +      +     a+     +
 95.0000u  680.036m +      +      +      +      +      +      +     a+     +
 96.0000u  679.732m +      +      +      +      +      +      +     a+     +
 97.0000u  679.436m +      +      +      +      +      +      +     a+     +
 98.0000u  679.151m +      +      +      +      +      +      +     a+     +
 99.0000u  678.873m +      +      +      +      +      +      +     a+     +
100.0000u  678.602m-+------+------+------+------+------+------+-----a+------+-
                    +             +             +             +             +

      ***** job concluded
       total cpu time          14.81 seconds
           job started at  11:00:35  27-JUL93
           job ended   at  11:01:10  27-JUL93
```