10-22-2001

Study of Tantalum nitride diffusion barrier films for coppper interconnect technology

Deepa Gazula

Study of Tantalum Nitride Diffusion Barrier Films for Copper Interconnect Technology

By

Deepa Gazula

Study of Tantalum Nitride Diffusion Barrier Films for Copper Interconnect Technology

by

Deepa Gazula

Deepa Gazula	10/22/01
	October 22, 2001

Study of Tantalum Nitride Diffusion Barrier Films for Copper Interconnect Technology

by

Deepa Gazula

A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Science

in Material Science and Engineering at the Rochester Institute of Technology

Approved by

Dr.Thomas Blanton
Scientist,
Eastman Kodak Laboratories,
Rochester, NY

Dr. Santosh K.Kurinec, Advisor
Department of Microelectronics Engineering
& Materials Science and Engineering
Rochester Institute of Technology,
Rochester, NY

Dr. Andreas Langner
Department of Chemistry & Materials
Science and Engineering
Rochester Institute of Technology,
Rochester, NY

Dr. Vern Lindberg
Department of Physics & Materials Science
and Engineering
Rochester Institute of Technology,
Rochester, NY

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACKNOWLEDMENTS

I express my deep sense of gratitude to Dr.Santosh Kurinec for her continuous guidance and motivation and for patiently answering all my questions during the course of this project. I am grateful to Dr.Dave Glocker and Dr. Vern Lindberg for helping with the Iontech Sputtering tool depositions. I acknowledge Dr.Tom Blanton and Dr.Vinnie Gupta for generous donation of XRD analysis and expertise. My sincere thanks to the Richard Battaglia, Dave Yackoff, Bruce Tolleson and Dr.Illingsworth for the facilities support. I appreciate Dr.Gabriel Braunstein for the RBS work and his discussions. I also appreciate the help of Jose Medina for the SEM pictures, Keith Udut for electroplating, Dilip kumar for the stress measurements and Fred Mathews for TEM analysis. I also acknowledge CVC-Veeco, Inc for allowing sheet resistance measurements. I am thankful to Dr. Andreas Langner for his guidance through out my masters program.

ABSTRACT

As technology progressed to ultra – large scale integration leading to smaller and smaller devices, there are continuous challenges in the fields of materials, processes and circuit designs. Copper is the interconnect material of choice because of its low electrical resistivity and high electromigration resistance. However, copper is quite mobile in silicon at elevated temperatures. Therefore, to prevent the diffusion of copper into silicon, a diffusion barrier layer that has fewer grain boundaries, good adhesion to Si and SiO_2, high thermal and electrical stability with respect to Cu is necessary. Tantalum nitride compounds have been investigated as potential barrier materials. TaN has a very high melting point of 2950°C. It is thermodynamically stable with respect to Cu and has good adhesion to the substrate. It has a dense microstructure and shows good resistance to heavy mobility of Cu in Si and has electrical stability at temperatures upto 750 °C.

The diffusion barrier properties of Ta and its nitrides for copper metallization at RIT have been investigated. The TaN_x films were reactively sputter deposited on SiO_2 substrates at various N_2/Ar ratios. The influence of nitrogen partial pressure on the electrical and structural properties of the films is studied. It has been observed that as-deposited pure Ta is tetragonal, which becomes bcc-Ta with small increase in N_2 flow to 5% of the sputtering gas mixture. When the nitrogen flow is increased from 12 up to 20%, amorphous and a mixture of amorphous and crystalline Ta_2N phase is formed. The amorphous phase crystallizes when annealed to higher temperatures. An fcc- TaN phase is formed at N_2 flow of 30%. At higher concentrations of N_2, nitrogen rich compounds like Ta_5N_6, Ta_3N_5 are formed.

During backend semiconductor processing, both Cu and TaN films are subjected to various annealing treatments in N_2, O_2, and Ar at relatively high temperatures. Since these treatments influence the stability of the metallization it was important to establish the effect of the ambients on the integrity of the copper interconnect. The Cu/TaN/SiO_2 films were annealed to various temperatures up to 600 °C in N_2, Ar ambients for 20 min and the thermal stability and barrier effectiveness of the films was studied. Annealing the films to temperatures above 500 °C cause de-lamination of films at the Cu/TaN interface,

which is attributed to the formation of copper oxides with a high density of voids. This was observed by XRD analyis and SEM. RBS spectra showed diffusion of tantalum into the surface of copper at temperatures ~ 500 to 600 ^{o}C. Therefore we can conclude that cubic TaN films act as stable barrier films upto 500 ^{o}C in an inert ambient.

1. COPPER METALLIZATION – AN OVERVIEW

1.1 INTRODUCTION

An integrated circuit (IC) or a chip is a group of discrete electrical devices such as transistors, diodes, resistors, capacitors or inductors manufactured simultaneously on a single substrate material and electrically connected to one another. The process of connecting these devices to each other and to the substrate by using conducting materials is known as metallization. The highly conductive material called the interconnect carries electrical signals to different parts of the substrate. The performance of an integrated circuit depends on the interconnect performance as much as the individual components. This requires efficient signal transmission with minimum propagation delays and power dissipation and low loss transitions between the interconnection and intrinsic devices.

Technology has progressed to ultra large-scale integration (ULSI) with more than one million circuit elements on a single chip. This increase in complexity of ICs has called for development in the interconnect technology. While materials other than metals have been used as interconnects, the term 'metallization' is generic in nature and is derived from origins of interconnect technology where metals were the first conductors used. Currently, several layers of materials stacked on top of one another are used to form the conducting connection between devices. This process is called multi – layered metallization.

For many years, aluminum and its alloys have been the industry's choice for metallization because of its low resistivity. However as devices continue to shrink and interconnect cross-sections get smaller, a high performance interconnection network is necessary to match the performance of the devices they interconnect. Such demand is reflected not only in the fundamental characteristics of the materials used but also in their processing and reliability at sub-quarter-micron dimensions.

1.2 ISSUES IN METALLIZATION

The miniaturization of interconnect feature size severely penalizes the overall performance of the interconnect, such as increasing interconnect resistance and current densities, which lead to reliability concerns due to electromigration. With high interconnect resistance, the RC time delay will also increase. Therefore, metals with low resistivity are preferred.

1.2.1 ELECTROMIGRATION

Electromigration is the current induced transport of conducting material. The decrease in thickness and width of the interconnects increases current density through the lines. In the presence of high current stresses, electron momentum is transferred to atoms in the conducting material, increasing their mobility and yielding a net atomic flux. This net flux causes conducting material to be depleted ``up wind" and accumulated "`down wind" as seen in figure 1.1.

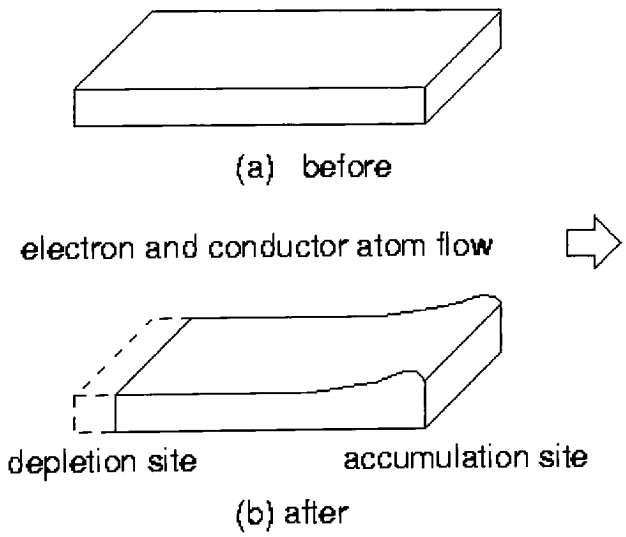


Figure 1.1: Simplified schematic of electromigration effect on metal interconnect segment [1]

Regions where the interconnect material has been depleted will form a *void*, leading to interconnect failure due to the formation of an open-circuit. Likewise, interconnect material can also accumulate and extrude to make electrical contact with

neighboring interconnect segments, potentially leading to circuit failure due to the formation of a *short circuit*. Either outcome can contribute to the gradual ``wearing out'' of current- stressed interconnects over time. Electromigration can lead to the breaking of interconnections and collapse of integrated circuits at large.

The atomic flux due to electromigration J_{atoms}, in a single crystal or large-grained crystal, where the grain-boundary contribution to atomic diffusion can be neglected, is given as

$$J_{atoms} = NDZ^{*}qj / (r\,kT) \qquad \text{---------- (1)}$$

where N, D, Z*, q, j, r, k, and T are atomic density, atomic diffusivity, effective charge on the moving ions, electron charge, current density, electrical conductivity, Boltzmanns constant, and temperature in degree K respectively. [2]

The diffusion of metal atoms in polycrystalline materials predominantly occurs along grain boundaries that usually have higher diffusivities than the grain lattice. This current induced diffusion can lead to void and hillock formation. Void formation can lead to an open circuit, while a hillock, which extends to make contact with another interconnect line, can lead to a short circuit. Either of these will lead to circuit failure. The failure rate is often modeled empirically, with the following equation for the Median Time To Failure (MTTF):

$$MTTF = A\,J^{-n} \exp(E_A/kT) \qquad \text{---------- (2)}$$

where J is the current density, n is typically close to 2, and A is a constant, which depends on film structure (grain size, etc.) and processing. E_A is the activation energy for electromigration and is often associated with grain boundary diffusion (the activation energy of lattice diffusion in bulk aluminum films is about 1.4 eV while it is 2.19 eV for copper). The parameters for this equation are usually determined under accelerated testing conditions that employ higher than normal current and temperature. Accelerated testing is also used to predict when shorts or opens occur in the interconnect lines or when the line resistance reaches a critical value.

Electromigration can be reduced by increasing the grain size of the interconnect material, thus reducing the grain boundary density or by reducing

diffusion across the grain boundary by addition of solute atoms, or by choosing an alternative metallization scheme – with the replacement of aluminum with copper.

1.2.2 RC DELAY

As the feature size decreases, there is an increase in chip size. This causes an increase in length of the interconnects, leading to higher resistance. There is a decrease in the distance between adjacent interconnects leading to an increase in capacitance between them although there is a decrease in capacitance between the interconnect and ground substrate, resulting in an increase in the total interconnect capacitance at the submicron range. Since both line resistance, R and capacitance, C associated with the dielectric contribute to interconnect delay, the total interconnect delay increases rapidly. As devices become smaller, RC delay will increase the carrier transient time, which will be a major obstacle to increasing the speed of the chips.

The RC delay is given by $RC = \rho L^2 \varepsilon_{ILD} / t_M t_{ILD}$ ---------- (3)

where ρ, L and t_M are the resistivity, length and thickness of the interconnect, and ε_{ILD} and t_{ILD}, the permittivity and thickness of the interconnect dielectric (ILD) respectively.[2] It is estimated that in the sub-micron range the total interconnect delay increases rapidly with decrease in feature size as shown in figure 1.2.

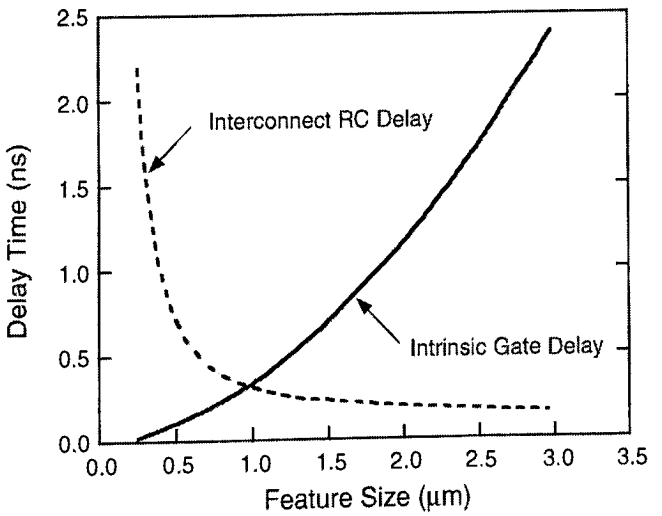


Figure 1.2: Delay time vs. Feature Size

There are two solutions to overcome this problem. One approach is to lower the capacitance by using low permittivity materials (also called as '*low k dielectrics*') as interlevel dielectrics. The other is to use interconnect materials with lower resistivity.

1.3 NEED FOR A NEW METALLIZATION

Aluminum has been commonly used as metallization material as it meets most of the metallization requirements for LSI device:

- it has a relatively low electrical resistivity.
- it has halide compounds with a relatively high pressure, which are suitable for reactive ion etching (RIE).
- it can form a thin protective oxide film that withstands various thermal process and has a good adhesion to oxide.
- it has a good step coverage.
- it is an inexpensive material.

For sub 0.5 μm technologies, aluminum deposited or reflowed at temperatures exceeding 450 °C is a means to achieve planarization. Usually, a layer of diffusion barrier is needed to prevent diffusion of Al into Si. The high temperatures involved during deposition place a stringent demand on the integrity of the barrier to prevent junction spiking caused by Al/Si interdiffusion [21]. TiN is presently considered to be the barrier material of choice for sub-0.5 μm metallization. For metallization of VLSI circuits, Al suffers from major limitations that are due to both properties of the metal and deposition techniques. One of the most important reliability problems is electromigration discussed in section 1.2.1. For the development of ultra-large scale integration (ULSI), the electrical resistivities of Al and its alloys are not low enough. As the minimum geometry is scaled down to one-quarter micron, Al and its alloys will be replaced by other interconnect materials.

An interconnect material should meet the following requirements:

- Low resistivity
- Void free deposition on high aspect ratio trenches and vias
- High deposition rate and easy control of microstructures
- Ease of patterning and planarization
- Good adhesion to interlayer dielectrics and other materials on a chip
- Low reactivity with environment, and
- Low stress and high resistance to electromigration and stress induced voiding

The new materials that were considered for metallization are gold, silver and copper. The material properties of these materials are listed in table 1.1 [3]. Gold has highest resistivity among them. Silver has the lowest resistivity, but it has poor electromigration resistance. Copper is a promising material because of its good electrical and mechanical properties.

	Cu	Al	Au	Ag
Resistivity (μΩ cm)	1.67	2.66	2.35	1.59
ΔR/ Δ T at 0 – 100 °C (10 – 3/K)	4.3	4.5	4.0	4.1
Melting Point (K)	1083.4	660.1	1063	960.8
At. Wt (amu)	63.54	26.982	196.967	107.868
Youngs Modulus (GPa)	129.8	70.6	78.5	82.7
Yield Strength (MPa)	216	55	130	172
Hardness (HV)	51	1.5	20-30	25
Do (cm^2/s) at 100 °C	0.78	1.71	0.67	1.89
Activation Energy (eV) for diffusion	2.19	1.48	1.96	2.01
D Diffusivity (cm^2/s) at 100 °C	2.1×10^{-30}	2.1×10^{-20}	2.2×10^{-27}	1.1×10^{-26}
Delay ($ps\ mm^{-1}$)	2.2	3.7	3.2	2.2
Thermal Conductivity (W/cm)	3.98	2.38	3.15	4.25
Deposition and Etching				
Sputtering	Yes	Yes	Yes	Yes
Evaporation	Yes	Yes	Yes	Yes
CVD	Yes	Yes (?)	?	?
Plating	Yes	?	Yes	Yes
Wet Etch	Yes	Yes	Yes	Yes
Dry Etch	?	Yes	?	?
Electromigration resistance	High	Low	High	Very low
Corrosion resistance in air	Low	High	Very high	Low

Table 1.1: Comparison of Material Properties

1.4 COPPER METALLIZATION

Resistivity of Cu is about 40% less than that of Al. It has high electromigration resistance. The self diffusion of copper is also the smallest among the four elements, resulting in improved reliability. Although a lot of research has been done on copper in the last several years, only recently has the industry begun to consider it as a feasible production technology. The IBM CMOS 7S technology illustrated in figure 1.3 was the first process to integrate Cu in a CMOS technology. [4]

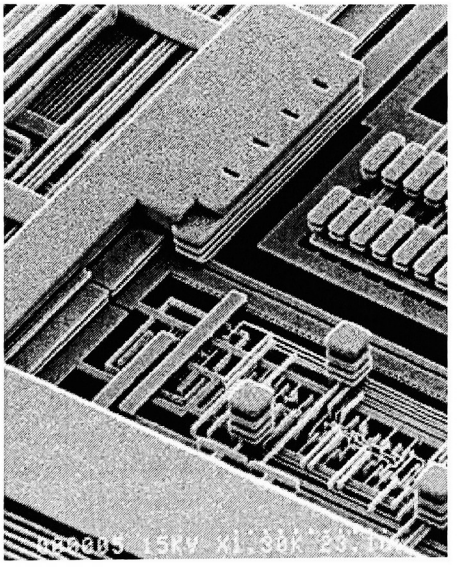


Figure 1.3: CMOS 7S - ASIC showing six levels of copper

Cu metallization has the following advantages:

- **Reduced RC time delay**

Cu has a lower resistance that that of Al. Therefore, RC time delay is reduced enabling the signals to move faster.

- **Increase in packing density and computing power**

Since Cu is a better conductor of electricity compared to Al, Cu interconnections can be made narrower to 0.1 microns instead of 0.25 microns. Hence, the packing density will be increased. It is possible to have 150 200 million of transistors on a single chip. Subsequently, there will be an increase in computing power as well.

- **Reduced power consumption**

Cu lines can be made thinner to execute the same function as Al. As the films get thinner, the capacitance on the chip, which is primarily sidewall capacitance between the adjacent lines of Cu is less. This helps to reduce the amount of power consumption if thin Cu lines are combined with a moderately low-k dielectric.

- **Superior resistance to electromigration**

As wiring linewidths decrease, current density carried by those lines, which is the driving force for electromigration, increases. However, Cu has a superior resistance to electromigration when compared to Al. It is reported that the electromigration lifetime for Al is in orders of magnitude higher than that of Cu. This is important for ICs used in non-temperature-regulated environments.

- **Prevent circuits from overheating**

Cu is also a better conductor of heat. It can prevent damage to the circuits from overheating. This has also made it possible to have close packing of transistors.

1.4.1 DISADVANTAGES OF COPPER

Copper is a fast diffuser in silicon. It can form three acceptor levels in the middle of silicon band gap at 0.24eV, 0.37eV and 0.52eV with respect to the valence edge. These deep energy levels provide a mechanism for excess minority carriers recombining with majority carriers [5]. Consequently, Cu will induce generation-recombination leakage current in p-n junctions and jeopardize the performance of bipolar transistors, leading to a reduction in current gain. Copper induced leakage current can also limit the performance of light detector that converts a photo flux to a charge packet or electric current. A high concentration of Cu near the Si – SiO_2 interface can result in a high concentration of surface states.

Copper forms silicides, Cu_3Si, by reacting with the substrate at temperature less than 200°C. After the formation of the Cu_3Si phase, the underlying silicon in the Cu_3Si/Si structure is readily oxidized even at room temperature, resulting in rapid growth of a layer of SiO_2 upto a few micrometers in thickness. [6]

Unlike the case of aluminum which forms a passivating oxide layer, copper is readily oxidized to form a Cu_2O and CuO phases at temperatures above 100 °C and no self protective oxide layer forms to prevent Cu from further oxidation. The oxidation rate depends on the orientation of copper surface. The most likely orientation planes are (100), (111) and (110), with the (100) plane having the highest oxidation rate. The lack of self-passivation makes a copper thin film susceptible to oxidation during processing. If copper is oxidized, the resistance of Cu interconnects increases rapidly. Therefore, Cu should not be exposed to air at high temperatures at any stage.

Copper reacts at low temperature with most metals, such as Al, Au and Pd, which are commonly used in microelectronic devices. $CuAl_2$ can be formed in a Cu/Al bilayer structure. At 150 °C, Cu reacts with Au to form CuAu, Cu_3Au and reacts with Pd to form Cu_3Pd compound at 200 °C.

Copper also reacts readily with most silicides, such as $CoSi_2$, $CrSi_2$, and $TiSi_2$, at temperature below 450 °C. Cu can diffuse through $CoSi_2$ to form Cu_3Si at the $CoSi_2/Si$ interface while the integrity of $CoSi_2$ layer is maintained. In the $Cu/CrSi_2/Si$ system, Cu_3Si forms on top of $CrSi_2$, due to silicon migration, to react with overlying Cu. Cu can induce partial decomposition of $TiSi_2$ to form Cu_3Ti and Cu_3Si in the $Cu/TiSi_2/Si$ structure.

Copper layers exhibit poor adhesion on both silicon dioxide and polymer substrate. In general, interfacial adhesion is strongly related to the bonding, surface morphology, and stress relaxation at the Cu/substrate interface. Annealing a Cu film on a SiO_2 substrate causes the film to peel under tensile stress. When copper contacts a polymer, such as polyimide, copper forms a weak chemical bond with polyimide and diffuses into it to form agglomerates at low temperature. However, it has been reported that sputtered copper films, deposited on clean and moisture free surfaces in equipment pumped down to a very high vacuum of $10^{-6} - 10^{-7}$ Pa show reasonable adhesion to both SiO_2 and polymer films. Most of them pass the Scotch tape peel test

in the as-deposited condition, but on annealing at higher temperatures, peeling is observed. The latter effect is related to the difference in thermal expansion coefficients of SiO_2 and Cu.

To avoid aforementioned problems, diffusion barrier, passivation layer, and adhesion promoter are needed. The ultimate objective is to find a diffusion barrier material between copper and the interlayer dielectrics that will also perform as an adhesion promoter. Fortunately, there are many diffusion barriers that are also good adhesion promoters.

1.4.2 PATTERNING OF COPPER

Copper is difficult to etch. The main difficulty of using conventional plasma etching to pattern Cu is the lack of Cu compounds that are volatile at low temperatures. Wet etching and lift-off techniques, used in a research environment, are inadequate for submicron geometries.

1.4.2.1 Wet etching

Copper can be attacked by various chemicals that can be used for etching. One example is an aqueous solution of ammonium persulfate and ammonium chloride. A mixture of 500 cc deionized water, 45 gm ammonium persulfate and 3 gm ammonium chloride etches copper at the rate of about 1000 nm/min. Since wet etch is an isotropic process, there is large undercutting making precise control of line width impossible. Therefore, wet etch is not suitable for submicron copper metallization.

1.4.2.2 Plasma etching

Plasma etching is the most widely used method for patterning Al-alloys. It has several advantages over wet etch. It gives anisotropic etching, which minimizes undercut, and there is a good control of the etching rate and time.

It is difficult to do plasma etching of copper because the copper halides are not volatile at low temperatures. Various chlorine-based chemistries have been attempted for Cu dry etch because copper chlorides have the highest vapor pressure among Cu halides. However, the wafer needs to be heated to 224-280 ^{o}C to achieve a sufficiently high etch rate, which is incompatible with the conventional photoresist materials.

1.4.3 CHANGES IN PROCESS TECHNOLOGY WITH COPPER METALLIZATION

Copper has a superior resistance to electromigration, which is a common reliability problem in aluminum lines at the deep submicron level. This means that copper can handle higher power transistors, which broadens its application to a whole new range of analog devices.

The main challenges of Cu interconnects are difficulties in line patterning and potential device contamination. These problems are overcome by use of barrier layers between Cu and the substrate and a new strategy called the *damascene* or 'inlaid' patterning to form the interconnect lines. The damascene approach requires 20-30% fewer steps than traditional subtractive patterning (by etching). This also reduces the cost of manufacturing.

The second way copper can reduce costs is that because smaller lines can be used to carry the same amount of current, a tighter packing density can be achieved per level. This means that fewer levels of metals are needed, which leads to a significant decrease in manufacturing costs.

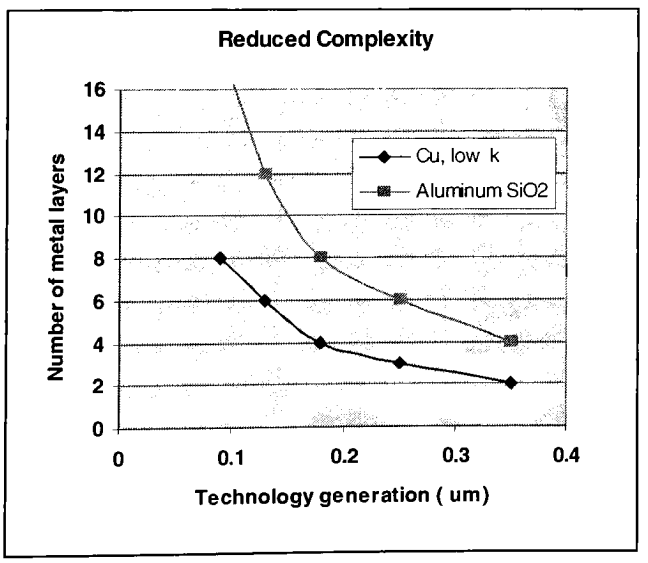


Figure 1.4: Plot of No. of metal layers vs. Feature Size

1.5 DIFFUSION BARRIERS

Diffusion barriers are thin film layers used to prevent two materials from coming into direct contact in order to avoid reactions between then. Ideally, a barrier layer X sandwiched between A and B should possess the following attributes. [7]

- It should constitute a kinetic barrier to the movement of A and B across it. i.e., the diffusivity of A and B in X should be small
- It should be thermodynamically stable with respect to A and B at the highest temperature of use. Further, the solubility of X in A and B should be small.
- It should adhere well to and have low contact resistance with A and B and possess high electrical and thermal conductivity. Practical considerations also require low stress, ease of deposition and compatibility with other processing

A large number of materials have been investigated for use as barrier layers between silicon and copper. A consideration for the choice of diffusion barrier is that it be metallurgically stable with respect to the metal that carries current. This is an easy condition to meet for copper, since many refractory metals do not form copper compounds. However, copper may penetrate through a metal without reacting with it. Selection of such a material starts with an investigation of mutual diffusivity and interactions. Since diffusivity is directly related to melting point of the material, the best diffusion barriers have the highest melting point. Also, the high activation energies associated with diffusion through refractory metals is the dominant factor. Refractory metals like titanium, tantalum and tungsten and their nitrides, carbides, silicides and borides act as good barrier layers.

We see from table 1.2 [18] that the melting temperature and the heat of formation of nitrides is higher than that of silicides, whereas the electrical resistivity and schottky barrier are comparable. It is due to their superior thermal stability that refractory nitrides have potential applications in microelectronics.

Property	TiN	$TiSi_2$	TaN	$TaSi_2$
Crystal structure	fcc	orthorhombic	Hex.	Hex.
T_m – Melting temp (°C)	2950	1500	2950	2200
ΔH°_{298} - Enthalpy of formation (kcal/mol)	-80.4	-32.1	-60.3	-28.5
ρ- Resistivity (μΩcm)	20-70	15-25	135-250	10-50
ϕ_{Bn} Barrier height	0.49	0.6		0.59

Table 1.2: Comparison of refractory nitrides and silicides

Single transition metal films are usually polycrystalline. They are stable as barrier between Cu and Si to temperatures of around 500 °C (for Pd, Cr and Ti) to 650 °C (for Ta). Cu reacts with near noble metals such as Cr, Co, Ni, Pd and Pt in the temperature range of 250 °C to 450 °C but is non-reactive and immiscible with refractory metals such as Mo, Ta and W. The near- noble metals also react with Si to form silicides at low temperatures between 100 – 450 °C, while the refractory metals do not react up to 525 – 650 °C. The failure mechanism is usually due to the high reactivities of barrier metal – Cu or Si – barrier metal, followed by Cu –Si reaction for the metals in the first group and diffusion of Cu through grain boundary of the polycrystalline barrier films at relatively low temperature for the metals in the second group. So, transition metals are not stable diffusion barriers between Cu and Si. [8]

The effectiveness of silicides or transition metal – silicon systems as diffusion barriers follows a trend similar to that of their corresponding transition metal diffusion barriers, but the silicides are better by 100 to 200 °C. The diffusion barriers formed by refractory metal (Ta and W) – Si are most stable upto 450 to 700 °C than those by near noble metal (Cr and Co) – Si barrier which are stable only to about 300 °C. Adding silicon to refractory metals to form an amorphous refractory metal – Si diffusion barrier also improves barrier performance. The barriers fail by the reaction of Cu with the silicide barriers to form Cu – silicide, by Cu diffusion through

polycrystalline transition metal silicides, or by Cu – induced premature crystallization of the amorphous metal silicon barrier films.

The metal – nitrogen systems of Ti – N, Ta- N and W N show a high stability as diffusion barriers. This is due to the non-reactivity of Cu with N, Ta and W. Barrier failure is caused by the diffusion of Cu along the grain boundaries or through defects generated at elevated temperature in the barrier films, which are relatively intact, or by reaction between barrier films and Si to form metal – rich silicides. [8]

1.6 BARRIER MATERIALS

The following are the commonly used barrier materials between copper and silicon.

1.6.1 TANTALUM

Tantalum is a greyish silver, heavy, and very hard metal. It has a melting point exceeded only by tungsten and rhenium. The bulk properties of tantalum are listed in table 1.3 and compared with other refractory materials.

Ta is stable as a barrier up to 600 deg C. Among six transition metals of Cr, Ti, Nb, Mo, Ta and W, only Ta and W retain their interface with Cu after annealing at 600 ^{o}C for 1 hour. At higher temperatures, a complex reaction occurs that involves the motion of all three elements. Cu permeated the Ta film to form Cu_3Si precipitates at the Ta-Si interface, and the Ta reacted with the Si substrate to form a planar layer of hexagonal – $TaSi_2$.

The stable state of bulk Ta has a bcc structure with a lattice parameter of 3.298 A^{o}. However, a thin sputtered Ta film typically has a metastable β - Ta structure that has a tetragonal crystal structure. Heteroepitaxial growth of Cu *in-situ* deposited on β Ta has been reported [27]. The [220] direction of Cu (111) plane is observed to line up with the [330] direction of β Ta (002) plane with a misfit strain of 7.6%. As a result, Ta has better adhesion with Cu and results in a stronger Cu texture than TiN. Although Ta is typically deposited by sputtering, plasma assisted chemical vapor deposition (CVD) has also been explored.

1.6.2 TANTALUM NITRIDES

The barrier properties of Ta can be further improved by the addition of impurities to the film. If the solubility limit is exceeded, solute atoms in a Ta grain would be expected to segregate to the grain boundaries, obstructing these fast pathways for copper diffusion.

Property	Ti	TiN	Ta	TaN
Melting point (deg C)	1668	2930	3014	3087
Thermal coefficient of Expansion (deg C)	8.6×10^{-6}	9.4×10^{-6}	6.5×10^{-6}	5.6×10^{-6}
Electrical Resistivity (μ-ohm cm)	40	1100-1800 (depends on %N)	14.7	160 (for 20% N)
Thermal conductivity (cal/sec -cm-degC)	0.22	0.544	0.046	
Stresses in Cu/x/SiO_2 x- Diffusion barrier	Tensile	Compressive	Compressive	Compressive
Barrier Stability Temp of Cu/Si/SiO_2 (deg C)	450	550	600	650-750
Methods of deposition Sputtering	yes	yes	yes	yes
Physical Vapor Deposition (PVD)	Yes for Al No for Cu	Yes for Al No for Cu	Yes for Al No for Cu	Yes for Al No for Cu
Chemical Vapor Deposition (CVD)	Same as PVD	Same as PVD	Same as PVD	Same as PVD
Activation energy (eV)	Al-Ti: 1.8 Cu-Ti: 3.2	Al-TiN: 1.2 Cu-TiN: 2.5	Al-Ta: 2.3 Cu-Ta: 1.5	Cu-TaN: 4.4
Phases	hcp	bcc-polycrystalline, columnar	bcc-β Ta columnar-	Crystalline fcc, amorphous

Table 1.3: Comparison of properties of various barrier materials

For a nitrogen concentration between 10 – 20 %, Ta_2N is present along with bcc- Ta phase. An amorphous component appears at around 15 %. The structure of tantalum nitrides can be described as close-packed arrangements of Ta atoms with N atoms inserted in interstitial sites. The space group of Ta_2N is P63/mmc, with equal number of sites for Ta and N atoms, while the nitrogen atoms occupy half of the sites randomly. However, deviations from this occupancy ratio can occur, which explains the finite range of existence of Ta_2N.

It has been reported that tantalum nitrides have better barrier properties than Ta or TiN. TaN is stable with Cu up to 750 °C. In PVD TaN, the phases of TaN_x changes from β Ta to bcc- Ta, then amorphous Ta_2N, and non-crystalline TaN to cubic TaN with the increase of N_2 flow. The superior barrier properties of TaN over Ta are due to the stable TaN compounds. CVD TaN has better step coverage than PVD TaN, but the deposition temperature of CVD TaN is 450-650 °C that is too high for back-end processes.

1.6.3 TANTALUM-SILICON-NITRIDE

Ta-Si-N has an amorphous structure. Since Cu diffusion is faster through grain boundaries than through crystal bulk lattice in barrier layer, an amorphous layer has superior diffusion barrier property over a polycrystalline layer. Ta-Si-N is stable as a barrier upto 900 °C. The crystallization temperature is higher than 1000 °C, but the barrier fails at around 900 °C by premature crystallization when Ta-Si-N is in contact with Cu. Under identical sputtering conditions, Ta-Si-N films have superior step coverage over TiN. However, compositional variation is a concern for Ta-Si-N films in trenches and vias.

1.6.4 TUNGSTEN NITRIDES

Although Ta-based materials have good barrier properties on Cu, Chemical Mechanical Planarization (CMP) of Ta without damaging Cu is very difficult. During the Ta CMP, dishing and over etching of Cu are very significant. Compared to the Ta-based barrier layer, WN_x is more appropriate for CMP. WN_x CMP can be performed nicely even with the same chemicals used in Cu CMP. Furthermore, plasma enhanced CVD is available for WN_x, which gives excellent coverage. W_2N is stable as a barrier upto 790 °C, while WN is stable upto 500 °C. The resistivity of WN_2 is about 210 μΩ

cm. However, a major concern of WN_x in Cu metallization is the poor adhesion of Cu on WN_x films.

1.7 DAMASCENE PROCESSING

The practice of creating patterns by metal inlays was first developed by the ancient artisans of Damascus. A similar process called *Damascene processing* is being adopted by the semiconductor industry to create interconnect lines by first etching a trench or canal in a planar dielectric layer, and then filling that trench with a metal. In *dual damascene processing* (figure 1.5), a second level is involved where a series of holes (i.e., contacts or vias) are etched and filled in addition to the trench. After filling, the metal and dielectric are planarized by chemical mechanical polishing (CMP).

The main advantage of damascene processing is that it eliminates the need for metal etch. This is very useful because copper is difficult to etch. A second advantage is that it eliminates the need for dielectric gap fill. [10]

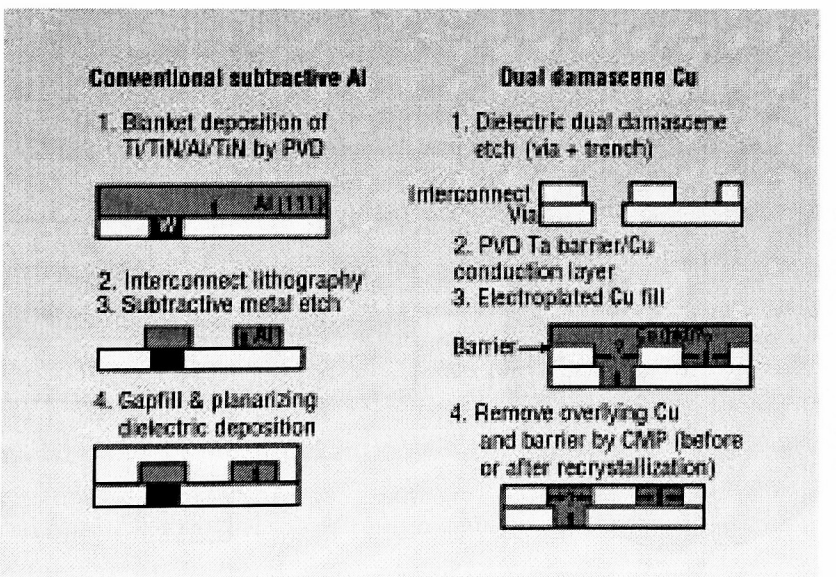


Figure 1.5: Dual Damascene Processing

1.8 CHEMICAL MECHANICAL PLANARIZATION (CMP)

As the semiconductor dimensions continue to shrink, modern photolithography equipment approaches its depth of field limits. Slight irregularities on the wafer surface or on deposited films can distort semiconductor patterns as they are transferred by a lithographic process to the wafer surface. Chemical Mechanical Planarization has evolved as the preferred method for preventing distortion.

This involves planarizing the wafer surface to a flat, uniform finish by use of an abrasive suspended in a chemical slurry and a circular (sanding) action as shown in figure 1.6. Conventional systems apply the slurry with rotating disks above and below the wafer. When the wafer is uniformly planar, photolithographic patterns can be transferred with minimal distortion. In complex semiconductors with multiple interconnect layers, CMP systems are used after each conductive or dielectric layer has been deposited to prepare it for the next photolithographic step.

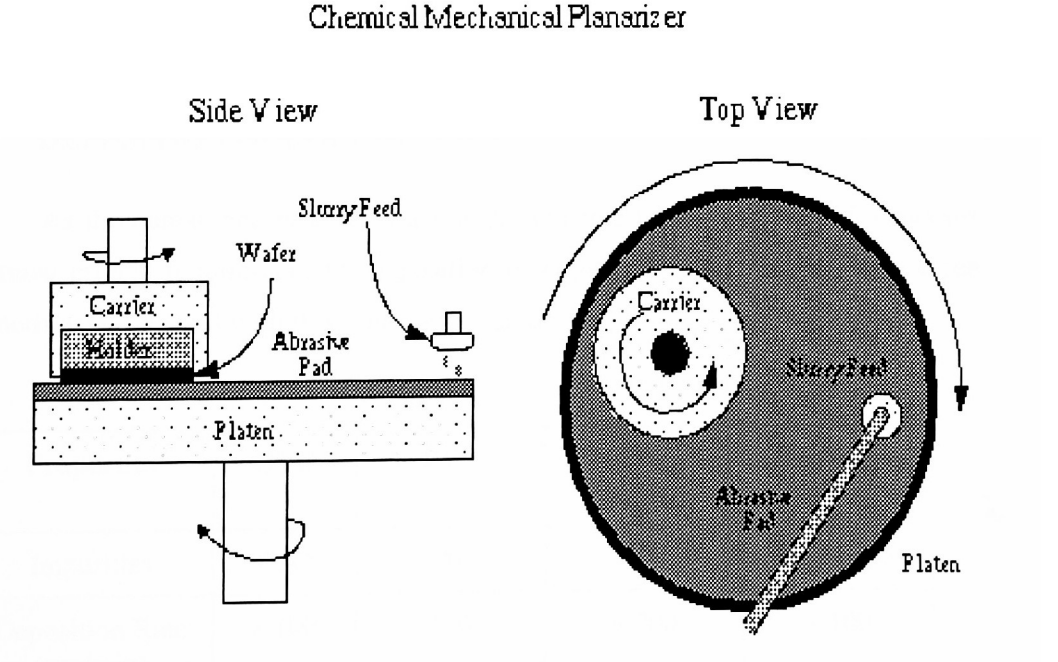


Figure 1.6: Schematic of a CMP set up

1.8.1 CMP OF COPPER

Planarizing copper is as challenging as the process of depositing copper for damascene interconnect structures. Copper CMP for damascene structure involves developing a polish process that minimizes the pattern density and feature size effects associated with typical CMP processes. Development is complicated by new barrier materials, lack of commercial slurries and the material properties of copper itself.

Copper is a material that is difficult to polish. It is soft and subject to scratching and embedded particles during polishing. Also because copper is highly electrochemically active and does not form a natural protective oxide, it corrodes easily. Therefore, protecting the copper surface during polish, clean and subsequent processing is essential.

Copper CMP is also more complex because of the need to remove the barrier layer and copper uniformly without overpolishing any features. This is difficult because current copper deposition processes are not as uniform as the oxide deposition processes.

1.9 DEPOSITION OF COPPER

As the damascene process is adopted, void free trench and via – fill become the most critical requirement for deposition of copper. In table 1.4 four deposition methods are compared with this criterion in mind.

Properties	CVD	PVD	Electrolytic plating	Electroless plating
Impurities	C, O	Ar		Seed Layer
Deposition Rate (nm/min)	» 100	100	» 200	~ 100
Process Temperature (°C)	» 250	Room	Room	50 – 60
Step Coverage	Good	Fair	Good	Good
Via-Filling Capacity	Good	Poor	Fair	Fair

Waste	Good	Good	Poor	Poor
Cost	High	High	Low	Low

Table 1.4: Comparison of various deposition techniques for Cu

1.9.1 PVD OF COPPER

Sputtering is an easy PVD method of depositing copper. The sputter yield of copper is among the highest of all the metals. At 600 V argon ion energy, the sputtering yield (atoms of copper deposited per ion of argon) of copper is reported to be 2.8, compared with 1.2 for Al and 0.6 for W.[3] For via filling, and planarization using biased sputtering, such high sputtering yields could be advantageous.

Conventional PVD techniques are not adequate for Cu deposition into high aspect ratio trenches because keyholes would from inside the trenches. The large angular distribution of sputtered atomic flux will pinch off Cu film at the top of the trenches during deposition. To overcome this problem, either high temperature reflow after sputtering or directional sputtering techniques such as ionized sputtering or magnetic field enhanced sputtering may be employed.

Although sputtering is not a suitable process for Cu interconnection, a thin sputtered Cu film can be used as a *'seed layer'* for other Cu deposition processes. The seed layer provides an atomically smooth and cohesive copper interface that encourages correct grain growth during the subsequent bulk copper fill step.

1.9.2 CVD OF COPPER

Chemical vapor deposition (CVD) has been extensively used in the ULSI technology due to its superior step coverage to physical vapor deposition. CVD is the formation of a single compound on a substrate by thermal reaction or decomposition of gaseous compounds, which contain the required constituents. For Cu CVD, metalorganic precursors are commonly used, i.e., MOCVD (Metalorganic Chemical Vapor Deposition), because it allows deposition at relatively low temperatures. Several metalorganic precursors have been explored for Cu deposition. Cu ^{II}(hfac)$_2$ and Cu ^{I}(hfac)(tmvs) are the two most extensively studied precursors. The *hfac*

represents hexafluoroacetylacetonate, and the *tmvs* represents trimethylvinylsilane. Properties of these Cu precursors are listed in Table 1.5.

	Cu ^{II}(hfac)$_2$	**Cu ^{I}(hfac)(tmvs)**
State	Solid	Liquid
Decomposition temp	> 200 °C	> 40 °C
Vapor Pressure	~ 10 Torr at 100 °C	~ 0.3 Torr at 40 °C
Reaction	Reducing agent required	Disproportionation reaction
Conversion to copper	Inefficient	Efficient
Deposition rate	~ 10 – 20 nm/min	~200 nm/min
Deposition temperature	~250-400 °C	~150-180 °C

Table 1.5: Properties of Cu ^{II}(hfac)$_2$ and Cu^{I}(hfac)(tmvs)

Cu ^{II}(hfac)$_2$ is a solid at room temperature. It exhibits good thermal stability, but its vapor pressure is not adequate at low temperatures (< 100 °C). Temperatures higher than 200 – 300 °C are required to get a reasonable deposition rate. The decomposition of Cu ^{II}(hfac)$_2$ to pure Cu requires reduction by hydrogen. The reaction is shown as follows:

$$Cu^{II}(hfac)_2\,(g) + H_2\,(g) \rightarrow Cu^{o} + 2Hhfac\,(g) \qquad \text{----------(4)}$$

The enthalpy for sublimation is 13.2 kcal/mole

Cu ^{I}(hfac)(tmvs) is a pale yellow liquid at room temperature. The deposition efficieny of Cu^{I}(hfac)(tmvs) is much higher than that of Cu ^{II}(hfac)$_2$, which allows deposition of Cu at lower temperatures and higher rates. At temperatures lower than 150 °C, the deposition rate is very low. Since film resistivity increases exponentially with temperature above 150 °C, 150 – 170 °C is the the optimum temperature range for Cu deposition. [13]

The deposition reaction steps on the heated wafer surface are as follows:

$2Cu^{I}(hfac)(tmvs)\ (g) \rightarrow 2Cu^{I}(hfac)(tmvs)\ (s)$

$2Cu^{I}(hfac)(tmvs)\ (s) \rightarrow 2Cu^{I}(hfac)\ (s) + 2(tmvs)\ (g)$

$2Cu^{I}(hfac)\ (s) \rightarrow Cu^{o}(hfac)\ (s) + Cu^{II}(hfac)\ (s)$

$Cu^{o}(hfac)\ (s) + Cu^{II}(hfac)\ (s) \rightarrow Cu^{o}\ (s) + Cu^{II}(hfac)_2\ (s)$ ----------(5)

Physical vapor depositions are different from chemical vapor depositions in the deposition mechanism. The deposition rate for CVD will be proportional to the deposition temperature. However, the deposition rate for PVD will generally decrease with increasing deposition temperature.

1.9.3 ELECTROLESS PLATING

During the early stages of Cu process development, electroless plating of copper drew attention because it offers a simple and cheap process and the possibility of selective deposition which may ease line definition.

In electroless deposition, Cu atoms are supplied to the film surface by catalytic reduction of aqueous ions. Since electrons for Cu reduction are provided by oxidation of the reducing agent in the deposition bath, and this oxidation is catalyzed only at conductive surfaces, electroless Cu deposition is inherently selective on conductive surfaces. A typical Cu electroless process is

$Cu^{+2} + 2HCHO + 4OH^{-} \rightarrow Cu^{0} + H_2 + 2HCOO^{-} + 2H_2O$ ----------(6)

where copper ions are supplied from the copper sulphate ($CuSO_4.5H_2O$) solution.

The growth of electroless Cu is highly dependent on the seed layer. Cu nucleation is very poor on Ti. The adhesion is poor on W. On TiN, either island deposition or rough surface is formed. Pd_2Si is an excellent seed layer for electroless Cu deposition. A thin sputtered or CVD Cu layer is perhaps the best seed layer for electroless plating.

1.9.4 ELECTROLYTIC PLATING

With the capability of Cu CMP, void free trench filling becomes a more important criterion over selective deposition. The trench or via filling capability of

electroplating is better than that of electroless plating because the deposition parameters can be easily controlled in electroplating while deposition progresses spontaneously according to the chemistry of the plating bath. By modulating the current flow direction in electroplating, both deposition and etching are possible.

Cu electroplating is as cheap and simple as electroless plating. The deposition rate is also very fast, typically faster than 3500 °A/min. It also has a excellent compatibility with low – K materials because the deposition temperature is low, i.e., room temperature.

Electrodeposition of metal is the process of deposition of metal by immersing a conductive surface in a solution containing ions of the metal to be deposited. The surface is electrically connected to an external power supply and current is passed through the surface into the solution. This causes reaction of the metal ions (M^{z+}) with electrons (e^-) to form metal (M)

$$M^{z+} + ze^- \rightarrow M \qquad \text{----------(7)}$$

In the case of electrodeposition of copper onto a silicon wafer, the wafer is typically coated with a thin conductive layer of copper seed and immersed in a solution containing cupric ions. Electrical contact is made to the seed layer, and current is passed such that the reaction

$$Cu^{2+} + 2e^- \rightarrow Cu \qquad \text{----------(8)}$$

occurs at the wafer surface. The wafer, electrically connected so that metal ions are reduced to metal atoms, is referred to as the cathode. Another electrically active surface, the anode, is present in the conductive solution to complete the electrical circuit. At the anode, an oxidation reaction occurs that balances the current flow at the cathode, thus maintaining electrical neutrality in the solution. In the case of copper plating, all cupric ions removed from solution at the wafer cathode are replaced by dissolution from a solid copper anode.

Electroplating can be carried out using a constant current, constant voltage, or variable waveforms of current of voltage. Using a constant current, accurate control of mass of the deposited metal is most easily obtained. Plating at a constant voltage and

using variable waveforms requires more complex equipment and control but can be useful in tailoring specific thickness distributions and film properties. [11]

1.10 ANALYSIS TECHNIQUES TO TEST BARRIER STABILITY

The properties of the barrier film like the electrical resistivity, density, grain structure, defect distribution and stress vary significantly depending on their deposition techniques and processing conditions. So, this causes a change in their maximum temperature of stability of barrier (T_s). Another reason leading to the variability of T_s is the application of different analysis techniques. Many conventional characterization techniques, including Rutherford Backscattering (RBS), Secondary Ion Mass Spectroscopy (SIMS), X-ray Photoelectron Spectroscopy (XPS) and Auger Electron Spectroscopy (AES), have been used in almost all barrier performance studies and act to measure the metallurgical stability. With these techniques, it is not necessary to pattern silicon. Therefore, they are very convenient. However, they lack great sensitivity as well as direct applicability to electrical performance.

Electrical characterization such as bias thermal stressing, or study of I-V characteristics provides greater sensitivity for quantifying the barrier response. Thus electrical characterization will indicate the onset of an instability before other less sensitive techniques. Usually, the real T_s is 50 to 100 °C below the T_s obtained by conventional analysis techniques. [8]

1.11 CONCLUSION

Copper will replace aluminum as the main interconnect metal in the next decade. Various transition and refractory metals, their alloys, silicides, nitride, oxide and ternary barrier are studied as potential diffusion barriers. It is very important to evaluate thoroughly the various barriers and optimize the properties and deposition techniques. Also, it is necessary to understand the change in process technology with the introduction of the damascene process and chemical mechanical planarization.

2. REACTIVE SPUTTERING OF TANTALUM NITRIDE FILMS

2.1 FUNDAMENTALS OF SPUTTERING

Sputtering is a vacuum process where ions in a plasma bombard a target under the influence of an electric field. The electric field can be generated by a d.c. potential (typically 500 to 5000 V), or a high frequency a.c. voltage source. The plasma is an electrically neutral glow discharge of electrons and positive ions. Noble gases work best as bombarding species because they are least likely to form reactants on the target surface. Argon is commonly used because the atoms are comparable in size to most target atoms and this results in optimum sputter yield. When argon ions collide with the target, target atoms are ejected by momentum exchange with energies in the range of 10 – 40 eV. These collisions also produce a small number of secondary electrons. These secondary electrons enter the plasma and ionize neutral Ar atoms and thus sustain the plasma. Target atoms that are able to pass through the plasma get deposited on a substrate and surfaces surrounding the substrate. Substrate is any material intentionally positioned to collect the sputtered material.

The schematic diagram of a sputtering system is shown in Figure 2.1.

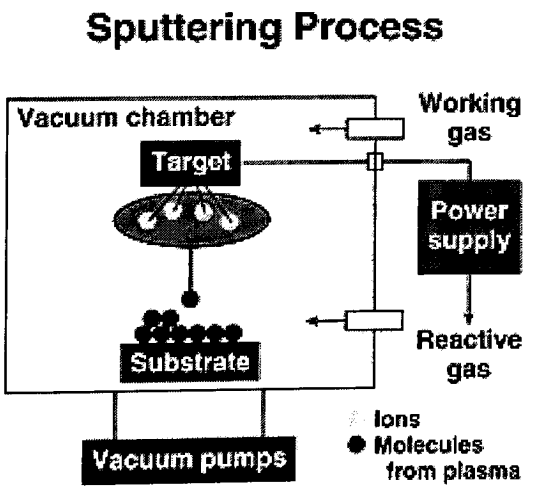


Figure 2.1: Schematic of a sputtering process

2.1.1 D.C. MAGNETRON SPUTTERING

In d.c. magnetron sputtering, electric field is the result of a d.c. voltage, where the target is cathode and the substrate holder is made anode. The target and substrate are separated by 5 to 10 cm but most of the volume between the target and substrate is occupied by the electrically neutral plasma. Visually the plasma appears as a glow discharge with a dark space over the cathode. The applied potential is concentrated in the dark space giving rise to a large electric field. Current flow is the result of Ar^+ ions from plasma to the target and electrons from plasma to the substrate. Electrons cause the substrate to heat up when they impact it. To prevent this, a magnetic field is applied in such a way as to confine the electrons to the vicinity of the target. This variation to the standard sputtering arrangement is called magnetron sputtering. A second gas may be intentionally mixed with the argon so that the deposited material is a compound of the target material and the second gas. This is called reactive sputtering.

2.1.2 R.F. MAGNETRON SPUTTERING

When an electrically insulating material is used as a target for sputtering in a standard d.c. arrangement, positive charge accumulates on its surface and the sputter yield decreases to zero. This can be overcome by applying an a.c. potential to the target instead of a d.c. potential. A magnetic field is also applied as in the case of d.c. sputtering. As the potential alternates, the electrodes reverse their cathode-anode roles every half cycle and there is a dark space over each electrode. The frequency of the oscillations must be high enough to prevent any charge accumulation during that part of a cycle the electrode serves as the cathode. The Federal Communications Commission has allocated the r.f. frequency range of 10 to 20 MHz for industrial, scientific, and medical applications and most r.f. sputtering tools operate at 13.6 MHz. RF sputtering is preferred to d.c. sputtering because of its versatility in depositing conducting, semi conducting as well as insulating materials.

2.2 HYSTERESIS BEHAVIOR DURING SPUTTERING

During reactive sputtering, a reactive gas, usually N_2 or O_2 is added to the usual Ar sputtering plasma to deposit a compound film from a metallic target. Reactions occur at the surfaces of target and substrate between metal atoms and the reactive gas. A layer of compound forms on both the substrate and the target. Coverage of target reduces the area of bare metal available for sputtering and leads to hysteresis, as shown in figure 2.2 [30]. When the metal target is sputtered in pure Ar (point A), the rate of sputtering is relatively high. For very low flow, the reactive gas is consumed by the growing film and the partial pressure remains low. The films deposited are sub-stoichiometric with free metal. As the flow of reactive gas is increased, the rate remains high until some critical flow, at which, the target is sufficiently covered by the compound so that less metal is sputtered, consuming less reactive gas. The gas adsorption rate on target exceeds the sputtering rate. Then the target becomes 'poisoned' with adsorbed gas, and the sputtering rate drops to a much lower level because much of the ion bombardment now goes into sputtering away the continuously adsorbing layer rather than sputtering the underlying metal. If the reactive gas flow is now decreased, the poisoned condition persists until point D, where the sputtering rate begins to exceed the adsorption rate so that the target can clean itself and return to the high metal sputtering rate.

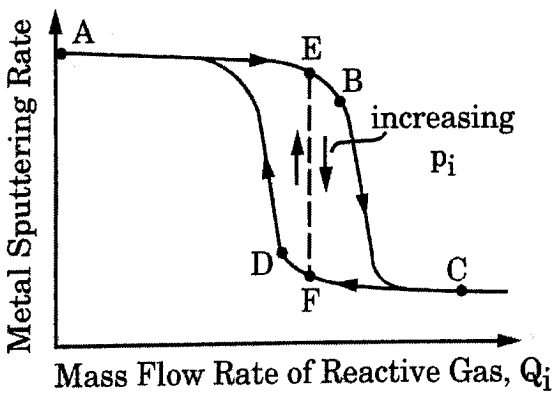


Fig 2.2: Hysteresis Behavior in Reactive Sputtering

2.3 DEPOSITION OF TANTALUM NITRIDE FILMS

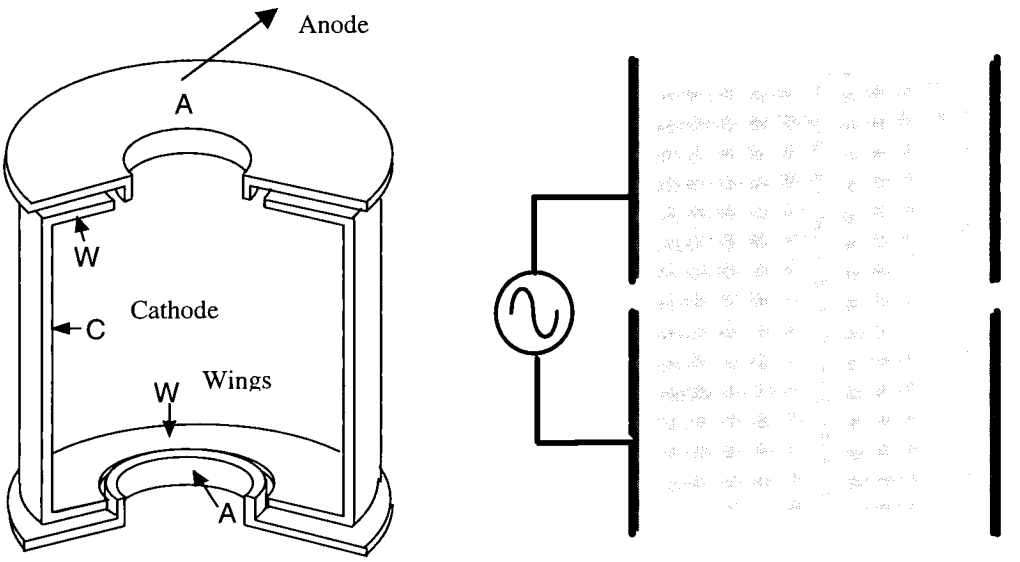
Tantalum and its nitrides have been extensively investigated as diffusion barriers for copper since they not only show relatively high melting temperature, but also are thermodynamically stable with respect to copper. Because of this reason, Ta and its nitrides have been chosen for the present study.

There are various methods for depositing thin films such as thermal evaporation, e-beam evaporation, chemical vapor deposition (CVD), molecular beam epitaxy and sputtering. Thermal and e-beam evaporation includes melting of the material in high vacuum that makes it an undesirable method for high melting point materials and it also suffer from out gassing and crucible/fixture contamination problem. CVD methods require a precursor that may be problematic due to the emission of undesirable gases. MBE method is epitaxial physical vapor deposition and requires ultra high vacuum ($\sim 10^{-10}$-10^{-12} torr) and has not yet found commercial application in CMOS semiconductor technology. Sputtering by far is the most preferred method of depositing thin films. For the present study, reactive sputtering of Ta in N_2 atmosphere has been investigated. By using reactive sputtering of Ta, the properties of TaN_x compounds can be tailored by varying the N_2 flow. The stoichiometry, electrical properties, crystallographic structure and the morphology of the TaN compounds depend on the sputtering conditions, pre-treatment and film thickness. The first step in the process is to characterize the hysteresis behavior of tantalum nitride to determine the working range of N_2 for deposition of the films.

2.4 IONTECH CYCLONE CYLINDRICAL MAGNETRON SYSTEM

The TaN films were reactively sputtered in an AC twin cathode inverted cylindrical magnetron configuration of the Ion Tech sputtering system developed by Ion Tech Veeco Inc. Ion Tech Cyclone is a fully automated system with short cycle times and high deposition rates. The AC inverted magnetron configuration has remarkable improvements over RF and DC configurations. To enable reactive sputtering, the cathode is split half way down the cylinder and the cylinders are powered by an AC power supply

operating at 40 kHz and 50 % duty cycle. The AC outputs float with respect to ground. For half a cycle, the top cylinder serves as cathode, while the bottom cylinder is neutralized. In the other half cycle, the roles of the cylinders are reversed. This design suppresses arcs very naturally without the need of any additional circuitry [15]. There is excellent target utilization and uniform deposition of even complex shapes. The sputtering source, seen in figure 2.3, is a cylindrical target that surrounds the substrate to be coated. This cylindrical design allows three-dimensional objects to be coated simultaneously in all directions without rotation. Magnetic field in the cylindrical magnetron produces uniform plasma and therefore leads to a more uniform use of materials, which is not possible in the planar magnetron. In addition, approximately 75% of the target is utilized because most of the target material that is not deposited on substrate is re-deposited on the target.



(a) Schematic of the tool **(b) Twin cathode set up**

Figure 2.3: Ion tech sputtering tool

2.4.1 EXPERIMENTAL DETAILS

The sputtering target used was a 7.5" diameter cylindrical sheet of tantalum. The chamber was evacuated with a 1600 l/s turbo pump backed by a rotary pump to a base pressure of 5 x 10^{-6} torr that was attained within less than 3 min of pumping. A working pressure of 8 mtorr was used during sputtering. Low pressures were measured with a hot cathode ionization gauge, and sputtering pressures were measured with a capacitance manometer. The gas mixture consisted of argon at 99 sccm and the nitrogen flow was varied for various runs. The total pressure, however, was maintained constant by using a VAT pendulum control valve that varies the pumping speed. The cathode was run in a constant power mode using an Advanced Energy PE5000 supply (40 kHz, maximum power 5 kW, maximum voltage 600V). Mass flow controllers were used to monitor the gas flow rates. A forward power of 2 kW was used for all the runs.

A hysteresis plot was first obtained by varying the N_2 flow from 0 to 50 sccm and back while measuring the voltage of the target without using any substrate. After analyzing the hysteresis behavior of TaN, films were deposited on SiO_2 wafers at 8mtorr pressure, 2 kW power and N_2 flow between 0-40 sccm for 5 min. To remove the surface oxide layer on the wafers, they were cleaned by dipping in buffered HF (50:1) for 2 min followed by a spin, rinse and dry in N_2 prior to sputtering. This is very essential for good adhesion of TaN films to the substrate.

The thicknesses of the films were measured with a Tencor AlphaStep profilometer. Steps were made by marking a line on the wafers prior to deposition with a sharpie pen, and then removing it after the deposition using acetone. Sheet resistance was measured by a standard four-point probe. The X-ray Diffraction Analysis was done on Rigaku x-ray diffractometer with Cu- K_α radiation. Adhesion of films to the substrate was qualitatively assessed using a scotch tape test.

2.5 X-RAY DIFFRACTION TECHNIQUE

X- ray diffraction analysis of the film samples was done to detect crystalline phases present. A Rigaku Geigerflex model diffractometer which uses a Cu- K_α radiation (λ = 1.54056 A) and has a maximum scan range of $2\theta = 0^o - 160^o$ is used for the analysis. The starting and ending scan angle, slew rate (0.06-6.0 deg/min), and step size (0.01^o-0.1^o) can be selected by the user for any scan. A software package called JADE automatically locates peaks by their angular position and planar spacing, and allows multiple spectra to be over-layed for comparison.

The peak positions of spectra of a material are a function of the crystal structure and planar spacing. Spacing of planes in the direct lattice is proportional to the position vector in reciprocal space. The position vector in reciprocal space is defined so it is normal to planes (hkl) in the direct lattice. Planes in reciprocal space, (h'k'l'), are proportional to those of the direct lattice, e.g. h'/h = k'/k = l'/l = N. The position, θ_b, of a peak corresponding to (hkl) planes of spacing, d_{hkl}, satisfies the Bragg relation,

$$N\lambda = 2d_{hkl} \sin\theta_b. \qquad \text{---------- (1)}$$

where N is an integer representing the order. [16]

The intensity of a peak is a function of the crystal structure and atoms forming the respective plane. For a given plane in the reciprocal lattice- (h'k'l'), the intensity of the respective peak is proportional to

$$F(h'k'l') = \Sigma_j f_j e^{i2\Pi (h'x_j + k'y_j + l'z_j)} \qquad \text{----------(2)}$$

where the sum taken is over the j atoms in the unit cell located at (x_j,y_j,z_j) and f_j is the scattering factor of the j^{th} atom in the cell. Scattering factors are tabulated for every known atom.

The five most intensive planes, along with their 'd' spacing and 2θ values of TaN, Ta_2N are listed in table 2.1, 2.2 respectively.

Plane	Spacing, Å	2θ	Rel. intensity
110	2.5959	34.522	100
101	2.4421	36.722	78
201	1.7784	51.332	28
211	1.4670	63.345	23
300	1.4987	61.855	14

Table 2.1: Five most intensive XRD peaks of TaN

Plane	Spacing, Å	2θ	Rel. intensity
101	2.3230	38.730	100
002	2.4570	36.541	25
100	2.6370	33.968	20
103	1.3910	67.251	20
214	0.7739	168.914	20

Table 2.2: Five most intensive peaks of Ta_2N

2.6 RESULTS

The hysteresis plot of sputter deposition of tantalum nitride is shown in figure 2.4. There is a gradual increase in target voltage with increase in N_2 content. It was observed that reactive sputtering of tantalum nitride does not show any significant hysteresis.

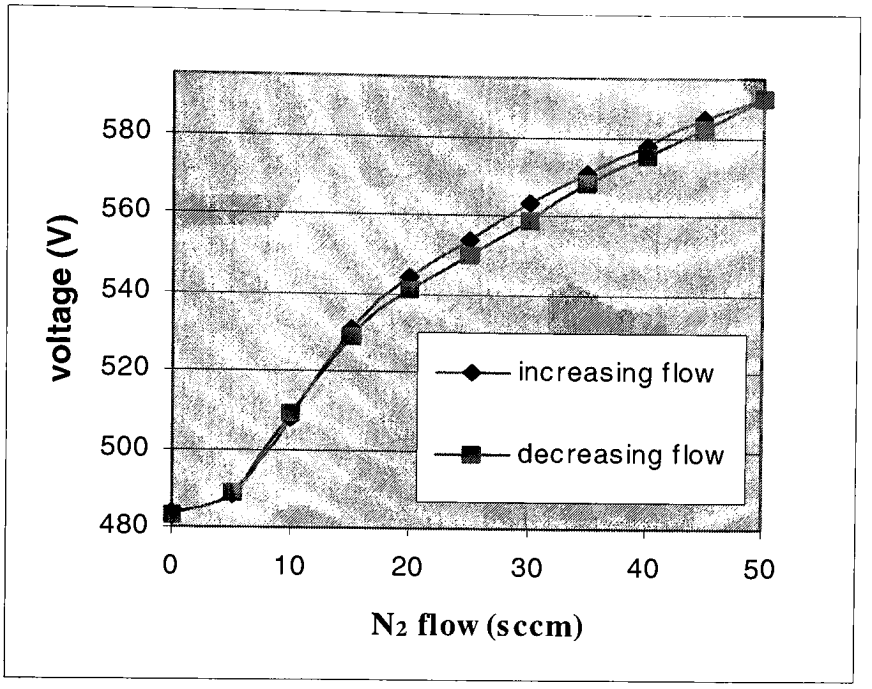


Figure 2.4: Hysteresis Behavior of Tantalum nitrides

Therefore, it was decided to deposit films in the range of 0-40 sccm of N_2. The parameters used for deposition of films are given in table 2.3.

Parameter	Value
Base pressure	5 x 10^{-6} torr
Working pressure	8 mtorr
Power	2 kW
Time	5 min

Table 2.3: Sputter parameters for deposition

Figure 2.5 and 2.6 shows the measured thickness and resistivity of tantalum nitride films for various concentrations of N_2 flow.

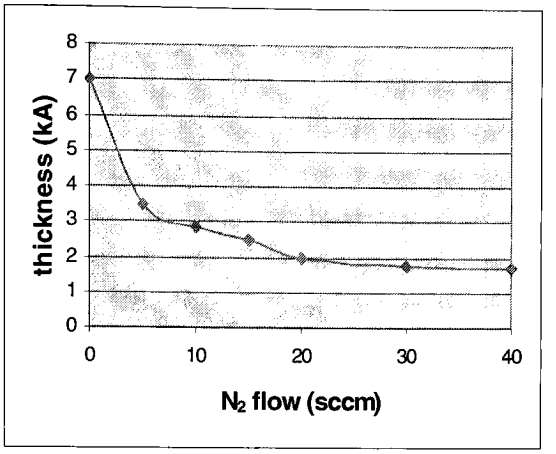


Figure 2.5: Dependence of thickness on N_2 flow

The resistivity of pure Ta film was measured to be about 630 μΩcm. As the nitrogen flow is increased to 5%, there is a decrease in resistivity to 276 μΩcm in the resulting films. Increasing the nitrogen content further to 20% causes a gradual increase to 1200 μΩcm. At higher levels of N_2, there is a steep increase in resistivity due to low deposition rate and high sheet resistance. As the N_2 flow is further increased, the appearance of the films changed from metallic silver to dark grey.

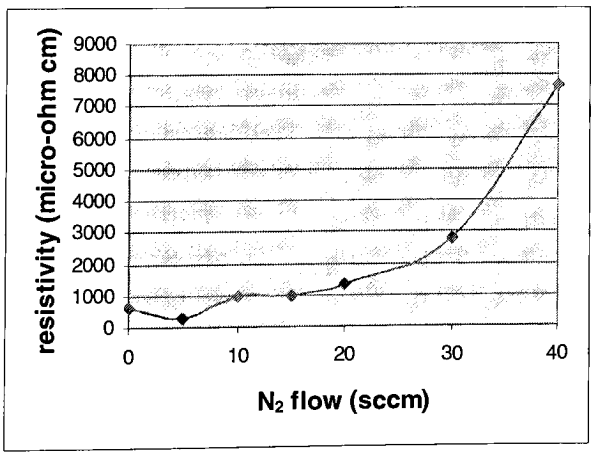


Figure 2.6: Dependence of resistivity on N_2 flow

The XRD analyses (from figures 2.7 – 2.10) reveal that the film deposited in pure Ar is bcc– Ta. As the N_2 flow rate is increased to 5-10%, Ta(N) phase is present along with the β Ta phase. Between 30-40 % N_2 flow, the crystalline phase present is fcc-TaN. However, an amorphous compound Ta_2N appears in the center portion of the range at about 15-20%. At 50 % N flow, fcc- TaN is formed along with other nitrogen rich compounds of Ta.

When the films were tested with a scotch tape, they did not peel. This means the adhesion of the films to the substrate was good.

2.7 DISCUSSION

2.7.1 HYSTERESIS BEHAVIOR

In the operating range of N_2 flow used, no hysteresis has been observed. This is because of the high pumping speed of 1600 l/s obtained by the turbo pump. There is no poisoning of the target, and the films were deposited in the high rate metal sputtering mode. According to a previously reported study by M.Staurev et al [19], there is a critical threshold value of N_2 that is equipment sensitive above which hysteresis is observed. However, this was not reached in the present experiment.

2.7.2 EFFECT OF N_2 CONTENT ON RESISTIVITY AND CRYSTAL STRUCTURE

The observed change in resistivity can be explained in terms of film composition and structure. Pure Ta film shows (002), (202), (413) peaks representing tetragonal β-Ta. With slight increase in N_2 to 5sccm, bcc-Ta phase starts forming, observed by the presence of (110) and (200) peaks [3], as seen in figure 2.7. The addition of small amounts of N_2 in sputtering gas induces a phase transformation from β-Ta to bcc- Ta. The initial drop in resistivity from about 630 to 276 μΩcm can be interpreted as due to this change in the crystal structure. There has been no explanation in the literature on the deposition conditions that cause this transformation.

This interesting change in resistivity of the films has also been observed by S.P. Murarka [2], but the overall resistivity of films obtained in present study is found to be an order higher than the reported values. The resistivity of β-Ta is reported to be about 180 μΩcm while that of bcc- Ta is about 40 μΩcm.[17] With increasing nitrogen, there is formation of Ta_2N, fcc -TaN and other nitrogen rich compounds that are responsible for the steep increase in resistivity. The resistivity of tantalum nitride sputtered films is strongly dependent on the processing conditions. Therefore, a design of experiments methodology was used for optimization of process parameters for depositing the films. This is discussed in section 2.8.

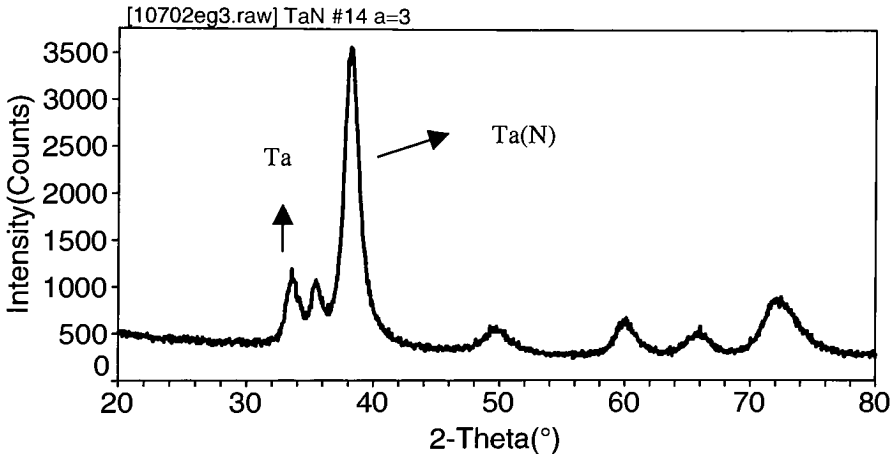


Figure 2.7: XRD Pattern with 5 % N_2

At N_2 flow of 12 sccm, no clear peaks of any tantalum nitrides are observed in the XRD spectrum as shown in figure 2.8. There are peaks corresponding to bcc- Ta(N). However, when the samples were annealed to 700 °C, peaks associated with Ta_2N phases are formed as seen in figure 2.9. This can be explained as due to the crystallization of Ta_2N phase at higher temperatures that was primarily amorphous when as-deposited. This is in accordance with the Ta- N phase diagram in figure 2.11. At 30% N_2, fcc-TaN phase is present as seen in figure 2.10. At 40 sccm N_2, the peaks are not sharp. For the films with higher nitrogen content it is difficult to identify the phases of the films by using XRD since only one or two weak and broad peaks appear. As the percentage of N_2 flow

in the sputtering gas is increased, the nitrogen content in the films also increases. It has been reported that the grains of the crystalline phases are considerably small and their size decreases with increasing nitrogen concentration. [28] Further analysis like TEM, AES needs to be done to analyze the microstructure and composition of the phases. At higher concentrations of N_2, nitrogen rich compounds like Ta_5N_6, Ta_3N_5 are formed that have very high resistivity.[3] Hence these materials are not desirable as diffusion barriers. Table 2.4 summarizes the various phases of tantalum nitride for various concentrations of N_2.

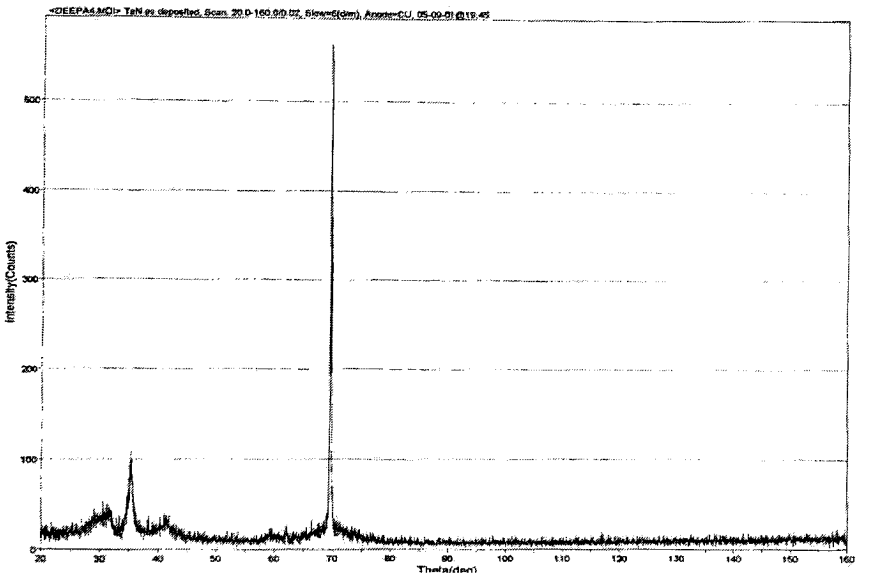


Fig 2.8: XRD Spectra of as-deposited TaN (N_2- 12 sccm) film

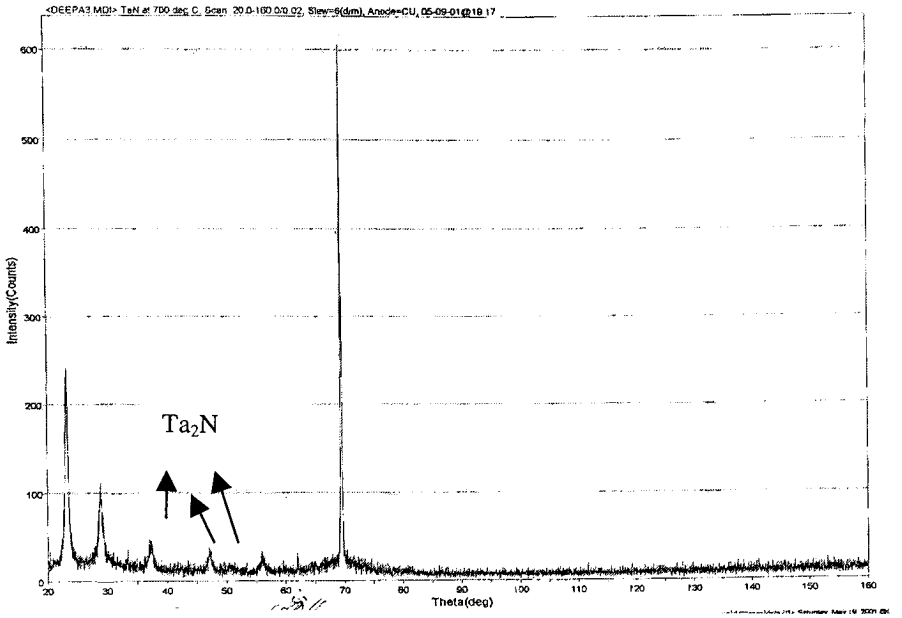


Fig 2.9: XRD Spectra of TaN (N_2- 12 sccm) annealed at 700 °C

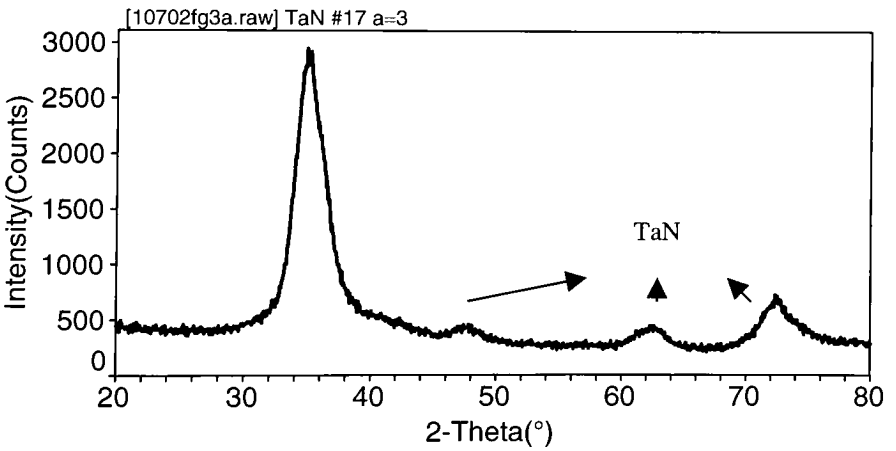


Figure 2.10: XRD Pattern with 20 sccm of N_2 flow

N_2 flow (sccm)	Crystalline phases
0	Tetragonal Ta
5	Tetragonal Ta +bcc Ta(N)
10	bcc Ta(N)
15	Amorphous Ta_2N
20	bcc Ta_2N
30	fcc TaN
40	fcc TaN + Ta_3N_5 [19]

Table 2.4: Phases of TaN

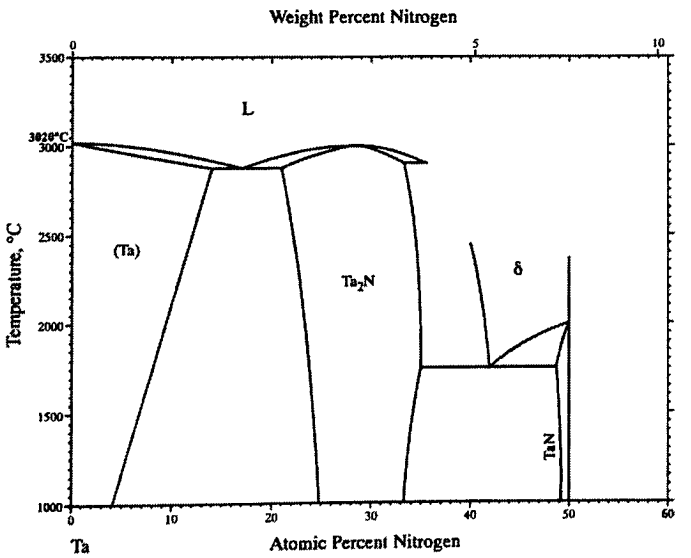


Figure 2.11: Binary Phase diagram of Tantalum and Nitrogen [35]

2.8 FRACTIONAL FACTORIAL DESIGN

A designed experiment is a test in which some purposeful changes are made to the input variables of a process or system so that we may observe and identify the reasons for changes in the output response. Experimental design methods play an important role in process development and process improvement.

Experimental designs in which every level of every variable is paired with every level of every other variable are called factorial designs. A basic experimental design is one with all input factors set at two levels each. These levels are called 'high' and 'low' or '+1' and '-1' respectively. A design with all possible high/low combinations of all the input factors is called a two level full factorial design. If there are k factors, each at 2 levels, a full factorial design has 2^k runs.

The need for fractionating the full factorial comes from:

- The inability to economically run a full factorial with many factors
- One needs only to understand main effects, not interactions, when screening
- Higher order interactions would be impossible to interpret

A factorial experiment in which only an adequately chosen fraction of the treatment combinations required for the complete factorial experiment is selected to be run is called a fractional factorial design.

2.8.1 THE ANALYSIS OF VARIANCE (ANOVA) TECHNIQUE

ANOVA is a data analysis technique for examining the significance of the factors in a multifactor model. The main effect of an independent variable is the effect of the variable averaging over all the other parameters. YATES analysis computes the mean square and half effect for two level factorial and fractional factorial experiments. All main effects and interactions are computed.

The following five factors were chosen to be investigated and a ½ fractional factorial experiment was run. The total number is $2^4 = 16$.

- N_2 flow rate: 5 and 20 sccm
- Pressure: 4 and 8 mTorr
- Power: 1 and 2 kW
- Substrate bias: 0 and 50 kV
- Time : 5 and 15 min

The experimental design set up is shown in table 2.5. The responses measured for each run thickness, sheet resistance and resistivity are also tabulated. Four randomly chosen runs were repeated to see if there were any noise factors affecting the runs. The 20 runs were randomized to avoid any systematic errors.

Std Order	Run Order	Flow	Bias	Pressure	Power	Time	Rs	thickness	Resistivity (μΩ)
		(sccm)	(V)	(mTorr)	(kW)	(min)	(ohms/sq)	(kA)	cm)
1	4	5	0	4	1	15	5.46	4.125	225
2	3	20	0	4	1	5	66.74	1.34	894
3	12	5	50	4	1	5	5.83	1.4	81
4	16	20	50	4	1	15	34.01	2.7	918
5	6	5	0	8	1	5	16.59	1.12	185
6	15	20	0	8	1	15	40.61	2.4	974
7	11	5	50	8	1	15	7.9	3.5	276
8	7	20	50	8	1	5	66.82	1.3	868
9	10	5	0	4	2	5	8.20	3.25	266
10	13	20	0	4	2	15	12.65	2.9	367
11	1	5	50	4	2	15	2.70	4.02	108
12	2	20	50	4	2	5	17.01	1.77	301
13	14	5	0	8	2	15	2.28	3.9	89
14	20	20	0	8	2	5	45.78	1.76	805
15	18	5	50	8	2	5	16.45	2.95	485
16	17	20	50	8	2	15	19.18	4.7	901
17	19	5	50	8	2	5	16.93	2.87	486
18	8	20	50	8	1	5	63.61	1.19	756.
19	9	5	0	4	1	15	6.38	4.36	278
20	5	20	0	4	2	15	14.22	3.2	455

Table 2.5: DOE runs along with the responses measured for each run

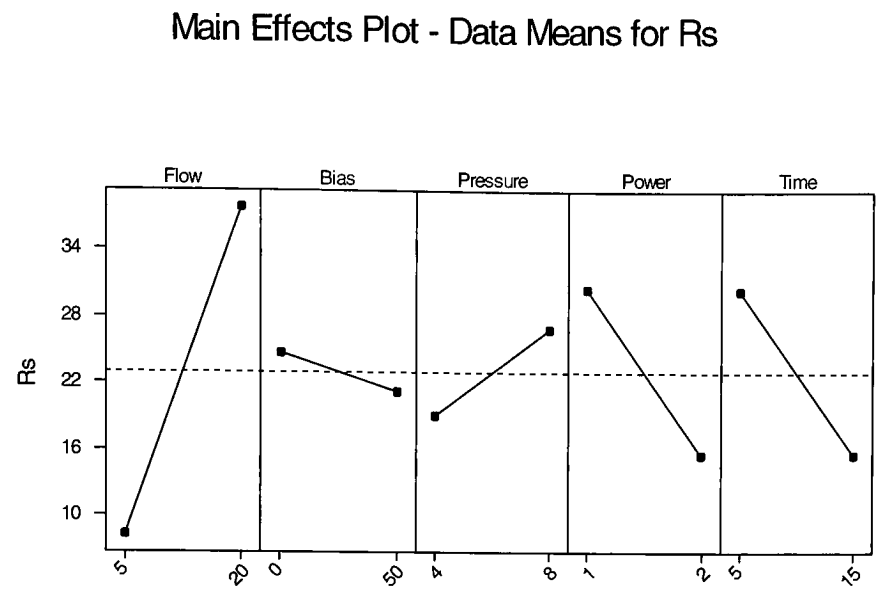


Fig 2.12: Dependence of factors on sheet resistance

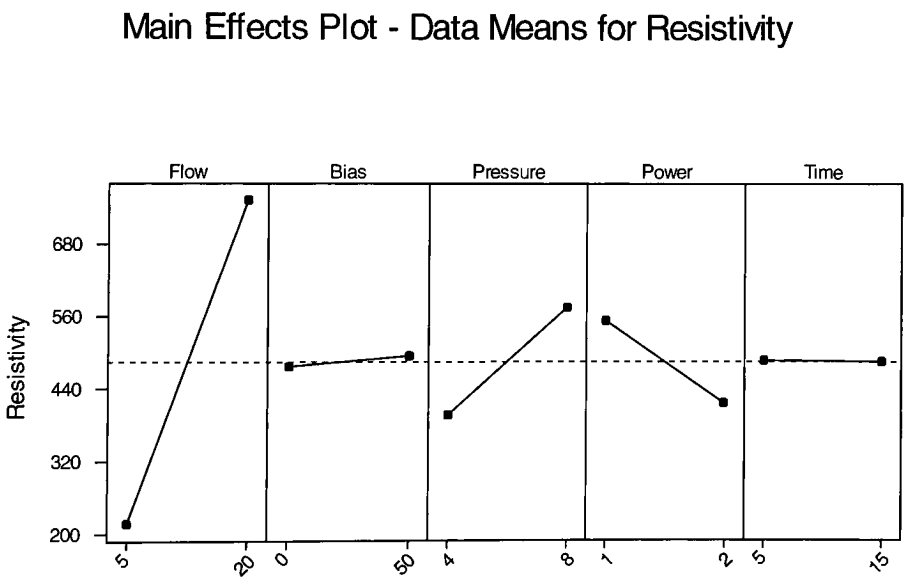


Fig 2.13: Dependence of factors on resistivity

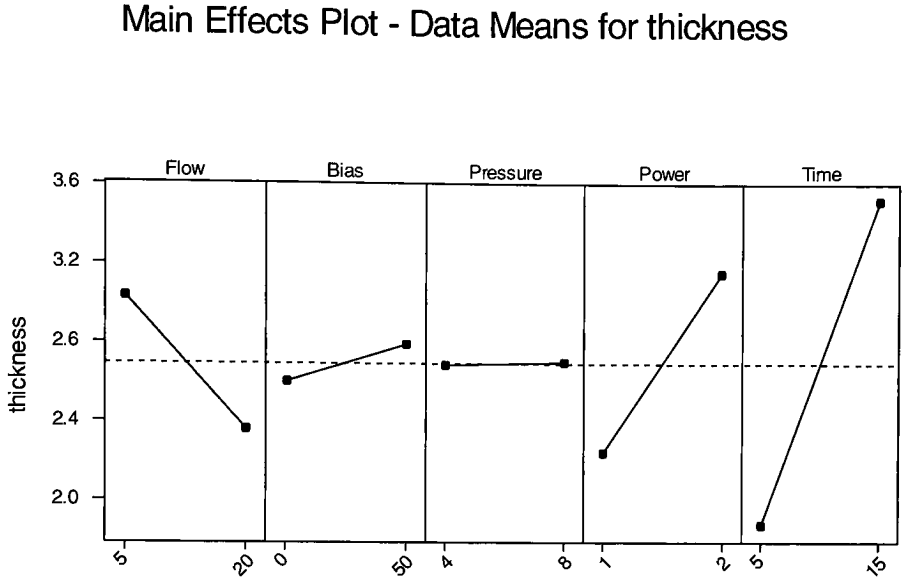


Fig 2.14: Dependence of factors on thickness

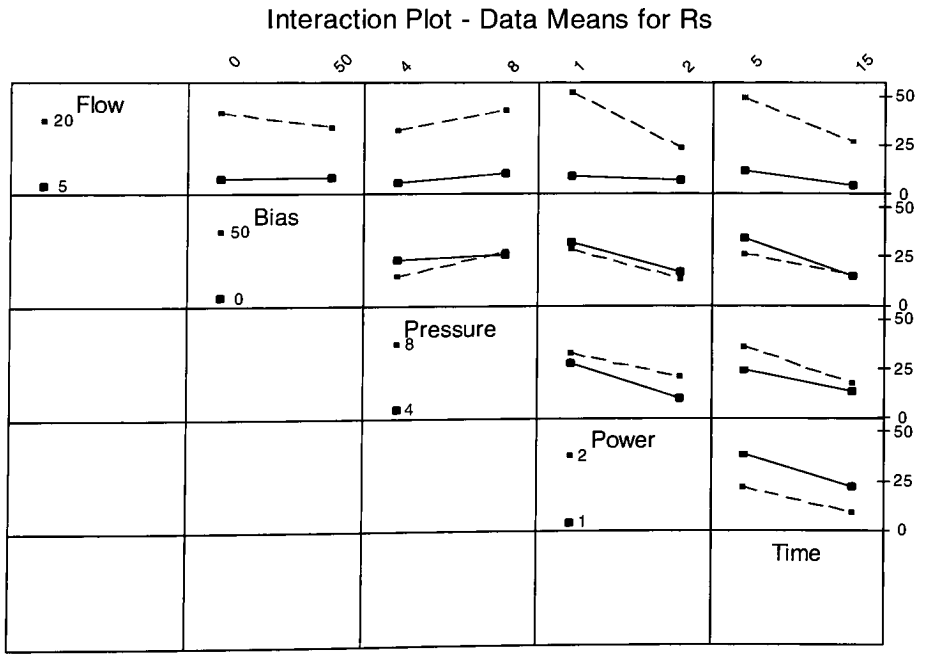


Fig 2.15: Effect of interactions between factors on sheet resistance

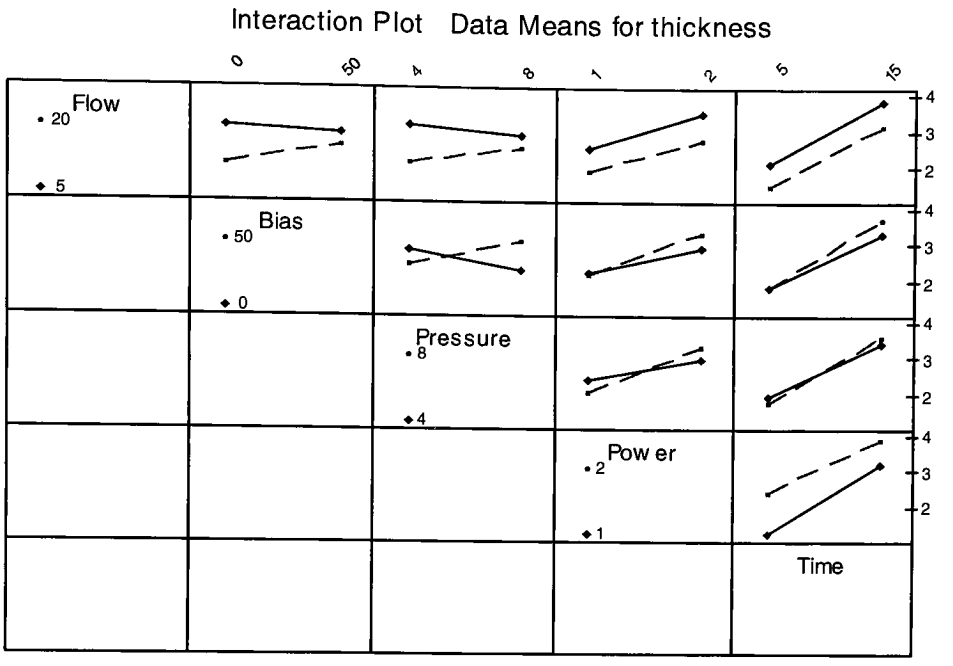


Fig 2.16: Effect of interactions between factors on thickness

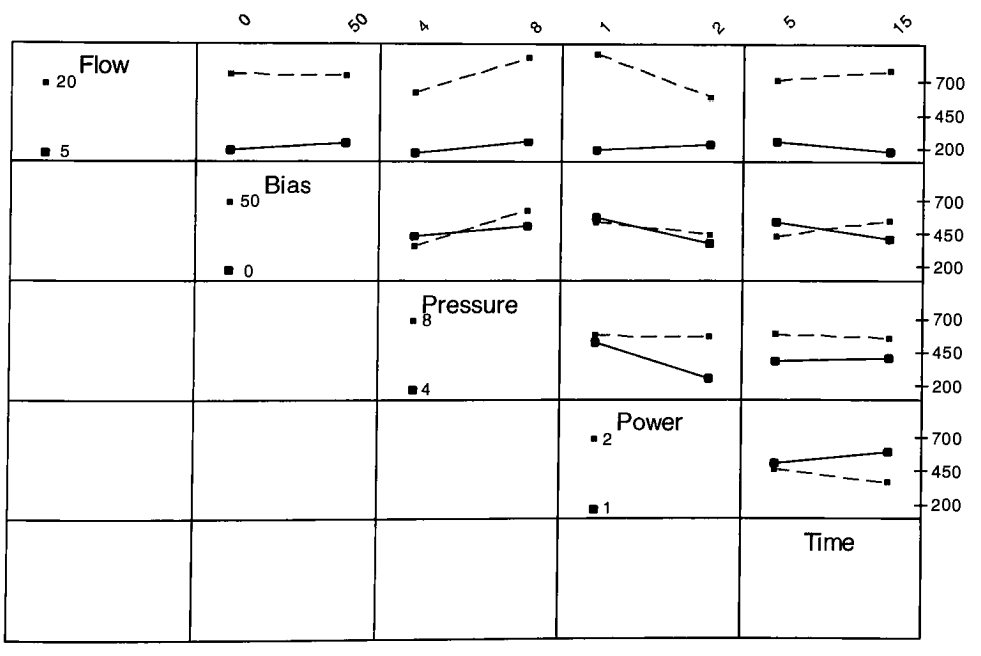


Fig 2.17: Effect of interaction between factors on resistivity

2.8.2 RESULTS AND DISCUSSION

The results were analyzed using statistical software (Minitab- version 13.30). The main effects and interaction plots of the responses were plotted with respect to the process variables as shown in figures 2.12 – 2.17. From the Yates ANOVA analysis it was determined that the optimum parameters required to obtain a low resistivity of 220 μΩcm were 10sccm N_2, gas pressure of 4 mtorr, 22 V bias, power of 2kW and a deposition time of 15 min.

At high gas pressure, there are more collisions between ions. Therefore, discharge current increases, causing voltage and cathode dark space to decrease. At low pressure, there is a decreasing influence of gas atoms, causing a lower concentration of trapped gas atoms. There is also a controlled direction and higher mean energy of the ejected atoms striking the substrate owing to smaller collision losses. A denser film is obtained thus making the resistivity of the film low.

Reasonable sputtering rates at low pressures may be obtained by increasing the ionization of the sputtering gas by

1. Increased ionizing efficiency of the available electrons
2. Increased supply of ionizing electrons
3. An ion beam source

At very low pressures (< 2 mtorr), the probability for ion production by energetic electrons is low. The probability of secondary electrons ionizing enough argon atoms to produce more electrons from the target can only be increased by increasing working pressure. However, if the pressure is too high, there would be a decrease in deposition rate of films, because significant number of sputtered atoms would not be able to penetrate the discharge atmosphere. Some atoms may even reflect back to the target.

Use of a bias during sputtering helps in reducing impurity concentration. By biasing the substrate negatively, ions may be accelerated out of plasma into the substrate to enhance resputtering. The ion bombardment removes adsorbed gases and loosely

adhering species producing films of higher purity. The bombardment of deposit influences the state of stress and crystallographic orientation of films. It is also expected to have a considerable influence on film structure and will increase the crystallite size, thus reducing the grain boundary scattering contribution to resistivity. The effect of bias is equivalent to adding energy to the substrate that is similar to sputtering at lower pressure. Use of high power during sputtering creates more energetic ions in the plasma and that is also equivalent to sputtering at low pressure. However, it is to be noted that high power induces high stresses in the deposited films.

2.9 PULSED DC SPUTTERING OF TANTALUM NITRIDE FILMS

Pulsed DC sputtering of TaN films was carried out in the CVC 601 sputtering tool developed by CVC- Veeco, Inc. CVC 601 is a multi-target DC sputtering system. The target is arranged to sputter upward and the substrate holder, a rotostrate can be stationary or rotating during sputtering. The base and sputter pressures of the chamber were measured by an ion gauge and a pirani gauge respectively and displayed on the control panel. Flow rate is monitored by a dual channel Brooks flow meter and the Ar and N_2 flows were based on the mass flow controllers (mfcs). The mfcs are calibrated such that the actual N_2 flow is the meter setting x 2 and the Ar flow is meter setting x 2.8.

The power and sputter time are set using a ENI power supply control. Pre heat of the chamber is done for 20 min to decrease the pump down time. Pre-sputtering of the target is done for 5 min to remove any unwanted oxides or contamination from the target. This is done by closing the shutter on the target that is to be sputtered. Sputtering is started after the designated pre sputter time had elapsed by manually opening the shutter. Between sputtering sessions, the user can change sputtering gas or the mixture of gases and the target.

CVC 601 system was used for further experiments because of the ability to sputter TaN and Cu without breaking vacuum, which is very critical for the stability of the barrier layer. Trial sputter parameters were determined from the results of the DOE runs on the iontech sputter tool and initial runs on the CVC 601. The films were deposited on bare Si and oxidized Si wafers with N_2 proportions of 12 % and 30 % to

obtain Ta_2N and TaN films respectively. The sputtering parameters are shown in table 2.6. The TaN films were annealed to higher temps of 600-700 °C in N_2 atmosphere after deposition for 40 min. in a Lindberg Model BF 51600 series box furnace. XRD analysis of the annealed films was done to observe phase changes and thermal stability of the films.

Parameter	Value
Base pressure	5 x 10^{-6} mTorr
Sputtering pressure	4 mTorr
Power	1000W
Time	15 min

Table 2.6: Sputtering parameters for TaN films

2.10 RESULTS AND DISCUSSION

There was no hysteresis observed under pulsed DC sputtering conditions. This indicates that the films were deposited in the high rate metal sputtering mode. The positions of reflection lines of Ta_2N (101) and TaN (111) in the 2θ values were shifted toward the lower diffraction angle with respect to those in the bulk phase. This may be explained as due to internal stresses in the films. The films were stable even at high temperature of 700 °C and do not react with silicon to form any tantalum silicides. The films show enhanced crystallinity at high temperature because of grain growth. The resistivity of Ta_2N and TaN films was measured to be 240 and 320 μΩcm respectively. This is a little higher than the values reported in literature as 190 and 250 μΩcm respectively. [29] This is believed to be due to the presence of oxygen contamination in the films. To check if there was any out diffusion of oxygen from the oxidized Si films during deposition, TaN films were deposited on bare Si and oxidized Si films. The sheet

resistance of the films was measured immediately after deposition by four-point probe technique to be 7.8 and 8.5 ohms/sq for bare Si and oxidized SiO_2 substrates respectively. There was no significant difference between resistivity values of the films deposited on the two substrates. This suggests that there was no oxygen out-diffusion from the thermally grown SiO_2 film. The high resistivity of the films is due to the oxygen picked up from the chamber. If the plasma contains atoms other than argon, they may react with the target at its surface. This includes contaminates from out-gassing and leaks. Since oxygen is usually present in trace amounts and is highly reactive, the deposited films are usually oxygen contaminated to some degree unless a very high vacuum ($<10^{-8}$ torr) can be attained. The CVC 601 tool employed for this study did not have a load lock chamber, and the chamber had to be opened to atmosphere for loading and unloading purposes. Low resistive tantalum nitride films may be obtained by use of ultra high vacuum of about 10^{-8}-10^{-9} torr during the deposition process.

3. DEPOSITION OF COPPER FILMS AND STUDY OF BARRIER CHARACTERISTICS

3.1 BACKGROUND

As discussed in section 1.9 there are various techniques for deposition of copper. For the present study, it was decided to sputter copper because of the ease of deposition, and the ability to deposit Cu after depositing the barrier layer of TaN in CVC 601 sputtering tool without breaking the vacuum. This is important because exposing the barrier layer to atmosphere before depositing copper causes formation of an oxide layer on TaN that increases the resistivity of the film and also causes adhesion problems with copper. During back-end processing, the diffusion barrier and the interconnect materials, TaN and Cu, are subjected to various annealing treatments in different ambients at relatively high temperatures. These heat treatments influence the stability of Cu/TaN metallization, due to their effect on microstructure and electrical properties. In this chapter, deposition of copper films and the effectiveness of TaN barrier layer under various annealing conditions will be studied.

3.2 EXPERIMENTAL PROCEDURE

Deposition of copper films was done using the CVC 601 tool. A few initial trial runs were done to characterize the deposition rate of copper and to obtain films with low stress. Copper films were sputter deposited at 2 and 4 mtorr pressure, 400W and 800W power for 20, 30 and 40 min respectively on thermally grown SiO_2 wafers. The thickness of the films was measured by using a step profilometer. Prior to the deposition of any film, 5000 Å of thermal oxide was grown on 4 in. diameter p- type Si wafers. The wafers were cleaned in a 50:1 buffered HF solution for 2 min and spin, rinse dried in N_2 before loading into the sputtering chamber. The chamber was pumped down to a vacuum of 5 x 10^{-6} torr. TaN films of thickness 1000 Å were deposited by sputtering using a total pressure of 4 mtorr, a power of 1000W for 15 min and N_2 flows of 12 and 20 sccm. Subsequently, 1200 Å of Cu was sputter deposited on top of the barrier layer without breaking the vacuum at a pressure of 2 mtorr, power of 500 W for 15 min as these were

decided to be the best parameters to produce films with low stress. Use of low pressure and low power during sputtering enables films with low stress.

Two sets of $Si/SiO_2/TaN/Cu$ samples were annealed at temperatures ranging from 200 to 600 °C for 20 min with a constant ramp rate of 12.5 °C /min starting from room temperature (20 °C) in a Lindberg Model BF 51600 series 1100 °C box furnace. It is important to use a slow ramp rate; otherwise, thermal stresses developed would cause delamination of the films. One set of samples was annealed in N_2 atmosphere while an Ar ambient was used for the other one. The change in electrical properties was monitored by sheet resistivity measurements. XRD analysis was used to examine the phases of as-deposited and annealed films. The composite films and the reactions between films were studied by Rutherford Back Scattering (RBS) analysis.

3.3 RUTHERFORD BACKSCATTERING ANALYSIS (RBS)

In Rutherford Backscattering Analysis, ions of a high kinetic energy (typically 1-3MeV) are directed at the sample. The incident ions are elastically scattered from atoms in the sample and the number of scattered ions and their energy is measured. This data provides information on the composition, distribution of the components and the thickness of the sample.

The incident ions are usually positively charged helium atoms. When they are incident on the sample, a vast majority of them end up implanted in it. Only a small fraction of the incident particles undergo a close encounter with an atomic nucleus and are back scattered out of the sample. When probing particles penetrate to some depth in a dense medium, projectile energy dissipates due to interactions with electrons (electronic stopping) and due to glancing collisions with the nuclei of target atoms (nuclear stopping). This means that a particle that backscatters from an element at some depth in a sample will have measurably less energy than a particle that backscatters from the same element on the sample surface. The amount of energy a projectile loses per distance traversed in a sample depends on the projectile, its velocity, the elements in the sample, and the density of the sample material. This energy loss dependence on sample

composition enables RBS measurements of layer thicknesses, a process called depth profiling.

A typical RBS system consists of an accelerator and a scattering chamber with sample manipulators and particle detectors. In the RBS system used for the present study, samples are bombarded with 1-3 MeV protons or alpha particles from a Van de Graff electrostatic accelerator and the scattered particles are detected by a surface barrier detector. The signal from detector is processed by common nuclear electronics and the particle energy spectra are stored in a computer based multi-channel analyzer. The data evaluation is accomplished using standard procedures and computer codes by a process called RUMP simulation.

3.4 SCANNING ELECTRON MICROSCOPY (SEM)

The Scanning Electron Microscope (SEM) is a microscope that uses electrons to form an image. There are many advantages to using the SEM instead of an optical microscope. SEM has a large depth of field, which allows large area of a sample to be in focus at one time. It also produces images of high resolution, which means that closely spaced features can be examined at a high magnification. Preparation of the samples is relatively easy since most SEMs only require the sample to be conductive. The combination of higher magnification, larger depth of focus, greater resolution, and ease of sample observation makes SEM one of the most heavily used instruments in research areas today.

A Philips Scanning Electron Microscope (Model XL-30) was used for SEM analysis of the copper films. The sample is mounted on a sample holder and placed inside the microscope's vacuum column through an airtight door. After air is pumped out of the column, an electron gun present at the top of the column, emits a beam of high-energy electrons. This beam travels downward through a series of magnetic lenses designed to focus the electrons to a very fine spot. Near the bottom, a set of scanning coils moves the focused beam back and forth across the specimen, row by row. As the electron beam hits each spot on the sample, secondary electrons are knocked loose from its surface. A

detector counts these electrons and sends the signals to an amplifier. Final image is built up from the number of electrons emitted from each spot on the sample.

3.5 TRANSMISSION ELECTRON MICROSCOPY (TEM)

A transmission electron microscope (TEM) uses a beam of high-energy electrons to project a magnified image of a sample onto a fluorescent screen or other viewing device. Its optical configuration resembles a 35-mm slide projector with the sample taking the place of the photographic slide. A TEM uses electrons instead of light, and the sample removes energy from the beam due to electron scattering rather than light absorption.

A TEM illuminates an entire sample and uses electromagnetic lenses to focus the transmitted electrons into a highly magnified image. In contrast, a scanning electron microscope (SEM) scans a finely focused probe of electrons over the imaged area, simultaneously monitoring an induced signal. It maps the signal variations to form a 2-D representation of the sample surface. A TEM requires thin samples, typically 100 nm or less, that can transmit most of the incident electrons. It offers a resolution of 0.8 to 1Å, an order of magnitude better than the resolution of SEMs. Because TEMs can use atomic lattice of silicon substrate as an internal calibration standard, they can make very accurate dimensional measurements.

The interactions between electrons and sample atoms generate a number of secondary signals that find use in both TEMs and SEMs. Transmitted electrons are the primary imaging signal in TEMs. Secondary electrons (sample electrons ejected by beam electrons) and backscattered electrons (beam electrons scattered backward by collisions with sample nuclei) provide the primary imaging signals in SEMs. TEM can analyze transmitted electrons to determine the energy they lost when scattered in the sample. The energy loss indirectly characterizes the state and type of the scattering atom. Electron diffraction analysis can provide information about the crystalline structure of the sample.

3.5.1 FOCUSED ION BEAM SYSTEM (FIB)

A focused ion beam (FIB) instrument is used to prepare samples for TEM. A FIB instrument uses an ion beam to image the sample and to remove material from both sides of the desired section. FIB can also "polish" the sample to make it transparent to electrons in a TEM. [22]

Pre-thinning uses traditional mechanical methods to cut a sample from a wafer and thin it to about 10 to 50 nm. After initial thinning, the sample is glued on to the TEM sample grid and placed in the FIB instrument. The ion beam removes, or mills, material from both sides of the desired section, leaving a thin membrane for TEM examination. Ion beam current may be varied to look at the top and bottom sections. The entire process, from FIB milling to TEM observation, is performed at a throughput of 2-3 samples/day, which is larger by an order of magnitude than the conventional process consisting of mechanical polishing and ion thinning.

A beam of Ga ions is focused and scanned over the surface of the sample. The interaction of ion beam with the sample results in ejection of atoms from the surface and the production of secondary electrons and ions. The production of ejected neutral atoms is generally referred to as sputtering. If the beam is rastered over one area for a length of time, material will be removed from that area.

The FIB instrument is very similar to SEMs. The major difference is that the electron beam is replaced by a beam of gallium ions. The secondary electrons generated in the sample as the ion beam rasters over the sample produces images. The resolution of a FIB image is not as high as SEM because the ion beam diameter size is larger ~ 500A. The primary application for the focused ion beam is its use as an ion mill to remove material precisely.

The FIB used to prepare the samples for the present investigation was a FEI model 620 that uses a dual gallium beam source. The FEI Company Model 620 Dual Beam is a combined scanning electron microscope and 30 kV Ga focused ion beam system. In order to obtain the higher resolution imaging needed to characterize thin film samples with TEM, a sample thinning procedure is needed. A FEI model cm-20 TEM was used to characterize the wafers.

3.5.2 PROCEDURE FOR PREPARATION OF SAMPLE FOR TEM

A section of cleaved wafer is mounted similar to a cross section sample, mounted to a stainless steel sample mount. The sample is trenched and thinned from both sides with the Gallium gun FIB, until the sample is at the proper thickness, typically (500 to 1000 Å). The sample is cut, pushed over, and plunk out with (plunk out tools), and placed on a TEM grid for examination.

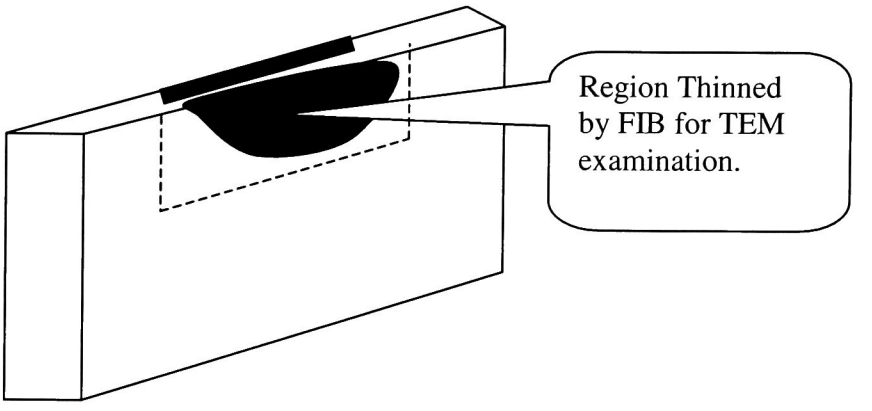


Figure 3. 1: Cross section of sample for TEM

3.6 RESULTS AND DISCUSSION

3.6.1 OPTIMIZATION OF DEPOSITION PARAMETERS

Figure 3.3 shows the plot of thickness of the copper films versus deposition time. At 400W of power, the thickness of the films deposited showed a polynomial variation with time. However, the rate of increase of thickness decreases with increase in power (at 800W) and decrease in pressure (to 2mtorr) with the rate of change becoming linear. Films deposited at 2 mtorr, 500W, for 15 min and a thickness of 1200 A were decided to be used for further runs as these parameters resulted in films with low stress. These films were stable and did not peel even after annealing at 600 °C in an argon atmosphere, unlike all the other films that peeled off by 450 °C of annealing. Figure 3.2 shows the optical micrographs at 40X magnification of the surfaces of the damaged films after annealing at temperatures from 300 to 400 °C.

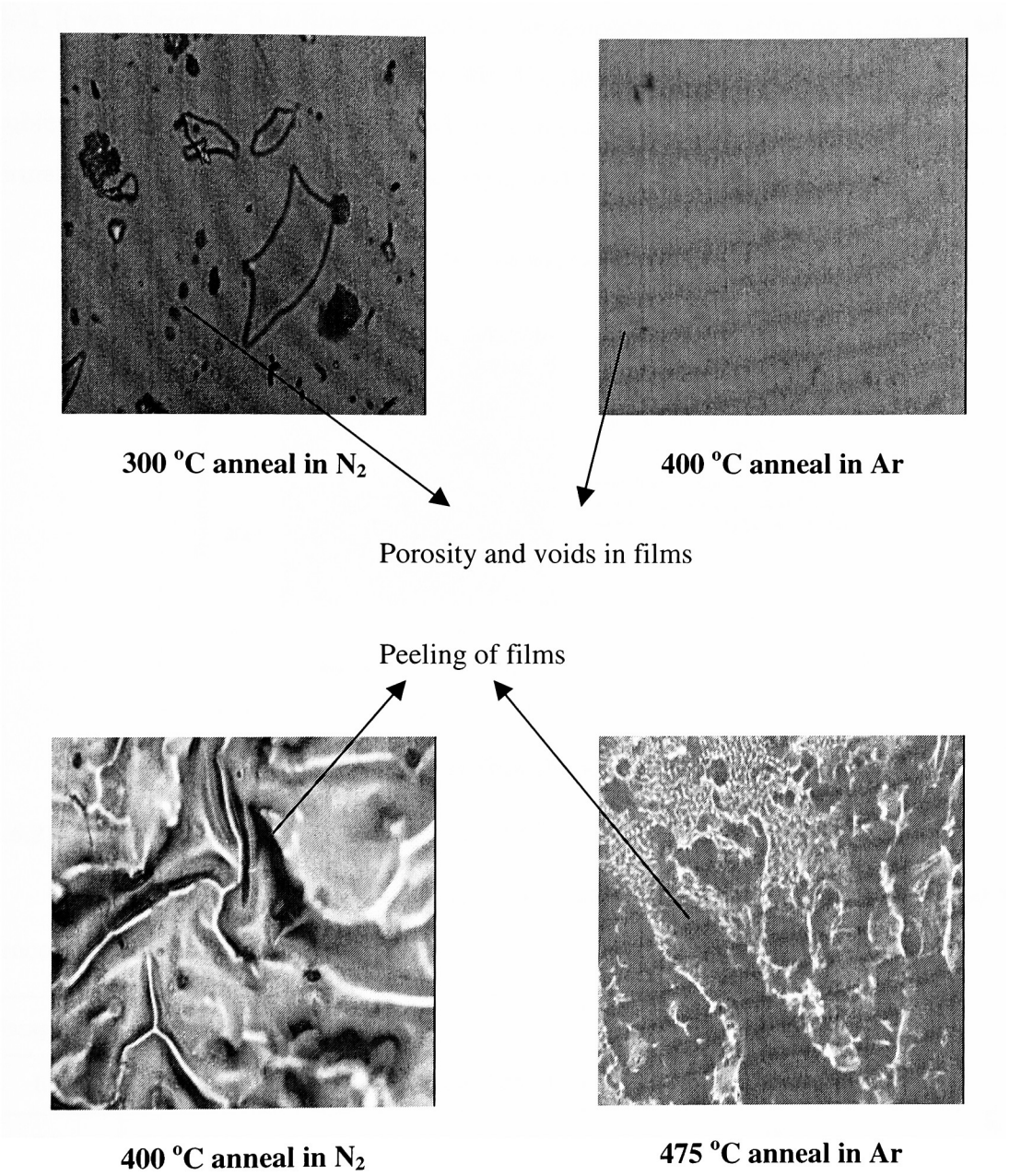


Figure 3.2: Optical micrographs of annealed films at 40X magnification

The annealing behavior of thin films shows dependence on the annealing ambient used. It was observed that films annealed in Ar atmosphere are stable up to 450 °C, while those annealed in N_2 are stable to only 300 °C. This is because of the inertness of the Ar ambient, while the N_2 gas has a small percentage of oxygen in it that accelerates the formation of copper oxide in the copper layer and causes the peeling of films.

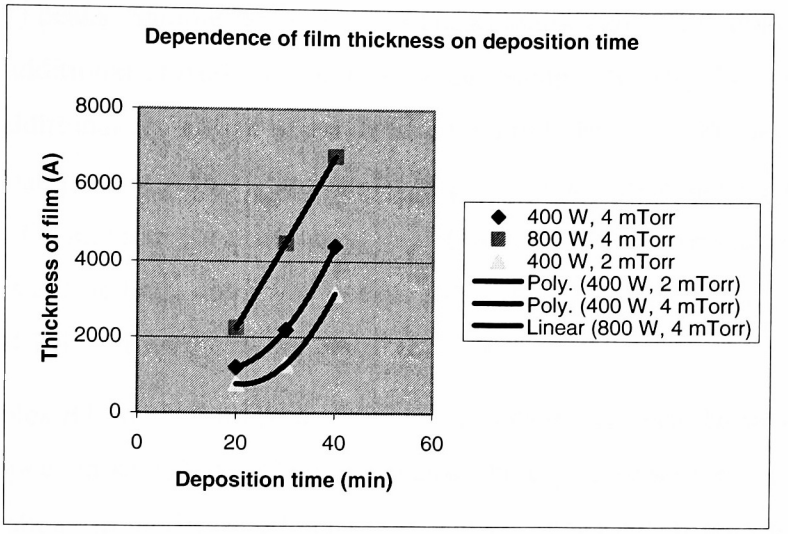


Figure 3.3: Dependence of film thickness on deposition time

3.6.2 X- RAY DIFFRACTION ANALYSIS

Seven samples were analyzed by XRD. Table 3.1 shows the sample IDs and the processing conditions of the films.

Sample ID	Film on Si/SiO_2	Annealing Temp (°C) in Ar Atm.
B1	TaN (1000 A) 12% N_2 flow + Cu (1200 A)	100
B2	TaN (1000 A) 12% N_2 flow + Cu (1200 A)	200
B3	TaN (1000 A) 12% N_2 flow + Cu (1200 A)	300
B4	TaN (1000 A) 12% N_2 flow + Cu (1200 A)	400
B5	TaN (1000 A) 12% N_2 flow + Cu (1200 A)	500
B6	TaN (1000 A) 30% N_2 flow + Cu (1200 A)	as deposited
B7	TaN (1000 A) 30% N_2 flow + Cu (1200 A)	400

Table 3.1: IDs of samples analyzed by XRD

All samples showed presence of (100) Si due to the wafer. XRD determined that sample B1 (fig 3.4) contains crystalline Cu [23], with no additional crystalline phase detected. Sample B2 (fig 3.5) contains Cu, a possible trace of Ta(N) [27], with no additional crystalline phase detected. Sample B3 (fig 3.6) contains major Cu, minor Ta_2N [24], Ta(N) [27] peaks. Sample B4 (fig 3.7) contains major Cu_2O [25] and moderate CuO [26], with no additional crystalline phase detected. Sample B5 (fig 3.8) contains major CuO with no additional crystalline phase detected. Sample B6 (fig 3.9) contains major Cu and a major broad peak at 2.56 Å. Sample B7 (fig 3.10) contains major Cu_2O [25], minor CuO, a trace of Cu and a major broad peak at 2.56 Å. The peaks observed at 2.56 Å are at a d-space that is a little large compared to fcc- TaN [34] peak (expected at 2.50 Å), which is a deviation of 2.4 % from the 'd' values of the bulk.

In samples B1 and B2, no peaks of tantalum nitride are seen. However Ta(N) and Ta_2N peaks appear in sample B3. This is because the crystallization of tantalum nitride that was amorphous in as-deposited state occurs after annealing to high temperature of about 300 °C. Formation of copper oxides in the annealed samples is discussed in section 3.6.4. The increase in lattice parameter of TaN in samples B6 and B7 may be explained as due to stresses in films, which probably originated from misfit with Si substrate and the defects such as interstitial sites and/or anti site atoms introduced during the nucleation of films, though the stress in the films was partly relaxed during annealing. There is no formation of copper silicide or tantalum silicides up to 500 °C. This shows that there is no diffusion of copper through the barrier and that tantalum nitrides act as an effective barrier in the annealing temperature of 100-500 °C.

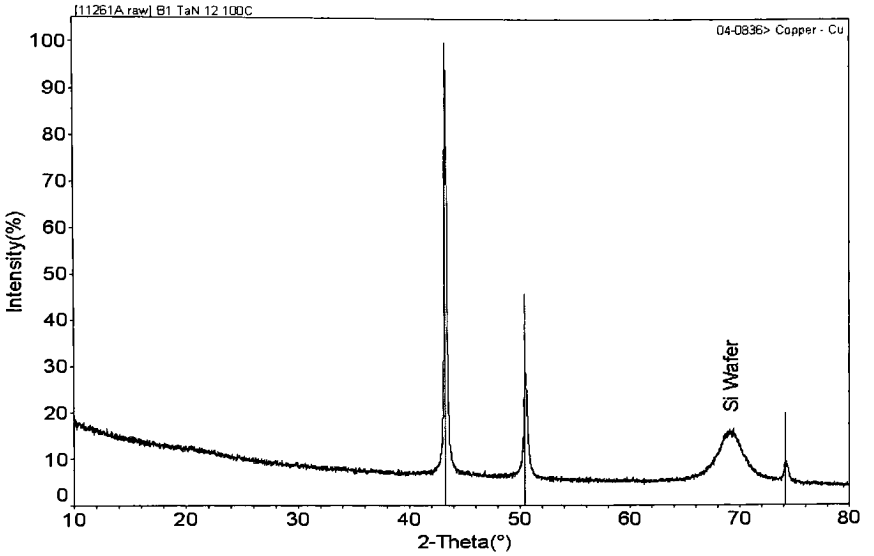


Figure 3.4: B1 – TaN (12% N_2 flow) /Cu on SiO_2/Si film annealed at 100 deg C

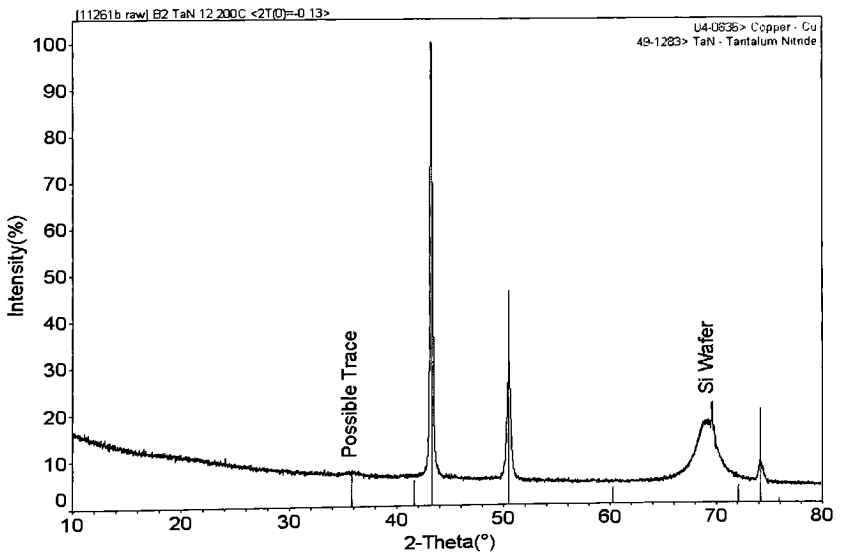


Figure 3.5: B2 – TaN (12% N_2 flow) /Cu on SiO_2/Si film annealed at 200 deg C

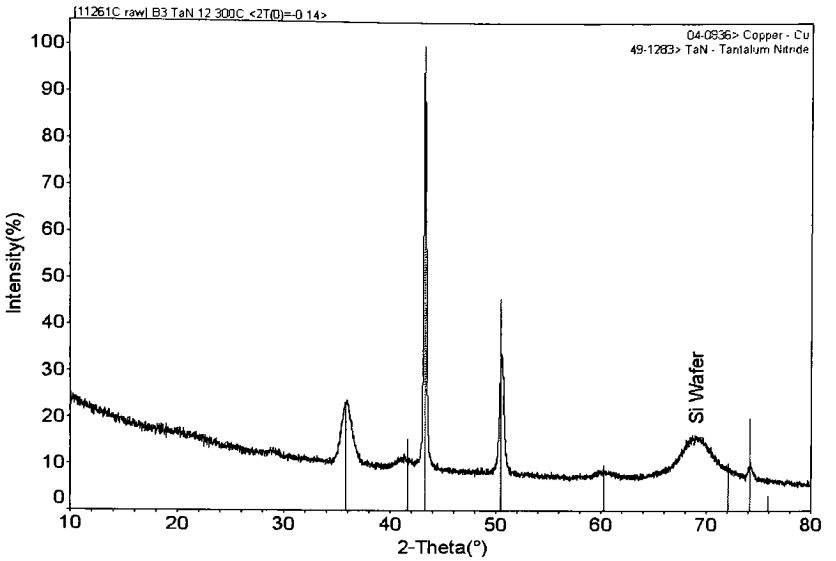


Figure 3.6: B3 – TaN (12% N_2 flow) /Cu on SiO_2/Si film annealed at 300 deg C

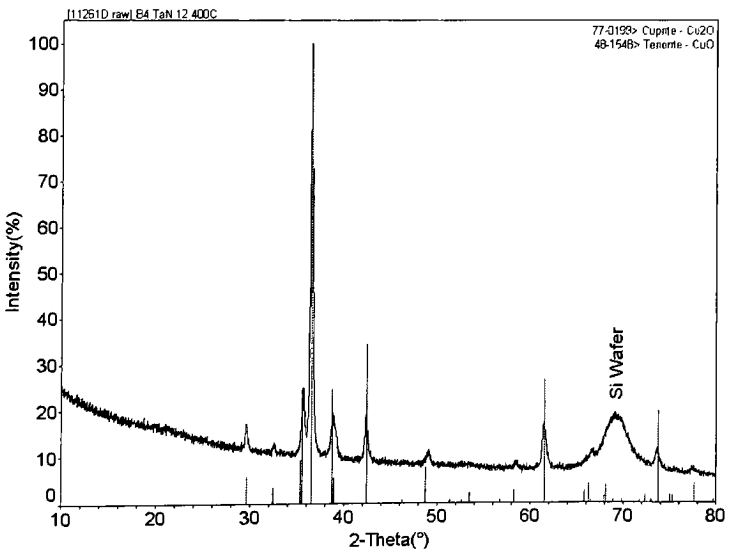


Figure 3.7: B4 – TaN (12% N_2 flow) /Cu on SiO_2/Si film annealed at 400 deg C

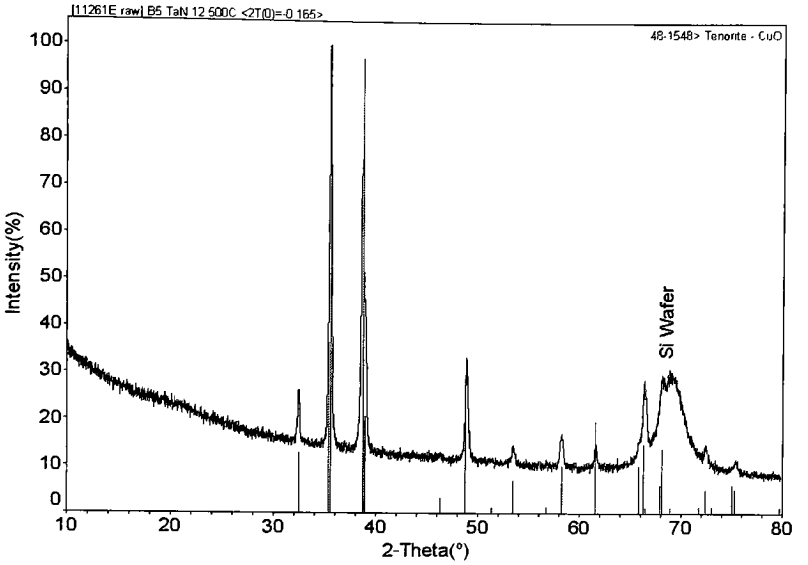


Figure 3.8: B5 – TaN (12% N_2 flow) /Cu on SiO_2/Si film annealed at 500 deg C

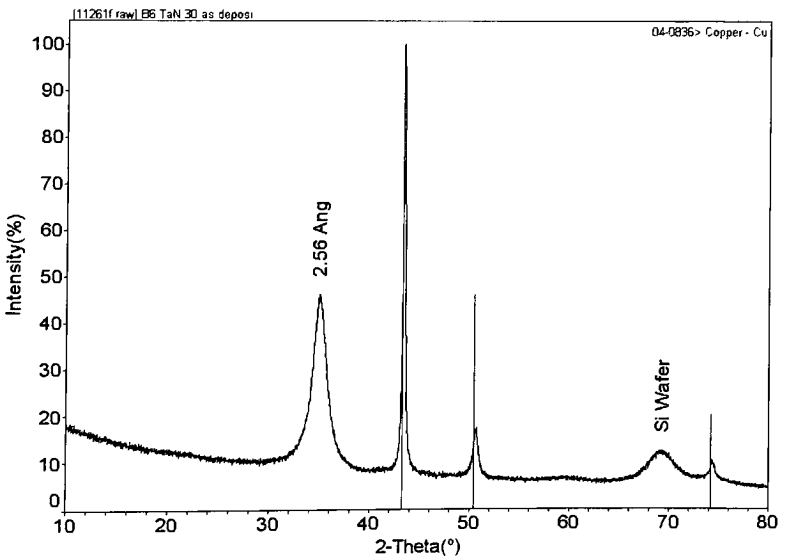


Figure 3.9: B6 – TaN (30% N_2 flow) /Cu on SiO_2/Si film as- deposited

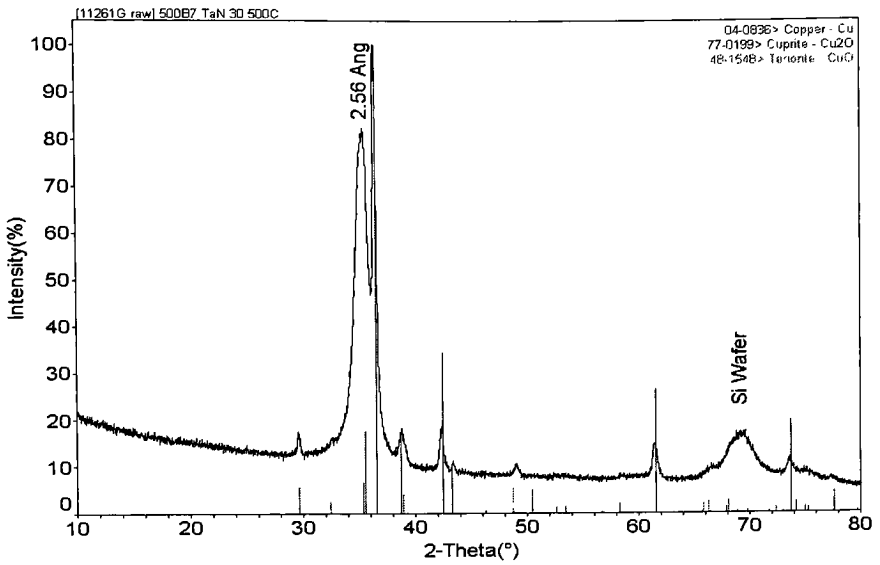


Figure 3.10: B7 – TaN (30% N_2 flow) /Cu on SiO_2/Si film annealed at 500 °C

3.6.3 TEM AND SEM ANALYSIS

The cross-section of TEM micrograph of the $Cu/Ta_2N/Si$ structure at 20,000X magnification, before heat treatment in figure 3.11 shows that the metal layers are uniform and planar. There is no evidence of reaction or intermixing at any interface. The artifact observed on the top surface of the film is due to the imaging process.

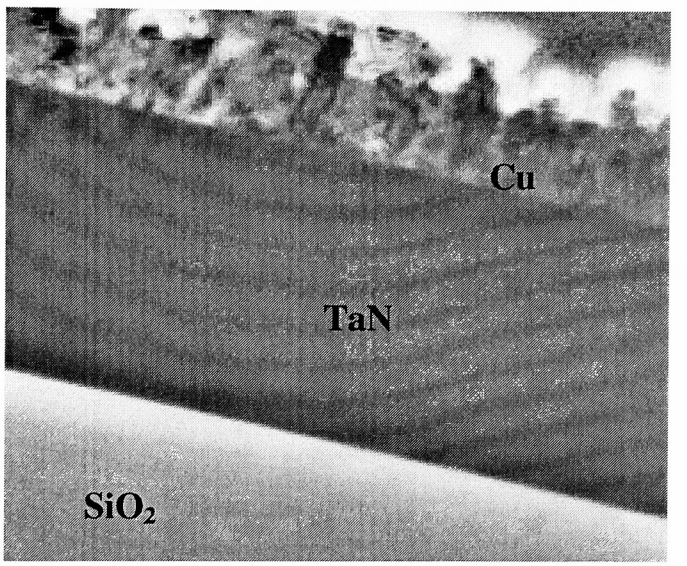


Figure 3. 11: Cross –section showing the interface of the $Cu/Ta_2N/SiO_2$

The sample annealed at 600 deg C is non-uniform. The surface constitutes rough, grey areas typical of oxidized Cu films. In the present investigation, no detailed work was done using TEM to look at the interfaces, phases, and grain growth in the annealed films because of difficulty in preparation of samples. Stresses and formation of surface oxide in the annealed films caused difficulties during sample preparation because of the peeling of the films. However, SEM pictures of the copper film surface at a magnification of 40,000X before and after annealing do not show any significant change in grain size. However there are a lot of voids present after annealing due to the formation of copper oxides. (Refer figures 3.12-3.15)

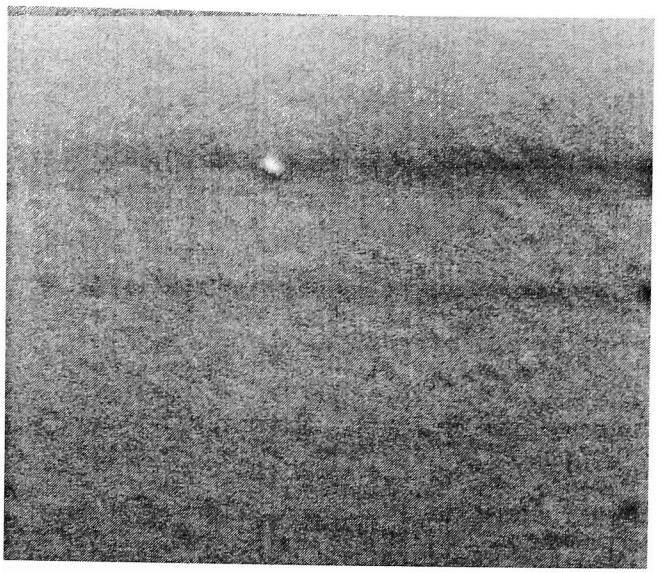


Figure 3.12: SEM picture of surface of Cu as – deposited at 20,000X mag

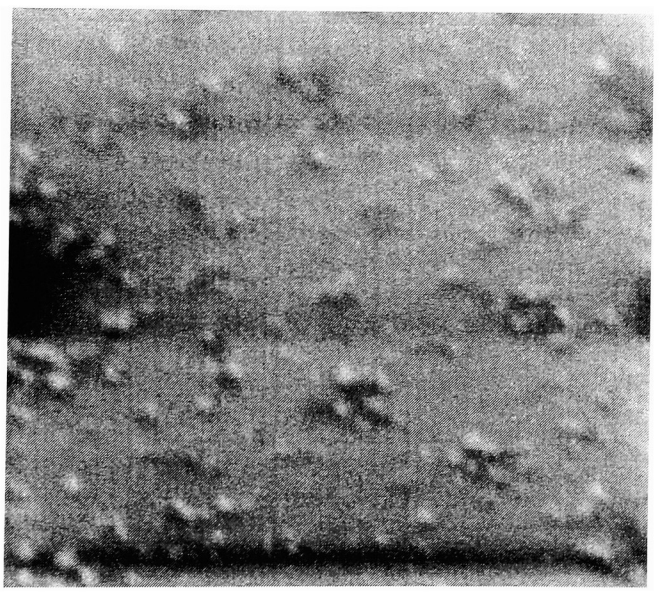


Figure 3.13: SEM picture of Cu annealed at 450 ^{o}C inside a void

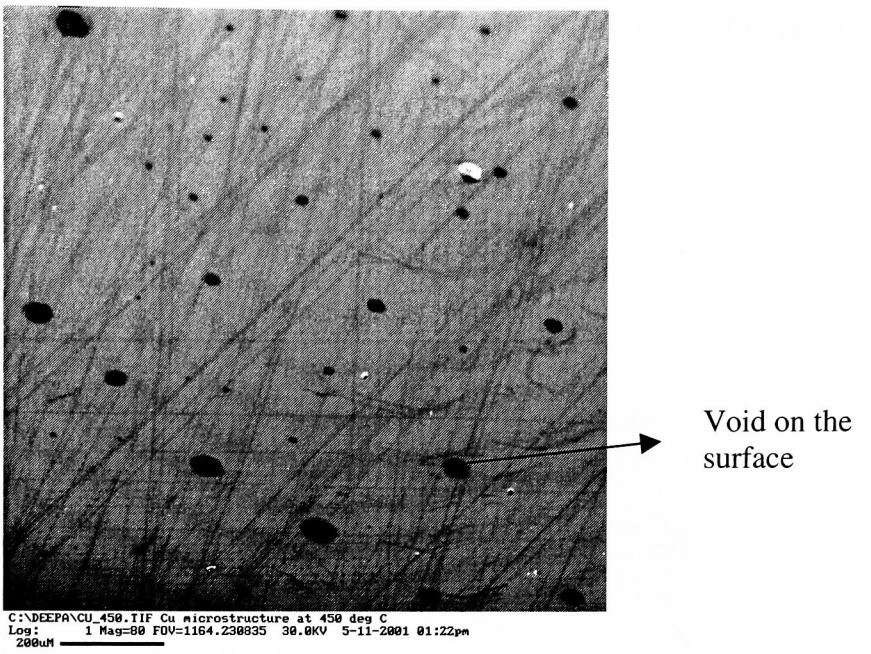


Figure 3.14 : SEM picture of Surface of Cu at 450 ^{o}C at 80X mag

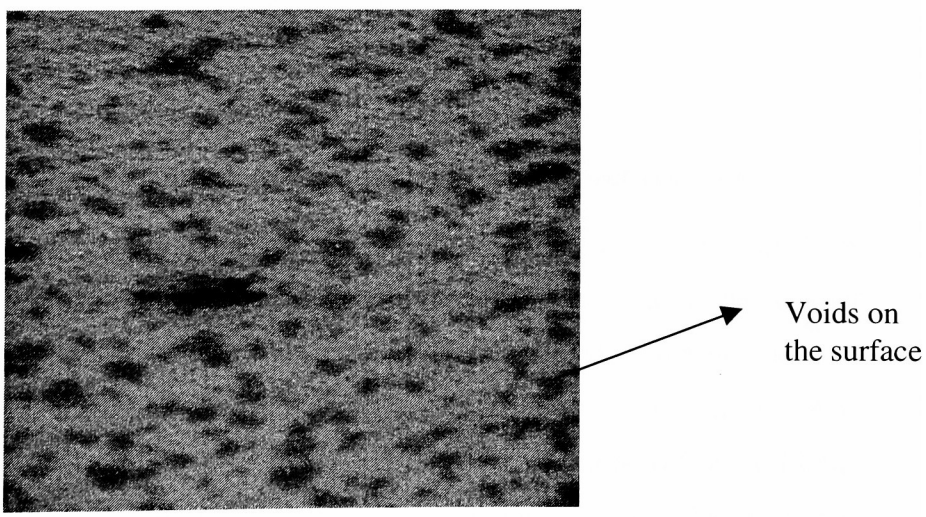


Figure 3.15: SEM picture of microstructure of Cu at 500 ^{o}C at 20,000 mag

3.6.4 EFFECT OF ANNEALING ON RESISTIVITY AND CRYSTAL PHASES

The measured resistivity was dominated by copper film since the latter is thicker and has markedly lower resistivity than that of TaN. The copper film structure has transformed from high conductivity to high resistivity.

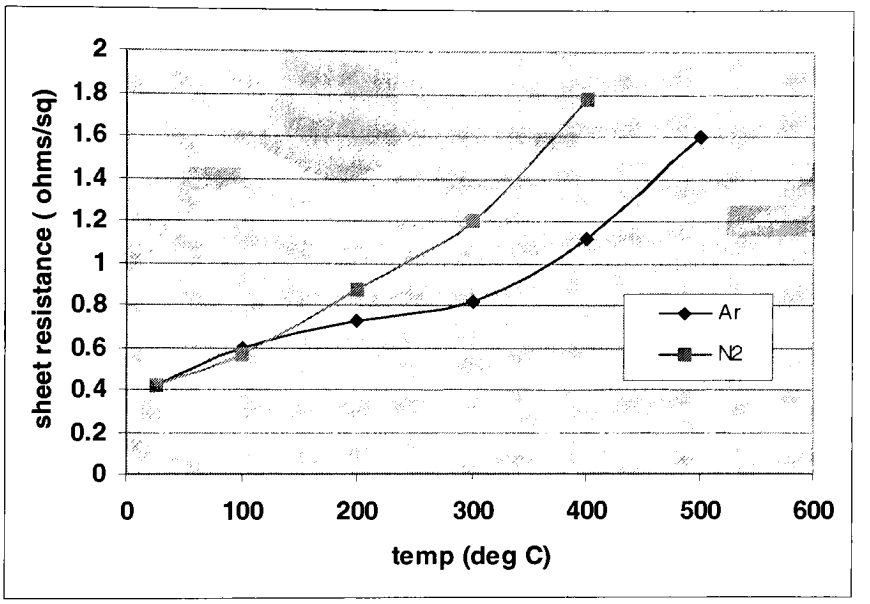


Figure 3.16: Effect of temperature and ambient on the sheet resistance

As the temperature of annealing is increased, there is a steep increase in resistivity. This is due to the formation of copper oxides. This is also seen by the change in the color of the samples. The increase in resistivity is more for samples annealed in nitrogen because of the presence of oxygen in the nitrogen atmosphere. The reddish color seen in 200°C annealed sample is due to the formation of Cu_2O phase. This converts to CuO at higher temperature, which is grey in color. The change in physical appearance of the samples is summarized in table 3.2.

Annealing temp (^{o}C)	Physical appearance of sample
RT	Copper color
100	Copper color
200	Reddish pink
300	Maroon
400	Bluish grey
500	Silvery grey, Cu peels off

Table 3.2: Physical Appearance of sample at various annealing temps

Copper is oxidized near the surface first. As oxidation proceeds with the growth of oxides in copper, the layer becomes progressively more resistive. Cu oxide exists in two stable forms: cuprous oxide, Cu_2O, (p-type semiconductor) and cupric oxide, CuO (insulator). In the initial stage of Cu oxidation, there is mainly growth of Cu_2O film. When Cu_2O film grows over 400-1000 Å, CuO film starts to grow on the surface of Cu_2O. The rate of Cu oxidation at various temperatures is shown in figure 3.18. [14].

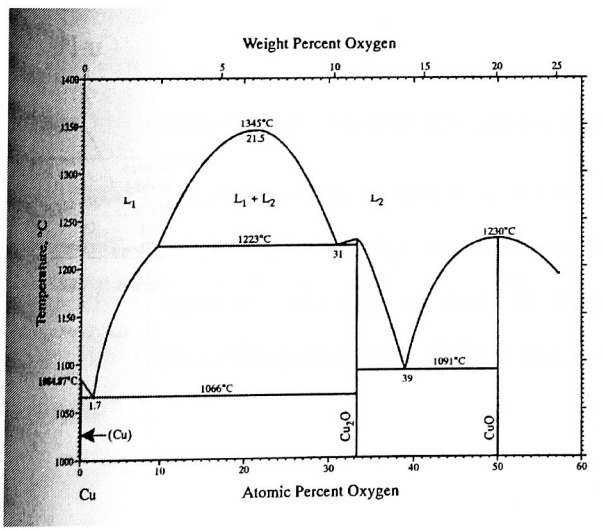


Figure 3.17: Binary phase diagram of Cu and O

It is generally accepted that copper ions are the dominant moving species during the formation of Cu_2O on copper. However, the power law of growth rate of Cu_2O phase is strongly dependent on the temperature range and partial pressure of oxygen. For further oxidation of Cu_2O to CuO, the oxidation rate becomes approximately independent of the oxygen pressure. Preferential oxidation in some planes was found in the order of (100), (111) and (110) copper faces, with the (100) face having the highest oxidation rate [36]. The binary phase diagram of Cu-O is shown in figure 3.17. [35]

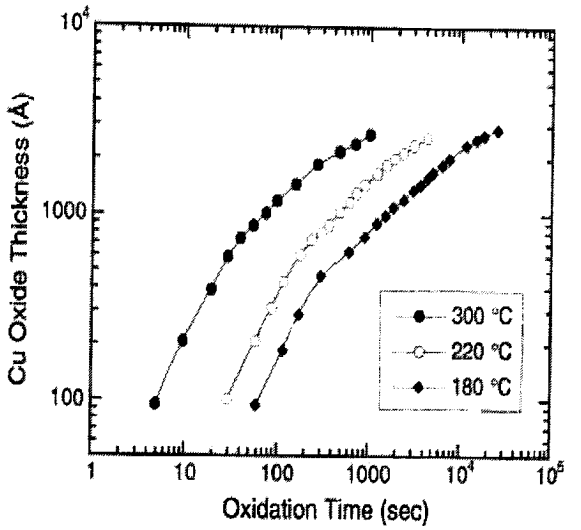


Figure 3.18: Oxidation rate of copper at various temperatures

Cu_2O is a red-colored direct-gap semiconductor material. It has a simple cuprite structure with a lattice constant of 4.2967 Å. CuO film has a dark iron-grey color. CuO has a complicated monoclinic tenorite structure as seen in figure 3.19. The unit cell contains four CuO molecules. The lattice parameter of CuO is a = 4.687 Å, b = 3.4226 Å, c = 5.1288 Å and $\beta = 99.54\ ^{\circ}$.

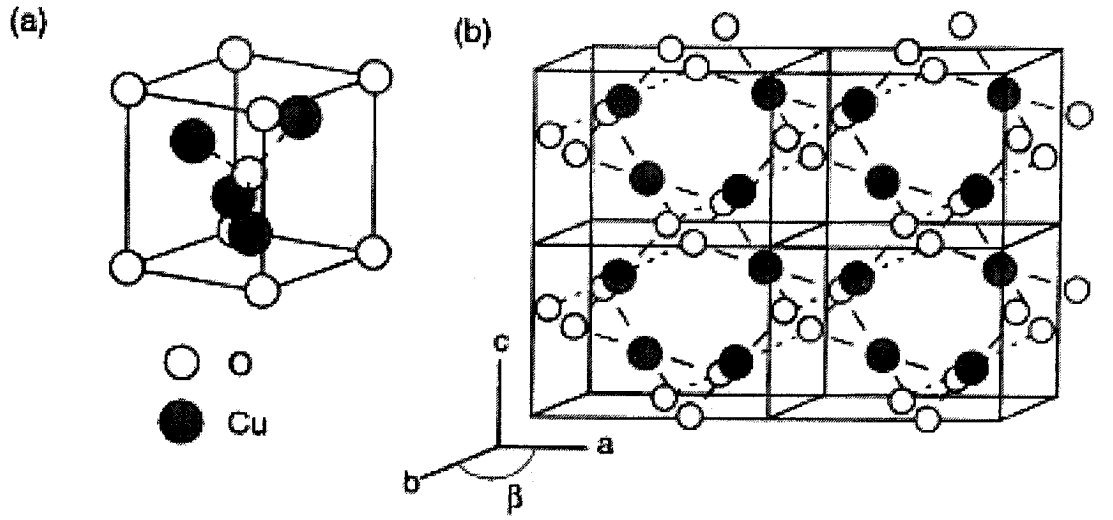


Figure 3.19: Crystal structure of copper oxides (a) cubic Cu_2O (b) monoclinic CuO

The oxidation mechanism of refractory metal nitrides is different from that of copper because the diffusion of silicon atoms through these materials is absent. Oxidation proceeds by diffusion of oxygen through the growing oxide layer. Nitrides can withstand prolonged heat treatments up to 1000 deg C if the annealing atmosphere is inert. [18]

3.7 STRESSES IN FILMS

All films irrespective of the method of deposition exist in a state of stress. They directly affect a variety of phenomenon, including adhesion, generation of crystalline defects, and formation of film surface growths such as hillocks and whiskers. The film stresses also influence band gap shifts in semiconductors. The stress consists of two components – thermal stress and an intrinsic stress. Thermal stress is due to the difference in thermal expansion of the coating and substrate materials. Intrinsic stress is due to the accumulating effect of crystallographic flaws that are built into the film during deposition. These stresses are strongly dependent on the deposition conditions and they strongly influence the performance of films. The parameter T/T_m, where T(K) is the substrate temperature and T_m is the coating material melting point, is particularly important in understanding the stress related behavior for differing materials. The

microstructure and thus the intrinsic stresses in vacuum deposited coatings are sensitive to the deposition conditions. Figure 3.20 is a schematic representation of the microstructure dependence of sputtered films on T/T_m and on the pressure of the working gas. The growth of vacuum deposited coatings involves atoms 1) arriving in a distribution that depends through self shadowing on the coating atom arrival directions, and on the roughness of the coating surface, and then 2) diffusing over the surface until they become trapped in low energy sites and are incorporated into the growing coating. Finally, these deposited atoms may readjust their positions within the coating lattice by recovery and recrystallization.

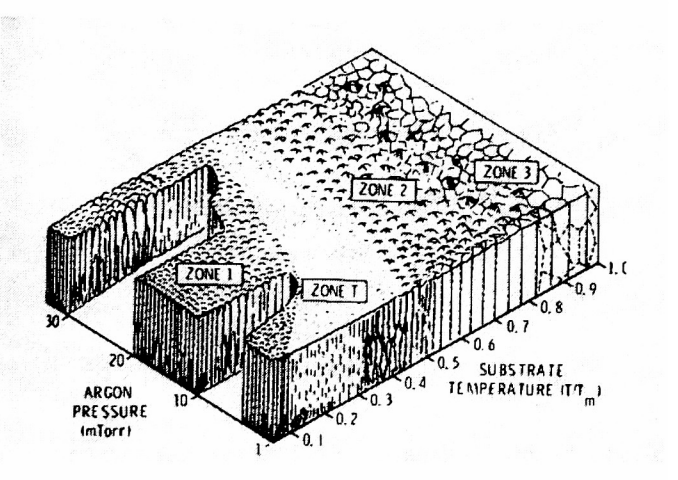


Figure 3.20: Schematic of dependence of microstructure of sputtered films on pressure, temperature [30]

The T/T_m dependence results because surface diffusion processes, like the bulk diffusion processes that characterize recovery and recrystallization are dependent on T/T_m. The pressure dependence is believed to result because collisions between the sputtered atoms and the Ar atoms at elevated pressures cause the depositing atoms to arrive at the substrate in randomized directions that promote shadowing.

Films deposited in the zone T (transition) region have a dense fibrous structure with a smooth, highly reflective surface. They form on smooth substrates at low T/T_m

when the coating flux arrives in a direction that is largely normal to the substrate surface, so that shadowing effects are minimized. Large stresses can form in the zone T region.

Films in the zone 1 region are characterized by a structure consisting of tapered crystals separated by open, voiding boundaries. This structure results from shadowing because high points on the growing surface receive more coating flux than valleys do, particularly when a significant oblique component is present in the arriving coating flux. The extreme zone 1 structure is too porous to support stresses and has a rough, poorly reflecting surface. The zone 2 structure consists of columnar grains separated by distinct, inter-crystalline boundaries. Recovery limits the intrinsic stresses in zone 2. Zone 3 is defined as that range of conditions where bulk diffusion has a strong influence on the final microstructure of the film. Re-crystallization occurs if sufficient stress is built into the film during deposition. Recovery and/or re-crystallization limit the intrinsic stresses in this region.

In sputtered films, generalization with respect to stress is difficult to make because of the plasma environment and the effect of working gas. Low sputtering pressures, with light sputtering gases, high-mass targets, and low deposition rates favor films with compressive intrinsic stresses.

3.7.1 STRESS MEASUREMENT

The Surface Metrology tool used to measure stresses in the films for this study is the Dektak 8000. This bench top model provides extremely accurate measurements of step heights, stresses and micro roughness for a wide variety of applications, including on semiconductor wafers, magnetic disks, sliders and thin film heads. The system provides a maximum of 65,400 data points per scan for high horizontal resolution and excellent baseline stability for superior measurement repeatability. The DEKTAK 8000 includes a programmable X-Y-Theta stage for samples up to 200mm to create an automated sequence with multiple scans at multiple locations. Optional features include the low inertia sensor and 3-D surface area analysis software.

To measure stress on the composite film of TaN – Cu deposited on the thermally grown SiO_2 wafer, the first step is to pre-measure stress on the SiO_2 wafer using the Dektak and the pre-measured file will be automatically saved in the hard drive. After

depositing TaN/Cu on the wafer it is post-measured for stress again. Then a program called "Compute Stress" is run. In order for this program to work the thickness of the substrate and the thickness of the film deposited should be known. Based on this data, the program automatically analyzes the pre and post measured files to give the stress on the deposited films. Tables 3.3 a and b summarize the results and the plots obtained are shown in figures 3.21 and 3.22.

Film	
Pre – measured	Si/SiO_2
Post - measured	Si/SiO_2 /TaN/Cu

Film ID	**Processing Conditions**	**Stress (dynes/cm^2)**
IN 2A	As – deposited	$-1.153 * 10^{10}$
IN 1A	Annealed at 500 °C, 20 min, N_2	$-8.444 * 10^{9}$

Table 3.3: (a) Stack of films measured (b) Stress data

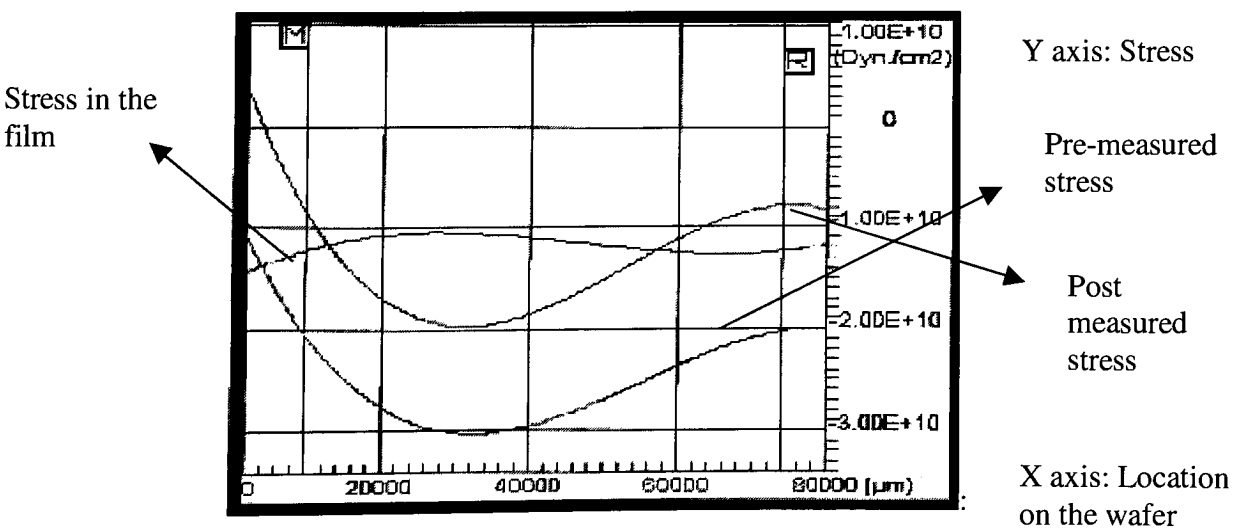


Figure 3.21: Stress on as-deposited film IN 2A

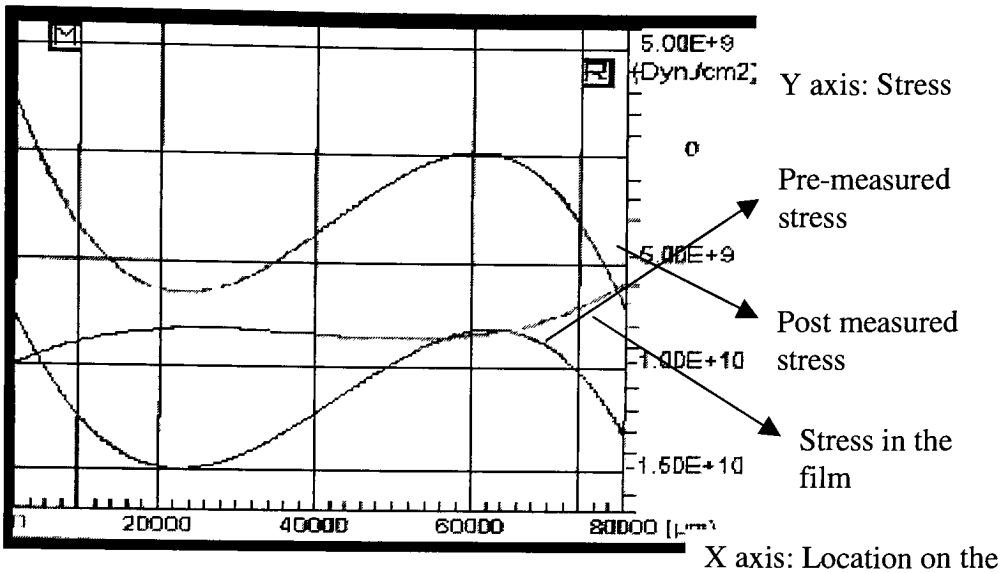


Figure 3.22: Stress in annealed film IN 1A

The compressive stresses are caused by energetic argon atoms that originate at the cathode (target) surface. It is not clearly understood whether the argon atoms produce stresses by becoming trapped in the deposited film or by driving surface atoms into the film. The copper and tantalum nitride films are formed in the zone T region of the schematic in figure 3.20 and therefore have a smooth interface, dense structure with high stress. For good barrier properties and good adhesion with Cu, an ideal barrier reacts with Cu to some self-limiting extent. Since adhesion of the thin film is determined by competition between thermal stress and physical/chemical bonding, the chemical bonding due to interface reaction such as that between Cu and Ta would enhance it. When the shear stress at the film substrate interface increases, the films peel off. However, if the peeling does not occur, mechanical failure may take place and stress relief occurs by means of a fracture, or buckling of the film, or by plastic flow if the stress exceeds the yield strength of the film. Fracture or buckling will take place depending on whether the net stress is tensile, or compressive, respectively. There is a slight reduction in the total stress of the films after annealing and the stresses are compressive. So buckling is observed in a few films as shown in figure 3.23.

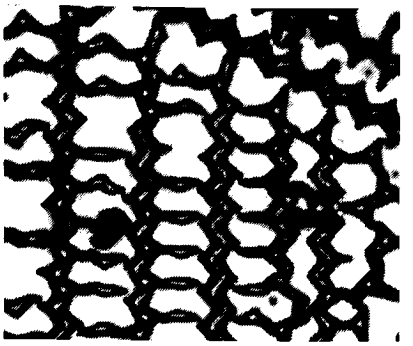


Figure 3.23: Buckling pattern on the surface of copper films

3.8 RBS ANALYSIS – RESULTS AND DISCUSSION

The processing conditions of films along with the sample IDs analyzed by RBS are shown in table 3.4.

Sample ID	TaN	Annealing Temp (deg C) in Ar ambient
A1	TaN (12% N) 1000 A + Cu 1200 A	100
A2	TaN (12% N) 1000 A + Cu 1200 A	200
A3	TaN (12% N) 1000 A + Cu 1200 A	300
A4	TaN (12% N) 1000 A + Cu 1200 A	400
A5	TaN (12% N) 1000 A + Cu 1200 A	500
A6	TaN (30% N) 1000 A + Cu 1200 A	200
A7	TaN (30% N) 1000 A + Cu 1200 A	400
A8	TaN (30% N) 1000 A + Cu 1200 A (Cu film peeled a little)	550

Table 3.4: IDs of samples analyzed by RBS

Sample A1 in figure 3.24 shows no evidence for Ta by RUMP simulation. The Cu layer appears to have pinholes. It is not clearly understood why Ta could not be detected in the simulation. The same sample, however, showed presence of tantalum nitride phase in XRD analysis. In a RBS spectra the position of a peak and the area in a peak, is dependent on the nature of the element and its location in the sample. Therefore the position of Cu and Ta in the spectra is dependent on their location in the film stack and the thickness of the films. It is possible that in the present situation, the Cu and Ta peaks are overlapped in the regions between channel lengths 300-410. The presence of pinholes on the copper layer is confirmed by the irregularities seen in the peak.

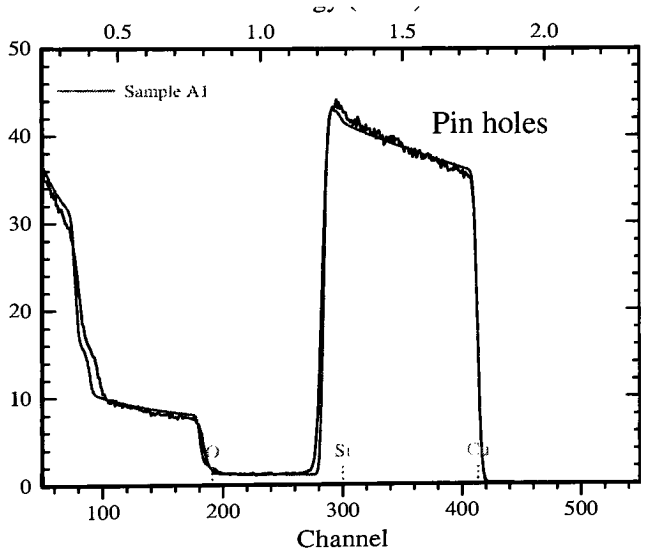


Figure 3.24: Sample A1 TaN (12% N_2 flow) /Cu on SiO_2/Si film annealed at 100 °C

RUMP simulation of sample A2 in figure 3.25 shows no evidence for Ta. Cu has pinholes (but less than A1).

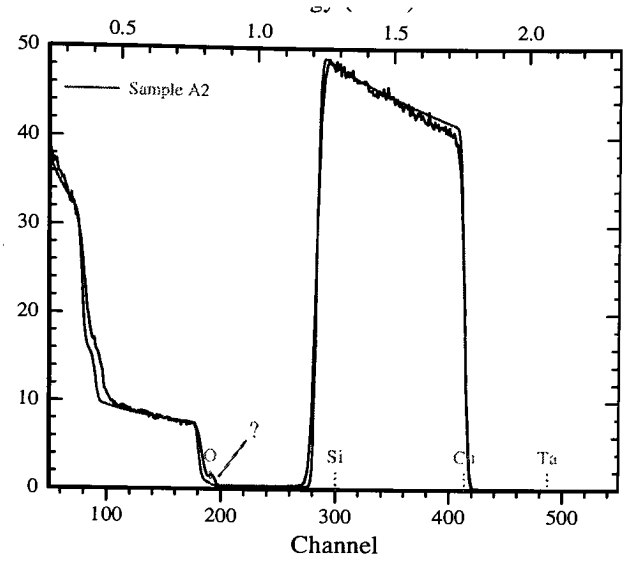


Figure 3.25: Sample A2 TaN (12% N_2 flow) /Cu on SiO_2/Si film annealed at 200 °C

Rump simulation of sample A3 in figure 3.26 shows no evidence for Ta. About 4/5 of the Cu layer is oxidized. The peak at channel 260-280 is Cu with less oxygen (than the surface region) near the interface with SiO_2.

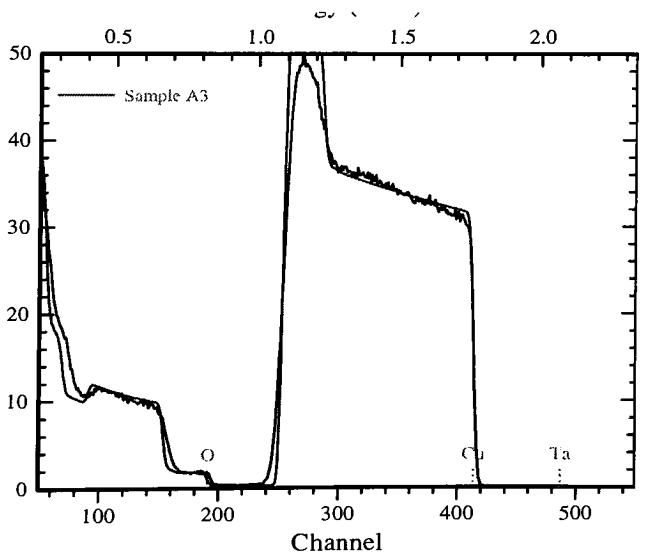


Figure 3.26: Sample A3 (12% N_2 flow) TaN /Cu on SiO_2/Si film annealed at 300 °C

Rump simulation of sample A4 in figure 3.27 shows no evidence for Ta. About 1/3 of the Cu (near the surface) is oxidized, the other 2/3 (near SiO_2) are less oxidized. It is believed that samples A1, A2 and A3 do not show any interaction between Cu and Ta because the line of the spectra between channel lengths 300-400 remains unchanged in all the spectra. There is formation of copper oxides. This is seen in samples A3 and A4 with the copper peak moving from 300 to 260 across the channel and the interaction of copper and oxygen peaks. However the change in slope across the channel position between 300 and 400 in sample A4 (figure 3.27) is believed to be the interaction between Ta and Cu.

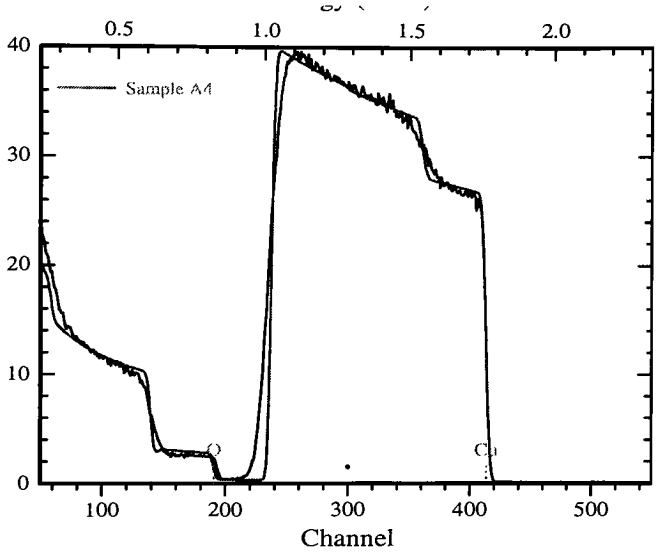


Figure 3.27: Sample A4 TaN (12% N_2 flow) /Cu on SiO_2/Si film annealed at 400 °C

Rump simulation of sample A5 in figure 3.28 shows no evidence for Ta. The entire Cu layer is oxidized. This is seen in the simulation by the small blimp at channel position of 200.

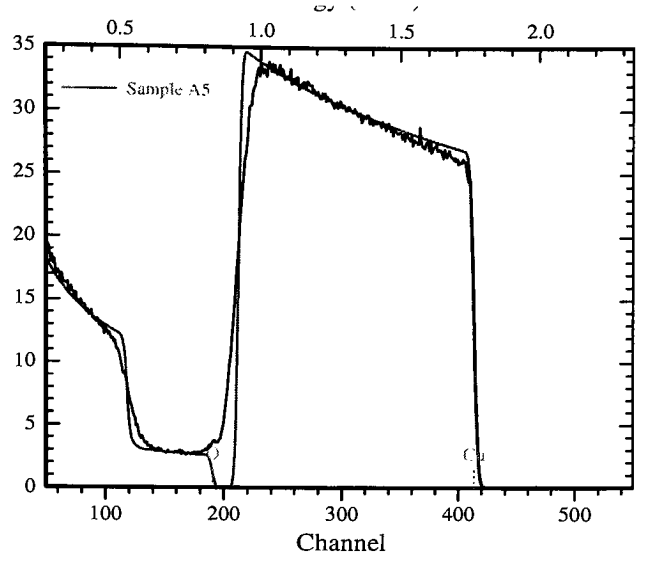


Figure 3.28: Sample A5 TaN (12% N_2 flow) /Cu on SiO_2/Si film annealed at 500 °C

Rump simulation of sample A6 in figure 3.29 shows the first layer as Cu with pinholes or oxide. The second layer is approximately 35% Ta and 65% N. RBS measurements of lighter elements are more difficult due to the low signal-to-background ratio. Therefore, the estimation of nitrogen content in the films may not be accurate. The surface is rough or the interfaces are somewhat mixed.

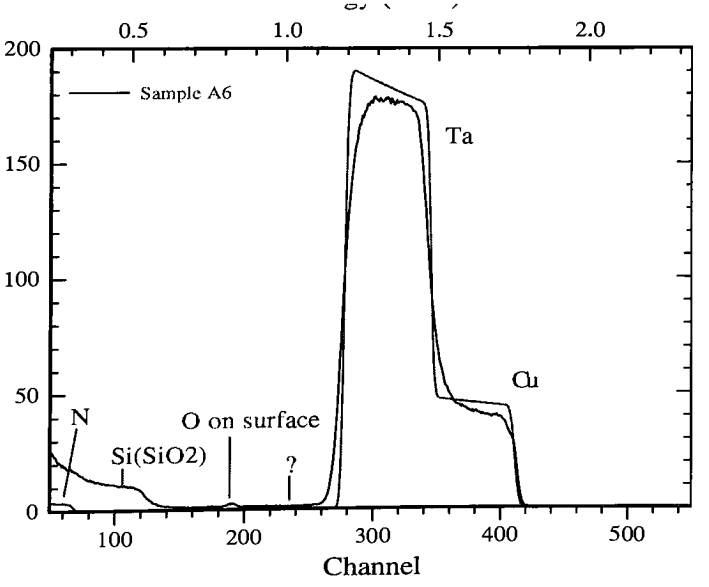


Figure 3.29: Sample A6 TaN (N_2 flow 30%) /Cu on SiO_2/Si film annealed at 200 °C

Rump simulation of sample A7 in figure 3.30 shows that the first layer is approximately 40% Cu and 60% O. There could be some Si too. The second layer is approximately 40% Ta and 60% N. the surface is rough or the interfaces are very mixed.

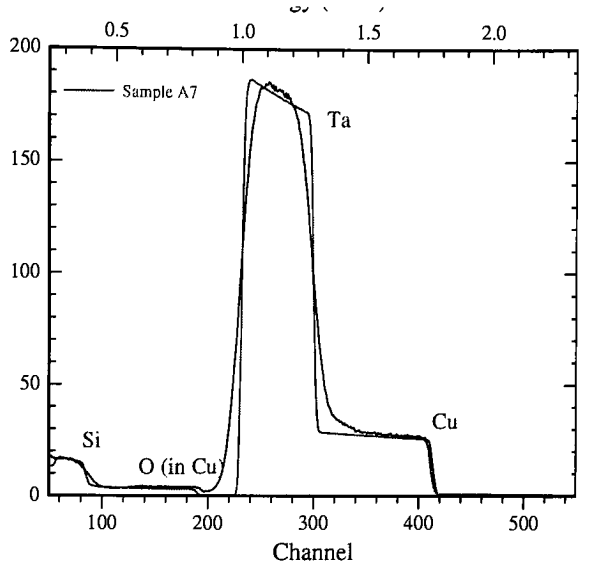


Figure 3.30: Sample A7 TaN (N_2 flow 30%) /Cu on SiO_2/Si film annealed at 100 °C

RUMP simulation of sample A8 in figure 3.31 shows very thin residual layers of Cu and Ta on the surface. This sample was used to obtain the thickness of the SiO_2 layer (RUMP calculates 9000 A of SiO_2), and this thickness was used for the rest of the samples.

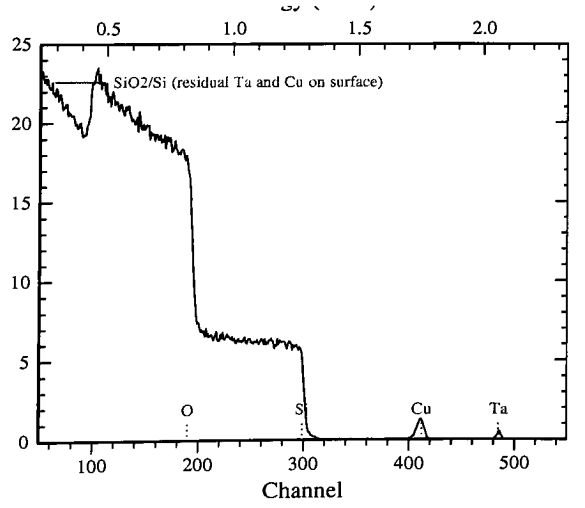


Figure 3.31: Sample A8 TaN (N_2 flow 30%) /Cu on SiO_2/Si film annealed at 550 °C

It is not clearly understood why films A1 A5 with tantalum nitride sputtered with a N_2 flow 12%, do not show any presence of tantalum in the RUMP simulation of RBS spectra. The same samples, however, showed tantalum nitride phases in XRD analysis. The samples that contained tantalum nitride sputtered with 30% N_2 flow do show the presence of Ta as a second layer in the $Si/SiO_2/TaN/Cu$ stack. The atomic concentration of nitrogen in the films could not be determined accurately because of its low atomic weight. However, it has been seen in the XRD spectra in section 2.7.2 that the nitride films sputtered with 30% N_2 flow for cubic TaN while those with 12% N_2 flow form Ta_2N.

According to the Cu-Ta-N ternary phase diagram shown in figure 3.32 (a), Cu is thermodynamically stable with respect to Ta, Ta_2N, and TaN. However, the ternary phase diagram drawn from the Gibbs free energy data at 900°K in figure 3.32 (b) shows that both tantalum and its nitrides are thermodynamically not stable with respect to Si. However, this high temperature is not reached in this investigation.

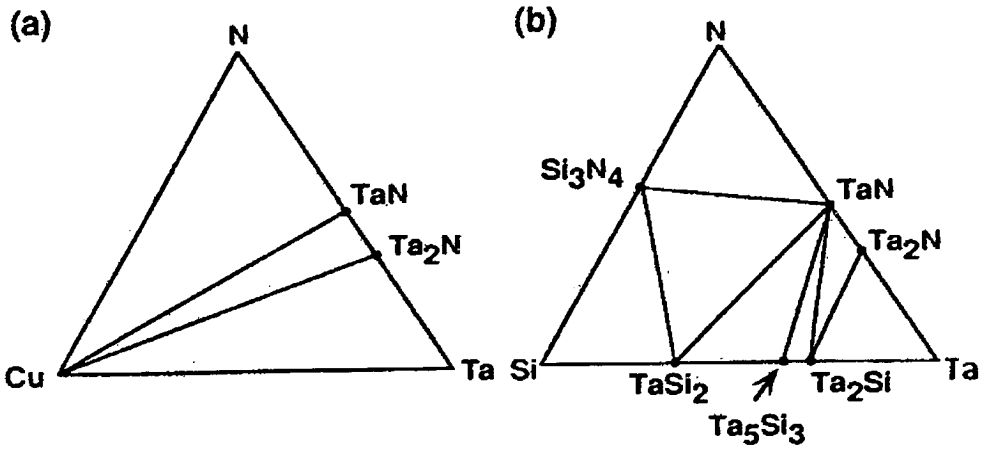


Figure 3.32: Isothermal section of ternary phase diagram of (a) Cu-Ta-N and (b) Ta-N-Si systems drawn at 900 K

There is no surface Ta present in as – deposited state in films A6 and A7 indicating that there is no diffusion of Ta. However, there appears to be some interaction between Cu and Ta when the sample was annealed to 500 °C. This is seen in the slope at the interface

in figure 3.30. It has been reported in the literature that the barrier failure of tantalum and its nitrides occurs by two different mechanisms. One is the diffusion of Cu into the Si substrate through the barrier layer resulting in the formation of Cu_3Si precipitates in the Si substrate. The other is by the chemical reactions between the barrier layer and the Si substrate. In the present study, outdiffusion of barrier is observed, while there is no formation of copper silicides. So, the barrier layer fails by the second mechanism. It is also observed that TaN films are more stable than Ta_2N films with the Ta in Ta_2N films showing interaction with copper at 400 °C while the Ta in TaN films do not show any outdiffusion. It has been reported in literature[20] that The chemical shift of Ta 4f electrons due to the formation of nitrides is 0.6 eV for films with 15 % N and it is 1.2 eV for films with 30 % N.. This shows the chemical bond in TaN is stronger than in Ta_2N. 12 % N has Ta_2N phase while the 30 %N has TaN phase. Therefore, we can conclude cubic tantalum nitride films act as an effective adhesion and diffusion barrier layer up to 500 °C in an inert ambient for copper metallization.

4. ELECTROLYTIC PLATING OF COPPER

4.1 BACKGROUND

As the technology is progressing to sub quarter micron feature sizes, it is necessary to have conformal deposition of copper in the trenches and vias. Copper electroplating has emerged as the preferred method because:

- Plated copper has a more desirable metallurgical structure (low stress, equiaxial, ductile).
- Plating provides improved filling of trenches and vias (less tendency for voids to form).
- The tools and processes used in plating are more scalable to large-format substrates.
- The processing time for plating is faster, thus providing higher throughput.
- Factoring in tooling, raw materials, and maintenance, plating is a relatively low-cost manufacturing process.

A basic copper interconnect process contains three layers that includes a barrier layer, seed layer, and copper electro fill layer. A typical cross section is shown in figure 4.1.

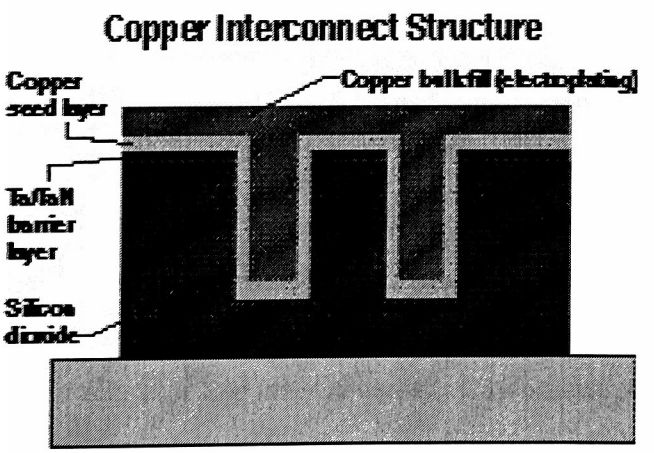


Figure 4.1: Dual damascene architecture, PVD-deposited tantalum-based diffusion barriers and copper seed layers, and electroplated copper fill. [11]

The amount of copper that is deposited during electrolytic plating can be estimated by using *Faraday's Law*. It states that in the absence of any secondary reactions, the current delivered to a conductive surface during electroplating is directly proportional to the amount of product formed, or in other words, "the mass of product formed is proportional to the electrochemical equivalent weight of the product." Using Faraday's law and Faraday's constant the following relationship can be derived to find the theoretical deposited weight.

$$\text{Weight deposited} = \frac{63.546\,\text{g/mol x (amps x time)}}{2 \text{ x } 96{,}500} \qquad \text{---------- (1)}$$

The thickness of the film during electroplating can be calculated as follows:

$$\text{Density} = \frac{\text{mass deposited}}{\text{volume}} \qquad \text{----------(2)}$$

$$8.9\frac{\text{g}}{\text{cm}^3} = \frac{\text{Mass Deposited (g)}}{\pi \cdot \text{r}^2 \cdot \text{Thickness (cm)}} \qquad \text{----------(3)}$$

$$\text{Thickness} = \frac{\text{Mass Deposited (g)}}{\pi \cdot \text{r}^2 \cdot 8.9} \text{ cm where r is the radius of the circular area of film}$$

Tantalum film deposited by sputtering was used as the barrier layer for the electroplating experiments. Tantalum was chosen because it has excellent step coverage properties and it is highly inert with other metals. The copper seed layer is also deposited by sputtering. This layer acts as a low resistance path for conduction. It also provides a nucleation layer for initiation of the plated copper film growth. In-situ deposition of copper seed layer on the barrier layer is very critical to obtain a strong (111) texture. If the barrier layer is exposed to air prior to Cu deposition, the resulting Cu texture is much

weaker than that without air break. This is likely attributed to oxidation of the barrier surface. It has been reported that Ta gives good adhesion compared to other barriers like Ti and TiN that reported peeling and poor adhesion between the barrier and copper. Also, Ta has a heteroepitaxial relationship with Cu as seen in figure 4.2. The Cu [220] direction on (111) planes is parallel to the Ta [330] direction on (002) planes that is a dominant texture plane of β- Ta. [32] It is believed that the heteroepitaxial growth of Cu improves the electromigration reliability of Cu interconnects; First, heteroepitaxial growth may reduce the number of interface defects that can act as void nucleation sites. It may also reduce the diffusion along the interface. Finally, it enhances the texture of Cu, which is known to improve the electromigration lifetime. [33]

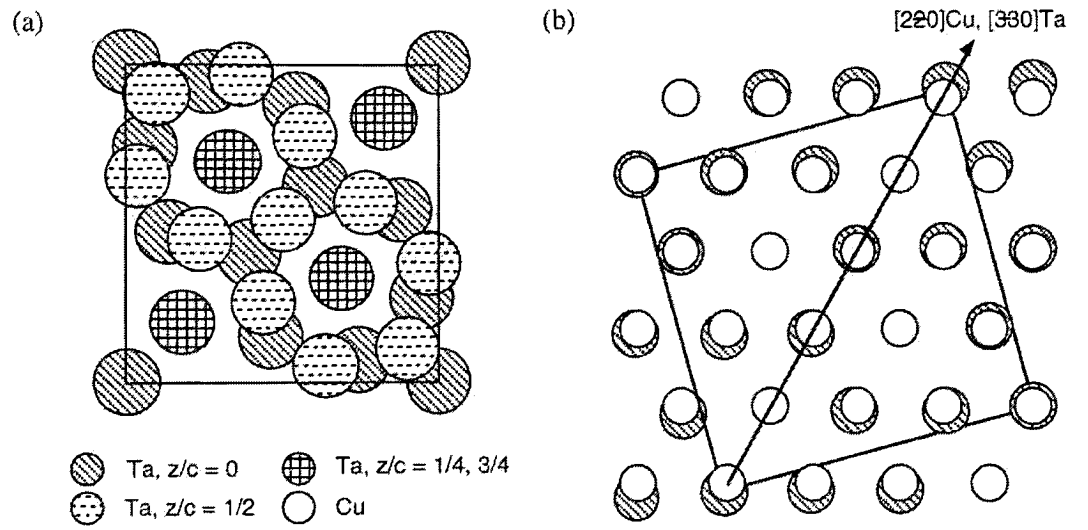


Figure 4.2: Schematic projection view of atoms (a) in a unit cell of tetragonal β-Ta and (b) monoatomic layers of Cu on Ta at the interface to illustrate atomic matching

The electrolyte used for plating is $CuSO_4$ solution. H_2SO_4 is added to the bath as a supporting electrolyte to increase the conductivity of the bath. The sulphuric acid

provides H^+ ions whose mobility is eight times that of the metal ions, which improves the conduction process.

4.2 EXPERIMENTAL PROCEDURE

A Reynolds Tech plating tool, which was newly installed at RIT was used for the electrolytic plating of copper. Figure 4.3 shows the layout of the tool. It is equipped with a bi-directional output power supply that allows for pulsed plating. The parameters – voltage, current, time, duty cycle are controlled manually via the plating control terminal.

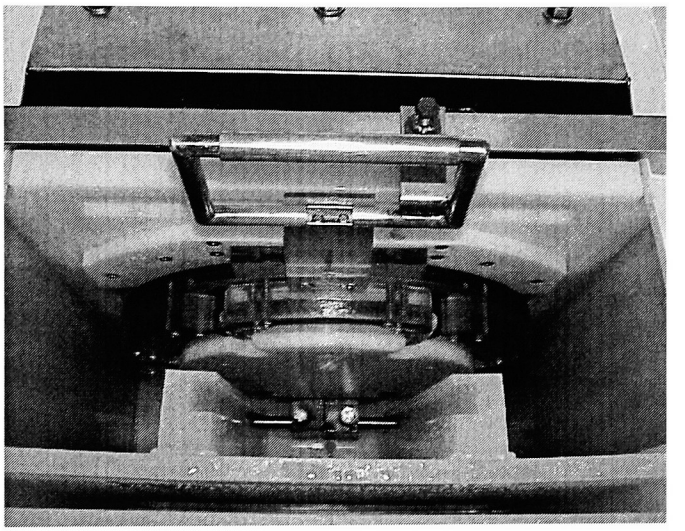


Figure 4.3: Electroplating tool set up

The volumes of chemicals that make up the bath are listed below:

$CuSO_4$ conc.: 10oz/gal – 38 liters

H_2SO_4 conc.: 25oz/gal 26 Liters

72 Liters of H_2O

136 Liters Total

Plating temperature: 26 °C

Wafers with a seed layer is placed in the substrate holder and immersed in the electrolytic solution that contains the cupric ions. Electrical contact is made to the seed layer, which becomes the cathode in the circuit and the reaction Cu^{2+} (aq) + $2e^{-}$ → Cu occurs on the wafer causing deposition of copper.

Plating was performed on several blanket SiO_2 wafers coated with adhesion and seed layer using varying current densities. To study the conformal filling of trenches, patterned silicon wafers were electroplated with copper. The following procedure was used to obtain the patterned wafers:

1. Oxide Growth:

10,000 Å of thermal oxide was grown on 4" bare Si wafers in a diffusion furnace (Model Horizontal Bruce Furnace). The recipe used in the furnace is given in table 4.1.

Move	**Time (min)**	**Temperature (deg)**
Push In	12	800
Stabilize	15	800
Ramp up	30	1100
O_2 Flood	4	1100
Soak	210	1100
N_2 Purge	5	1100
Ramp Down	55	25
Pull Out	15	25

Table 4.1: Recipe for deposition of 10,000 Å of oxide

2. Photolithography and etch of oxide:

A CMP test mask consisting of lines and spaces ranging from 1 μm to 30 μm was used for patterning the oxide. A g-line wafer exposure tool (GCA 6700 stepper) was

utilized to transfer pattern from the mask onto the wafer. Standard RIT photolithography steps were used to coat, expose and develop the photo resist.

The wafers were then dipped in buffered oxide etch (BOE) for 3 min to etch the oxide. The oxide was etched at the rate of 1000 Å per minute. This process trenched the oxide in areas where the substrate was exposed after development of photo resist. The wafers were ashed in an oxygen plasma asher to strip the photo resist from the unexposed areas.

4.2.1 DEPOSITION OF TANTALUM AND COPPER FILMS

The CVC 601 sputter tool was used for deposition of Ta barrier layer and Cu seed layer on blanket thermally grown SiO_2 wafers and patterned SiO_2 wafers. The system was pumped down to a base pressure of 5 x 10^{-6} Torr. 1000 Å of Ta was deposited at 900 W power, 4 mtorr pressure, and time of 8 min. 1000 Å of Cu was then deposited at 400 W power, 2 mtorr pressure for 8 min. The targets were pre-sputtered for 15 min prior to deposition of both the films to remove any impurities on the target.

Various currents and plating times were tested to obtain uniform film thickness. Theoretical mass of copper deposited was calculated by Faradays law and then compared against the actual mass values by measuring the mass of the wafer before and after plating. An actual thickness was determined by the alpha step profilometer at the edge of the wafer and compared against the theoretical values. A recipe to deposit two-micron thick copper film was standardized. Global profilometry of sheet resistance was done to estimate the non-uniformity in thickness. A four-point probe that maps sheet resistance at 49 locations across the wafer over a test area of diameter 75 mm was used for this purpose. The software calculates mean and standard deviation of the sheet resistance over that area. SEM pictures were taken to look at the surface morphology and cross sections of the films. Also, XRD analysis of the films before and after plating was done to study any preferred orientation.

4.3 RESULTS AND DISCUSSION

In the initial runs of experimentation for plating characterization, it was observed that during plating process, the voltage increases for constant current due to the dissolution of seed layer. This phenomenon is called as *"bipolar behavior"*. When this occurs the electronic resistance of the seed layer is less than the electrochemical resistance thus causing under plating of wafer and de-plating of the copper seed layer as seen in figure 4.4, giving lesser thickness than that expected from the theoretical values and creating a bulls-eye effect to the center of the wafer. This was due in part to the electrolytic solution seeping behind the wafer and disrupting the plating process. A single O-ring was placed behind the wafer to create seal between the stainless steel holder and copper seed electrical connection of the wafer. This fix steadied the voltage and increased plating thickness bringing the actual thickness values closer to the theoretical values.

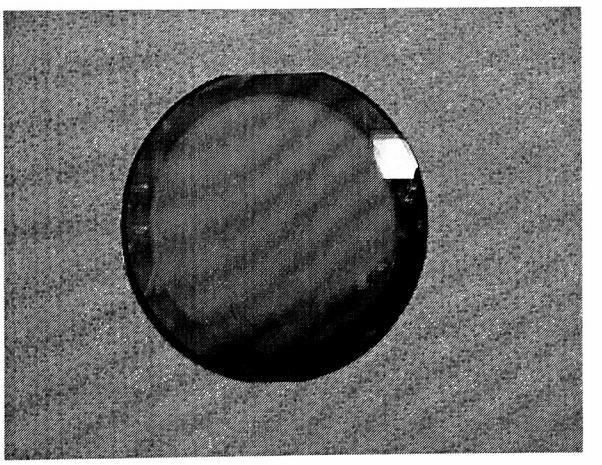


Figure 4.4: De-plating of copper seed layer

The recipe shown in table 4.2 gives an ~ 2 μm thick electroplated copper film. In the initial stage of plating process, a low current and voltage is used so as to not pass very high currents through the thin copper seed layer.

	Current (amp)	Voltage (V)	Time (min)
Stage 1	0.2	2.5	5
Stage 2	1.0	7.5	15

Table 4.2: Recipe for 2 μm thick copper electroplating

Based on the sheet resistance of the plated film and its thickness, the resistivity was calculated to be 1.78 μΩ cm, which is close to the actual resistivity for bulk copper that is 1.67 μΩ cm.

The patterned wafers were successfully filled with copper. Figure 4.5 shows the optical image of 5 um lines that were resolved prior to copper plating. This was also seen in the uniform change in step height by the profilometer. A top down SEM image of the seed layer at 20,000X magnification is shown in figure 4.6. Electrolytic plating filled these lines conformally giving a uniform film of copper. Figure 4.7 is an SEM image of the electroplated copper at a magnification of 40,000 X. Figure 4.8 is the cross sectional SEM of the wafer after deposition of copper, showing a smooth interface between the films. The visual inspection of the wafer shows a good film of electroplated Cu. When the wafers were cleaved for cross sectional SEM analysis, the layers did not peel, showing good adhesion of the films to each other and the effectiveness of the barrier and seed layer.

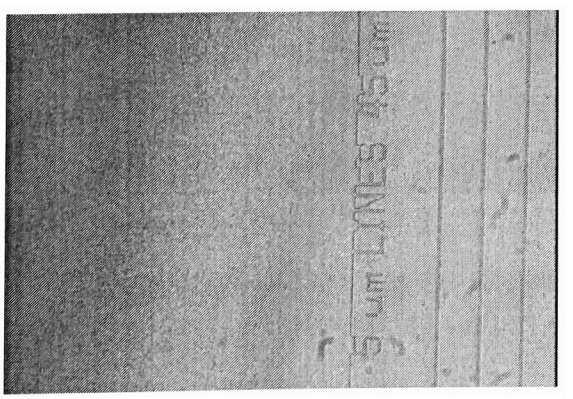


Figure 4.5: 5 um lines observed in the optical microscope

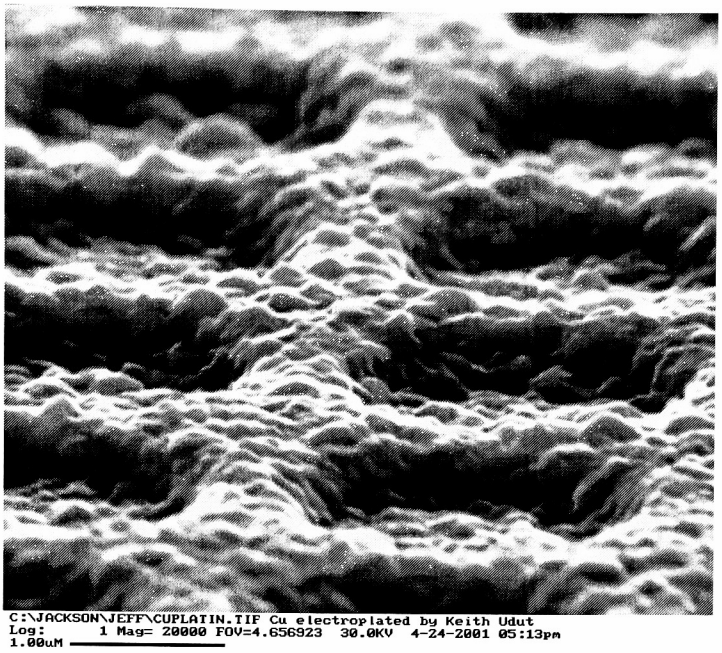


Figure 4.6: SEM image of Copper seed layer at 20,000X

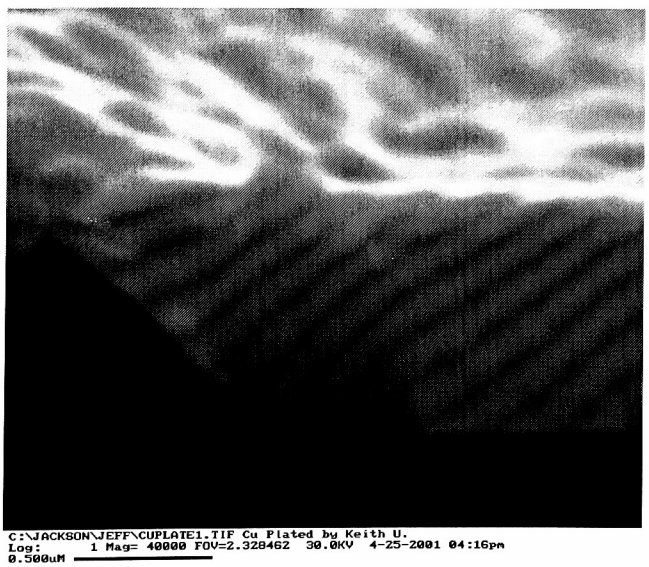


Figure 4.7: SEM picture of surface of electroplated copper at 40,000X magnification

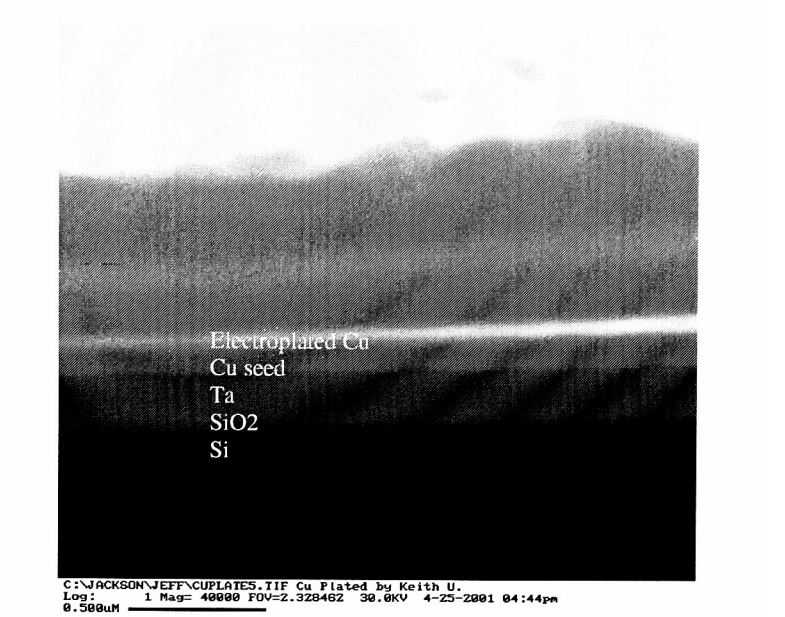


Figure 4.8: SEM image of cross section showing Electroplated Cu, Cu seed, Ta, SiO_2 and Si

Figure 4.9 is the global profilometry map of a wafer plated with current of 1 amp showing uniform sheet resistance across the wafer. However, at very high current densities, there is a higher deposition at the edge of the wafer than the center because of the configuration of the electroplating tool, causing an increase in the thickness of plating. The sheet resistance contour lines of a wafer plated at 5 amps were observed to be dense at the edge as seen in figure 4.10. When a low current is used, there are less current density effects yielding a uniform plating thickness across the wafer.

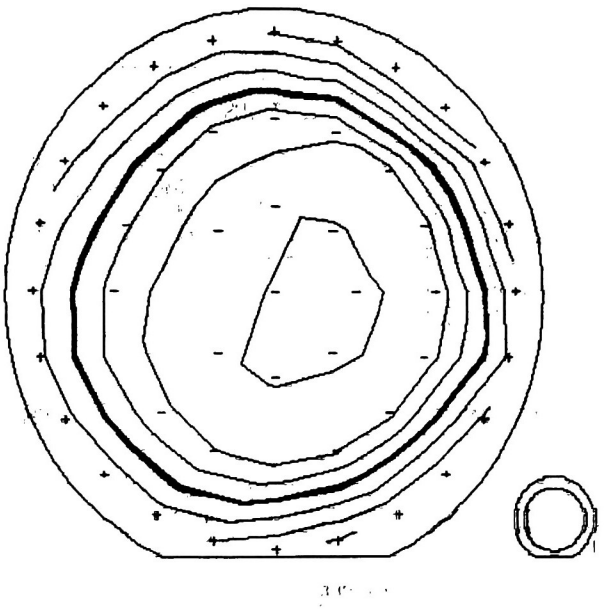


Figure 4.9: Sheet resistance contour plot of a uniformly plated wafer

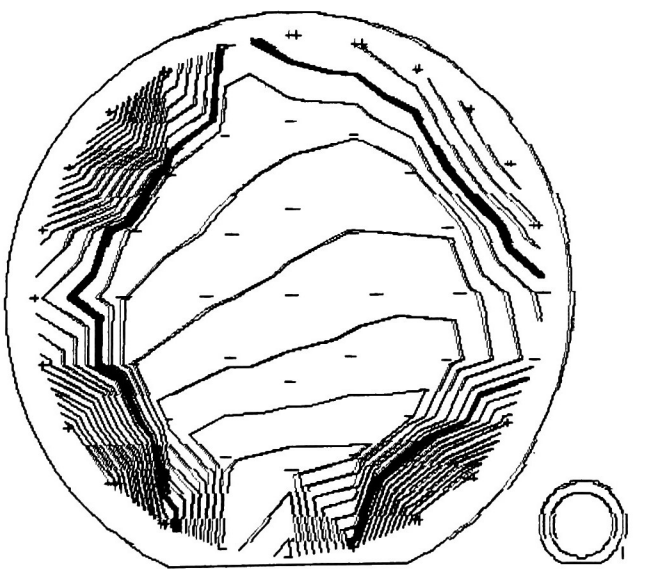


Figure 4.10: Sheet resistance contour plot showing non-uniform plating

Figure 4.11 is the plot of sheet resistance as a function of the theoretical deposited weight for various amp-min that shows that as the deposited weight of copper plating increases, the sheet resistance decreases. This means that the electroplating was proceeding according to Faraday's law and confirmed that the electroplating set up was working as expected.

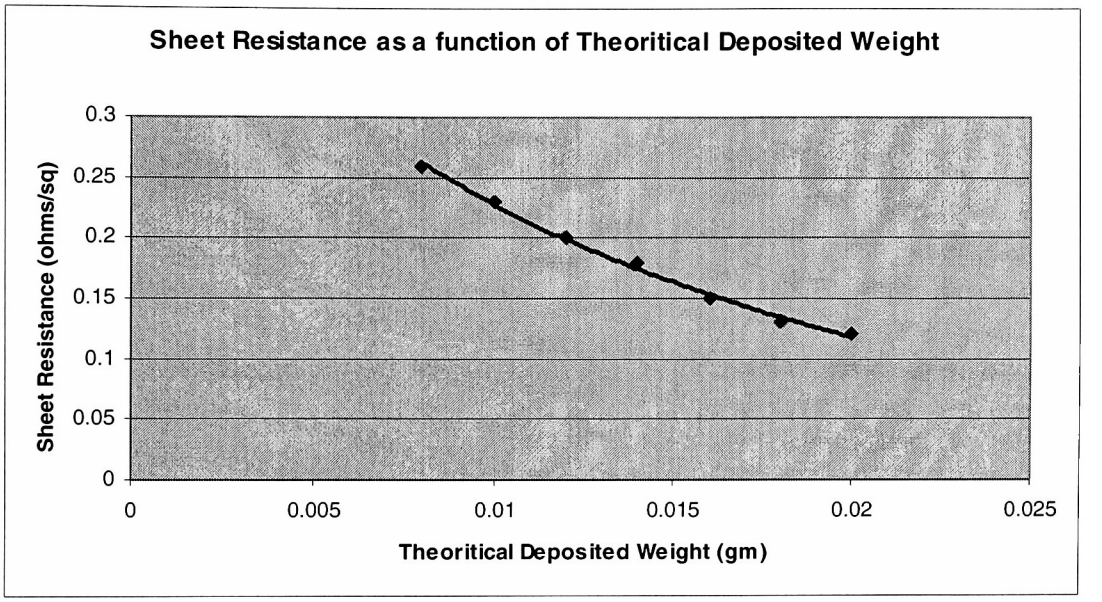


Figure 4.11: Plot of sheet resistance Vs theoretical weight deposited

The XRD of the wafers before and after plating is shown in figures 4.12 and 4.13 respectively. It is observed that the plated Cu films show a preferred (111) orientation. The microstructure of electroplated Cu is highly dependent on the Cu seed layer and the barrier layer. It has been reported that strong interrelationships exist between the Cu seed texture and the grain size and texture of electroplated copper. If the seed layer has a strong (111) texture, the electroplated Cu film also has a strong (111) texture.[31] A strongly textured seed layer also has a smoother surface. This is because randomly oriented grains tend to produce a rough surface due to non-uniform growth rate and growth direction.

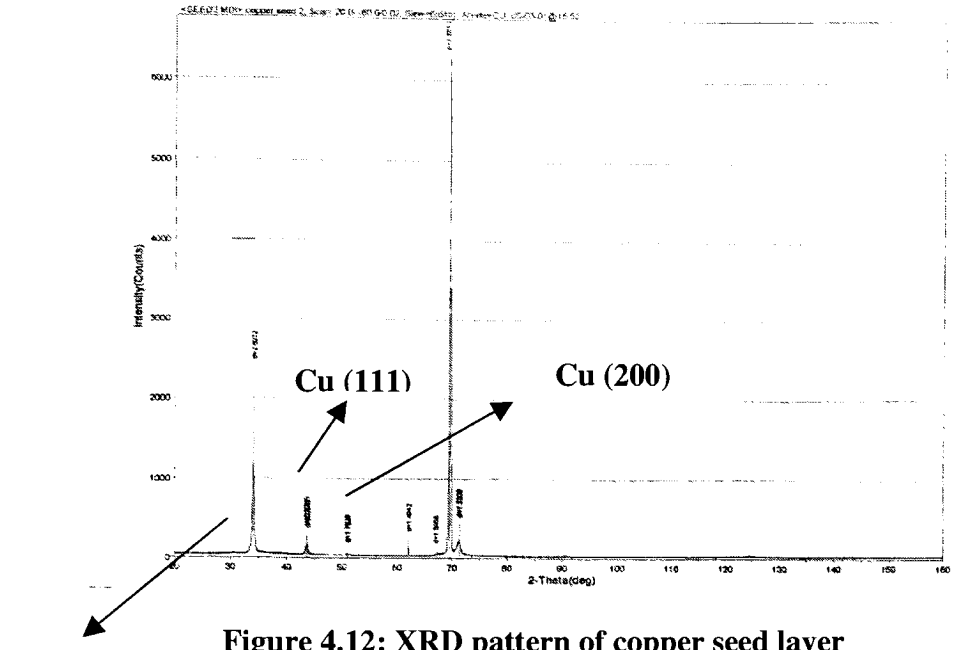


Figure 4.12: XRD pattern of copper seed layer

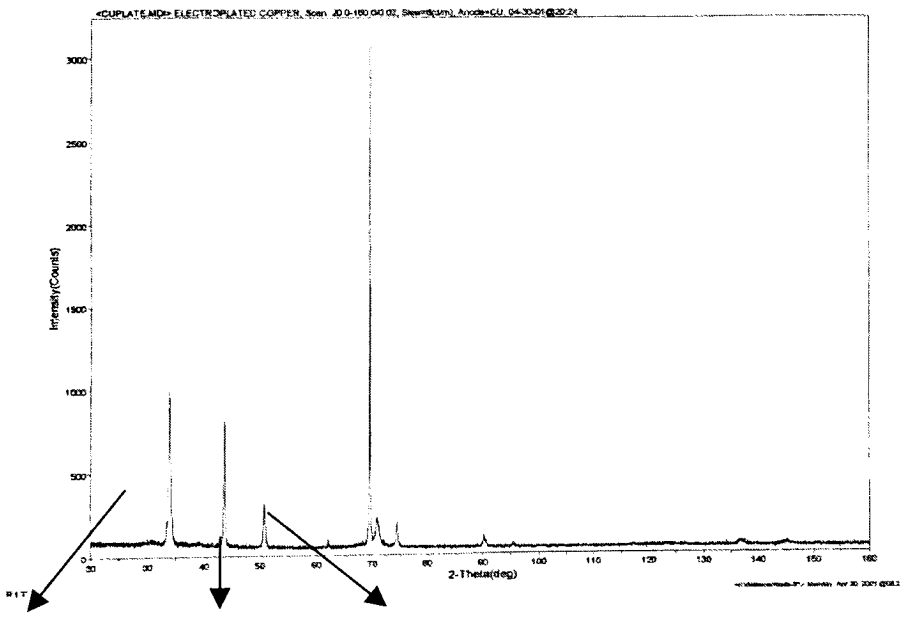


Figure 4.13: XRD pattern of electroplated copper

4.4 CONCLUSION

The electroplating tool was set up and the process was characterized for plating 2um thick copper. Bringing copper electroplating to the Rochester Institute of Technology speaks volumes and has far reaching potentials for new patents, innovative research, thin film labs, chemical mechanical polishing and replacing the aluminum metal layer with copper for the advanced 1.0μm and 0.5μm CMOS process currently used in the R.I.T. integrated circuit processing student run factory.

An electroplating process must address a variety of other issues. Because of concerns of copper contamination, it is critical that no copper be deposited on the backside of the wafer. One greatest challenge that is out of the electroplater's control is the quality of the seed layer. If the seed layer is not perfect (i.e., not continuous), it can create a void in the copper fill. Further studies in copper processing need to be done to optimize the plating process for further applications like CMP and dual damascene processing.

5. CONCLUSIONS

The phases of Ta-N system have been investigated by sputter deposition of Ta-N films by varying the nitrogen flow during sputtering. It has been observed that as-deposited pure Ta is tetragonal, which becomes bcc-Ta with small increase in N_2 flow to 5% of the sputtering gas mixture. When the nitrogen flow is increased to 12- 20%, amorphous and a mixture of amorphous and crystalline Ta_2N phase is formed. The amorphous phase crystallizes when annealed to higher temperatures. fcc- TaN phase is formed at N_2 flow of 30%. At higher concentrations of N_2, nitrogen rich compounds like Ta_5N_6, Ta_3N_5 are formed. The process parameters for deposition were optimized to obtain low resistive films by using a design of experiment methodology. Use of a low pressure, high power and bias of substrate are necessary to obtain low resistive films. However the tantalum nitride films obtained have a slightly higher resistivity than the actual values. This is due to oxygen pick up from the chamber. Use of ultra high vacuum of $10^{-8} - 10^{-9}$ torr will enable that there is no oxygen or impurity atoms in the films. However, the vacuum reached in the present study was only 10^{-6} torr, and also there was no load lock to the chamber causing exposure of wafers to atmosphere during loading.

Copper films were sputter deposited on thermally grown SiO_2 wafers after deposition of the nitride barrier layer. It is very important to deposit copper without breaking the vacuum after deposition of the nitride because exposing the barrier layer to atmosphere before depositing copper causes formation of an oxide layer on TaN that increases the resistivity of the film and also causes adhesion problems with copper. The films obtained had a smooth interface with the barrier, thus showing good adhesion. During back-end processing, the diffusion barrier and the interconnect materials, TaN and Cu, are subjected to various annealing treatments in different ambients at relatively high temperatures. The effect of annealing ambient on the integrity of the metallization was studied using sheet resistance measurements, XRD, RBS, XTEM and SEM techniques. It has been observed that annealing the films to temperatures above 500 ^{o}C cause delamination of films at the Cu/TaN interface, which is attributed to the formation of copper oxides with a high density of voids. The films annealed in a N_2 ambient have higher resistivity than those in an inert Ar atmosphere, because of the presence of some

oxygen in N_2. Therefore, it is very important to isolate the Cu/TaN metallization from oxygen exposure during backend processing. To prevent oxidation of copper and diffusion of copper between metal layers a Si_3N_4 cap may be used. It also acts as an etch stop during dual damascene process. However, this was beyond the scope of the present study. Diffusion of tantalum into the surface of copper was observed in the films at temperatures ~ 500 to 600 °C. Therefore we can conclude that cubic TaN films act as stable barrier films upto 500 °C in an inert ambient.

The electroplating tool was set up and the process was characterized for plating 2um thick copper. Bringing copper electroplating, along with the study of diffusion barrier materials for developing the copper interconnect technology has far reaching potentials for further research, thin film labs, chemical mechanical polishing and replacing the aluminum metal layer with copper for the advanced 1.0μm and 0.5μm CMOS process currently used in the Rochester Institute of Technology integrated circuit processing student run factory.

REFERENCES

1. J. R. Black, Proceedings of 6th annual International Reliability Physics Symposium, page 148. IEEE, 1967.
2. S.P. Murarka, Materials Science and Engineering, R19, Nos 3-4, May 1997.
3. S.P. Murarka and J.Gutmann, Thin Solid Films, 236 (1993), 257 -266
4. http://chip.ibm.com/news/cmos7s.htm
5. M.T. Wang et.al, Thin Solid Films, 307, 79 – 88, 1997.
6. Karen Holloway et.al, J. Appl. Phys. 71, 1 June 1992
7. M.Ohring, The Materials Science of Thin Films.
8. http://www.esm.psu.edu/HTMLs/Graduate/qian/Lit.html
9. B.Chin et.al, Solid State Technology, 141-44, July 1998
10. P.Singer, Semiconductor International, p 79-81, August 1997
11. P.Singer, Semiconductor International, p 90-96, June 1998
12. http://www.semiconductor.net/semiconductor/issues/Issues/1998/jun98/docs/feature3.asp
13. A.T. Norman et.al, *Proc. 8th VLSI Multilevel Interconnection Conf.*, IEEE, New York, 1991, p.123
14. H.gong et.al, Journal of Electrochemical Society, 147 (6) 2312-2318 (2000)
15. V.W. Lindberg et.al Surface and Coatings Technology, 133-134 (2000) 484-488
16. John P. Mckelvey, Solid State Physics, Kreiger Publishing Company, Malabar, Florida, (1993), PP. 45-51.
17. K.Min et.al J. Vac. Sci. Technol. B 14(5), Sep/Oct 1996
18. M.Wittmer et.al J. Vac. Sci. Technol. A, Vol.3, No.4, Jul/Aug 1985
19. M.Stavrev et.al Thin Solid Films, Vol 307 (1997) 79-88
20. M. Takeyama et.al J. Vac. Sci. Technol. B 14(2), Mar/Apr 1996
21. M. Eizenberg, MRS Bull. Nov. 1995
22. http://www.tmworld.com/articles/05_1999_TEM_Performance.html
23. PDF #4-836
24. PDF #26-0985

25. PDF #77-199
26. PDF #48-1548
27. PDF #49-1283
28. X.Sun, J.S. Reid et.al Thin Solid Films, 236, pg 347 (1993)
29. P.Catania, R.A. Roy and J.J. Cuomo, J. Appl. Phys. 74, 1008 (1993)
30. Donald L. Smith. Thin film Deposition – Principles and Practice (McGraw Hill 1995)
31. http://marco.stanford.edu/swong/publications/paper28.pdf
32. K.W.Kwon et.al Appl. Phys. Lett. 71(21), 3069-3071 (1997)
33. C.Ryu et.al, IEEE/IRPS. Proc.,p.201, (1997)
34. PDF #25-1279
35. Binary phase diagrams
36. J.Li, J.W.Mayer and E.G. Colgan, J. Appl. Phys., 70, 2820 (1991)