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Stability analysis of switched dc-dc boost converters for integrated circuits

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Stability Analysis of Switched DC-DC Boost Converters for Integrated Circuits

by

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Abstract

Boost converters are very important circuits for modern devices, especially battery-operated integrated circuits. This type of converter allows for small voltages, such as those provided by a battery, to be converted into larger voltage more suitable for driving integrated circuits.

Two regions of operation are explored known as Continuous Conduction Mode and Discontinuous Conduction Mode. Each region is analyzed in terms of DC and small-signal performance. Control issues with each are compared and various error amplifier architectures explored. A method to optimize these amplifier architectures is also explored by means of Genetic Algorithms and Particle Swarm Optimization.

Finally, stability measurement techniques for boost converters are explored and compared in order to gauge the viability of each method. The Middlebrook Method for measuring stability and cross-correlation are explored here.

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List of Notations

ΔV_O	Output Ripple Voltage
η	Efficiency
ω_0	Resonant Frequency in radians per second
ϕ_M	Phase Margin
τ_L	Unitless Time Constant Equivalent to $\frac{LF_S}{R}$
ζ	Damping Coefficient
C_D	Capacitance of Schottky Diode
C_{OSS}	Capacitance of MOS Switch
C_{SW}	Total Capacitance of Switching Elements
D or $\hat{d}$	Duty Cycle
F_S	Switching Frequency
g_m	Transconductance of an Operational Transconductance Amplifier (OTA)
G_{d0}	Low Frequency Converter Gain
I_D	Diode Current
I_L or $\hat{i_L}$	Inductor Current
I_O	Output Current

M	Converter DC Gain
P_{SW}	Power Absorbed by All Switching Elements
Q	Quality Factor of Filter
R	Load Resistance
r_C	Capacitor Series Resistance
r_L	Inductor Series Resistance
r_{SW}	Parasitic Switching Resistance
T_S	Switching Period
V_c	Control Voltage (or Error Voltage)
V_O or $\hat{v_o}$	Output Voltage
V_S	Input Voltage
BIST	Built-In Self-Test
CCM	Continuous Conduction Mode
CMC	Current Mode Control
DCM	Discontinuous Conduction Mode
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistor
FPGA	Field-Programmable Gate-Array
FRA	Frequency Response Analyzer
GA	Genetic Algorithm
KCL	Kirchoff's Current Law
KVL	Kirchoff's Voltage Law

LTI	Linear Time-Invariant
NPFF	Normalized Parabolic Fitness Function
OTA	Operational Transconductance Amplifier
PID	Proportional-Integral-Derivative
PRBS	Psuedo-Random Binary Sequence
PSO	Particle Swarm Optimization
PWM	Pulse-Width Modulation
QBGA	Queen-Bee Genetic Algorithm
RHP	Right-Hand-Side of Imaginary Plane
SMU	Source Measurement Unit
SSA	State Space Averaging
VMC	Voltage Mode Control

Chapter 1

Introduction

Modern mobile integrated circuits contain many different sub-circuits with varying degrees of power requirements [1]. Likewise, these circuit are typically designed to be high-performance and thus require fast and stable power supplies in order to guarantee proper operation [2]. Because of these requirements, Switched DC-DC Boost Converters have become commonplace in such integrated circuits due to their ability to 'boost' the small voltage of a battery coupled with their high efficiency [3–6].

In order to guarantee the commercial viability of a Boost Converter, the circuit itself must be well understood. This includes understanding the impact of non-ideal components on the DC and transient responses of the system, as well as understanding the regions that a converter may operate in. Understanding these effects helps to illustrate different regions that may cause instability in a DC-DC Boost Converter and, thus, gives important information to the designer as to what type of component tolerances and values are acceptable.

1.1 Importance of Stability

For low-performance circuits, converter stability may not be as important as other design criteria such as output voltage range or output power dissipation capabilities; however, for mobile integrated circuits, especially those used for display purposes, stability is a very important factor [7].

Maintaining a highly stable power supply for a display, such as an LCD, helps

to guarantee that pixel brightness exhibits little variation from the expected ideal value. This is a very important design consideration since the human eye perceives brightness on a non-linear scale, known as luminance. This means that there exist levels at which the change in voltage or current is very slight, yet the change in luminance is large. As such, it is important for a mobile-integrated-display-circuit power-supply to be very stable as any ringing could cause perceivable changes in pixel brightness which lowers the quality of the product [8].

An unfortunate reality for integrated display-circuits is that they typically have to function properly for a multitude of different display backplanes which, in turn, alters the load requirements for the circuit power supply [9]. In addition, these displays can have vastly different numbers of pixels which, yet again, alters the load requirements for the supply. In every one of these conditions, the need for stability (due to the luminance concerns addressed earlier) is of the utmost importance. Thus, the ability to accurately measure stability as well as understanding what areas of the converter are likely to cause *in*stability is paramount to ensuring a commercially viable product.

1.2 Thesis Organization

To begin the discussion of Boost Converter Stability, the DC performance is analyzed and discussed in Chapter 2. Two different Boost Converter operating modes are explored, known as Continuous-Conduction Mode (CCM), and Discontinuous-Conduction Mode. Each mode of operation is explored in terms of voltage conversion ratios, duty-cycle requirements, efficiency and output ripple. These results are then compared to determine the trade-offs of operation in either region. The efficiency of the converter is analyzed in terms of sensitivity to two primary sources of non-ideal power-loss in order to develop an understanding of their effects on DC performance.

Chapter 3 covers the small-signal analysis of a Boost Converter in order to develop accurate models that help to form an understanding of what conditions typically cause instability. Again, both the CCM and DCM converters are explored. First, a small-signal modeling technique known as State-Space Averaging is explored wherein the Boost Converter is averaged and linearized around a given operating point [14]. As a comparison, a technique known as Averaged PWM Modeling is performed which

produces similar results with less overall work [18, 19]. The transfer functions for both Boost Converters with ideal components and Boost Converters with non-ideal components are then compared via Bode plots and transient step responses. An approximation is presented wherein an non-ideal Boost Converter operating in DCM can be approximated to that of an ideal Boost Converter operating in DCM, which enables the simplification of various small-signal parameters.

Chapter 4 analyzes various error-amplifier control architectures for integrated circuits. These circuits utilize Operational Transconductance Amplifiers (OTAs) due to high speed and low layout area cost. Various control schemes are analyzed and compared via frequency response characteristics. Controller selection recommendations are made based on converter requirements. Appendix A also explores error-amplifier controller design via sophisticated high-dimensional optimization algorithms, specifically that of Genetic Algorithms and Particle Swarm Optimization Algorithms.

Chapter 5 deals with the full Boost Converter circuit from power conversion stage all the way through the control stage. Here, various design methods are presented based on converter region of operation (CCM or DCM) and the issues associated with ensuring a stable converter explored. The different architectures are compared via Bode plots and transient step response plots in order to better visualize the important differences. The converters are also analyzed via the complex plane in order to better visualize pole-zero placement and the effects on converter stability.

Chapter 6 introduces various Switched DC-DC Converter stability measurement techniques. These include ubiquitous step response plots as well as Bode plots. Another measurement technique explored utilizes the cross-correlation of input noise and the output waveform in order to extract a Bode plot mathematically. These stability test methods are explored and potential test implementations are presented. Recommendations are made based on the benefits of each test setup.

Chapter 2

Boost Converter DC Characteristics

A boost converter (shown in Figure 2.1) has two primary modes of operation: Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). As these names would indicate, they are defined by whether or not the converter is continuously or discontinuously conducting; specifically, whether or not the inductor current saturates or drops to zero within one switching period. This is explained graphically in Figure 2.2. In this chapter, the DC equations for voltage transfer function, output ripple voltage, and efficiency will be derived for both CCM and DCM. These equations will be compared in order to better determine the benefits of using either conduction method.

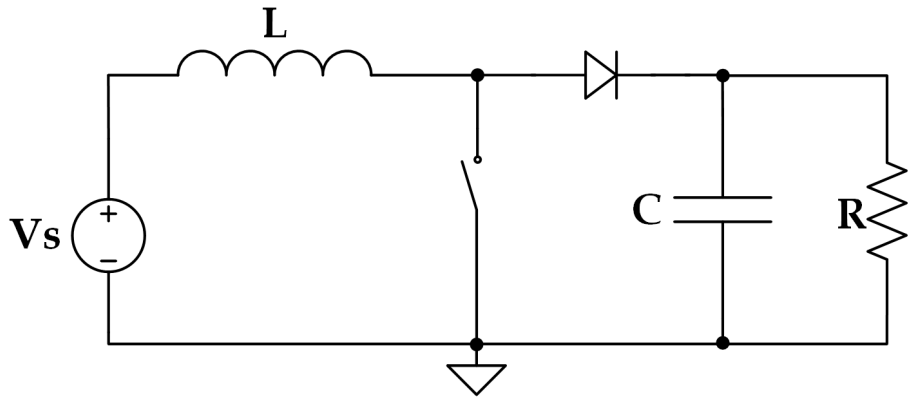

Figure 2.1: Ideal Boost Converter Circuit

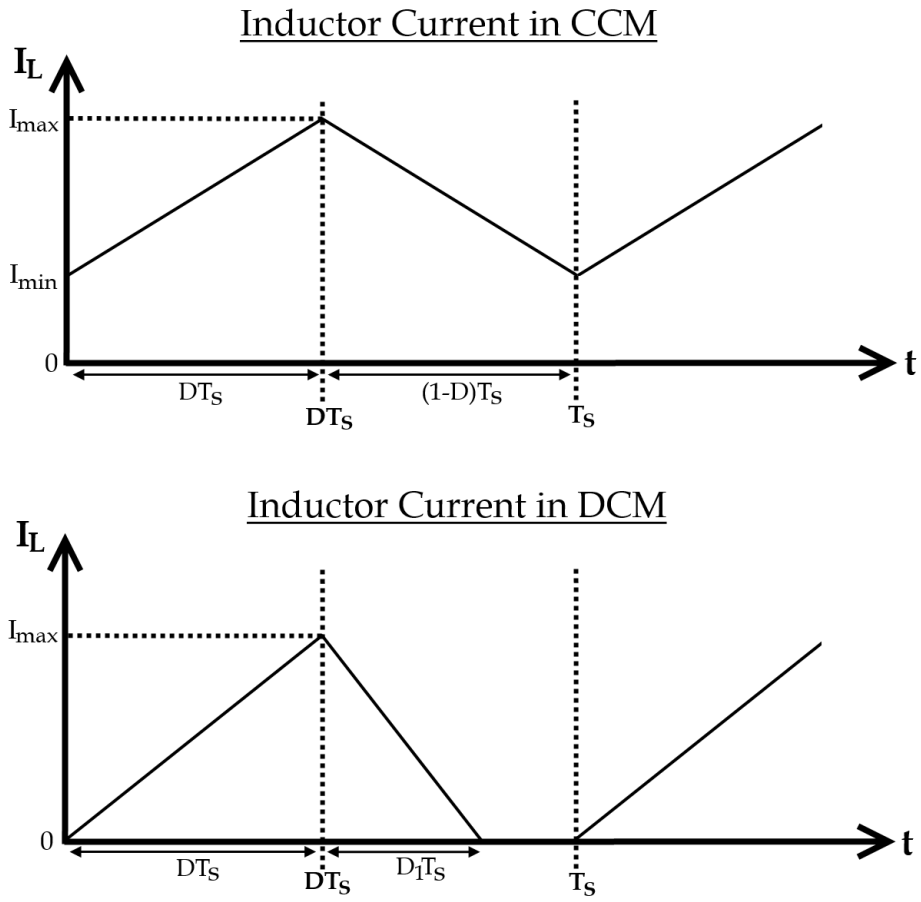

Figure 2.2: Inductor Current in Boost Converter for CCM and DCM

2.1 Continuous Conduction Mode (CCM)

In order to begin analysis, it is important to observe the converter behavior without any added parasitics (switch resistance, inductor resistance, diode forward voltage drop, *et cetera*). Thus, Figure 2.1 will be used for the ideal derivations.

2.1.1 Ideal Converter

During steady-state operation when the switch is closed, the voltage across the capacitor causes the diode to become reverse-biased since the anode will be grounded. Thus, the voltage across the inductor, V_L is equal to the source voltage, V_S. Since the voltage across an inductor is equal to $L\frac{di_L}{dt}$ and the inductor current is approximately

constant (in that it is increasing linearly), it can be said that (taking $dt = DT_S$):

$$\Delta i_{L,closed} = \frac{V_S D}{L F_S} \tag{2.1}$$

Next, it is necessary to open the switch. Since current through an inductor cannot change instantaneously and the diode is the only device which can provide a conduction path for the inductor current, the diode *must* become forward-biased. As such, the voltage across the inductor becomes $V_S - V_O$. Since the switch is open, and referring to the inductor current graph for CCM shown in Figure 2.2, $dt = (1-D)T_S$. Rearranging the equation for voltage in an inductor yields:

$$\Delta i_{L,open} = \frac{(V_S - V_O)(1 - D)}{L F_S} \tag{2.2}$$

In steady-state, the total change in inductor current must equal zero, thus by using (2.1) and (2.2):

$$\begin{aligned} 0 &= \Delta i_{L,closed} + \Delta i_{L,open} \\ 0 &= \frac{V_S D}{L F_S} + \frac{(V_S - V_O)(1 - D)}{L F_S} \\ 0 &= V_S D + V_S(1 - D) - V_O(1 - D) \end{aligned}$$

Rearranging the above equation to solve for the DC output-to-input transfer function yields:

$$\frac{V_O}{V_S} = \frac{1}{1 - D} \tag{2.3}$$

Output Ripple

To solve for the output ripple voltage, it is important to consider how the charge is changing within the output filter capacitance. Consider the period for which the switch is closed, that is during the interval DT_S. Since the diode is reverse biased, the capacitor discharges in order to provide current to the load resistance. Thus, since the voltage at the output is positive and maintaining the convention that current

flows *into* positive nodes,

$$I_C = -I_R = -I_O$$

Thus, for this interval the change in capacitor charge is given by the product of the current and the interval, or:

$$\Delta Q = -I_O DT = -\frac{I_O D}{F_S}$$

Because the charge in a capacitor is equal to the product of both the voltage and the capacitance, it can be said that:

$$\Delta Q = \Delta V C$$
$$\Delta V = \frac{\Delta Q}{C}$$

which yields the output ripple voltage equation of:

$$\Delta V_O = \frac{D I_O}{C F_S} \tag{2.4}$$

Efficiency

To find efficiency, a simple relation between input and output power can be established. Since there are no loss mechanisms in the circuit using the ideal diode model, all power delivered by the source will be absorbed in the load. Therefore the efficiency will be 100% for an ideal boost converter.

2.1.2 Non-Ideal Converter

Figure 2.3 shows the boost converter circuit with parasitics added in.

In order to derive the output voltage of the non-ideal boost converter in CCM, the concept of energy-conservation [10] is used wherein:

$$P_S = P_O + P_{Loss}$$

Thus it is necessary to observe what mechanisms will cause power loss in the non-ideal

model. Unfortunately, Figure 2.3 doesn't provide a completely accurate picture as to what will cause power loss as it ignores the dynamic switching losses in both the transistor switch and the diode. Since both the switch and diode have parasitic capacitances associated with them, during each switching cycle they need to be charged and discharged. Doing so provides a momentary short to ground and there will be non-negligible power loss as a result, given by (2.5).

$$P_{C_{SW}} = \frac{1}{2} C_{SW} V_{sw}^2 F_S \tag{2.5}$$

In the worst-case situation, the voltage across the switch, V_{sw}, will be equal to the output voltage plus at least the forward voltage drop of the diode, or $V_O + V_D$. The parameter C_{SW} is device-specific but typically has a range between $10\,pF$ to $200\,pF$ (commonly shown as C_{OSS} on datasheets). Figure 2.4 shows a plot for the normalized power consumption of all parasitic components.

There is one noticeable characteristic of Figure 2.4: operation in DCM is far more dependent on the dynamic switching loss than operation in CCM. The explanation is rather simple: in CCM, the current through the inductor never goes to zero, thus during the period in which the switch is open there is a continuous amount of power loss through the inductor and diode which ends up contributing to far more loss than the switching elements. In DCM, however, there is a period in which no current flows (Figure 2.2) and thus the power losses through the inductor and diode are much smaller in value. Because of this, the loss due to the switch capacitance becomes far more noticeable. Note that during the portion of the time there is no current flow in

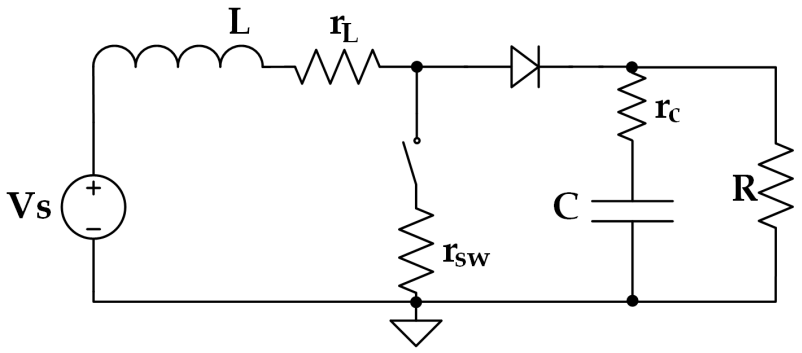

Figure 2.3: Non-Ideal Boost Converter Circuit

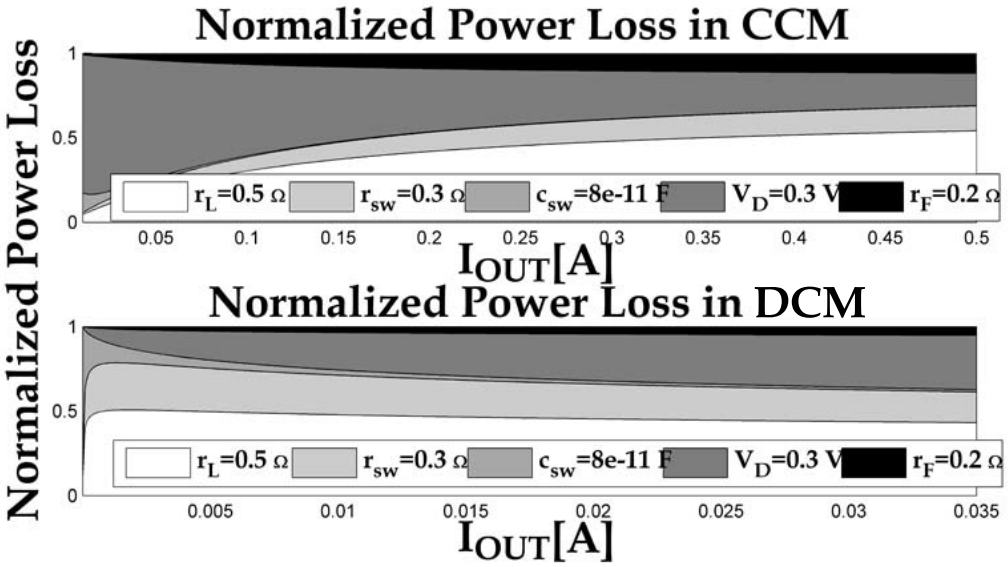

Figure 2.4: Normalized Power Loss in CCM and DCM

the DCM operating mode, the switch capacitance will charge to V_S. This is because the diode must stop conducting which means there is no path for current from the input source, V_S, so the node on the positive side of the diode will charge to V_S. Over time, the total voltage change at the switch will be approximately equal to V_O rather than V_S and this will cause a discontinuity at the CCM/DCM boundary for efficiency calculations [11].

Now, consider the silicon diode as it begins to switch from reverse-biased to forward-biased. Here, the depletion region begins to decrease in width which, in turn, increases the depletion capacitance. However, there is also an increase in diffusion capacitance due to the minority charge located near the junction [12]. This diffusion capacitance will contribute to dynamic switching losses similar to that of the transistor. As a result, silicon diodes are commonly replaced by Schottky diodes in switched power systems because Schottky diodes do not store minority charge and, hence, do not exhibit diffusion capacitance [12]. The only capacitance they will have is due to the depletion region and will be quite small in comparison to the capacitance of a silicon diode, for example. This is an added benefit of using Schottky diodes in switched DC-DC converter circuits as increasing that capacitance causes a corresponding linear increase in power consumption as evidenced by plugging (2.6)

into (2.5).

$$C_{SW} = C_{OSS} + C_D \tag{2.6}$$

Assuming that the diode ON-resistance is small and that the forward voltage drop will be the primary source of static loss in the diode (which is valid except for large load currents in CCM operation), the total power loss can be given as,

$$P_{Loss} = P_{r_L} + P_{SW} + P_D$$

where P_{SW} is equal to both the conduction loss due to the switch, $P_{r_{SW}}$, as well as the dynamic switching losses, $P_{C_{SW}}$ and P_D is equal to the conduction loss due to the diode.

Since the current through the inductor is always I_L by definition, the power absorbed by the inductor's series resistance is simply $r_L I_L^2$. Since the switch resistance will only absorb power when the switch is on, that is during time interval DT, and the current through it will be equivalent to I_L, it's clear that the static power absorbed by the switch will be $Dr_{SW}I_L^2$ whereas the dynamic power consumption is $\frac{1}{2}C_{SW}V_O^2F_S$. Likewise, since the diode is only conducting for the time interval of $(1-D)T_S$, the average power absorbed by the diode is just $(1-D)V_D I_L$. This yields the equation:

$$P_{Loss} = r_L I_L^2 + Dr_{SW}I_L^2 + \frac{1}{2}C_{SW}V_O^2F_S + (1-D)V_D I_L \tag{2.7}$$

Since,

$$P_S = P_O + P_{r_L} + P_{SW} + P_D$$

$$\therefore V_S I_S = V_O I_O + r_L I_L^2 + Dr_{SW}I_L^2 + \frac{1}{2}C_{SW}V_O^2F_S + (1-D)V_D I_L \tag{2.8}$$

Since current through the diode is equal to $(1-D)I_L$, and all of the DC component of the diode current must be delivered to the load, the following relationship can be established and then solved for I_L:

$$(1-D)I_L = I_O$$

$$I_L = \frac{I_O}{(1-D)} \tag{2.9}$$

Dividing (2.8) through by I_L and plugging (2.9) into I_L yields:

$$V_S = (1-D)V_O + r_L\frac{I_O}{1-D} + Dr_{SW}\frac{I_O}{1-D} + \frac{1-D}{I_O}C_{SW}V_O^2F_S + (1-D)V_D$$

Plugging $\frac{V_O}{R}$ in for I_O and solving for V_O then results in the following expression for output voltage of a Boost Converter in CCM with parasitics:

$$V_O\left[(1-D) + \frac{r_L}{R}\frac{1}{1-D} + \frac{R(1-D)}{2}C_{SW}F_S + \frac{D}{1-D}\frac{r_{SW}}{R}\right] = V_S - (1-D)V_D$$

$$V_O = \frac{V_SR(1-D) - V_DR(1-D)^2}{R(1-D)^2 + r_L + Dr_{SW} + \frac{1}{2}(1-D)^2R^2C_{SW}F_S} \tag{2.10}$$

To check this answer, simply set all of the parasitics equal to zero and it's clear that (2.10) will yield the ideal expression shown in (2.3).

Output Ripple

The ripple voltage at the output due to the capacitor is the same in the non-ideal case as it is in the ideal case which is given in (2.4). However, there is an additional ripple voltage caused by the capacitor's series resistance. When the capacitor is charging, the current will be decreasing at the same rate as the changing inductor current, Δi_L, thus the largest peak current is $I_{L,max}$ which can be expressed as a sum of the average inductor current (2.9) and $\frac{\Delta i_L}{2}$.

First, an expression for Δi_L needs to be derived for the non-ideal converter. The process is similar to that of the ideal case wherein the voltage across the inductor is found and then solved for Δi_L. Referring to Figure 2.3, when the switch is closed it's clear that:

$$V_L = V_S - \Delta i_L(r_L + r_{SW})$$
$$L\frac{\Delta i_L}{DT_S} = V_S - \Delta i_L(r_L + r_{SW})$$

Rearranging and solving for Δi_L yields (2.11).

$$\Delta i_L = \frac{DV_S}{LF_S + D(r_L + r_{SW})} \tag{2.11}$$

Since I_L is given in (2.9), $I_{L,max}$ can be found as per (2.12).

$$I_{L,max} = I_L + \frac{\Delta i_L}{2}$$

$$I_{L,max} = \frac{I_O}{(1-D)} + \frac{DV_S}{2LF_S + 2D(r_L + r_{SW})} \tag{2.12}$$

Since the ripple voltage due to the capacitor's ESR can be expressed in (2.13) and $\Delta i_C = I_{L,max}$, (2.12) can be plugged into (2.13) for Δi_C to yield (2.14).

$$\Delta V_{O,esr} = \Delta i_C r_C \tag{2.13}$$

$$\Delta V_{O,esr} = \left[\frac{I_O}{(1-D)} + \frac{DV_S}{2LF_S + 2D(r_L + r_{SW})}\right] r_C \tag{2.14}$$

In a worst-case situation, the ripple peaks due to the capacitor and ESR coincide and thus will need to be summed in order to produce a correct expression for output voltage ripple. In realistic circuits, these peaks will rarely be at the exact same spot, so (2.15) is a worst-case expression for total output voltage ripple.

$$\Delta V_{O,total} = \frac{DI_O}{CF_S} + \left[\frac{I_O}{(1-D)} + \frac{DV_S}{2LF_S + 2D(r_L + r_{SW})}\right] r_C \tag{2.15}$$

Efficiency

The efficiency in a boost converter can be modeled as shown in (2.16). Here, the power loss, P_{Loss}, has already been derived in (2.7) where I_L is given in (2.9). Using these two relationships, it can be shown that P_{Loss} is equivalent to the expression in (2.17).

$$\eta = \frac{P_O}{P_O + P_{Loss}} \tag{2.16}$$

$$P_{Loss} = I_O \left[\frac{r_L I_O + D r_{SW} I_O + V_D(1-D)^2}{(1-D)^2}\right] + \frac{1}{2} C_{SW} V_O^2 F_S \tag{2.17}$$

Since P_O is simply the power absorbed by the load, the efficiency of the non-ideal converter in CCM can be expressed as (2.18) after plugging in for I_O.

$$\eta_{CCM} = \frac{R(1-D)^2}{R(1-D)^2 + r_L + Dr_{SW} + \frac{1}{2}C_{SW}F_S R(1-D)^2 + \frac{V_D}{V_O}R(1-D)^2} \tag{2.18}$$

2.2 Discontinuous Conduction Mode (DCM)

Similar to the process involved in deriving the DC equations for CCM, the ideal DCM converter will be considered before addition of parasitics. From a theoretical standpoint, the derivation is nearly identical to that of CCM with the exception of needing to find an expression for D_1 in place of $(1-D)$ (refer to Figure 2.2).

2.2.1 Ideal Converter

When the switch is closed in the circuit shown earlier in Figure 2.1, the same thing happens in DCM as CCM so $\Delta i_{L,closed}$ is the same as (2.1). When the switch is open, however, there is a slight difference due to the fact that the inductor current goes to zero before the switching cycle. This difference can be attained by simply replacing the $(1-D)$ term in (2.2) with D_1, as shown in (2.19).

$$\Delta i_{L,open} = \frac{(V_S - V_O)D_1}{LF_S} \tag{2.19}$$

Since the sum of the change in inductor currents over one period must equal zero, adding (2.1) with (2.19) and solving for V_O results in an ideal DC output voltage equation shown in (2.20).

$$V_O = V_S\left(\frac{D+D_1}{D_1}\right) \tag{2.20}$$

However, (2.20) doesn't really say much since D_1 is currently unknown. Solving for this is important and also fairly easy; since the Δi_L is zero before any switching cycle starts (as this is what defines DCM operation), the maximum current, and thus the height of the triangular waveform in Figure 2.2, can be given by $\Delta i_{L,closed}$ in (2.1). From here, consider the average current through the diode. Since the diode only conducts during the D_1 cycle (as it is reverse-biased when the switch is closed

as described in Section 2.1.1), the average current through it is given by:

$$I_{D,avg} = \frac{1}{T_S}\left(\frac{1}{2} I_{max} D_1 T_S\right)$$
$$I_{D,avg} = \frac{1}{2} I_{max} D_1$$

When the diode is conducting, all of its current is delivered to the load, such that,

$$I_{D,avg} = I_O = \frac{V_O}{R}$$

After substituting (2.1) in for I_{max} and solving for D_1 yields (2.21):

$$D_1 = I_O\left(\frac{2LF_S}{V_S D}\right) = \left(\frac{V_O}{V_S}\right)\left(\frac{2LF_S}{RD}\right) \tag{2.21}$$

From here, equation (2.21) can be plugged into (2.20),

$$\frac{V_O}{V_S} = \frac{D + \left(\frac{V_O}{V_S}\right)\left(\frac{2LF_S}{RD}\right)}{\left(\frac{V_O}{V_S}\right)\left(\frac{2LF_S}{RD}\right)}$$
$$0 = \left(\frac{V_O}{V_S}\right)^2\left(\frac{2LF_S}{RD}\right) - \left(\frac{V_O}{V_S}\right)\left(\frac{2LF_S}{RD}\right) - D$$
$$\therefore 0 = \left(\frac{V_O}{V_S}\right)^2 - \left(\frac{V_O}{V_S}\right) - \frac{RD^2}{2LF_S}$$

Solving this quadratic for $\frac{V_O}{V_S}$ yields the final DCM output votlage expression shown below in (2.22).

$$V_O = \frac{V_S}{2}\left(1 + \sqrt{1 + \frac{2D^2}{\tau_L}}\right) \tag{2.22}$$

where

$$\tau_L = \frac{LF_S}{R} \tag{2.23}$$

Output Ripple

The derivation for output ripple is the same as that of CCM since the output current waveform is identical for the period when the switch is on. Because of this, the change

in charge in the output filter capacitor is $-I_O DT_S$, thus the output ripple for both CCM and DCM is given by (2.4).

Efficiency

As was the case for CCM, all of the input power must be delivered to the load due to the absence of loss mechanisms in the ideal DCM converter. Thus, efficiency must be 100%.

2.2.2 Non-Ideal Converter

In the Non-Ideal CCM converter, power loss was observed in order to obtain an output voltage expression and the same technique is used here for the Non-Ideal DCM Converter. The same parasitic losses in CCM operation contribute loss in DCM such that,

$$P_{Loss} = P_{r_L} + P_{SW} + P_D$$
$$P_S = P_O + P_{Loss}$$

Unlike the CCM derivation, however, it is not accurate to simply state that $P_S = V_S I_S$. In DCM, and as Figure 2.2 shows, there is a period of time during each switching cycle that the inductor current goes to zero. Since the switch is open, current can only flow from the source, through the inductor and diode, and then into the load. However, since there is no current in the inductor, there cannot be any current from the source which implies no power is being supplied by the source during that period. Thus, it's clear that,

$$P_S = (D + D_1) V_S I_S$$

Again, since the inductor only conducts during DT_S and $D_1 T_S$, its series resistance only absorbs power during that time. The rest of the loss mechanisms are similar to that of the CCM converter where the switch resistance absorbs power during DT_S while the diode only absorbs during $D_1 T_S$. Using this knowledge, (2.24) can be

constructed in order to derive an expression for the output voltage.

$$(D + D_1)V_S I_L = V_O I_O + (D + D_1)r_L I_L^2 + D r_{SW} I_L^2 + \frac{1}{2} C_{SW} V_O^2 F_S + D_1 V_D I_L \quad (2.24)$$

Since the output current is the same as the inductor current during the D_1 cycle, I_O can be said to be the same as $D_1 I_L$. Solving for I_L and plugging into (2.24) yields:

$$DV_S + D_1 V_S = D_1 V_O + \frac{D}{D_1} r_L I_O + r_L I_O + \frac{D}{D_1} r_{SW} I_O + \frac{D_1}{2I_O} C_{SW} V_O^2 F_S + D_1 V_D$$

From here, a few re-definitions are needed in order to keep the resulting equation manageable. First, recalling that D_1 is given as $\left(\frac{2LF_s}{DR}\right)\left(\frac{V_O}{V_S}\right)$ in (2.21) and $\tau_L = \frac{LF_S}{R}$ in (2.23), redefine:

$$M = \frac{V_O}{V_S} \quad (2.25)$$

$$r_X = \frac{r_L + r_{SW}}{R} \quad (2.26)$$

$$\kappa = \frac{V_D}{V_S} \quad (2.27)$$

$$\tau_{sw} = R C_{SW} F_S \quad (2.28)$$

Thus, D_1 becomes $\frac{2\tau_L}{D} M$ and the above parameters can be plugged into the power conservation equation which results in,

$$M^2 \left[1 + \frac{\tau_{sw}}{2}\right] + M \left[\frac{D r_L}{2R\tau_L} + \kappa - 1\right] + \left[\frac{D^2(D r_X - 2\tau_L)}{(2\tau_L)^2}\right] = 0$$

Solving this quadratic equation for M and plugging $\frac{V_O}{V_S}$ back into M yields the final output voltage equation for a Non-Ideal converter in DCM as shown in (2.29).

$$V_O = V_S \left[\frac{\sqrt{2D^2(\tau_{sw}+2)(2\tau_L - r_X) + 4\tau_L(\kappa-1)^2\left[\tau_L + D\frac{r_L}{R}\right] + \left(D\frac{r_L}{R}\right)^2}}{2\tau_L(\tau_{sw}+2)} \cdots \right.$$
$$\left. \cdots - \frac{2\tau_L(\kappa-1) - \frac{r_L}{R}}{2\tau_L(\tau_{sw}+2)} \right] \quad (2.29)$$

Obviously, (2.29) is rather vague due to the re-definitions from (2.25)-(2.28), but

it lends itself well to solving via software such as MATLAB®. In order to check the answer, eliminate all of the parasitics (κ, r_X, τ_{sw}, and r_L). This process yields:

$$M = \frac{\sqrt{8\tau_L D^2 + 4\tau_L^2} + 2\tau_L}{4\tau_L}$$

$$V_O = \frac{V_S}{2}\left(1 + \sqrt{\frac{8\tau_L D^2}{4\tau_L^2} + \frac{4\tau_L^2}{4\tau_L^2}}\right)$$

$$\therefore V_O = \frac{V_S}{2}\left(1 + \sqrt{1 + \frac{2D^2}{\tau_L}}\right) \checkmark$$

which verifies the ideal converter equation in (2.22).

Output Ripple

Just like in the ideal case, the output ripple due to the capacitor is identical to that of a converter operating in CCM (2.4). The ripple due to the ESR, however, does have a slight change: $(1 - D)$ in equation (2.12) is replaced with D_1. Plugging in for D_1 with (2.21) yields the following new expression for $I_{L,max}$ in DCM:

$$I_{L,max} = \frac{DV_S}{2LF_S} + \frac{DV_S}{2LF_S + 2D(r_L + r_{SW})} \tag{2.30}$$

Thus, by utilizing the expression for the ESR ripple voltage found previously in (2.13), the ESR ripple in DCM is determined by (2.31) where the worst-case total output ripple voltage is given by (2.32).

$$\Delta V_{O,esr} = \left[\frac{DV_S}{2LF_S} + \frac{DV_S}{2LF_S + 2D(r_L + r_{SW})}\right] r_C \tag{2.31}$$

$$\Delta V_{O,total} = \frac{DI_O}{CF_S} + \left[\frac{DV_S}{2LF_S} + \frac{DV_S}{2LF_S + 2D(r_L + r_{SW})}\right] r_C \tag{2.32}$$

Efficiency

To find the efficiency of the Non-Ideal converter in DCM, equation (2.16) is employed where P_{Loss} is given by (2.33).

$$P_{Loss} = (D + D_1) r_L I_L^2 + D r_{SW} I_L^2 + \frac{1}{2} C_{SW} V_O^2 F_S + D_1 V_D I_L$$

$$P_{Loss} = \frac{D}{D_1^2} r_L I_O^2 + \frac{1}{D_1} r_L I_O^2 + \frac{D}{D_1^2} r_{SW} I_O^2 + \frac{1}{2} C_{SW} V_O^2 F_S + V_D I_O$$

$$P_{Loss} = \frac{V_O^2}{R}\left[\left(\frac{D}{2LF_S}\right)^2 \left(\frac{V_S}{V_O}\right)^2 RDr_L + \frac{Dr_L}{2LF_S}\left(\frac{V_S}{V_O}\right) \cdots \right.$$
$$\left. \cdots + \left(\frac{D}{2LF_S}\right)^2 \left(\frac{V_S}{V_O}\right)^2 Dr_{SW} + \frac{1}{2} RC_{SW} F_S + \frac{V_D}{V_O}\right] \tag{2.33}$$

Plugging (2.33) into (2.16) results in an expression for the efficiency of a Non-Ideal converter in DCM given in (2.34).

$$\eta_{DCM} = \frac{1}{1 + \frac{D^3 R}{(2LF_S)^2}\left(\frac{V_S}{V_O}\right)^2 [r_L + r_{SW}] + \frac{Dr_L}{2LF_S}\left(\frac{V_S}{V_O}\right) + \frac{1}{2} RC_{SW} F_S + \frac{V_D}{V_O}} \tag{2.34}$$

2.3 CCM vs. DCM

Being able to compare the different parameters for CCM and DCM is important to develop understanding of the design trade-offs involved. However, comparison isn't as straight-forward as it initially may seem since operation in either mode depends on a number of parameters (L, F_S, I_O, etc.). In order to properly compare the two modes, the *realistic* operation needs to be compared to the converter ONLY in CCM and the converter ONLY in DCM (despite there being regions where the equations are invalid). To do so, the boundary between CCM and DCM needs to be defined.

Refer to Figure 2.2. Since DCM operation is defined by the inductor current reaching zero before the end of the switching cycle, the transition between CCM and DCM must occur when $D + D_1 = 1$. Thus,

$$1 = D + \left(\frac{V_O}{V_S}\right)\left(\frac{2LF_S}{RD}\right)$$
$$L = \frac{R(D - D^2)V_S}{2F_S V_O}$$

Since $\frac{V_O}{V_S} = \frac{1}{1-D}$ given in (2.3):

$$L_{crit} = \frac{(1 - \frac{V_S}{V_O})V_S^2}{2F_S V_O I_O} \tag{2.35}$$

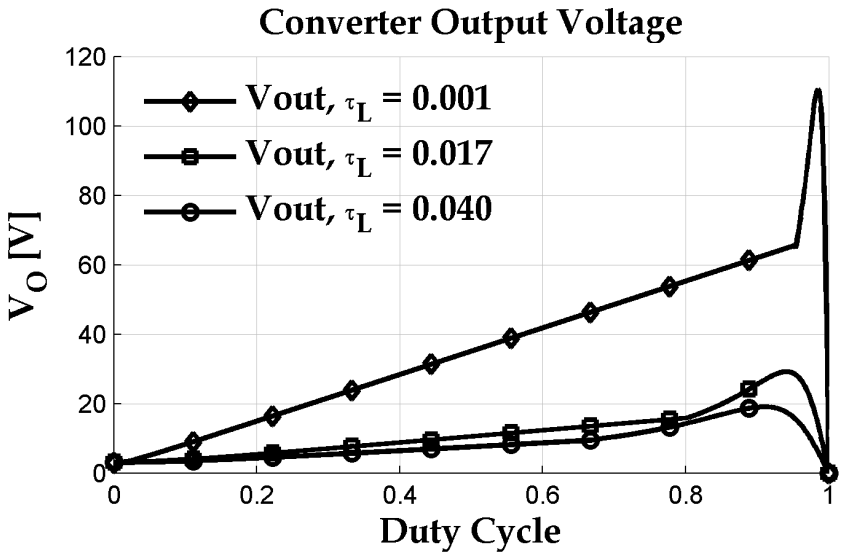

Figure 2.5: Output Voltage versus Duty Cycle Comparison for DCM and CCM

So if $L > L_{crit}$, that implies that the converter is operating in CCM whereas in any other case the converter is operating in DCM. Using this definition allows relatively seamless transition between modes, as shown in Figure 2.5. Note that the following parameters were used in all examples in this section: $L = 18\,\mu H$, $C = 4.7\,\mu F$, $V_S = 3.5\,V$, $F_S = 350\,kHz$, $r_L = 1\,\Omega$, $r_{SW} = 0.3\,\Omega$, $r_C = 0.1\,\Omega$, $V_D = 0.3\,V$, $C_{OSS} = 50\,pF$, and $C_D = 10\,pF$ with an ideal $V_O = 5.5\,V$ and I_O varying as $1\,mA$, $15\,mA$, and $35\,mA$. The load resistance, R, was simply calculated by taking the ideal V_O value and dividing by each defined load current.

Figures 2.6 and 2.7 show the converter efficiency and ripple voltage. As mentioned in Section 2.1.2, the discontinuity in the efficiency plot can be attributed to the approximation that in DCM the switch capacitance charges and discharges to V_O rather than V_S [11].

Sensitivity to Parasitics

Observing the sensitivity that different parasitics have on the DC operation of the converter is important to develop an understanding of which parameters contribute most to the non-ideal behavior. Figures 2.8, and 2.9 depict the sensitivity of the converter efficiency in both CCM and DCM with respect to r_L and C_{SW}, respectively.

The inductor resistance, r_L exhibits similar sensitivity effects for both CCM and

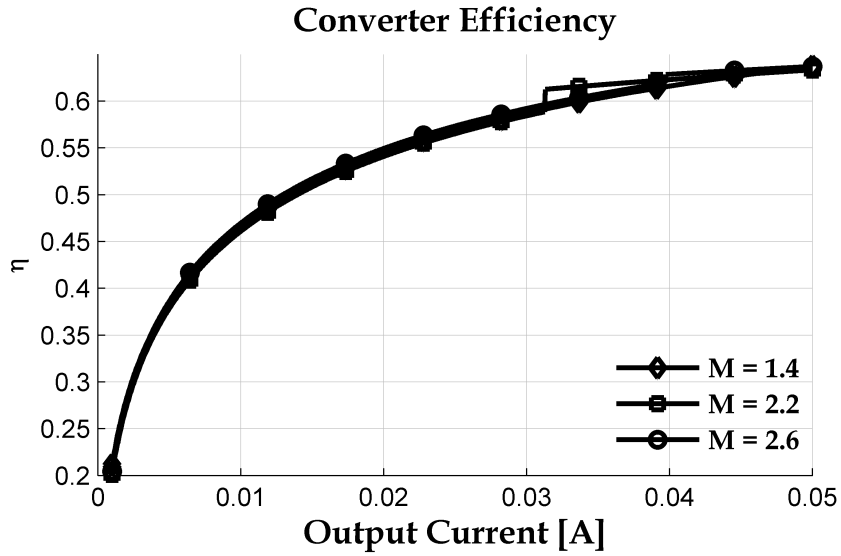

Figure 2.6: Efficiency versus Output Current Comparison for DCM and CCM

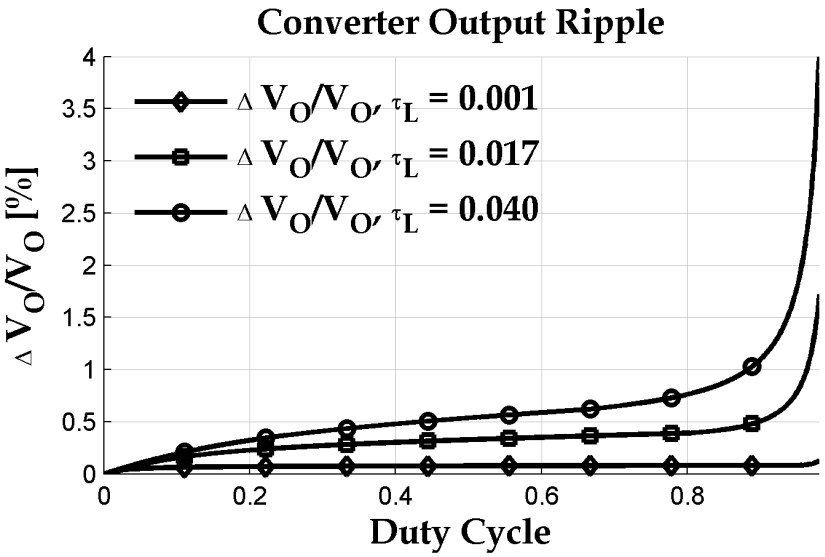

Figure 2.7: Output Ripple Voltage versus Duty Cycle Comparison for DCM and CCM

DCM with the DCM plot being slightly more affected. For large resistances ($10\,\Omega$ or higher), the sensitivity of the efficiency plots approaches -1 which implies that an r_L of those sizes would essentially render the converter unusable (since efficiency, at best, can be 1). Typical inductor series resistance values fall in the $m\Omega$ range, and thus have a much smaller impact on efficiency (as indicated in Figure 2.8). However, the slope of the sensitivity in this range is quite large, thus any small variations in r_L can

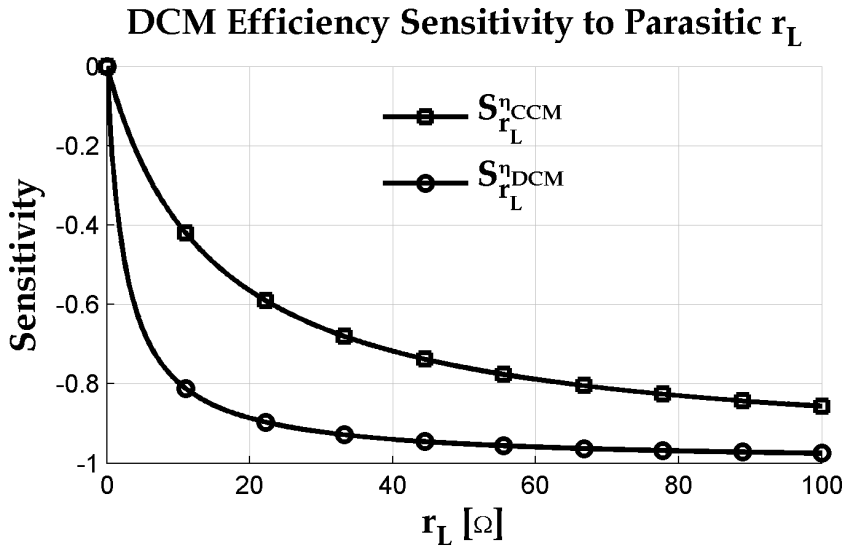

Figure 2.8: Sensitivity of Efficiency to Changing r_L for CCM and DCM

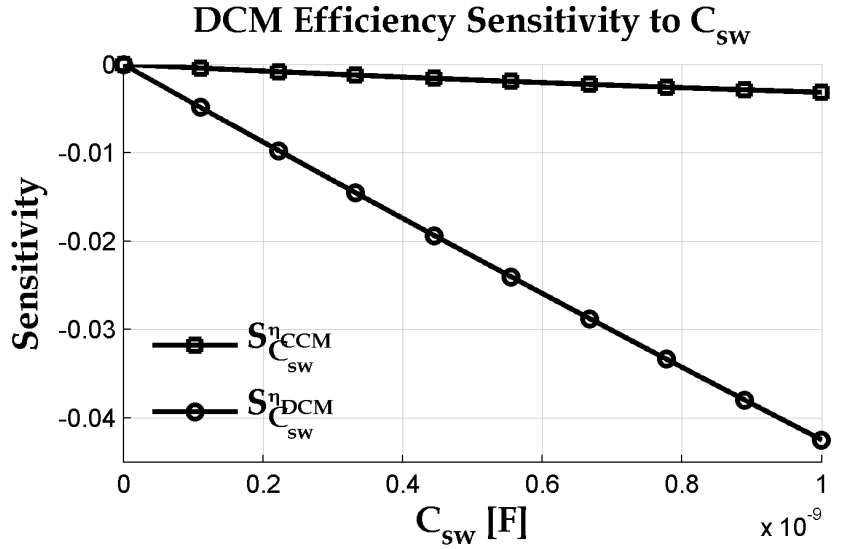

Figure 2.9: Sensitivity of Efficiency to Changing C_{SW} for CCM and DCM

result in a rather substantial decrease in efficiency. Another problem associated with this is that typically an inductor's series resistance will have a positive temperature coefficient so as the inductor's temperature begins to increase, the resistance will increase, and thus the efficiency will decrease. The equation for this sensitivity plot

is found in (2.36) and (2.37).

$$S_{r_L}^{\eta_{CCM}} = \frac{-r_L}{R(1-D)^2 + r_L + Dr_{SW} + \frac{1}{2}C_{SW}F_S R(1-D)^2 + \frac{V_D}{V_O}R(1-D)^2} \tag{2.36}$$

$$S_{r_L}^{\eta_{DCM}} = \frac{-r_L\left[\frac{D^3R}{(2LF_S)^2}\left(\frac{V_S}{V_O}\right)^2 + \frac{DR}{2LF_S}\left(\frac{V_S}{V_O}\right)\right]}{1 + \frac{D^3R}{(2LF_S)^2}\left(\frac{V_S}{V_O}\right)^2[r_L + r_{SW}] + \frac{Dr_L}{2LF_S}\left(\frac{V_S}{V_O}\right) + \frac{1}{2}RC_{SW}F_S + \frac{V_D}{V_O}} \tag{2.37}$$

The plot in Figure 2.9 is almost comical in that the converter in CCM seems to be totally unaffected by increasing the C_{SW} value, whereas the converter in DCM has a nearly linear relationship with increasing this value. It should be noted that if the graph were to be extrapolated into the μF range that the curve resembled something more along the lines of Figure 2.8. For switch capacitance values less than $1\,nF$, the sensitivity of the DCM converter will increase by 0.005 for roughly every 100 pF increase in capacitance. The sensitivity equations for CCM and DCM are given in (2.38) and (2.39), respectively.

Overall, the capacitance has a significantly smaller impact on the efficiency than that of the inductor series resistance. It may not be a negligible amount, but it's fairly clear the inductor series resistance poses a very large threat to converter operation.

$$S_{C_{SW}}^{\eta_{CCM}} = \frac{-\frac{1}{2}RC_{SW}F_S(1-D)^2}{R(1-D)^2 + r_L + Dr_{SW} + \frac{1}{2}C_{SW}F_S R(1-D)^2 + \frac{V_D}{V_O}R(1-D)^2} \tag{2.38}$$

$$S_{C_{SW}}^{\eta_{DCM}} = \frac{-\frac{1}{2}RC_{SW}F_S}{1 + \frac{D^3R}{(2LF_S)^2}\left(\frac{V_S}{V_O}\right)^2[r_L + r_{SW}] + \frac{Dr_L}{2LF_S}\left(\frac{V_S}{V_O}\right) + \frac{1}{2}RC_{SW}F_S + \frac{V_D}{V_O}} \tag{2.39}$$

Final Thoughts

It's rather difficult to state which mode is "better" since each have their own merits. Operating in DCM allows for the inductor size to be smaller since it doesn't need to maintain a current through each switching cycle. However, DCM is affected far more by the dynamic switching power loss mechanisms as discussed previously and as evidenced by Figure 2.6. As Figure 2.5 shows, as the output current decreases, the dynamic switching loss begins to have a large impact on the converter efficiency and is much worse in the case of the DCM converter. However, despite the apparent

shortcomings of operating a Boost Converter in DCM, there is increased controllability which is important to maintain a stiff, regulated output. This will be discussed in detail throughout Chapter 3.

Chapter 3

Small-Signal Analysis

A conventional DC switched converter consists of three main components: DC Converter, Error Amplifier, and PWM Generator. This architecture is shown in block diagram form in Figure 3.1.

The DC characteristics of the converter block have already been discussed in Chapter 2. The purpose of this block is simply to take a DC voltage, V_S, and convert it to a different, scaled, voltage. This block can assume a number of different architectures (Buck, Boost, Buck-Boost, *etc.*), but the boost architecture is what is specifically focused on within the contents of this thesis. That said, Figure 3.1 is a general form that can be used for any DC-DC converter.

The Error Amplifier block is simply an amplifier that serves to minimize the steady-state error of the converter. This is typically done with a resistive voltage divider that is fed from the output of the Converter block to the input of an Op-Amp or OTA. The various Error Amplifier architectures are explored more thoroughly throughout Chapter 4.

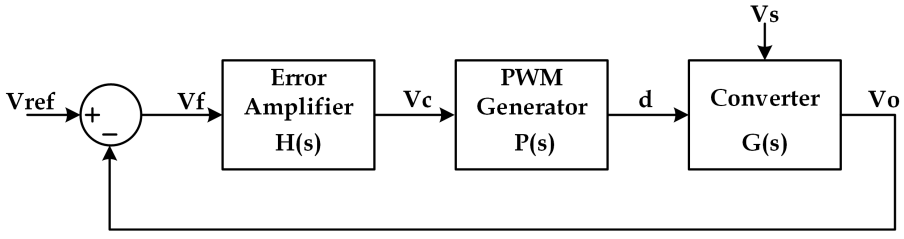

Figure 3.1: Regulated DC Converter Block Diagram (Adapted from [13])

Finally, the last major block within a regulated DC-DC converter is the PWM Generator. This takes the error signal produced by the amplifier, V_c, and converts it to a digital signal in order to properly drive the switch within the converter. Based on the DC level of V_c, the PWM Generator will modulate the pulse-width which results in a varying duty-cycle.

Understanding the role of each of these blocks is incredibly important because the system is, inherently, a feedback network. This requires careful consideration to be taken in regards to small-signal performance has the system as the potential to become unstable and create an oscillator instead of a steady, regulated output voltage.

This chapter will illustrate the analytic techniques used for deriving small-signal models and transfer functions for a Boost Converter in CCM and DCM operation. The PWM Generator block transfer function will also be derived. Since the Error Amplifier is observed in more detail within Chapter 4, the small-signal analysis of that block will be deferred.

3.1 PWM Generation

Figure 3.2 depicts the conventional circuit used for PWM generation. The amplified error signal, V_c, is fed into the inverting terminal on the comparator and a voltage ramp operating at the switching frequency, F_S, is fed into the non-inverting terminal. When the error voltage matches the value of the input ramp, the comparator triggers

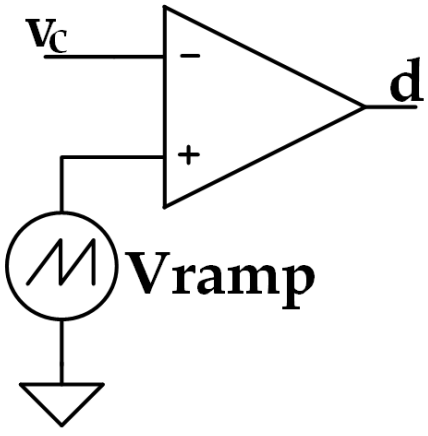

Figure 3.2: PWM Generation Circuit

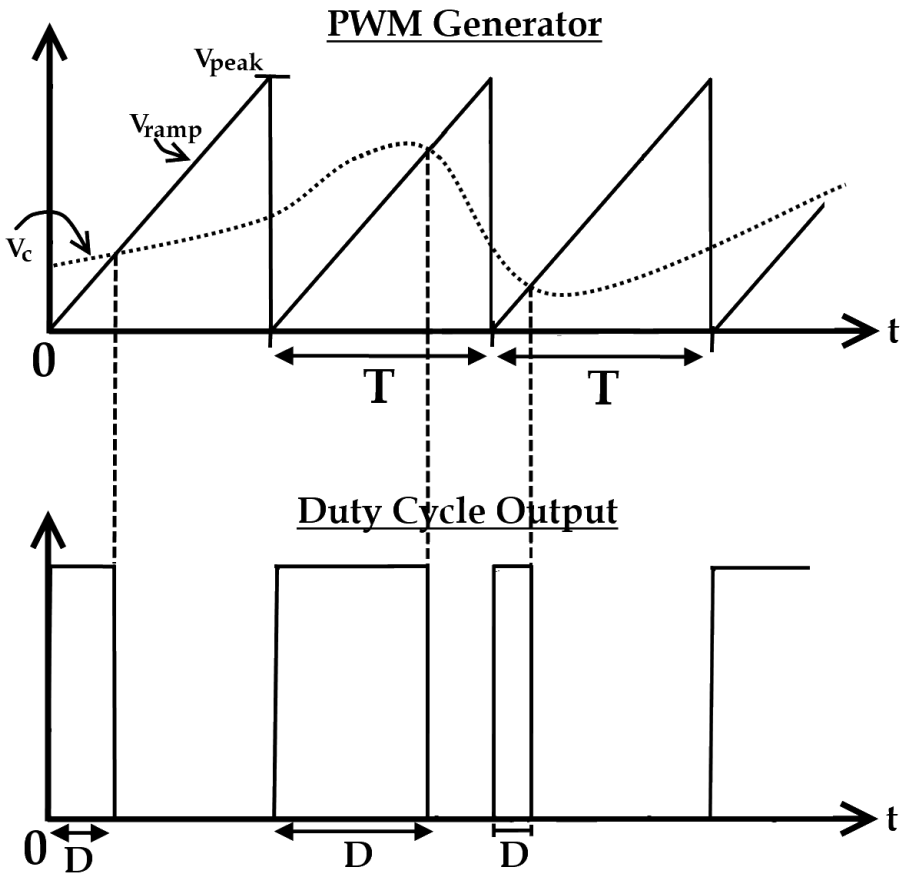

Figure 3.3: PWM Generation Circuit Waveforms

high (causing the switch to open) which, with a varying error signal, will cause a modulation of the duty cycle in the output digital waveform. Modulation of this duty cycle is what controls the output voltage of the converter block. This process is depicted schematically in Figure 3.3.

Since the input to the PWM block is V_c and the output is d, it is necessary to find the small-signal transfer function $\frac{d}{V_c}$. Doing so is rather straight forward by observation of the waveforms in Figure 3.3: the duty cycle will simply be equal to the ratio of the error signal to the ramp voltage peak (as V_c increases, the duty cycle follows linearly). Thus,

$$P(s) = \frac{d}{V_c} = \frac{1}{V_{peak}} \tag{3.1}$$

3.2 State-Space Averaging

The idea of using State-Space Averaging (commonly shortened to SSA) as a way to model switched converters was first introduced by R.D. Middlebrook and Slobodan Ćuk [14]. Since then, it has widely been used as a way to extract various small-signal and averaged DC transfer functions [15–17].

The basic premise is simple: by obtaining *averaged* values for each relevant node voltage and current, a model can be developed which effectively ignores the effects of the high-frequency switching which, in turn, allows for a linear small-signal model to be developed. In order to properly obtain a small-signal model for a given converter, the following steps must be performed:

1. Obtain equations for each state (closed/open).
2. Average the equations over one switching period.
3. Perturb the average equations so that each variable has a DC and AC component.
4. Take Laplace Transform.
5. Place new equations into matrices.
6. Extract desired transfer function.

To illustrate this process, an ideal Boost Converter operating in CCM will be used.

State 1: Switch Closed

The first state under consideration where the switch is closed is shown schematically in Figure 3.4. Using KVL along the left-hand loop, it's clear that:

$$\begin{aligned} V_S &= V_L \\ V_S &= L\frac{di_L}{dt} \\ \therefore \frac{di_L}{dt} &= \frac{V_S}{L} \end{aligned} \tag{3.2}$$

Applying KCL along the right-hand loop yields:

$$\begin{aligned} I_C &= -I_R \\ C\frac{dv_o}{dt} &= -\frac{v_o}{R} \\ \therefore \frac{dv_o}{dt} &= -\frac{v_o}{RC} \end{aligned} \tag{3.3}$$

State 2: Switch Open

The next state is when the switch is open, as shown schematically in Figure 3.5. Using KVL along the left-hand loop, and KCL along the right-hand loop (as was done previously), it's clear that:

$$\begin{aligned} V_S &= V_L + v_o \\ V_S &= L\frac{di_L}{dt} + v_o \\ \therefore \frac{di_L}{dt} &= \frac{V_S}{L} - \frac{v_o}{L} \end{aligned} \tag{3.4}$$

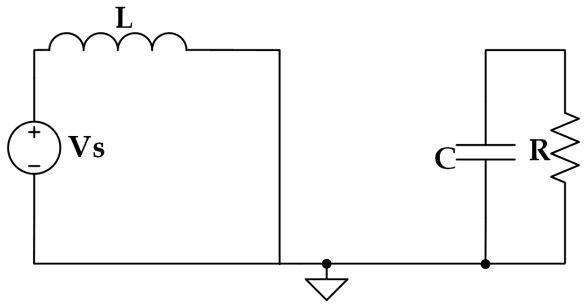

Figure 3.4: Ideal Boost Converter with Switch Closed

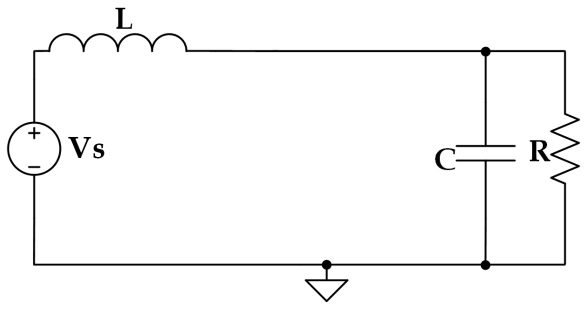

Figure 3.5: Ideal Boost Converter with Switch Open

And,

$$\begin{aligned} I_C &= i_L - I_R \\ C\frac{dv_o}{dt} &= i_L - \frac{v_o}{R} \\ \therefore \frac{dv_o}{dt} &= \frac{i_L}{C} - \frac{v_o}{RC} \end{aligned} \tag{3.5}$$

Averaging the State Equations

Because the converter is assumed to be operating in CCM, the switch will be closed for the duration of some time dT_S while it will be open for some time $(1-d)T_S$ (where d is the duty-cycle and T_S is the switching period). Thus, the averaged state equations can be determined by adding (3.2) with (3.4) and (3.3) with (3.5) such that:

$$\begin{aligned} \dot{i_L} &= \frac{1}{T_S}\left[dT_S\left(\frac{V_S}{L}\right) + (1-d)T_S\left(\frac{V_S}{L} - \frac{v_o}{L}\right)\right] \\ \dot{i_L} &= \frac{1}{L}V_S - \frac{1-d}{L}v_o \end{aligned} \tag{3.6}$$

And,

$$\begin{aligned} \dot{v_o} &= \frac{1}{T_S}\left[dT_S\left(-\frac{v_o}{RC}\right) + (1-d)T_S\left(\frac{i_L}{C} - \frac{v_o}{RC}\right)\right] \\ \dot{v_o} &= \frac{1-d}{C}i_L - \frac{1}{RC}v_o \end{aligned} \tag{3.7}$$

Perturbation and Laplace Transformation

In order to derive small-signal models, the averaged equations must contain small signal variables. This is done by replacing each variable with both a DC and AC value such that a variable x would be equated to $X + \hat{x}$. Performing this perturbation to the variables i_L, v_o, and d yields:

$$\begin{aligned} \frac{d(I_L + \hat{i_L})}{dt} &= \frac{1}{L}V_S - \frac{1-D-\hat{d}}{L}(V_O + \hat{v_o}) \\ \frac{d(V_O + \hat{v_o})}{dt} &= \frac{1-D-\hat{d}}{C}(I_L + \hat{i_L}) - \frac{1}{RC}(V_O + \hat{v_o}) \end{aligned}$$

After expanding the above equations and eliminating both pure DC quantities and quantities containing multiples of AC quantities (since two small numbers multiplied by each other yield an even smaller number), the following equations are produced:

$$\hat{i_L} = \frac{\hat{d}}{L}V_O - \frac{1}{L}\hat{v_o} + \frac{D}{L}\hat{v_o} \tag{3.8}$$

$$\hat{v_o} = \frac{1-D}{C}\hat{i_L} - \frac{\hat{d}}{C}I_L - \frac{1}{RC}\hat{v_o} \tag{3.9}$$

Taking the Laplace Transform of (3.8) and (3.9) and rearranging such that the state variables $\hat{i_L}$ and $\hat{v_o}$ end up on the right-hand side of each equation yield:

$$\hat{d}V_O = sL\hat{i_L} + (1-D)\hat{v_o} \tag{3.10}$$

$$\hat{d}I_L = (1-D)\hat{i_L} - \left(sC + \frac{1}{R}\right)\hat{v_o} \tag{3.11}$$

Matrix Creation

Creating the state matrices is straight forward by observation of (3.10) and (3.11):

$$\begin{bmatrix} V_O \\ \\ I_L \end{bmatrix} \hat{d} = \begin{bmatrix} sL & (1-D) \\ \\ (1-D) & -\left(sC + \frac{1}{R}\right) \end{bmatrix} \begin{bmatrix} \hat{i_L} \\ \\ \hat{v_o} \end{bmatrix}$$

Since the goal is to obtain a transfer function for $\frac{\hat{v_o}}{\hat{d}}$, the inverse of the A-Matrix (that is, the 2×2 matrix on the right-hand side of the above equation) must be pre-multiplied on each side and the variable $\hat{d}$ must be divided by each side such that the expression in (3.12) results,

$$\frac{1}{\hat{d}} \begin{bmatrix} \hat{i_L} \\ \\ \hat{v_o} \end{bmatrix} = \begin{bmatrix} sL & (1-D) \\ \\ (1-D) & -\left(sC + \frac{1}{R}\right) \end{bmatrix}^{-1} \begin{bmatrix} V_O \\ \\ I_L \end{bmatrix} \tag{3.12}$$

Taking the inverse of the A matrix can be tedious, especially as the matrix dimen-

sions begin to increase. As such, it's wise to use a program such as MATLAB® in order to eliminate any potential mistakes that are likely to arise in a hand-derivation. The inverse of the A-matrix is shown in 3.13. Thus, it's clear that the expression in 3.14 is the correct small-signal control-to-output transfer function.

$$A^{-1} = \frac{1}{s^2RLC + sL + R(1-D)^2} \begin{bmatrix} sRC+1 & R(1-D) \\ R(1-D) & -sLR \end{bmatrix} \tag{3.13}$$

$$\frac{\hat{v_o}}{\hat{d}} = \frac{V_O}{1-D}\left[\frac{-sL + R(1-D)^2}{s^2RLC + sL + R(1-D)^2}\right] \tag{3.14}$$

In a more general form, this transfer function can be expressed as:

$$\frac{\hat{v_o}}{\hat{d}} = G_{d0}\frac{(1-\frac{s}{\omega_{z,1}})(1+\frac{s}{\omega_{z,2}})}{\frac{s^2}{\omega_0^2} + \frac{s}{Q\omega_0} + 1} \tag{3.15}$$

$$G_{d0} = \frac{V_O}{1-D} \tag{3.16}$$

$$\omega_{z,1} = \frac{R(1-D)^2}{L} \tag{3.17}$$

$$\omega_{z,2} = \infty \tag{3.18}$$

$$\omega_0 = \frac{1-D}{\sqrt{LC}} \tag{3.19}$$

$$Q = R(1-D)\sqrt{\frac{C}{L}} \tag{3.20}$$

SSA is a very nice way to generate switched-converter transfer functions; however, they're quite tedious. Any time the converter topology changes or components are added to the circuit (parasitics, for example), all of the state equations and perturbations need to be repeated.

3.3 Average PWM Model

As a solution to the problems associated with State-Space Averaging, Vatché Vorpérian introduced the idea of an averaged PWM Switch model [18,19]. Since the only switch-

ing components within a converter are the diode and switch itself, Vorpérian reasoned that an equivalent circuit model for this switch/diode combination would be simpler than SSA as a single, general model could be generated and placed in any converter topology [18].

The circuit used to generated the equivalent circuit for both CCM and DCM operation is shown in Figure 3.6. There are three terminals: active, passive, and common. The active node is the node which connects to only the switch, the passive connects only to the diode, and the common connects to both (as Figure 3.6 indicates). Once the equivalent PWM Switch circuit is derived, it can be used in *any* configuration in *any* converter topology; in essence, it only needs to be derived once.

The PWM Switch can be derived in three different ways, depending on the orientation of the switch. Regardless of which configuration used, the resultant circuit model will be the same. Since the analysis up to this point has focused solely on boost converter topologies, the switch will be assumed to be in a common-active configuration for all derivations, as shown in Figure 3.7. This nomenclature refers to which node is connected to the common point on the circuit, typically ground. Thus, three orientations can be used: common-active, common-passive, or common-common.

3.3.1 PWM Switch in CCM

The analysis of the PWM Switch in CCM is rather straight forward under the assumption that the current through the inductor is constant. Consider the active current, I_a. When the switch is on, during time interval dT_S, $I_a = I_c$. When the switch is

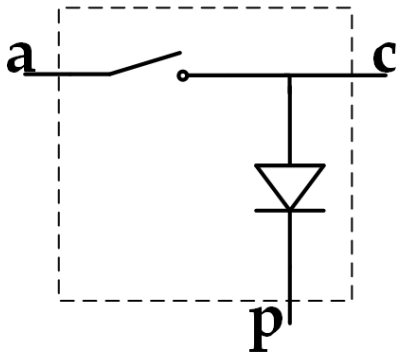

Figure 3.6: PWM Switch (adapted from [18] and [19])

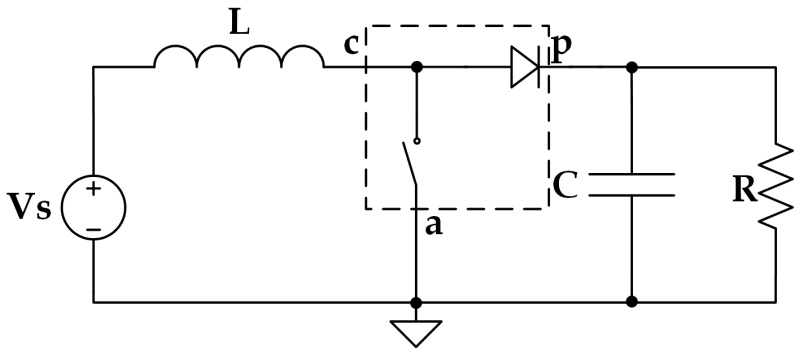

Figure 3.7: Ideal Boost Converter with Common-Active PWM Switch

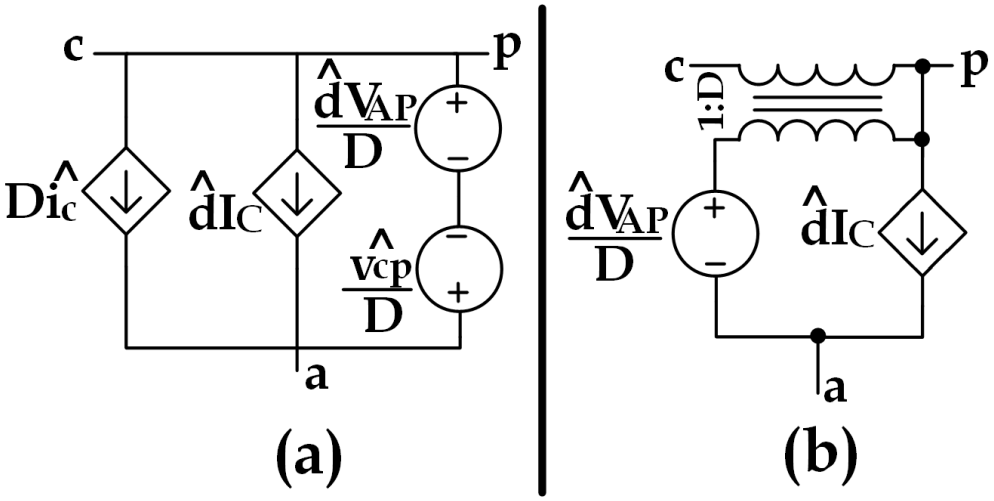

Figure 3.8: Common-Active PWM Model in CCM (a) direct equation-to-circuit model (b) transformer model

closed, the active node is floating and, thus, $I_a = 0$. Averaging these conditions over the entire switching period, T_S, results in (3.21). Likewise, during the interval dT_S, the common-passive voltage, V_{cp} will be the same as the active-passive voltage, V_{ap} since in this state $V_c = V_a$. When the switch is opened, $V_c = V_p$, thus, $V_{cp} = 0$. Averaging V_{cp} over the entire switching period results in (3.22).

$$I_a = dI_c \tag{3.21}$$

$$V_{cp} = dV_{ap} \tag{3.22}$$

These equations are then perturbed, similar to the process used in the State-Space Averaging technique explained earlier. After perturbation of the variables I_a, d, V_{cp}, and V_{ap} (along with the cancellation of higher-order small-signal terms), the small-signal parameters of $\hat{i_a}$ and $\hat{v_{cp}}$ can be derived, as shown in (3.23) and (3.24), respectively.

$$\hat{i_a} = D\hat{i_c} + \hat{d}I_C \tag{3.23}$$

$$\hat{v_{cp}} = D\hat{v_{ap}} + \hat{d}V_{AP} \tag{3.24}$$

Figure 3.8a shows the average PWM Model in CCM with (3.23) and (3.24) dropped right into the circuit while Figure 3.8b shows the circuit with a $1 : D$ ideal transformer used to replace the $D\hat{ic}$ voltage source and $D\hat{v_{ap}}$ current source.

3.3.2 PWM Switch in DCM

To begin analysis, it is necessary to consider both switching events; that is when the switch is open, dT_S, and when the switch is closed, d_1T_S. By defining the currents at each node of the PWM switch as always *entering* a node, the following can be said of the average voltages and currents during the "on" state:

$$\begin{aligned} I_c &= -I_a = I_L \\ I_{L,avg} &= \frac{I_{L,max}}{2} \\ \therefore I_a &= -d\frac{I_{L,max}}{2} \end{aligned} \tag{3.25}$$

Since the change in inductor current, Δi_L, in DCM will go from zero to some maximum value during one switching cycle, the change will just end up equaling that maximum value. Since $I_{L,max} = \Delta i_L$, it is clear that:

$$\begin{aligned} V_{ac} &= -V_L = -L\frac{\partial i_L}{\partial t} \\ V_{ac} &= -L\frac{\Delta i_L}{\Delta t} \end{aligned}$$

$$V_{ac} = -L\frac{I_{L,max}}{dT_S} \tag{3.26}$$

During the "off" state, it is clear that the same process can be used to derive expressions for I_p and V_{cp} such that,

$$\begin{aligned} I_c &= -I_p = I_L \\ I_{L,avg} &= \frac{I_{L,max}}{2} \\ I_p &= -d_1\frac{I_{L,max}}{2} \end{aligned} \tag{3.27}$$

Likewise, since this is a small-signal derivation, $V_S = 0\,V$ which implies:

$$\begin{aligned} V_{cp} &= -V_L = -L\frac{\partial i_L}{\partial t} \\ V_{cp} &= -L\frac{\Delta i_L}{\Delta t} \\ V_{cp} &= -L\frac{I_{L,max}}{d_1 T_S} \end{aligned} \tag{3.28}$$

From these equations, the following relationships between terminal currents and voltages can be derived:

$$-\frac{I_{L,max}}{2} = \frac{I_p}{d_1} = \frac{I_a}{d}$$

and

$$-L\frac{I_{L,max}}{T_S} = dV_{ac} = d_1 V_{cp}$$

Therefore, it's clear that:

$$I_a = I_p\frac{d}{d_1} \tag{3.29}$$

$$V_{ac} = V_{cp}\frac{d_1}{d} \tag{3.30}$$

Rearranging equations (3.25) and (3.26) and plugging it into (3.28) and (3.27),

respectively, yields

$$V_{cp} = \frac{2LI_aF_S}{(d)(d_1)}$$

and

$$V_{ac} = \frac{2LI_pF_S}{(d)(d_1)}$$
$$\therefore d_1 = \frac{2LF_S}{d}\frac{I_a}{V_{cp}} = \frac{2LF_S}{d}\frac{I_p}{V_{ac}} \tag{3.31}$$

This expression for d_1 can then be plugged into (3.30) to yield:

$$V_{ac} = \frac{2LF_S}{d}\frac{I_a}{V_{cp}}(\frac{1}{d})V_{cp}$$
$$V_{ac} = \frac{2LF_S}{d^2}\frac{I_a}{V_{cp}}V_{cp}$$
$$\therefore V_{cp} = \frac{d^2}{2LF_S}\frac{V_{cp}}{I_a}V_{ac}$$

and

$$V_{ac} = \frac{2LF_S}{d}\frac{I_p}{V_{ac}}(\frac{1}{d})V_{cp}$$
$$V_{ac} = \frac{2LF_S}{d^2}\frac{I_p}{V_{ac}}V_{cp}$$
$$\therefore V_{cp} = \frac{d^2}{2LF_S}\frac{V_{ac}}{I_p}V_{ac}$$

Thus,

$$V_{cp} = \mu V_{ac} \tag{3.32}$$

where

$$\mu = \frac{d^2}{2LF_S}\frac{V_{cp}}{I_a} = \frac{d^2}{2LF_S}\frac{V_{ac}}{I_p} = \frac{d}{d_1} \tag{3.33}$$

Now, by taking the expression for d_1 in (3.31) and substituting it into (3.29), the following relationship appears:

$$I_a = I_p d(\frac{d}{2LF_S})(\frac{I_a}{V_{cp}})$$

$$I_a = \frac{d^2}{2LF_S}(\frac{I_a}{V_{cp}})I_p$$
$$\therefore I_a = \mu I_p \tag{3.34}$$

Using the average equations derived in the previous section, a small-signal model can be derived by perturbing each node current and voltage as well as the duty-cycle. To perform this perturbation analysis, the following relationships must be established:

$$I_a = I_A + \hat{i_a}$$
$$I_p = I_P + \hat{i_p}$$
$$V_{ac} = V_{AC} + \hat{v_{ac}}$$
$$d = D + \hat{d}$$

The first step will be to substitute these values, which contain steady-state and small-signal components, into both (3.34) and (3.31) (and ignoring higher-order small-signal quantities),

$$I_A + \hat{i_a} = \frac{D + \hat{d}}{d_1}(I_P + \hat{i_p})$$
$$d_1 = \frac{2LF_S}{D + \hat{d}}\frac{I_P + \hat{i_p}}{V_{AC} + \hat{v_{ac}}}$$
$$\therefore I_A + \hat{i_a} = \frac{D + \hat{d}}{\frac{2LF_S}{D+\hat{d}}\frac{I_P+\hat{i_p}}{V_{AC}+\hat{v_{ac}}}}(I_P + \hat{i_p})$$
$$I_A + \hat{i_a} = \frac{DV_{AC} + D\hat{v_{ac}} + \hat{d}V_{AC}}{2LF_S}(D + \hat{d})$$
$$\therefore \left(\frac{I_A}{V_{AC}}\right)\left(\frac{2LF_S}{D^2}\right)(I_A + \hat{i_a}) = I_A + \frac{I_A}{V_{AC}}\hat{v_{ac}} + \frac{2I_A}{D}\hat{d}$$

From (3.30), $V_{AC} = \frac{D_1}{D}V_{CP}$, therefore:

$$\left(\frac{1}{D_1}\right)\left(\frac{I_A}{V_{CP}}\right)\left(\frac{2LF_S}{D}\right)(I_A + \hat{i_a}) = I_A + \frac{I_A}{V_{AC}}\hat{v_{ac}} + \frac{2I_A}{D}\hat{d}$$

From (3.31), $D_1 = \frac{2LF_S}{D}\frac{I_A}{V_{CP}}$, so the term on the left-hand side of the equation cancels leaving:

$$\hat{i_a} = \frac{I_A}{V_{AC}}\hat{v_{ac}} + \frac{2I_A}{D^2}\hat{d}$$

From here, the coefficients to the small signal parameters can be defined as:

$$g_i = \frac{I_A}{V_{AC}} \tag{3.35}$$

$$k_i = \frac{2I_A}{D} \tag{3.36}$$

$$\therefore \hat{i_a} = g_i\hat{v_{ac}} + k_i\hat{d} \tag{3.37}$$

Next it is necessary to perturb equation (3.30) in order to obtain a relationship for the small-signal current at the passive terminal, $\hat{i_p}$:

$$\begin{aligned}
V_{AC} + \hat{v_{ac}} &= \frac{d_1}{D + \hat{d}}(V_{CP} + \hat{v_{cp}}) \\
V_{AC} + \hat{v_{ac}} &= \frac{2LF_S}{D^2 + 2D\hat{d}}\left(\frac{I_P V_{CP} + I_P\hat{v_{cp}} + \hat{i_p}V_{CP}}{V_{AC} + \hat{v_{ac}}}\right) \\
\frac{V_{AC}^2 + 2V_{AC}\hat{v_{ac}}}{2LF_S} &= \frac{I_P V_{CP} + I_P\hat{v_{cp}} + \hat{i_p}V_{CP}}{D^2 + 2D\hat{d}} \\
(I_P + \hat{i_p})V_{CP} &= \frac{V_{AC}^2 + 2V_{AC}\hat{v_{ac}}}{2LF_S}(D^2 + 2D\hat{d}) - I_P\hat{v_{cp}} \\
I_P + \hat{i_p} &= \frac{1}{2LF_S}\left[\frac{V_{AC}^2 D^2}{V_{CP}} + \frac{2V_{AC}^2 D\hat{d}}{V_{CP}} + \frac{2D^2 V_{AC}\hat{v_{ac}}}{V_{CP}}\right] - \frac{I_P}{V_{CP}}\hat{v_{cp}}
\end{aligned}$$

From (3.30), $\frac{V_{AC}}{V_{CP}} = \frac{D_1}{D}$, therefore:

$$\begin{aligned}
I_P + \hat{i_p} &= \frac{D_1}{2LF_S}[DV_{AC} + 2V_{AC}\hat{d} + 2D\hat{v_{ac}}] - \frac{I_P}{V_{CP}}\hat{v_c}p \\
\therefore I_P + \hat{i_p} &= \frac{I_P}{DV_{AC}}[DV_{AC} + 2V_{AC}\hat{d} + 2D\hat{v_{ac}}] - \frac{I_P}{V_{CP}}\hat{v_c}p \\
\hat{i_p} &= \frac{2I_P}{D}\hat{d} + \frac{2I_P}{V_{AC}}\hat{v_{ac}} - \frac{I_P}{V_{CP}}\hat{v_{cp}}
\end{aligned}$$

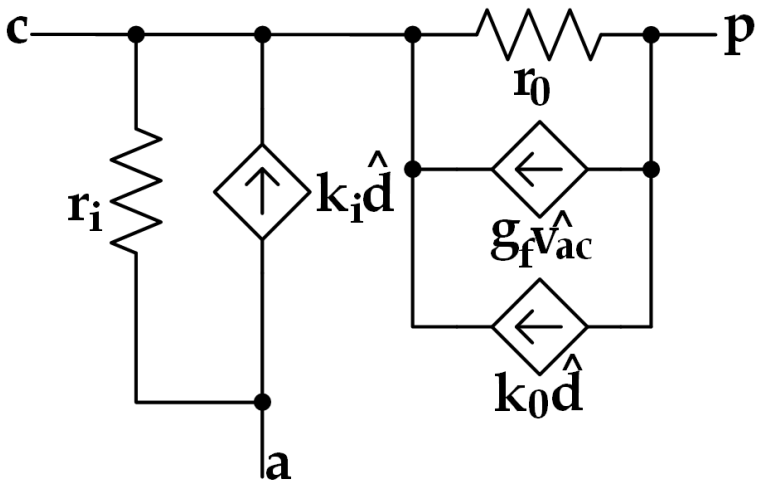

Figure 3.9: Equivalent Circuit for Small-Signal PWM Switch in DCM

Thus, the following parameters can be defined:

$$k_0 = \frac{2I_P}{D} \tag{3.38}$$

$$g_0 = \frac{I_P}{V_{CP}} \tag{3.39}$$

$$g_f = \frac{2I_P}{V_{AC}} \tag{3.40}$$

which results in a final expression for the small-signal current at the passive node as:

$$\hat{i_p} = g_f \hat{v_{ac}} + k_0 \hat{d} - g_0 \hat{v_{cp}} \tag{3.41}$$

Now, since expressions for both the small-signal currents at the active and passive nodes have been derived, a small-signal circuit model can be created for the PWM switch as shown in Figure 3.9. Note that this model is in agreement with those derived by both by Vorpérian in [19] and by Reatti and Kazimierczuk in [20].

3.4 Transfer Functions

In order to derive the small-signal transfer functions for the boost converter in both CCM and DCM, the derived models (Figures 3.8 and 3.9, respectively) will be placed

into the boost architecture and then analyzed. Using State-Space Averaging, the ideal CCM transfer function was derived in (3.14) but will be re-derived in order to illustrate the accuracy of the PWM Model. Parasitics will be added to the circuit as well in order to observe their impact on small-signal performance (specifically, the inductor resistance and capacitor resistance).

3.4.1 CCM: Ideal Transfer Function

By taking the CCM small-signal model for the PWM Switch derived earlier and placing it into the boost converter circuit, Figure 3.10 can be created. This circuit is now a linear small-signal model which can be analyzed to find any given transfer function (control-to-output, input-to-output, etc). Since the control-to-output, $\frac{\hat{v_o}}{\hat{d}}$, is the transfer function of concern here, the small-signal source v_i is set to 0.

In order to simplify analysis, the circuit shown in Figure 3.10 can be modified, as explained in [21]. This simplification involves moving the voltage source and current source to the *other* side of the transformer and connecting the capacitor and load resistance to the common, as opposed to passive, terminal. The resultant circuit is shown in Figure 3.11.

From here, nodal analysis can be used to derive the proper transfer function. First, observe that $\hat{v_p} = \hat{v_o}$. Since $\hat{v_{cp}} = D\hat{v_{ap}}$, due to the transformer's $1 : D$ turns ratio, the value for $\hat{v_c}$ can be derived as follows:

$$\hat{v_c} - \hat{v_o} = -D\hat{v_o}$$

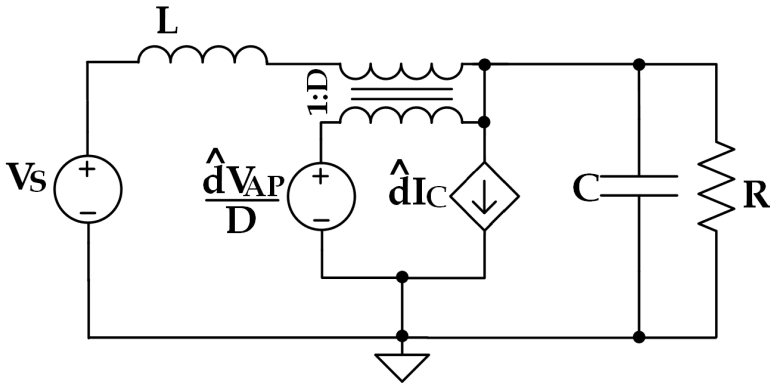

Figure 3.10: Equivalent Small-Signal Boost Circuit in CCM

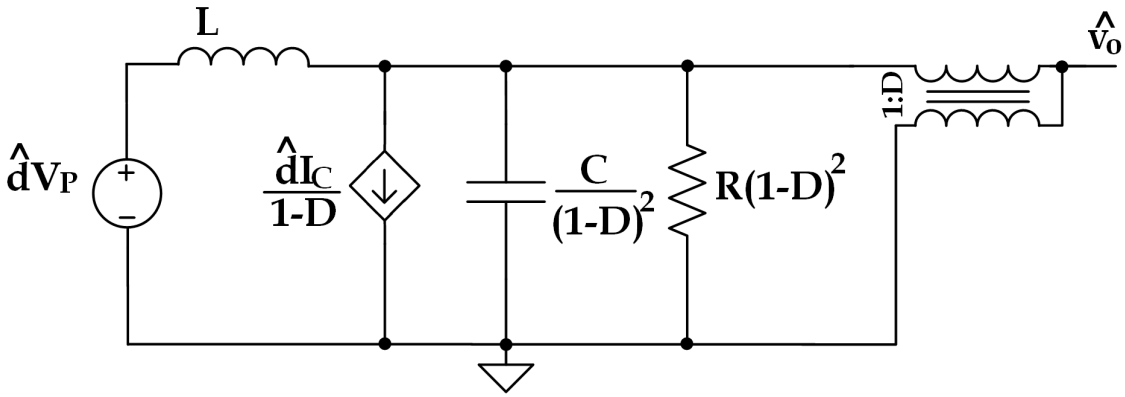

Figure 3.11: Equivalent Small-Signal Boost Circuit in CCM After Transformation Given in [21]

$$\hat{v_c} = \hat{v_o}(1-D) \tag{3.42}$$

Using nodal analysis, and plugging V_O in for V_P and plugging $\frac{V_O}{R(1-D)}$ in for I_C results in the following expression,

$$\frac{-V_O}{R(1-D)^2}\hat{d} = \frac{\hat{v_c} - V_O\hat{d}}{sL} + \frac{sC\hat{v_c}}{(1-D)^2} + \frac{\hat{v_c}}{R(1-D)^2}$$

$$\frac{-V_O}{R(1-D)^2}\hat{d} = \frac{(1-D)}{sL}\hat{v_o} - \frac{V_O}{sL}\hat{d} + \frac{sC}{1-D}\hat{v_o} + \frac{1}{R(1-D)}\hat{v_o}$$

After rearranging and finding a common denominator, the following expression emerges,

$$\hat{v_o}\left[\frac{s^2RLC + sL + R(1-D)^2}{sLR(1-D)}\right] = \hat{d}V_O\left[\frac{R(1-D)^2 - sL}{sLR(1-D)^2}\right]$$

thus, $\frac{\hat{v_o}}{\hat{d}}$ is given as:

$$\frac{\hat{v_o}}{\hat{d}} = \frac{V_O}{1-D}\left[\frac{-sL + R(1-D)^2}{s^2RLC + sL + R(1-D)^2}\right] \checkmark$$

which verifies the answer found in (3.14).

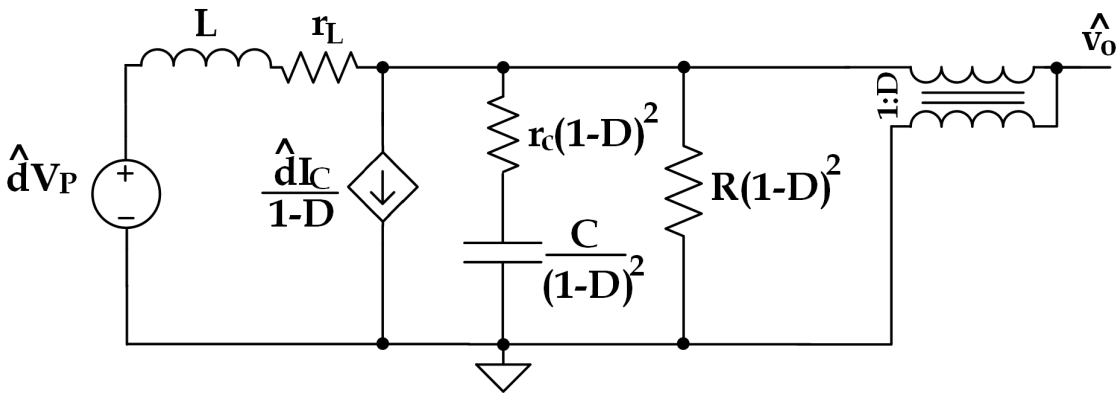

Figure 3.12: Equivalent Small-Signal Boost Circuit in CCM with Non-Idealities Included

3.4.2 CCM: Non-Ideal Transfer Function

By adding in the non-ideal inductor and capacitor series resistances, as shown in Figure 3.12, a more accurate (and, unfortunately, more complex) transfer function can be derived. The same process used in the ideal derivation will be used here. Since $\hat{v_c} = \hat{v_o}(1-D)$ from the previous derivation, it's clear that:

$$-\frac{V_O}{R(1-D)^2}\hat{d} = \frac{(1-D)\hat{v_o} - V_O\hat{d}}{sL+r_L} + \frac{sC}{(sr_CC+1)(1-D)}\hat{v_o} + \frac{1}{R(1-D)}\hat{v_o}$$

Rearranging the above equation so that the $\hat{v_o}$ and $\hat{d}$ terms are separated and above common denominators yields:

$$\hat{v_o}\left[\frac{R(sr_CC+1)(1-D)^2 + s^2RLC + sRr_LC + (sL+r_L)(sr_CC+1)}{R(sL+r_L)(sr_CC+1)(1-D)}\right]\cdots$$
$$\cdots = \hat{d}V_O\left[\frac{R(1-D)^2 - (sL+r_L)}{R(sL+r_L)(1-D)^2}\right]$$

After solving for $\frac{\hat{v_o}}{\hat{d}}$ and expanding the terms in both the numerator and denominator, the small-signal non-ideal transfer function for a boost converter in CCM was found as shown in (3.43).

$$\frac{\hat{v_o}}{\hat{d}} = \frac{V_O}{1-D}\left[\frac{-s^2\frac{r_C}{R}L + s(r_C(1-D)^2 - \frac{L}{RC} - \frac{r_Cr_L}{R}) - \frac{r_L}{RC} + \frac{1}{C}(1-D)^2}{s^2L(\frac{r_C}{R}+1) + s[r_C(1-D)^2 + r_L + \frac{r_Cr_L}{R} + \frac{L}{RC}] + \frac{r_L}{RC} + \frac{(1-D)^2}{C}}\right] \tag{3.43}$$

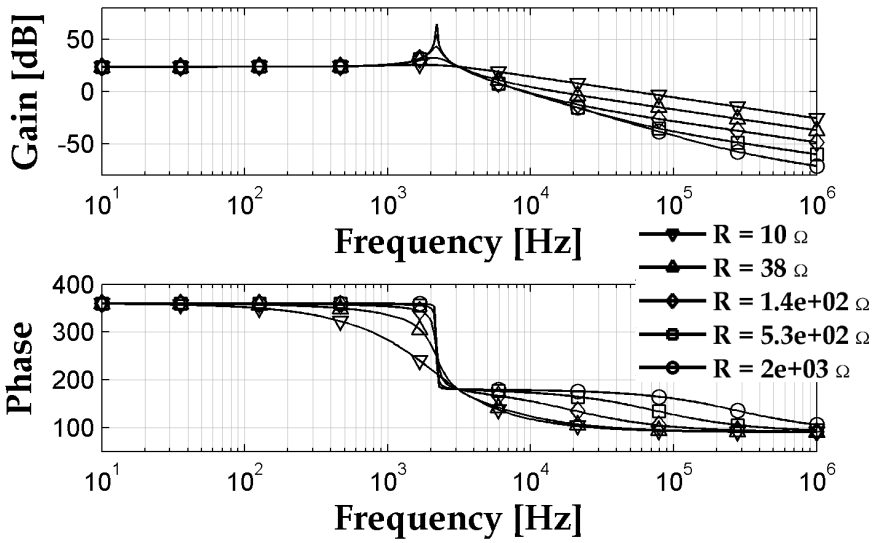

Figure 3.13: Bode Plot for Ideal Boost in CCM with $L = 180\,\mu H$, $C = 4.7\,\mu F$, $F_S = 350\,kHz$, and $\frac{V_O}{V_S} = 2.5$.

Alternatively, the transfer function can be expressed in the more general form given in (3.15) with:

$$G_{d0} = \frac{V_O}{1-D}\frac{R(1-D)^2 - r_L}{R(1-D)^2 + r_L} \tag{3.44}$$

$$\omega_{z,1} = \frac{R(1-D)^2 - r_L}{L} \tag{3.45}$$

$$\omega_{z,2} = \frac{1}{r_C C} \tag{3.46}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}\sqrt{\frac{R(1-D)^2 + r_L}{R + r_C}} \tag{3.47}$$

$$Q = \sqrt{LC}\frac{\sqrt{(R+r_C)(R(1-D)^2 + r_L)}}{Rr_C C(1-D)^2 + Rr_L C + r_C r_L C + L} \tag{3.48}$$

Ideal and Non-Ideal Comparisons

Figure 3.13 shows the Bode plot for the ideal transfer function given in (3.14). Figure 3.14 shows the Bode plot for the non-ideal transfer function given in (3.43). The parameters used were: $L = 180\,\mu H$, $C = 4.7\,\mu F$, $F_S = 350\,kHz$, $\frac{V_O}{V_S} = 2.5$, $r_L = 0.8\,\Omega$, and $r_C = 0.1\,\Omega$.

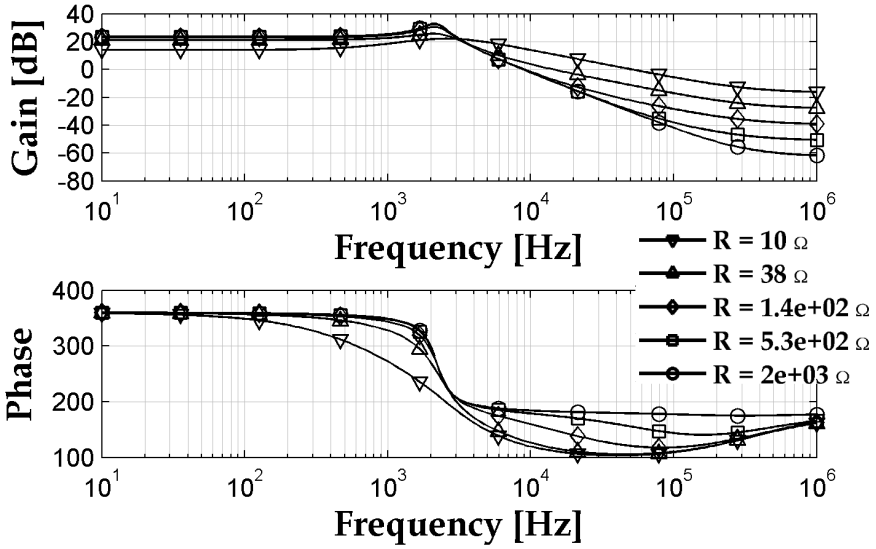

Figure 3.14: Bode Plot for Non-Ideal Boost in CCM with $L = 180\,\mu H$, $C = 4.7\,\mu F$, $F_S = 350\,kHz$, $\frac{V_O}{V_S} = 2.5$, $r_L = 0.8\,\Omega$, and $r_C = 0.1\,\Omega$.

A notable feature of Figure 3.13 is the resonant peak that occurs for large load resistances. The explanation for this is rather simple: as the load resistance increases, the load current must decrease. Since the diode is reverse-biased during the interval when the switch is closed, the load current must be supplied by the capacitor. Since load current is small, the RC time constant is large indicating that it will take a large amount of time for the capacitor to fully discharge. Since this is the case, there is a large amount of energy still stored in the capacitor at the time where the switch opens. This, along with the energy stored in the inductor, causes resonance if the switch is modulated at an appropriate frequency. The location of this peak can easily be predicted by (3.19) and is $2.2\,kHz$ for the ideal transfer. In the non-ideal case, the peak exhibits a slight decrease in frequency due to the series resistances of the inductor and capacitor as shown in (3.47).

Figures 3.15 and 3.16 depict the step responses for the ideal and non-ideal CCM converters, respectively. As predicted by the Bode plot comparison, the non-ideal converter is noticeably more stable. Likewise, stability begins to increase with an increase in load current.

From a transient perspective, it's clear that the loss mechanisms in the circuit contribute to a decrease in the steady-state value of the converter. This is expected

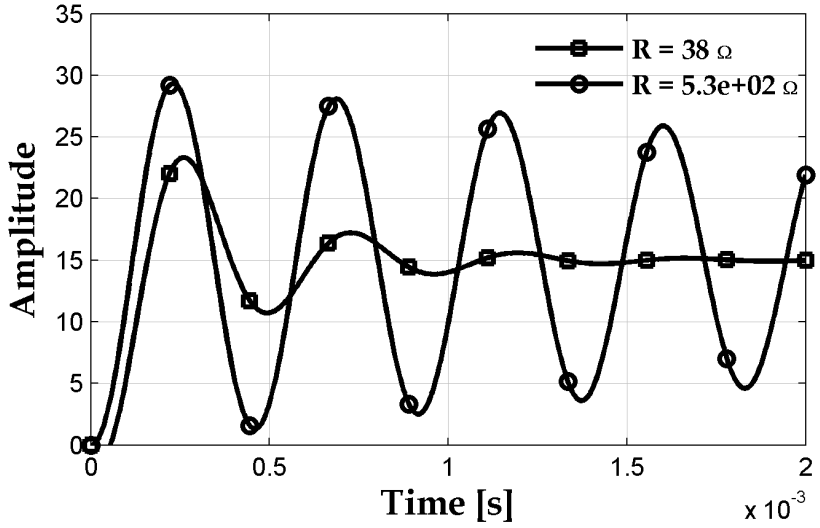

Figure 3.15: Step Response for Ideal Boost in CCM with $L = 180\,\mu H$, $C = 4.7\,\mu F$, $F_S = 350\,kHz$, and $\frac{V_O}{V_S} = 2.5$.

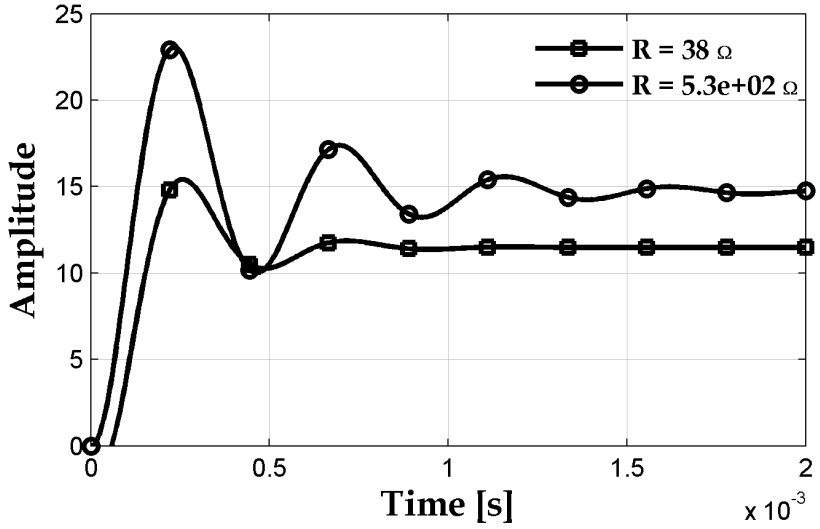

Figure 3.16: Step Response for Non-Ideal Boost in CCM with $L = 180\,\mu H$, $C = 4.7\,\mu F$, $F_S = 350\,kHz$, $\frac{V_O}{V_S} = 2.5$, $r_L = 0.8\,\Omega$, and $r_C = 0.1\,\Omega$.

from the equations derived in Chapter 2 that showed that the ideal CCM converter has no load dependence in (2.3), while the non-ideal CCM converter *does* in (2.10). This indicates that a controller used to try and maintain a fixed DC voltage for varying loads not only has to compete with the inherent instability of the converter (thanks to the conjugate pair pole in the system), but also needs to provide enough

gain in order to maintain a regulated output.

3.4.3 DCM: Ideal Transfer Function

Using the circuit derived in Figure 3.9 and placing it into the boost converter model results in the circuit shown in Figure 3.17.

In order to derive the control-to-output transfer function (ignoring all parasitics), the small-signal source $\hat{v_i}$ needs to be set to zero. Doing so allows for the following equation to be developed using KCL at the control node:

$$0 = \frac{v_{ac}}{sL} + v_{ac}g_i + k_i\hat{d} + g_f v_{ac} - v_{cp}g_o + k_o\hat{d}$$

Since $v_a = 0$ and $v_p = \hat{v_o}$, with some rearranging of terms, the following expression for v_c can be generated:

$$v_c = \frac{\hat{v_o}sLg_o + \hat{d}[sL(k_i + k_o)]}{sL(g_i + g_f + g_o) + 1} \tag{3.49}$$

Next, it is necessary to develop an expression using KCL at the output node:

$$0 = v_{cp}g_o - g_f v_{ac} - k_o\hat{d} - v_o sC - \frac{v_o}{R}$$

Again, with some rearranging and by substituting $v_a = 0$ and $v_p = \hat{v_o}$, another

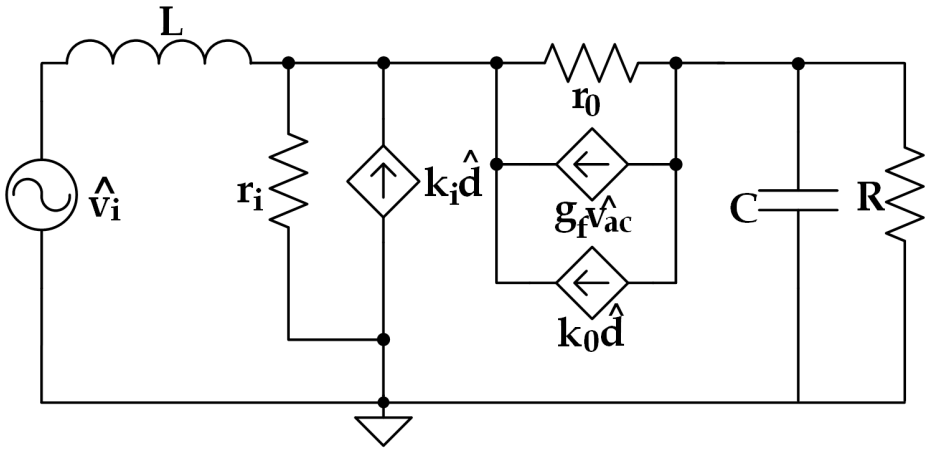

Figure 3.17: Equivalent Small-Signal Boost Circuit in DCM

expression for v_c can be generated:

$$v_c = \frac{\hat{v_o}[sC + \frac{1}{R} + g_o] + k_o\hat{d}}{g_o + g_f} \tag{3.50}$$

In order to obtain an expression for the transfer function $\frac{\hat{v_o}}{\hat{d}}$, (3.49) must be set equal to (3.50):

$$\hat{v_o}\frac{sC + \frac{1}{R} + g_o}{g_o + g_f} + \hat{d}\frac{k_o}{g_o + g_f} = \hat{v_o}\frac{sLg_o}{sL(g_i + g_f + g_o) + 1} + \hat{d}\frac{sL(k_i + k_o)}{sL(g_i + g_f + g_o) + 1}$$

$$\hat{v_o}\left[\frac{sRC + Rg_o + 1}{R(g_o + g_f)} - \frac{sLg_o}{sL(g_i + g_o + g_f) + 1}\right] = \cdots$$
$$\cdots \hat{d}\left[\frac{sLk_i + sLk_o}{sL(g_i + g_o + g_f) + 1} - \frac{k_o}{g_o + g_f}\right]$$

$$\hat{v_o}\left[\frac{(sRC + g_oR + 1)(sL[g_i + g_f + g_o] + 1) - sLRg_o(g_o + g_f)}{R(g_o + g_f)(sL[g_i + g_f + g_o] + 1)}\right] = \cdots$$
$$\cdots \hat{d}\left[\frac{sL(k_i + k_o)(g_o + g_f) - sLk_o(g_i + g_o + g_f) - k_o}{(g_o + g_f)(sL[g_i + g_o + g_f] + 1)}\right]$$

Therefore, the small-signal control-to-output transfer function is:

$$\frac{\hat{v_o}}{d} = \frac{sLR[k_i(g_f + g_o) - k_og_i] - k_oR}{s^2LRC[g_i + g_o + g_f] + s[RC + L(g_i + g_o + g_f) + LRg_og_i] + g_oR + 1} \tag{3.51}$$

Equation (3.51) verifies the findings reported in [20] by Reatti and Kazimierczuk for the boost-converter control-to-output transfer function.

For a proper comparison, this transfer function can be manipulated in order to fit the general form of (3.15). First, recall the definitions for g_i, k_i, k_0, g_0, and g_f given in (3.35), (3.36), (3.38), (3.39), and (3.40), respectively. By analyzing these parameters and plugging in for known circuit quantities, the expressions can be manipulated as shown in (3.52)-(3.56) where $M = \frac{V_O}{V_S}$ and $\tau_L = \frac{LF_S}{R}$:

$$g_i = \frac{I_A}{V_{AC}} = \frac{\frac{D}{D_1}\frac{V_O}{R}}{D_1V_O} = \frac{D}{R}\left(\frac{D}{2\tau_LM}\right)^2 \tag{3.52}$$

$$g_0 = \frac{I_P}{V_{CP}} = \frac{\frac{V_O}{R}}{DV_O} = \frac{1}{RD} \tag{3.53}$$

$$g_f = \frac{2I_P}{V_{AC}} = \frac{2\frac{V_O}{R}}{D_1 V_O} = \frac{D}{R}\frac{1}{M\tau_L} \tag{3.54}$$

$$k_i = \frac{2I_A}{D} = -\frac{2\frac{V_O}{R}}{D_1} = -\frac{D}{R}\frac{V_O}{M\tau_L} \tag{3.55}$$

$$k_o = \frac{2I_P}{D} = -\frac{2\frac{V_O}{R}}{D} = -\frac{2V_O}{RD} \tag{3.56}$$

After plugging the above equations into (3.51) and some algebraic manipulation, the following parameters were extracted for the general transfer function in (3.15).

$$G_{d0} = \frac{2V_O}{1+D} \tag{3.57}$$

$$\omega_{z,1} = -\frac{2(M\tau_L)^2}{D^2\frac{L}{R}\left(\frac{D}{2} + \frac{M\tau_L}{D}\right)} \tag{3.58}$$

$$\omega_{z,2} = \infty \tag{3.59}$$

$$\omega_0 = \frac{2M\tau_L}{\sqrt{LC}}\sqrt{\frac{1+D}{D^4 + 4D^2M\tau_L + 4M^2\tau_L^2}} \tag{3.60}$$

$$Q = \frac{1}{\omega_0}\left[\frac{4(M\tau_L)^2(1+D)}{4RCDM^2\tau_L^2 + \frac{L}{R}(D^4 + 4D^2M\tau_L + 4M^2\tau_L^2) + \frac{L}{R}D^3}\right] \tag{3.61}$$

3.4.4 DCM: Non-Ideal Transfer Function

Using Figure 3.18, the non-ideal DCM small-signal transfer function can be derived. The process follows the same structure as the ideal derivation where nodal analysis was utilized.

First, observe the currents at the $\hat{v_c}$ node. Using KCL, the following expression

can be created:

$$0 = \frac{\hat{v_c}}{sL + r_L} + \hat{v_c} g_i - k_i \hat{d} + \hat{v_{cp}} g_0 + g_f \hat{v_c} - k_0 \hat{d}$$

Such that:

$$\hat{v_c} = \frac{\hat{v_o} g_0 (sL + r_L) + \hat{d}(k_i + k_0)(sL + r_L)}{(sL + r_L)(g_i + g_0 + g_f) + 1} \tag{3.62}$$

Moving to the output of the converter and, again, utilizing KCL gives the following expression:

$$0 = \hat{v_{pc}} g_0 + g_f \hat{v_{ac}} + k_0 \hat{d} + \frac{\hat{v_o} sC}{sr_C C + 1} + \frac{\hat{v_o}}{R}$$

After rearranging terms and plugging (3.62) in for $\hat{v_c}$ yields:

$$\hat{v_o} \left[\frac{s(RCr_C g_0 + RC + Cr_C) + Rg_0 + 1}{sRCr_C + R} - \frac{g_0 (sL + r_L)(g_f + g_0)}{(sL + r_L)(g_i + g_f + g_0) + 1} \right] = \cdots$$
$$\cdots \hat{d} \left[\frac{(g_f + g_0)(k_i + k_0)(sL + r_L) - k_0 (sL + r_L)(g_i + g_f + g_0) - k_0}{(sL + r_L)(g_i + g_f + g_0) + 1} \right]$$

Clearly, the resulting equation will be very long. Thus, in order to condense the transfer function, the form of (3.63) is used where each parameter is given in (3.64) through (3.69):

$$T(s) = \frac{a_2 s^2 + a_1 s + a_0}{b_2 s^2 + b_1 s + b_0} \tag{3.63}$$

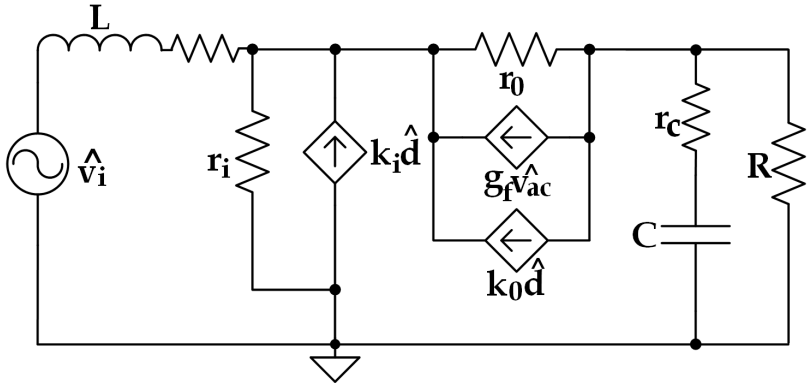

Figure 3.18: Equivalent Small-Signal Non-Ideal Boost Circuit in DCM

$$a_2 = LRCr_C[(g_f + g_0)k_i - k_0 g_i] \tag{3.64}$$

$$a_1 = RCr_C[r_L(g_f + g_0)k_i - r_L k_0 g_i - k_0] \cdots$$
$$\cdots + LR[(g_f + g_0)k_i - k_0 g_i] \tag{3.65}$$

$$a_0 = Rr_L[(g_f + g_0)k_i - k_0 g_i] - Rk_0 \tag{3.66}$$

$$b_2 = LRCr_C g_i g_0 + LC(R + r_C)(g_i + g_0 + g_f) \tag{3.67}$$

$$b_1 = LRg_0 g_i + L(g_i + g_0 + g_f) + RCr_C(r_L g_i + 1) \cdots$$
$$\cdots + (RC + r_C C)[r_L(g_i + g_0 + g_f) + 1] \tag{3.68}$$

$$b_0 = r_L(g_i + g_0 + g_f) + g_0 g_i R r_L + Rg_0 + 1 \tag{3.69}$$

These values verify the findings in [20]. Of course, to better compare to the previous functions, it's important to fit these values to the general equation given in (3.15). Obtaining ω_0 and Q are straight forward, but obtaining the zeros of the transfer function are not quite as simple. The best approach is to place the numerator into an A matrix and solve for the eigenvalues. The A matrix has a structure of:

$$A = \frac{1}{a_0}\begin{bmatrix} -a_1 & -a_2 \\ a_0 & 0 \end{bmatrix}$$

By plugging (3.64)-(3.66) into the A matrix and solving for the eigenvalues, λ_i, the zeros of the function can be extrapolated as:

$$\omega_{z,1} = \frac{1}{\lambda_1} \quad \text{and} \quad \omega_{z,2} = \frac{1}{\lambda_2}$$

After performing the aforementioned operations, the general-structure parameters were found to be:

$$G_{d0} = \frac{\frac{2V_O}{D} + Rr_L\left(\frac{D^2 V_O}{2(M\tau_L)^2 R^2} - \frac{V_O}{R} - \frac{D^2 V_O}{RM\tau_L}\right)}{r_L\left(\frac{1}{DR} + \frac{D^3}{4(M\tau_L)^2 R} + \frac{D}{M\tau_L R}\right) + \frac{1}{D} + \frac{D^2 r_L}{4(M\tau_L)^2 R} + 1} \tag{3.70}$$

$$\omega_{z,1} = -\frac{r_L D^3 + 2r_L DM\tau_L - 4R(M\tau_L)^2}{LD^3 + 2M\tau_L LD} \tag{3.71}$$

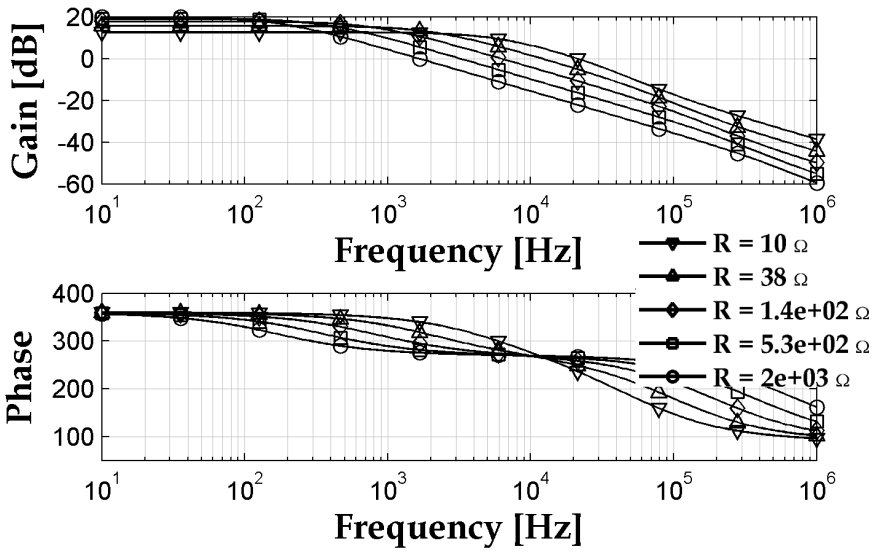

Figure 3.19: Bode Plot for Ideal Boost in DCM with $L = 18\,\mu H$, $C = 4.7\,\mu F$, $F_S = 350\,kHz$, and $\frac{V_O}{V_S} = 1.6$.

$$\omega_{z,2} = \frac{1}{r_C C} \tag{3.72}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}\sqrt{\frac{(1+D)(r_L D^3 + 4R(M\tau_L)^2) + 4M\tau_L r_L(D^2 + M\tau_L)}{D^3 r_C + (R + r_C)(D^4 + 4D^2 M\tau_L + 4(M\tau_L)^2)}} \tag{3.73}$$

$$Q = \frac{r_L[D^2(D^2 + 4M\tau_L) + 4(M\tau_L)^2 + D^3] + 4R(M\tau_L)^2(1+D)}{\omega_0 Q_d} \tag{3.74}$$

$$\begin{aligned} Q_d = {} & L(D^4 + D^3 + 4M\tau_L D^2 + 4(M\tau_L)^2) + r_C C(r_L D^3 + 4R(M\tau_L)^2) \cdots \\ & \cdots + (RC + rc_C)[r_L(D^4 + 4M\tau_L D^2 + 4(M\tau_L)^2) + 4DR(M\tau_L)^2] \end{aligned} \tag{3.75}$$

Ideal and Non-Ideal Comparisons

A comparison of the Bode plots for the ideal and non-ideal DCM transfer functions is shown in Figure 3.19 and Figure 3.20, respectively. The parameters used were: $L = 18\,\mu H$, $C = 4.7\,\mu F$, $F_S = 350\,kHz$, $\frac{V_O}{V_S} = 1.6$, $r_L = 0.8\,\Omega$, and $r_C = 0.1\,\Omega$.

Besides the noticeable effects due to the additional zero given in (3.72) which, ultimately, has little effect on the overall converter performance, there is a noticeable decrease in open-loop gain as the current increases. Once the load resistance drops below a certain range, $0.72\,\Omega$ for the parameters listed above, the open-loop gain dips below $0\,dB$ which renders the converter essentially inoperable (without external

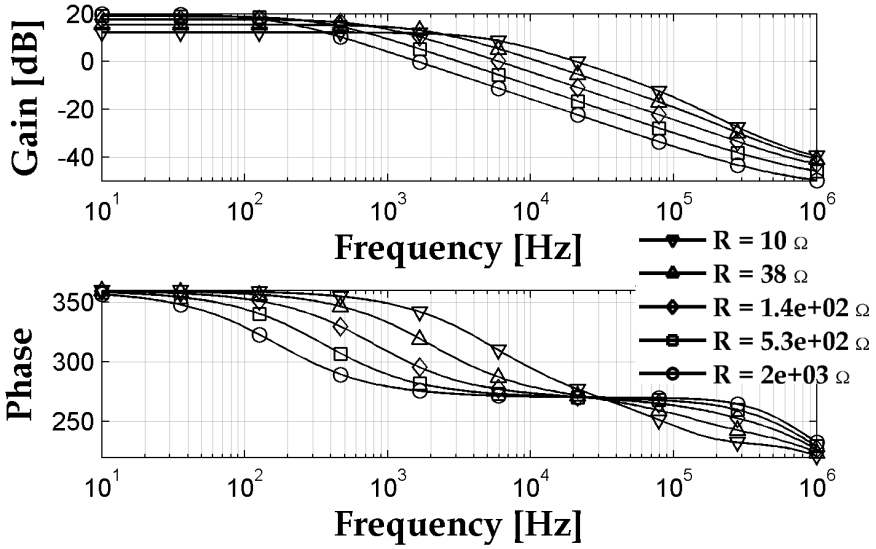

Figure 3.20: Bode Plot for Non-Ideal Boost in DCM with $L = 18\,\mu H$, $C = 4.7\,\mu F$, $F_S = 350\,kHz$, $\frac{V_O}{V_S} = 1.6$, $r_L = 0.8\,\Omega$, and $r_C = 0.1\,\Omega$.

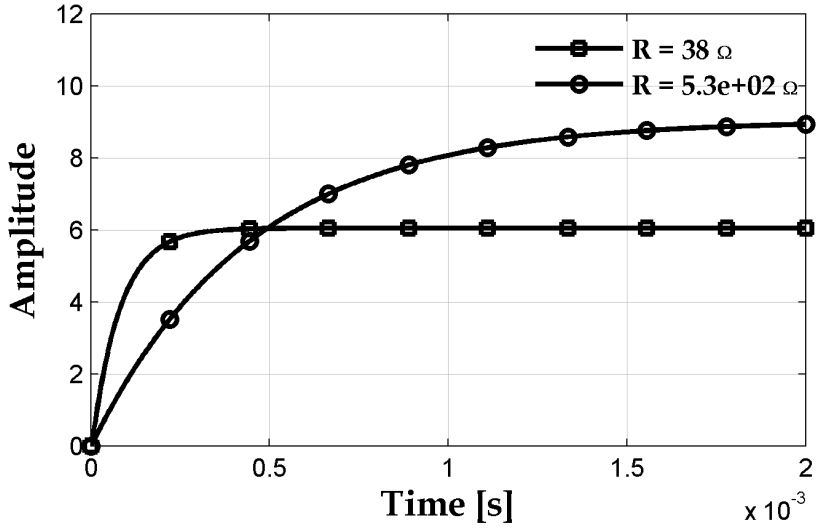

Figure 3.21: Step Response for Ideal Boost in DCM with $L = 18\,\mu H$, $C = 4.7\,\mu F$, $F_S = 350\,kHz$, and $\frac{V_O}{V_S} = 1.6$.

control, that is).

Figures 3.21 and 3.22 show the step response for the ideal and non-ideal DCM transfer functions, respectively. Here, two different loads were used, as indicated on each figure, in order to see the transient behavior as a function of the load. The steady-state behavior is a function of the load, as predicted in the DC voltage gain function

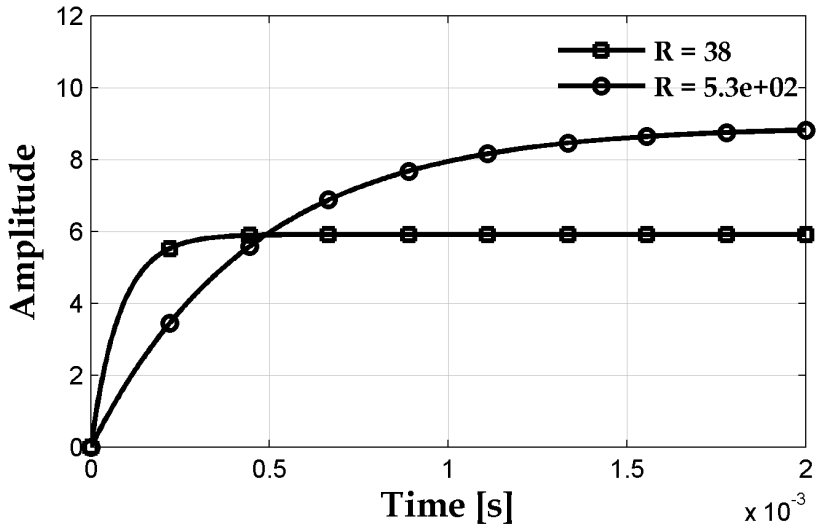

Figure 3.22: Step Response for Non-Ideal Boost in DCM with $L = 18\,\mu H$, $C = 4.7\,\mu F$, $F_S = 350\,kHz$, $\frac{V_O}{V_S} = 1.6$, $r_L = 0.8\,\Omega$, and $r_C = 0.1\,\Omega$.

in (2.22) in Chapter 2. This is a primary reason why feedback control is incredibly important as the duty cycle (the only controllable parameter in the circuit) must be modulated in order to maintain a given steady-state DC voltage for varying loads. As shown previously, this is not the case for CCM; however, the two-pole behavior of the system requires control in order to move the $0\,dB$ crossing point such that the converter is stable in all required operating conditions.

Another observation of these two step responses is that they look identical. This indicates that the ideal and non-ideal transfer function may be approximately equal which, in turn, also implies that the loss mechanisms present in the circuit have a negligible effect on transient and small-signal performance. This will be discussed more thoroughly throughout the next section.

3.5 Transfer Function Comparison

It's difficult to compare the transfer functions for CCM and DCM since both are defined by different operating regions. A function valid in DCM, by definition, cannot be valid in CCM. Various parameters have to be carefully selected to guarantee that the converter is operating in a desired region. This is why the CCM and DCM

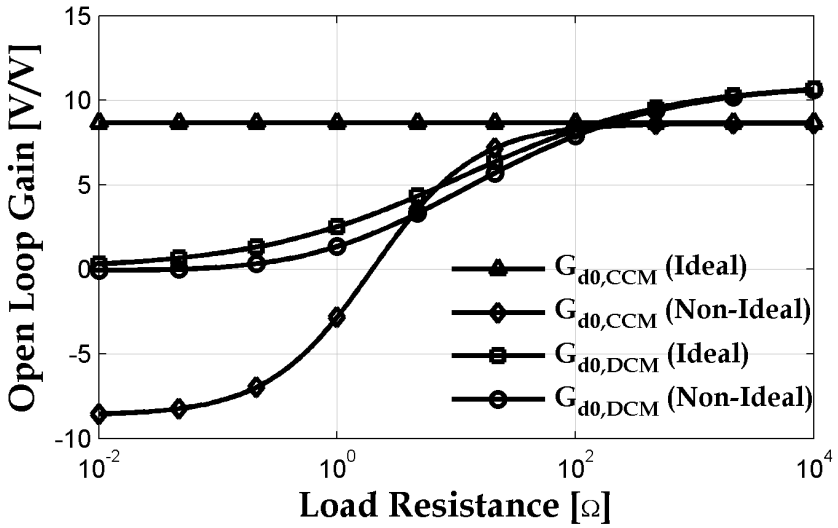

Figure 3.23: Open-Loop Gain Comparison for Varying Load Resistances with $L = 18\,\mu H$, $C = 4.7\,\mu F$, $F_S = 350\,kHz$, and $M = 1.6$.

converters were generated with different parameters.

To alleviate this problem, it's possible to observe the individual transfer function parameters as a point of comparison (referencing the general transfer function equation given in (3.15)). Table 3.1 shows a comparison of the Open-Loop Gain expressions for each transfer function while Figure 3.23 shows a comparison of the open-loop gain values for varying load resistance. Here, the only parameter being modified to achieve the correct region of operation is the duty cycle, D.

A very interesting feature of Figure 3.23 is that the open-loop gain for the converter in DCM is very similar in both the ideal and non-ideal case across a large range of load

Table 3.1: Comparison of Transfer Function Open Loop Gain Equations

	G_{d0}
CCM (Ideal)	$\frac{V_O}{1-D}$
DCM (Ideal)	$\frac{2V_O}{1+D}$
CCM (Non-Ideal)	$\frac{V_O}{1-D}\frac{R(1-D)^2-r_L}{R(1-D)^2+r_L}$
DCM (Non-Ideal)	$\frac{\frac{2V_O}{D}+Rr_L\left(\frac{D^2V_O}{2(M\tau_L)^2R^2}-\frac{V_O}{R}-\frac{D^2V_O}{RM\tau_L}\right)}{r_L\left(\frac{1}{DR}+\frac{D^3}{4(M\tau_L)^2R}+\frac{D}{M\tau_L R}\right)+\frac{1}{D}+\frac{D^2r_L}{4(M\tau_L)^2R}+1}$

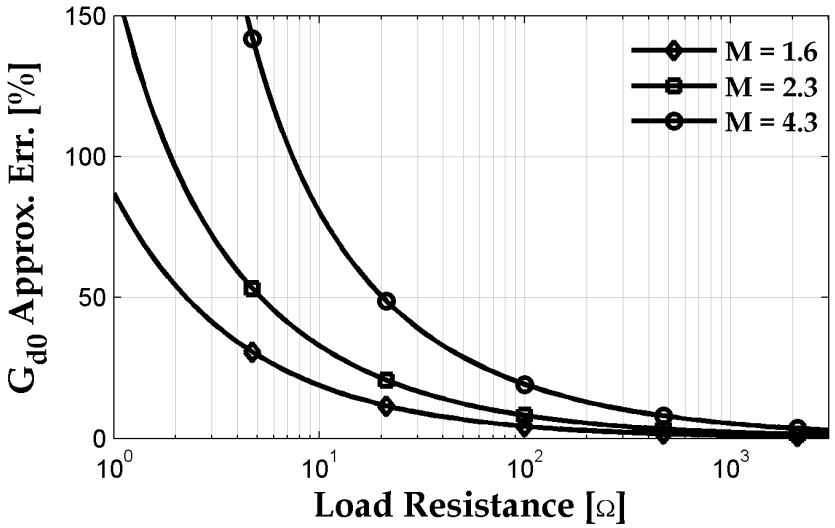

Figure 3.24: Open-Loop Gain DCM Approximation Error

resistances. This differs from the ideal and non-ideal curves for the CCM region of operation in that the gain clearly begins to diverge at large output currents. Luckily, the expression for the non-ideal CCM open-loop gain given in (3.44) is not very complex when compared to the non-ideal DCM expression in (3.70). Because of the complexity of the DCM expression, it is very attractive to try and approximate the non-ideal gain to the ideal gain given in (3.57). Figure 3.24 shows the percent error in doing so.

Approximating $G_{d0,nonideal}$ to be $\approx \frac{2V_O}{1+D}$ is perfectly valid for a small load currents. However, the definition for a "small load current" varies on the DC gain of $M = \frac{V_O}{V_S}$: as Figure 3.24 clearly shows, an increasing DC gain causes the error to increase at smaller load current (presented here as larger load resistances). That said, given that operation in DCM is typically dictated by small load currents, this approximation will hold true in most applications; however, it is always wise to verify that the approximation will hold based on the application.

Table 3.2 shows the equations for ω_0 for each transfer function while Figure 3.25 compares them graphically with a varying load resistance. Similar to the open-loop gain comparison plot (Figure 3.23), the ideal and non-ideal DCM ω_0 curves exhibit almost identical behavior for large load resistances. Due to the complexity of the non-ideal expression in (3.73), it would be very beneficial to be able to approximate

Table 3.2: Comparison of Transfer Function Resonant Frequency Equations

	ω_0
CCM (Ideal)	$\frac{1-D}{\sqrt{LC}}$
DCM (Ideal)	$\frac{2M\tau_L}{\sqrt{LC}}\sqrt{\frac{1+D}{D^4+4D^2M\tau_L+4M^2\tau_L^2}}$
CCM (Non-Ideal)	$\frac{1}{\sqrt{LC}}\sqrt{\frac{R(1-D)^2+r_L}{R+r_C}}$
DCM (Non-Ideal)	$\frac{1}{\sqrt{LC}}\sqrt{\frac{(1+D)(r_LD^3+4R(M\tau_L)^2)+4M\tau_Lr_L(D^2+M\tau_L)}{D^3r_C+(R+r_C)(D^4+4D^2M\tau_L+4(M\tau_L)^2)}}$

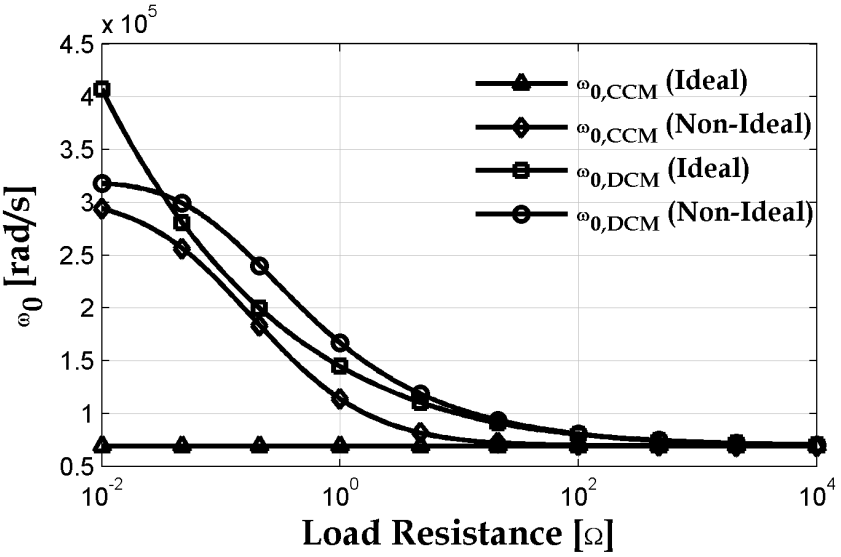

Figure 3.25: Resonant Frequency Comparison for Varying Load Resistances with $L = 18\,\mu H$, $C = 4.7\,\mu F$, $F_S = 350\,kHz$, and $M = 1.6$.

$\omega_{0,nonideal}$ to $\omega_{0,ideal}$. Thus, a graphical comparison is presented in Figure 3.26.

As was observed in the approximation error graph for G_{d0} in Figure 3.24, the approximation holds best for small load currents and small DC conversion ratios. This behavior is also exhibited for the resonant frequency approximation in Figure 3.26.

Next, Table 3.3 compares the expression for the quality factor, Q, for each transfer function while Figure 3.27 graphically compares them for varying load resistances. The Q-factor is an important consideration for the small-signal response since it gives an indication of how stable the system actually is. In canonical second-order systems, the step-response can be plotted just through knowledge of ω_0 and Q alone. When

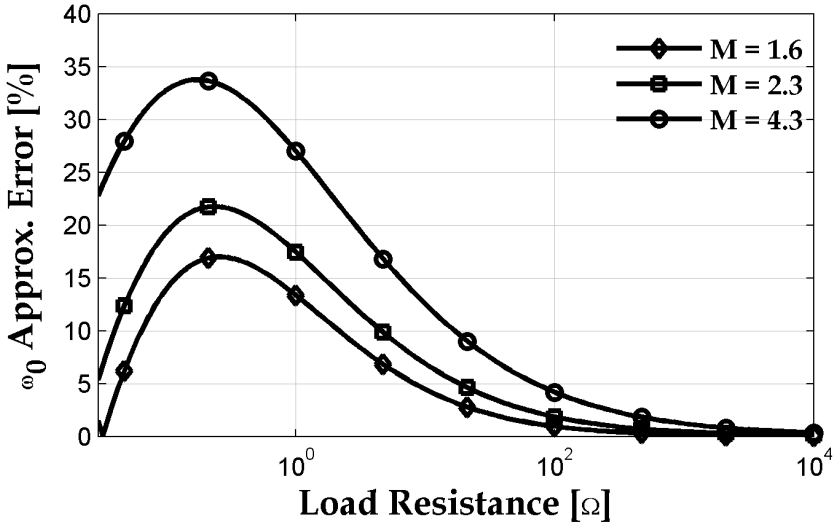

Figure 3.26: Resonant Frequency DCM Approximation Error

$Q > 0.5$, the system is said to be *underdamped* in that oscillations will occur when the system is stepped, but they will die out after a certain interval. Conversely, when $Q < 0.5$, the system is *overdamped* which causes the system to be slow, but no 'ringing' will occur. However, since the boost converter has second order zeros associated with its transfer function, the step-response cannot be extracted as easily (although the underlying canonical second-order effects are still observable). Despite the added complexity due to the presence of $\omega_{z,1}$ and $\omega_{z,2}$, the general trend is still the same for Q in that aiming for a value around 0.5 is most ideal (as it has the fastest rise-time and settling-time). Unfortunately, it's incredibly difficult to observe the effects of various parameters on the value of Q due to the complexity (especially for the non-ideal DCM case in (3.74)).

As with the previous parameters of G_{d0} and ω_0, the error introduced by approximating $Q_{nonideal}$ to Q_{ideal} is displayed in Figure 3.28. Again, as with the previous parameters, for small load currents the approximation is valid.

Finally, Table 3.4 compares the expression for the zeros of each transfer function while Figure 3.29 graphically compares them for varying load resistances. Figure 3.30 shows the error in using an approximation of $\omega_{z,1,nonideal} \approx \omega_{z,1,ideal}$. As was the case for all previous parameters, the approximation is valid for small load currents.

The result of comparing each transfer function parameter is that for small load cur-

Table 3.3: Comparison of Transfer Function Quality Factor Equations

	Q
CCM (Ideal)	$R(1-D)\sqrt{\frac{C}{L}}$
DCM (Ideal)	$\frac{1}{\omega_0}\left[\frac{4(M\tau_L)^2(1+D)}{4RCDM^2\tau_L^2+\frac{L}{R}(D^4+4D^2M\tau_L+4M^2\tau_L^2)+\frac{L}{R}D^3}\right]$
CCM (Non-Ideal)	$\sqrt{LC}\frac{\sqrt{(R+r_C)(R(1-D)^2+r_L)}}{Rr_CC(1-D)^2+Rr_LC+r_Cr_LC+L}$
DCM (Non-Ideal)	$\frac{r_L[D^2(D^2+4M\tau_L)+4(M\tau_L)^2+D^3]+4R(M\tau_L)^2(1+D)}{\omega_0 Q_d}$

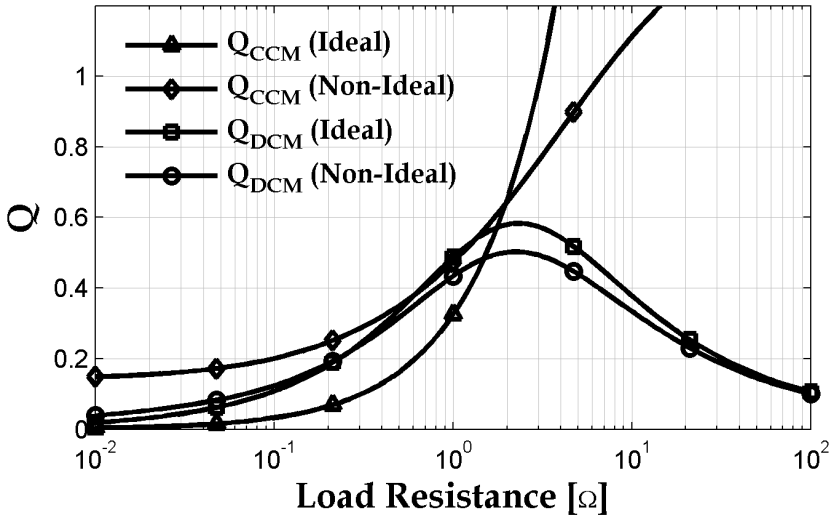

Figure 3.27: Quality Factor Comparison for Varying Load Resistances with $L = 18\,\mu H$, $C = 4.7\,\mu F$, $F_S = 350\,kHz$, and $M = 1.6$.

Table 3.4: Comparison of Transfer Function Zero Frequency Equations

	$\omega_{z,1}$	$\omega_{z,2}$
CCM (Ideal)	$\frac{R(1-D)^2}{L}$	∞
DCM (Ideal)	$-\frac{2(M\tau_L)^2}{D^2\frac{L}{R}\left(\frac{D}{2}+\frac{M\tau_L}{D}\right)}$	∞
CCM (Non-Ideal)	$\frac{R(1-D)^2-r_L}{L}$	$\frac{1}{r_CC}$
DCM (Non-Ideal)	$-\frac{r_LD^3+2r_LDM\tau_L-4R(M\tau_L)^2}{LD^3+2M\tau_LLD}$	$\frac{1}{r_CC}$

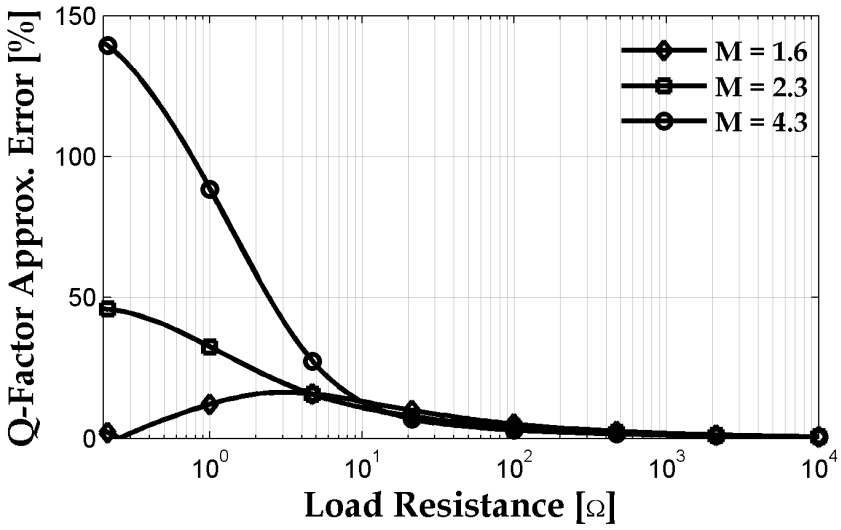

Figure 3.28: Quality Factor DCM Approximation Error

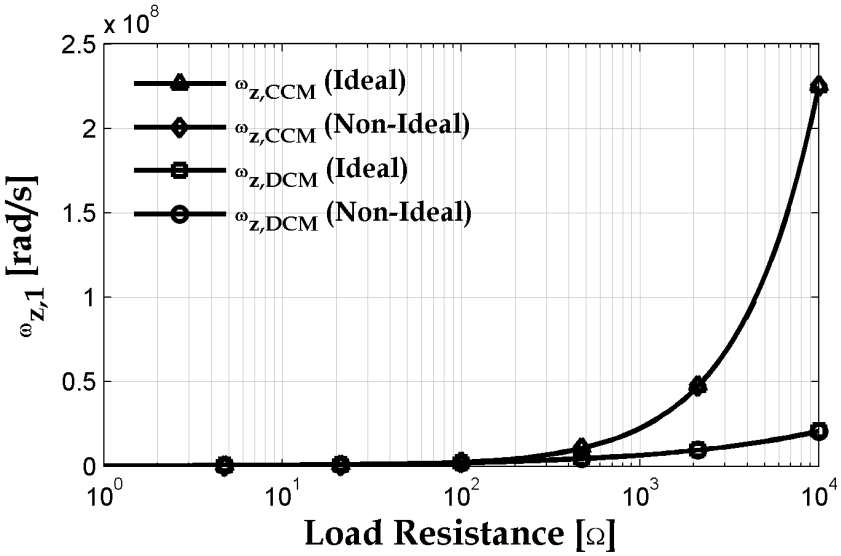

Figure 3.29: RHP Zero Comparison for Varying Load Resistances with $L = 18\,\mu H$, $C = 4.7\,\mu F$, $F_S = 350\,kHz$, and $M = 1.6$.

rents the non-ideal DCM function can be approximated to the ideal transfer function with the only change being $\omega_{z,2} = \frac{1}{r_C C}$ as opposed to ∞. Since DC-DC converters are typically pushed into DCM operation due to small load currents, this approximation will be valid for a wide range of loads, provided the DC conversion ratio is not very large. The area in which the approximation is not valid will occur near the transition

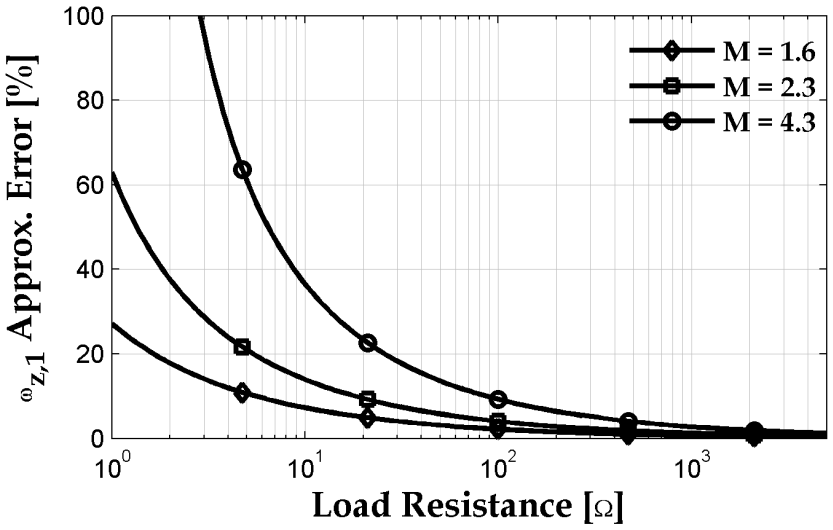

Figure 3.30: RHP Zero DCM Approximation Error

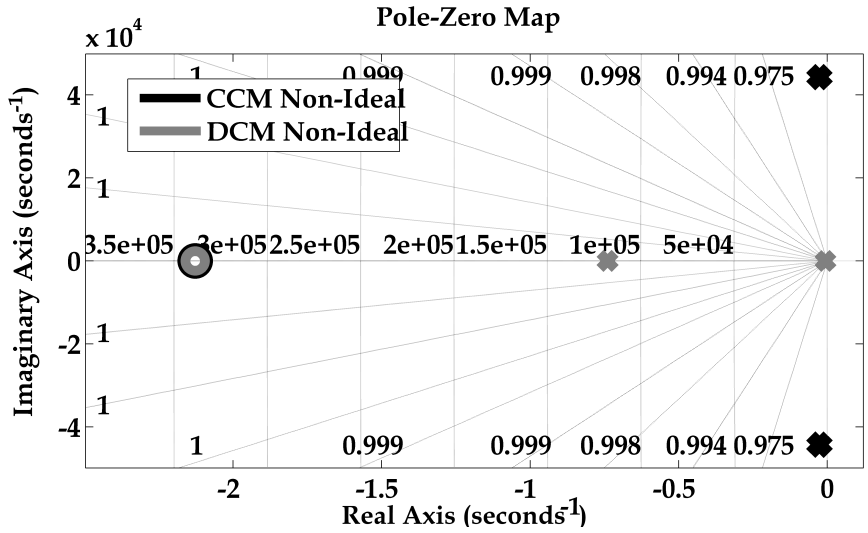

Figure 3.31: Pole Zero plot for Non-Ideal CCM and DCM Transfer Functions (RHPZs Not Plotted)

between CCM and DCM. This result is somewhat similar to the modes of operation in a MOS transistor in that the weak-inversion and strong-inversion equations are rather simple but are invalid in a certain boundary between weak and strong [22]. Here, the transistor equations become far more complex and the transistor is said to be in moderate inversion. Another similarity between the approximations for MOS equations and boost transfer functions is that a MOSFET is typically used deep in

strong-inversion or deep in weak-inversion. DC-DC converters, too, are either operating deep in CCM or deep in DCM since the converter's characteristics undergo significant alterations when transitioning into either operation mode, as previously shown.

The ability to approximate the non-ideal DCM boost converter to that of an ideal one is very powerful, but can be very dangerous if analysis is not done to ensure that the approximation is valid. At low DC conversion ratios, the approximation will be able to hold for a larger range, but even small increases of said conversion ratio can cause massive increases in error which limits the region at which the approximation is valid.

Another important note is the increased controllability by operating a converter in DCM. In Vorpérian's paper on the Average PWM Model in DCM, he mentions that in State-Space Averaging the transfer function for a converter in DCM is found to be a first-order system. However, as was previously found, the system is *clearly* second-order. The reason for the discrepancy, as discussed by Vorpérian, is that the location of the second pole is far from the origin [19].

Figure 3.31 verifies this through observation of the pole/zero locations of both the ideal and non-ideal CCM and DCM transfer functions. Here, the secondary pole in the DCM case is located at a value much greater than that of the first pole. This causes the value for Q to be small, as proven in Figure 3.27, since resonant peaks are a direct effect of conjugate-pair poles. Since the converter in DCM does not have conjugate-pair poles (directly observable in Figure 3.31), it does not have a resonant peak.

The reason this point is important for controllability is that the DCM transfer function *acts* like a first-order system for the given region of interest (frequencies less than that of the switching frequency). This means the phase-margin will be greater than in CCM (since the CCM transfer function clearly exhibits the effects of a second-order system) which, in turn, means that the Error Amplifier in Figure 3.1 doesn't have to contribute a large phase-shift in order to guarantee stability. This is the primary reason DCM is such an attractive region of operation for boost converters.

Chapter 4

Converter Control

The reason control is important for switched DC-DC converters is to maintain a stable output at various load conditions. Recall from the non-ideal DC equations for CCM and DCM in (2.10) and (2.29), respectively, that each equation has a clear dependence on the size of the load. Thus, in order to maintain a fixed voltage output, the duty cycle *must* be modulated in order to supply said fixed voltage to varying loads.

There are two control methods to perform such an operation: Voltage Mode Control (VMC) and Current Mode Control (CMC).

Current Mode Control

Current Mode Control will not be analyzed in this thesis; however, it is a very popular and well-documented technique for controlling switched power converters [25–29]. The topology is shown in Figure 4.1. The control method employs two feedback loops: one for the output voltage and one for the inductor current. The operation is rather simple in that the inductor current is monitored through the switch and when it reaches a certain peak value, the switch is turned off.

The benefits of this type of control method are speed, large bandwidth, and simple compensation requirements [24]. However, the cost is in complexity (due to the existence of two feedback loops), and limited load regulation.

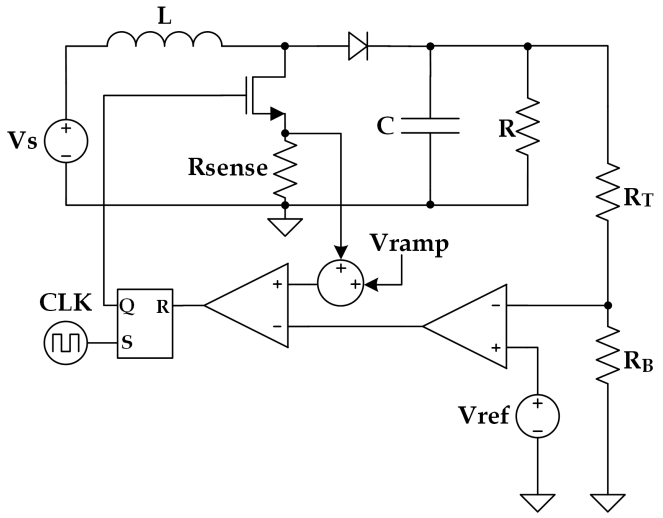

Figure 4.1: Boost Converter with Current Mode Control (Adapted from [29])

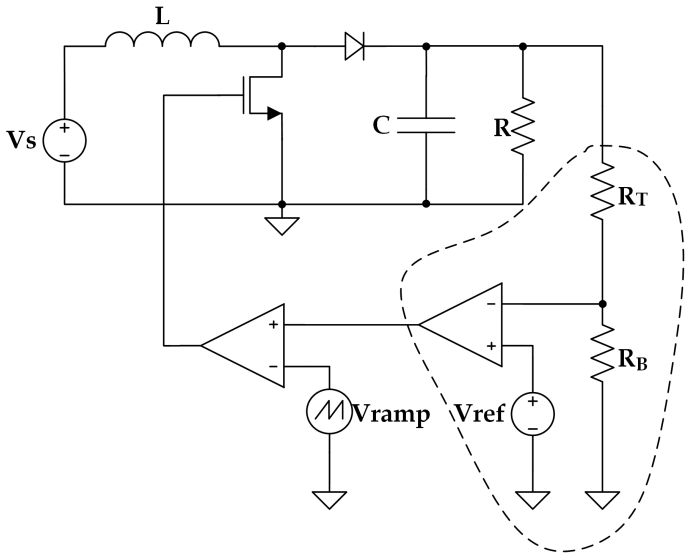

Figure 4.2: Circuit Implementation of a Voltage-Mode Controlled Boost Converter

Voltage Mode Control

Voltage Mode Control can be implemented with the architecture shown in Figure 4.2, and is the architecture that is dealt with throughout this thesis. While the benefits of CMC are certainly tantalizing, the decreased load regulation performance when compared to an equivalent VMC converter is undesirable for applications which need a regulated output for a large range of loads. The downside is that the converter

will be noticeably slower to respond when compared to CMC techniques and that compensation will typically require more components [24].

4.1 Error Amplifiers

The first requirement of an Error Amplifier (in either the VMC or CMC case) is a stable, load-invariant voltage reference that has little to no temperature variation to serve as V_{REF}. These requirements are usually met quite well by implementing a bandgap reference. Since V_{REF} will typically be different than that of V_{OUT}, a resisitive voltage divider is commonly used to divide the desired output voltage down to the value supplied by V_{REF}.

During operation, the error amplifier is attempting to compensate for small variations in the output voltage hence the loop gain must be very large; however, having a large loop gain is not enough. In order to guarantee a stable output (in that the converter does not begin to oscillate), the Barkhausen Stability Criterion states that circuit cannot have any frequency that satisfies both of the following conditions:

1. The magnitude of the Loop Gain, $|A\beta|$, is $= 1$.
2. The shift in phase around the loop has a net change of 180° (noting that the inverting terminal of the amplifier contributes to an additional 180° phase shift around the loop).

The most common way to verify this criterion is to observe the Bode plot of the system, which will be done in the next chapter. However, in the context of this chapter, it's important to understand what will cause Barkhausen's Criterion to hold true and, most importantly, how to ensure that it is satisfied with careful error amplifier selection.

4.1.1 Op-Amps vs. OTAs

In most switched converter designs, Op-Amps are employed as the Error Amplifier due to their availability as "off-the-shelf" parts. The different architectures associated with them are very well documented [21,23]; however, while not ill-suited for the job, Op-Amps are certainly unnecessary. Consider what the error amplifier is driving: an

input pin of a Comparator. Since a comparator will have high input impedance, it is completely unnecessary to drive it from a low-impedance source (in this case, the Op-Amp).

For integrated circuits, utilizing an Op-Amp instead of an OTA is a very ill-advised design choice. The result is an increase in required circuitry as well as a decrease in response time due to the output voltage buffer. A further benefit to using OTAs is that the gain of the amplifier can be easily set by varying the value of a resistive load. In fact, for control circuitry built on ICs, OTAs are overwhelmingly used over Op-Amps for all of these reasons [3, 4, 6, 28, 29].

Since this focus of this work is on boost converters in an integrated circuit context, the analysis of error amplifier architectures will focus around those utilizing OTAs. Note that for all equations in this chapter,

$$K = g_m R_O \frac{R_B}{R_T + R_B} \tag{4.1}$$

4.1.2 Lag Compensation (Proportional-Integral)

The Lag Compensator is given in Figure 4.3 and has a transfer function given by (4.2). The feature of this type of compensator is that it provides a phase "lag" at a given peak frequency (determined by the geometric mean of the pole and zero frequency,

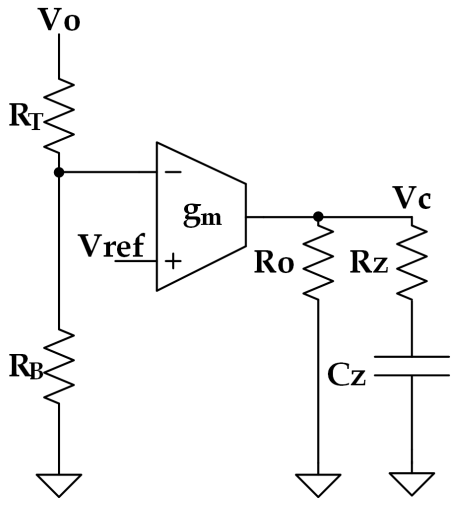

Figure 4.3: Lag Compensator Circuit

$\sqrt{f_z f_p}$ [21]). The DC gain of the system is just the gain of the OTA, as shown in (4.2), while the pole and zero locations are given in (4.3) and (4.4), respectively. Note that for (4.2) to be true, $R_O \gg R_Z$.

$$\frac{V_c}{V_o} = K\left[\frac{sR_ZC_Z + 1}{sR_OC_Z + 1}\right] \tag{4.2}$$

$$|f_p| = \frac{1}{2\pi R_O C_Z} \tag{4.3}$$

$$|f_z| = \frac{1}{2\pi R_Z C_Z} \tag{4.4}$$

The benefit of using a lag compensator, also known as a proportional-integral (PI) controller, is that it can be used to boost the gain of a system without affecting the behavior near the $0\,dB$ crossing point. As such, it's ideal for converters that already have a good phase margin, but just need the DC gain boost in order to eliminate steady-state error.

The primary requirement when designing a lag compensator is to guarantee that the controller's zero frequency is greater than the pole frequency. This is easily done by simply making R_Z much smaller than R_O. As previously mentioned, the frequency at which the controller produces its minimum phase is given by the geometric mean of

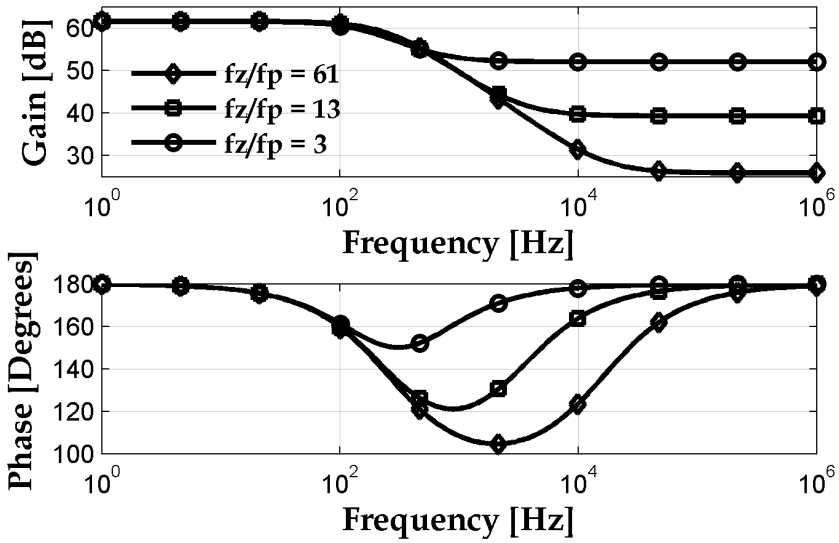

Figure 4.4: Bode Plot for Lag Compensator Circuit with $R_O = 6\,k\Omega$, $C_Z = 100\,nF$, $g_m = -1\,S$, $R_T = 2\,M\Omega$, $R_B = 500\,k\Omega$ and R_Z swept with values of $100\,\Omega$, $500\,\Omega$, and $3\,k\Omega$.

the pole and zero frequency, or $\sqrt{f_z f_p}$. In terms of circuit parameters, this frequency location is given by equation (4.5). Likewise, the total phase shift can be easily calculated using equation (4.6). For example, for a ratio of $\frac{R_Z}{R_O} = \frac{1}{2}$, the phase lags by approximately 20°. A decrease in the ratio by a factor of 2, however, increases the phase lag by 15° (to 35°) - a total change of 75%.

$$f_{min} = \frac{1}{2\pi C_Z \sqrt{R_O R_Z}} \tag{4.5}$$

$$\phi_{min} = sin^{-1}\left(\frac{R_Z - R_O}{R_Z + R_O}\right) \tag{4.6}$$

4.1.3 Lag Compensation Plus Pole

By adding a capacitor, C_C, in parallel with the series RC string, a high-frequency pole can be added to the system, as shown in Figure 4.6. In terms of equations, this circuit can be shown to have a transfer function equivalent to equation (4.7) where $R_O \gg R_Z$ and $C_Z \gg C_C$. Note that the only difference between this compensator and the one shown previously in Figure 4.4 is the addition of the high frequency pole at $f_{p,2} = \frac{1}{2\pi R_Z C_C}$.

$$\frac{V_c}{V_o} = K\frac{sR_Z C_Z + 1}{s^2 R_O R_Z C_C C_Z + sR_O C_Z + 1} \tag{4.7}$$

The benefit of this circuit, rather obviously, is that is provides a high-frequency pole which will help attenuate signals near the switching frequency of the circuit. For this reason, it is a very popular choice in switched-converter controller design [3,21,29].

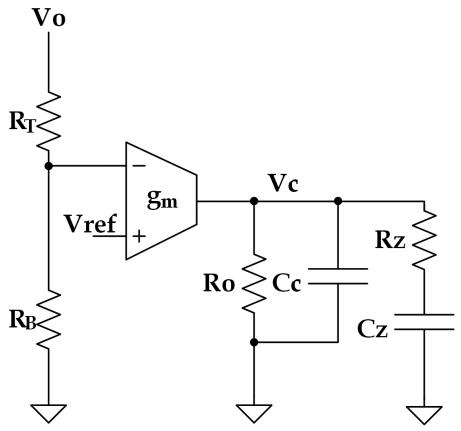

Figure 4.5: Lag Compensator Circuit

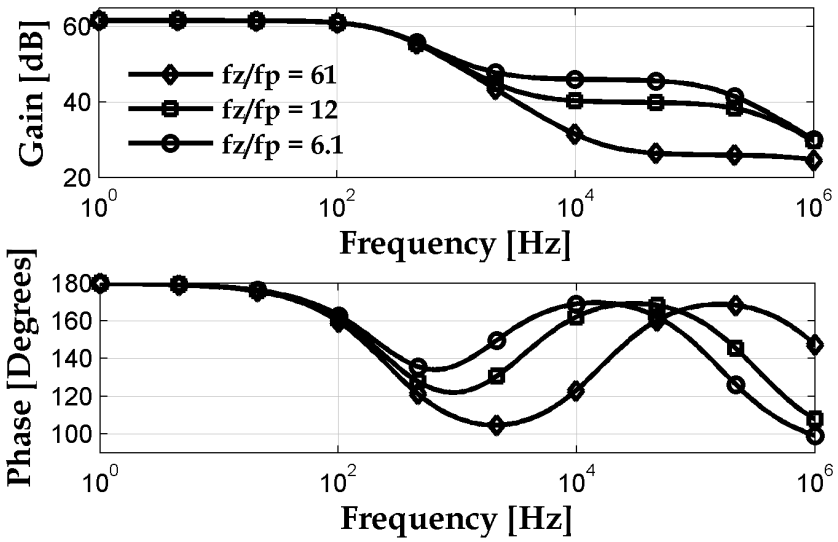

Figure 4.6: Bode Plot for Lag Compensator Circuit Plus Pole with $R_O = 6\,k\Omega$, $C_Z = 100\,nF$, $C_C = 1\,nF$, $g_m = -1\,S$, $R_T = 2\,M\Omega$, $R_B = 500\,k\Omega$ and R_Z swept with values of $100\,\Omega$, $500\,\Omega$, and $1\,k\Omega$.

The sizing of C_C will typically be chosen such that the high-frequency pole cancels out the high-frequency zero caused by the ESR of the output capacitance of the converter. This allows for switching frequencies and any sub-harmonic oscillations (a prominent problem in Current-Mode Control [24, 29]) to be attenuated such that they have a negligible effect on converter performance.

4.1.4 Lag Compensation Plus Pole with Feedback

A modification of the lag compensator with the high-frequency pole is shown in Figure 4.7. The modification is simply to take the RC string and connect it between the inverting terminal of the OTA and the output. The benefit is that the capacitor sizes can be reduced which, in an integrated circuit context, will help to save layout area. The downside is that R_Z needs to be made much larger than R_O which will typically require very large values.

The equation for this controller is shown in (4.8) with the relationship to the compensator without feedback given in (4.9) and (4.10) where variables denoted by the subscript fb indicate it is part of the feedback architecture while the subscript nfb is for the architecture without feedback. Note that C_C, R_O, and g_m are all assumed

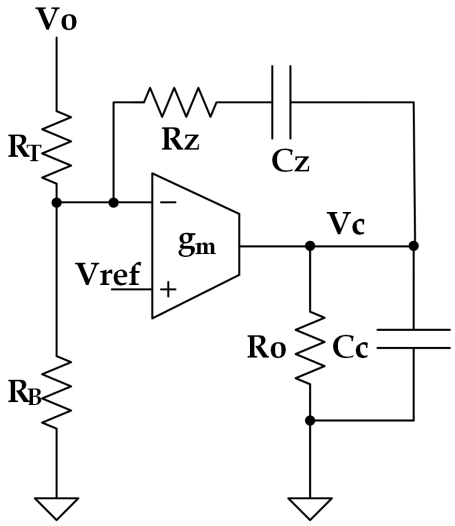

Figure 4.7: Lag Compensator Circuit with Feedback Zero

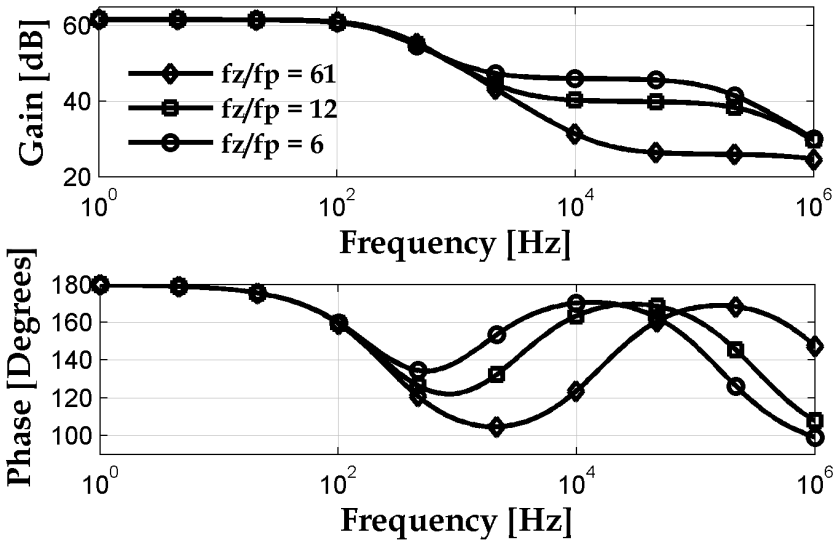

Figure 4.8: Bode Plot for Lag Compensator Circuit Plus Pole with $R_O = 6\,k\Omega$, $C_Z = 250\,fF$, $C_C = 1\,nF$, $g_m = -1\,S$, $R_T = 2\,M\Omega$, $R_B = 500\,k\Omega$ and R_Z swept with values of $40.7\,M\Omega$, $218\,M\Omega$, and $480\,M\Omega$.

to not change between the two architectures and are requirements for (4.9) and (4.10) to hold true. A further assumption is that $g_m R_O \gg 1$.

$$\frac{V_c}{V_o} = K\frac{sC_Z R_Z + 1}{s^2 R_O R_Z C_C C_Z + s(R_Z C_Z + R_O C_C - g_m R_O (R_B \| R_T) C_Z) + 1} \tag{4.8}$$

$$R_{Z,fb} = R_{Z,nfb}\left(\frac{g_m R_O(R_B \| R_T)}{R_{Z,nfb} - R_O}\right) \tag{4.9}$$

$$C_{Z,fb} = \frac{R_{Z,nfb}}{R_{Z,fb}} C_{Z,nfb} \tag{4.10}$$

A Bode plot for this circuit is presented in Figure 4.8 and is identical to the plot without feedback in Figure 4.6. The only circuit parameters to change were an increase in R_Z and a decrease in C_Z. The reduction in C_Z is particularly tantalizing from a design standpoint because, as mentioned earlier, it can help to reduce layout size. However, the massive increase in R_Z can be problematic for processes that lack highly resistive layers that can be used for resistors in the Meg-Ohm range. A potential solution to mitigate this problem would be to move R_Z off chip. Since the value will typically be very large, any increased resistance due to external pin contacts will be negligible.

4.1.5 Lead Compensation (Proportional-Derivative)

Lead compensation doesn't have much use in switched converter circuits due to their increase in gain at high-frequencies, but they're worth talking about in order to provide a complete overview of controller architectures.

The circuit used to implement a lead controller is shown in Figure 4.10. The

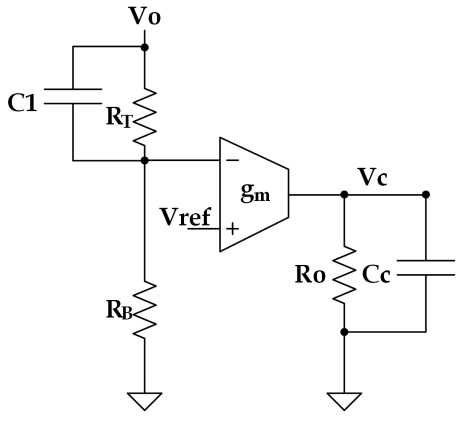

Figure 4.9: Lead Compensator Circuit

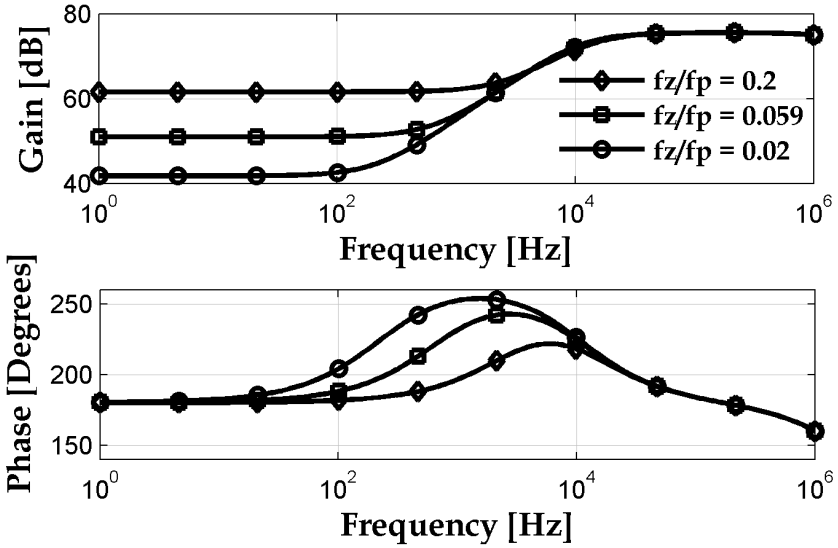

Figure 4.10: Bode Plot for Lead Compensator Circuit with $R_O = 6\,k\Omega$, $C_1 = 30\,pF$, $C_C = 10\,pF$, $g_m = -1\,S$, $R_B = 500\,k\Omega$, and R_T swept with values of $2\,M\Omega$, $8\,M\Omega$, and $24\,M\Omega$.

transfer function for this circuit is given in (4.11).

$$\frac{V_c}{V_o} = K\left[\frac{sR_TC_1 + 1}{(s(R_B\|R_T)C_1 + 1)(sR_OC_C + 1)}\right] \tag{4.11}$$

The phase peak occurs at a frequency given by (4.12) while the total phase boost is given in (4.13). The primary benefit to the lead controller is that it can provide a phase boost at a given frequency which can help to either boost the phase margin, or increase the bandwidth of the system. However, the cost is that higher frequencies also see a boost in gain which is undesirable for switched converters since switching noise and subharmonic oscillations can begin to affect the output voltage and have an undesirable effect on EMI [23]. However, if output voltage quality can be neglected in favor of speed, the lead controller is a solid controller choice.

$$f_{max} = \frac{1}{2\pi C_1\sqrt{(R_B\|R_T)R_T}} \tag{4.12}$$

$$\phi_{max} = sin^{-1}\left(\frac{R_T}{R_T + 2R_B}\right) \tag{4.13}$$

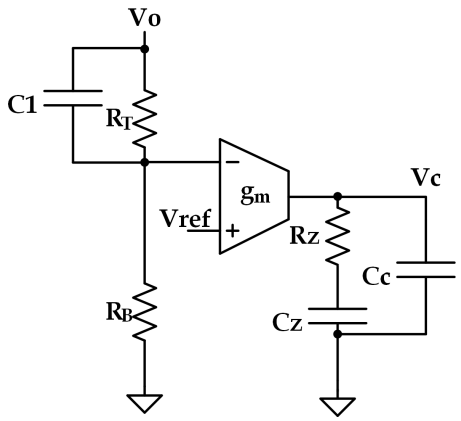

Figure 4.11: Lag-Lead Compensator Circuit

4.1.6 Lag-Lead Compensation (Proportional-Integral-Derivative)

The lag-lead compensator, as shown in Figure 4.11, does just as the name suggests: first lags the phase, then leads it. This architecture is simply a merger of both the lag and lead compensators shown in Figures 4.3 and 4.9, respectively. The transfer function for this controller can be found below in (4.14). Note the familiar pole and zero locations from the lag and lead transfer functions in (4.2) and (4.11), respectively. It is assumed that $R_O \gg R_Z$.

$$\frac{V_c}{V_o} = \frac{g_m R_B}{s(R_B + R_T)(C_Z + C_C)} \frac{(sR_T C_1 + 1)(sR_Z C_Z + 1)}{(s\frac{R_Z C_Z C_C}{C_Z + C_C} + 1)(s(R_T \| R_B)C_1 + 1)} \tag{4.14}$$

The Bode plot for this controller is shown in Figure 4.12. As mentioned previously, the point of this control scheme, as is evident from the graph, is to first lag the phase and then boost it. The benefit to using a lag-lead controller is to obtain the high low-frequency gain that's indicative of a lag controller as well as the phase boost from the lead architecture that allows for an increase in phase margin. The cost, rather obviously, is that it increases the number of components required to implement a controller and, less obviously, is far more sensitive to pole and zero locations.

In order for a lag-lead controller to be properly designed, $|f_{p,1}| < |f_{z,1}| < |f_{z,2}| < |f_{p,2}|$ where the pole and zero relationships are given in (4.15) through (4.19). The

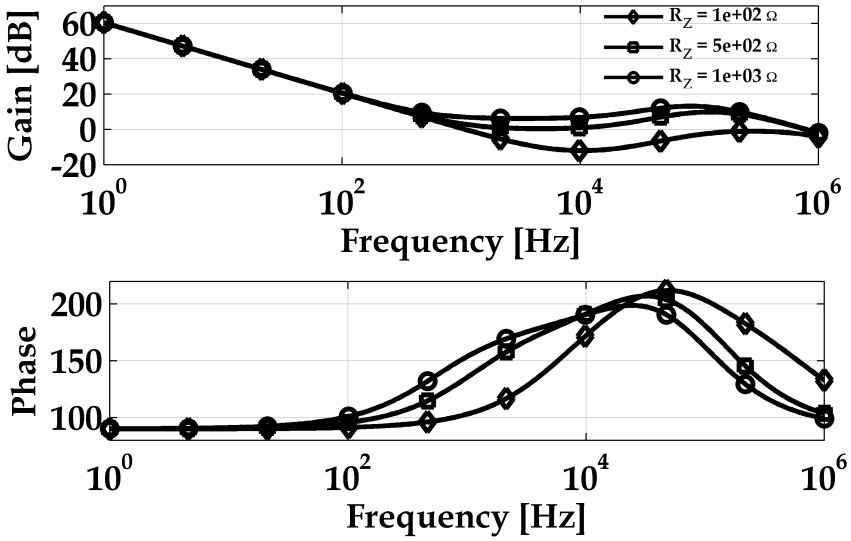

Figure 4.12: Bode Plot for Lag-Lead Compensator Circuit with $C_1 = 0.8\,pF$, $C_C = 2\,nF$, $g_m = -10\,\mu S$, $R_B = 500\,k\Omega$, $R_T = 2\,M\Omega$, $C_Z = 300\,nF$, and R_Z swept with values of $100\,\Omega$, $500\,\Omega$, and $1\,k\Omega$.

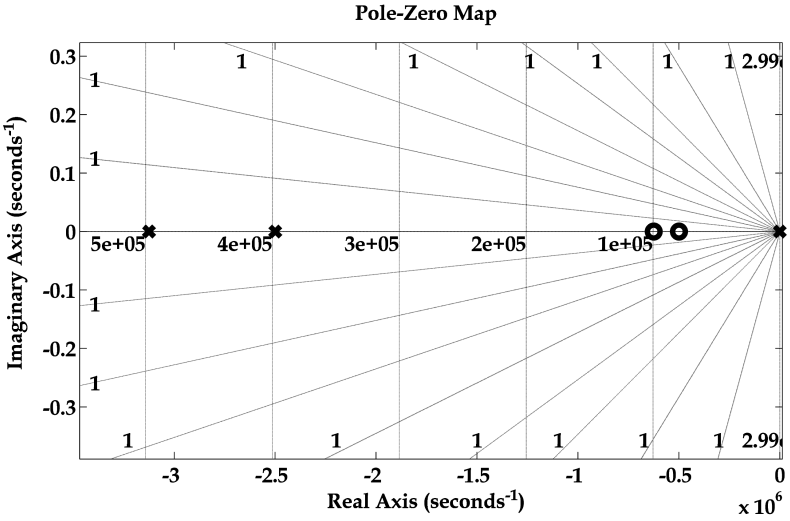

Figure 4.13: Pole-Zero Plot for Lag-Lead Compensator Circuit with $C_1 = 0.8\,pF$, $C_C = 2\,nF$, $g_m = -10\,\mu S$, $R_B = 500\,k\Omega$, $R_T = 2\,M\Omega$, $C_Z = 300\,nF$, and R_Z swept with values of $100\,\Omega$, $500\,\Omega$, and $1\,k\Omega$.

third pole, $f_{p,3}$ is less sensitive to its location as it is a much higher frequency than the other values. Typically, this is placed at one half the switching frequency in order to properly attenuate the noise caused by switching [30].

Figure 4.13 shows the pole and zero locations on an imaginary plane. Note the

progression of pole → zero → zero → pole from right to left, which is needed in order for the lag-lead compensator to function correctly. Also, as mentioned previously, there is a high-frequency pole that sits at a location that is far enough away from the other poles and zeros where it will not have a heavy influence on the converter (other than to attenuate events near the switching frequency).

$$f_{p,1} = 0 \tag{4.15}$$

$$f_{p,2} = \frac{1}{2\pi(R_B \| R_T)C_1} \tag{4.16}$$

$$f_{p,3} = \frac{C_C + C_Z}{2\pi R_Z C_Z C_C} \tag{4.17}$$

$$f_{z,1} = \frac{1}{2\pi R_Z C_Z} \tag{4.18}$$

$$f_{z,2} = \frac{1}{2\pi R_T C_1} \tag{4.19}$$

4.2 Controller Selection

Being able to determine what controller architecture is best suited for a given switcher design is paramount in guaranteeing a stable and well-performing switched converter. Each controller topology, like any circuit, has a series of advantages and disadvantages associated with them that need to be weighed against device requirements. These advantages and disadvantages have been discussed in each controller architecture description, but to fully understand the implications it's best to observe their use in typical circuits.

As Basso describes in his book, the lag-plus-pole architecture is the most popular as it provides good low-frequency gain as well as the ability to cancel the effect of the zero due to the series resistance on the filter capacitor [21]. For example, consider a converter in DCM with a zero caused by the aforementioned capacitor ESR. By applying a basic lag architecture (with only one pole and zero), the converter has a frequency response shown in Figure 4.14. Here, the ESR of the filter capacitor causes the gain to level off at high frequency resulting in a crossover frequency near $300\,kHz$ which is near the frequency many switchers are typically operated at. Clearly, this is not ideal as the switching noise will either be amplified by the system

(for switching frequencies under $300\,kHz$) or just slightly attenuated (for frequencies above $300\,kHz$).

To solve this problem, C_C is added in parallel with R_O on the controller to create the lag-plus-pole compensator. Without modifying any other parameters in either the boost circuit or compensator, C_C can be chosen such that is cancels out the zero caused by the boost ESR. In doing so, the crossover frequency is decreased down to around $60\,kHz$ with a $-20\,dB$ attenuation at the previous crossover frequency of $300\,kHz$ which is a huge improvement for only adding in a $5\,nF$ capacitor (2000 times smaller than that of C_Z!).

The lag-lead compensation architecture is best suited for converters with conjugate-pair poles such as the CCM boost converter. The primary reason for this is that it provides the needed low-frequency gain boost that minimizes steady-state error while also providing the higher frequency phase boost that increases phase-margin. However, designing a controller that guarantees CCM stability is still no trivial task. The resonant frequency peak is still quite a problem as the large phase shift (180° worst-case) will require a large phase boost from the controller in order to achieve any semblance of stability.

Since the controller in a switched converter has well defined architectures, as has

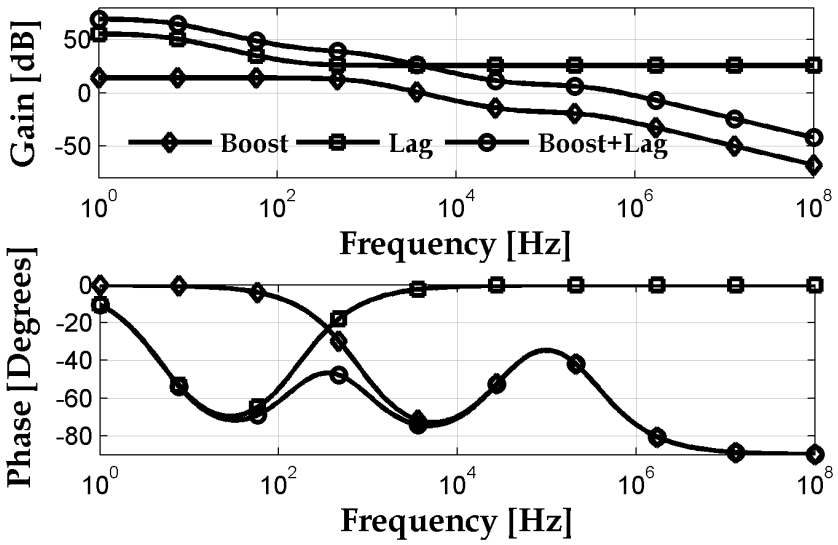

Figure 4.14: Bode Plot for Lag Compensator with DCM Boost with $G_{d0} = 5$, $C_O = 10\,\mu F$, $R_{ESR} = 0.5\,\Omega$, $Q = 0.05$, $\omega_0 = 16\,kHz$, $R_O = 3\,k\Omega$, $R_Z = 100\,\Omega$, $C_Z = 10\,\mu F$, $g_m = -1S$, $R_T = 2\,M\Omega$, and $R_B = 500\,k\Omega$

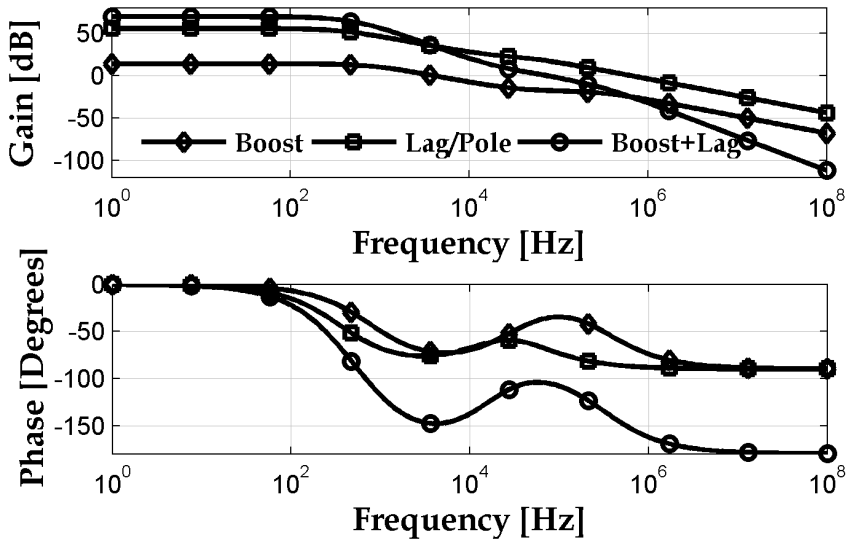

Figure 4.15: Bode Plot for Lag Compensator Plus Pole with DCM Boost with $G_{d0} = 5$, $C_O = 10\,\mu F$, $R_{ESR} = 0.5\,\Omega$, $Q = 0.05$, $f_0 = 16\,kHz$, $R_O = 3\,k\Omega$, $R_Z = 100\,\Omega$, $C_Z = 10\,\mu F$, $C_C = 50\,nF$, $g_m = -1S$, $R_T = 2\,M\Omega$, and $R_B = 500\,k\Omega$

been shown throughout this chapter, the only real unknowns are which architecture is best suited for a given converter, as well as what the optimum component values are. As such, it's possible to use AI techniques such as Genetic Algorithms in order to optimize the design of a converter controller. This technique is discussed more in Appendix A.

Choosing a controller topology is highly dependent on converter type as well as operating mode, as shown. Component value selection is extremely critical in order to ensure a robust and repeatable design that is accurate and stable in all operating conditions.

Chapter 5

Full Boost Converter Model Analysis

Utilizing the models derived throughout the previous chapters, a full small-signal model of a boost converter can be constructed. This will allow for a thorough investigation of what parameters have the largest impact on boost converter stability. This, in turn, will allow for more comprehensive studies in ways to test said stability as well as present useful debugging methods.

Throughout this chapter, both the CCM and DCM converters will be analyzed. A baseline design will be presented and various parameters will be modified in order to gauge the sensitivity of frequency response performance metrics to these parameters.

5.1 CCM Converter Model

As mentioned in Chapter 4 and outlined in various sources [15, 21, 23], due to the conjugate-pair-pole intrinsic to CCM Boost Converters the only truly acceptable control topology is that of a PID (*a.k.a.* Lag-Lead) controller. A full circuit implementation is shown in Figure 5.1.

Table 5.1 lists the component values used in this design and the non-ideal component values are as follows: $r_L = 0.8\,\Omega$, and $r_C = 0.5\,\Omega$.

From the previous analysis in Chapter 4, it's possible to find the pole and zero

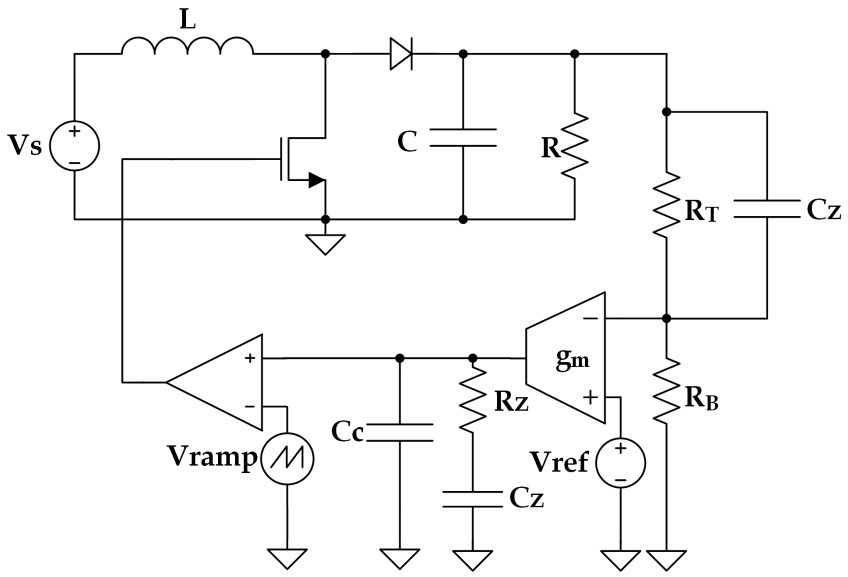

Figure 5.1: Boost Converter with PID Control

locations of this converter. The equations for the poles are given in (5.1) [31].

$$s_1, s_2 = \frac{f_0}{4\pi Q}(-1 \pm \sqrt{1 - 4Q^2}) \tag{5.1}$$

Based on the parameters given in Table 5.1 as well as the parasitic values presented earlier, the values for f_0, Q, and the pole/zero locations are shown in Table 5.2. The value for Q is larger than 0.5 therefore there is a conjugate pole - as is expected for a CCM converter. The frequency at which the pole exists is given in Table 5.2 as $2.68\,kHz$. Using (5.1), this occurs at $-\sigma \pm j\omega = -7.2 \times 10^3 \pm j15.2 \times 10^3$ when plotted on the complex plane. The Bode plot and pole-zero plot can be seen in Figures 5.2 and 5.3, respectively.

Table 5.1: CCM Boost Converter DC Specs

Parameter	V_S	V_O	I_O	L	F_S	C
Value	$3\,V$	$6\,V$	$300\,mA$	$200\,\mu H$	$350\,kHz$	$5\,\mu F$

Table 5.2: CCM Boost Converter Pole and Zero Locations

f_0	Q	$f_{p,1}$	$f_{p,2}$	$f_{z,1}$	$f_{z,2}$
$2.68\,kHz$	1.17	$2.68\,kHz$	$2.68\,kHz$	$3.34\,kHz$	$63.7\,kHz$

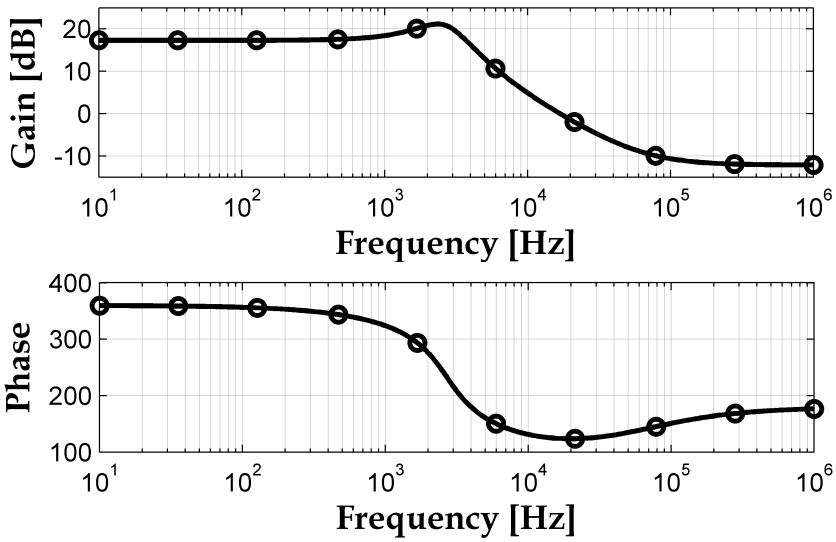

Figure 5.2: CCM Boost Converter Bode Plot

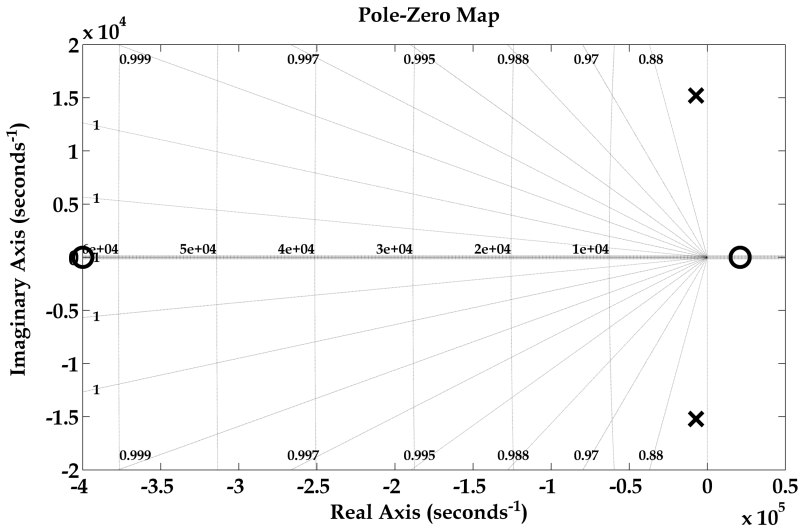

Figure 5.3: CCM Boost Converter Pole-Zero Plot

In order to properly design this converter and to guarantee stability, the zeros of the PID controller must be placed at or near the resonant frequency, f_0, which occurs at $2.68\,kHz$. To do so, the component values included in the equations $\frac{1}{2\pi R_Z C_Z}$ and $\frac{1}{2\pi R_T C_1}$ (from (4.18) and (4.19)) must be chosen such that the ensuing frequency occurs near f_0.

First, the value for R_T should be chosen. Since the value for this resistor is

constrained by the need for the R_T and R_B string to divide down the output voltage to the reference (which will be $1.3\,V$ used for this example), it's given that $R_T = 3.583R_B$. In order to guarantee that the power consumption of the resistive feedback string is minimized, the value for both R_T and R_B must be large. The choice of these parameters is, ultimately, up to the designer so for this controller design the values were selected as $\boldsymbol{R_B = 560\,k\Omega}$ which yields $\boldsymbol{R_T = 2\,M\Omega}$.

With the selection of R_T, C_1 can be determined to be $\boldsymbol{C_1 = 30\,pF}$ via (4.19) which was presented again earlier in this section. Next, the values for R_Z and C_Z must be selected. For this design example, it was decided that the second zero frequency would be placed at $3\,kHz$ which is slightly larger than the resonant frequency of the converter, but still close enough such that dual-zero behavior would still be exhibited near f_0. By setting $\boldsymbol{R_Z = 200\,k\Omega}$, the capacitor value becomes $\boldsymbol{C_Z = 260\,pF}$.

With the values that determine the controller's zero frequency selected, the pole frequencies must be calculated and shown to be valid (recall from Chapter 4 that $f_{z1,2}$ must be less than $f_{p2,3}$). Since $f_{p,2} = \frac{R_T+R_B}{2*\pi R_T R_B C_1}$, it's clear that this pole will be located at $12\,kHz$. The last pole, $f_{p,3}$ has some flexibility as to where it is placed. Because there is a high-frequency zero from the converter due to the ESR of the filter capacitor, it's wise to place $f_{p,3}$ such that it cancels this zero out. Since $f_{p,3} = \frac{C_C+C_Z}{2\pi R_Z C_C C_Z}$, $\boldsymbol{C_C = 13\,pF}$.

Finally, the only parameter left is the transconductance of the amplifier itself, g_m. This value can be modified by changing the bias current of the OTA which allows for the gain to be modified in order to achieve both a good phase margin and DC gain (which eliminates steady-state error). In this example, $\boldsymbol{g_m = 1.03\mu S}$ as it allows for a decent phase margin of $\phi_M = 45°$ and DC gain of $40\,dB$. The Bode plot, root-locus plot, and step-response are showed in Figures 5.4, 5.5, and 5.6, respectively.

As Figure 5.4 shows, just a slight increase in gain will result in instability due to the large phase change near the converter's resonant frequency. In fact, the gain margin of the circuit is near $2\,dB$ which is *much* smaller than what a commercial design would require. Observation of the root-locus in Figure 5.5 confirms this as it shows that by increasing the gain, the conjugate poles will transition to the RHP which is a characteristic of system instability. However, by decreasing the gain any further, the steady-state error will begin to noticeably worsen. Figure 5.6 shows the

problems with low DC-gain: the converter struggles to reach steady-state.

5.1.1 Component Sensitivity

Observing the sensitivity of stability to various parameters is important in order to understand what types of component tolerances are acceptable in a switched converter.

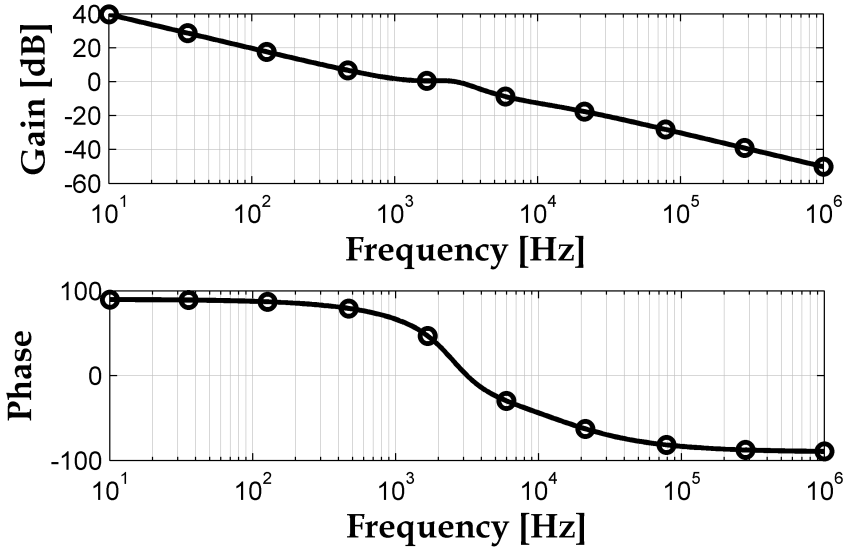

Figure 5.4: CCM Boost Converter Bode Plot with PID Control; $g_m = 1.03\,\mu S$, $R_B = 560\,k\Omega$, $R_T = 2\,M\Omega$, $R_Z = 200\,k\Omega$, $C_C = 13\,pF$, $C_Z = 260\,pF$, $C_1 = 30\,pF$.

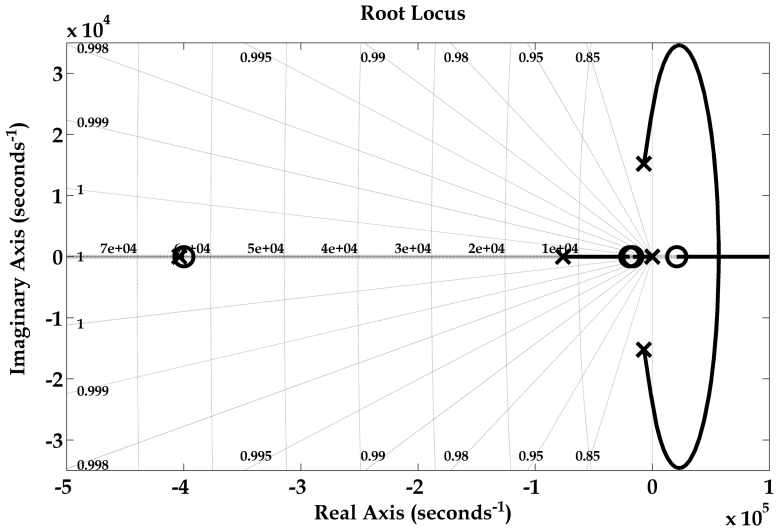

Figure 5.5: CCM Boost Converter Root-Locus with PID Control

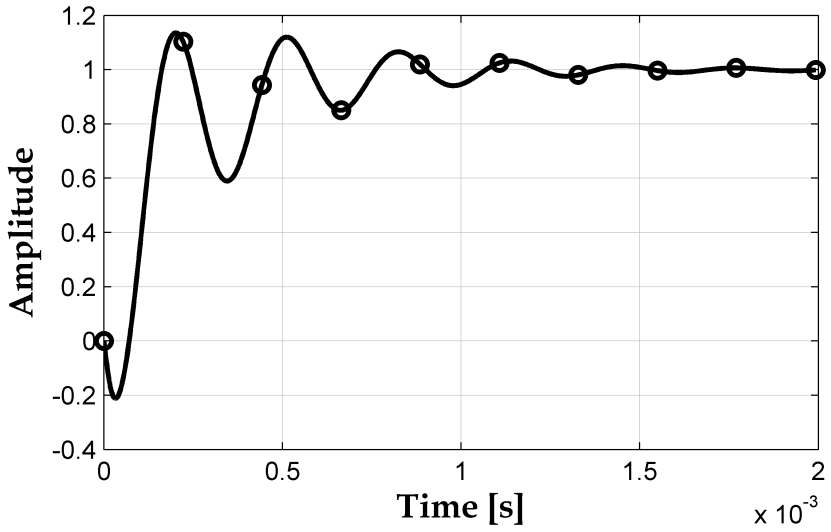

Figure 5.6: CCM Boost Converter Step-Response with PID Control

Unfortunately, due to the complexity of the system, it's rather tedious to mathematically derive general sensitivity equations. Even if said expressions were derived, the relationship between the parameter values and stability parameters, such as phase margin, would be difficult to ascertain. As such, a better approach is to observe how these values change graphically.

To begin, the converter design from the previous section will be used again here. First, the tolerances of various components will be defined. The best, nominal, and worst-case values will then be used and plugged into back into the design and the phase margin, gain margin, DC gain, and bandwidth recorded. The values that will be modified are shown in Table 5.3.

Figure 5.7 shows how the phase margin, ϕ_M, changes with different parameter combinations. Note that each division shown on the graph contains two further unmarked corners from the value for L and g_m. As the bars progress from left to right in each load current division, L varies from minimum to nominal to maximum while g_m varies through its values each time *per* L value.

Table 5.3: CCM Boost Converter Parameter Corners

Component	V_S	I_O	L	g_m
Tolerance	$\pm$40%	$\pm$50%	$\pm$15%	$\pm$10%

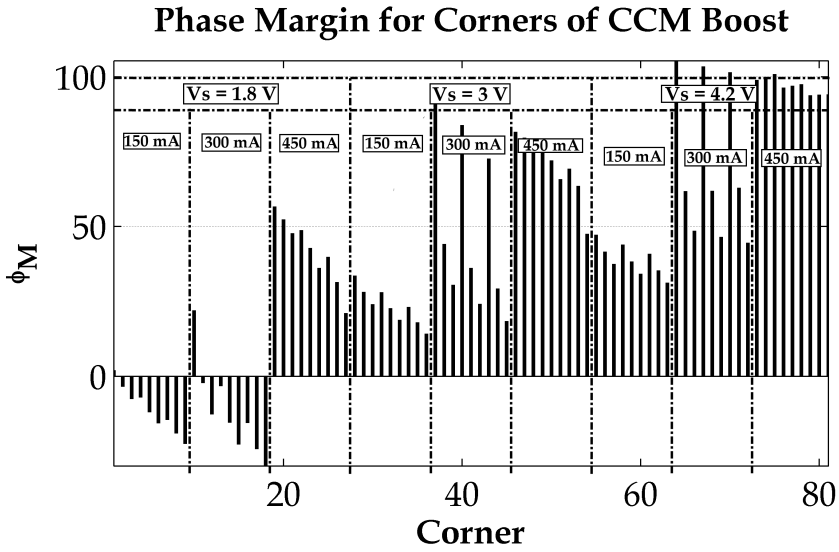

Figure 5.7: CCM Boost Converter Phase Margin Over Parameter Corners. $V_S = [1.8\,V,\ 3\,V,\ 4.2\,V]$, $I_O = [150\,mA,\ 300\,mA,\ 450\,mA]$, $L = [170\,\mu H,\ 200\,\mu H,\ 230\,\mu H]$, $g_m = [0.93\,\mu S,\ 1.03\,\mu S,\ 1.13\,\mu S]$.

From this graph, three general trends are readily apparent:

1. As the DC conversion ratio increases, the phase margin increases.

2. As the load current increases, the phase margin increases.

3. As the inductance increases, the phase margin decreases.

The most stable operation region is when $V_S = 4.2\,V$ (which translates to $M = 1.4$) and $I_O = 450\,mA$. Here, ϕ_M hovers around the 80° mark regardless of the values for either g_m or L. However, this comes at a cost. Figure 5.8 depicts the bandwidth of the converter across the same corners and, as can be seen, bandwidth decreases with increasing phase margin. This is downside of requiring a fast converter: less stability.

Figures 5.9 and 5.10 show the gain margin and the DC Gain of the converter, respectively. The gain margin has a slightly different parametric relationship with the load current when compared to the phase margin. Here, larger load currents cause smaller values of gain margin. This is due to the fact that the phase margin is only increasing because the zero-crossing frequency is being moved to a lower value (*i.e.,* lowering the bandwidth). The phase at these lower frequency values is located

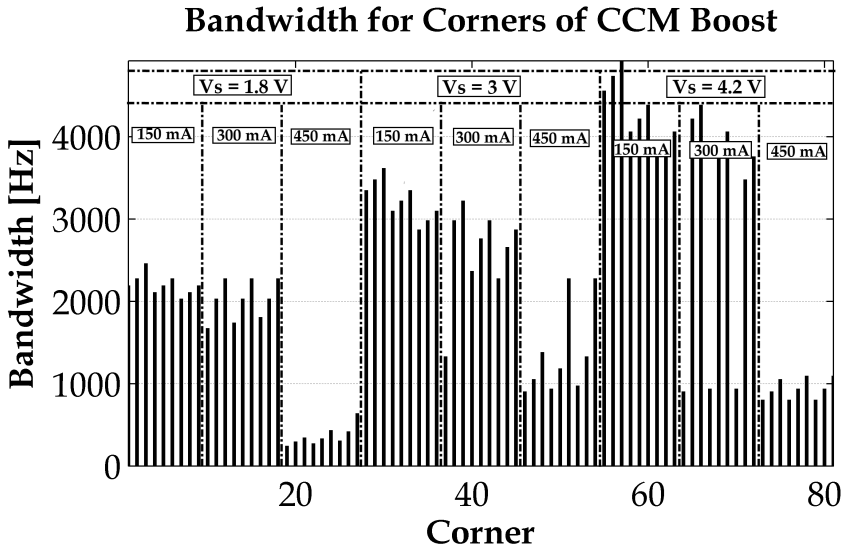

Figure 5.8: CCM Boost Converter Bandwidth Over Parameter Corners. $V_S = [1.8\,V,\ 3\,V,\ 4.2\,V]$, $I_O = [150\,mA,\ 300\,mA,\ 450\,mA]$, $L = [170\,\mu H,\ 200\,\mu H,\ 230\,\mu H]$, $g_m = [0.93\,\mu S,\ 1.03\,\mu S,\ 1.13\,\mu S]$.

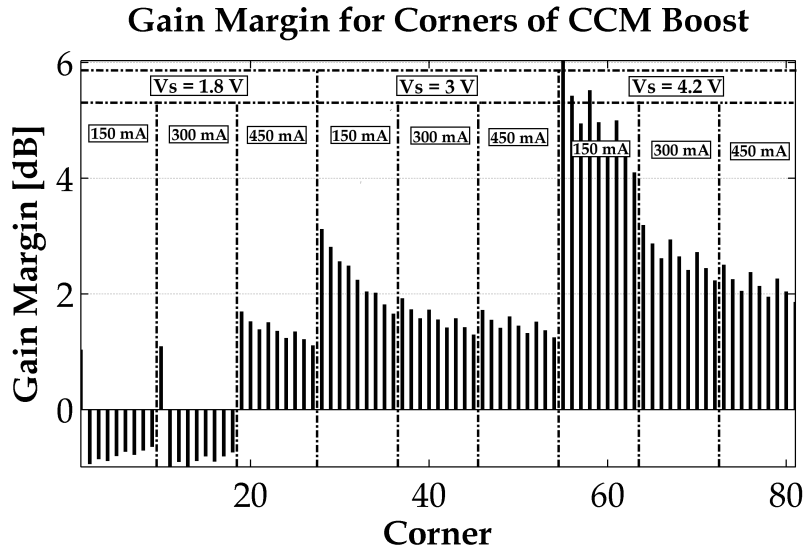

Figure 5.9: CCM Boost Converter Gain Margin Over Parameter Corners. $V_S = [1.8\,V,\ 3\,V,\ 4.2\,V]$, $I_O = [150\,mA,\ 300\,mA,\ 450\,mA]$, $L = [170\,\mu H,\ 200\,\mu H,\ 230\,\mu H]$, $g_m = [0.93\,\mu S,\ 1.03\,\mu S,\ 1.13\,\mu S]$.

just before the 'drop-off' caused by the conjugate-pair pole and as can be observed in the Bode plot back in Figure 5.4. Because there is a rather rapid decrease in phase

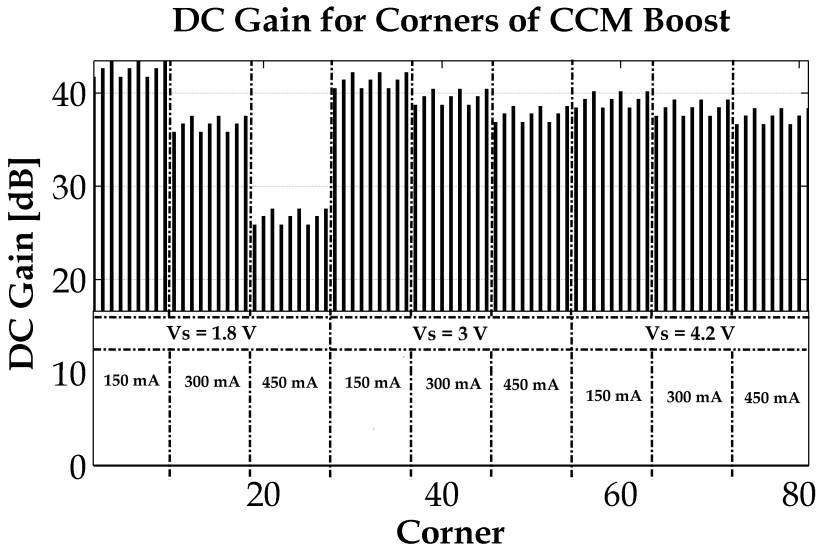

Figure 5.10: CCM Boost Converter DC Gain Over Parameter Corners. $V_S = [1.8\,V,\ 3\,V,\ 4.2\,V]$, $I_O = [150\,mA,\ 300\,mA,\ 450\,mA]$, $L = [170\,\mu H,\ 200\,\mu H,\ 230\,\mu H]$, $g_m = [0.93\,\mu S,\ 1.03\,\mu S,\ 1.13\,\mu S]$.

shortly after the zero-crossing, it's conceivable that the phase will equal 0° before the gain drops a sufficient amount to provide a large gain margin. The DC gain, in Figure 5.10, seems to be rather resilient to changes in parameter barring large load currents at large conversion ratios. This is most easily explained by observing the gain of just the switched converter block itself and ignoring the controller. The expression was defined previously in Chapter 3 in equation (3.44). The expression is a function of both the duty cycle and the load resistance. By plugging in conversion ratio into D and the load current into R, (3.44) can be modified as follows in (5.2),

$$G_{d0,CCM} = MV_O\frac{V_O - r_L I_O M^2}{V_O + r_L I_O M^2} \tag{5.2}$$

It's clear that as both I_O and M increase, the gain of the converter block *must* decrease since the denominator will become larger than the numerator. Likewise, the larger M is, the smaller (5.2) will become which is why the effect is more prevalent at the larger conversion ratio in Figure 5.10.

5.2 DCM Converter Model

The DCM Converter is shown in Figure 5.11 with a Lag-Plus-Pole Feedback OTA (also considered a PI Controller). The specifications for the converter are shown below in Table 5.4.

As shown in Chapter 3, the DCM boost converter does not have a conjugate pole and thus is easier to control. Table 5.5 shows the locations of the poles and zeros for the DCM converter. Again, because $Q < 0.5$, the converter does not have any poles with imaginary components.

Figure 5.12 shows the Bode plot for the boost converter while Figure 5.13 shows

Table 5.4: DCM Boost Converter DC Specs

Parameter	V_S	V_O	I_O	L	F_S	C
Value	$3\,V$	$6\,V$	$30\,mA$	$20\,\mu H$	$350\,kHz$	$5\,\mu F$

Table 5.5: DCM Boost Converter Pole and Zero Locations

f_0	Q	$f_{p,1}$	$f_{p,2}$	$f_{z,1}$	$f_{z,2}$
$9.33\,kHz$	0.06	$586\,Hz$	$150\,kHz$	$298\,kHz$	$63.7\,kHz$

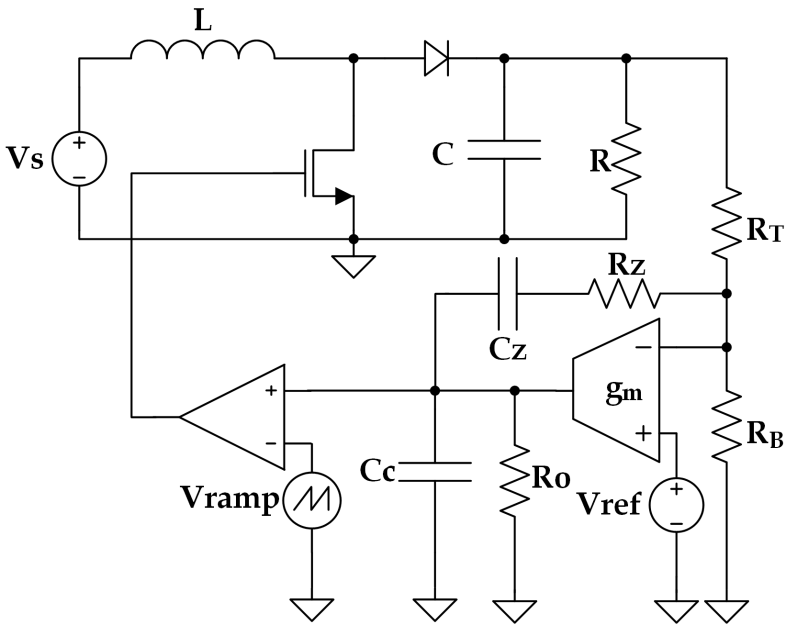

Figure 5.11: Boost Converter with PI Control

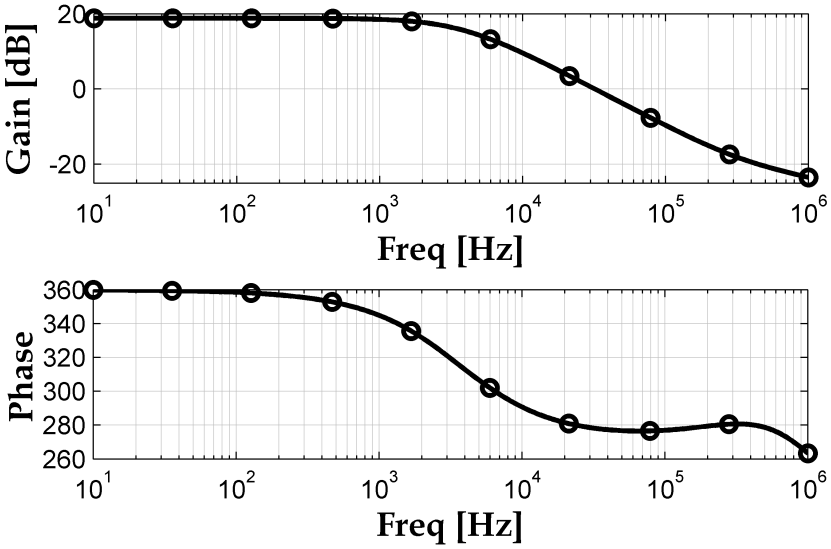

Figure 5.12: DCM Boost Converter Bode Plot

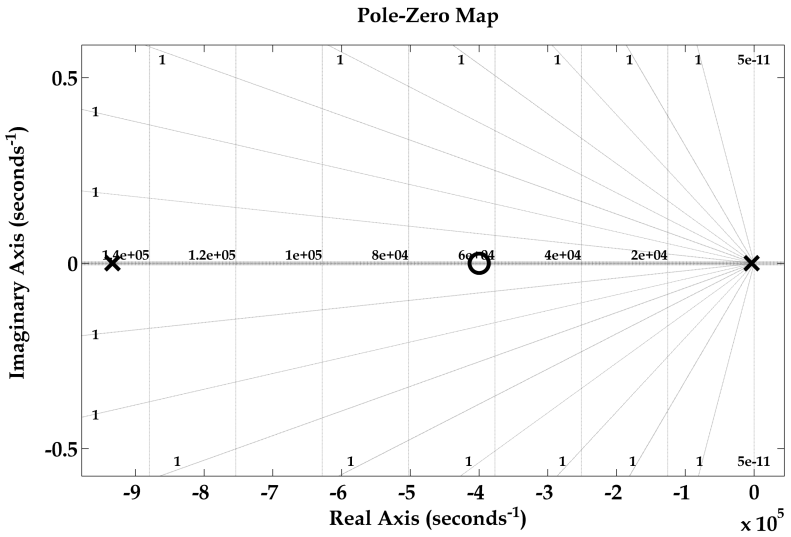

Figure 5.13: DCM Boost Converter Pole-Zero Plot (RHPZ Not Shown)

the pole and zero locations on the complex plane. The convenient reality of the DCM boost converter is that it behaves like a single-pole system at frequencies less than half of the switching frequency. Ideally, a controller would be designed that just raises the DC gain of the system while not disturbing the crossover frequency.

To achieve such a design, the first pole of the controller should be placed at a low frequency while the second pole should be placed such that it minimizes the effect

of the converter zero due to the ESR. The zero of the controller should be placed such that it cancels the pole from the converter so that the phase lag it produces can be eliminated. The overall effect is that the controller frequency response becomes more dominant than that of the converter frequency response. This indicates that time constant $R_Z C_Z$ should be equal to $272\,\mu s$. Choosing $\boldsymbol{C_Z = 100\,pF}$ results in $\boldsymbol{R_Z = 1.7\,M\Omega}$.

Choosing the pole locations, however, is not as simple. The complexity of the transfer function for this type of controller, as given in (4.8) in Chapter 4 whose denominator is reproduced below in (5.3), makes it more difficult to ascertain the relationship between parameter values and pole locations. The easiest approach is to plug in the known values of R_Z and C_Z as well as expected values for R_O, g_m, R_T, and R_B. As was the case with the CCM converter, R_T is constrained to be $3.583 R_B$ so by setting $\boldsymbol{R_B = 600\,k\Omega}$, it follows that $\boldsymbol{R_T = 2.15\,M\Omega}$. Likewise, since R_O must be large and $g_m R_O \gg 1$, good estimates as to what those values will be can be discovered. These parameters largely depend on the architecture of the OTA, but $\boldsymbol{R_O = 1\,M\Omega}$ and $\boldsymbol{g_m = 10\,mS}$ are not unreasonable.

$$0 = s^2 R_O R_Z C_C C_Z + s(R_Z C_Z + R_O C_C - g_m R_O (R_B \| R_T) C_Z) + 1 \tag{5.3}$$

By taking those calculated values, the expression in (5.3) reduces to:

$$0 = s^2(270 C_C) + s(10^6 C_C + 0.4) + 1$$

By choosing a secondary pole frequency of $6\,kHz$, the value for C_C emerges when the magnitude of the above expression is solved for 0 (plugging $j\omega$ in for s). This yields $\boldsymbol{C_C = 44\,nF}$. The choice of the secondary pole location is somewhat arbitrary as it just needs to help attenuate high-frequency signals. Here it was also used to move the crossover frequency to a slightly lower value in order to achieve a better phase margin.

Figure 5.14 shows the Bode plot of the whole system. The crossover freqeuncy occurs near the secondary pole of the PI Controller at $6\,kHz$ with a phase margin equal to $\phi_M = 60°$. The root locus of the system is shown in Figure 5.15 and never crosses the imaginary axis which indicates that the system is inherently stable.

However, the poles of the controller can end up 'colliding' on the real-axis causing them to breakaway and become a conjugate pair pole. This is easily controllable by not allowing the gain of the controller to exceed a certain value (most OTAs will be naturally constricted to some operating range anyway). The step response in Figure 5.16 verifies the stability of the system by showing very little oscillation (much different than the CCM step response in Figure 5.6), as would be expected from a

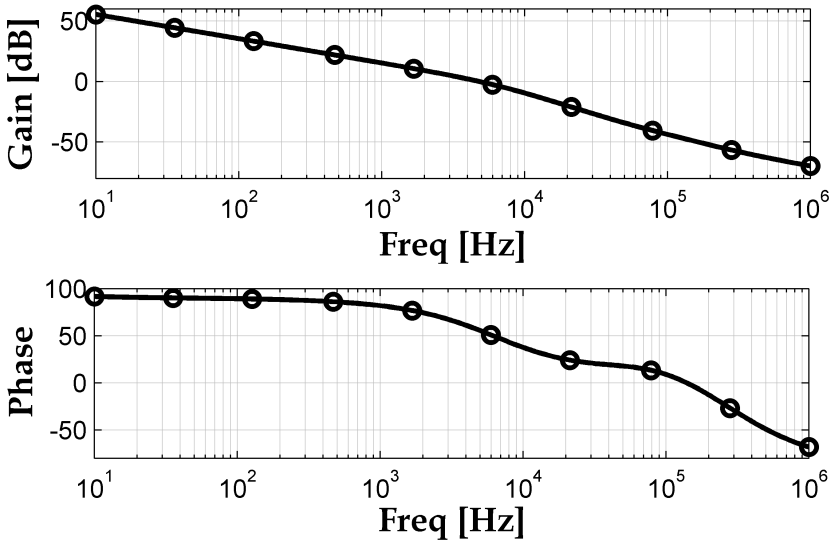

Figure 5.14: DCM Boost Converter with PI Control Bode Plot

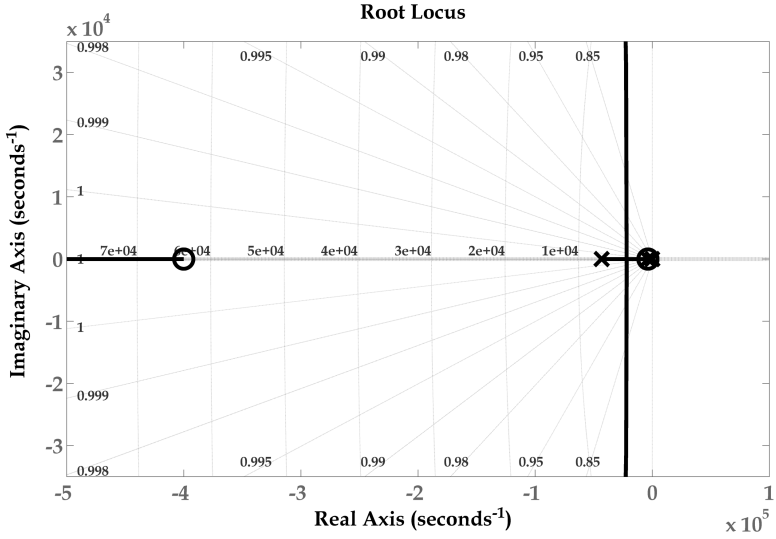

Figure 5.15: DCM Boost Converter with PI Control Root Locus

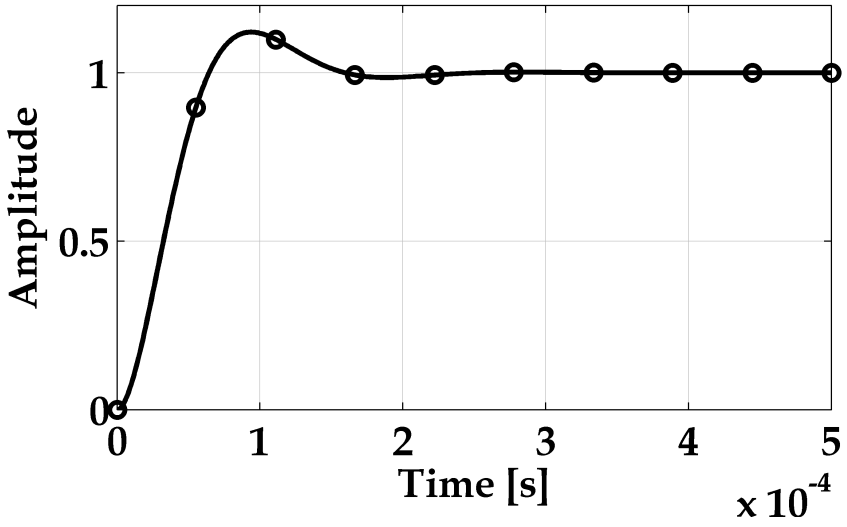

Figure 5.16: DCM Boost Converter with PI Control Step Response

system with a phase margin of 60°.

5.2.1 Component Sensitivity

As was done with the CCM with PID Control Converter, the sensitivity of various frequency-domain measurements will be graphically observed in relation to varying parameters. Table 5.6 shows the tolerances used for various components.

Figure 5.17 shows how the phase margin changes when each component is varied. Unlike in the CCM case, it's clear that as the load current increases, the phase margin decreases. However, the change is very slight as it takes an 80% increase in the load current to drop the phase margin by only 15°. Likewise, this value is very resilient to changes in conversion ratio and inductor size as the only major value shift is due to the load current.

Since the phase margin decreases with increasing load current, it follows that the bandwidth is likely increasing which is verified in Figure 5.18. Again, as was the case with the phase margin, the bandwidth is relatively immune to changing any other

Table 5.6: DCM Boost Converter Parameter Corners

Component	V_S	I_O	L	g_m
Tolerance	±40%	±80%	±25%	±20%

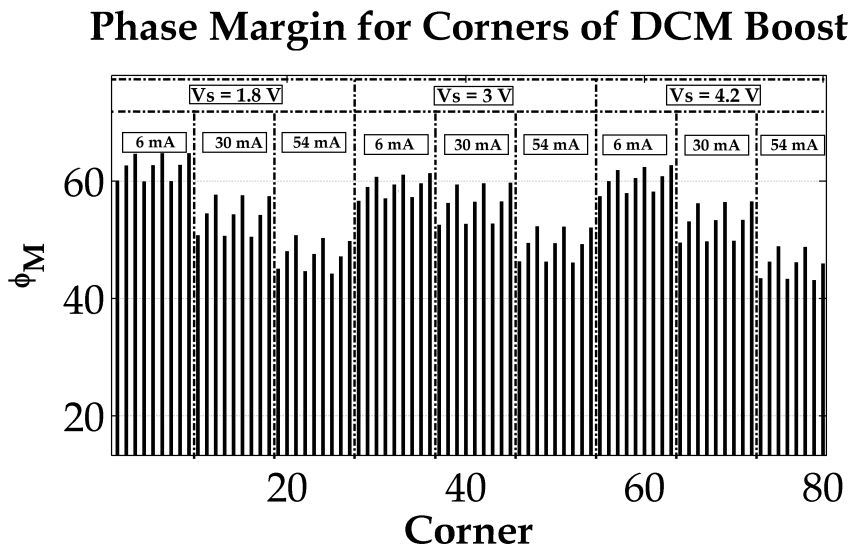

Figure 5.17: DCM Boost Converter Phase Margin Over Parameter Corners. $V_S = [1.8\,V,\ 3\,V,\ 4.2\,V]$, $I_O = [6\,mA,\ 30\,mA,\ 54\,mA]$, $L = [15\,\mu H,\ 20\,\mu H,\ 25\,\mu H]$, $g_m = [8\,mS,\ 10\,mS,\ 12\,mS]$.

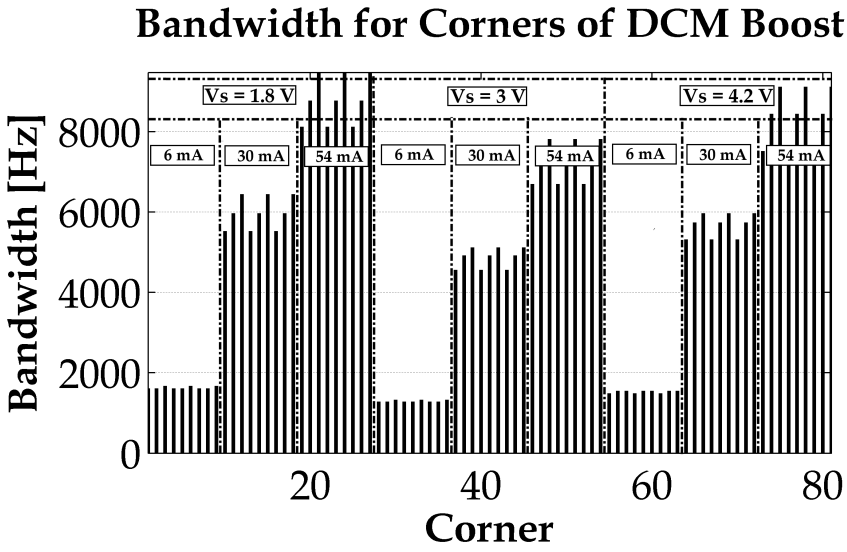

Figure 5.18: DCM Boost Converter Bandwidth Over Parameter Corners. $V_S = [1.8\,V,\ 3\,V,\ 4.2\,V]$, $I_O = [6\,mA,\ 30\,mA,\ 54\,mA]$, $L = [15\,\mu H,\ 20\,\mu H,\ 25\,\mu H]$, $g_m = [8\,mS,\ 10\,mS,\ 12\,mS]$.

parameter outside of the load current which is a testament to the robustness of the VMC-DCM Converter.

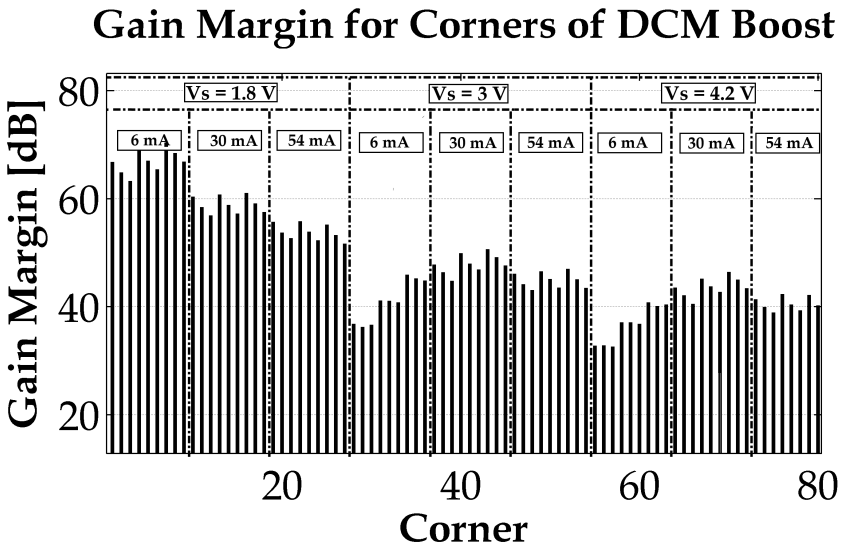

Figure 5.19: DCM Boost Converter Gain Margin Over Parameter Corners. $V_S = [1.8\,V,\ 3\,V,\ 4.2\,V]$, $I_O = [6\,mA,\ 30\,mA,\ 54\,mA]$, $L = [15\,\mu H,\ 20\,\mu H,\ 25\,\mu H]$, $g_m = [8\,mS,\ 10\,mS,\ 12\,mS]$.

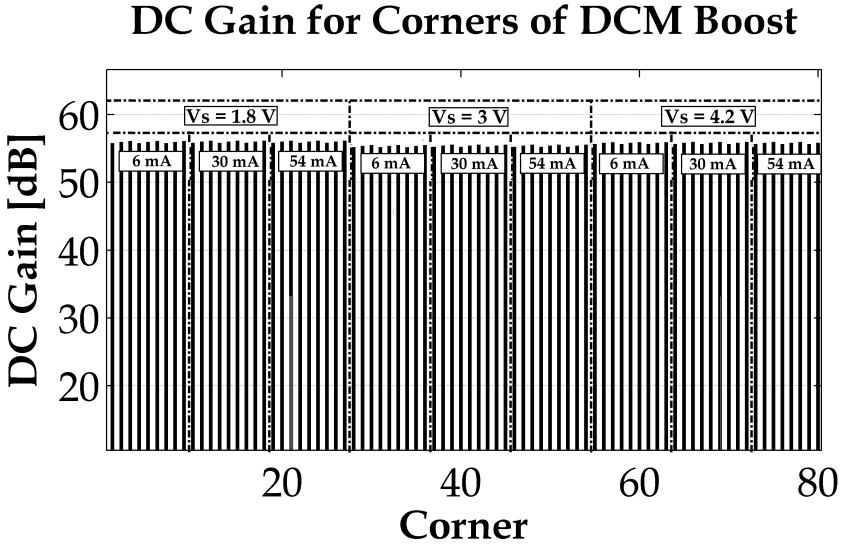

Figure 5.20: DCM Boost Converter DC Gain Over Parameter Corners. $V_S = [1.8\,V,\ 3\,V,\ 4.2\,V]$, $I_O = [6\,mA,\ 30\,mA,\ 54\,mA]$, $L = [15\,\mu H,\ 20\,\mu H,\ 25\,\mu H]$, $g_m = [8\,mS,\ 10\,mS,\ 12\,mS]$.

The gain margin in Figure 5.19 exhibits a slightly different trend than seen with the phase margin. Here, this value decreases with an increasing conversion ratio. At the larger conversion ratio of $M = 3.3$, the gain margin decreases with increasing

load current; however, for all other conversion ratios the gain margin stays relatively constant. This is possible since the slight increase in phase margin indicates that the zero frequency crossing occurs at a point with a small phase slope. It is likely, therefore, that the zero crossing also occurs just before a rapid decrease in phase (which would be caused by the high-frequency pole in this design). Since the phase margin is hovering around a value of 50°, the phase just needs to shift by that much to hit the 0° phase point. Since the gain plot will not exhibit a decrease in gain due to a pole until the phase has shifted by 45°, this causes a low value for gain margin. That said, the minimum gain margin shown for any corner in the DCM case is roughly *twenty times* larger than the *largest* gain margin in the CCM case!

Finally, the DC Gain plot in Figure 5.20 shows an almost complete invariance to component values and has a value in all instances around $55\,dB$. This shows the versatility of the DCM converter in that it can achieve the same level of steady-state error rejection over a wide range of operating regions.

5.3 Performance Comparisons

The difficulty of controlling a CCM converter presents many stability issues, as shown throughout this chapter. It takes a lot of design effort to create a controller that can achieve an acceptable amount of steady-state error rejection (DC Gain), speed (Bandwidth), and stability (Phase/Gain Margin). Even with a very careful design and very high tolerance controller components (which is unlikely in an integrated circuit), the external component variations can have a detrimental impact on converter performance which limits the effective operation range.

The DCM converter, in contrast, exhibits significantly less performance degradation with parameter variation. In addition, the design of the controller itself requires fewer components and is less susceptible to cause instability due to the simple single-pole nature of the DCM converter itself. This makes VMC Boost Converters significantly more desirable for mobile integrated circuit applications where external components can have large tolerances and where the operating range must be rather wide in order to function correctly in different conditions.

Chapter 6

Stability Measurement Techniques

The ability to accurately measure the stability of a DC-DC converter is vital in not only correlating hardware with simulation, but also in gauging the viability of design inclusion in a commercial product. Unfortunately, traditional analytic methods of measuring loop stability involve physically 'breaking' the loop and applying a test signal to one end and calculating the return signal. In a switched DC-DC converter, this is simple not possibly due to the large loop gain that serves to correct any variations from the steady-state value. By breaking the loop, the steady-state operating point will become disturbed and the very small difference in operating points will cause the high-gain controller to ramp up and saturate at its supply voltage, rendering the converter useless.

In 1975, Middlebrook proposed a method to deal with this problem [32]. Instead of breaking the loop to apply the test signal, the signal would be injected at a point where it would be functionally equivalent to breaking the loop. This will be described more thoroughly in Section 6.2.

Middlebrook's method for determining loop stability is very attractive, but it is limited by the need for certain impedance assumptions to hold true. To circumvent this, simple transient responses can be measured and the stability can be ascertained from the step and/or impulse responses [33]. This transient behavior can also be used to obtain freqeuency response characteristics by means of cross-correlation and system identification [34, 35].

6.1 Step Response

Transient step responses are very important waveforms to observe when trying to determine the stability of any closed-loop system, let alone a switched converter. The reason is because unlike traditional AC-Analysis methods, it does not rely on circuits operating in some linear region: it just shows you *exactly* how the circuit will behave given some stimulus. As such, it's an important type of measurement that should be discussed before analyzing any other methods.

Switched DC-DC Converters are usually designed to operate within fairly large regions. This may include a variety of input voltages, output voltages, load currents, or any combination of all three. As such, there can be *many* different combinations that could cause instability.

One of the simplest ways of testing supply stability is by stepping the load [33]. This is done by quickly changing the load current so as to put strain on the converter and force it to rise back up to a stable state. This can be done quite easily with modern test equipment, such as a Keithley 2400 SourceMeter SMU. By stepping the load from some point near the minimum load operating range to the maximum load current, a step response can be recorded on an oscilloscope and captured for analysis.

The type of step response that the converter exhibits offers some insight as to its

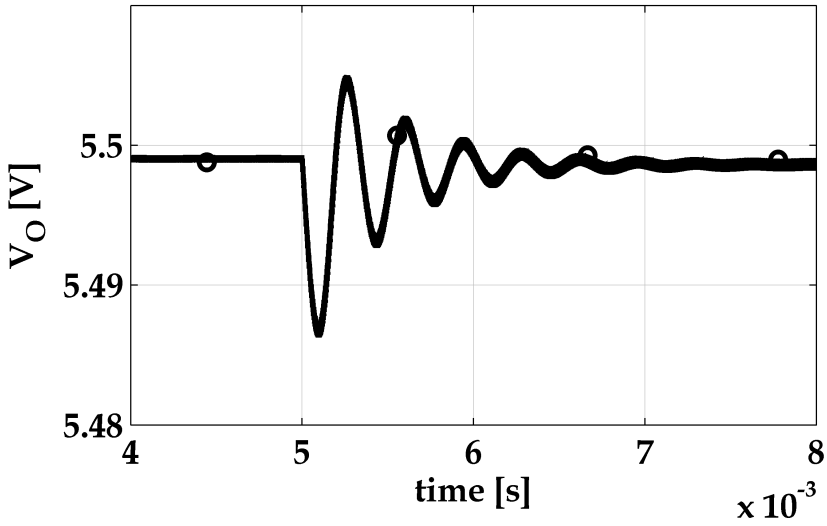

Figure 6.1: DCM Boost Converter Load Step from 10 mA to 20 mA with an Underdamped Step Response

stability. Figure 6.1 shows the response for a Boost Converter in what is known as an underdamped condition (the thick waveform is due to the high-frequency-switching). Intuitively, the more 'ringing' the waveform exhibits, the less stable the converter. Figure 6.2 shows an overdamped case where there is no ringing and the converter takes a longer time to increase to its steady-state voltage

Unfortunately, the amount of ringing that the converter exhibits is just about all the information that can be garnered from a step response. While it offers insight into the stability, it provides no insight as to what the phase margin may be nor what the frequency response actually looks like. This requires the designer to manually observe the response and deem it either acceptable or unacceptable in terms of stability which is very difficult, if not impossible, for products meant for mass production. As another downside to using this method, it is possible that the ringing exhibited by the controller can be 'buried' in the switching noise from the converter. As such, at a large voltage scale (on an oscilloscope), it's possible that the converter response *appears* stable when, in fact, there could be a significant amount of ringing.

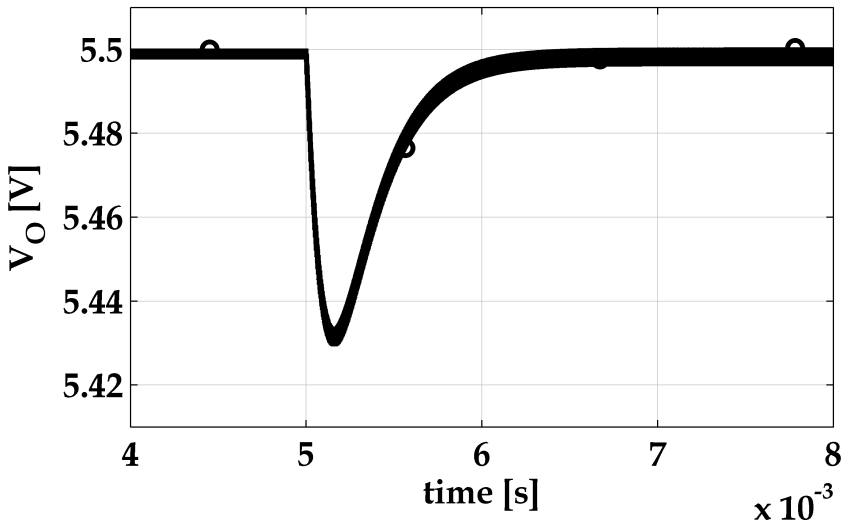

Figure 6.2: DCM Boost Converter Load Step from $10\,mA$ to $20\,mA$ with an Overdamped Step Response

6.2 Frequency Response

The frequency response, unlike the step response, provides much more information about the circuit under test. Characteristics such as resonant frequencies, phase margin, and gain margin can all be extracted from a frequency response which allows a quantitative measure of the stability of the system as opposed to simply comparing waveform shapes or observing the number of peaks that a step or impulse response has.

Unfortunately, the ability to accurately measure the loop gain and phase of a switched converter is dependent on a few criteria:

- The feedback loop is not broken.
- Measurements are made with high-accuracy equipment.
- Injected signals do not alter the steady-state operation of the converter.

6.2.1 Injecting a Voltage

Injecting a voltage signal without disturbing the steady-state characteristics of the converter was first described in Middlebrook's paper in 1975 [32]. In normal AC circuit analysis on a closed-loop system, a point within the loop is broken in order to apply a test signal. The transfer function of the circuit is then characterized by the ratio of the return signal, V_r, to injected signal, V_i. Since these two potentials exist on either end of the point at which the loop was broken, as shown in Figure 6.3, it can be said that $T(s) = \frac{V_r}{V_i}$.

However, as previously mentioned, breaking the loop within a switching converter (or any system with large loop gain) is not possible without disturbing the steady-state operating point. To alleviate this problem, Middlebrook proposed injecting the voltage in series with the loop, as shown in Figure 6.4. Since this voltage will still have a potential at the injection node of V_i and a return potential of V_r, this method is functionally equivalent to physically breaking the loop while keeping the steady-state operation undisturbed (besides the injected signal, of course).

Unfortunately, there is a *caveat* to this approach: the equivalent impedance at the positive injection node must be greater than the equivalent impedance at the

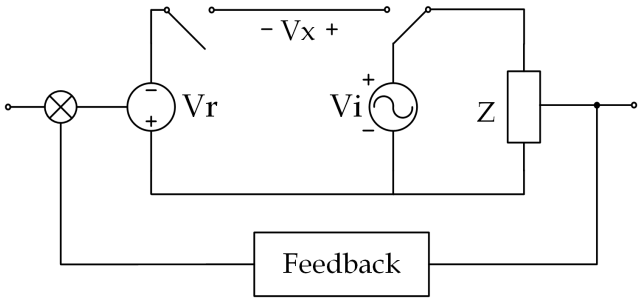

Figure 6.3: Voltage Injection via Opening the Loop (Adapted from [32]).

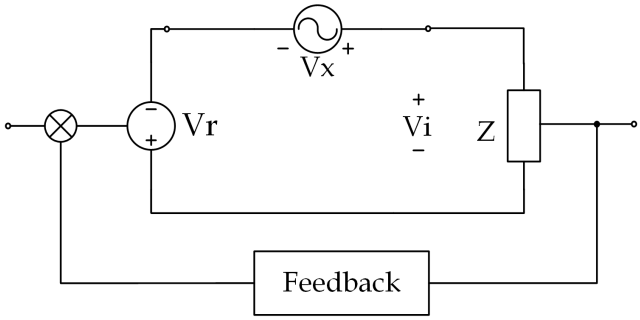

Figure 6.4: Voltage Injection via Middlebrook's Method.

negative injection node. This means that the return signal should be located at a node that approximates to an ideal voltage source. Fortunately, such a point exists on a switched converter between the output of the power conversion stage and the input of the resistive feedback string. Being a voltage source, the output impedance of the conversion stage is very low while the resistive feedback string is, typically, on the order of Meg-Ohms of resistance. As such, it is the ideal place for voltage injection via Middlebrook's method.

6.2.2 Injecting a Current

In the same paper, Middlebrook also proposed current injection as opposed to voltage injection. Similarly to the voltage injection method, the transfer function is characterized by the ratio of the return signal, I_r, to the injected signal, I_i. Since this causes a third current I_x, it's possible to simply apply a known current as the test signal at I_x and measure the current at the injection and return branches to extract the transfer function. Again, however, there is a *caveat*: the impedance at the injection branch must be much less than the impedance at the return branch. The reason for

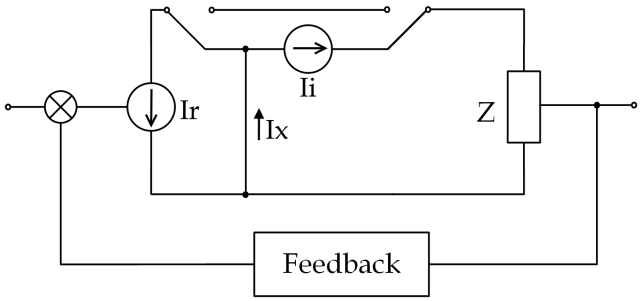

Figure 6.5: Current Injection via Opening the Loop (Adapted from [32]).

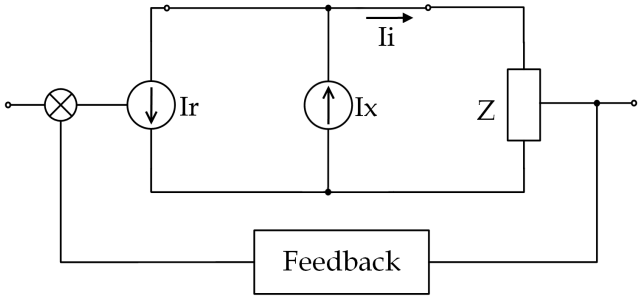

Figure 6.6: Current Injection via Middlebrook's Method.

this, much like the reasoning for the voltage injection, is that the return branch must approximate to a current provided by an ideal current source. As such, an adequate injection point would be at the output node of an OTA which has very large output impedance as it is, essentially, a voltage-controlled current source.

6.2.3 Response Measurement

The easiest way to measure the frequency response via Middlebrook's Method is with a Frequency Response Analyzer (FRA) [44]. These analyzers provide an oscillator output that can sweep through frequency ranges and can make very precise voltage measurements at the frequency being swept which allows for very accurate magnitude and phase plots of the converter under test.

In order to apply the voltage injection, the source should be isolated from the circuit through an isolation transformer. Since the positive and negative leads of the source cannot be placed at the same node, it must be applied across some injection resistor that is placed in series with the loop. This can be done in the resistive feedback string of the switched converter with no penalty on converter performance

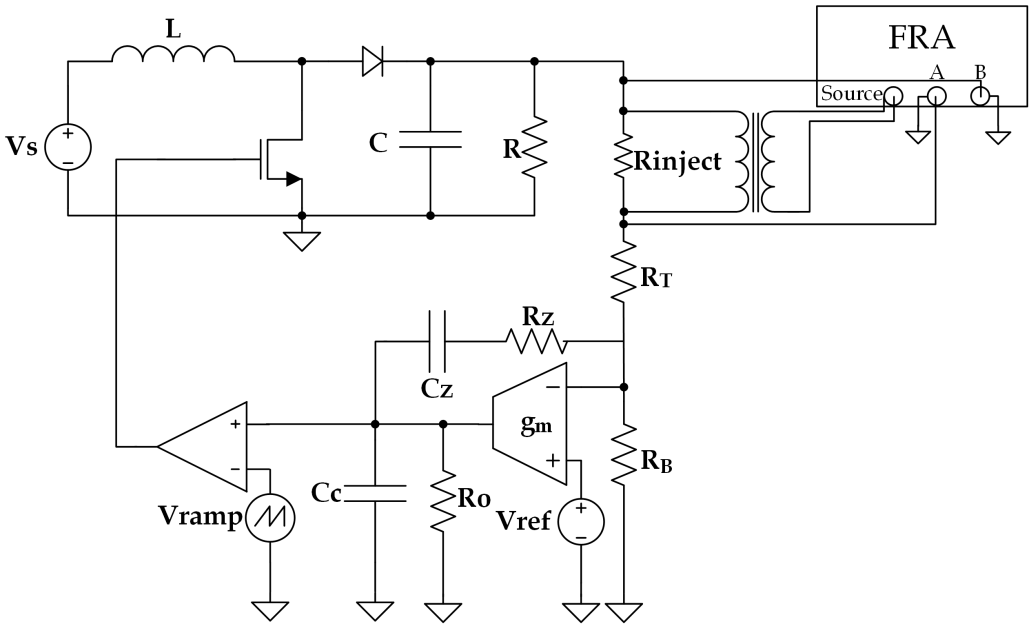

Figure 6.7: Voltage Injection Test Setup.

since the injection resistor will be in the tens-to-hundreds of Ohms range while the feedback string value is orders of magnitude greater. Figure 6.7 shows the required test set-up for frequency response analysis of a switched converter.

6.3 Frequency Response via Cross-Correlation

The idea of using Cross-Correlation as a way to extract the frequency response of switched DC-DC converters is the subject of much research [34–41]. The idea is attractive as it provides the ability to have a BIST circuit on chip which would allow for automated frequency response testing. While the design and implementation of such a circuit fall beyond the scope of this thesis, the underlying principles will be described here.

6.3.1 Cross-Correlation

Cross-Correlation is a statistical process relating the correlation between two signals. Autocorrelation is simply the cross-correlation of a signal with itself. For continuous

systems, the cross-correlation of signals $x(t)$ and $y(t)$ are given as:

$$R_{xy}(t) = \int_0^\infty x^*(\tau)y(t+\tau)\ d\tau \tag{6.1}$$

However, it is highly likely that the signals will be quantized before any cross-correlation operation occurs so (6.1) must be modified in order to hold true for discrete sets of data. Such an equation is given in (6.2).

$$R_{xy}[m] = \sum_{n=1}^{\infty} x[n]y[n+m] \tag{6.2}$$

In order to use the cross-correlation method of determining a system's frequency response, an assumption must be made that the converter is an LTI system for small output disturbances. With this assumption, the sampled converter can be described by (6.3) where $h[k]$ is the converter's sampled impulse response, $x[k]$ is the control signal, and $v[k]$ is representative of any disturbances in the system, as reported in [34, 36])

$$y[n] = \sum_{k=1}^{\infty} h[k]x[n-k] + v[n] \tag{6.3}$$

Using (6.3) and plugging it in for $y[n+m]$ in (6.2) yields the cross-correlation of the control and output signals:

$$R_{xy}[m] = \sum_{n=1}^{\infty} h[n]R_{xx}[m-n] + R_{xv}[m] \tag{6.4}$$

If the assumption is made that the input control signal, $x[k]$ is white noise, the autocorrelation of this signal is given by an ideal delta function, $\delta[m]$ and the cross-correlation of this noise with external disturbances must be zero since it implies that $x[k]$ and $v[k]$ are statistically independent. Thus, using white noise as $x[k]$, the cross-correlation of $x[k]$ and the converter output, $y[k]$, is simply the discrete impulse response of the system:

$$R_{xy}[m] = h[m] \tag{6.5}$$

By taking the DFT of this cross-correlation, the transfer function of the system can be extracted which allows for the loop gain and phase to be plotted.

6.3.2 Pseudo-Random Binary Sequences (PRBS)

A popular way to generate noise, especially in digitally controlled converters, is through the use of PRBS. These binary sequences have a length as a function of how many bits they contain. For an n-bit converter, one period of the PRBS is given by (6.6) where f_k is the clock frequency of the PRBS circuit which is typically set equal to the switching frequency of the DC-DC converter [36].

$$T_{PRBS} = \frac{2^n - 1}{f_k} \tag{6.6}$$

Figure 6.8 shows an example implementation of an 8-bit PRBS generation circuit and Figure 6.9 shows the output waveform after start up for a small sampling of the PRBS period.

As mentioned previously, white noise has an autocorrelation equivalent to that of an ideal delta function. Therefore, in order for a PRBS implementation to be

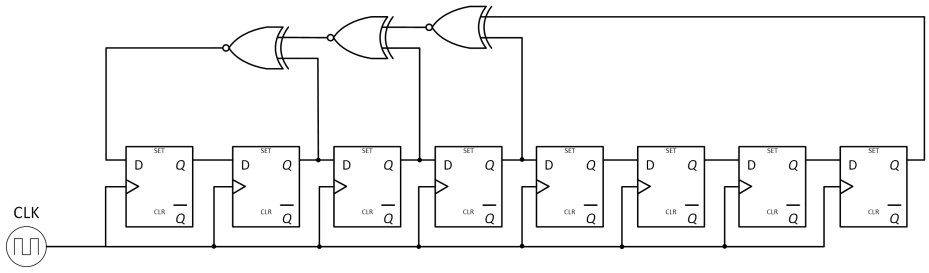

Figure 6.8: 8-bit PRBS Circuit.

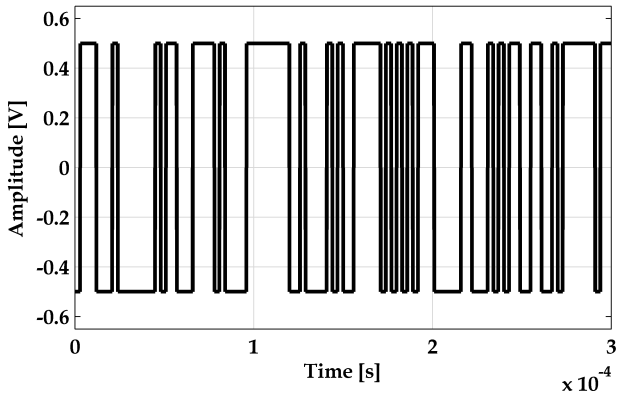

Figure 6.9: 8-bit PRBS Signal.

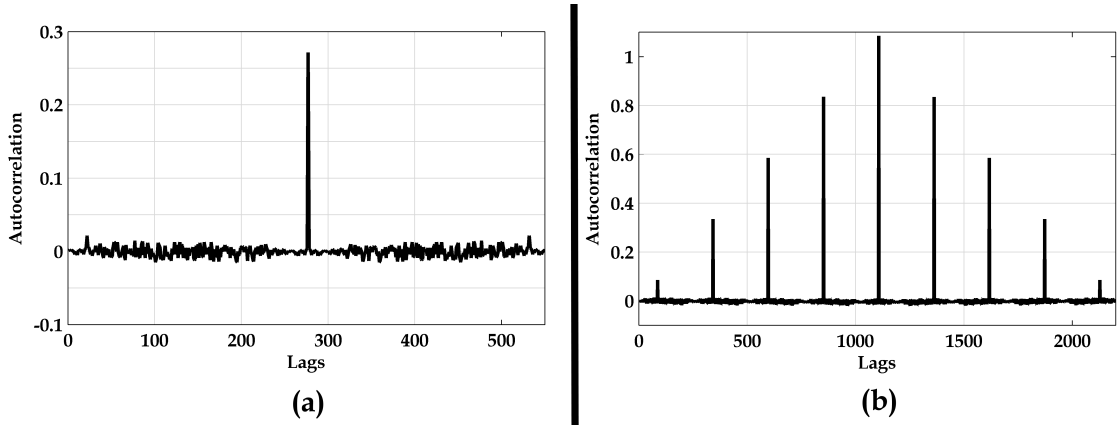

Figure 6.10: Autocorrelation of (a) Single-Period 8-bit PRBS, and (b) Four-Period 8-bit PRBS.

appropriate it must also have an autocorrelation that is approximately equal to a delta function. This is proven in Figure 6.10a. Of course, the autocorrelation of the PRBS can not be exactly equal to an ideal delta function since it does have some periodicity, but it is a good approximation. The correlation 'noise' around the approximate delta function in Figure 6.10a causes frequency response measurement errors which negatively impact the accuracy of this type of modeling.

As a solution to this problem Botao Miao *et al.* proposed sampling the output of the converter for a duration of N-PRBS periods and averaging the cross-correlations in order to obtain a more accurate frequency response measurement [34]. The reason this implementation is preferred is most easily explained by viewing Figure 6.10b which shows the autocorrelation of four periods of an 8-bit PRBS. The amplitude is noticeably larger than that of the single-period PRBS autocorrelation which provides a better approximation to an ideal delta function which has an infinite amplitude. In addition, the correlation 'noise' on each side of the approximate delta functions is much smaller which, again, provides a better approximation to ideal delta functions which have zero-amplitude at all locations besides the location of the impulse itself.

6.3.3 Implementation of a PRBS Cross-Correlation Method

In order to properly implement a stability test method that utilizes a cross-correlation and PRBS, the PRBS circuit itself must be injected at a proper point. Since the goal is to use the PRBS to modulate the duty cycle of the converter, the most logical place

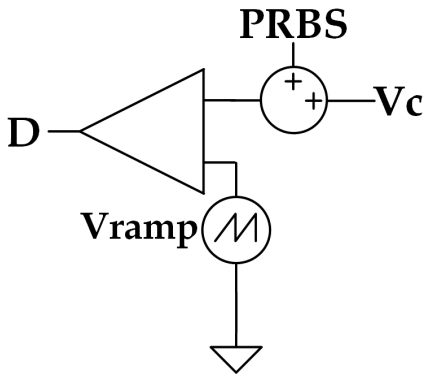

Figure 6.11: Injection Point for PRBS in a Switched DC-DC Converter

to inject the signal is into the input of the PWM Generator. This is done as per the circuit in Figure 6.11

The digital PRBS can be superimposed on the analog V_c signal since all the PRBS will do is slightly modify the error voltage at the input of the comparator. As far as the converter itself is concerned, this just appears to be noise that is modulating the duty cycle. The only requirement is that the amplitude of the PRBS signal be constrained such that it does not alter the steady-state operating point of the converter.

Once the PRBS signal is injected into feedback loop of the converter, providing the ability to measure this signal is the required next step. If post-processing of data is possible in a given test environment, the simplest approach would be to place a pin at the output of the PRBS circuit as well as the output of the converter itself and externally sample the signals.

If externally sampling the signals is a non-ideal approach given a particular test environment, another option would be to stream the data to internal memory and use dedicated circuitry to cross-correlate and possibly perform the required DFT as well. From here, the information can be streamed to external measurement equipment. This sort of implementation is rather costly in terms of required design effort as well as in physical chip area. Designs that utilize this type of method are typically done with FPGAs [34, 35, 37, 38] which are, rather obviously, impractical for mobile integrated circuit applications.

6.4 Stability Measurement Comparisons

The method of testing stability by way of cross-correlation is quite appealing due to the ability to have on-chip BIST capabilities. The task of any external equipment would be to simply sample the PRBS and output signal and perform the cross-correlation and DFT. This form of measurement is very methodical and can easily be automated which helps eliminate user error.

A large negative, however, is that the data must only be correlated across a known number of PRBS periods. In addition, if the converter does not settle within one PRBS period (which is a distinct possibility for low-bit PRBS circuit), the ensuing frequency response data will be inaccurate.

Middlebrook's method, however, simply measures the converter 'as-is'. It does not rely on correlation functions nor any form of transform; it simply sweeps the frequency of an injected voltage, measures the return signal and plots the results. The obvious downside is the lack of automation available since, ultimately, the waveform must be manually captured and stored.

As mentioned earlier, the manual capture of data could have a negative impact on testing time if the frequency response data is required for a product in mass production. The benefit over cross-correlation, however, is the ease of implementation and accuracy of the results.

Chapter 7

Conclusion

Boost converters operated in VMC-CCM benefit from enhanced efficiency and are able to handle larger loads, but suffer from a control standpoint due to the presence of a conjugate pole in its small-signal transfer function. Boost converters operating in VMC-DCM, on the otherhand, have a much simpler transfer function and are much easier to control as a result.

An implication of the control issues associated with VMC-CCM boost converters is that in order to achieve an acceptable DC-gain and phase margin, the crossover frequency must be small, which results in a slow converter. This can be problematic for applications that require high response speeds as the converter may never reach a steady state before critical events occur which can result in circuit malfunction. Thus, VMC-DCM boost converters become more palatable as a power conversion architecture despite the limited load they can handle. By utilizing such an architecture, the required control circuitry can be minimized and the converter as a whole can achieve high DC-gains and large phase margins with a minimal impact on speed.

Ensuring the stability of the converter is important, and observation of the frequency response is critical if stability in all operating regions must be guaranteed. Observation of the step response provides some insight as to whether or not the converter is stable, but it does not offer any quantifiable frequency-response data that can be compared and validated against simulations. Measurement of loop gain and phase can easily be done with external equipment, or with internal circuitry by cross-correlating the output signal with injected white noise.

7.1 Future Work

VMC-CCM boost converters have very non-ideal frequency response characteristics; however, CMC-CCM boost converters behave similarly to VMC-DCM in that no conjugate pole exists. As such, it may be possible to use a combined VMC/CMC approach in order to design a boost converter that transitions seamlessly between CCM and DCM with no performance degradation.

Cross-correlation by means of PRBS injection is a very promising stability analysis technique that could be implemented in a BIST circuit for an integrated circuit. The design and implementation in silicon would help to verify the viability of such a technique as well as help to characterize some of its limitations.

Appendices

Appendix A

Use of Optimization Algorithms in Controller Design

Switched DC-DC converters have many frequency response characteristics that must be optimized in order to produce the best product and eliminate stability concerns. As shown throughout Chapters 4 and 5, the design of the error amplifier is critical as it determines the steady-state accuracy, response time, and stability margins (both gain and phase). Unfortunately, amplifier design is not trivial as improving one performance metric will, typically, decrease another. For example, in order to increase the phase margin of a system, one must typically lower the gain in order to compensate. While this would improve stability, it would also decrease steady-state accuracy.

Due to this complexity, switched converter controller design is well suited to solving via optimization algorithms. Electronics design via optimization algorithms is a well-established field of research and shows promise in providing optimal solutions for high-complexity design [49, 50, 53, 55, 57–62]. Two algorithms explored here are Genetic Algorithms (GAs) and Particle Swarm Optimization (PSO).

Both algorithms attempted to optimize the transfer function of a controller by iterating over the parameters R_O, R_T, the number of poles and zeros, and the coefficients of the transfer function. Both algorithms operated on the results of the controller transfer function multiplied by the DCM Boost Converter transfer function (presented previously in Chapter 3).

A.1 Genetic Algorithms

The basic flow of a GA is to initialize a population with random values and evaluate each member of the population against some fitness criteria. Once this is done, the best performing members then 'mate' wherein random 'genes' are selected from each participant and crossed over to produce children that populate the next generation. During this crossover period, there is a a small chance of gene mutation which helps to add variability into the gene pool which serves to eliminate localized convergence problems.

There are many different GA implementations, but the one analyzed here is known as the 'Queen-Bee' method [52, 59]. Figure A.1 shows the flow of a Queen-Bee-type GA (abbreviated as QBGA).

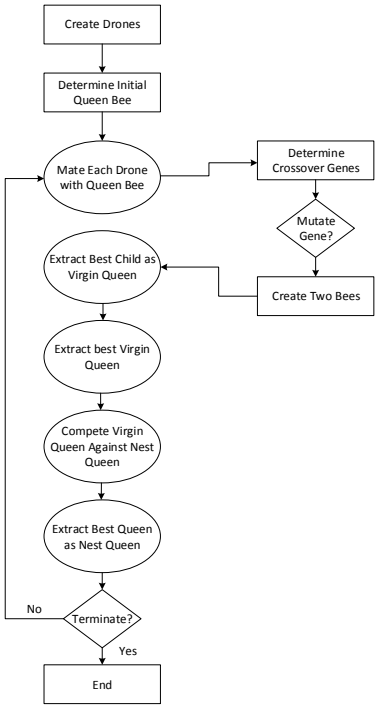

Figure A.1: Block Diagram for a Queen-Bee Genetic Algorithm for Optimization of Switched-Converter Controller Transfer Function.

A.1.1 Queen-Bee Genetic Algorithm (QBGA)

The QBGA is an algorithm based around the interactions of bees in a hive. Essentially, there exists a single queen with which all other bees, known as drones, mate. Occasionally a female bee is produced that ousts the current queen and becomes the new queen.

To implement this in software, drones are created with completely randomized genes. As an initialization stage, each drone competes with each-other in a tournament-style fashion and whichever is the best is selected as the queen.

Next, all of the drones mate with the queen and produce two offspring. To do so, a set of genes are randomly selected from each bee's chromosome and crossed over. If the selected genes are grouped into a category called 'A' and the ones not chosen are in 'B', one offspring will receive the 'A' group from the queen and the other will receive it from the drone. The remaining genes are taken from group 'B' of the *opposite* parent. These two offspring then compete with each other and the best survives.

Once each drone mates with the queen, there should be N offspring for N drones. Thee offspring then competes with each other and the best is selected as a 'virgin queen'. This virgin queen then competes with the current queen and whoever is the best proceeds on to the next generation as the nest queen. This process then repeats with randomized drones.

However, during gene crossover, it is not sufficient to *only* crossover the genes as there must be some probability of gene mutation in order to guarantee variability in the gene pool to avoid converging on local optima. To do so, most algorithms implement a constant that determines the gene mutation probability [52, 53, 59].

In order to speed up convergence, a variable mutation probability was used in this implementation based on the age of the nest queen as an alternative to simply choosing a constant. As the nest queen moves from generation to generation, it is likely that the QBGA has either converged on the best solution or it could be stuck on a local optima. By setting the mutation probability as a variable based on how many generations the nest queen has existed for, more and more variability will be introduced into the gene pool. The goal here is to attempt to push the algorithm out of any potential locally optimal points. If the program has, in fact, found a global

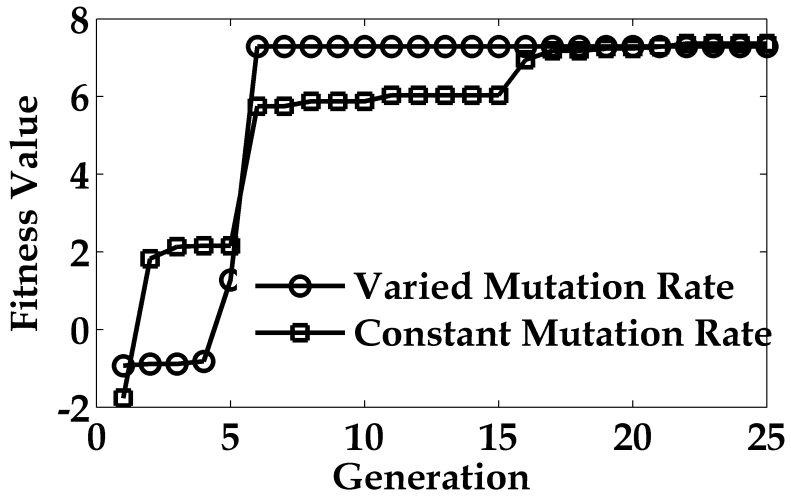

Figure A.2: Comparison of QBGA Convergence with a Varied and Constant Rate of Mutation.

optimum, then an increased mutation rate should have no effect on the solution. The pseudo-code for such a mutation algorithm is described below:

Algorithm A.1: Variable QBGA Mutation Based on Queen Age

```
for gene in crossover do
    if rand() ≥ C*queenAge then
        gene = mutate(gene);
    end
    crossover[i] = gene;
end
```

By setting C to some fractional value, it will eventually converge to have a 100% mutation rate when $\frac{1}{C} = queenAge$. However, this value *must not* be set too high as otherwise the GA will mutate too quickly and have difficulty converging on a solution. It is recommended to set the value between 0.05 and 0.2 for best results.

A comparison of convergence rates for the QBGA with and without the variable mutation rate is shown in Figure A.2. Here it takes only six generations for the varied mutation rate implementation to converge while it takes *twenty-one* generations for the constant rate of mutation implementation to converge to the same fitness value. This indicates that the variable rate of mutation does, indeed, aid in convergence speed as expected.

A.1.2 Fitness Function

The biggest design challenge with GAs in particular is that of the fitness function [45–47, 54]. Care must be taken to add in as many variables as possible in order to eliminate the possibility of unwanted states (for example, a 90° Phase Margin but $10\,Hz$ Bandwidth). However, when more variables are added they will typically need to be weighted in order to emphasize the more important parameters of the circuit.

A way to aide in the convergence of GAs is to add a penalty to the fitness function [47, 48]. The idea is to decrease the value of the fitness function based on the region that the variable is in. For example, in order for a circuit to be stable, ϕ_M must be greater than 0°. However, in real-world circuits, having a designed $\phi_M = 0°$ is essentially equivalent to being unstable since components vary and can very easily (and likely *will*) cause the circuit to oscillate. As such, the phase margin should be designed so it is *at minimum* greater than 45°, typically. The lower the phase margin is, the more the circuit 'rings' before settling to its final value which is why 45° is typically chosen as a minimum accepted value. Thus, a penalty function could produce a value for anything below this range to cause the fitness value to decrease more rapidly the further it is away from this point.

A generalized fitness function equation with penalties is shown below in (A.1) where α is a weighted constant for variable θ and $P(\theta)$ is a function that determines the penalty associated with the solution presented by θ.

$$F = \sum_{i=1}^{N} \alpha_i \theta_i - P(\theta_i) \tag{A.1}$$

For this GA implementation, the following variables were selected for the fitness function:

- Phase Margin, ϕ_M
- Gain Margin, G_M
- DC Gain, A_0
- Bandwidth, BW

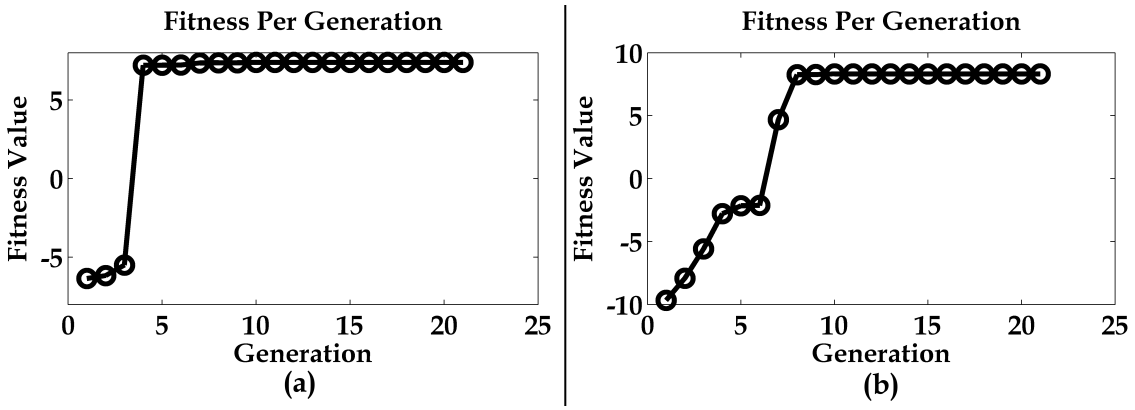

Figure A.3: Comparison of Convergence Speeds for a) QBGA with NPFF and b) QBGA with Linear Fitness.

Since each of these variables have varying sizes (ϕ_M will be in the sub-100 range while BW will get into the 1000s range) it is wise to normalize them to some ideal value such that the sum of all the ideal, normalized values is equal to the number of parameters. This makes it significantly easier to determine the necessary values for α that help to speed convergence.

In addition to normalizing all of the variables, each value was placed into a function that transforms the linear data into parabolic data such that it has a maximum at the ideal point. For example, if the ideal ϕ_M is chosen as 70°, $N_{\phi_M} = \frac{\phi_M}{70}$ and thus $f(\theta(\phi_M)) = -(N_{\phi_M} - 1)^2 + 1$. The constant scalar is there so that the maximum value occurs at a value of 1 instead of 0.

Preliminary results show that the normalized parabolic fitness function, NPFF, exhibits faster global optimum convergence than using only the normalized data alone as shown in Figure A.3. Note that the fitness value in the linear case is, in fact, larger than the NPFF case. This, however, is expected as values *greater* than the normalized ideal parameter will subtract from the fitness value in the NPFF while it adds in the linear case. As such, comparing the fitness values directly does not result in a good comparison of fitness function strength. The only valid comparison is to compare the number of generations it takes to converge.

As Figure A.3 shows, the NPFF takes a mere 4 generations to converge while it takes 8 for the linear function. The simulation was run with 30 drones per generation and a mutation rate of $0.1 \cdot queenAge$ for both simulations. The values for α were

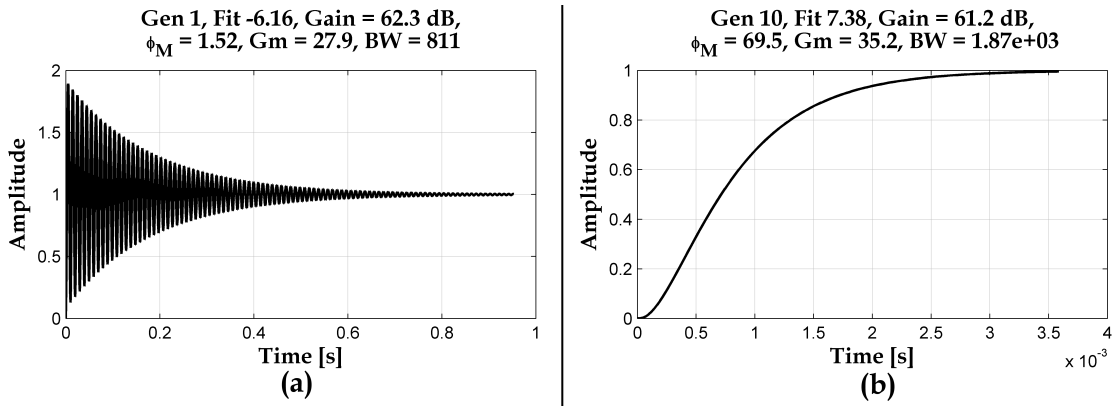

Figure A.4: Step Responses of QBGA with NPFF for a) Generation 1 and b) Generation 10.

$\alpha_{\phi_M} = 3$, $\alpha_{G_M} = 0.6$, $\alpha_{A_0} = 2$, $\alpha_{BW} = 1.8$ and were determined experimentally. Equation (A.2) shows the full NPFF used for this QBGA implementation.

$$F = \sum_{i=1}^{N} -\alpha_i (N(\theta_i) - 1)^2 + \alpha_i - P(\theta_i) \tag{A.2}$$

A.1.3 QBGA Results

The simulation of the QBGA was done on a machine with an Intel Q6600 CPU running at $2.4\,GHz$ with $4\,GB$ of DDR800 RAM at a FSB rate of $1333\,MHz$. During the simulation, output wave-forms were written to a local 7200 RPM hard disk every five generations. The QBGA had 30 drones per generation and was simulated for 50 generations which had an elapsed time of 130 seconds.

Figure A.4a shows the step response of the first generation. This response is clearly non-ideal as it exhibits ringing for almost a full second. Figure A.4b shows the step response after ten generations where it has fully converged on a solution. This response exhibits great behavior as it has a large phase margin, large gain margin, high DC gain, and adequate bandwidth.

A.2 Particle Swarm Optimization

Another type of optimization algorithm that is useful for high-complexity circuit design is PSO. Using PSO as a circuit design optimization tool has been explored

previously in [60, 61].

This method is different from that of GAs in that there are a set number of particles that have an associated position and velocity in N-dimensional space. Each particle's position is evaluated and each keeps track of its own best position. All of the best positions for each particle are then evaluated and the best global position is stored. Each particle has knowledge of its current position, current velocity, best local position, and best swarm global position. As the swarm begins to move, the velocity of the particles change based on those parameters in order to converge on a solution.

In 2002, Maurice Clerc *et al.* introduced a new way to modify a particle's velocity in order to speed convergence to a solution in [51] and which was later explored more in depth in [56]. This is done by use of constriction factor, χ, and weighted velocity constants, $C1$ and $C2$. This constriction factor serves to limit the swarm to a smaller search area as it converges on an optimal solution. The velocity coefficients of $C1$ and $C2$ are used to provide more emphasis on a particle's local best solution or the global best solution, respectively. The velocity update equation can be seen in equation (A.3) where β_p is the best local particle position, X_p is the current particle position, and G is the global best position. Equation (A.4) shows the equation to determine the new particle position. Equation (A.5) shows the equation used to calculate the constriction factor, χ.

$$V_p = \chi(V_p + C_1[U(0,1) \cdot (\beta_p - X_p)] + C_2[U(0,1) \cdot (G - X_p)]) \tag{A.3}$$

$$X_p = X_p + V_p \tag{A.4}$$

$$\chi = \left| \frac{2}{2 - (C1 + C2) - \sqrt{(C1 + C2)^2 - 4(C1 + C2)}} \right| \tag{A.5}$$

The benefit of PSO over GAs is that it is significantly easier to implement as there are no crossover probabilities, mutation probabilities, *etc.* that need to be dealt with. However, the same issues exist with fitness function creation as described in the Genetic Algorithms section which can cause a lot of design issues if not done properly.

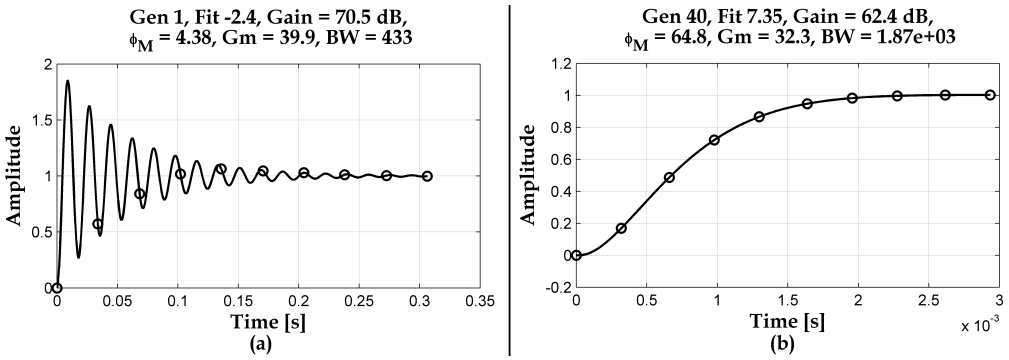

Figure A.5: Step Response PSO at a) Iteration 1 and b) Iteration 40.

A.2.1 PSO Results

The fitness function and dimensions simulated are identical in this PSO implementation to the previously described GA implementation and will not be repeated here. The values $C1$ and $C2$ were determined, through experimentation, to be 2 and 1.9, respectively. This results in $\chi = 0.95$. Now these values differ from the results found in [56], which provide an ideal $C1 + C2 = 4$. The reason that $C1 + C2$ was chosen to be 3.9 was because after thorough investigation, it was discovered that any $C1 + C2$ value above 4 would result in convergence to a local optimum while values less than 4 would slowly converge towards an optimal solution. To fix this issue, the value of 3.9 was chosen as it stays close to the ideal value of 4 while still allowing additional exploration which prevents convergence on a local optimum.

Figure A.5 shows a comparison between the step response in iteration 1 with iteration 40. Here, all parameters are quite good and it's clear that the PSO algorithm has converged on an acceptable solution.

A.3 QBGA and PSO Performance Comparison

Figure A.6 shows a comparison in the convergence rate of both algorithms. As is quite clear, the PSO algorithm takes much longer to converge than the QBGA. Both converge to similar fitness values, but the PSO takes almost 5× longer to reach the optimal value. This can be attributed in part to the constriction and velocity constant chosen but is more a testament to the robustness of the QBGA with variable mutation rate. As previously shown in Figure A.2, the constant mutation rate converges at

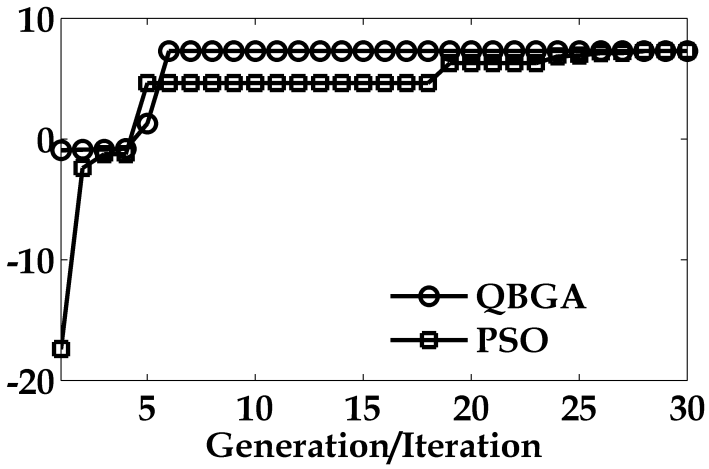

Figure A.6: Fitness Value Convergence Comparisons for QBGA and PSO

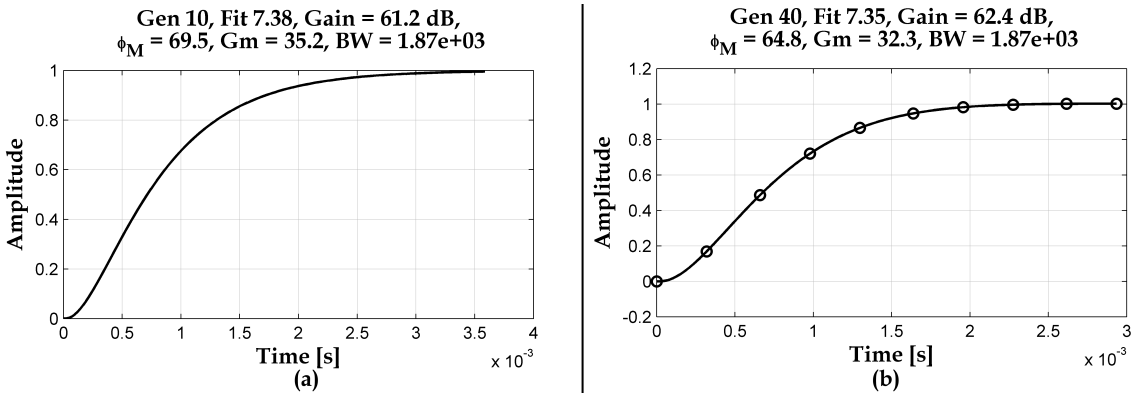

Figure A.7: Step Response Comparisons Between a) QBGA and b) PSO for Full System

nearly the same speed as the PSO here which indicates that the variable mutation has a *significant* effect on convergence speed.

As a further comparison, the step response of the full system is shown in Figure A.7. As expected, both the QBGA and PSO converge to similar solutions with relative differences of $\Delta A_0 = 1.9\%$, $\Delta\phi_M = 6.8\%$, $\Delta G_M = 8.2\%$, and $\Delta BW = 0\%$.

It is clear, after thorough experimentation, that utilizing a Queen-Bee Genetic Algorithm with variable mutation rates and a normalized parabolic fitness-function is superior to both a PSO implementation and a QBGA implementation with a constant mutation rate. The quick convergence to an optimal solution indicates that it performs well in a high-dimensional search space. This type of algorithm could benefit from additional research in order to improve functionality and efficiency.

Appendix B

Power Supply Simulation Tutorial with MATLAB®

One of the primary issues with switched DC-DC converters is the simulation time involved. There are many options outside of the classical circuit simulation software, all of which do a fine job; however, having the ability to simulate a circuit quickly and accurately within MATLAB® is a very powerful tool for a Power Supply Designer. In order to properly simulate a converter, the Simulink and SimScape toolboxes are required. This tutorial will go over the creation of a Controlled Switched DC-DC Boost Converter, but can easily be adapted for any converter topology.

1. To begin, type the command 'powerlib' into the MATLAB® command line. This initializes the tool used for circuit creation.

   ```
   >> powerlib
   ```

2. An empty window should pop up along with an array of blocks that can be used within the circuit, as shown in Figure B.1. Each block has elements associated with it. For example, the 'Electrical Sources' block has such things as DC voltage sources, Sinusoidal Sources, *etc.*

3. Open the 'Elements' box and click on 'Series RLC Branch' and drag it to the circuit window, as shown in Figure B.2.

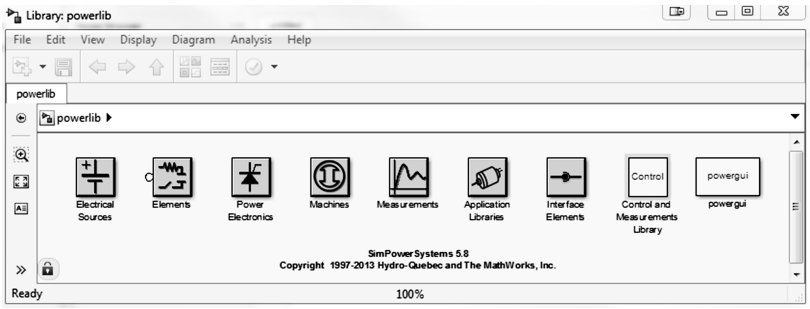

Figure B.1: Powerlib Toolbar

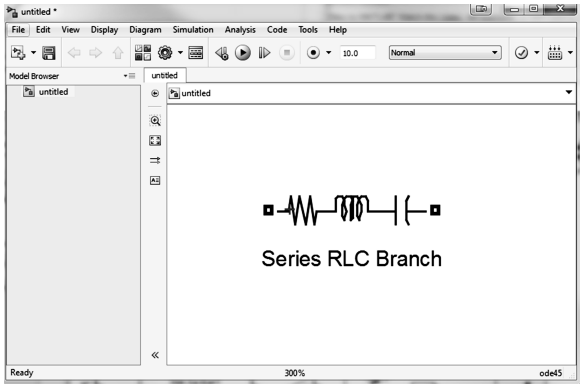

Figure B.2: Series RLC Branch

4. Double-click on the Series RLC Branch. Here, the branch type can be changed to R, C, L, or any combination of the three. This is also true for the 'Parallel RLC Branch' within the 'Elements' box.

   Select 'L' and enter the desired inductance value. The initial inductor current can also be set in order to speed simulation time, but is not a necessary parameter. This is also true for the output filter capacitor (where it is recommended to set the initial condition to the desired output voltage as this helps speed up the transient simulation tremendously).

5. Next, add in all necessary passive components using the same 'Series RLC Branch' used to generate the inductor. This includes the output filter capacitor, resistive load, and resistive feedback branch. The diode and switch can be found within the 'Power Electronics' box and the voltage supplies and grounds can be found within the 'Electrical Sources' block, as was mentioned earlier. At this point, the circuit should look similar to Figure B.4.

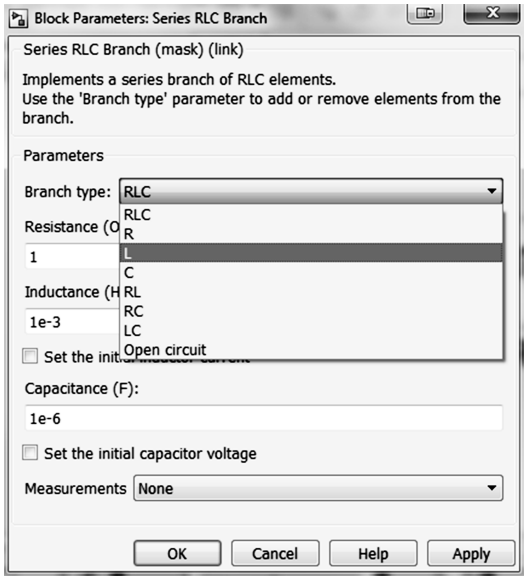

Figure B.3: Changing Series RLC Branch Parameters

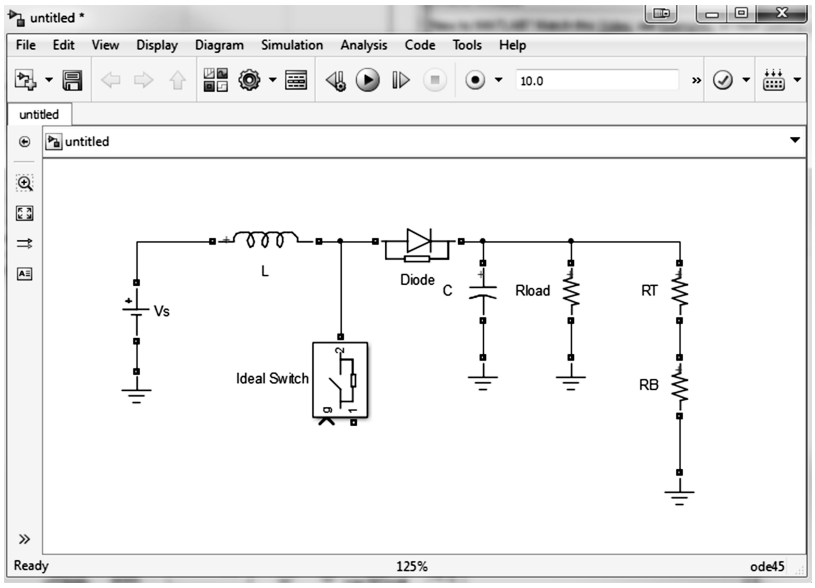

Figure B.4: Boost Converter in Powerlib (no Controller)

6. The next step is to add in the controller. Unfortunately, a model for the op-amp is going to be needed in order to properly simulate the converter. To do so, two voltage measurements are going to be needed (from the 'Measurements' box in the Powerlib tool pane) and an 'Add' block will be needed from the Simulink→Math Operations library. This is the amplifier's differential stage.

7. Once the differential stage is implemented, the controller itself must be modeled. The easiest method is to use one of the equations given throughout Chapter 4 to model the controller and implement it with a 'Transfer Fcn' block in the Simulink→Continuous library. At the output of the transfer function, it's wise to play a 'Saturation' block to clamp the amplifier so that it doesn't increase (or decrease) to unrealistic values.

8. Finally, add in the 'PWM Generator (DC-DC)' block from the 'Control and Measurements' Library within the Powerlib tool pane. The end circuit should look like the circuit in Figure B.5.

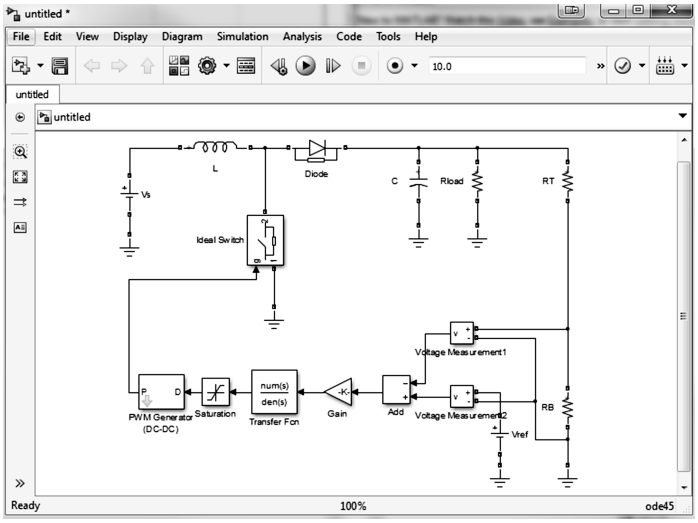

Figure B.5: Boost Converter in Powerlib

9. Now that the converter has been entered schematically within Powerlib, measurements must be set up in order to view the output waveforms as shown in Figure B.6. To do so, first place down a 'Voltage Measurement' block near the output of the converter and connected it between the output of the converter and ground. Then place a 'Scope' block from the Simulink→Sinks library and connect it to the output of the Voltage Measurement block. Finally, from the Powerlib tool pane, place a 'Powergui' block anywhere within the circuit. This is required for **all** Powerlib simulations.

10. In order to speed up the simulation as well as guarantee convergence, the simulation solver needs to be changed to **ode23tb**. This is done by navigating to the

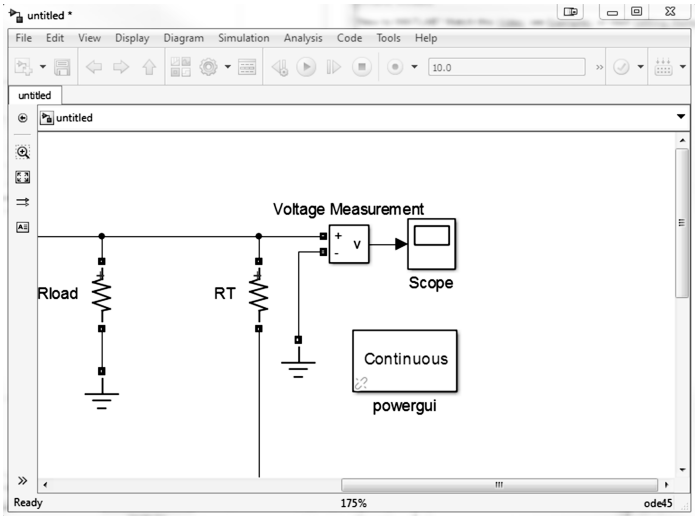

Figure B.6: Boost Converter in Powerlib Output Measurement

'Simulation' menu on the menu bar in the Powerlib schematic editor and clicking on 'Model Configuration Parameters'. This brings up a settings window, as shown in Figure B.7. Change the solver to **ode23tb (stiff/TR-BDF2)**. The stop time can also be set within this window and was set to 50 ms here.

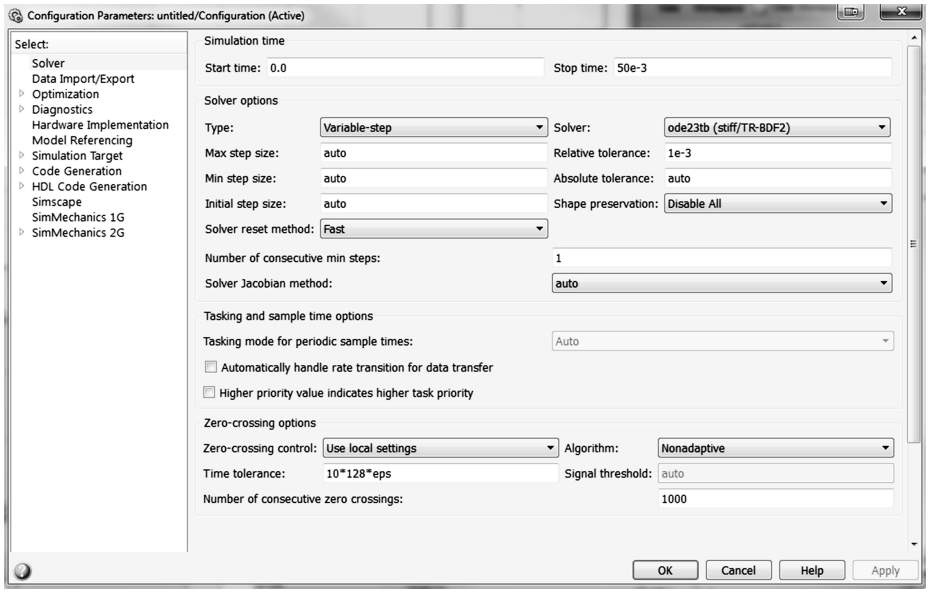

Figure B.7: Powerlib Simulation Configuration Settings

11. At this point, the simulation can be run by either clicking the green 'Run' button or by pressing **Ctrl+T**. The output waveform can be viewed by double-clicking

the scope of interest. By navigating to the scope parameters within the scope window, the data can be saved to any variable name in either a Structure or Array format. This is a useful feature that makes post-processing of data very easy.

The simulation for this particular converter took roughly $30\,s$ to simulate $50\,ms$. This is significantly faster than conventional circuit simulation software which can take $10\times$ as long, if not longer, which is what makes supply simulation in MATLAB® a very attractive option for designers.

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