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Design, development and simulation of sub-lithographic process for patterning nm scale features

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Design, Development and Simulation of Sub-Lithographic Process for Patterning nm Scale Features

A thesis submitted in
partial fulfillment of the requirements for the degree of
Masters of Science in
Microelectronic Engineering

By
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KATE GLEASON COLLEGE OF ENGINEERING
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CERTIFICATE OF APPROVAL
MASTER OF SCIENCE DEGREE THESIS

A thesis entitled

Design, Development and Simulation of Sub-Lithographic Process for Patterning nm Scale Features

by
Guriqbal Singh Josan

The Masters of Science Degree Thesis of Guriqbal Singh Josan
has been examined and approved by the thesis committee
as satisfactory for the thesis requirement of a
Master of Science degree

We the undersigned have had the opportunity to attend, question, and discuss the candidate's presentation of research results upon which this thesis is based. We believe this work constitutes satisfactory completion of the requirements for a Master of Science degree.

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Abstract

The ability to create sub-lithographic nm-scale features without the need of high-end lithography tools will create new opportunities for the electronics industry. Most current technologies are lithography dependent and inherit associated CD variations.

The mainstay of this work is mathematical modeling, simulation and verification of a revolutionary void transfer process for patterning nm scale features originally introduced by Breitwisch *et al.* at IBM. The technique studied involves intentional creation of voids using a conformal chemical vapor deposition (CVD) followed by controlled etch-back to form nanoscale pores. This method provides features that are independent of lithographically defined parent holes and exhibit lower critical dimension (CD) variations. It offers efficient low thermal budget and backend process compatible integration scheme that requires just one additional mask level. To the best of author's knowledge no simulation study of the void transfer process has been reported in the literature so far. Thus, this project initiated scores of 'firsts' towards the development of a reliable nano-patterning technique and a robust process infrastructure for future projects at RIT. The pores with diameter of 130 nm were obtained *i.e.* an impressive ~7X reduction from lithographically defined hole of 714 nm using conventional i-line lithography. Critical parameters affecting the void formation and the final pore size have been identified and modeled. Simulation of the void transfer process has been investigated using plasma etch module of 'Elite' by Silvaco that employs 2-D Monte Carlo ion transport modeling. The results of this investigation show that the geometrical design parameters can be coupled with the plasma process simulations to develop an efficient module for the void transfer process.

Dedicated to my parents,
Narinder Singh Josan and Ravinder Kaur Josan and to my wife Amandip Kaur

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CHAPTER 1

Introduction and Motivation

The relentless drive for smaller, faster and cheaper devices has pushed the existing semiconductor technology to their limits. In the past decade lithography technology has been the key driving force for the phenomenal rate of increase in the integration density of silicon-based microelectronics circuits following Moore's law. However, miniaturization based on optical lithography wavelength reduction has already hit a roadblock. There are many post-optical era lithography contenders capable of patterning down to nano-scale - such as Extreme ultraviolet lithography (EUV), Electron projection lithography (EPL), Multicolumn direct-write E-beam, Scanning probe arrays, Nanoprinting, Scattering with angular limitation projection electron-beam lithography (SCALPEL), X-ray lithography and Immersion Lithography [1-3]. The applications of these technologies may not be financially viable for small manufacturers and researchers and for products to compete in the market.

Nonetheless, the incessant appetite for the evolution of semiconductor devices has pushed researchers to look into other non-conventional nano-patterning techniques in order to understand the effects and properties at nanometer scales. Figure 1.1 shows the evolutionary trends comparing the minimum critical dimensions (CD) and wavelength of the exposure source. The slope of miniaturization trend is steeper than the rate at which exposure wavelengths have been reduced, illustrating the increasing practical importance of high-numerical-aperture (high-NA) systems, strong resolution-enhancement techniques (RETs) and/ or non-conventional patterning methods.

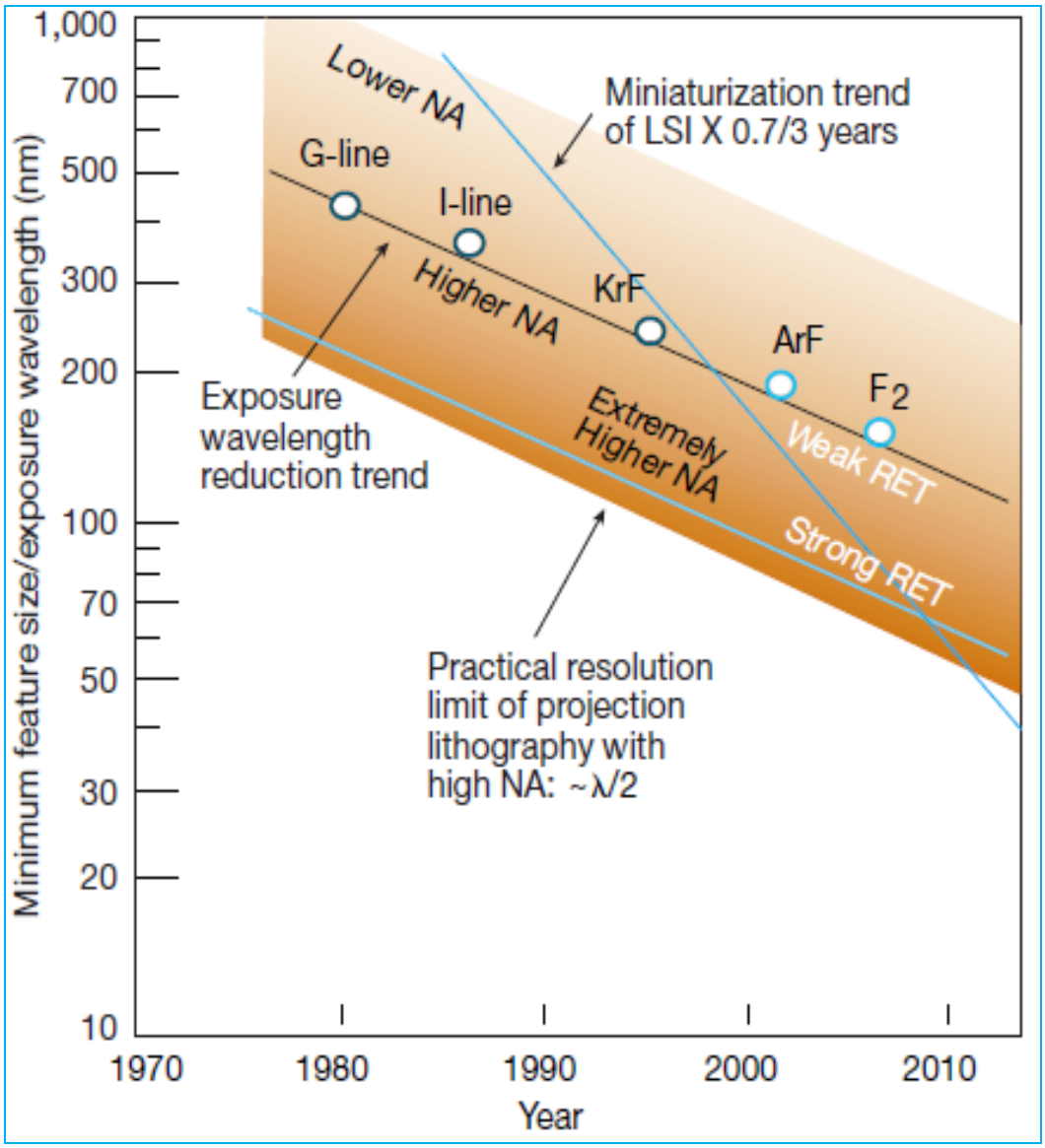

Fig. 1.1. Comparison of trends in the wavelength of exposure light and the minimum feature size [1].

1.1. Motivation

The ability to create sub-lithographic nm-scale features without the need of high-end lithography tools will create new opportunities for the electronics industry and an immense resource for future projects at RIT that require nano-features.

As the flash memory scalability is nearing its limits, the phase change memory (PCM) based on variable resistance contrast is at the forefront of research. Better performance, scalability [4], larger cycling endurance [5] and faster read/write time have been reported. However, with the projection of increasingly smaller cells for future technology, PCM technology can succeed only if it continues to promise the scaling trends for many future generations. The greatest challenge in designing large-scale PCM arrays for commercial use is the requirement of high programming current densities ($>10^7$ A/cm^2 as compared to 10^5-10^6 A/cm^2 for transistors). This means that an active area needs to be scaled much smaller than the transistor area in the driving circuit. Many recent attempts detailing feasible scaling technologies involved in realizing the prototype to large scale production of these chalcogenide based PC-RAMs have been already reported in literature [6-10]. Nonetheless, a more reliable technique to form nanometer-sized structures with the extreme scaling potential is required for the realization of such next generation nano-electronic devices.

Some of the solutions for creating features below 180 nm include x-ray lithography [11], electron-beam (e-beam) lithography [12], and focused ion beam lithography [13]. However, these techniques lack in line-width homogeneity and suffer from lower throughput. Patterning of sub-lithographic features is still feasible and economical using other non-conventional techniques such as spacer patterning technique

[14], resist ashing and trimming [15], electroplating [16] and lift-off process [17]. But, all these technologies are lithography dependent and inherit associated CD variations. This is extremely crucial for memory applications where even subtle CD variations affect vital device characteristics such as retention time and endurance.

The mainstay of this work is mathematical modeling, simulation and verification of a revolutionary '*Void Transfer Patterning Process*' for nm scale features. This process was originally introduced by Breitwisch *et al.* [18] to demonstrate a fully integrated 256 Kbit phase change memory test array with 20-80 nm pore sizes using 180 nm CMOS technology. Even though the final pore size by this method is lithography-independent, higher density of pores can be achieved as the lithography node shrinks. This process offers a simple technique for fabricating devices without the need of e-beam lithography and line width beyond the scope of optical lithography. An ability to simulate these processes is extremely important because it enables faster technology development cycles by replacing expensive wafer fabrication processes with simulations and it provides information that is difficult or immeasurable. Detailed topographical plasma simulations of reactive ion etching has been developed by Takagi *et al.* [19] by employing 'Elite' Monte Carlo etch module by Silvaco [20]. However, no simulation study of the void transfer process has been reported in the literature. In this study, simulation of void patterning technique for prediction of final feature size obtainable is investigated [21]. Thus, this project initiated scores of 'firsts' towards the development of a reliable nano-patterning technique and a robust process infrastructure for future projects at RIT.

1.2. Summary and Organization of Thesis

Various challenges dealing with mask design, process integration and the fabrication issues involved have been identified. The research objectives are outlined and rationale behind the work is elucidated. This thesis is presented in total of five chapters. Chapter 1 is an introduction and motivation section revealing the interests and demand for a reliable non-conventional patterning technique. Chapter 2 is the theory chapter and provides the literature review related to the existing patterning methods. In addition, it includes the basic theory and terminologies pertaining to the different aspects of process development associated with this work such as thin film deposition and dry etch. Chapter 3 details the process development and identifies challenges involved. Chapter 4 presents detailed analysis using process simulations and discussion of results with validation of the mathematical and simulated models. Chapter 5 gives conclusions, summary and potential applications for the void transfer process and recommendations for future work.

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CHAPTER 2

Theory

Miniaturization based on optical lithography wavelength reduction has already hit a roadblock and the changeover to newer technology is financially constrained. Figure 2.1 shows the nanotechnology roadmap since 1940's illustrating different approaches incorporated for crossover to nanotechnology. Solutions for features below 180 nm are Electron-beam (e-beam) lithography [1, 2], X-ray lithography [3], Focused ion beam lithography [4, 5] etc. But, these techniques lack in line-width homogeneity over the whole wafer, offer lower throughput, and are time consuming, complicated and expensive. Thus, their exploitation in integrated circuit processing is still putative. However, with the invention of some revolutionary techniques, patterning of sub-lithographic features is still feasible and in-fact very widely used in industry.

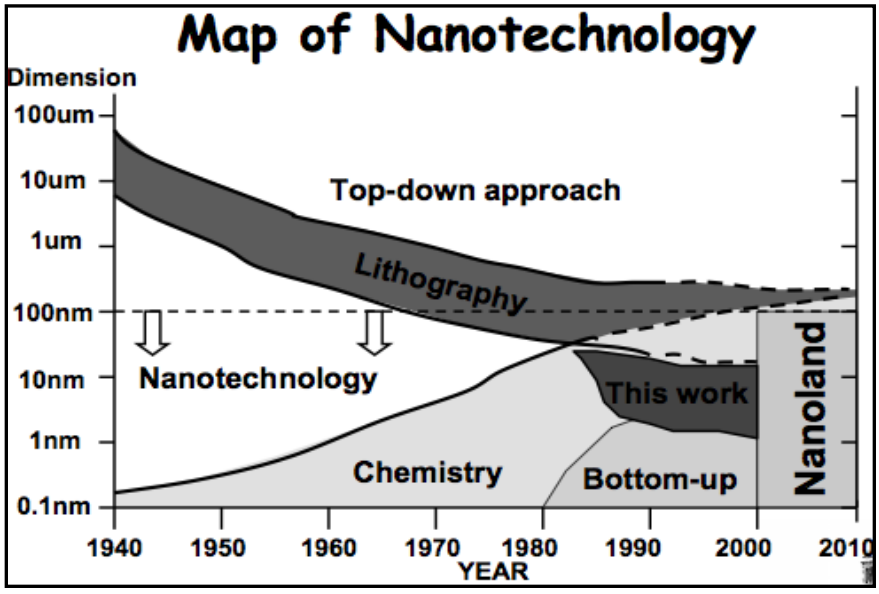


Fig. 2.1. Nanotechnology roadmap from 1940-present. The figure illustrates the possible regime for non- conventional patterning and this work. Figure adopted from [6].

2.1. Non-Conventional Patterning Techniques: A Literature Review

Some of the non-conventional patterning techniques include Spacer patterning technique (SPT) [7-9], lift off process [10], Electroplating [11] and Ashing and trimming [12]. These techniques are briefly discussed as follows.

2.1.1. Spacer Patterning Technique (SPT)

The SPT [7-9], [13] incorporating the use of conventional optical lithography, conformal chemical vapor deposition (CVD) process and the anisotropic etch back has been used successfully to pattern sub 7-nm features [7]. As seen in Fig. 2.2, it comprises of the following steps: (1) deposition of a sacrificial layer; (2) defining a vertical step by means of lithography and anisotropic etching; (3) deposition of a conformal layer; and (4) finally the anisotropic etch to get the desired sub-lithographic line.

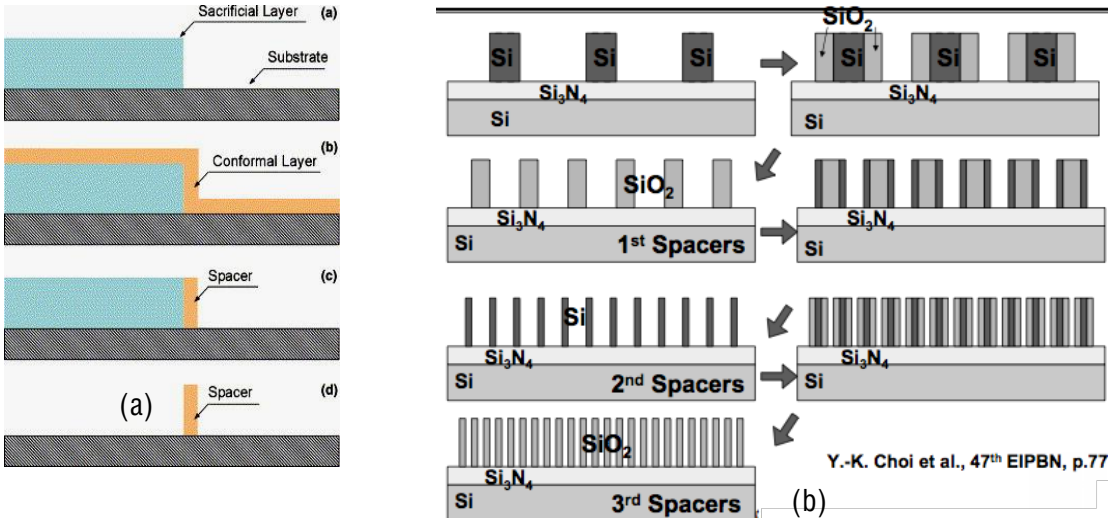


Fig. 2.2. Schematic diagram of the process flow for; a) single spacer; b) multiple spacers for nanowires [13] [6].

The final length of the transformed vertical to horizontal features can be controlled by the steepness of sacrificial layer and the anisotropy of etching. This technique offers a very good pattern fidelity, density and low CD variation and has been effectively used by Intel to produce MOSFETs with gate length of 10 nm [13].

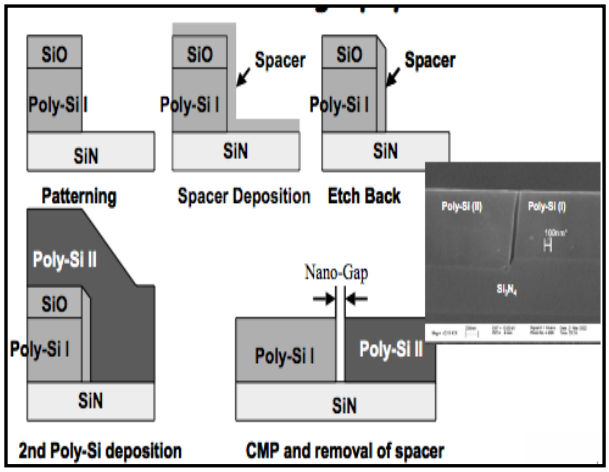


Fig. 2.3. Process flow for producing polysilicon nanogaps using spacer lithography [6].

The drawbacks of this technique are that 1) only one line width is possible and narrow width devices cannot be fabricated and 2) Pattering nanogaps and pores is possible as illustrated in figure 2.3 but involves more number of process steps and results in higher CD variations.

2.1.2. Lift-off Process

This technique combines the use of optical lithography and the metal liftoff process to form high aspect ratio line-and-space patterns. Metal electrodes with 20 nm or lesser gap have been reported by using the negative photo resist (PR) without the use of any sophisticated tools or e-beam lithography [10]. Figure 2.4 shows the process flow schematic of this process, a) Conventional lithography step, b) PMER ash using plasma

asher, c) 100 nm thick Al metal deposition using double angle deposition system to prevent shadow effects, and d) final nano-sized structure after PMMA resist lift-off.

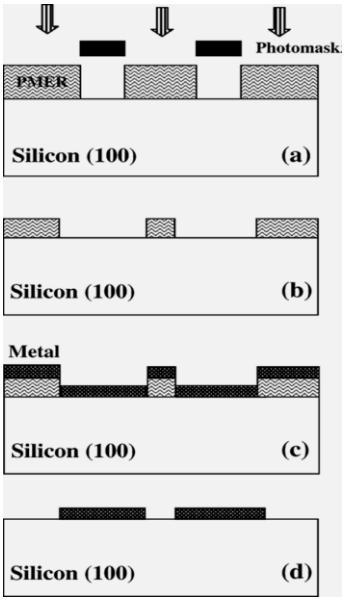


Fig.2.4. Process flow schematic: Liftoff process [10].

The aspect ratio and the resist profiles are the strong functions of resist types. Higher aspect ratios are reported by using negative tone resist systems like PMER instead of positive resists, which is extremely important for the successful lift-off process. Figure 2.5 shows the SEM image of PMER resist lines after etch and the final sub-lithographic sized feature of 20-nm formed post lift-off process. Drawbacks of this process are larger CD variations, and dependence of successful lift-off on high aspect ratios, which in turn depends on reproducibility and uniformity of resist ashing. Another disadvantage is the inability of this process to form high aspect ratio vertical structures or lines because of prematurely closing of the top opening of the structure during evaporation of metal [11].

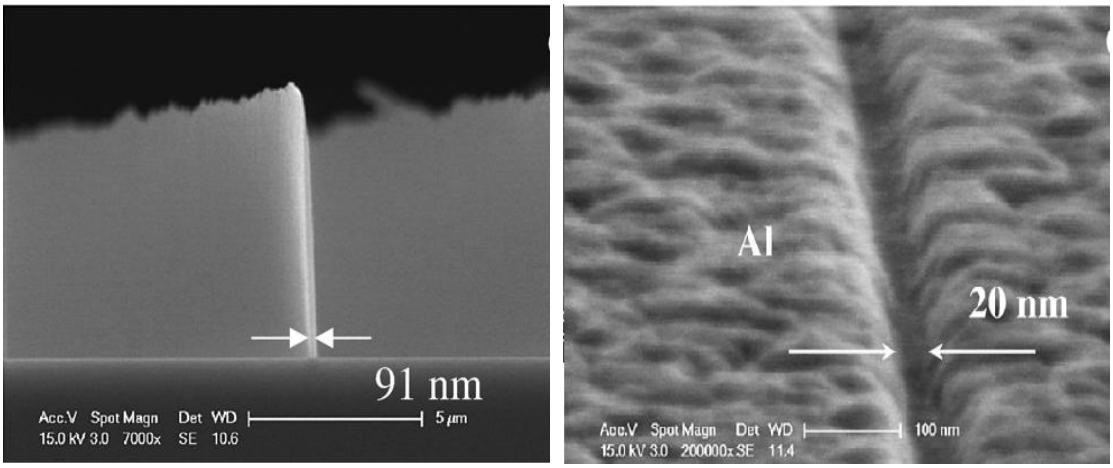


Fig.2.5. SEM micrographs showing (left) PMER line after ashing, (right) smallest 20 nm gap formed after lift-off process [11].

2.1.3. Electroplating

Electrodeposition or the electroplating is the pattern transfer technique proposed as an alternative to a cumbersome lift-off technique in the 20 nm regime for high aspect ratio vertical structures without edge defects [11]. 15 nm electroplated wires are accounted in the paper by Simon *et al.* with a high aspect ratio of ~ 10 utilizing PMMA resist and 200 KV electron beam.

The processing steps involves: 1) e-beam evaporation with 10 nm thick Cr/ 20 nm Au to form a plating base, 2) anneal the sample at 100^0 C for 30 minutes, 3) pattern the PMMA using 200 KV e-beam, 4) develop the resist using 1:3 methylisobutylketone: isopropylic (MIBK:IPA) alcohol bath at 24 ^{0}C, 5) anneal samples for 24 hours to improve adhesion of resist in plating bath and 6) finally, gold plate the samples in a cyanide bath and remove the resist. Figure 2.6 shows the CD variations as the function of electron dose for Au structures plated in 150 nm and 400 nm thick PMMA resist on bulk Si. It shows that gold cannot be deposited in resist patterns for dose lower than 2 nC/cm.

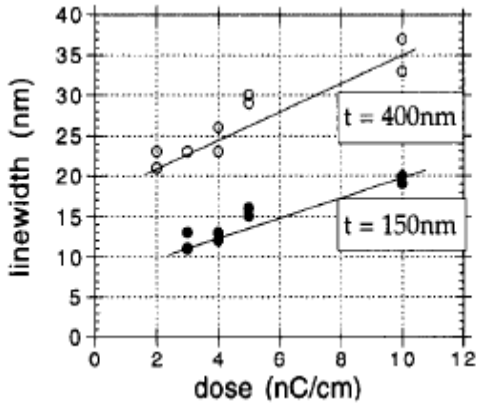


Fig.2.6. CD variations as function of electron dose for gold structures plated in 400 nm and 150 nm resist [11].

The minimum line-width is about 20 nm and 15 nm for two PMMA thicknesses. The final patterns demonstrate continuous vertical sidewalls and high resolution. Again, this technique has its own drawbacks of lower throughput and complexity involved with the use of e-beam writing.

2.1.4. Ashing and Trimming

This sub-lithographic pattern transfer technique exploits the resist ashing and oxide hard mask trimming to form sub-30 nm MOSFET gate. 25 nm pattern using i-line lithography and sub-20 nm using e-beam lithography has been reported with this technique [12]. The process steps as illustrated in figure 2.7 are: 1) pattern using conventional i-line lithography, 2) ash using oxygen plasma to trim the line width, 3) oxide hard mask trimming anisotropically to transfer the pattern to oxide layer, 4) wet etch of the oxide layer to a further trim the mask to a desired smaller size, and 5) anisotropic polysilicon etching to get the final features. This process is compatible with metal gate patterning too. The drawback includes the prerequisite of a high degree of smoothness of initial lines for good ashing results which inturn depends on the quality of

mask. Other turn-offs are lower uniformity/ reproducibility, larger line-width variations, lower throughput and inability to pattern pores or spaces on nano-length scale.

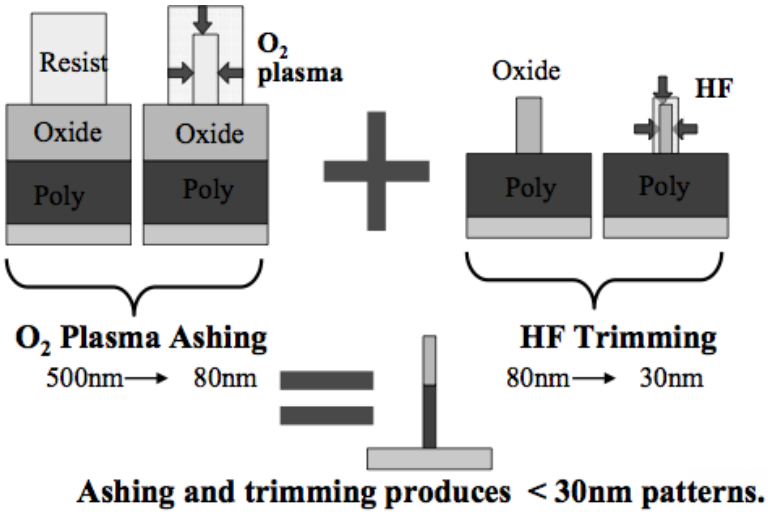


Fig. 2.7. Process flow schematic for Ashing and Trimming process [6].

2.2. Disadvantages of Existing Non-conventional Patterning Techniques

All the techniques for patterning discussed till now have their disadvantages and are not viable for patterning of densely spaced nanometer sized trenches or pores. All these attempts were more or large developed to get nm-sized lines. Spacer patterning technique can be utilized but needs increased number of processing steps using multi-spacer patterning technique as proposed by Cerofolini *et al.* and Choi *et al.* [13]. All these technologies are lithography dependent and inherit the associated CD variations. Figure 2.8 shows the CD variations for three different nano-length scale (NLS) patterning techniques discussed above. As depicted CD variation in the spacer technology is lower compared to other two. Measurements taken post spacer etch in SPT, after hard mask oxide trimming in the ashing and trimming technique, and after resist development in e-beam lithography

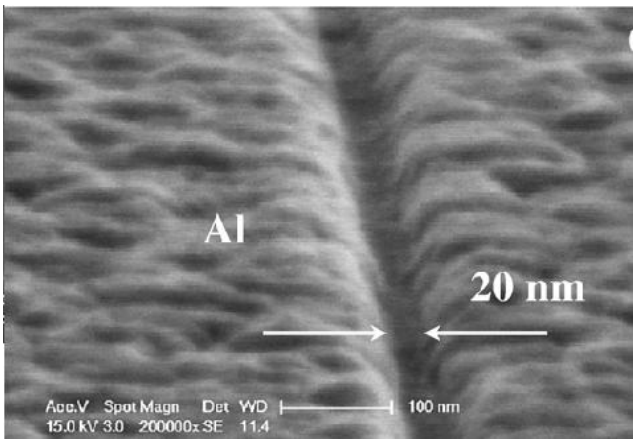


Fig. 2.8. CD variations for three different nano-length scale (NLS) patterning techniques [7].

2.3. Keyhole Patterning Technique

The lithography-independent method of intentionally creating keyhole void structures followed by an effective hard mask pattern transfer process to produce sub-lithographic features for a 'pore' phase change memory cell has been successfully demonstrated by Breitwisch *et al.* [14].

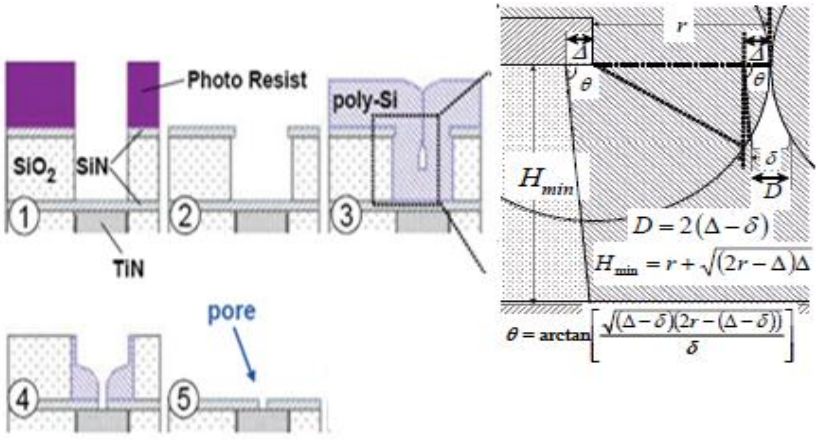


Fig. 2.9. Schematic of a process flow for a 'pore' PCM cell. Figure on right shows keyhole parameter calculations [14].

The dimensions of pore formed using conformal deposition and highly anisotropic void etch-back is independent of the original lithographically defined feature size, thereby de-coupling the pore size from lithography dependent CD variations. The actual pore diameter or the diameter of the trench feature thus formed depends on the diameter of the intentionally formed keyhole void. Thus, understanding and controlling the void formation mechanism and the basic trigonometry is helpful in developing the sub-lithographic pores of different sizes. The sequence of process steps as shown in figure 2.9 in defining the pore memory element are outlined as follows: 1) a lithography defined hole (patterned using conventional lithography) is etched-back through PECVD Nitride-SiO_2-PECVD Nitride (SiN) stack ceasing at bottom SiN, 2) a selective wet etch to create a recess in SiO_2 layer, forming an overhang, 3) a highly conformal polysilicon deposition that pinches off prematurely at top forming voids in polysilicon, 4) void etch-back to bottom SiN, and finally 5), SiO_2 and polysilicon stingers removal using wet etch. Fig. 2.10 shows the cross-sectional SEM image of the voids formed in two different sized lithographically defined holes and the etch-back process. Since, the void size does not depend on lithography, pore dimension are truly de-coupled from lithography variations.

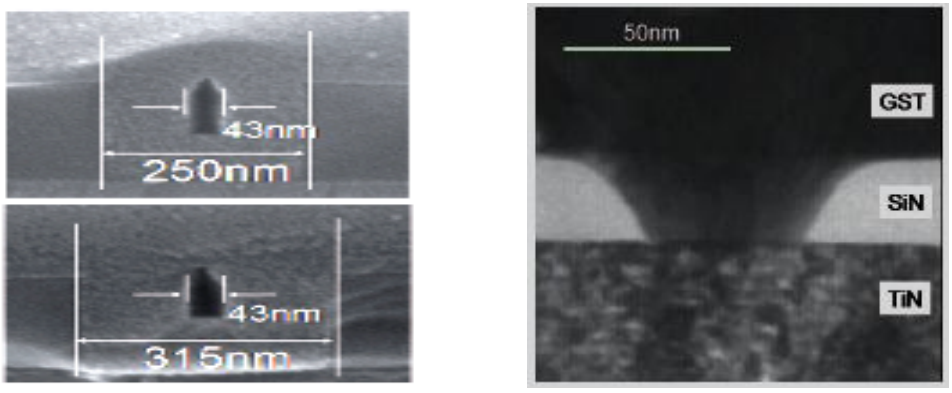


Fig. 2.10 (left) SEM cross-sectional image after step 3 in process sequence showing similar sized keyholes voids in 250 nm and 315 nm initial holes, (right) STEM image of the final pore after step 5 [14].

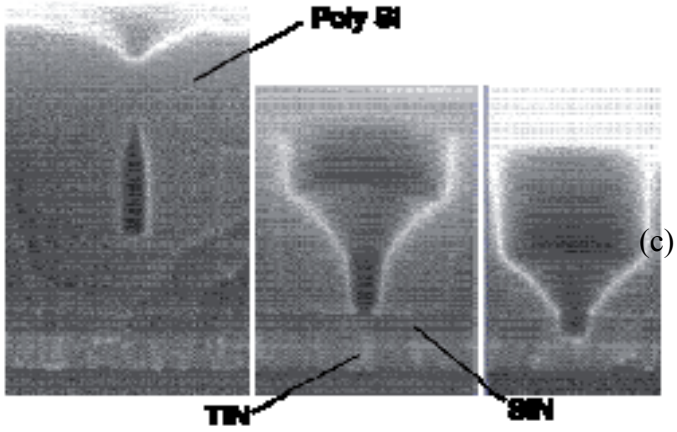


Fig.2.10 (c). Sequence of SEM micrographs showing successful transfer of keyhole into SiN [14].

2.4. Thin Film Deposition

Great strides in thin film deposition techniques have sustained the development of high-density microelectronics circuits. For micro-fabrication a large variety of thin films such as metals, semiconductors, or insulators are deposited from vapor phase. The use of chemical vapor deposition (CVD) for semiconductor device fabrication is of foremost importance. The CVD process has evolved greatly from being initially used for films required for passivation involving the pyrolysis of silane to newer applications demanding higher deposition rates, better step coverage that resulted in invention of plasma enhanced CVD (PECVD) techniques. Figure 2.11 gives different thin-film deposition techniques. The techniques in green are detailed in this work and others are out of scope of this thesis.

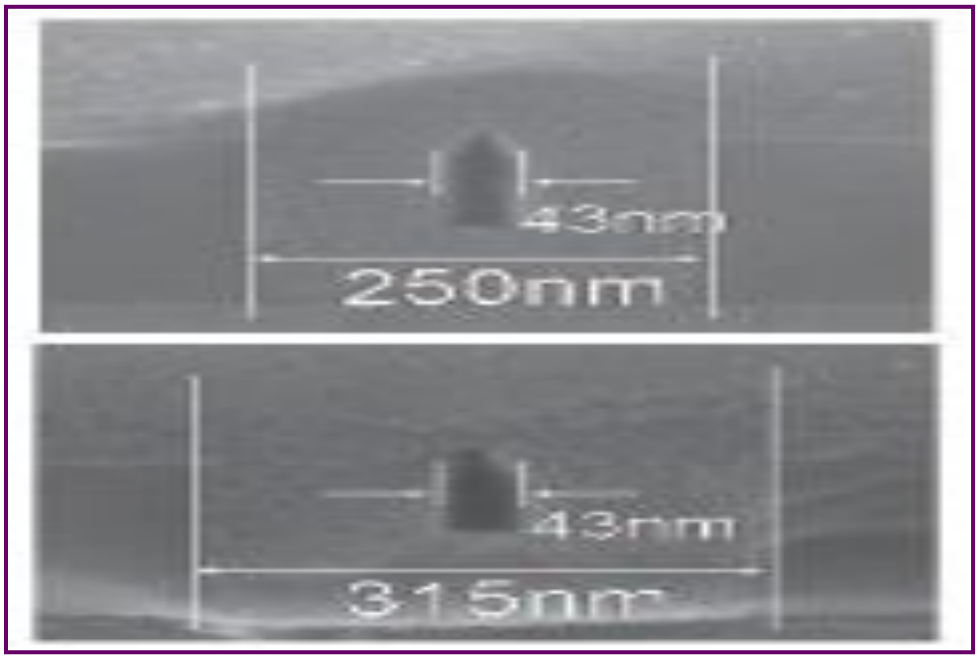


Fig. 2.11. Different thin-film deposition techniques.

Chemical vapor deposition is a generic name for a group of chemical processes that involve condensation of atoms or molecules from a gaseous phase onto a substrate. Most modern chemical vapor deposition processes can be further classified according to pressure used, characteristic of the vapors, plasma methods, types of deposition, and heat source used as follows:

Atmospheric pressure (APCVD), low pressure (LPCVD), metal-organic (MOCVD), plasma assisted/ enhanced (PECVD). In a typical CVD system, one or more volatile precursors are introduced in a system, which react and/or decompose on the substrate surface to produce the desired film. The reactive species, energy, rate of chemical supply, substrate temperature, pressure and substrate itself largely determines the type of film and its properties. A typical Chemical vapor deposition system consists of several parts categorized below:

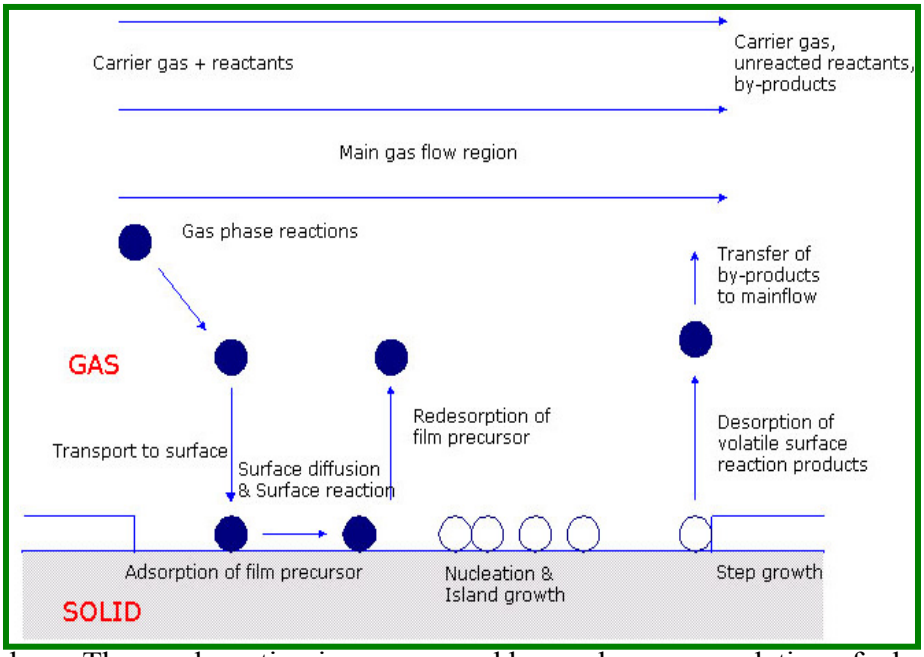
- Gas Delivery System: to supply the precursors to the reactor chamber.
- Reactor Chamber: chamber where deposition occurs.
- Substrate Loading Mechanism: to introduce and withdraw substrates.
- Energy Source: provides energy required for the reaction.
- Vacuum System: to remove all gases not required for the reaction.
- Exhaust System: to remove any volatile by-products from the chamber.
- Exhaust Treatment Systems: to treat/convert harmful gases.
- Process Control Equipment: gauges, controls, alarms and safety devices.

2.4.1. CVD Thin Film Growth Mechanism

The mechanism behind CVD process can be generalized as a sequence of following steps and is shown if Fig. 2.12.

- Gas phase diffusion from the gas flow
- Gas phase reaction
- Diffusion to the growth surface
- Adsorption
- Surface reaction
- Surface diffusion to growth sites
- Incorporation into the lattice
- Desorption of byproducts Vacuum System

Thin films deposition involves condensation of atoms or molecules from the



vapor phase. The condensation is commenced by random accumulation of adsorbed atoms to form clusters (or nuclei). These nuclei begin to expand to form coherent film and this stage is coined as '*growth'*.

Fig 2.12. Generalized sequence for thin film growth mechanism for CVD deposited films [15].

The thin films growth and nucleation mechanism is studied in detail by Chopra [16] and Maissel *et al.* [17]. The growth process can be summarized as Nucleation, followed by 3-D nuclei growth controlled by surface diffusion and its subsequent filling yielding a continuous film. Thin film growth is initiated by ad-atoms [18]. The mean residency time of ad-atoms τ_S is given by

$$\tau_s = \tau_v \exp\left[\frac{E_{ad}}{KT}\right] \tag{2.1}$$

Where τ_V is period of vibration perpendicular to surface, and E_{ad} is adsorption energy of adatoms on the substrate. The thermal equilibrium time of ad-atoms is then expressed as,

$$\tau_r = \tau_v \exp\left[\frac{-E_{ad}}{KT}\right] \tag{2.2}$$

If $E_{ad} > KT$, the adatoms will stay on the surface or if $E_{ad} \cong KT$ the adatoms will reevaporate. The growth stage of thin films is governed by surface energy of thin films γ_f, the surface energy of the substrates γ_S, and the interfacial energy between the thin film and the surface, γ_{fS}. The island growth is dominant if $\gamma_S - \gamma_{Sf} < \gamma_f$ according to Volmer-Weber mode [18].

2.4.2. Structure and Properties of CVD Thin films

The topographical details and structure of thin film depends on growth kinetics and hence on surface temperature, surface mobility, pressure, gas source, surface topography etc.

Grain Size

Grain Size is a function of annealing temperatures and deposition conditions. As observed from figure 2.13, thicker films possess larger grains and the effect increases with the deposition (or surface) temperature because of increased surface mobility. If the deposition rates are very high, the clusters get quickly buried under subsequent layers even though they have high mobility, thereby leading to bigger grain size.

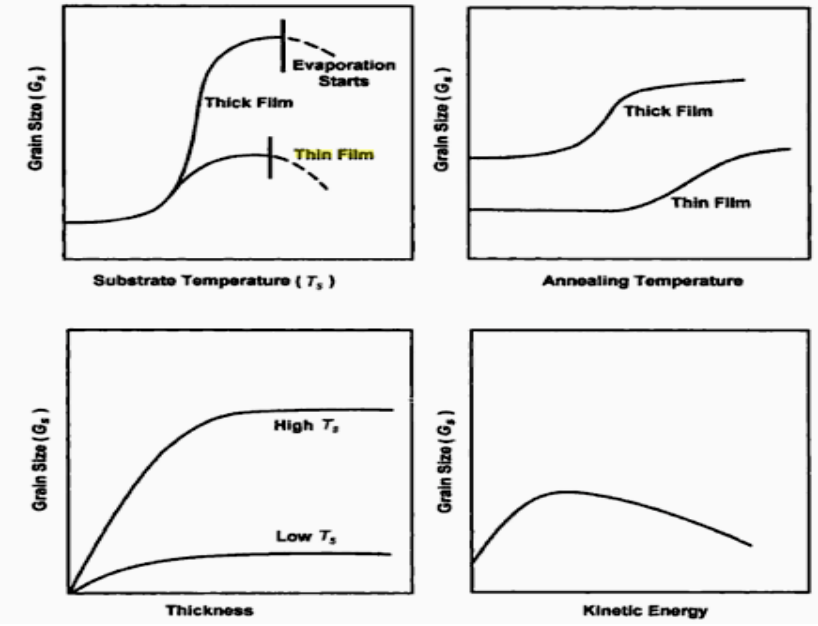


Fig. 2.13. Quantitative representation of the influence of various deposition parameters on grain size of thin films. Picture adapted from [18].

Surface Roughness

Surface roughness results from randomness of the deposition process and practically all films exhibit surface roughness even though if it means an energetically unstable high-energy state. Large nucleation barrier and low supersaturation leads to a fewer nuclei formation resulting in coarse-grained films showing possible continuity at relatively large thicknesses. Higher surface mobility helps filling the concavities leading to a much smoother film. The exception this theory is increased surface roughness by the preferential growth along some crystal. *Shadowing effect* can also aggravate the surface roughness problem where the impinging species fall obliquely on the substrate as

opposed to a normal incidence. Presence of surface contaminants during deposition and strain due to surface mismatch between the surface and the film can also cause increased surface roughness.

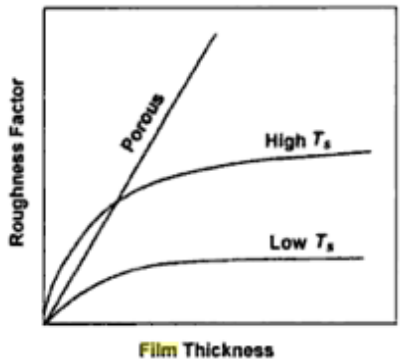
Roughness factor ('$\Delta\theta$') is used to measure the surface roughness of thin films and is the ratio of real effective area to the geometrical area.

$$\Delta\theta = \left[\left|\theta^2 - \left(\frac{1}{N}\sum_i h_i^{\,2}\right)\right|\right]^{1/2} \tag{2.3}$$

Where θ, represents the average film height or coverage and is defined as,

$\theta = \frac{1}{N}\sum_i h_i$,N is the number of surface sites and h_i is the film height of each site.

Fig. 2.14 show the increase in surface roughness with increasing film thickness and the substrate temperature. Fig. 2.15 shows the SEM micrographs showing the surface of rough and smooth films; a) obliquely deposited GeSe film has higher surface roughness due to the *Shadowing effect*; b) rough CdS film; and c) smooth CdS film with conditions optimized to deliver lower surface roughness.



(a)

Fig. 2.14. Qualitative variation of roughness factor with film thickness for lower and higher temperatures [18].

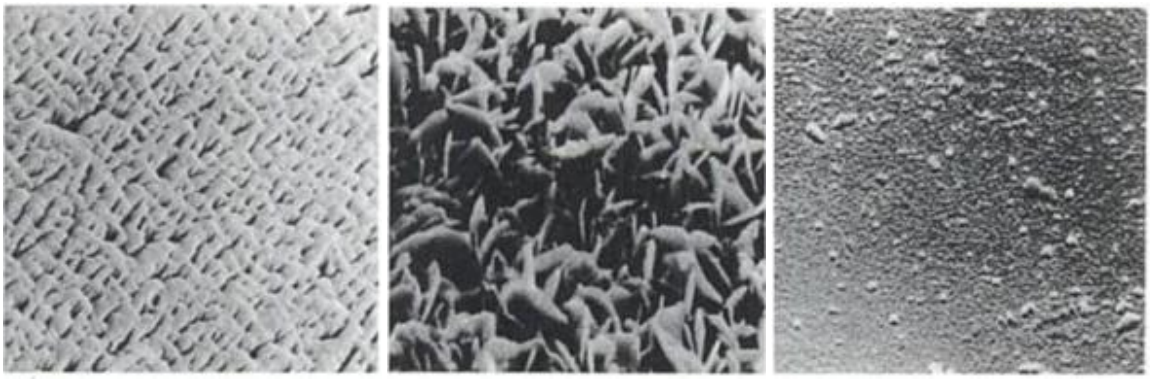


Fig. 2.15. Scanning electron micrographs showing surface of rough and smooth films; a) obliquely deposited GeSe film; b) rough CdS film; and c) smooth CdS film with conditions optimized to deliver lower surface roughness [18].

Density

This is another crucial physical film characterization parameter. It gives information about the physical structure and helps in estimating film thickness using gravimetric techniques. As observed from figure 2.16, density decreases with decreasing film thickness. At a given thickness lower temperatures yield comparatively denser films.

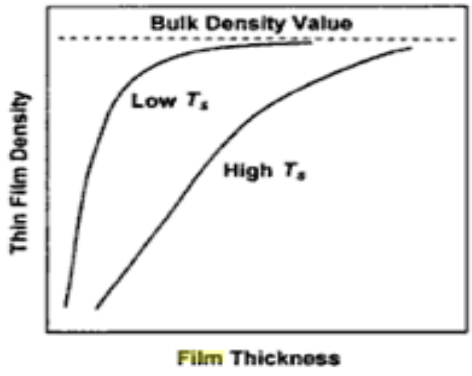


Fig. 2.16. Thin film density as a function of film thickness for low and high substrate temperature (T_S) [18].

Crystallographic Structure

The adatom mobility is extremely important in determining the crystallographic orientation of the thin film. The structure of these films can vary from a single crystal (crystalline) to a disordered amorphous state. Typically, the dielectric films such as SiO_2, and Si_3N_4 deposit in amorphous states, whereas metals attain polycrystalline structure. Silicon and polysilicon can obtain crystalline, polycrystalline or amorphous structures depending upon deposition conditions. Silicon generally possesses three deposition regimes: a) low deposition rate, high substrate temperature (T_S) yields films that tend to be single crystal; b) high deposition rate, low T_S gives amorphous deposited films; and c) polycrystalline films tend to appear at median deposition parameters.

Adhesion

Poor adhesion poses a potential reliability problem if the film lifts-off and results in device failure. Figure 2.17 show the results of tape tests for adhesion on films deposited by two different methods. The film on the right was deposited by evaporation, which is frequently linked with film de-lamination problems.

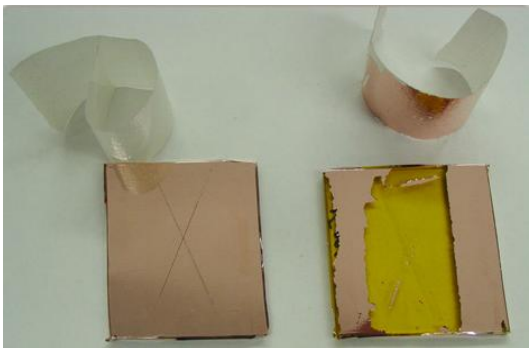


Fig. 2.17. Tape test performed to check adhesion; proper adhesion (left) and poor adhesion (right). The film on the right was deposited by evaporation, which is frequently linked with film de-lamination problems. Picture adopted from [19].

The film adhesion is a strong function of following parameters:

a) *Substrate quality* (*i.e.* cleanliness of substrate)

Cleaning the substrate prior to deposition ensures good adhesion. There might be some exceptions where presence of contaminants may improve adhesion by increasing the overall adsorption energy.

b) Kinetic energy of incident species and initial nucleation density

Adhesion is better if there is high initial nucleation density of incident species. Therefore, providing more nucleation centers by using fine-grained substrates promotes adhesion. Higher values of kinetic energy of incident species also help improve adhesion.

c) *Chemical nature of film/ substrate*: Oxide substrate provides a non-sticky surface before metallization. Therefore, it is advised to use adhesion promoters for *e.g.* use of chromium layer is suggested before gold metallization to prevent adhesion failure or cracking.

d) *Surface microscopic topography* (Surface roughness): Certain amount of surface roughness promotes adhesion; 1) by providing more surface area than the smooth substrate; 2) or by interlocking the two surfaces. On contrary, excessive surface roughness may also lead to de-lamination due to coating defects.

Film Stress

All the deposited films are prone to inherent stress during film growth that can be *compressive* or *tensile*. Compressively stressed films tend to buckle up under extreme conditions while expanding parallel to surface, whereas severe tensile stress may cause film cracking or peeling of film as it contracts parallel to surface if the elastic limits are

surpassed. Acceptable stress in thin films falls with in range of 10^8 - 5 x 10^{10} dynes/cm^2 as the higher stresses in films may cause following problems:

a) Poor adhesion leading to de-lamination

b) Corrosion

c) Brittle nature of films leading to cracking under tensile stress

d) Higher resistivity compared to annealed films

The elastic energy stored in deposited films due to stress is measured by quantity known as elastic energy density, u_V, and is expressed as [18];

$$u_v = \frac{\sigma^2}{2Y}(inJ / m^3) \tag{2.4}$$

Where Y denotes Young's modulus of thin films.

The total stress in thin film is denoted by 'σ' and is given by [31]

$\sigma = \sigma_{ext} + \sigma_{th} + \sigma_{int}$

Where σ_{ext} is the external stress on film, σ_{th} is the thermal stress, and σ_{int} is the internal stress. (2.5)

I. *Thermal Stress (σ_{th})* originates from difference in the thermal expansion coefficients between the film and substrate and is given by,

$$\sigma_{th} = (\alpha_f - \alpha_S)(\Delta T) E_F \tag{2.6}$$

Where, α_f and α_S are the average thermal expansion coefficients of film and substrate respectively, ΔT is the film growth temperature subtracted from temperature of measurement; and E_F is the Young's modulus of the film. Negative value for σ_{th} indicates tensile, while the positive value of σ_{th} indicates compressive stress. Films deposited by

evaporation are often associated to adhesion problems. One option is to switch to a different deposition method, or otherwise by lowering the substrate temperature when performing evaporation mitigates some of the thermal stress related problems. Fig. 2.18 show the buckling and bending of beams and cantilever structures under stress in polysilicon films. High temperatures anneal (1000 ^{0}C) may help alleviate stress.

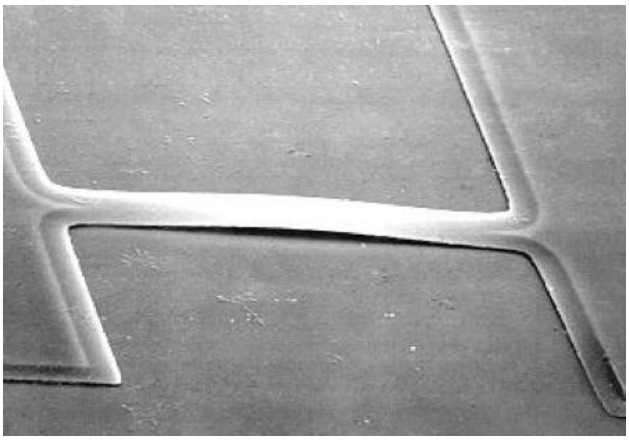


Fig. 2.18. Stress in poly films leading to buckling and bending of beams and cantilever structures. High temperatures anneal (1000 ^{0}C) helps alleviate stress [20].

II. *Internal or Intrinsic Stress (σ_{int}):*

Intrinsic film stress depends on deposition rate, temperature, pressure, substrate type, method of film preparation, thickness, and the energy of impinging species.

II.1. Temperature Effects:

Metal films manifest tensile stress at low substrate temperatures, which decreases to zero with increasing temperature in a linear manner and might changeover to compressive as depicted in figure 2.19. Post deposition annealing can help relieve some stress from the films by releasing some of the stored energy in the system.

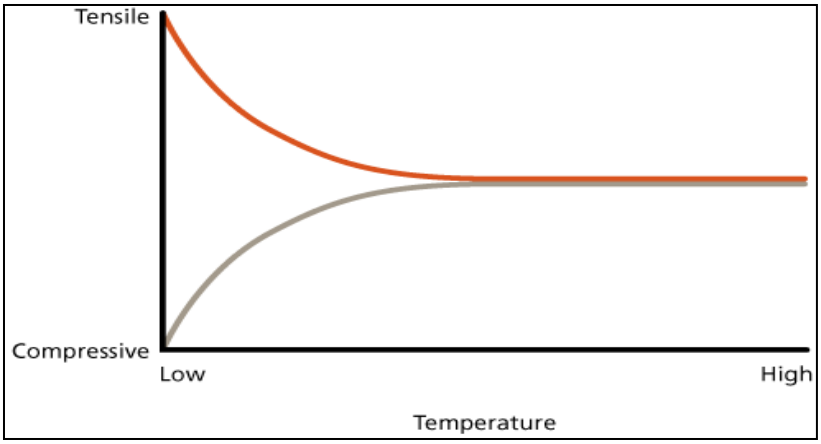


Fig. 2.19. Effect of temperature on type of film stress. Thermal annealing alleviates both tensile and compressive stress [19].

II.2. Impinging Species Energy Management

Many factors control the kinetic energy of the impinging species such as pressure, source to substrate distance and power. Fig. 2.20 shows that lower kinetic energy of ions cause film-shrinkage by *tensile stress* producing concave curvature of the substrate (left). Excessive ion energy can produce compressive stress, causing the film to expand and resulting in convex curvature (right).

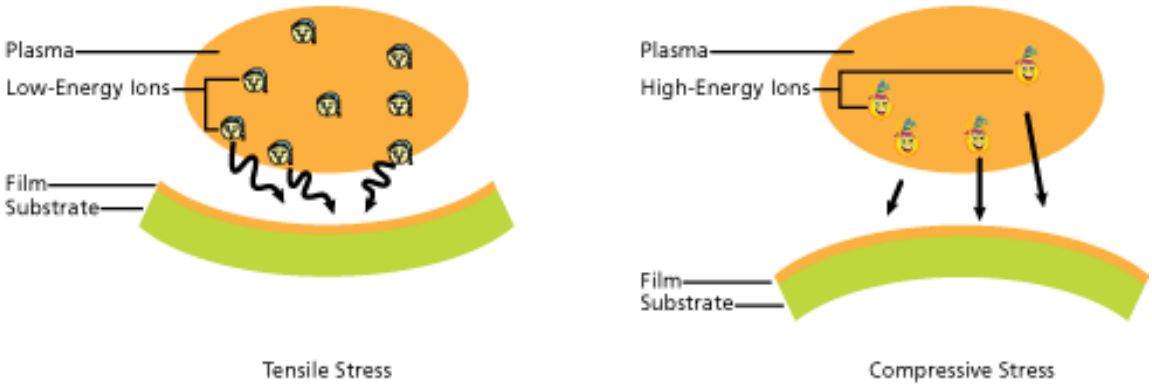


Fig. 2.20. *Tensile stress* producing concave curvature of the substrate (left), compressive stress resulting in convex curvature (right) [19].

Pressure

Mean free path refers to the average distance a particle travels without any collision and is given by;

$$\lambda = \frac{0.05}{P(torr)} \tag{2.7}$$

Therefore at higher pressures and as seen in figure 2.21, mean free path length of particles is small as more particles are present per volume leading to more inter-particle collisions. Collisions tend to reduce the surface bombarding energy of these particles. This results in greater *tensile film stress* because of lower packing density.

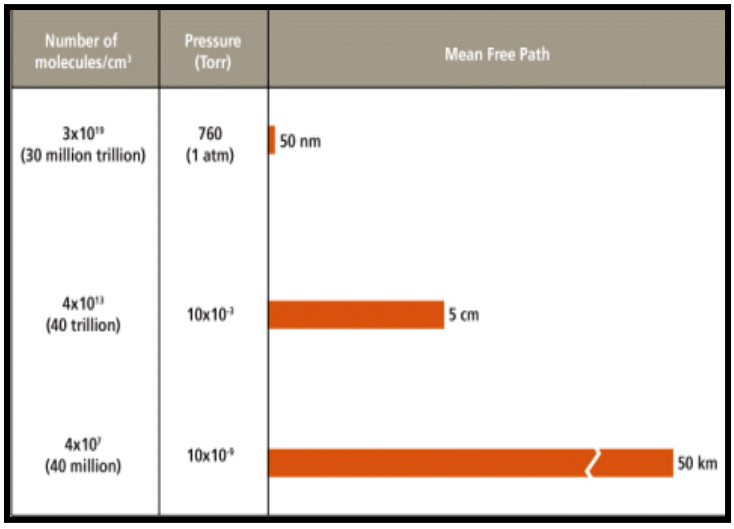


Fig. 2.21. Low pressure and longer mean free path results in fewer collisions delivering high-energy particles. Whereas, at higher pressures, more particles are present, mean free path and ion energy are lower [19].

On the contrary, very low-pressure yields mean free path length that is long and resulting in overly energized particles. This may produce superfluous packing density leading to *compressive stress*. Figure 2.22 shows a typical quantitative relationship between pressure and tensile/compressive film stress. Pressure fine-tuning is extremely

important to achieve low stress films. A general rule is to tweak only the pressure knobs and not to manipulate deposition rate, or any other process parameter while controlling the film stresses.

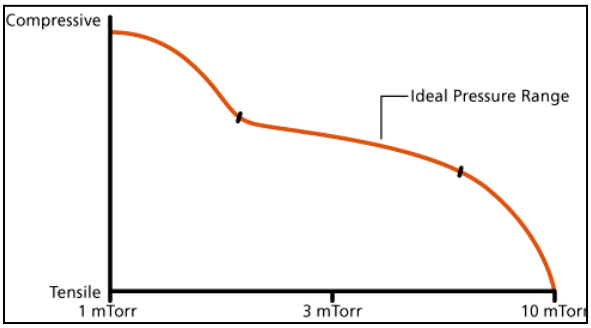


Fig. 2.22. Typical film stress variation as a function of pressure [19].

The process of determining the right process pressure involves hit and trial methodology. For *e.g.* a tensile stress in films, would suggest lowering down of pressure to increase ion energy and continue until minimal or zero tensile stress is achieved depending on the tolerance. On the other hand, increasing pressure can eliminate compressive stress. In the case of PECVD, too low of pressure may also extinguish the plasma or if the pressure has been turned up too high, plasma becomes unstable and can causes arcing. This necessitates pressure equilibrium to keep thin films stresses within a process tolerance.

Source to Substrate Spacing

In case of PECVD systems, plasma ignition/stability and thin-film stress are pivotal in determining Source-to-substrate spacing. Spacing is extremely important to control the particle acceleration for stronger collisions in order to knock-off electrons. This leads to a Cascade effect that helps in igniting the plasma required for film

deposition. Equivalently, the source-to-substrate distance can also be adjusted to manipulate kinetic energy of ions that can help mitigate stress problems.

Power Selection

Amount of power is another factor coupled with the kinetic energy of bombarding species. RF/ AC and pulsed DC power sources provides highly energetic ions that helps in improving film density. Figures 2.23 show the tremendous improvement of film uniformity, roughness and density obtained by using a pulsed-DC power source as compared to normal DC. Tuning the power to a right equilibrium can help reduce stress as depicted in the graph of figure 2.24.

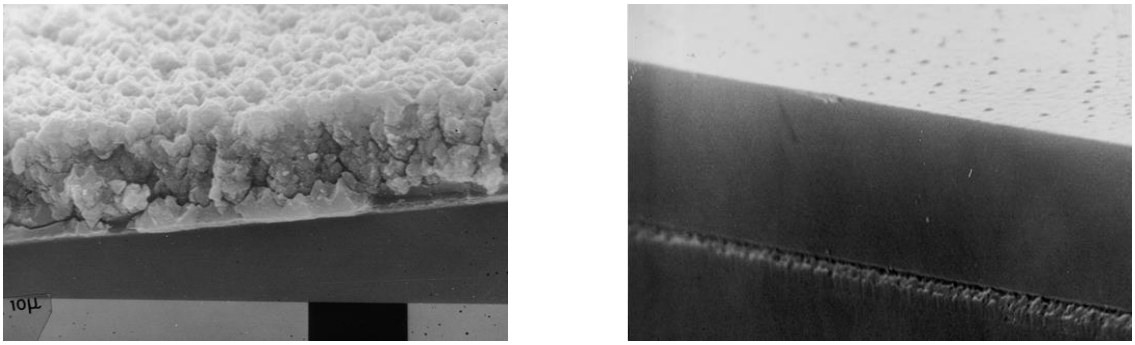


Fig. 2.23. SEM image for quality of film using straight-DC power supply (left) And using pulsed-DC power supply (right) —Higher ion energy produces better film uniformity, smoother film and greater packing density [19]

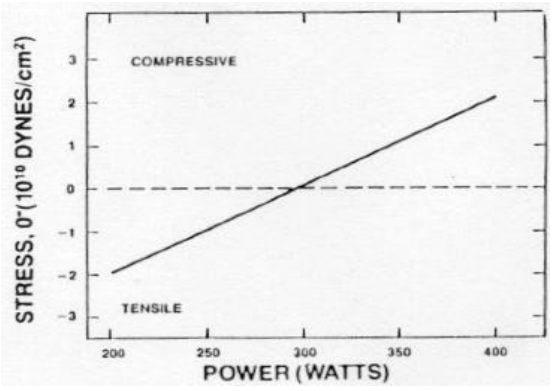


Fig. 2.24. Stress in CVD deposited film as a function of power [20].

2.4.3. Basic Characteristics of CVD and Deposition Conditions

The Table below defines the characteristics of homogenous and the heterogeneous reactions.

Homogenous Reaction	Heterogeneous Reaction
1. Gas phase chemical reaction of the reactant gases	Reactions between the species on or very close to substrate surface
2. Less desirable as they may form gas phase clusters of film and cause adhesion problems.	More desirable, occur selectively over heated surfaces
3. Produces low density films and defects in films	Better films quality
4. Reduces deposition rates by consuming reactants	Accompanies relatively higher deposition rates

Temperature dependence of Growth Rate for CVD films

Many models have been developed to describe the thin film growth kinetics. Grove *et al*. tried to approximate the flux of reactants from the gas bulk to the substrate surface [21] whereas Prandtl in 1904 employed a more realistic approach in 1904 and is termed as boundary layer theory [22]. The surface reaction rate increases with temperature and is given by an Arrhenius relation as [20];

$$R = R_0 e^{[-E_a/KT]} \tag{2.8}$$

Where R_0 is the frequency factor, E_a is the activation energy in eV, and T is temperature in ^{0}K. This regime where deposition rate increases with temperature in accordance with above relation is known surface reaction rate limited regime. Above this range, the increase in deposition rate with temperature saturates. Now, the deposition rate is determined by the rate at which the reactant gases are supplied to the substrate by mass transport. This region on the rate curve is known as mass-transport limited regime and would eventually determine the deposition rate no matter how high the temperature is increased. Thus, as demonstrated in figure 2.25, at low temperatures deposition rate is usually surface reaction rate limited and at high temperatures the deposition is mass-transport limited.

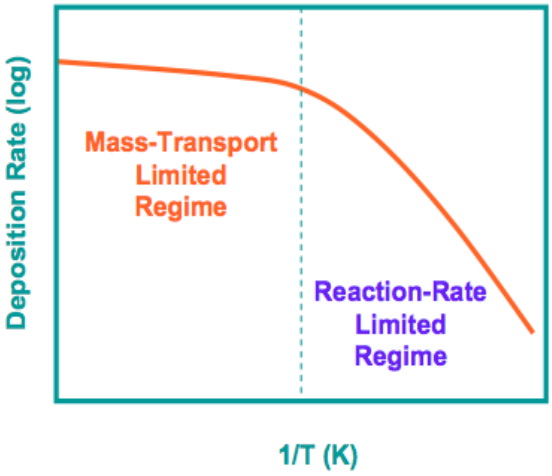


Fig. 2.25. Growth rate of CVD films as a function of temperature.

For example, LPCVD systems operate in reaction rate limited mode and are not dependent on flux of reactants arriving at wafer surface, whereas the APCVD systems are usually operated in mass transport mode. This is because of the large diffusivity of reactants in a system operating at low pressures and the rate-limiting step being the surface reaction.

2.4.4. Different types of CVD reactions

- Pyrolysis (Thermal Decomposition)

$AB\,(gas) \rightarrow A\,(solid) + B\,(gas)$

For Example: α-Silicon deposited at 580 - 650 ^{0}C *(At RIT 610^0 C-300 mT-25 sccm SiH_4)*

$SiH_4\,(gas) = Si\,(solid) + 2H_2\,(gas)$

- Reduction (lower temperature than Pyrolysis)

$AB\,(gas) + H_2\,(commonly\ used\ reducing\ gas) \leftrightarrow A\,(solid) + HB\,(gas)$

For Example: W deposited at 300 ^{0}C: Reversible process, used for chamber cleaning

$WF_6\,(gas) + 3H_2\,(gas) = W\,(solid) + 6\,HF\,(gas)$

- Oxidation

$AB\,(gas\ or\ solid) + O_2\,(commonly\ used\ oxidant) \leftrightarrow AO\,(solid) + [O]\,B\,(gas)$

For Example: Low-temperature SiO_2 (LTO) deposited at 450 ^{0}C:

$SiH_4\,(gas) + O_2\,(gas) \rightarrow SiO_2\,(solid) + 2H_2\,(gas)$

For Example: SiO_2 formed through dry oxidation a 900 - 1100 ^{0}C:

$Si\,(Solid) + O_2\,(gas) \rightarrow SiO_2\,(solid)$

- Compound Formation

$AB\,(gas\ or\ solid) + XY\,(gas\ or\ solid) \leftrightarrow AX\,(solid) + BY\,(gas)$

For Example: SiO_2 formed through wet oxidation at 900 - 1100 ^{0}C:

$Si\,(Solid) + 2H_2O\,(vapor) \rightarrow SiO_2\,(solid) + 2H_2$

For Example: SiO_2 formed through PECVD at 200 - 400 ^{0}C:

$SiH_4\,(gas) + 2N_2O\,(gas) \rightarrow SiO_2\,(solid) + 2N_2 + 2H_2$

For Example: Si_3N_4 formed through LPCVD at 700 - 800 ^{0}C:

$3\,SiH_2Cl_2\,(gas) + 4\,NH_3\,(gas) \rightarrow Si_3N_4\,(solid) + 6H_2 + 6HCl$

2.4.5. Low-Pressure Chemical Vapor Deposition (LPCVD) [23][24]

Essential Features:

- Reaction-rate limited mode of operation with activation energy for reaction provided thermally
- Low Pressure operation (~100 mTorr – 1Torr) resulting in high reactant gas species diffusivity assuring high wafer-to-wafer, within wafer uniformity
- Precise temperature control by "flat" temperature zone using multiple heaters and low gas pressure ensures heterogeneous reaction for better film quality.
- A typical LPCVD deposition of polysilicon at RIT is done using Pyrolysis or Thermal decomposition of Silane at Temperature 610^0 C, pressure 300-315 mT and silane flow of 25 sccms.

$$SiH_4\,(gas) = Si\,(solid) + 2H_2\,(gas)$$

- Temperature (T) < 580 ^{0}C gives amorphous films, whereas T > 580 ^{0}C gives polycrystalline films with preferred orientation.

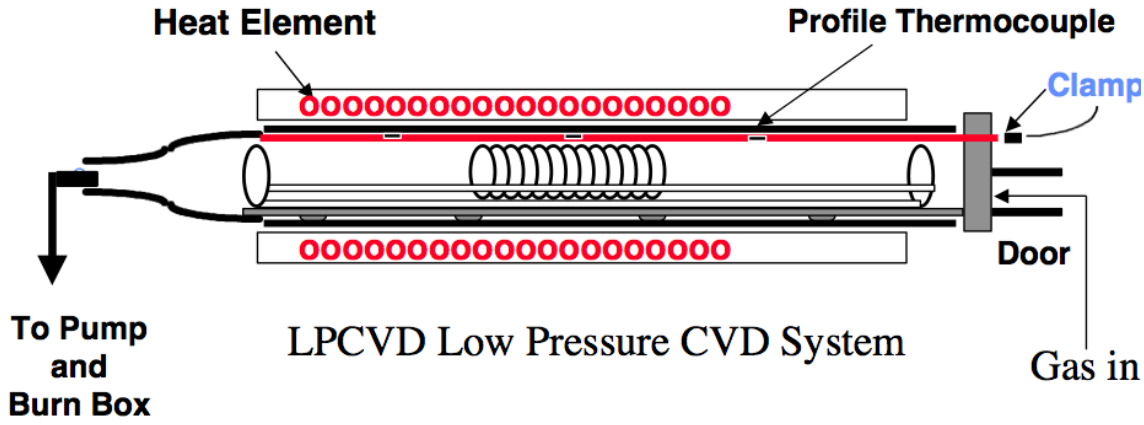


Fig. 2.26. Schematic of a typical LPCVD system at RIT [20].

2.4.6. Plasma Enhanced Chemical Vapor Deposition (PECVD)

Plasma Enhanced CVD (PECVD) shown in figure 2.27 uses RF-induced plasma (as in sputtering) for depositions at lower substrate temperatures as compared to traditional CVD. Energy is transferred into reactant gas that undergoes decomposition reaction to form radicals.

The range of applications is enhanced by reducing the challenges of CVD and by lowering the temperature budget requirements. PECVD deposition ensures higher deposition rates, wider scope for adjustment of film composition and improved film density and film stress. Also, PECVD is the primary deposition method used to deposit low-k thin film dielectrics. It operates in surface reaction limited mode and to ensure film thickness uniformity wafer cooling to control substrate temperature is important.

PECVD SiO_2 deposition using a) Tetraethylene orthosilicate ($TEOS$ gas) b) Silane (SiH_4)

a) $Si(OC_2H_5)_4 \rightarrow SiO_2 + C_xH_yO_z \uparrow$

b) $SiH_4(gas) + 2N_2O(gas) \rightarrow SiO_2(solid) + 2N_2 + 2H_2$ (Temperature= 200-400 ^{0}C)

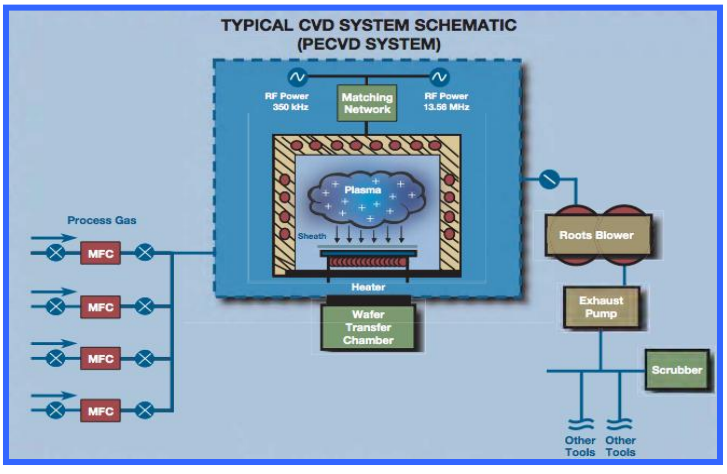


Fig. 2.27. A typical PECVD system schematic [25].

2.5. Comparison between Wet and Dry Etching

	Wet	Dry
Method	Chemical Solutions	Ion Bombardment or Chemical Reactive
Environment and Equipment	Atmosphere, Bath	Vacuum Chamber
Advantage	1) Low cost, easy to implement 2) High etching rate 3) Good selectivity for most materials	1) Capable of defining small feature size (< 100 nm)
Disadvantage	1) Inadequate for defining feature size < 1um 2) Potential of chemical handling hazards 3) Wafer contamination issues	1) High cost, hard to implement 2) low throughput 3) Poor selectivity 4) Potential radiation damage
Directionality	Isotropic (Except for etching Crystalline Materials)	Anisotropic

Table 2.1. Comparison between wet and dry etch [26].

2.5.1. Important Etch Terminology

- *Isotropic Etching*: Etching rate is the same in both horizontal and vertical direction
- *Anisotropic Etching*: Etching rate is different in horizontal and vertical direction
- *Lateral Etch Ratio*: Ratio of horizontal etch rate to vertical etch rate components.

$$R_L = \frac{Horizontal\_Etch\_Rate(r_h)}{Vertical\_Etch\_Rate(r_v)} \quad (2.9)$$

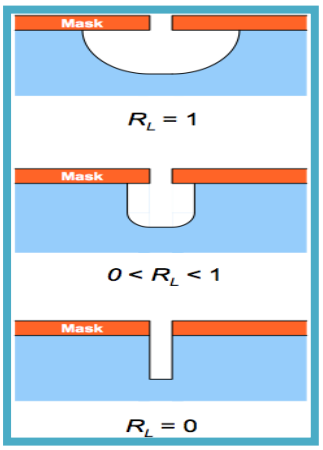


Fig. 2.28. Etch profiles corresponding to different lateral etch ratios (R_L).

- *Bias:*

The difference in lateral dimensions between the feature on mask and the actually etched pattern. Smaller R_L results in smaller bias. The etch bias problem can be mitigated by using a compensation factor in mask dimensions. For example an etch bias of 0.5 μm can be counter balanced by using a 5.5 μm etch mask to get 5 μm transferred feature.

- *Under Cut and Over Etch:*

As seen in figure 2.29, For R_L =1 (left), over etching results in more vertical profile but larger bias and severer undercutting, whereas for 0< R_L <1 over etching results in poor CD control in thicker films.

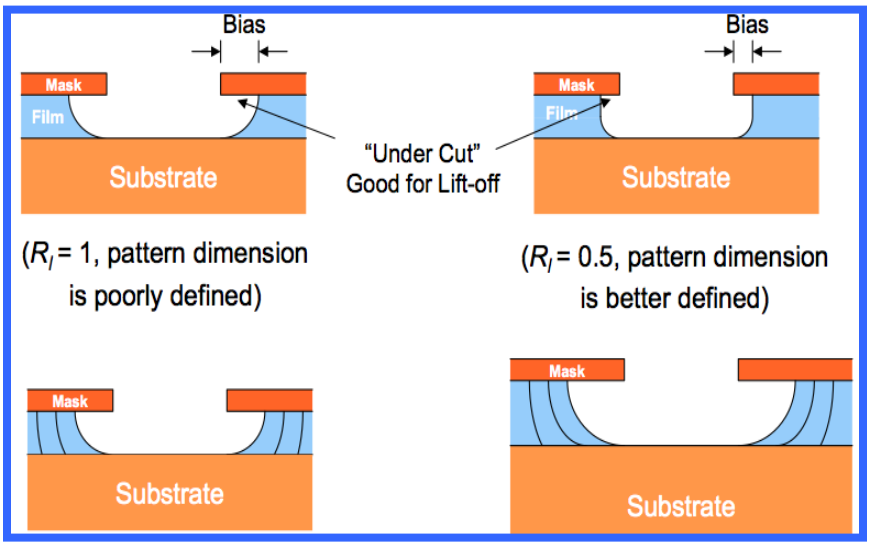


Fig. 2.29. Pattern transfer for different lateral etch ratios (R_L) during wet etch. [26].

- *Selectivity:*

Selectivity is the ratio of etch rates of different materials in a etch process. The selectivity with respect to mask material is denoted by S_{fm} and with respect to underlying film or substrate is denoted by S_{fs}.

$$S_{fs} = \frac{V_f}{V_s} \text{ and } S_{fm} = \frac{V_f}{V_m} \tag{2.10}$$

- *Degree of Anisotropy:*

  $A = 1 - R_L$ where, R_L=0 represents isotropic etching and, R_L=1 represents anisotropic etching

- *Mask Erosion (Faceting): Film-Mask Etching Selectivity:*

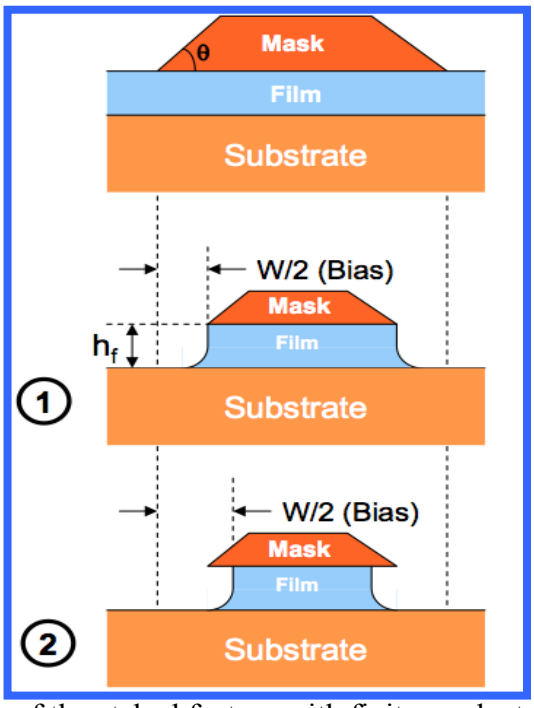


Fig. 2.30. The progression of the etched feature with finite mask etch rate (mask erosion). The CD loss is twice the bias width and is given *by* '*W*' [26].

As depicted in figure 2.30, the ratio of the total loss of linewidth (*W*) dimension of the mask to film thickness (h_f) is given by;

Case I: If film horizontal etch rate (r_{fh}) < mask horizontal etch rate (r_{mh})

$$\frac{W}{h_f}(\%) = \frac{2}{S_{fm}}\left(R_m + \cot\theta\right) \tag{2.11}$$

Mask lateral etch ratio,

$$R_{mL} = \frac{r_{mH}}{r_{mV}} \tag{2.12}$$

Case II: Film horizontal etch rate (r_{fh}) > mask horizontal etch rate (r_{mh})

$$\frac{W}{h_f}(\%) = 2R_m \tag{2.13}$$

Thus, it is extremely important to have a good etch mask for anisotropic etching. Resist is most widely used as an etch mask, but, is not good for high aspect ratio etching because it is readily attacked by the etch chemistries used. Many approaches have been used to improve the etch resistance capabilities of resists such as hard baking the resists at near glass transition temperatures. But, this leads to serious reflowing of resist owing to higher temperatures leading to rounded-resist tops, which itself is problematic and may cause undue increase in CD's due to mask erosion and faceting issues during etching. The corner of resist is always rounded even when the mask walls are vertical. These corners etch faster and erode quickly than the other areas. Also, the sputter etch yield of materials is a function of incident angle of the ions.

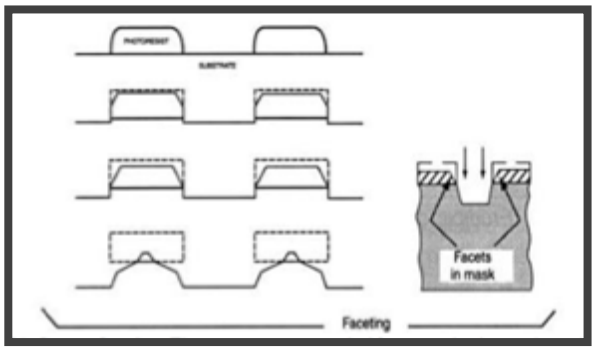


Fig. 2.31. Corner faceting. The sputter action creates angled facets that propagates down with the eroding mask causing sloped etch profiles [27].

The corner-faceting is shown in figure 2.31. For example, the sputter etch rate of resists is maximum at the incident angles of 60^0 as compared to normal ionic incidence. Thus, the sloped sidewall of a mask may lead to sloped etching sidewalls, which may further deteriorate due to increased electric field at the corners because of the applied bias. The faceting can be controlled by an ideal or near-squared resist top profile. Other techniques available for increasing the etch endurance of the resist mask are UV-hardening and e-beam hardening [28], but they are not feasible here at RIT due to special tool requirements.

- *Loading and Micro-loading effects*

The etch rates decrease with increase in etchable surface in chamber is termed as loading effect. This effect is caused by gas phase etch species depletion by reaction with material being etched. The loading effect is predominant in silicon etching in fluorine-based chemistries because etching reactions dominate the loss of fluorine. However, in bromine and chlorine based chemistries etch rates are less vulnerable to load size and circuit topology conditions as the concentration of atoms in such plasmas are limited by atom-atom recombination [29]. The loading effect is undesirable because it causes: a) etch rate drop, b) loss of throughput and leads to process non-uniformities from run-to-run and c) once the end point is achieved, the etchable area increases abruptly and causes increased etch rate with just the sidewalls being exposed. This aggravates the undercutting problem. Micro-loading effect accounts for slower etching of denser features than isolated features (within wafer non-uniformities), and isolated lines etch slower than trenches. This effect is even more severe from center to edge of the wafer. The effects due to loading can be minimized by: a) using etch chamber with large volume

and high surface area; b) allowing the removal rate by pumping to dominate by using large gas flows and; c) by using an electrode made of material similar to one being etched to reduce process dependence on wafer quantity.

2.5.2. Dry Etching

Figure 2.32 illustrates the sequence of events occurring during a plasma-assisted etch process. The slowest process is the ultimate rate-determining step.

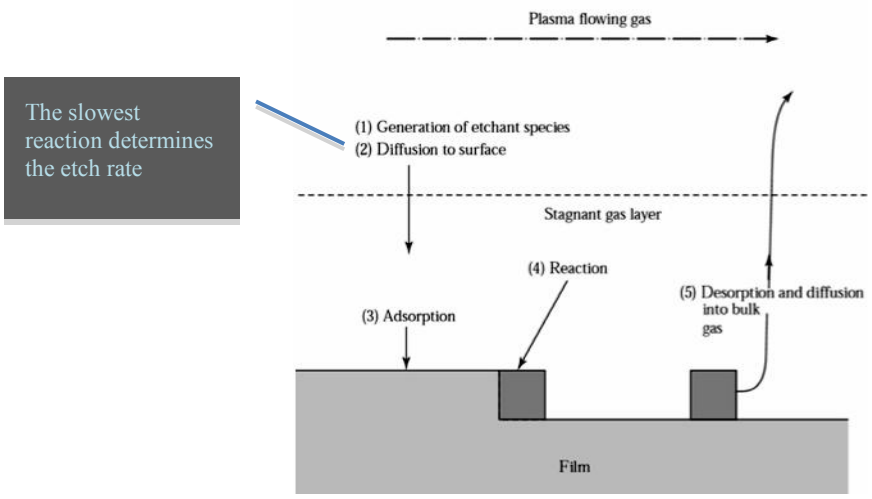


Fig. 2.32. Plasma etching mechanism with the sequence of processes.

I. Generation of etching species (Gas phase reactions)– The etching will not proceed without any etch species. Reactive species (radicals and ions) are generated in the plasma. Radicals cause chemical reaction and ions cause bombardment.

II. Surface Diffusion (Mass transport) – Reactive species diffuse towards the surface to be etched, the mechanics of getting to the surface can limit etch rates, *aspect ratio, undercutting and uniformity*

III. Adsorption- Also affects the aspect ratio

IV. Chemical Reaction (Reaction rate controlling step)- Strong temperature dependence (Arrhenius relationship)- affects the etch rate

V. Desorption – The etch by-products needs to be highly volatile or the etch ceases

VI. Diffusion to bulk gas- May cause dilution of un-reacted etching species leading to non-uniform etching

The ultimate goal of an etch process is to reproduce the features on the mask with precision and possess following attributes:

1) High selectivity with respect to mask and underlying layer.
2) Suitably high throughput.
3) Etch uniformity; wafer to wafer, across wafer and over different runs.
4) The process should be safe and cause minimum substrate damage.

2.5.3. Reactive Ion Etching (RIE)

As seen in the figure 2.33, a typical RIE system consists of a vacuum chamber and two parallel electrodes connected to a high frequency RF power supply (usually 13.56 MHz). The wafers are placed on a cathode plate that is grounded to electrically isolate from the rest of the chamber. Gas enters the chamber through a showerhead, and exits to the vacuum pump system through the bottom. The gas selection depends upon the etch process. The pressure inside the chamber is maintained between a few mTorr - few hundred mTorr to sustain the plasma. This can be achieved by tuning the gas flow rates and/or throttle valve position.

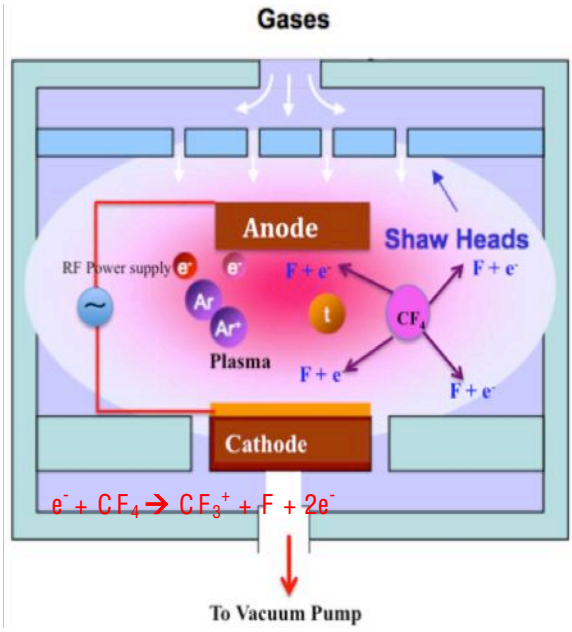


Fig.2.33. Schematic of a typical parallel plate RIE system [26].

Operation

Applying a strong radio frequency electromagnetic field to the wafer plate ignites the plasma. The oscillating electric field ionizes the gas molecules by impact ionization, stripping them of electrons, creating plasma. The electrons are accelerated up and down in the chamber due to the E-field sometimes striking both the upper wall and the cathode. However, the ions being much more heavier move relatively lesser in response to the E-field. The electrons absorbed into the cathode leads to charge build up due to its DC isolation. This build up leads to a negative self-dc bias on the cathode, of the order of few hundred volts. Whereas, the plasma is always positive relative to grounded electrode due to the higher concentration of positive ions compared to free electrons.

Under the influence of a large potential difference, positive ions tend to drift toward the cathode causing collisions with the sample/wafer. These ions can react chemically with the wafer surface or cause ionic bombardment and remove some

material. The vertically directed reactive ions/ species, can produce near 90 degree etch profiles, which contrast with the typically sloped wet etching profiles. The sheath thickness is of the order of '*Debye length*' and features smaller than this characteristic length can be etched directionally. The mean free path length must be greater than chamber dimensions (*i.e.* low gas pressure) to prevent the reflection and re-deposition of sputtered species.

Parameter control in RIE process

Implementing an etch process that possesses the desired characteristics involves control of the large number of parameters affecting that process. Figure 2.34 illustrates some of the parameters that affect the gas-phase and the surface phase interactions. The more macroscopic factors being pressure, power and the gas flow rates. In fact, the macroscopic factors are coupled to the basic plasma parameters. A change in macroscopic parameters may lead to complex interactions and alter two or more basic parameters such as potential or temperature.

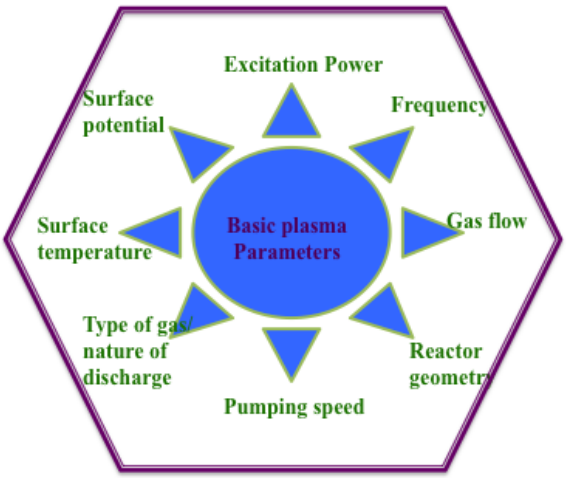


Fig.2.34. Various Plasma parameters affecting the reactive-ion etching process.

For example: gas flow, pumping speed and pressure are interrelated factors and needs simultaneously fine tuning to control pressure. This makes the Dry-Etch process development a profound challenge and demands a designed experimental approach.

Effect of Pressure and Frequency

At pressures lower than ~ 50 - 100 mTorr, the sheath thickness and sheath potential increases from 10s - 100s of volts. In this regime, plasma potential goes up and ionic bombardment energy is precipitously increased with decreasing pressure. Finally, at very high ionic energies and low gas pressure, physical sputtering dominates. However, sputtering does not occur until ionic energy exceeds a material and ion-specific threshold [29]. The similar effect is seen when frequency is lowered from around 5 MHz to ≤ 1MHz with gas pressures being in range of 100-100 mTorr. Thus, either low frequency or low pressure can be used to induce anisotropy.

Effect of Temperature

Just like pressure, temperature has a profound influence on etching. For *e.g.* etch rate constant are Arrhenius function of temperature. Physisorption and diffusion are sensitive to temperature which inturn can affect selectivity and anisotropy. High temperatures ($>120^0$) assist in anisotropic sidewalls.

Table 2.2 compares the different etching methods commonly employed in semiconductor technology.

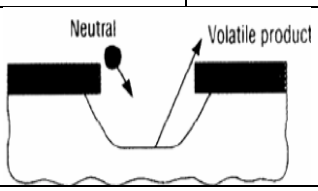
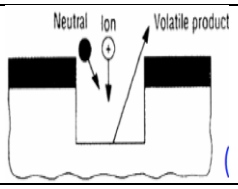
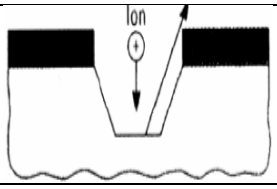
Types of Etching	Gas/vapor Etching	Plasma Etching	Reactive ion Etching	Sputtering Etching
Methods	Chemical	Chemical	Chemical & Physical (ion)	Physical
Geometry	Isotropic	Isotropic	Directional	Directional
Selectivity	Very High	High	Fair	Low
Excitation Energy	None	10's to 100's of Watts	100's of Watts	100's to 1000's of Watts
Pressure	High (760-1torr)	Medium (>100 mtorr)	Low Medium (10-100 mtorr)	Low (~10 mtorr)
				

Table 2.2. Dry etching spectrum with typical etching characteristics.

2.5.4. Dry Etch Gas Selection

Gas mixture of $CF_4 + O_2 + N_2$ gives high Si_3N_4/ SiO_2 etch selectivity, where N_2 acts as diluent gas, improves heat transfer and forms active etch species [30] and $CHF_3 + O_2$ gives high SiO_2/ Si selectivity and anisotropy [31].

Materials	Etch Gas	Etch Product
Silicon	Cl_2, CCl_2F_2	$SiCl_2$, $SiCl_4$
Si, SiO_2, Si_3N_4 (Si3N4 etch rate > SiO_2 E.R)	$CF_4 + H_2$, SF_6, NF_3, $CHF_3 + O_2$	SiF_4 (Low Si_3N_4/ SiO_2 Selectivity)
High selectivity (~10:1) Si_3N_4/ SiO_2	$CF_4 + O_2 + N_2$	
Aluminum	BCl3, CCL4, $SiCl_4$, Cl2	$AlCl_3$, Al_2Cl_6
Organics	O_2, $O_2 + CF_4$	CO, CO_2, H_2O, HF

Table 2.3. Typical etch chemistries and the byproduct of dry etching reactions.

n-type doped Si etches faster (reaction rate increased by ~2.5 X) than P type doped Si (reaction rate reduced by 0.8X) [32] in fluorine based feed gas system, while heavily doped n-type Si and polysilicon in Cl atom plasmas etch 15-25 times faster than undoped films.

2.5.5. Dry Etching Si/ SiO_2 in Fluorine Based Gases and Plasmas

- CF_4 does not chemisorb on Si, and would not etch silicon in absence of plasma.
- Etching is accomplished by creation of radical species (fluorine atoms) produced by dissociation of CF_4 molecules.

Etch Rate and Si/ SiO_2 selectivity dependence on O_2/ CF_4 ratio

- Insufficient F- atom concentration leads to a slower etch rate even with plasma.
- However, with the addition of O_2, F-atom concentration increases according to reactions;

  $O + CF_3 \rightarrow COF_2 + F$,

  And, then $O+COF_2 \rightarrow CO_2 + 2F$

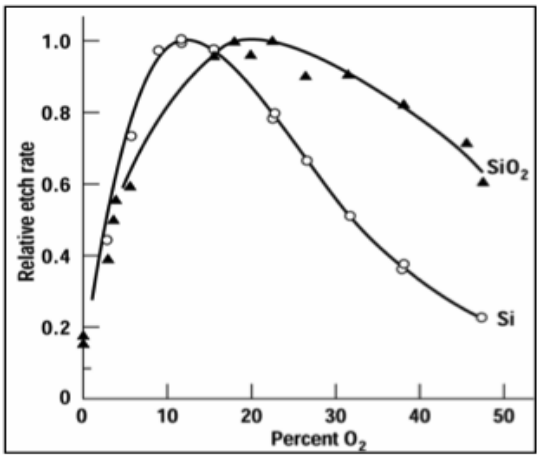


Fig. 2.35. Normalized etch rate of Si and SiO_2 versus the O_2 concentration in $CF_4 – O_2$ gas [31].

- As illustrated in figure 2.35, etch rate maximizes around 12% O_2 and decreases at higher O_2 concentration because of dilution of F atom concentration by overly abundant O_2.
- Etch rate is higher for Si than for SiO_2 thereby giving higher Si/SiO_2 selectivity.

Etch Rate and SiO_2/ Si selectivity dependence on H_2/ CF_4 ratio

- H_2 is a fluorine scavenger, *i.e.* reduces Fluorine to Carbon ratio (F/ C ratio), thereby reducing F- atoms concentration by following reaction:

  $H^+ + F + e^- \rightarrow HF$

- Addition of H_2 increases SiO_2/ Si etch selectivity tremendously. As seen in the figure 2.36, at 40% of H_2 concentration Si etch rate reduces to zero whereas SiO_2 rate remains unaffected.

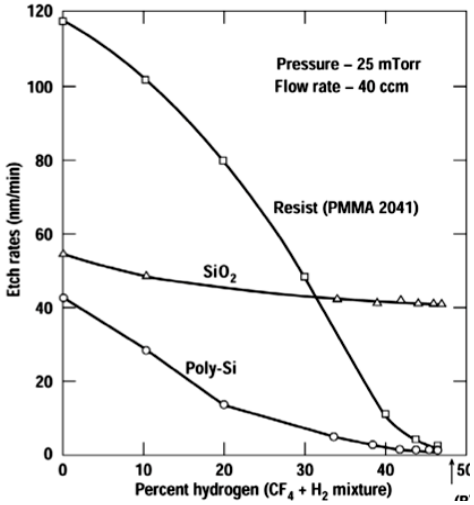


Fig. 2.36. The etch rate of resist, SiO_2 and poly-Si in a RIE configuration versus H_2 concentrations in CF_4 - H_2 feed gas system [31].

- Increased etch selectivity involves two mechanisms;
  1) Higher deposition of non-volatile (carbon like) residues on Si surface terminates the etching of Si.
  2) Lesser accumulation of residue on SiO_2 surface than on Si surface: Carbon combines with locally available O_2 (available from the byproduct of the etch reaction of SiO_2) to form volatile CO and CO_2 allowing SiO_2 etch to continue.

Fluorine-to-Carbon Ratio (F/ C) model

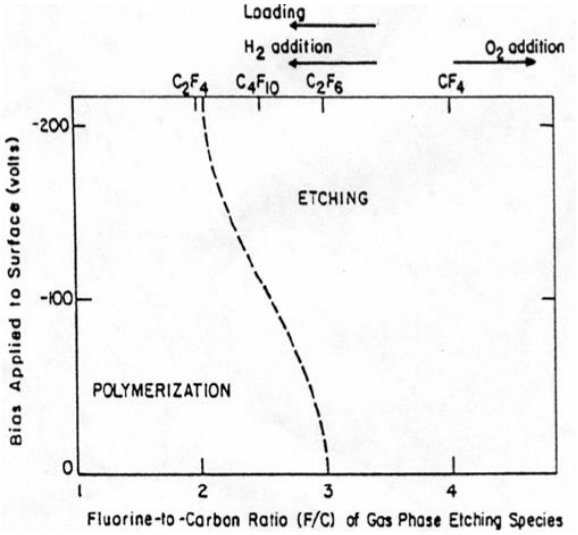


Fig. 2.37. The boundary between etching and polymerization conditions influenced by F/ C ratio of reactive species and the applied bias [31].

- Plasmas with F/ C ratio less than 4 (for *e.g.* CHF_3 has F/ C ratio of 3) are known as fluorine deficient plasmas and produce similar effect as if adding H_2 to the etch gas. Increasing F/ C ratio increases Si etch rates, and decreasing the F/ C ratios lowers them.
- Conversely, the addition of O_2 increases the F/ C ratios, because the oxygen consumes more carbon than F atoms. The feed gases emulating similar effect are CO_2, F_2, and NO_2.
- Also illustrated in the figure 2.37, the boundary between polymerization and etching varies with the applied bias. Higher bias allows etching to occur at lower F/ C ratios due to increased bombardment by energetic ions.

Sidewall Profile Control for Anisotropic Etching

- The degree of anisotropy can be increased by formation of sidewall passivating films (Polymerization).
- The reaction rates are increased due to the lattice damage of the surface induced by high energy (> 50 *eV*) impinging ions (*Energetic Ion Induced Anisotropy*).
- Lower energy ($\leq$ 50 *eV*) ions provide enough energy to desorb the deposited nonvolatile fluorocarbons by physical sputtering action (*Inhibitor Induced Anisotropy*) as shown in figure 2.38.

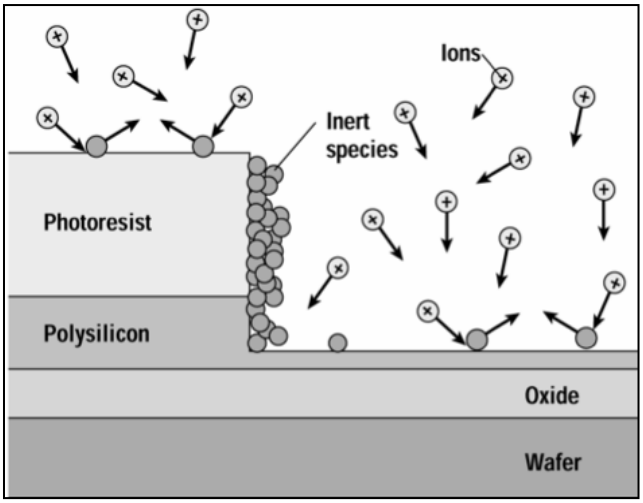


Fig. 2.38. Surface inhibitor mechanism for ion assisted anisotropic etching.

- The E-field in RIE systems causes perpendicular ionic acceleration. As a result, the fluorocarbon film accumulates on the sidewalls where ionic bombardment is minimum.
- Adding hydrogen scavenges fluorine and encourages the fluorocarbon film formation, creating a carbon-rich plasma (similar effect produced by if C_2F_6 or CHF_3 is used instead of CF_4).

- SiO_2 surface observes lesser polymer accumulation than Si surfaces leading to an increase in SiO_2/ Si etch selectivity.
- Inherent Tradeoff exists between Si/ SiO_2 *selectivity* and *Anisotropy*

2.5.5. Etching Trend Chart for different materials

Figure 2.39 shows the etching trend table that can be extremely helpful guide for developing a dry etch process. Experimental design procedures and response analysis are valuable tools to explore important variables and to fine tune an etch process as desired. This table can assist in reducing the data required to design an efficient experiment and in no way a substitute for a response charts derived out of factorial designs that use gas composition, pressure and power as factors.

	Power	Pressure	Passivant	Frequency
Rate	↑	↑	↓	↓
Selectivity	↓	↑	↑	↑
Anisotropy	↑	↓	↑	↓
Uniformity		↓	↓	

Fig. 2.39. Etching trend chart for different materials.

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CHAPTER 3

Process Development

3.1. Process Design

The void transfer process employed in this study is depicted in figure 3.1. As described in reference [1], the process essentially consists of: 1) deposition of a low stress thin film PECVD stack of SiN-SiO_2-SiN-pad oxide on silicon wafers; 2) etching of a lithographically defined window of size '*R*' (=*2r*) ceasing at bottom silicon nitride (SiN); 3) creation of overhang '*Δ*' in SiO_2 using selective isotropic etch; 3) deposition of conformal LPCVD polysilicon that pinches off at top to deliberately form bottle shaped voids; 4) etching back polysilicon selectively to transfer the void to underlying SiN; 5) finally, removing the polysilicon stingers and SiO_2 using a selective wet-etch leaving the small pores in SiN.

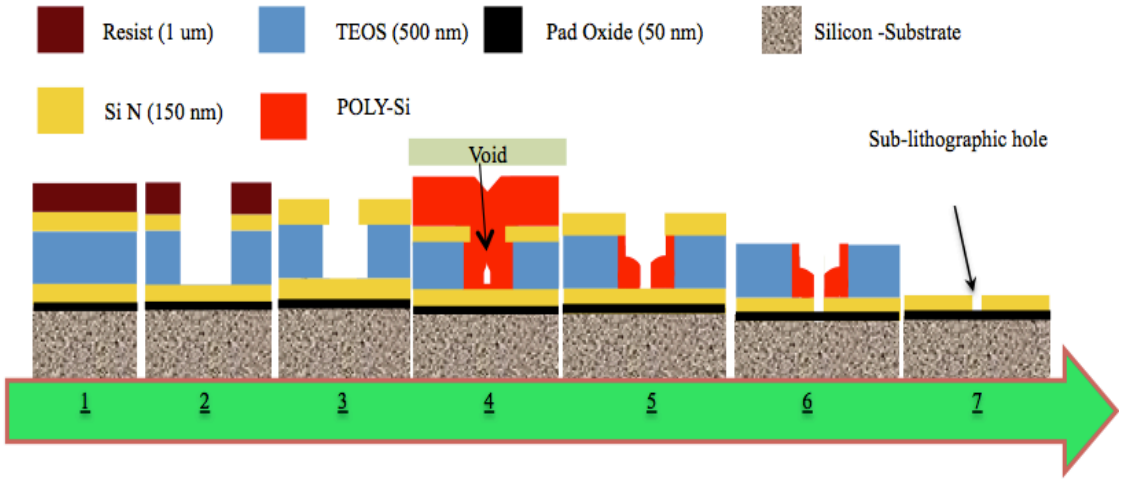

Fig 3.1. Void patterning process flow schematic.

The entire process is envisioned as a self-sustaining process infrastructure for future projects. Therefore the entire process flow was tailored to comply with the toolset

available at Semiconductor and Microsystems Fabrication Laboratory (SMFL) at RIT. Many process and characterization steps, such as materials deposition, dry/wet etching, lithography, high temperature oxidation/diffusion, Scanning electron microscopy (SEM) and substrate cleaning are available in house. Different processes were tuned to get the desired process characteristics. The author attempts to organize the thesis into a self-contained resource. Some paramount processes in the thesis are examined in detail in this chapter, whereas the processes that are standard procedures at RIT (RCA clean, pad oxide growth *etc.*) are included in the Appendix III.

3.2. Mathematical Modeling and Critical Process Design Considerations

The process is mathematically modeled based on geometrical concepts to predict the void size. Based on this mathematical model, vital design and process parameters affecting void formation are identified and then simulated in detail using Silvaco TCAD tools (ATHENA/ Elite) as detailed in chapter 4. Figure 3.2 defines the various geometrical parameters as also described by Breitwisch *et al.* [1].

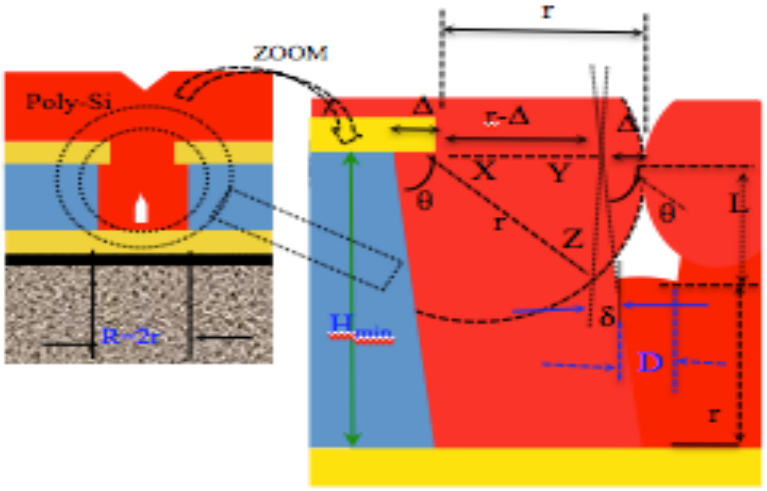

Fig. 3.2. Void parameters and diameter calculations: 'Δ' represents the overhang, 'θ' represents the sidewall angle, 'D' is the final void diameter, 'r' is half the lithographic defined hole (*i.e.* r=R/2) and 'L' is the void length.

3.2.1. Critical Design Parameters

From Figure 3.2, the critical design parameters are identified and the valid assumptions are formulated to model the void formation process. These conditions are crucial for void formation and successive etch-back in order to develop a robust yet user-controlled process with the potentiality of producing desired nanoscale features.

- The overhang length 'Δ' must be less than 'r' for an effective CD miniaturization, and the parameter'Δ' essentially controls the void diameter.
- Thickness of SiO_2 layer 'T_{Sio2}' must be greater than a certain minimum thickness 'H_{Min}' in order to prevent the premature filling of lithographically defined holes without forming any voids.
- Higher aspect ratio of H_{Min}: R is desirable for producing voids with longer length 'L' for lower etch related CD variations
- The sidewall angle 'θ' must be near 90^0 to get vertical profiles of final sub-lithographic pore instead of sloped sidewalls. The parameter 'δ' manifests from variation in angle'θ' from 90^0 and leads in further reduction of void diameter 'D'.
- The Poly-Si CVD deposition should be highly conformal for accurate CD control.
- The void size can be predicted using the geometry of the design.

3.2.2. Mathematical Void Formation Model

Assuming the LPCVD polysilicon deposition is highly conformal and the overhang length 'Δ' is less than 'r' and other crucial design conditions mentioned above are met, void diameter can be estimated using set of derivations below:

In Figure 3.2, triangle XYZ,

$H_{Min} = r + YZ$ 3.1

Where, length of line segment YZ is given:

$YZ = \sqrt{\Delta(2r - \Delta)}$; Or 3.2

$H_{Min} = r + \sqrt{\Delta(2r - \Delta)}$ 3.3

Equation 3 gives the value of 'H_{Min}' (*i.e.* the minimum thickness 'T_{SiO2}') required for successful formation of voids without premature filling of hole. The value for 'r' and 'Δ' is fixed to a reasonable number as shown in table 1. Thus, the effective thickness 'T_{SiO2}' must always be kept greater than H_{Min}. Equation 4 gives the relationship between the sidewall slope 'θ', overhang 'Δ', compensation factor 'δ' and lithographically defined hole size of (R=2r):

$$\tan\theta = \left[\frac{\sqrt{(\Delta-\delta)(2r-(\Delta-\delta))}}{(\delta)}\right] \quad 3.4$$

Equation (4) can be re-arranged as a quadratic equation and solved for value of 'δ' as,

$$(1+\tan^2\theta)\delta^2 + 2(r-\Delta)\delta + (\Delta^2 - 2r\Delta) = 0 \quad 3.5$$

$$\delta = \frac{\sqrt{r^2 + \tan^2\theta(2r\Delta - \Delta^2)} - (r-\Delta)}{(1+\tan^2\theta)} \quad 3.6$$

Equation (6) is the solution of the quadratic equation (5) and gives the values for 'δ' which in turn can be used to estimate the effective void size 'D' using equation 7;

$$D = 2(\Delta - \delta) \qquad 3.7$$

Table 3.1 summarize the calculation results of the mathematical model developed in equations (1-7) and illustrate the effect of varying parameters on the final void size. Note that the lithography defined hole size ('R') is fixed at 500nm for the calculations so as to match our experimental data.

		θ=80^0		θ=85^0		θ=89^0	
Δ ⬇	**H_{Min}**	**δ**	**D**	**δ**	**D**	**δ**	**D**
10	320	6.86	6.27	4.51	11	1.15	17.704
30	368.7	14.7	30.6	8.68	43	2	56.004
50	400	20	60	11.4	77	2.54	94.913
70	423.5	24.1	91.9	13.4	113	2.95	134.09
90	442.1	27.3	125	15.1	150	3.28	173.44
110	457.1	29.9	160	16.4	187	3.54	212.92
130	469.3	32.1	196	17.4	225	3.75	252.49
150	479.1	33.8	232	18.3	263	3.92	292.15

Table 3.1. Final pore diameter for different values of overhang and sidewall angle (Fixed R=500 nm).

As observed from the table, for a particular overhang 'Δ' say 110 nm, the minimum oxide thickness 'H_{Min}' requirement is 457 nm. Now, if our sidewall angle slope 'θ' varies from 80-89^0, the final void diameter is in the range of 160 - 212 nm which represents an impressive possibility of ~ 2.5x - 3x reduction in feature size.

3.3. Process Development

As illustrated in section 3.1, the void transfer patterning process involving the intentional creation of voids followed by controlled etch-back has a great potential for a reliably producing nano-scale pores. However, some vital processes must be modulated in order to get the desired process outcome. These key process adjustments areas are:

3.3.1. Mask Design

As shown in figure 3.3, a special test mask was made using Mentor Graphics mask layout editor and MEBES III electron beam mask writer. It consisted of different shaped test structures including lines for cross-sectional scanning electron microscopy and density varying from 500 nm to 5000 nm and three different '*R*' values of 500, 750 and 1000 nm to verify the packaging density effects on void formation.

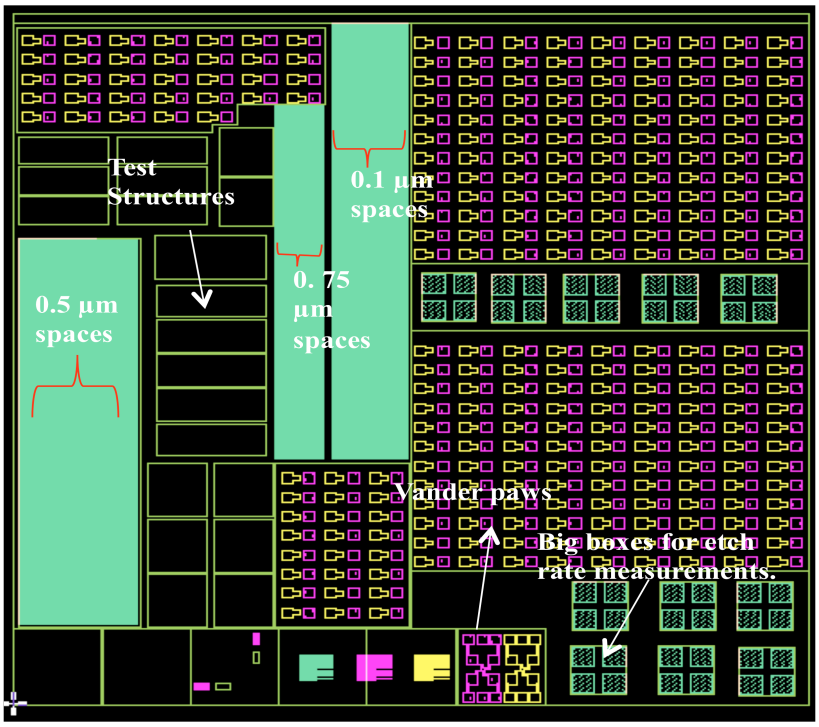

Fig. 3.3. Test mask designed using Mentor Graphics mask layout editor and MEBES III electron beam mask writer.

The maximum exposed area (green regions in the mask represent level I) of the mask was kept lower than 25% to minimize the loading effects.

3.3.2. Stack Formation (Thin Film Deposition)

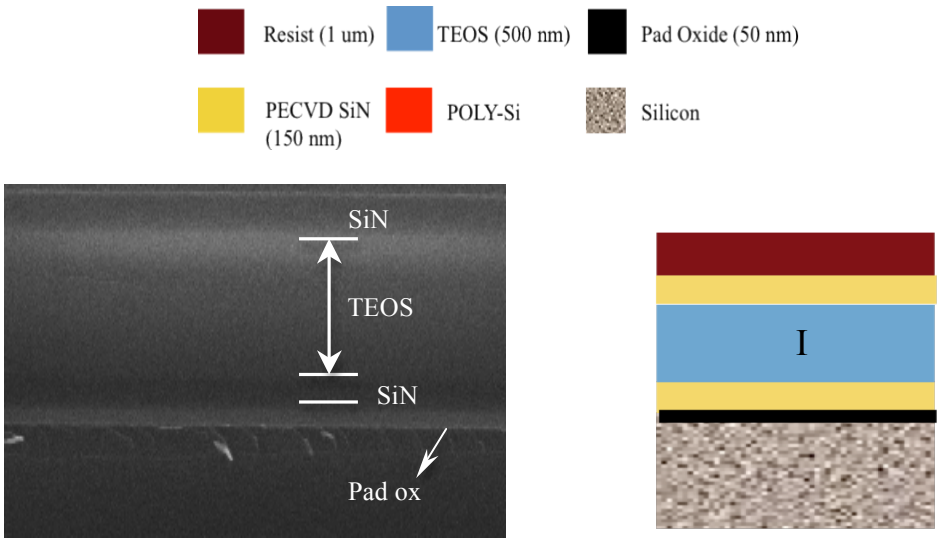

Fig. 3.4. SEM image for the low stress PECVD stack (SiN-SiO_2-SiN) deposited using Applied materials P-5000 (Chamber A and B), and corresponding process flow schematic step 1.

As discussed in chapter 2, the topographical and structural properties of thin films such as grain size, surface roughness, adhesion and stress depends largely on deposition conditions *viz.* surface temperature, surface mobility, kinetic energy of impinging species, pressure, gas source, and surface topography. The thin film stress and adhesion being paramount. Poor adhesion poses a potential reliability problem if the film lifts-off and results in device failure, whereas the higher stresses in films may cause following problems: Poor adhesion leading to de-lamination, corrosion, brittle nature of films leading to cracking under tensile stress and higher resistivity compared to annealed films. Thus, it is pivotal to tune the thin film deposition parameters to control these properties.

In this work, the PECVD SIN-SiO_2-SiN stack was deposited using Applied Materials P-5000 tool. Recipe employed for SiO_2 was 'A6 5K TEOS LS' in chamber A and PECVD Nitride recipe 'B-6 1500 CON NIT' (see recipe details in appendix III). Franceschinis *et al.* characterized the existing low stress PECVD Nitride recipe 'B-6 1500 CON NIT' at RIT. The maximum compressive stress of 1.5E9 dynes/cm^2 at 600 watts, tensile stress of -4.9E8 dynes/cm^2 and -7.2E8 dynes/cm^2 at 400 watts and 500 watts respectively is reported [2] [3]. A thermally grown pad oxide layer using 'recipe 250' in Bruce furnace tube 4 featuring thickness one-third of the required nitride thickness helps lower stresses in nitride deposited films by acting as a buffer. The buffer pad oxide layer compensates stress by reducing lattice mismatch and the thermal expansion coefficients difference between film and substrate.

The author of this work suggests tuning of pressure and power to lower stress. For *e.g.* tensile stress in films is a signal to lower down the pressure and augment the power and continue until minimal or zero tensile stress is achieved depending on the tolerance. On the other hand, increasing pressure and reducing power can eliminate compressive stress. In the case of PECVD, too low of pressure may also extinguish the plasma or if the pressure has been turned up too high, plasma becomes unstable and can causes arcing. This necessitates pressure/ power equilibrium to keep thin films stresses within a process tolerance.

3.3.3. Photolithography Optimization

A key to anisotropic etching is an etch mask that is a) fairly square-topped, and b) offers high etch selectivity with respect to films being etched. Although, resist is most widely used as an etch mask, but, is not good for high aspect ratio etching because it is

readily attacked by the etch chemistries used. Many approaches have been used to improve the etch resistance capabilities of resists such as hard baking the resists at near glass transition temperatures. But, this leads to serious reflowing of resist owing to higher temperatures leading to rounded-resist tops, which itself is problematic and may cause undue increase in CD's due to mask erosion and faceting issues during etching. The corner of resist is always rounded even when the mask walls are vertical. These corners etch faster and erode quickly than the other areas. The corner-faceting is described in detail in chapter 2. The faceting can be controlled by an ideal or near-squared resist top profile. The techniques available for increasing the etch endurance of the resist mask are UV-hardening and e-beam hardening [4], but they are not feasible here at RIT due to special tool requirements. Therefore, this necessitates developing of a process to achieve desired initial profiles using toolset available at RIT.

Fig. 3.5 show the resist profiles when using standard RIT 'coat' and 'develop' recipe on SSI track. The rounded resist tops and overexposure effects for both the densely and sparsely packed features can be seen. Increased reflow is observed in more-widely spaced features because of more even heat distribution. Fig 3.6 show the undesirable after effects of etching Aluminum with such resist masks with rounded tops. As seen in the SEM picture, dual etch fronts were created by mask erosion that eventually lead to increased feature CD's.

Suppressing Resist Round-off

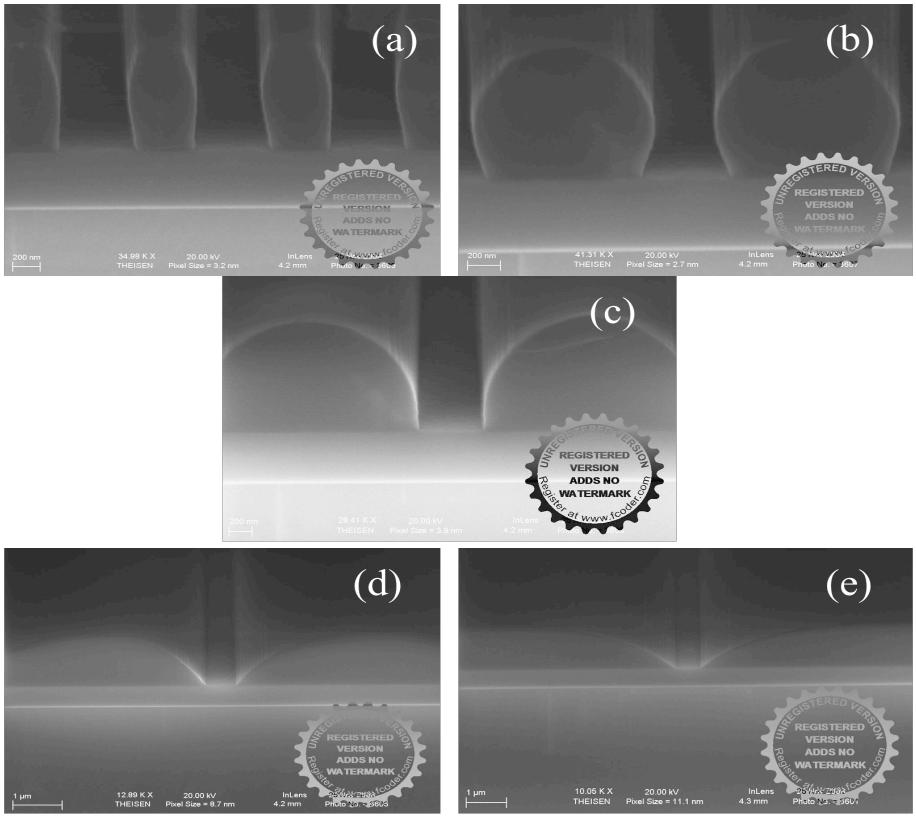

Fig. 3.5. Initial resist profiles showing rounded resist tops and overexposure effects for varying density features. Increased reflow is observed in widely spaced features. The pitch varies from a) 1, b) 1.5, c) 2.5, d) 5.5 and e) 10.5 μm as seen in the figure.

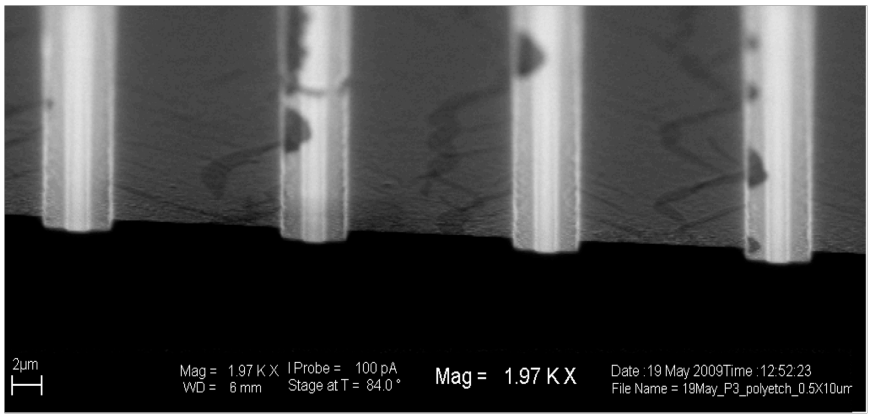

Fig. 3.6. Aluminum etching results using initial resist profiles resembling Fig. 3.5.

Canon i-line stepper at RIT has a minimum resolution limit of 0.5 µm. Since, the stepper is being to its limits and the process window is extremely small, a Focus-exposure matrix (FEM) is required to find the correct dose and focus settings. Figure 3.5 showed rounded resist tops and indications of a possible overexposure or inefficient exposure manifested by standing waves owing to a higher film stack reflectivity. Consequently, to start with, the entire stack was simulated using 'Prolith' (lithography optimization simulator). The reflectivity component from the different layers of stack and the range of dose to clear and focus settings was simulated and given in figure 3.7. The simulation results indicate a comparatively lower reflection from the top SiN - SiO_2 interface for the SiO_2 thickness range of 500-550 nm, which is good considering our H_{Min} > 500 nm requirement as described in section 3.2.1. Eventhough, the simulator suggests a lower reflectivity from bottom SiN for a thickness range of 120-130 nm, a higher thickness is chosen for effective pattern transfer during etch-back.

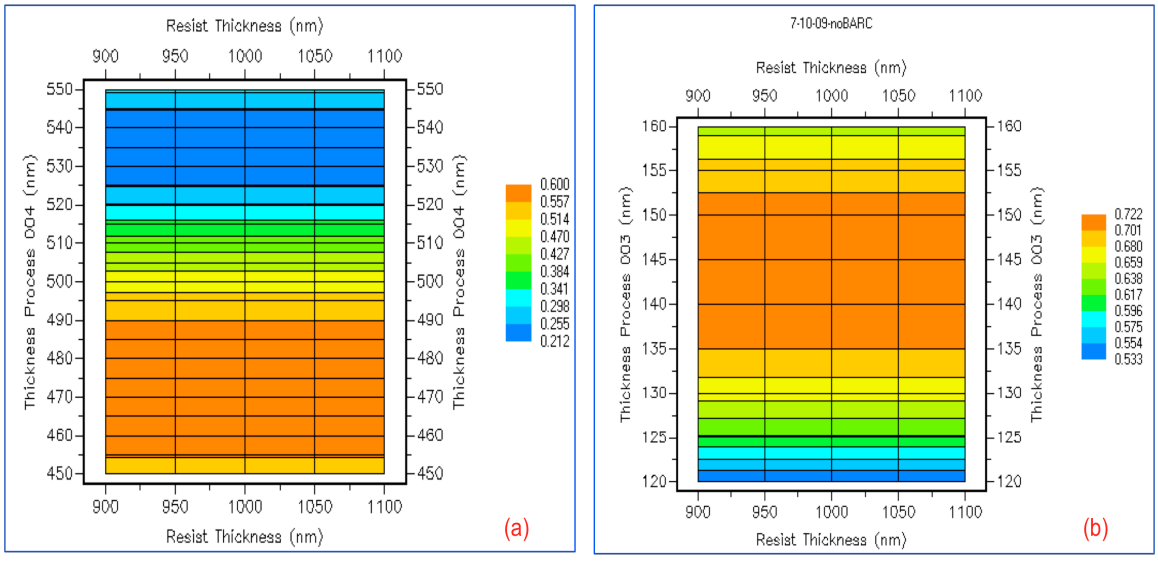

Fig. 3.7. Reflected component from different interfaces in SiN-SiO_2-SiN stack: a) reflection from top SiN-SiO_2 interface, b) reflection from SiO_2- bottom SiN interface. Lithography simulation done using 'Prolith'.

Improving Resist Etch Endurance

An intrinsic trade-off exists amid the etch endurance improvement available by higher post development bake temperatures and the rounding of the resist profiles due to high temperature reflow; both being equally important. Thus, experiments were performed to find the right hard bake temperature in-order to improve the etch resistance of a resist mask. Fig. 3.8 show the final results of resist mask optimization employing lower hard-bake temperature (130 ^{0}C for 2 minutes as compared to standard 145 ^{0}C for 1 minute) and the best focus and exposure settings determined by FEM on this film stack. Therefore, a longer and low temperature hard bake is suggested to control the reflow.

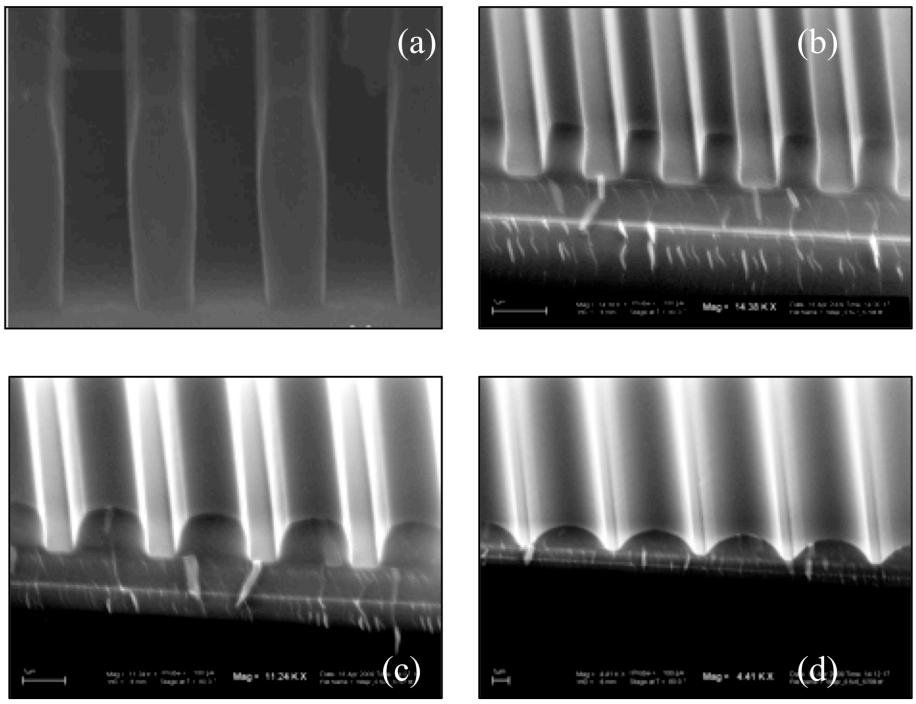

Fig. 3.8. Optimized resist profiles for varying density. The pitch varies from 1 µm, 1.5 µm, 2.5 µm and 5.5 µm. Figure (d) still shows the rounding of resist tops associated with reflow during post development bake (hard bake).

It can be interpreted that lowering the hard-bake temperature can significantly lower the resist-rounding effect yielding anisotropic etch friendly resist mask profiles. Next step is to test the resist endurance by etching films underneath the resist.

3.3.4. Dry Etch Process Development: Process Flow Step 2

As described in previous sections, existing lithographic processes are inadequate and new processes coherent to this work are needed. A trade-off between selectivity and anisotropy is inherent to an RIE process. As clarified in section 3.2.1, anisotropic etching is crucial step for this work and trade-off with this parameter needs to be minimum considering the process requirements. This section delineates three different approaches used in this work in order to develop an efficient anisotropic dry etch process while employing an optimized resist mask.

Goal: To develop highly anisotropic etch process for etching SiN-PECVD SiO_2-SiN stack stopping at bottom SiN with high SiN/ SiO_2 and SiO_2/ SiN selectivity ratios.

Approach I

Resist Coat (SSI track)	Coat.rcp
Exposure (Canon i-line stepper)	260 mj/cm^2
Focus	0.65
PEB	110 ^{0}C for 1 min on hot plate
Hard bake	130 ^{0}C for 2 min on hot plate
Develop	Manual CEE developer, program 1
Etching	Drytek Quad RIE tool

Table 3.2: Details of parameter employed in approach I for dry etch process development.

As discussed in detail in chapter 2, experimental design procedures and response analysis are valuable tools to explore important variables and to fine tune an etch process as desired. The trend table given in chapter 2 can assist in reducing the data required to design an efficient experiment.

Based on these trends, the factorial experiments were designed (first coarse and then fine-tuned experiments) and conducted. The factors adjusted were power, pressure and gas flows and the response variables were anisotropy and selectivity. Figure 3.9 shows the etching results when the best settings were employed out of the design matrix. Table 3.3 displays various parameters employed in order to achieve the best settings.

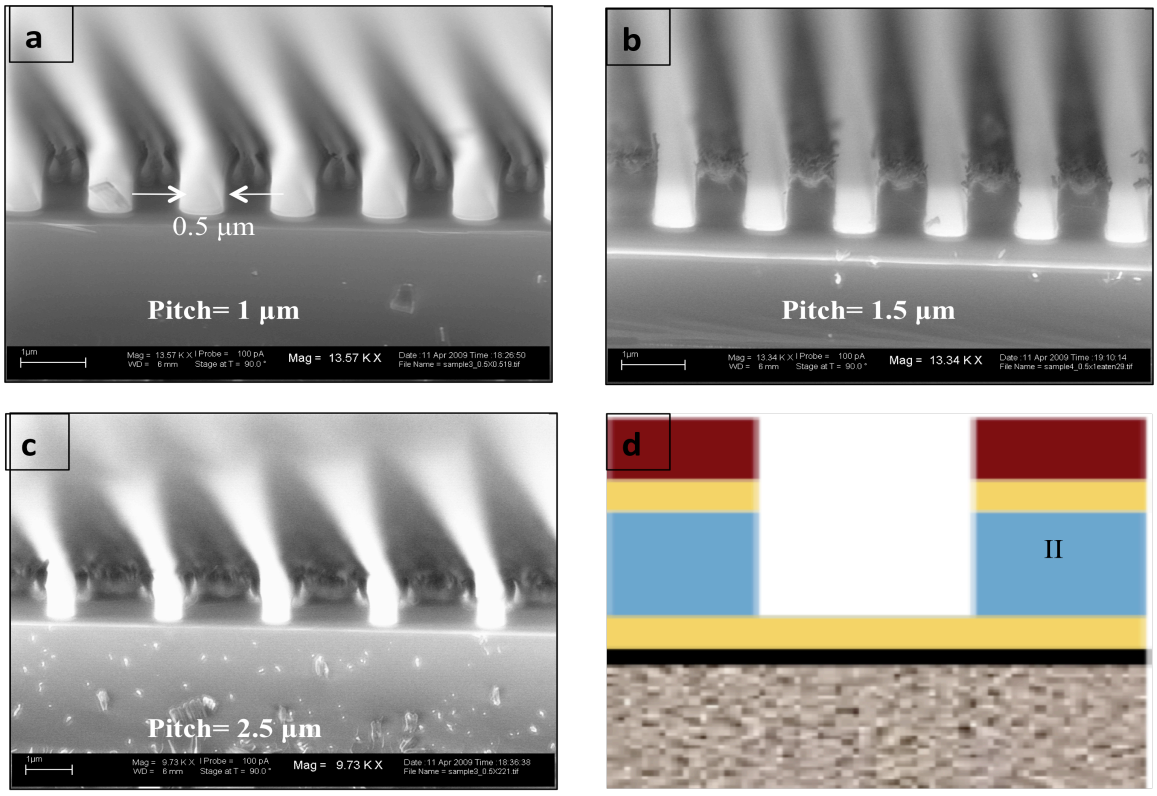

Fig. 3.9. (a-c) SEM images showing etch results for approach I, (d) process flow step 2.

As seen in Figure 3.9, the resist hard baked at temperature lower than normal hard bake temperature of 145 ^{0}C barely survived the etch attack by fluorine based chemistry. It seemed like some highly energetic etch species that were able to pierce through the resist, and thereby started etching the underlying film slightly. Hence, lowering the resist hard bake temperature might not be a good trade-off to get the desired etch characteristics. Even though not the best, these settings did give a close enough results. This attempt yielded best LPCVD Si_3N_4/ annealed PECVD SiO_2 etch selectivity ever reported at RIT using flouring based chemistry with high degree of anisotropy.

PECVD and LPCVD Nitride Etch- Drytek Quad RIE tool (Timed etch Mode)					
		Nitride Etch (Recipe: GuriNitr step1- chamber 2)			**PECVD SiO_2 Etch (Recipe: GuriNitr step2)**
Gas flows (sccms)	**CHF_3**	35			70
	SF_6	30			0
	Ar	0			75
	O_2	0			10
Power		205 W			210 W
Pressure		40 mTorr			55-60 mTorr
		PECVD Nitride (Patterned)		LPCVD Nitride (Patterned)	
Measurement Area		Dense Lines (SEM)	Big Boxes (Nanospec)	Big Boxes (Nanospec)	Big Boxes (Nanospec)
Etch Rates (in nm/sec)		2.92	3.86	3.14	1.12
	i-line resist (no HB)	2.3			NA
Selectivity		**Si_3N_4/ SiO_2 ~ 2.4**			SiO_2 / Si_3N_4 ~ 0.6

Table 3.3. Different etch parameters used in approach I. Best LPCVD Si_3N_4/ annealed PECVD SiO_2 etch selectivity ever reported at RIT using flouring based chemistry with high degree of anisotropy in this work.

Hybrid Approach II

This approach is a blend of above method with a newer technique where stack etching is split between two tools *viz.* Drytek Quad for etching nitride using nitride etch recipe developed in approach I followed by PECVD SiO_2 etch in Applied materials P-5000 MERIE tool (Chamber C). No Hard bake was performed in this technique to restrict the resist flow as shown in table 3.4.

Resist Coat (SSI track)	Coat.rcp
Exposure (Canon i-line stepper)	TBD from FEM on film stack
PEB	110 ^{0}C for 1 min on hot plate
Hard bake	**Not performed**
Develop	Manual CEE developer, program 1
Etching	Drytek Quad RIE for Nitride and P-5000 MERIE for PECVD SiO_2

Table 3.4. Details of parameters employed in approach II for dry etch process development

The whole idea of using two different tools is due to the tool restrictions on etching Nitride in P-5000. The success of this recipe lies in the fact that resist is less severely attacked during this approach. Resist erosion is more aggressive when utilizing step 2 of '*GuriNitr*' etch recipe for PECVD oxide etch. However, the resist integrity is more when etching PECVD oxide in MERIE as compared to etching in Drytek quad tool. This is attributable to the fact that a higher degree of anisotropy along with increased selectivity can be achieved by the use of comparatively higher pressures assisted by magnetic field as employed in this recipe. Therefore, it can be observed from the etch results shown in figure 3.10 that this split approach yielded the desired anisotropic etch results with improved mask and film selectivites. Table 3.5 displays the necessary etch parameters employed in this technique.

PECVD SiO_2 Etch- P5000 MERIE Chamber C Recipe C-6 Oxide Experimental (Timed etch Mode)				
Gas flows (sccms)	**CHF_3**	100		
	CF_4	50		
	O_2	15-20		
Power		500 W		
Pressure		250 mTorr		
Magnetic Field		40 gauss		
Measurement Area/ Techniques		Unpatterned wafer	100 µm box (nanospec)	Dense Lines (SEM inpection)
Etch Rates (nm/sec)	Unannealed PECVD SiO_2	2.61	2.5 - 3.0	2.29
	Oir 620M i-line resist (no Hard Bake)	2.35	NA	NA

Table 3.5. Different etch parameters used for anisotropic PECVD SiO_2 etch in P5000 MERIE Chamber C.

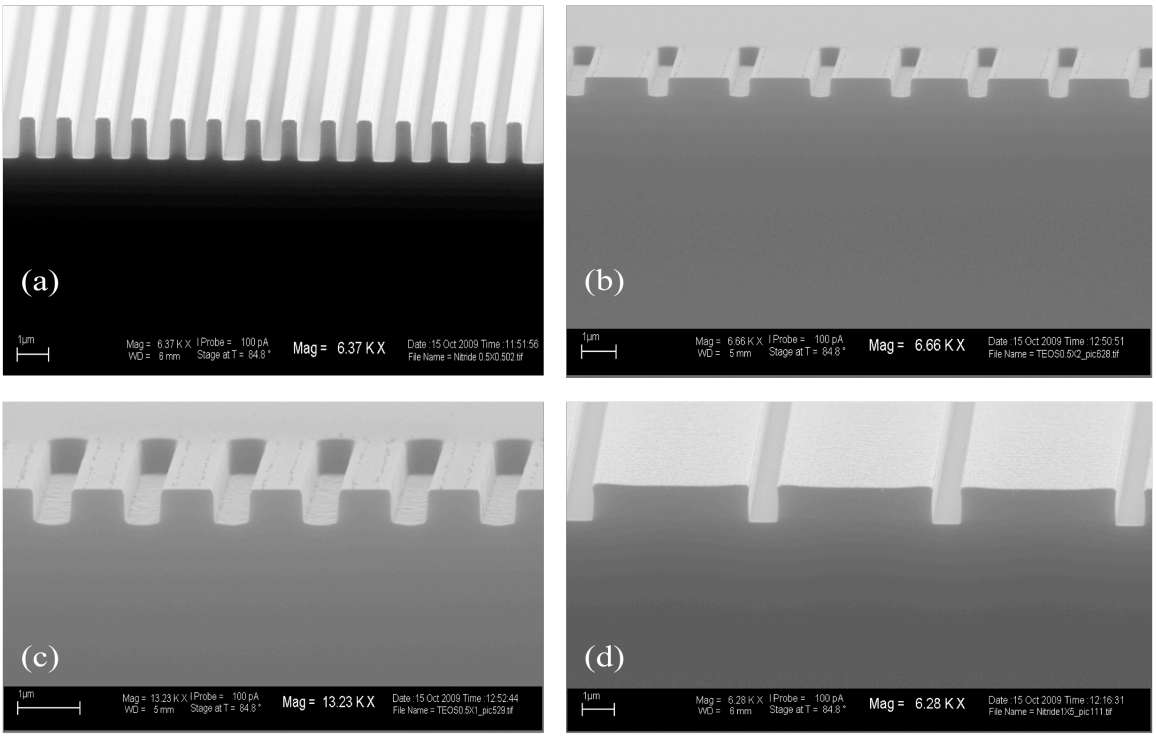

Fig. 3.10. SEM images showing highly anisotropic stack etching for a pitch of a) 1 µm, b) 2.5 µm, c) 1.5 µm, and d) 5.5 µm.

The in graphs in figure 3.11 plots the etch rate variations due to microloading. It can be seen that denser features etch slower (primary axis) than sparse features and bigger features etch faster than smaller features (secondary axis).

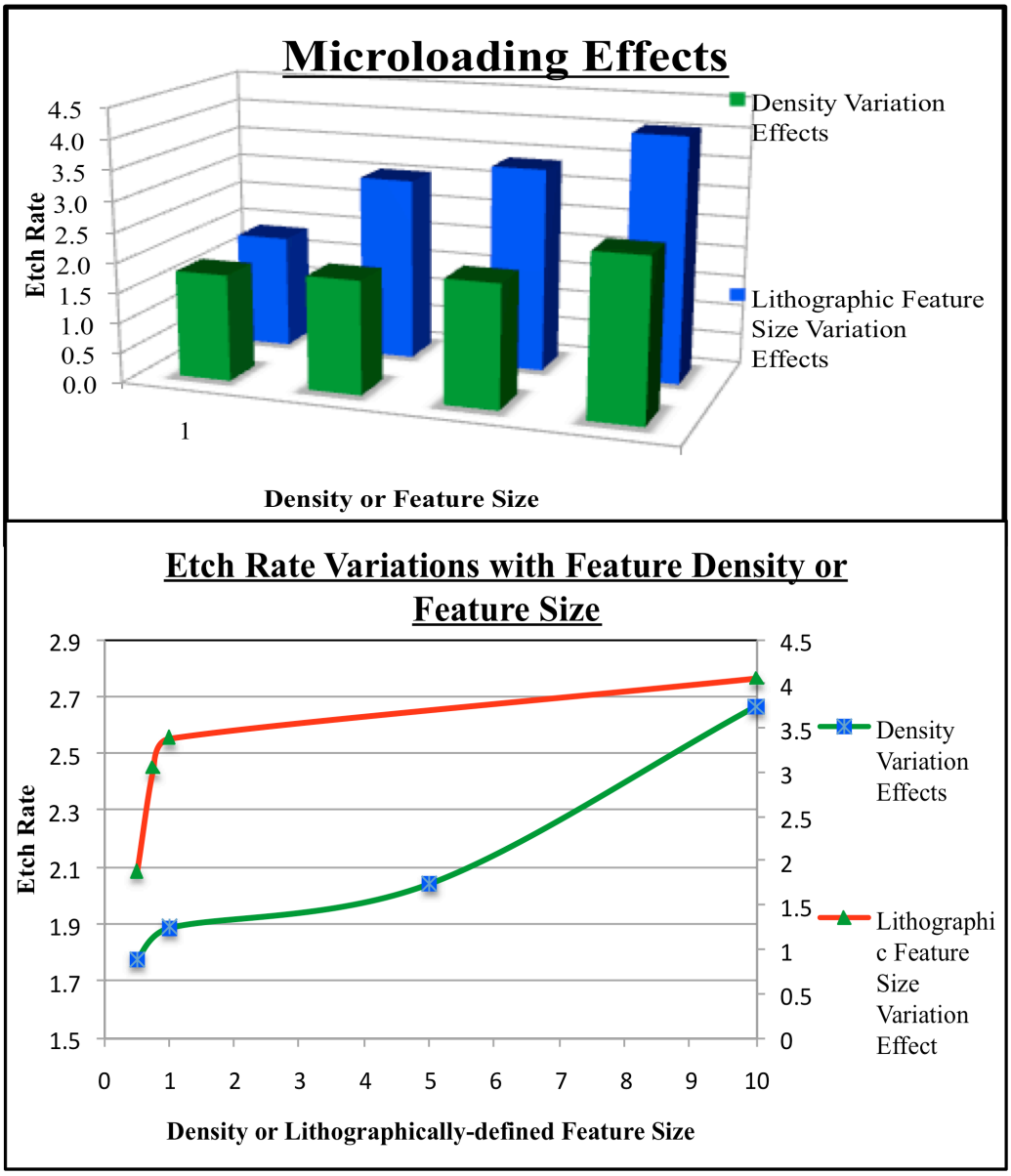

Fig 3.11. Micro-loading effects affecting the MERIE etch rates for unannealed PECVD oxide. Density varies as 0.5, 2, 5 and 10 µm and feature size varies from 0.5, 0.75, 1 and 10 µm. All measurements are approximate and derived from SEM images

Therefore, these considerations must be taken in to account while calculating the etch rates to etch features of desired size and density. The etch rates were henceforth measured in big boxes using nanospec and corresponding over-etch time factor was added to etch the smallest and the densest features.

Approach III: Use of Aluminum Hard Mask

Another alternative approach considered in this work was the use of Aluminum hard mask. In this technique a thin layer of Aluminum is patterned using a resist mask and the pattern is transferred into the Aluminum film by a successive dry etch. This patterned Aluminum (as seen in figure 3.12) then serves as a hard mask for any subsequent etching because it has a higher tolerance to fluorine based dry etch chemistries. The stack etch can then be performed using any of the above techniques II or I. This approach will not be described in detail in this work but results are shown for the sake of completion.

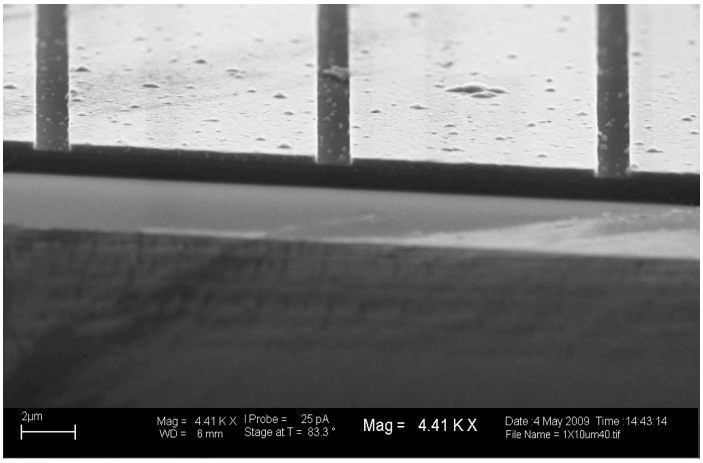

Fig. 3.12. SEM image showing that the Aluminum etched anisotropically using the recipe developed in this work.

- BCl_3 helps removes hard to remove oxide layer. Etching would not proceed if this layer is not pierced through and therefore needs ionic bombardment.
- N_2 is used as purge gas or diluent
- CFORM helps in achieving anisotropy by sidewall passivation

Step #	I	II	III	IV	V
Pressure (mTorr)	100	100	100	100	0
RF top	0	0	0	0	0
RF bottom	0	250	125	125	0
N_2	10	10	15	20	20
BCl_3	35	35	20	20	0
Cl_2	10	10	20	20	0
CFORM	5	5	5	5	5
	Stabilize (15 sec)	Time=20 sec	EtchTime= ??	Over etch Time= ??	

Table 3.6. Details of various parameters used in Aluminum etch recipe.

3.3.5. Overhang Formation: Process Step 3

As elucidated in critical design parameters in section 3.2, the amount of overhang 'Δ' determines the diameter of the void formed, and therefore the size of the final nanopore feature. Therefore, creating an overhang 'Δ' using a selective wet etch is a crucial step in the process flow. The recess in oxide layer is created by exploiting isotropic etch properties of buffered hydrofluoric acid (BOE) in concentration of 5.2:1. BOE etches oxide selectively over nitride thereby receding the oxide edge by an amount 'Δ' called the overhang as illustrated in figure 3.13. Calculations based on the mathematical model developed in section 3.2 assists in deciding the overhang size required in order to get the desired feature size. Once the overhang size required is

determined, the wafers were etched for time determined by etch rate of unannealed PECVD oxide using formula below:

$$\text{Time to Etch} = \frac{\Delta}{E.R} \qquad 3.8$$

Where E.R. is the etch rate of unannealed PECVD SiO_2.

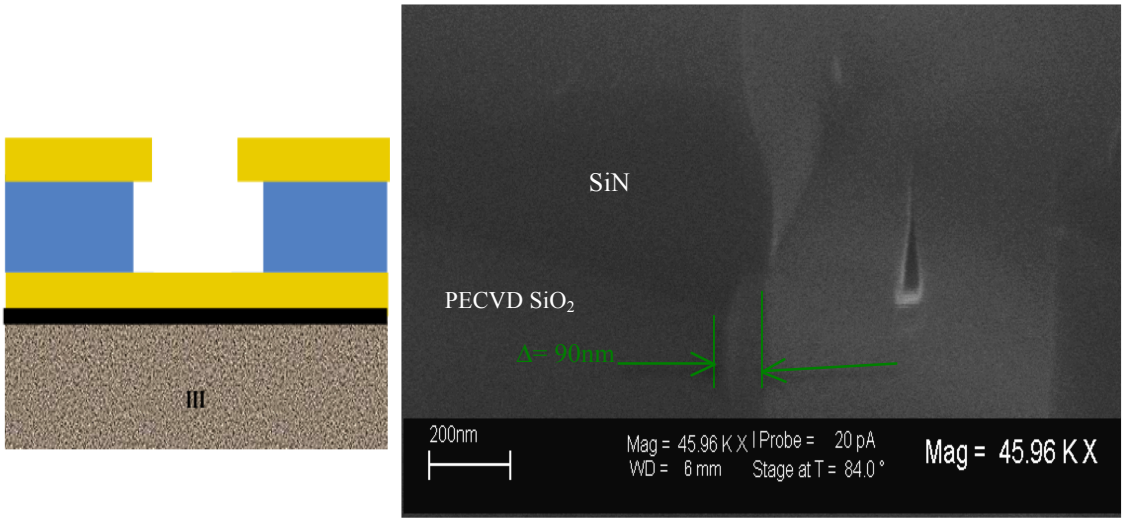

Fig. 3.13. Process flow schematic step 3 (left), SEM image showing the overhang formed in oxide layer (right).

3.3.6. Polysilicon Deposition: Process Step 4

One of the assumptions in deriving a mathematical model for void transfer patterning process was that the film deposition must be highly conformal. This is vital for preventing any artifact factor from playing a decisive role in void formation process. This factor can self-couple with the existing parameters and start affecting the void sizes, thereby, making the size predictions by the model very complex. Thus, the film that pinches off at top to deliberately form bottle shaped voids as shown in figure 3.14 needs to be highly conformal. LPCVD films are typically very conformal in nature. Therefore, LPCVD polysilicon is chosen as the filling layer. Polysilicon was deposited using

standard LPCVD Poly 610 recipe. Deposition parameters are as follows: (See appendix III for details)

Temperature = 610 °C
Pressure = 300 mT
Silane flow =25 sccm, Deposition Rate = 80 Å/min
Chemical reaction: $SiH_4 = Si+2H_2$

The deposition temperature should be kept as low as possible to minimize the thermal budget of the void transfer patterning process for potential backend applications. Lower deposition temperatures and higher deposition rates yields amorphous films with smaller grain size. The conformality of the above LPCVD polysilicon process seems reasonably good as shown in figure 3.15.

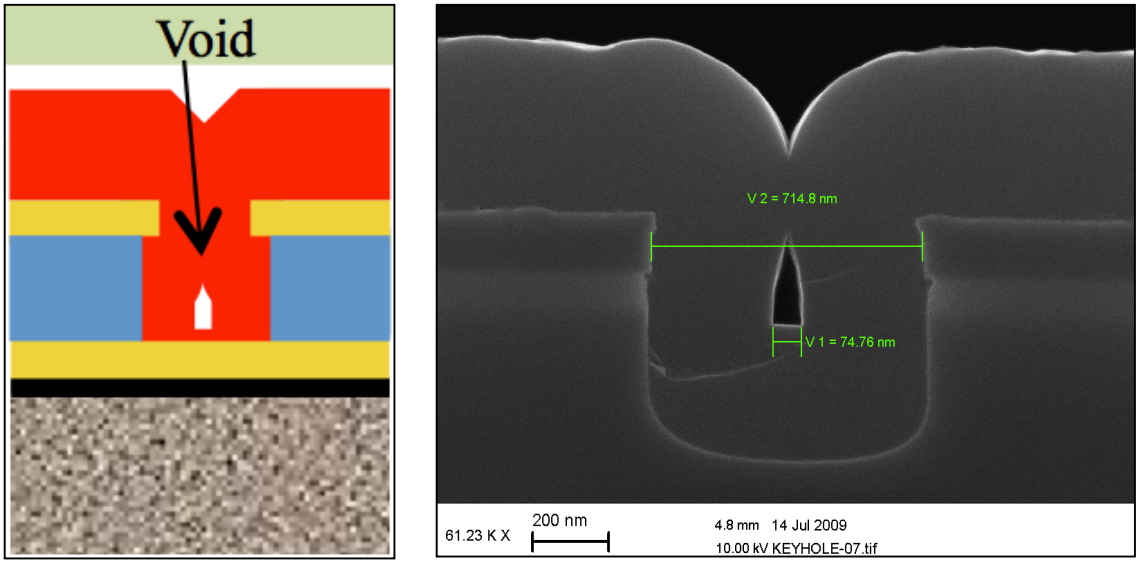

Fig. 3.14. Process flow schematic step 4 (left), SEM image showing the void formed in polysilicon (right). The combined effect of overhang and the conformal polysilicon deposition pinches off at top to intentionally form bottle shaped voids. Image courtesy Keith Fogel, IBM T.J. Watson research center.

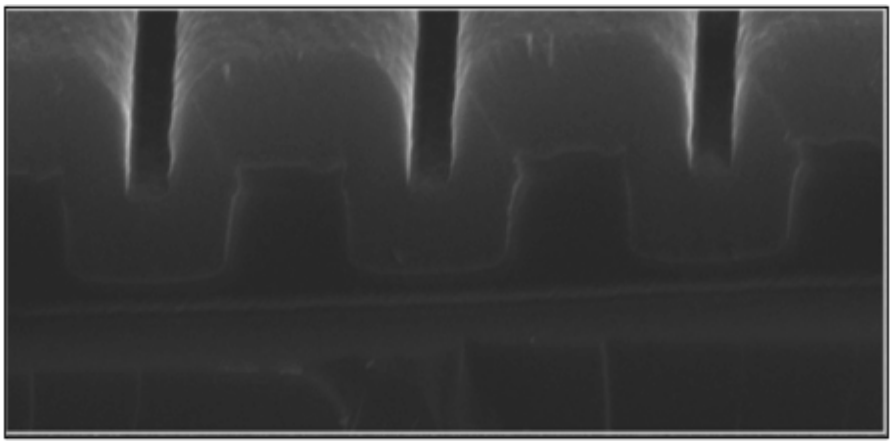

Fig 3.15. SEM micrograph showing conformal nature of 610 poly recipe.

3.3.7. Void etch-back for Pore Definition: Process Step 5

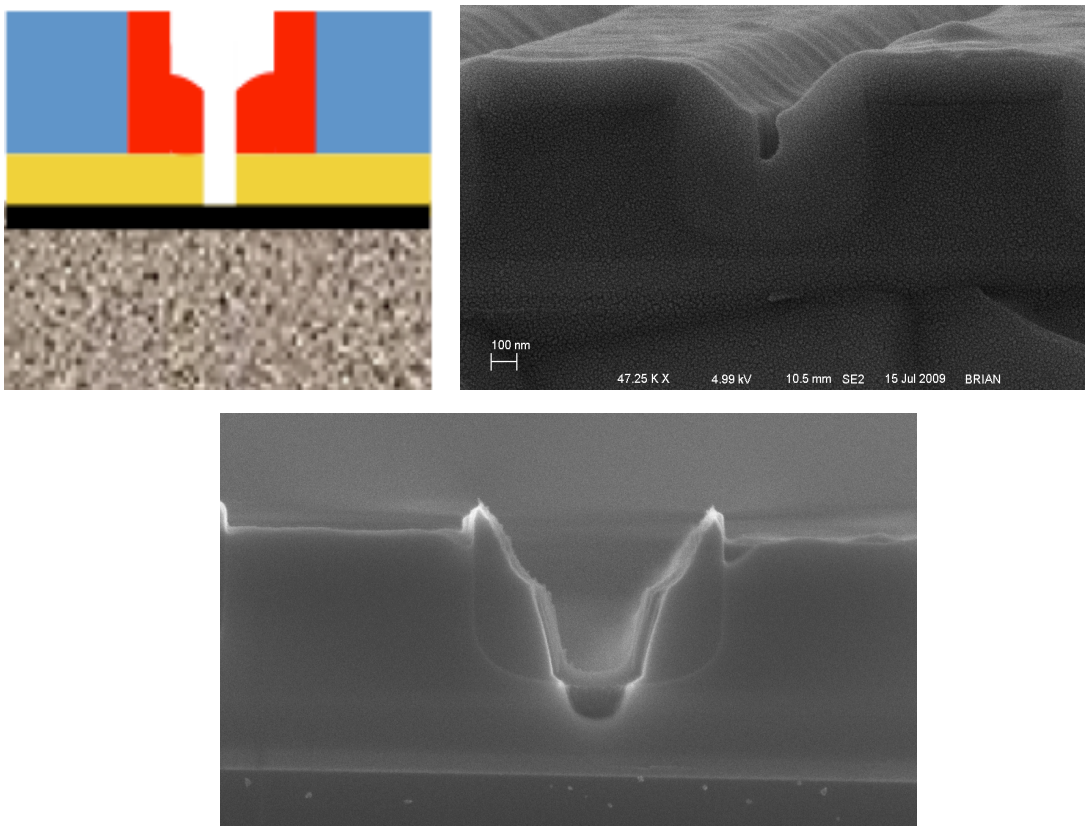

Fig. 3.16. Process flow schematic step 6 (left), SEM micrograph showing the void etch-back in progress (right, bottom). Image courtesy Brian mcIntyre from UofR.

The precise and accurate polysilicon etch process is pivotal in etching down the voids to bottom nitride layer with minimal CD variations or shifts from the void size. Thus, the etch-back process needs to be highly directional. Table 3.7 show the etch parameters for polysilicon etch recipe developed on Drytek Quad RIE tool at RIT. 'Facpoly recipe' was used as the baseline process to develop a new recipe that employed lower pressure and higher power to assist directionality. SEM results confirm lesser than 20% CD shift with this recipe. It is extremely difficult to control the etch process for variability lower than 20% due to the tool limitations. Maintaining etch parameters such as pressure and gas flows within a range was onerous and tool related deviations might be held accountable for the observed CD variations. Figure 3.16 shows the void etch-back process in progress. Therefore, it is not the process related limitations but the inherent isotropic component and tool limitations of an RIE tool that ultimately dictates the patterning potential of this technique. The tool variations over a period of time make feature CDs even more erratic. Even with these limitations the void transfer process at RIT has a patterning capability below 180 nm.

Polysilicon Etch-back (Timed etch Mode) FacPoly Recipe: Chamber 2		
Gas flow (Sccm)	**CHF_3**	30
	SF_6	30
Power		180 W
Pressure		35 mTorr
DC Bias (display)		~ 420 W

Table 3.7. Details of various parameters used in Polysilicon etch recipe.

3.3.8. Left-over Polysilicon and SiO_2 Wet Etch: Process Step 6

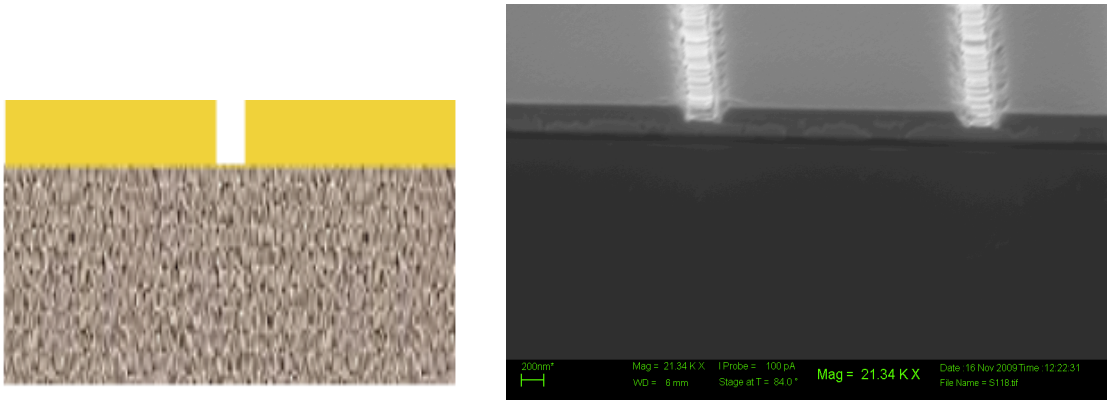

Fig. 3.17. Process flow schematic step 6 (left) and the actual SEM micrograph displaying the small pore defined in SiN layer after the polysilicon and SiO_2 etch (right).

Once the pore is defined by etch-back process, the last step in this patterning technique is the removal of polysilicon stingers and the left over SiO_2 layer. This etch step is particularly critical since high etch selectivity with respect to other layers is required. Thus, the bottom SiN and the underlying layer exposed in regions where pores are formed needs high etch resistance to any attack by the etch chemistry. In our process the layers underneath are pad oxide and silicon substrate. This step was preceded by O_2 plasma ash in Branson IPC 3200 Asher to remove any organics or the polymer deposits post polysilicon etch that might hinder the wet etch process.

The ability to etch silicon or polysilicon after metallization is extremely desirable in CMOS, MEMS and bio-electronic applications. But, most of the etch chemistries would attack the metals such as aluminum, tantalum or other refractory metals. However, solutions to etch these metals selectively over metals have been reported by Yan *et al.* and Thong *et al.* Considerable Aluminum etch rates reduction has been reported by the addition of the ammonium peroxodisulfate and dissolving certain amount of silicon in

TMAH solution [5]. The TMAH solution is more favored for etching polysilicon since it is CMOS compatible and does not cause mobile K^+ ion contamination often confronted in the KOH type etch chemistries. Secondly, it is less toxic as compared to EDP. Last but not the least, this whole patterning process is developed for back end friendly applications. Usually, the regions exposed under pores in such applications are metals such as Tantalum, Aluminum or Molybdenum acting as back end metal electrodes or interconnects. Thus, TMAH is used because it is very selective in etching polysilicon over these metals [7].

A two-staged, CMOS compatible selective wet etch process was developed that utilizes tetra-methyl ammonium hydroxide solution (TMAH) and the buffered hydrofluoric acid to remove polysilicon stingers and then the remaining PECVD SiO_2 respectively. CD-26 developer containing ~ 2.3% TMAH is available in SMFL at RIT and should be suitable for etching polysilicon selectively over SiN and SiO_2. During the first stage, CD-26 heated to temperatures > 80 ^{0}C [5] is used to etch polysilicon. This chemistry would not etch pad-oxide and therefore protects the underlying silicon from etching. Once the polysilicon is etched, remaining oxide can be etched by using buffered HF (BHF 5.2:1) and we are left with just the desired pores in SiN layer as seen in figure 3.17.

3.4. Process Flow

The complete process flow outline for the void transfer patterning process is shown in table 3.8 below:

Step #	Process Step	Recipe and process details	Special Instructions	Tools
1	Wafer Scribe	Verify Wafer	Scribe lot number at the flat (backside) Record the same in notebook	Diamond Scribe
2	RCA Clean	See Appendix III (See RCA bench wall for cleaning procedure)	Do not add H_2O_2 until the bath warms up to 75°C.	RCA Bench
3	Pad oxide	Recipe 250	Target oxide thickness = 500A Include 5 dummy wafers at front and behind the device wafers.	Bruce Furnace-Tube 4
4	PECVD nitride	B6 1500 CON Nitride (See Appendix for recipe details)	Target=1500 A, Add monitor to check deposition rate. Measure Nitride thickness (use Spectramap SM300)	P-5000 Chamber B
5	PECVD oxide	Recipe: AK 6" LS 5K (See Appendix III)	Target=5000-6000A (Add monitor to measure dep rate first).	P-5000 Chamber A
6	PECVD nitride	B6 1500 CON Nitride (See Appendix III for recipe details)	Target=1500 A, Use monitor to measure Nitride thickness (use Spectramap SM300)	P-5000 Chamber B
7	Level 1 Photo	SSI track-Coat.rcp, Canon Stepper, jobfile: Keyhole Manual CEE developer prog. 1 (See Appendix III)	Include 3 dummy wafers before coating. Use Manual CEE developer. **Only 1 min Post Expo bake at 110 ^{0}C , No Hard bake.**	SSI Track coater, Canon Stepper, manual CEE developer
8	Nitride Etch ****	Recipe: GuriNitr step1 (Details in Appendix)	Use monitor wafer to measure etch rate and profile X-SEM (optional)	Drytek Quad Chamber 2
9	Oxide Etch****	Use Drytek Quad recipe GuriNitr step2 **or** P-5000 Experimental etch recipe (See Appendix III)	Use monitor wafer to measure etch rate and profile XSEM (optional)	Drytek Quad 482 dry etch Or P5000 MERIE (Chamber C)
10	Resist Ash	6" Factory recipe	Check to see if resist has been removed. Use 6" normal ash recipe to remove remaining resist	Branson IPC 3200 Asher
11	Overhang structure	Use MOS grade BOE 5.2:1	Etch time depends on calculated Delta. Note etch Time.	
12	LPCVD Polysilicon****	Poly 610 recipe, Temperature = 610 °C SiH4 = Si+2H2, Pressure = 300 mT Silane=25 sccm, Rate = 80 Å/min	Target poly thickness (calculate using mathematical model) (Profile XSEM optional) Use monitor with 1000 A^0 oxide to determine Poly thickness	ASM LPCVD
13	PolySi Etch back	Modify Facpoly Recipe (details in Appendix)	**Recipe details in section 3.2.2.6.**	Drytek
14	Etch Poly and SiO_2 stingers	CD-26 developer, Temp.80 ^{0}C, and then 5.2:1 BOE (See appendix)	CD 26 developer is ~2.3 % TMAH **See section 3.2.2.6.**	CD-26 developer
****	Characterization SEM LEO-Evo	Cleave the monitor wafer along the long test lines for XSEM		LEO SEM EVO-50

Table 3.7. Complete process flow for void transfer patterning process.

References: Chapter 3

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2. **http://people.rit.edu/lffeee/pecvd_recipes.pdf**

3. **http://people.rit.edu/lffeee/stress_measurement.pdf**

4. R.A. Morgan, C.J. Pollard, "Enhancement of resist plasma erosion rates by electron-beam hardening," *Electronics Letters*, vol.18, no.24, pp.1038-1040, November 25 1982

5. G. Yan, P.C.H. Chan, I.M. Hsing, R.K. Sharma, Y. Wang, "Improved TMAH Si-etching solution without attacking exposed aluminum", *Sensors and Actuators A: Physical*, vol. 89, pp. 135-141, Mar. 2001.

6. J.T.L. Thong, W.K. Choi and C.W. Chong, " TMAH etching of silicon and the interaction of etching parameters", *Sensors and Actuators A*, vol. 63**,** pp. 243–249, 1997.

7. K. R. Williams*,* K. Gupta*,* and M. Wasilik, "Etch Rates for Micromachining Processing—Part II", Journal of Microelec. Systems, vol. 12, NO. 6, pp 761-778, December 2003.

CHAPTER 4

Process Simulation And Experimental Verification

The entire pattering process is simulated using process modeling tool known as ATHENA by Silvaco to prove the miniaturization capability and to get in-depth understanding of the critical process parameters. The merits of process simulations include; faster technology development cycles by substituting the expensive experiments with simulations, the process simulators can forecast the profile structures by solving equations detailing the physics and chemistry behind the semiconductor processes. These simulations provide information that is difficult or immeasurable and predicts and provides process insights. In depth analysis of different aspects of process simulation are specified in [1-3].

However, physical-based simulations involve more meticulous analysis when compared to the mathematical modeling technique developed in chapter 3. Theoretical models developed so far can help predict process capabilities but do not capture any process related physical and/or chemical knowledge to provide structural/profile insights. The aim of the theoretical model was to predict void sizes with minimum complexity by deriving the analytic formulae. Thus, physically based simulation can be an effective substitute to experiments as a source of data. Detailed topographical plasma simulations of reactive ion etching has been developed by Takagi *et al*. [6] by employing 'Elite' Monte Carlo etch module by Silvaco [1]. However, no simulation study of the void transfer process has been reported in the literature. In this study, simulation of void patterning technique for prediction of final feature size obtainable is investigated.

Simulation of the void transfer process has been investigated by employing a simulator module called 'Elite', within the substructure of ATHENA by Silvaco. The investigations include plasma etch module in 'Elite' that employs 2-D Monte Carlo ion transport modeling.

Process Simulator Organizational Framework

ATHENA framework integrates various user-friendly process simulation modules. These modules provide solutions for simulating a wide array of semiconductor processes such as thin film deposition, etch, diffusion, oxidation, and lithography etc.

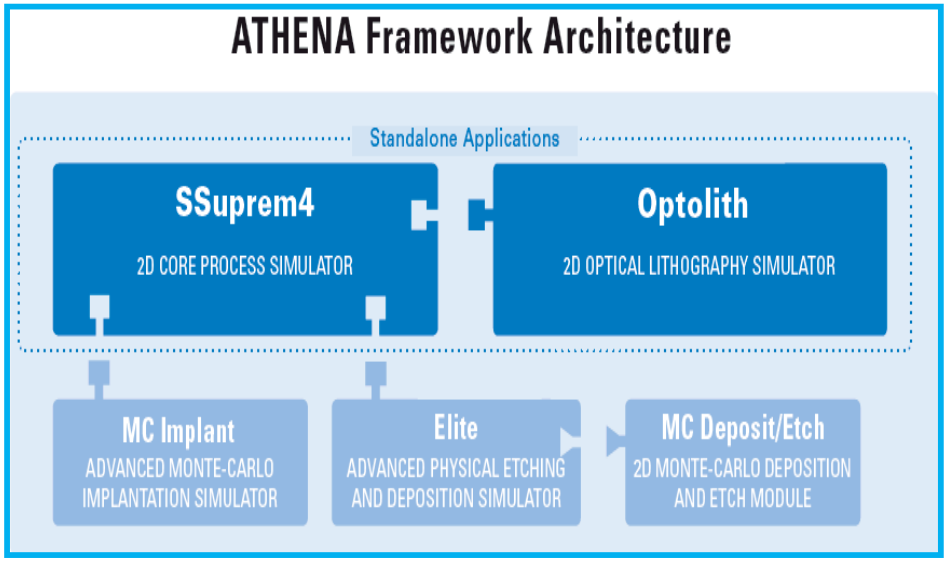

Fig. 4.1. ATHENA Architectural Framework with different interfaced modules. [1]

4.1. Elite Topography Simulator

Elite is an advanced topography simulator for modeling physical etching, thin film deposition, and CMP for semiconductor technologies and organized as a subset within ATHENA Architecture. It is interfaced to an advanced 2-D Monte Carlo atomistic deposition/etch and plasma-etching models in addition to primitive time based

geometrical etching models. All the models in Elite incorporates an algorithm known as "string algorithm" to monitors the topographical changes during the deposition and etching processes, the only exception being the Monte Carlo deposition and etching models.

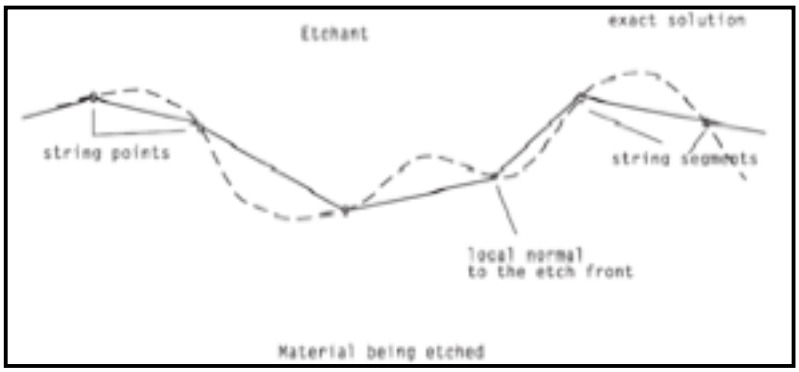

Fig. 4.2. String Model approximation to the Etch Front [1].

In String algorithm, the simulation routine contains information on the materials being simulated in a group of triangles. Every interface is treated in string algorithm as a group of segments that travel in response to a specific process calculation. The moving etch front is simulated by a series of points connected by straight line-segments, making a string. As illustrated in figure 4.2, each point moves perpendicularly to a local etch front with each progressing time increment. The algorithm automatically manipulates the number of segments so as to keep their length approximately equal. Different subroutines are called simultaneously to input the data and to get output of each moving etch front. Two significant assumptions limiting the generality of this algorithm in Elite are: 1) Problems can be solved only in two dimensions, and 2) etch rate is unrelated to the direction of motion of local etch front and the history of the front, thereby making it a

scalar function of position. These limitations lead to some directional and positional errors of a point in a string if the incremental time step is too large [1].

4.1.1. Process Simulation Methodology

The process was simulated using various applicable model parameters in Elite topography simulator. These models can be invoked by defining a machine that imitates experimental conditions in order to model the LPCVD and RIE processes. Process modifications can be implemented easily by altering individual machines without even affecting rest of the simulator. It provides a set of etch models for different physical etching techniques. In order to conduct processing on a structure any model can be selected and invoked. The simulation physics involves the tracking of ion trajectories from the neutral plasma or bulk, through the dark sheath and walls by Monte Carlo method. The user-specified sheath thickness and the calculated mean free path length determines the collision frequency encountered by a particular ion. The final etch rate is estimated from the simulated Monte Carlo distributions that calculate an incident ion flux on the substrate surface and surface evolution is then displayed by string algorithm.

4.1.2. Deposition Models in Elite

ELITE comprises of several deposition models that correlate to different thin film deposition techniques such as PVD, CVD, LPCVD, and evaporation etc. Most of the models were implemented in the topography simulator SAMPLE [1], [4, 5] and were developed at UC Berkeley [1]. The models investigated in this work are discussed briefly in this section, for details of other models and their use user manuals can be referred [1].

Monte Carlo Deposition

Low-pressure chemical vapor deposition (LPCVD) is an important process in semiconductor processing technology. Modeling the polysilicon LPCVD process is important for void transfer process. Parameters *SIGMA.DEP, DEP.RATE, MONTE1* and *ANGLE1* invokes the Monte Carlo based deposition models that can be employed to model low-pressure chemical vapor deposition (LPCVD) [1]. The essential parameters accounted for in this model are physical calculations involving reflection and sticking probabilities of deposited species, surface diffusion, and density variations. Sticking coefficient is important because the radicals impinging the substrate with non-zero thermal velocities may not stick to the surface before they could react. The sticking coefficient can be defined by specifying '*STICK*' parameter in the RATE.DEPO statement. The number of incoming particles can be defined by the N.PARTICLE parameter in the DEPOSIT statement. The model calculates surface diffusion through a normalized gaussian distribution '*nd'* analytically as:

$$nd = \exp\left[-\frac{x^2}{Sigma.Dep^2}\right] \tag{4.1}$$

Conformal CVD Model

Conformal deposition model can be invoked by specifying a material to deposit, defining thickness, and a number of vertical grid spacings on the DEPOSIT statement in Elite. The conformal deposition model produces unity step coverage.

4.1.3. Etch models in Elite

Etching in the Elite simulation regime is based on "*string algorithm*". The etching models in ATHENA that were investigated in this work are as follows:

RIE Model

It is a simplistic time and direction-rate based etching model based on two adjustable components isotropic etching and anisotropic etching. Each of these components is characterized by empirical etch rates (r_{iso} and r_{dir}). User defined inputs of these components defines the resulting etch profiles. The ratio defines the degree of anisotropy:

$$A = \frac{r_{Dir}}{r_{Iso} + r_{dir}} \tag{4.2}$$

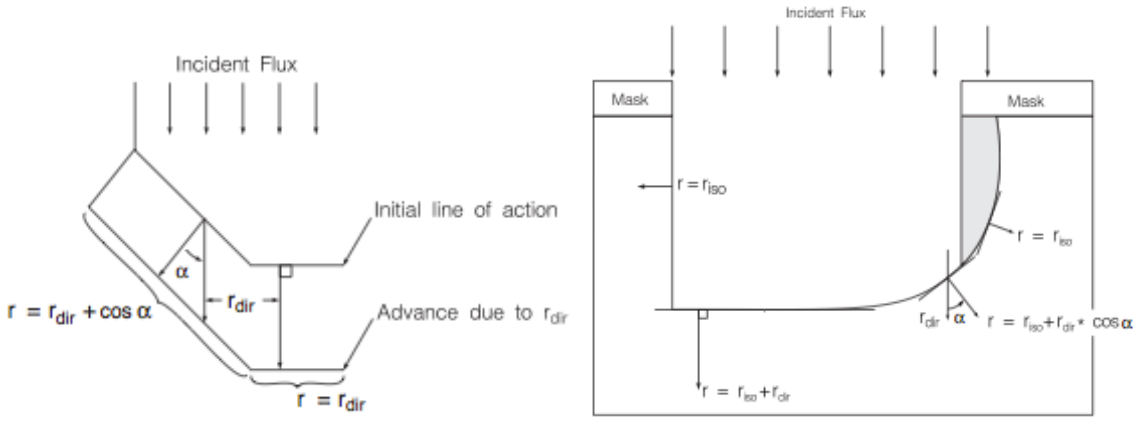

Fig. 4.3. (left) Etch-front motion due to directional influence, (right) areas of significance of r_{Iso} and r_{Dir} where shadowing effect is accounted for by the r_{Iso} component in the shadowed area. Figure Adapted from [1].

Plasma Etch Model

The simulation physics involves the tracking of ion trajectories from the neutral plasma or bulk, through the dark sheath surrounding the electrodes/walls by Monte Carlo

method. The user-specified sheath thickness and the calculated mean free path length determines the collision frequency encountered by a particular ion. The final etch rate is estimated from the simulated Monte Carlo distributions that calculate an incident ion flux on the substrate surface and surface evolution is then displayed by string algorithm. This model does not account for inter-ionic interactions to reduce the computational time. The ion trajectories are calculated independently and only a linear surface kinetic model for etching is incorporated. Parameters enabling this model are given in appendix IV.

Monte Carlo Etching Model

This is the most advanced physics-based etching model in Elite and involves more complex plasma distribution simulations. The model includes plasma species interactions with the substrate, the inter-ionic interactions and the re-deposition of polymer materials in order to precisely model the reactive ion etching. This module has been successfully implemented in simulation of a narrow-deep trench etch in oxide by Takagi *et al.* [6]. Figure 4.4 shows the comparison between plasma etching model and the Monte-Carlo based atomistic etching model.

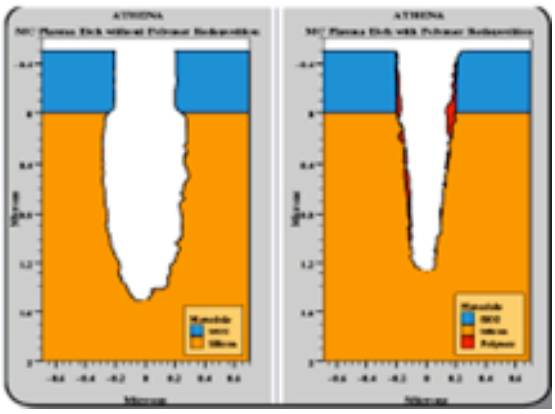

Fig. 4.4. Comprison of etch profiles for Monte Carlo and plasma etching models using oxide as etch hard mask [1].

It can be observed that later one is more realistic model and enables controlled anisotropic etching, assisted by polymer deposition on the sidewalls. Details of all the required process modeling set-up parameters are given in appendix IV.

4.1.4. Simulation Physics

The ion and neutral motions can be effectively simulated using a built-in '*plasma sheath model'* in Elite. The movement of ions in sheath region is tracked continuously which helps in determining the etch rate and the resulting profiles. The sheath thickness can be assumed to five times the *Debye length* [6]. Assuming the ions and neutrals fluxes departing sheath region to be represented by bimaxwell velocity distribution function along the direction determined by user specified incident angle:

$$f(v_{\parallel}, v_{\perp}) \sim I.\exp\left[\frac{v_{\parallel}}{T_{\parallel}} - \frac{v_{\perp}}{T_{\perp}}\right] \tag{4.3}$$

where $v_{//}$ and $v_{\perp}$ are the ionic velocity component parallel and perpendicular to incident direction respectively. '*I' is* the current density of ions (or neutral), $T_{\parallel}$ and $T_{\perp}$ being the dimensionless parallel and the lateral temperature components respectively. These parallel and lateral components are coupled with gas pressure and the RF power as shown in figure 6 in reference [6].

4.1.5. Etch Rate Calculations

The experimental etch rate in ion-assisted etching is governed by 'Langmuir adsorption kinetics' and given by equation [6]:

$$ER = \frac{Y_S \Gamma_i \Theta}{\rho_S} \tag{4.4}$$

where Γ_i is the ion flux, Θ is the surface coverage of the reaction species ($0 \le \Theta \le 1$), Y_S represents the etching yield on the saturation surface ($\Theta = 1$), and the ρ_S is the atomic density of the etched materials. Ion flux Γ_I is given as,

$$\Gamma_i = n_p v_{av} \tag{4.5}$$

where n_p is the ion density and v_{av} is the average incident velocity of ions bombarding the wafer due to the acceleration provided by the dc bias across the sheath region (V_{dc}). In plasma n_p is assumed to be approximately equal to the electron density n_e. Hence, v_{av} is assumed to be proportional to the square root of V_{dc}. Therefore, Γ_i is defined by equation;

$$\Gamma_I = n_p v_{av} \propto n_e V_{dc}^{1/2} \tag{4.6}$$

Consequently, the etch rate reported in reference [6] is proportional to electron density n_e and the wafer bias V_{dc} and is defined as;

$$ER = \Gamma_i Y_S \Theta/\rho_S \propto n_e V_{dc} \tag{4.7}$$

4.2. Simulation Results

Figure 4.5 show the compiled simulation results for different density of initial lithographic holes. From the voids thus formed, it can be interpreted that density of lithographically defined holes does not affect the void formation as long as the LPCVD polysilicon is conformal. This is crucial for developing a high-density pattern transfer process that is scalable to future technology generations. For 'Δ'=110 nm and'θ'=80-89^0,

the diameter of void '*D*' obtained from simulations was ~170 nm which closely match with the predicted mathematical results as given in Table 3.1.

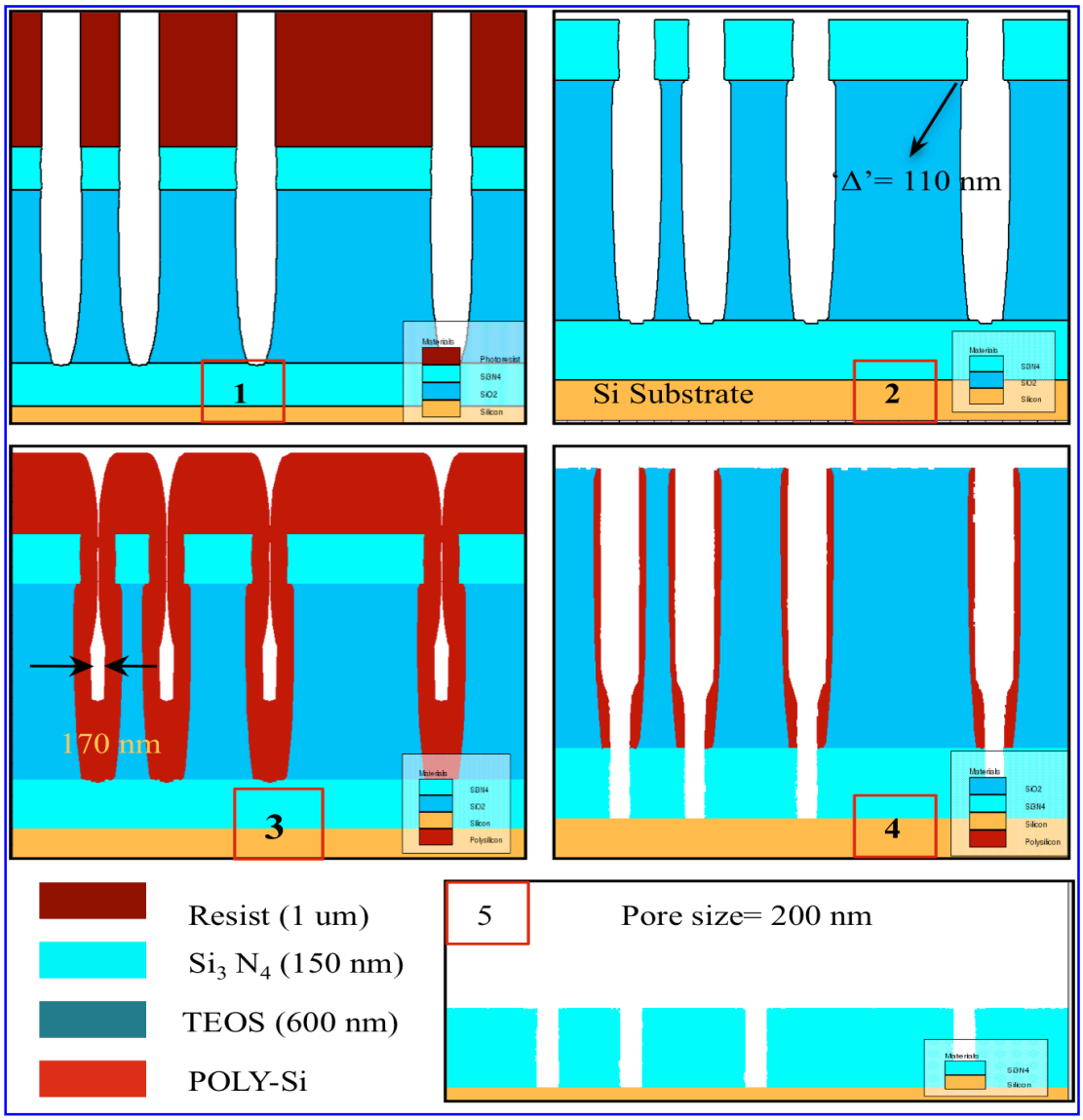

Fig. 4.5. Compiled simulation results for the void patterning technique. Overhang *Δ*~110 nm, the void size '*D*'~176 nm and sub-lithographic pore has diameter of 200 nm.

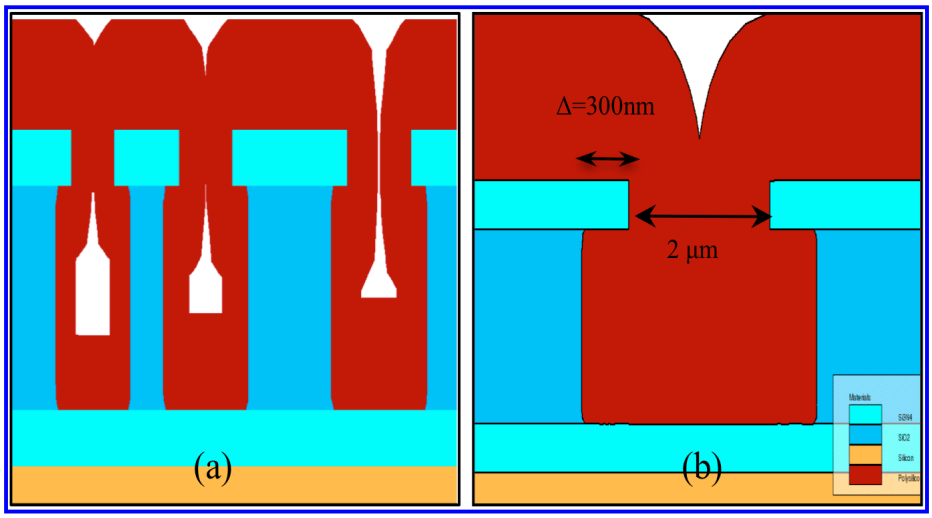

Fig. 4.6. Effect of CD variations: voids are raised/lifted-up with the increase in lithographically defined hole size from 500 nm→700 nm.

The effect of variation in lithographically defined hole size '*R*' (from 500 nm → 700 nm) is shown in Fig. 4.6 (a). The values of 'T_{SiO2}' and 'Δ'were fixed at 600 nm and 100 nm respectively which did not affect the void diameter if the critical conditions mentioned in section 3.2 were still valid.

However, it can be observed that if the hole diameter is increased but the 'T_{SiO2}' kept same *i.e.* if the aspect ratios of trench is decreased, the voids are raised in height from the bottom SiN layer or in other words the void length '*L*' is decreased. The raised voids are more prone to CD widening because of an inherent isotropic component during etch-back. Higher the isotropic etch component more is the CD widening. Therefore higher aspect ratios are desirable to yield more controlled pattern transfer with lower CD variations. Fig. 4.6 (b) illustrate results when the critical condition of $T_{SiO2} > H_{Min}$ is intentionally violated resulting in premature filling of trench without any voids. Fig. 4.7 shows the effect of variation in 'θ' on void formation. A deviation in sidewall angle from

90^0 results in sloping of voids that yields pores with sloped sidewalls. However, under controlled conditions this effect can be utilized to get even smaller features if pore slope is not that critical for a particular application.

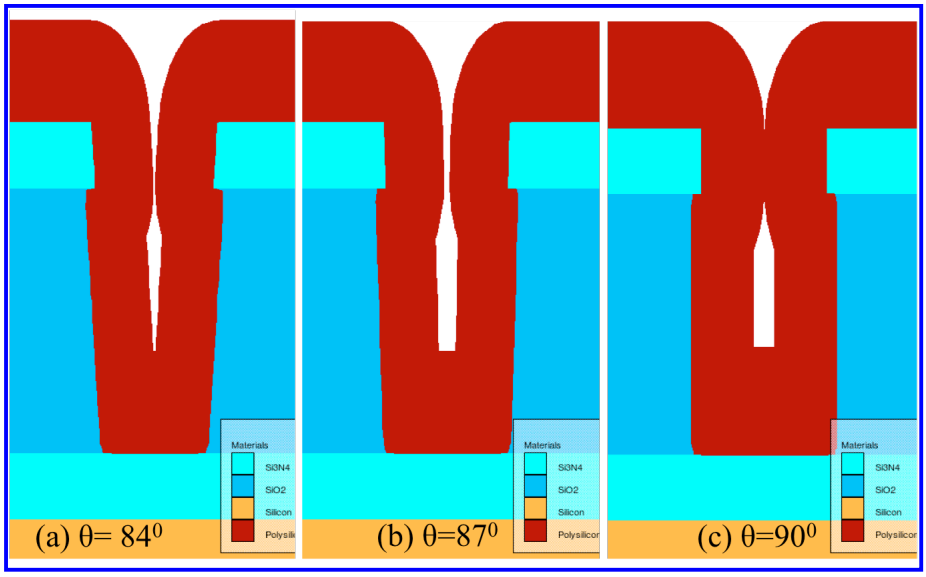

Fig. 4.7. Effect of sidewall angle 'θ' on keyhole diameter 'D'. Decrease in 'θ' manifests decrease in 'D'.

4.3. Experimental Procedure

The individual processes that were developed in chapter 3 were integrated and the entire void transfer process was implemented. Starting with 6" diameter <100> silicon substrates, a low stress thin film stack of SiN-SiO_2-SiN with respective thicknesses of 150 nm, 500-600nm and 150 nm was deposited using plasma enhanced CVD in Applied Materials P-5000 system. Wafers were coated with FujiFilm OiR 620M positive photoresist using SSI coat/develop track, exposed in a Canon i-line stepper and developed manually using manual CEE developer. The photoresist also served as an etch mask.

It was observed in chapter 3 that both the post-exposure and the post-development bakes caused resist reflow that led to mask faceting. As the unbaked resist withstood the subsequent stack etching, it was therefore not baked in this work. The top SiN was etched using $SF_6 + CHF_3$ chemistry in a Drytek Quad 482 RIE tool followed by SiO_2 etch using $CF_4 + CHF_3 + O_2$ in Applied Materials P-5000 MERIE etch tool for a directional etch stopping at bottom SIN layer. Low temperature (610 ^{0}C) polysilicon was deposited in ASM LPCVD tool that was conformal causing pinching off at top to form voids. Void etch-back was done in Drytek Quad RIE tool with $SF_6 + CHF_3$ chemistry for directional etching and lower CD widening.

A two-staged, CMOS compatible selective wet etch process using tetra-methyl ammonium hydroxide solution (TMAH) and buffered hydrofluoric acid was developed to remove polysilicon stingers and the remaining PECVD SiO_2. The process was characterized by examining the profiles using cross-sectional scanning electron microscopy (SEM).

4.4. Experimental Verification

With the trench aspect ratio of ~1, similar voids were observed in trenches of different densities. Figure 4.8 shows an interesting SEM micrograph of a die region following the polysilicon etch. A stray contaminant particle is observed to have masked the etch leaving the original void intact that can be seen behind the etched void. Fig. 4.9 (a) shows the cross-sectional SEM images of the voids with diameter of 74 nm when '*R*' is 750 nm.

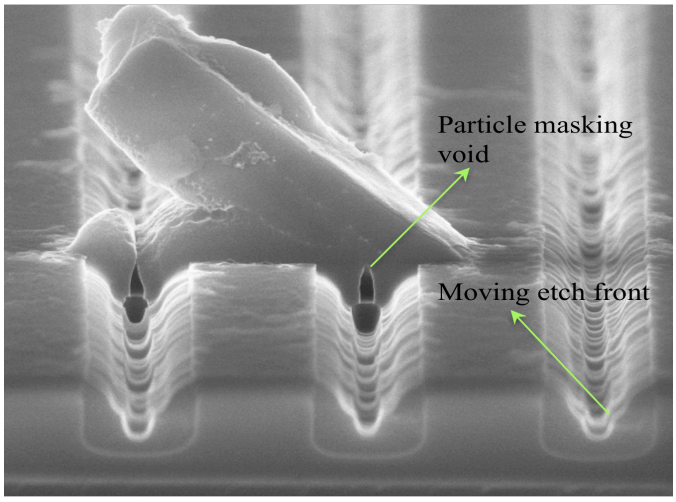

Fig. 4.8. SEM micrograph showing a contaminant particle masking a portion of a die during void transfer etching.

Fig 4.9 (b-f) show profiles views at different stages of etch-back process. Fig. 4.9 (g) shows the final sub-lithographic aperture in SIN with diameter of 130 nm which represents ~5.4X reduction from the lithographic trench size '*R*'. The final sub-lithographic pore diameter is increased in size from void size of 74 nm owing to a smaller '*L'* and raised voids. This is in agreement with simulation results as the similar effect of voids being raised was also observed with the decrease in H_{Min}/ R ratio in figure 4.6.

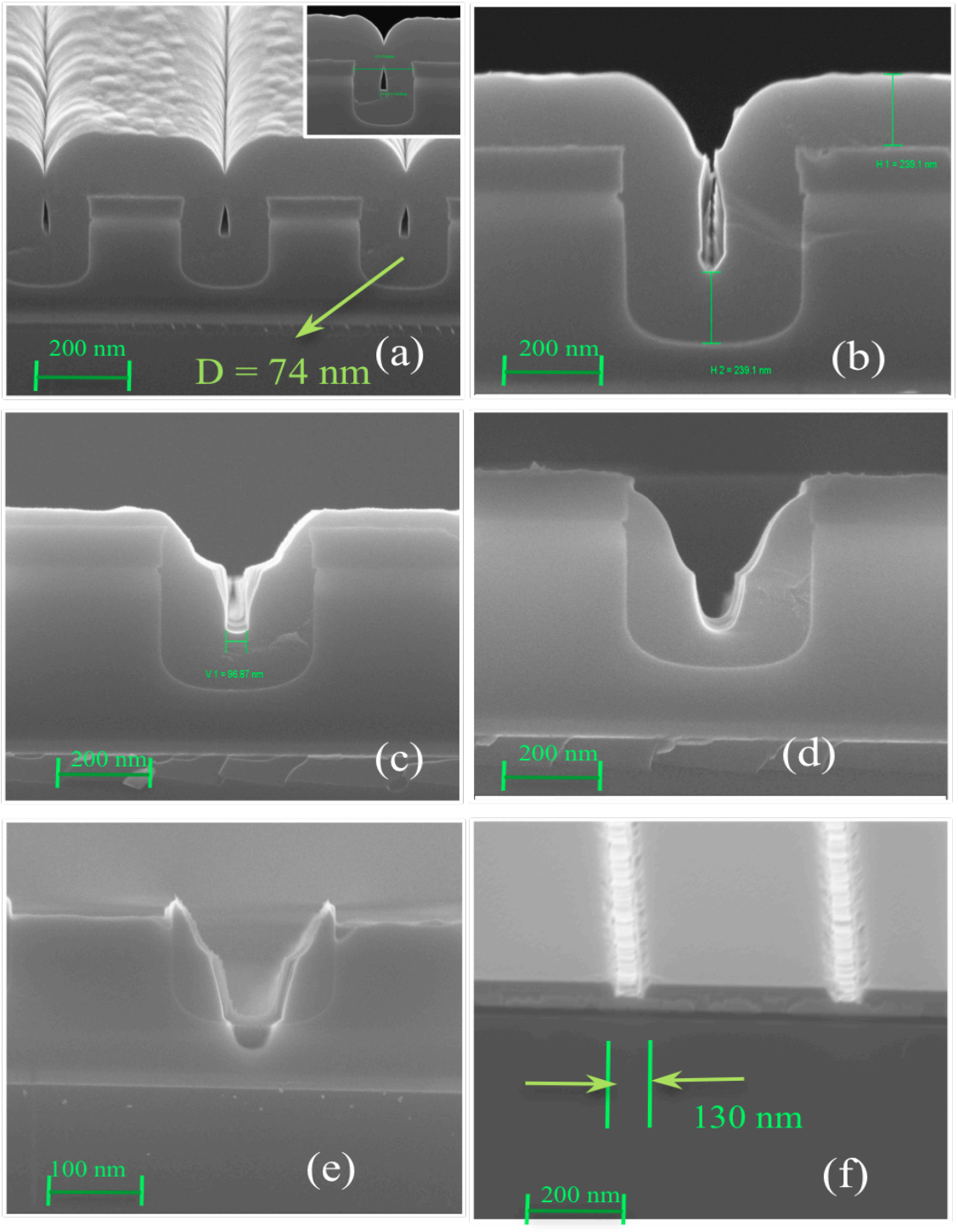

Fig. 4.9. X-SEM image of (a) void formed, (b-f) polysilicon etch-back and (g) final Sub-lithographic aperture.

Even though the diameter of transferred sub-lithographic aperture was higher than the void diameter, a higher aspect ratio trenches together with an accurately controlled etch-back process would promise lower CD widening to successfully pattern sub-100 nm features.

4.5. Simulation Model Calibration

The model parameters were explored to achieve a reasonable experimental correlation. The main parameters that control the etch profile are pressure, '*Vpdc'* (DC bias in plasma sheath), '*Lshdc'* (mean sheath thickness), '*Freq'* (frequency of current), '*Mgas/Mion'* (the atomic mass of gas atoms and plasma ions), 'K_i' (plasma etch rate linear coefficient related to the ion flux) and 'K_f' (plasma etch rate linear coefficient related to the chemical flux). In order to simulate the effect of these parameters a calibration process was conducted in two stages as follows.

4.5.1. Stack Trench Etch and CVD model calibration

Fig. 4.9 displays the effect of parameters listed above on the etched trench profile and the void formation. It can be inferred from figure 4.10 (b) and figure 4.10 (j) that neither the default model parameters nor the experimental parameters were sufficient to get a good agreement with the experimental results. Therefore extensive simulations were carried out. Row(1) in Fig. 4.10 shows that varying 'K_i' and 'K_f' determine the sidewall angle of etched trenches. Parametric values were assigned to emulate the inherent ionic and isotropic etch components and the best settings are displayed in the last column of each row. Once these values were assigned, the effect of pressure was simulated and shown in row (2) of Fig. 4.10.

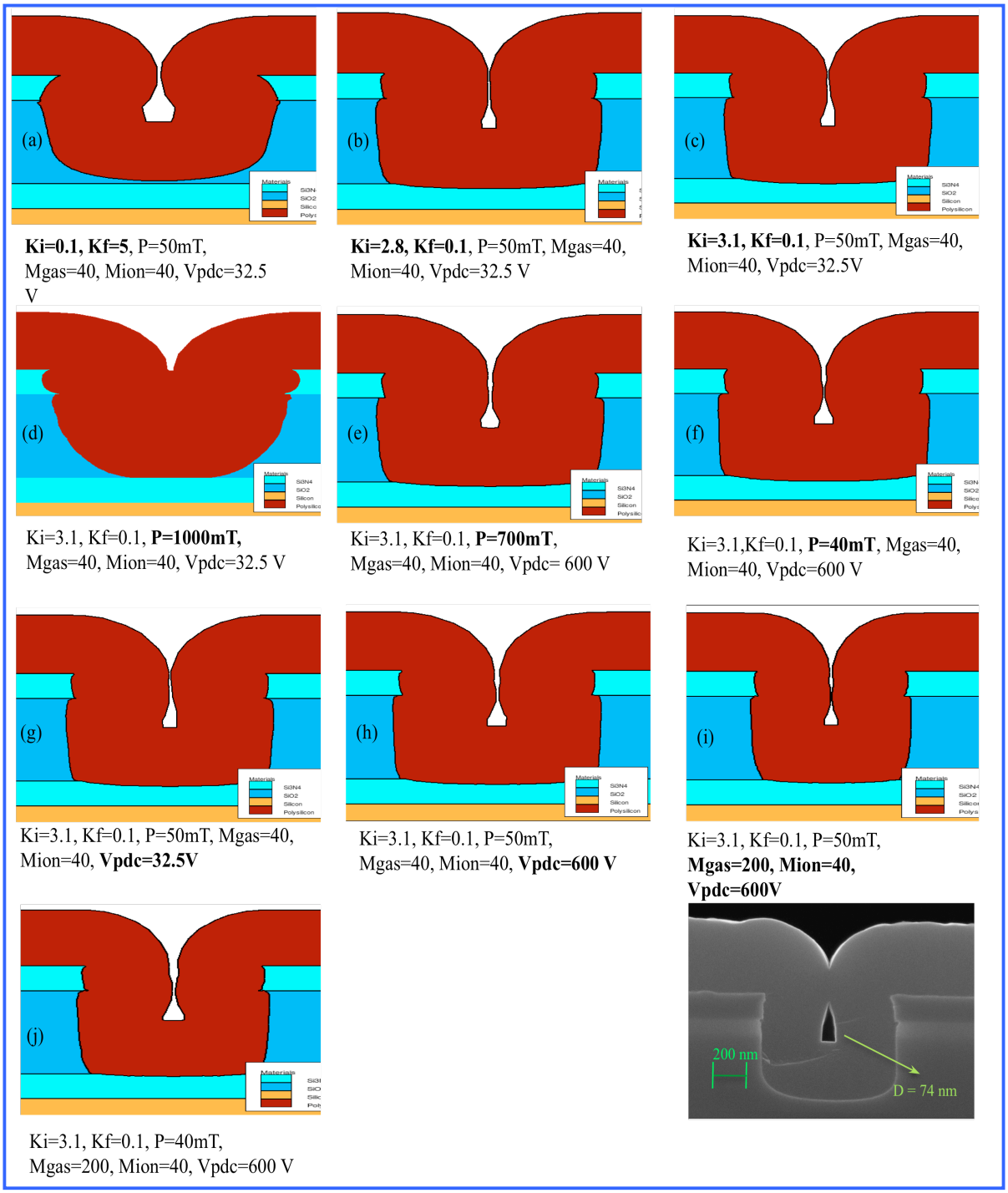

Fig. 4.10. Simulation model calibration showing effects of variation in parameters on trench profile and void formation. Row (1) shows the effect of Ki and Kf, row (2) shows the effect of pressure, row (3) shows the effect of Vpdc and row (4) shows the profile obtained using experimental values and the experimental X-SEM image.

Further fine-tuning the plasma sheath dc bias '*Vpdc*', a successful correlation was achieved as observed from row (3). The polysilicon CVD process can be modeled by using conformal CVD model in 'Elite' by varying the step coverage factor in simulations. After calibrating different model parameters, excellent correlation with the experimental profiles was obtained as illustrated in figure 4.10 (i) and figure 4.10 (k). Table 4.1 lists the model parameters and compares them with the experimental parameters.

Parameters → Etch Type ↓		Pressure (mTorr)		Vpdc (Volts)		Mgas (a.m.u)	Mion (a.m.u)	K.i	K.f
		Exp.	Sim	Exp.	Sim				
Stack Etch	SiN	40	50	~600	600	200	40	0.3	0
	PECVD SiO_2	55	50	~600	600	200	40	3.1	0.1
Polysilicon etch back		40	200	~600	32.5	80	20	1.1^{P} 1.0^{S} 1.0^{O}	0.1 0 0

LShdc=0.005 mm, Freq.=13.56MHz, Tion, Tgas=300 ^{0}K, ^{P} polysilicon, ^{S} SiN and $^{o}SiO_2$
N=10000, Exp = Experimental and Sim = Simulated values

Table 4.1. Model parameters used for simulation model calibration.

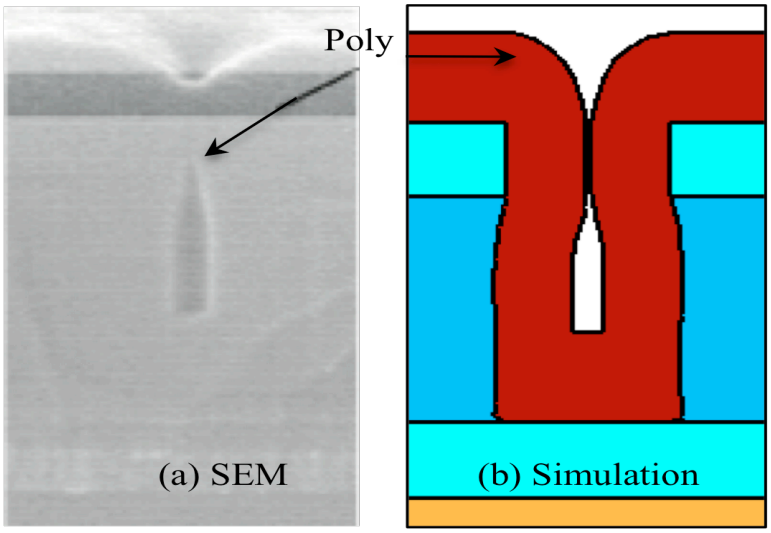

Fig. 4.11. Simulation model applied to reproduce the work done in [7]. SEM picture (a) adapted from reference [7].

The model was applied to a trench size of 250 nm as used in reference [8] and the results are in fairly good agreement with the reported experimental values of keyhole size of 43 nm as illustrated in Fig. 4.11.

4.5.2. Void Etch-back Calibration

The void etch back process was calibrated on similar lines to find the right parameter values also listed in Table 4.1. The experimentally observed profiles could be replicated as shown in figure 4.12 by adjusting model parameters given in table 4.1. It was observed that the pressure adjustment (in 50-200 mTorr range) in the model had a relatively minor effect on etch profiles.

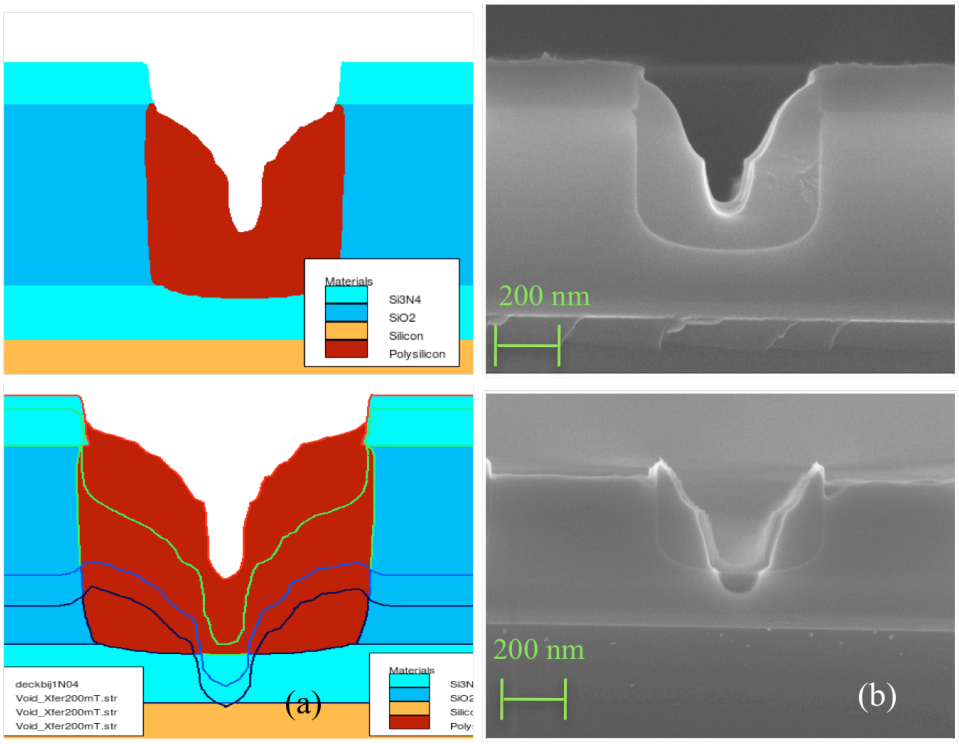

Fig. 4.12. Model calibration results and the illustration of moving etch interface in comparison with experimental X-SEM images of the void transfer in progress.

However, the best match was observed using 200mTorr in the model while the experimental value was 40 mTorr as given in Table 4.1. This is not surprising as the model may not exactly emulate tool/process specific conditions. Nevertheless it successfully models the process and offers a powerful simulator for the void transfer technique.

4.6. Proposed Unified Simulation Model

It has been corroborated in previous sections that the model parameters in the simulator can be adjusted and coupled to our design parameters to get process insights for void transfer process in advance. The model calibration resulted in a very reasonable experimental correlation. The main parameters that control the etch profile are pressure, *Vpdc*, *Lshdc*, *Frequency, Mgas/Mion,* K_i, K_f. T_{gas}, T_{ion} , Time '*T*' and mean free path length 'λ'. The Design parameters are T_{SiO2} , *R*, and θ which can be used to calculate Δ and δ. These geometrical parameters can then determine the experimental data inputs that can be fed and coupled to the simulation parameters in the plasma simulator. The simulator calculates inter-ionic collisions and incident ion flux on the substrate surface using Monte Carlo ion transport simulation. This calculated flux is then used to calculate the etch rate & determine surface evolution after each time increment.

The flowchart in Fig. 4.13 summarize a methodology that could enable an efficient unified simulation model coupling the geometrical and experimental process parameters to the simulation parameters.

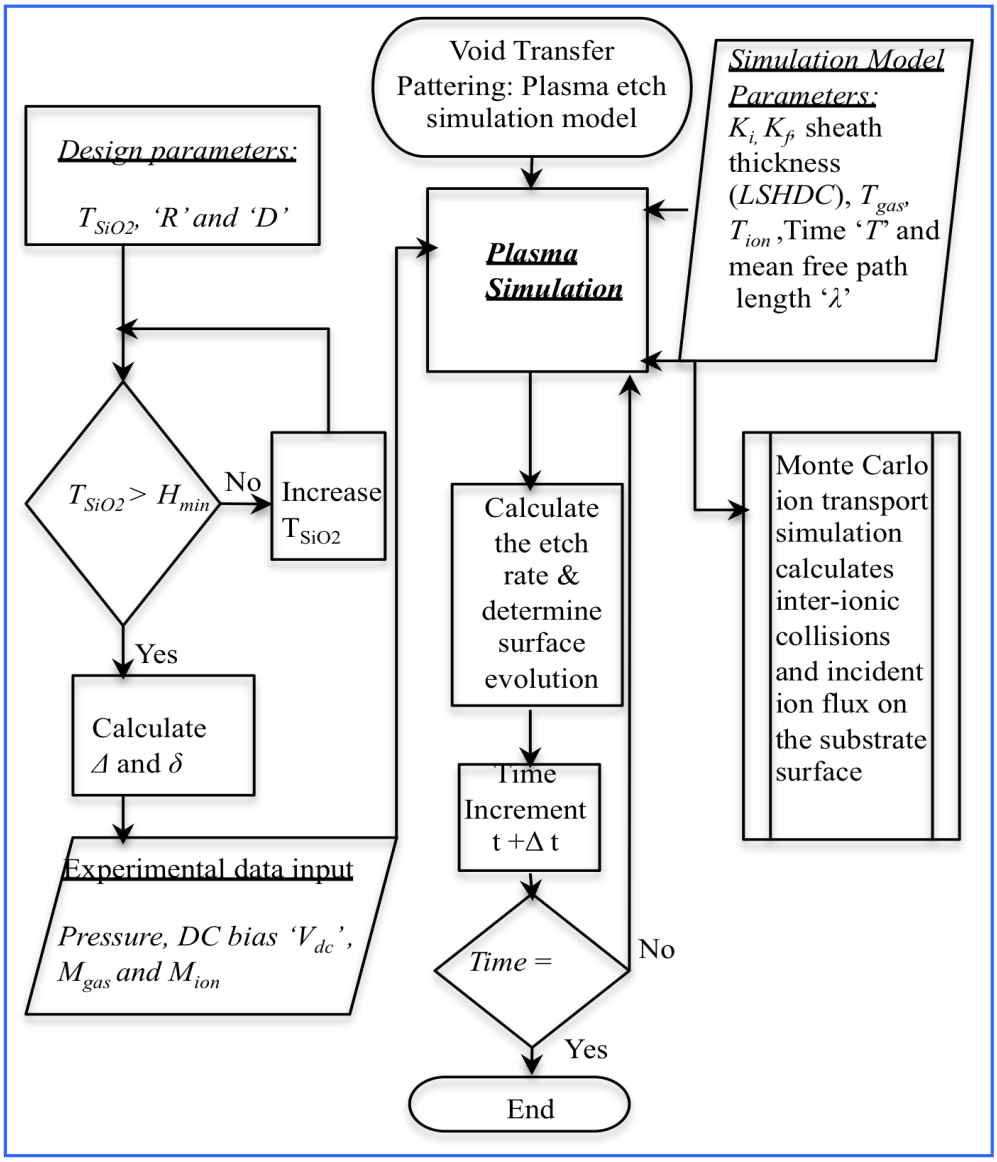

Fig. 4.13. The proposed unified simulation model flowchart for void transfer patterning technique.

References: Chapter 4

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CHAPTER 5

Conclusions and Future Work

In this study a robust yet simple void-assisted pattern transfer technique has been successfully modeled, simulated and validated. The process consists of intentionally creating keyhole void structures in conformal polysilicon film followed by an effective etch-back process to transfer the void creating pores in an underlying layer. The dimensions of pore formed are independent of the original lithographically defined feature size, thereby de-coupling the pore size from lithography associated CD variations.

The void patterning technique can be potentially scaled to any technology node. The critical process parameters influencing the void formation and pattern transfer have been identified and corroborated using simulations and experiments. This method provides a technique for creating nanometer scaled features for laboratories that are not equipped with the state of the art lithography tools yet are engaged in emerging device research requiring smaller dimensions. It offers an efficient low thermal budget and backend process compatible integration scheme.

Simulation of void patterning technique for prediction of final feature size obtainable is investigated. To the best of author's knowledge no such simulation study of void-assisted patterning process has been reported so far in the literature. Furthermore, the modeling of ion-assisted etch process has not been reported till date at RIT. Thus, this project initiated and accomplished scores of "firsts" towards the development of a reliable nano-patterning technique and a robust process infrastructure for future projects at RIT. The results illustrates that the 2-D Monte Carlo ion transport

effectively simulates the plasma etching processes using standard dry etch chemistries used in this study. The void diameter obtained in this work is 74 nm *i.e.* an impressive ~10X reduction from lithographically defined hole of 714 nm using i-line (λ=365 nm) lithography. Finally, the results of this investigation show that the geometrical design parameters can be coupled with the plasma process simulations to develop an efficient unified simulation module for the void transfer process.

Various issues related to design and process integration are identified and addressed as summarized in Table 5.1.

Process Issues	Solution
Mask faceting and erosion	I. Post exposure bake of 1 minute at 110 ^{0}C followed by a low temperature resist hard bake at 130 ^{0}C for 2 minutes if using Drytek Quad for etching the SiN-PECVD SiO_2 stack.
	II. 1-minute post exposure bake at 110 ^{0}C and no hard bake.
Highly anisotropic/ selective etch process	Two stage etch: SiN etch using CHF_3 + SF_6 etch chemistries in Drytek Quad 483 tool and PECVD SiO_2 etched using CF_4 + O_2 + CHF_3 in P-5000 MERIE tool.
Polysilicon grain size is large	Recommended a lower temperature poly deposition for reducing the grain size.
Poly stinger and PECVD SiO_2 removal	TMAH (CD 26 developer) heated to temperatures about 80 ^{0}C to remove polysilicon selectively and then 5.2:1 BHF.

Table 5.1. Summary of design and process integration related issues and proposed solutions.

5.1. Potential Applications for Void-assisted Pattern Transfer Process

Patterning nanometer scaled features using conventional lithography with a low thermal budget back end compatible process may find many applications in

nanotechnology. Some such applications are already underway and are summarized below.

Phase Change Memory

Breitwisch *et al.* [1] demonstrated a fully integrated 256 Kbit pore-phase change memory test array on 180 nm CMOS technology employing void-assisted patterning process with 20-80 nm pore sizes. The pore size is defined by purposely creating voids with conformal deposition. Very accurate CDs with diameter less than 20% the size of the original lithographically defined hole were reported. Fig. 5.1 shows each pore memory cell made of the phase change element in series with an nMOSFET and a functional 256-kbit test array. Fig. 5.2 shows comparison between the keyhole patterning technique and the simulated version of spacer patterning process. The reduced spread in RESET current associated with CD variations in keyhole process as observed in graph when compared with a spacer process shows the elimination of the RESET current dependence on the initial lithographic size. Thus, the ability to pattern sub-lithographic features in keyhole process is more immune to the lithography associated CD variations as compared to spacer process.

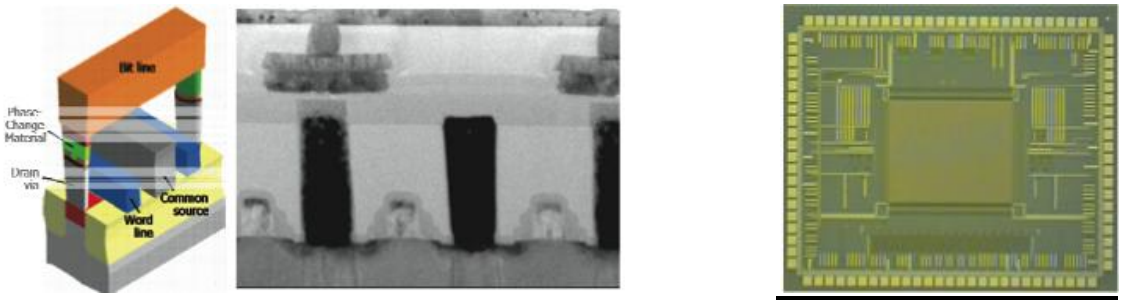


Fig. 5.1. Schematic of two neighboring unit cells and TEM image of pore memory cells above FET access transistors (left) and 256kbit functional test array (right) [1].

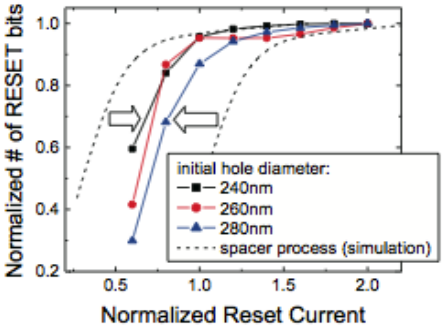
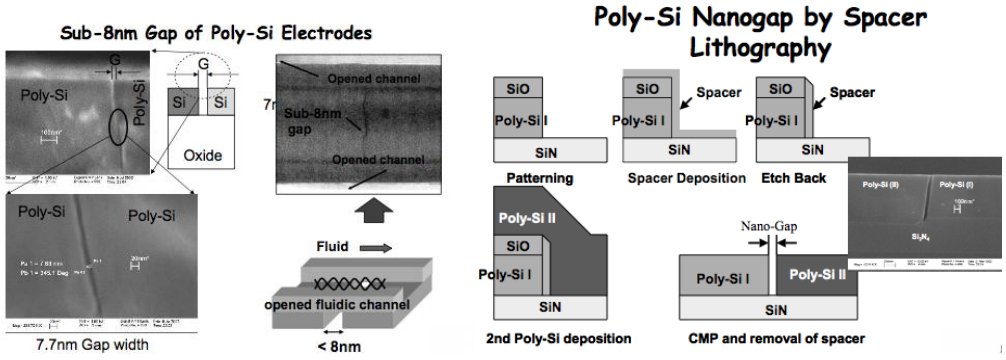


Fig. 5.2. The keyhole process greatly reduces the spread expected from a conventional spacer process under the same CD variations [1].

Nanogap capacitors for Detecting DNA Hybridization

The ability to create nanoscale gaps on silicon based technology opens a new era of collaboration for the realization of next generation bio- and nano-electronic devices like chemical- and bio-sensors. DNA and protein chips based on nanogap capacitors produced by spacer process have been reported for DNA hybridization [2-4]. The dissimilarities in dielectric properties of a single-stranded and double stranded DNA enables the use of capacitance measurements for in-situ monitoring of DNA hybridization without labeling. The patterning prospects of the void transfer process to produce low CD variation nanogaps can also be exploited in applications shown in Fig. 5.3 that were originally realized by employing spacer process.



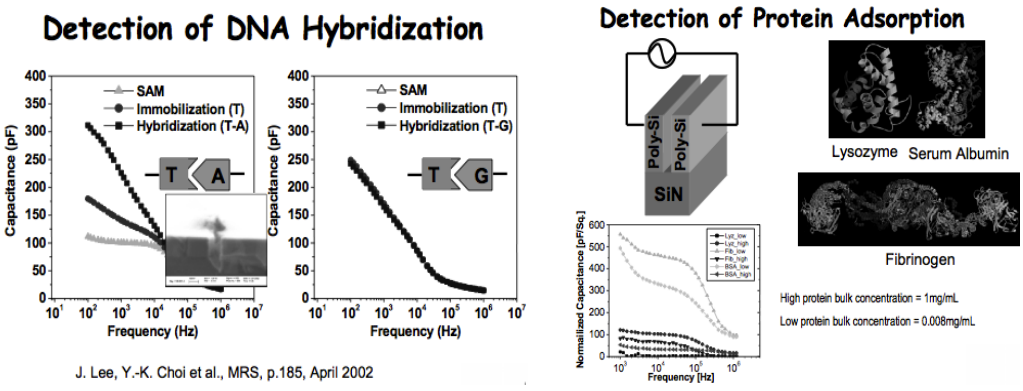


Fig. 5.3. Various applications of nanogaps formed using spacer process. Figures adopted from [4].

MEMS fluid sensors

Figure 5.4 show the SEM images of voids formed during void transfer process that can potentially serve as fluidic channels for MEMS based sensors. Highly controlled nm-scale fluidic channels for use with MEMS applications is achievable due to the accuracy of controllability of LPCVD polysilicion process.

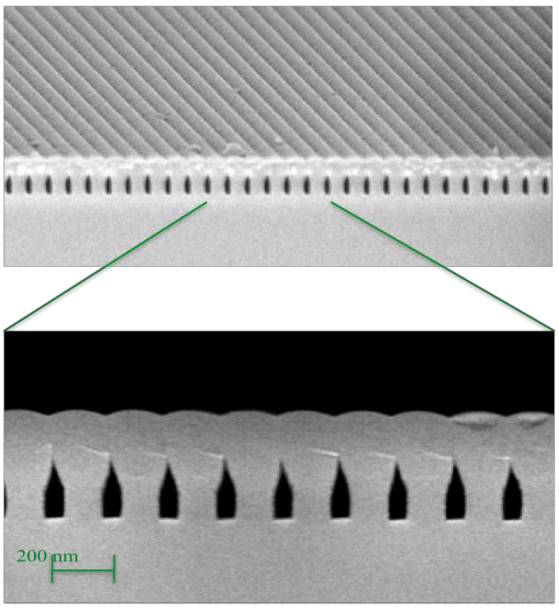


Figure 5.4. Voids formed in polysilicon can serve as fluidic channels for MEMS or NEMS based application.

5.2. Future Work

The process developed in this thesis can provide a basis for realizing new devices at RIT. In the near future, void transfer process will enable making phase change memory cells. The greatest challenge in designing large-scale phase change memory (PCM) arrays is high programming current densities (>10^7 A/cm^2 as compared to 10^5-10^6 A/cm^2 for transistors). Thus the active area needs to be scaled much smaller than the transistor area in the driving circuit. A reliable technique to form nanometer-sized structures with the extreme scaling potential is developed in this work. The future work will include integration of this process to fabricate a two terminal PCM cell being explored at RIT employing stacked bi-layer chalcogenide structure. The proposed schematic of a single celled PCM device is displayed in Fig. 5.5. Correspondingly, the mask designed with such PCM test structures is shown in Fig. 5.6.

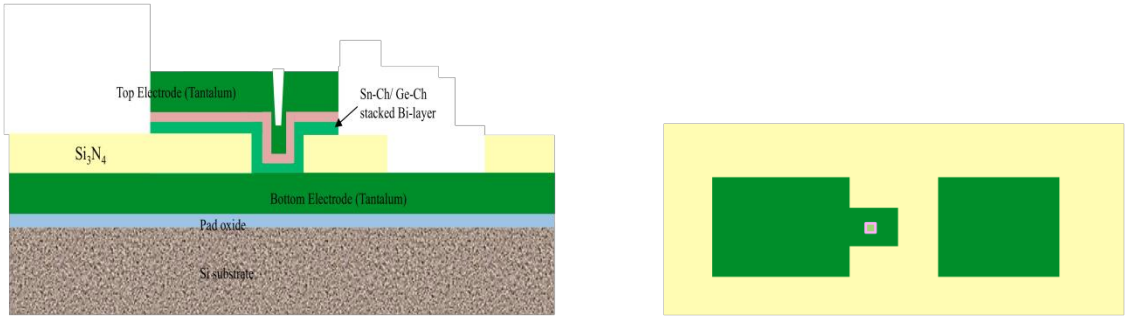


Fig. 5.5. Cross-sectional schematic of a proposed single celled PCM device (left) and top view (right).

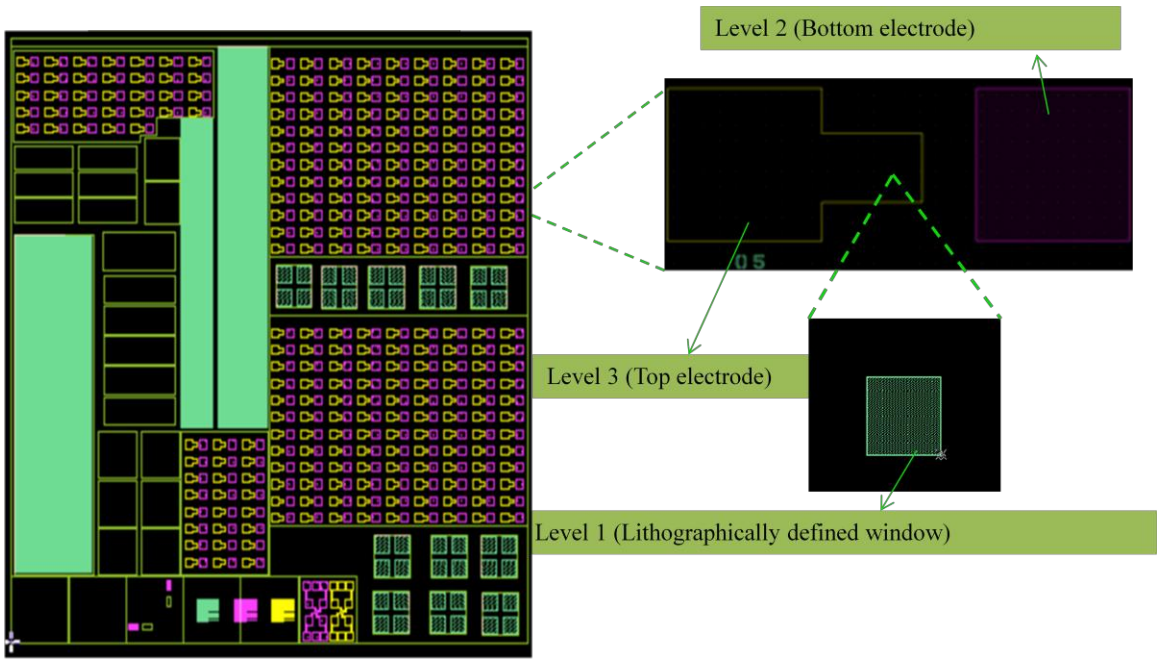


Figure 5.6. Mask designed with PCM test structures.

Subsequently, the process may also be applicable in MEMS fluidic and bioelectronic devices for future studies.

In summary, a robust process complete with physical design, process parameters and simulation codes has been created and made available as a research tool.

Chapter 5: References

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Appendix III

Process Details/ Recipes

Equipment: MOS/ RCA wet bench
Recipe: Standard RCA clean
Purpose: Cleaning wafer prior to all deposition and furnace runs
Comments: Remember to add H_2O_2 not more than 10 minutes before the run and allow temperatures to reach 75 ^{0}C.

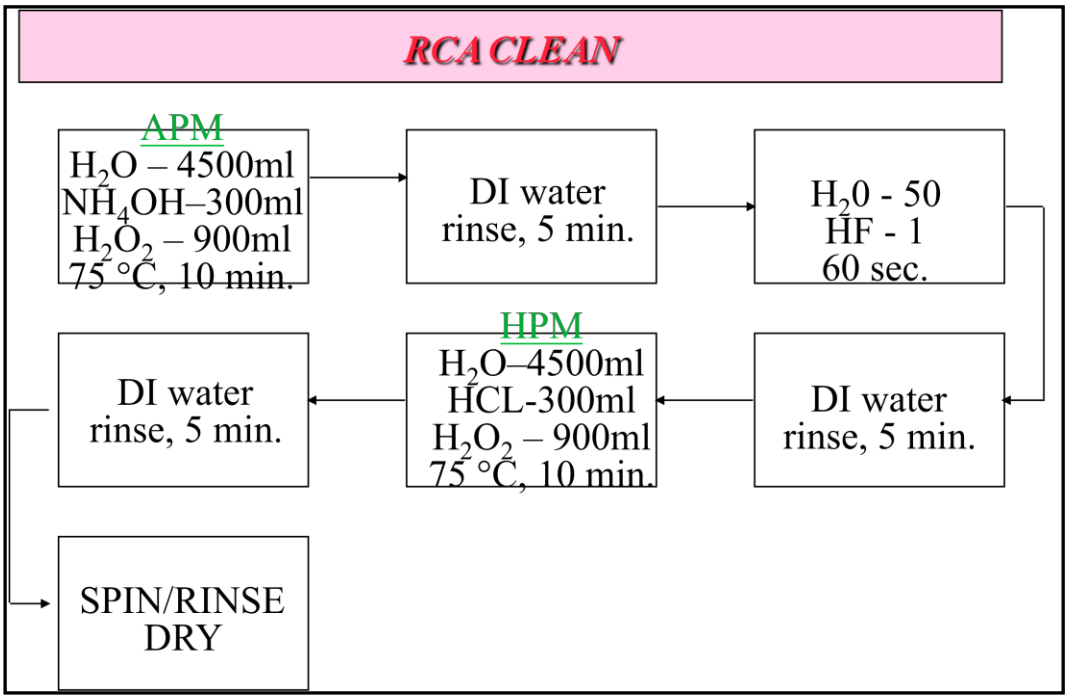

Fig. III.1. RCA clean procedure.
Reference: people.rit.edu/lffeee/PMOS.PPT

Equipment: Bruce BDF4 diffusion System (tube-4) Recipe: 'Lynn fuller 500 Dry Ox'- Recipe 250 Purpose: Pad Oxide growth				
Step #	Step Description	Time (hh:mm:sec)	Temperature (^{0} C)	Gas Flow (in lpm)
0	Boat Out	0:00:00	25	0
1	Push in	0:12:00	800	10 lpm N_2
2	Stabilize	0:15:00	800	10 lpm N_2
3	Rampup	0:20:00	1000	5 lpm O_2
4	Soak	0:48:00	1000	10 lpm O_2
5	N2 Purge	0:05:00	1000	15 lpm N_2
6	Ramp Down	0:40:00	25	10 lpm N_2
7	Pull Out	0:15:00	25	5 lpm N_2

Table III.1. Pad oxide growth recipe.

Equipment: Applied Materials P-5000 Recipe: B6-1500 A CON NIT (Chamber B) Purpose: PECVD Nitride Film deposition			
	1) Stabilize	2) Set Up	3) Deposit
Chamber Selection	B	B only	B only
Step End control	By time	Press. in Spec	Press. in Spec
Max. Step Time	30 Sec	15.0 sec	User input secs
End Point Selection	No End pt.	No End pt.	No End pt.
Pressure	Servo 5.0 Torr	Servo 4.5 Torr	Servo 4.5 Torr
Pressure Ramp rate	0 torr/sec	Same as step 1	0 torr/sec
RF power match mode	0 W, Auto, B-to-B	Same as step 1	600W, Auto, B-to-B
RF time set up	0.0V	Same as step 1	Same as step 1
RF2 Power, match	0W, Auto	Same as step 1	Same as step 1
DPA RF	Off	Same as step 1	Same as step 1
Susp. Temp.	400 ^{0}C (wafer ~348)	Same as step 1	Same as step 1
Temp. Ramp	0.0 ^{0}C/sec	Same as step 1	Same as step 1
Purge Flow	Off	Same as step 1	Same as step 1
Susceptor spacing	290 mils	Same as step 1	Same as step 1
Chamber bypass	OFF	Same as step 1	Same as step 1
Page 2			
Plasma monitor	OFF	Same as step 1	Same as step 1
CVD-I microwave	OFF	Same as step 1	Same as step 1
Page 3 (Gas flows) N_2: SiH_4 NH_3	2000 sccms 0 0	2000 sccms 130 sccms 60 sccms	2000 130 60

Table III.2. PECVD Nitride film deposition recipe.

Equipment: Applied Materials P-5000 Recipe: A6-6KA TEOS LS (Chamber A) Purpose: PECVD SiO_2 (TEOS) Thin Film deposition			
	1) Set up	2) Deposit	3) DESCUM
Chamber Selection	A	A only	A only
Step End control	By time	By time	By time
Max. Step Time	15 Sec	User input in sec	10 sec
End Point Selection	No End pt.	No End pt.	No End pt.
Pressure	Servo 9.0 Torr	Servo 9.0 Torr	Throttle open
Pressure Ramp rate	0 torr/sec	Same as step 1	0 torr/sec
RF power match mode	0 W, Auto, B-to-B	290 W, Auto, B-to-B	50W, Auto, B-to-B
RF time set up	0.0V	Same as step 1	Same as step 1
RF2 Power, match	0W, Auto	Same as step 1	Same as step 1
DPA RF	Off	Same as step 1	Same as step 1
Susp. Temp.	390 ^{0}C (wafer ~354)	390 ^{0}C (wafer ~366)	390 ^{0}C (wafer ~360)
Temp. Ramp	0.0 ^{0}C/sec	Same as step 1	Same as step 1
Purge Flow	Off	Same as step 1	Same as step 1
Susceptor spacing	220 mils	Same as step 1	990 mils
Chamber bypass	OFF	Same as step 1	Same as step 1
Page 2			
Plasma monitor	OFF	Same as step 1	Same as step 1
CVD-I microwave	OFF	Same as step 1	Same as step 1
Page 3 (Gas flows) O_2 TEOS	285 sccms 400 sccms	285 sccms 400 sccms	285

Table III.3. PECVD SiO_2 Film deposition recipe.

Equipment: SSI coat/develop track, track 1 Recipe: Coat.rcp Purpose: Oir 620 M i-line positive Photoresist coat process				
	Oven 1	Oven 2	Cool 1	Cool 2
Set	145.0 ^{0}C	93.0	25	25
Tolerance	5	5	20	20
Bake Time	60.0	60.0	10	10
Dispense	30			
Step 1	Mode (0 spin)	Accel 100	Time= 3.0	
Step 2	Mode (0 spin)	Speed 3250	Accel=15000	Time= 30 sec

Table III.4. Photoresist coat recipe.

Equipment: Manual CEE developer Recipe: Program 1- 6” Purpose: Post Exposure Develop process		
Step #	Dispense	1
Step 1: Stream	PG/0 VEL/0	300 RPM
	PG/0 RPM/0	10000 R/S
	PG/0 Step-0	Nozzle #1
	PG/0 Time/0	3 sec
Step 2: Puddle	PG/0 VEL/1	30 RPM
	PG/0 RPM/1	10000 R/S
	PG/0 Step-1	Nozzle #1
	PG/0 Time/1	2 sec
Step 3: 50 sec develop	PG/0 VEL/2	0 RPM
	PG/0 RPM/2	10000 R/S
	PG/0 Step-2	Nozzle #0
	PG/0 Time/2	50 sec
Step 4: Rinse	PG/0 VEL/3	200 RPM
	PG/0 RPM/3	10000 R/S
	PG/0 Step-3	Nozzle #2
	PG/0 Time/3	15 sec
Step 5: Dry	PG/0 VEL/4	2500 RPM
	PG/0 RPM/4	5000 R/S
	PG/0 Step-4	Nozzle #0
	PG/0 Time/4	30 sec
Step 6: End	PG/0 VEL/5	End RPM

Table III.5. Post Exposure Develop process recipe

Equipment: Applied Materials P-5000 Recipe: C6-OX ETCH XPRMT (Chamber C) Purpose: PECVD SiO_2 MERIE Etch			
	1) Stabilize	2) Etch	3) Pump
Chamber Selection	C	C only	C only
Step End control	Press. In Spec.	By time	By time
Max. Step Time	20 Sec	User input in sec	15 sec
End Point Selection	No End pt.	No End pt.	No End pt.
Pressure	Servo 250.0 mTorr	Servo 250 mT	Throttle open
Pressure Ramp rate	0 torr/sec	Same as step 1	0 torr/sec
RF power match mode	0 W, Auto, B-to-B	500 W, Auto, B-to-B	0W, Auto, B-to-B
RF time set up	0.0 V	Same as step 1	Same as step 1
DC bias set limit	0W, Auto	Same as step 1	Same as step 1
Magnetic Field	Off	Same as step 1	Same as step 1
Magnetic Modulation	390 ^{0}C (wafer ~354)	390 ^{0}C (wafer ~366)	390 ^{0}C (wafer ~360)
Magnetic rotation freq.	0.0 ^{0}C/sec	Same as step 1	Same as step 1
Process position	Off	Same as step 1	Same as step 1
Page 2: Empty			
Page 3 (Gas flows) O_2 CHF_3–B CF_4-B	20 100 50	20 100 50	

Table III.6. PECVD SiO_2 MERIE Etch recipe.

Equipment: Branson Asher Recipe: 6” Hard Ash Purpose: To ash photoresist						
Step #	1	2	3	4	5	6
Step Active	Yes	Yes	Yes	No	No	No
Pump down	Slow	Slow	None	None	None	None
Purge	None	None	Fast	None	None	None
Step terminator	Time	Time	Time	EOP	EOP	EOP
Step time (sec)	140	20	30	30	30	30
RF forward	500	0	0	300	300	300
Lamp (W)	1800	0	0	2000	2000	2000
Lamp time	15	0	0	15	15	15
Platen Temp.	40	40	40	40	40	40
Platen mode	Up	Up	Up	Up	Up	Up
Press. (mTorr)	4500	50	8000	0	0	0
Gas flow 1 (sccm)	4000	0	0	0	0	0
Gas flow 2 (sccm)	0	0	1000	0	0	0
EOP time out (secs)	120	0	120	120	120	120

Table III.7. Resist Ash recipe.

Equipment: ASM LPCVD Recipe: 610 Poly Purpose: LPCVD polysilicon deposition		
Parameter	Setting	Tolerance
Base Pressure	50 mTorr	20 %
Deposition Temperature	610 ^{0}C	20%
SiH_4 flow	25 sccms	10%
Deposition Pressure	315 mTorr	5-10%

Table III.8. LPCVD polysilicon deposition recipe.

PECVD and LPCVD Nitride Etch- Drytek Quad RIE tool (Timed etch Mode)					
		Nitride Etch (Recipe: GuriNitr step1- chamber 2)			PECVD SiO_2 Etch (Recipe: GuriNitr step2)
		Setting		Tolerance	
Gas flows (sccms)	CHF_3	35		20 %	70
	SF_6	30		20 %	0
	Ar	0		20 %	75
	O_2	0		20 %	10
Power		205 W (input)		240 W (effective)	210 W
Pressure		40 mTorr		20 %	55-60 mTorr
		PECVD Nitride (Patterned)		LPCVD Nitride (Patterned)	
Measurement Area		Dense Lines (SEM)	Big Boxes (Nanospec)	Big Boxes (Nanospec)	Big Boxes (Nanospec)
Etch Rates (in nm/sec)		2.92	3.86	3.14	1.12
	i-line resist (no HB)	2.3			NA
Selectivity		Si_3N_4/ SiO_2 ~ 2.4			SiO_2 / Si_3N_4 ~ 0.6

Table III.9. PECVD SiN etch recipe.

Polysilicon Etch-back (Timed etch Mode) FacPoly Recipe: Chamber 2			
Paramter		Setting	Tolerance
Gas flow (Sccm)	CHF_3	30	20 %
	SF_6	30	20 %
Power		180 W (input)	230 W effective
Pressure		35 mTorr	20 %
DC Bias (display)		~ 420 W	

Table III.10. Polysilicon Etch-back recipe.

Appendix IV

Process Simulations

IV.1. List of Plasma etch parameters crucial in modeling the void transfer process

- *PRESSURE:* describes the plasma etcher reactor pressure. Units are mTorr. Default 50 mTorr.
- *TGAS:* describes the plasma etcher reactor gas temperatures. Units are ^{0}K. Default is 300 K.
- *TION:* describes the plasma etcher reactor ion temperatures. Units are ^{0}K. Default is 300 K.
- *VPDC:* describes the DC bias in the plasma sheath. Units are V. Default is 32.5 V.
- *VPAC*: describes the AC voltage in the sheath-bulk interface. Units are V. Default is 32.5 V.
- *FREQ:* describes frequency of the AC current. Units are Mhz. Default is 13.6 MHz.
- *LSHDC*: describes the mean sheath thickness. Units are mm. Default is 0.005 mm.
- LSHAC: describes the AC component of the sheath thickness. Units are mm. Default is 0.0.
- *K.I*: describes the plasma etch rate linear coefficient related to the ion flux.
- *K.F*: describes the plasma etch rate linear coefficient related to the chemical flux.
- *K.D*: describes the plasma etch rate linear coefficient related to the deposition flux.
- *MGAS:* describes the atomic mass of the gas atoms. Default is 40.
- *MION:* describes the atomic mass of the plasma ions. Default is 40.
- *QIO*: describes the momentum transfer cross-section. Units are m^2. Default is 1.7e-19
- *QCHT*: describes the charge exchange cross-section. Units are m^2. Default is 2.1e-19.

- *CHILD.LANG, COLLISION, LINEAR, and CONSTANT*: specify a model used in calculation of the voltage drop in the plasma sheath. Default is LINEAR.

- *IONS.ONLY*: states that neutrals to be ignored in plasma simulation. Default is false

- *NPARTICLES*: defines number of particles used for Monte Carlo calculation of the ion flux coming from plasma. Default is 10,000.

- *ENERGY.DIV*: specifies number of energy divisions used for calculation of the plasma ion flux. Default is 50.

IV.2. Parameters Specific to ELITE Depositions

- MACHINE: describes the name of the machine to be run for ELITE deposits. The machine name must be specified in a previous RATE.ETCH statement.

- N.PARTICLE: describes the number of particle trajectories to calculate for the Monte Carlo deposit model.

- OUTFILE: describes the name of the file to be written with Monte Carlo particle positions.

- SUBSTEPS: describes the number of time increments made for each division of the deposit in the ELITE module.

- VOID: describes that the voids formed during deposition are to remain unfilled with deposit material.

IV.3. Parameters used only with RIE, WET.ETCH, and PLASMA models

- DT.FACT: By default, the movement of a string node is limited to less than or equal to one quarter of the median segment length. This is a good compromise between simulation speed and the danger of loop formation. The optimization factor DT.FACT must not exceed 0.5. You may decrease it if necessary for more accuracy.

- DT.MAX is used to limit the time-steps size. By default, the upper limit for the maximum time-step is one tenth of the total etch time specified. This is a good compromise between calculation accuracy and calculation time. But sometimes, it is useful to adapt this value to the specific simulation problem. Allowing the time steps to become greater gives a higher simulation speed but the accuracy may suffer. For smaller time steps, the simulation speed will decrease but the accuracy may be greater.

- DX.MULT is the accuracy multiplier for ELITE etches. The discretization size used for the etch calculation will be multiplied by DX.MULT. For improved accuracy at the cost of extra simulation time, decrease the value of DX.MULT.

IV.4. Parameters used for RIE and WET.ETCH models

- A.H, A.M, A.S, U.H, U.M, U.S, and N.M describes that the etch rates are in Angstroms per hour, Angstroms per minute, Angstroms per second, microns per hour, microns per minute, microns per second, and nanometers per minute respectively.

- DIRECTIONAL describes the directional component of the etching rate used by the RIE model. The ionic etch rate is the contribution of the ions to the chemically oriented etching mechanisms. The ions are assumed to have an anisotropic angular distribution specified by divergence parameter.

- ISOTROPIC describes the isotropic etch rate used by the WET.ETCH and RIE models. The isotropic etch rate is the contribution of thermal atoms, radicals, and molecules coming out of the plasma. These are assumed to have an isotropic angular distribution. Therefore, the isotropic etching may lead to an underetching of the mask.

- CHEMICAL, DIVERGENCE: CHEMICAL is the etch rate in the RIE model normal to the ion beam when the DIVERGENCE is specified as non-zero. DIVERGENCE describes the beam divergence used by the RIE model. The angular distribution of the ions coming down to the wafer is Gaussian.

IV.5. Code used to model void transfer process.

```
go athena

#### MESH----------------------------------------------------------

line x loc=0.00 spac=0.10
line x loc=1.1 spac=0.005
line x loc=2.0 spac=0.005
line x loc=2.5 spac=0.1
line y loc=0.00 spac=0.008
line y loc=0.1 spac=0.008

init silicon orientation=100

#### Stack Formation-----------------------------------------------

deposit nitride thick=0.150
deposit oxide thick=0.5 divisions=10
deposit nitride thick=0.150
deposit photoresist  thick=0.5 divisions=8


#### Photoresist Patterning and Etch ------------------------------

etch photoresist start x=1.25 y=-1.9
etch cont x=1.25 y=-0.8
etch cont x=1.95 y=-0.8
etch done x=1.95 y=-1.9

#### Stack Etching ------------------------------------------------
#### Define the plasma etch parameters for Stack (SiN-SiO2)---------

set DIVERG = 1

Rate.Etch Machine=PEMach \
    Plasma \
    Pressure = 20 \
    Tgas = 300.0 \
    Tion = 3000.0 \
    Vpdc = 32.5 \
    Vpac = 32.5 \
    Lshdc = 0.005 \
    Lshac = 0.0 \
    Freq = 13.56 \
    Nparticles = 4000 \
    Mgas = 40.0 \
    Mion = 40.0 \
    Constant \
    Energy.Div = 50 \
    Qio = 1.7e-19 \
    Qcht = 2.1e-19
```

Define the plasma etch parameters for Stack (SiN-SiO_2)--------

```
Rate.Etch Machine=Stack \
    Plasma \
    Material=nitride \
    k.i = 0.3

Rate.Etch Machine=Stack \
    Plasma \
    Material=oxide \
    k.i = 3.1
    k.f=0.1
```

Define the plasma etch parameters for the photo-resist--------

```
Rate.Etch MAchine=Stack \
    Plasma \
    Material=SPR500 \
    k.i = 0.7
```

Etch the trench using the plasma etcher Stack----------

```
Etch Machine=Stack Time=1.4 minutes Dx.Mult=1
```

Save the trench structure and plot----------

```
Structure Outfile=Trench.str

tonyplot

#init infile=Trench.str
```

Remove Resist----------

```
etch photoresist all
```

Overhang formation----------

```
rate.etch machine=overhang oxide a.m  wet.etch isotropic=500.00
etch machine=overhang time=30.0 seconds dx.mult=1.0

tonyplot
```

Conformal Polysilicon deposition----------

```
deposit polysilicon thick=0.346 void
structure outf=plasma_cvd.str
tonyplot  plasma_cvd.str

init infile=plasma_cvd.str

#### Polysilicon etch-back--------------------------------------


Rate.Etch Machine=poly_etch \
    Plasma \
    Pressure = 200 \
    Tgas = 300.0 \
    Tion = 3000.0 \
    Vpdc = 32.5 \
    Vpac = 32.5 \
    Lshdc = 0.005 \
    Lshac = 0.0 \
    Freq = 13.56 \
    Nparticles = 4000 \
    Mgas = 80.0 \
    Mion = 20.0 \
    Constant \
    Energy.Div = 50 \
    Qio = 1.7e-19 \
    Qcht = 2.1e-19

#### Define the plasma etch parameters for polysilicon and nitride--

Rate.Etch Machine=poly_etch \
    Plasma \
    Material=poly  \
    k.i = 1.1

Rate.Etch MAchine=poly_etch \
    Plasma \
    Material=nitride \
    k.i = 0.2

#### Etch the trench using the plasma etcher poly_etch----------

Etch Machine=PEMach Time=0.8 minutes Dx.Mult=0.5


#### Etch the poly-stingers and oxide ------------------------------


etch poly all
etch oxide all
structure outf=porefinal.str
tonyplot

quit
```