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DESIGN OF RIT'S SUB-MICRON CMOS PROCESS

By

Suraj Bhaskaran

A Thesis Submitted

in

Partial Fulfillment

of the

Requirements for the Degree of
Master of Science in Microelectronic Engineering

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**DEPARTMENT OF MICROELECTRONIC ENGINEERING
COLLEGE OF ENGINEERING
ROCHESTER INSTITUTE OF TECHNOLOGY
ROCHESTER, NY
July 6, 2000**

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1. ABSTRACT

The design and simulation of RIT's sub-micron CMOS process is studied in this work. The work has demonstrated a process capable of producing working transistors with a channel length of 0.5 μ m.

New advancements such as dual well, low doped drain (LDD) regions and self-aligned silicides are a few mentioned highlights. The devices will be fabricated on 6" wafers using equipment recently donated to the RIT Microelectronic Engineering cleanroom facility. This calls for characterization of the new processes and equipment for optimized results.

Device simulation was performed using MicroTec 2D Process/Device simulator from Siborg Systems. Simulated threshold voltage for the NFET device was on target, whereas the PFET transistors will require further process improvement.

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2. INTRODUCTION

Sub-micron Complimentary Metal-Oxide Semiconductor (CMOS) transistors with channel lengths smaller than 0.2 microns are currently being fabricated by the IC manufacturers. One of the main ways of achieving increased speeds is by scaling of CMOS devices. This approach also increases the packing density, which leads to smaller die sizes.

Although the current RIT p-well CMOS process^[5] has produced satisfying results for the past 10 years, the channel lengths for the working devices well above sub-micron. Fabrication of sub-micron CMOS devices at RIT calls for an entirely redesigned process that can be used as an educational tool as well as keeping pace with the semiconductor industry. Decreasing the channel lengths, while keeping the drain/source regions relatively large was the approach that was chosen for the Testchip layout. The main objective of creating a new process was to enhance device fabrication capabilities and utilize the new equipment, as well as using it as an advanced teaching tool for the CMOS Factory at RIT.

The upgrade of the RIT cleanroom facility to 6-inch wafer processing capability is an additional driving force for a new sub-micron process. The new process will utilize all 6-inch tools such as the state-of-the-technology Canon FPA 2000I i-line Stepper, the SSI Coat/Develop Track, ASM Low Pressure Chemical Vapor Deposition (LPCVD) system, BTI 6" Furnace stack and the DryTek Quad Plasma system. Technology advances such as dual well, Low Doped Drain (LDD) region, 150Å gate oxide, and titanium silicide contacts are implemented in this process. The process is designed and optimized to fabricate transistors with channel lengths smaller than 0.8 microns.

The layout for the Advanced CMOS testchip has channel lengths ranging from 10 microns to 0.5 microns. The devices are designed for 5 Volts operation. With further improvements in the process, the supply voltage can be brought down as low as 3.3 Volts. The formation of a new process also involves development of new etching techniques. Currently, RIT students are working on improved anisotropic etching processes for 6-inch wafer fabrication.

New procedures for device testing will focus on some of the unique characteristics of short channel MOSFET's. The Testchip is designed with varying channel lengths for easy testing of the relationship between the threshold voltage (V_t) and the decreasing channel length (threshold-voltage roll-off). Further testing can be performed to study the subthreshold characteristics of the devices, such as the off-state current and the subthreshold swing (S).

3. DESIGN THEORY

It is essential to lay down some foundation before developing the process flow. Basic understanding of the MOSFET device physics can be used to calculate the required gate oxide thickness and other key steps such as the well concentration and threshold adjust implant, if needed. The transistors were designed for a drain voltage of $+5V$ and the channel length of $0.5 \mu m$ is used in the following calculations.

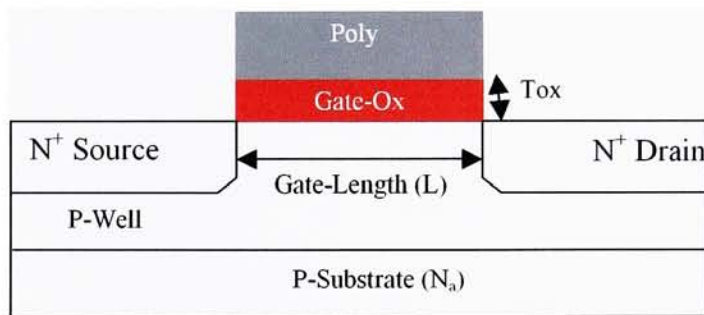


Fig 3.1 The NMOS device

In this section, the following parameters are calculated:

- 1) Gate oxide thickness
- 2) Long Channel Threshold Voltage (V_{TLC})
- 3) The Subthreshold Swing (S)
- 4) The Short Channel Threshold Voltage (V_{TSC})
- 5) Leakage and Full-drive currents
- 6) The Early Voltage

3.1 Basic Equations

There are several basic equations used to solve for some primary device parameters such as the threshold voltage, saturation current and the sub-threshold swing. A few of these equations are shown in this section

The Work Function for n-type and p-type silicon substrates are shown below:

$$\phi_{n-type} = \frac{kT}{q} * \ln\left(\frac{N_d}{n_i}\right) \quad (1)$$

$$\phi_{p-type} = \frac{kT}{q} * \ln\left(\frac{N_a}{n_i}\right) \quad (2)$$

where the thermal voltage, $\frac{kT}{q} = 0.0259V$

The metal-semiconductor workfunction (Φ_{ms}) is the difference between the gate and the bulk silicon contact potential, as shown below.

$$\Phi_{ms} = \phi_{gate} - \phi_{bulk} \quad (3)$$

Another required equation is that of the gate oxide capacitance, as shown in equation 4.

$$C_{ox} = \frac{\epsilon_o K_o}{t_{ox}}, \quad (4)$$

where ϵ_{ox} is the permittivity of free space ($8.85 \times 10^{-14} \text{ F/cm}$), K_o is the dielectric constant for silicon-dioxide (3.9) and t_{ox} is the oxide thickness.

3.2 Gate-Oxide Calculation

To prevent Fowler Nordheim (F-N) tunneling ^[9] from taking effect, the electric field across the gate oxide should be less than 4 MV/cm. Using this criteria the oxide thickness can be calculated as follows:

$$t_{ox} \geq \frac{V_{dd}}{4 \frac{MV}{cm}} = \frac{5.0 \text{ Volts}}{4 \frac{MV}{cm}} = 1.25 \times 10^{-6} \text{ cm} = 125 \text{ \AA} \quad (5)$$

The calculated value for the gate-oxide thickness is **125 Å**. However, a 'practical' value of 150 Å is chosen for the gate oxide thickness. It is necessary to have the gate oxide as thin as possible, while avoiding tunneling (F-N).

It is also necessary to calculate the well doping required in order to successfully fabricate a working

transistor. In order to do this, a few initial assumptions are made. The well doping will be calculated in the following sub-section, which applies to NMOS transistor.

3.3 Long Channel Threshold Voltage

The following initial conditions are used to calculate the theoretical value for the long channel threshold voltage (V_{TLC}). The IC Industry's target threshold voltage has been 0.6 - 0.8 volts, for a rail potential of 5 volts.

1st initial condition:

- $\Phi_{ms} = -1$ volts, where Φ_{ms} is the metal-semiconductor work function.
- $\Psi_{SUR} = 1$ volts, where Ψ_{SUR} is the substrate surface potential in strong inversion.

2nd initial condition:

- Choose $V_{TLC(NMOS)}$, which is also the target value = 0.8 volt

The equation on the following page can be used to calculate the oxide capacitance (C'_{ox}) for either transistor.

$$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{0.0345}{0.0150} = 2.30 \frac{fF}{\mu m^2} = 2.30 \times 10^{-7} \frac{F}{cm^2} \quad (6)$$

The doping density (NMOS in p-well (N_A)) can now be calculated using the threshold voltage equation for a long channel device,

$$V_{TLC} = \Phi_{ms} + \psi_{SUR} + \gamma \sqrt{\psi_{SUR}} \quad (7)$$

where γ is gamma of the transistor. Substituting for V_{TLC} , Φ_{ms} and ψ_{SUR} , the equation simplifies as,

$$0.8 = -1 + 1 + \gamma \sqrt{1} \Rightarrow \gamma = 1.0 \text{ volt}^{\frac{1}{2}} \quad (8)$$

Gamma is defined by the equation,

$$\gamma = \frac{F \sqrt{N_A}}{C'_{ox}} \quad (9)$$

where, $F = 0.00579 fF * V^{1/2} * \mu m^{-1/2}$ and N_A is the p-well doping concentration. Substituting for F and C_{ox} reveals the value for N_A :

$$N_A = 1.0 \times 10^{17} / cm^3$$

The Fermi work function (ϕ_f) can now be calculated using the following equation;

$$\phi_f = kt * \ln\left(\frac{N_A}{ni}\right) = (0.0259) \ln\left(\frac{1.0 \times 10^{17}}{10^{10}}\right) = 0.417v \quad (10)$$

$$2\phi_f = 0.835v$$

The metal to semiconductor work function (ϕ_{ms}) can now be easily calculated. This is given as,

$$\phi_{ms} = \phi_{bi} = -\frac{Eg}{2} - \phi_f = -\frac{1.12}{2} - 0.417 = -0.977volts \quad (11)$$

where ϕ_{bi} is the built-in potential.

Substituting the calculated values into equation 7, and assuming the source-bulk voltage (V_{sb}) to be zero, reveals a new value for V_{TLC} .

$$V_{TLC} = -0.977 + 1 + 0.8 = 0.823v$$

The inversion charge (Q'_I) can be calculated, which can be used to find the surface density (n_s).

$$Q'_l = -C'_{ox} [V_{gs} - V_{TLC}]$$

$$V_{gs} = 5 \text{ volts}$$

$$Q'_l = -2.30 \frac{fF}{cm^2} * [5 - 0.823] = -9.61 \frac{fC}{\mu m^2}$$

The surface density calculations are as follows:

$$n_s = \frac{Q'_l{}^2}{F^2 \phi_t} \quad (13)$$

$$n_s = \frac{-9.61^2}{0.00579^2 * 0.0259} = 1.06 \times 10^8 \mu m^{-3} = 1.06 \times 10^{20} cm^{-3}$$

Using the calculated values find the surface potential

(ψ_{SUR}):

$$\psi_{SUR} = 2\phi_F + a\phi_t \quad [8] \quad (14)$$

$$\text{where } a = \ln\left(\frac{n_s}{N_A}\right) = \ln\left(\frac{1.06 \times 10^8}{1.0 \times 10^5}\right) = 6.97$$

$$\psi_{SUR} = 0.835 + 6.97 * 0.0259 = 1.02 \text{ volts}$$

Recalculating all the parameters, including V_{TLC} :

$$V_{TLC} = -0.995 + 1.02 + 0.8 * \sqrt{1.02} = 0.83 \text{ volts}$$

$$Q'_I = -C'_{ox} [V_{gs} - V_{TLC}] = Q'_I = -2.3 * [5 - 0.833] = -9.58 \frac{fC}{\mu m^2}$$

$$n_s = \frac{Q'_I{}^2}{F^2 \phi_i} = \frac{-9.58^2}{0.00579^2 * 0.0259} = 1.06 \times 10^8 \mu m^{-3} = 1.06 \times 10^{20} cm^{-3}$$

$$a = a = \ln\left(\frac{n_s}{N_A}\right) = \ln\left(\frac{1.06 \times 10^8}{1.0 \times 10^5}\right) = 6.96$$

$$\psi_{SUR} = 2\phi_F + a\phi_i = 0.835 + 6.96 * 0.0259 = 1.02 \text{ volts}$$

Therefore a well concentration of $1.0 \times 10^{17} cm^{-3}$ will result in a V_{TLC} of **0.83 volts**, which is less than 5% error from the target of 0.8 volts.

3.4 OFF STATE CONSIDERATIONS

When the transistor is 'off', or the applied gate voltage is less than the threshold voltage, certain parameters, namely the subthreshold swing, the short channel threshold voltage and the off-state current (leakage current) are extracted to characterize the quality of the transistor.

3.4.1 The Subthreshold Swing

This parameter describes how quickly the transistor can be turned off. This is measured as the reciprocal-slope of off-state characteristic (in the Log I_d versus V_g graph), and is denoted as 'SS', 'S' or 'S_t'. It simply shows the amount of gate voltage that is required to cause a one-decade change in the drain current. Long channel devices demonstrate higher subthreshold swing than the short channel ones due to the independence of drain on the channel depletion. The value can be calculated from a log I_d versus gate-source potential (V_{GS}) chart. Ideally, the value for subthreshold swing will never be less than 60mV/decade, as signified by the equation below:

$$\text{Ideal Swing} = 0.0259 * \ln(10) = 60mV$$

where 10 is the change in drain current.

To calculate the swing for the NMOS transistors, the following equation will be used^[1].

$$S = 60mV * n \quad (15)$$

$$n = 1 + \frac{\gamma}{2 * \sqrt{1.5\phi_F}} \quad (16)$$

Substituting the values found in the previous section results in a value of 1.51 for 'n', which leads to a swing of 90.3mV. This means that it takes 90.3mV to cause a decade drop in the drain current, or **90.3mV/decade**.

3.4.2 The Short Channel Threshold Voltage (V_{TSC})

As mentioned in the previous section, the short channel threshold voltage has to be four times the subthreshold swing (S). This is an approximate value, but is acceptable for all calculation henceforth.

$$V_{TSC} \sim 4 * S = 361mV$$

3.4.3 Off-state Current

To find the leakage current the following relationship is used^[8].

$$\frac{I_D}{z} = \frac{\mu_0 \phi_i |Q'_{IS}|}{L} \quad (17)$$

where I_D/z is the drain current per micron of channel length and Q_{IS}^l is the inversion charge depicted by the following equation^[8]:

$$Q_{IS}^l = \frac{-F\sqrt{N_A}}{2\sqrt{\psi_{S(x=0)}}} * \phi_i * e^{\frac{\psi_{S(x=0)} - 2\phi_F - V_{sb}}{\phi_i}} \quad (18)$$

$$\psi_{S(x=0)} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{gb} - V_{FB}} \right)^2 \quad (19)$$

Substituting the numbers found from the previous calculations, $\Psi_{SI} = 0.443$ volts. Q_{IS}^l is calculated to be $-9.52 \times 10^{-9} \text{ fC}/\mu\text{m}^2$.

Entering the above values into equation 17 reveals the maximum off-state current for a given width and a $0.5\mu\text{m}$ transistor is $29.6 \text{ pA}/\mu\text{m}$. This value is acceptable because it is greater than 4 decades of current less than $1 \mu\text{A}/\mu\text{m}$.

3.5 ON STATE CONSIDERATIONS

While the transistor is in the operational mode it is desirable to know the full-drive current. The Early

voltage is also calculated, which will determine the capability of the transistor as a current source.

3.5.1 Full-drive Current

The following series of equations are used to calculate the full drive current.

$$\frac{I_{Dsat}}{z} = \frac{v_l C_{ox}^l (V_{gs} - V_{TSC})^2}{(V_{gs} - V_{TSC}) + L * E_{sat}} \quad (20)$$

$$E_{sat} = \frac{2v_l}{\mu_n}$$

$$v_l = 1 \times 10^{11} \frac{\mu m}{s}$$

$$\Theta = \frac{2 \times 10^{-7} \frac{cm}{V}}{t_{ox}} = 0.133 V^{-1}$$

Full drive can be achieved when $V_{gs} = V_{dd} = 5$ volts,

$$\mu_n = \frac{\mu_0}{1 + \Theta(V_{gs} - V_{TSC})} = \frac{65}{1 + 0.133(5 - 0.361)} = 40.2 \frac{cm^2}{V \cdot s}$$

$$E_{sat} = \frac{2 * 10}{40.2} = 4.98 \frac{V}{\mu m}$$

Entering all the above-calculated values into equation 20 results in a full drive current of $0.69 \text{ mA}/\mu\text{m}$.

3.5.2 Early Voltage

The following relationship can be used to calculate the Early voltage.

$$V_A = \frac{1}{\lambda} V_{ds_{sat}} \quad (20)$$

λ and $V_{ds_{sat}}$ have to be calculated.

$$V_{ds_{sat}} = \frac{(V_{gs} - V_{TSC})LE_{sat}}{(V_{gs} - V_{TSC}) + LE_{sat}} = \frac{(5 - 0.361) * 4.98}{4.98 + 5 - 0.361} = 2.4 \text{ volts}$$

The velocity saturation region can be calculated as follows^[9]. The value for ' λ ' has been previously calculated, and is an approximate value.

$$\Delta L = l * \sinh^{-1} \left[\frac{V_{ds} - V_{ds_{sat}}}{L * E_{sat}} \right] \sim 0.1587 * \sinh^{-1} \left[\frac{5 - 2.4}{0.1587 * 9.95} \right] = 0.20 \mu\text{m}$$

Proceeding with the relationship between the drain current and $V_{ds_{sat}}$ will result in a value for λ .

$$\frac{I_D}{I'_D} = \left[\frac{L - \Delta L}{L} \right] * \left[\frac{\frac{V_{gs} - V_{TSC}}{L - \Delta L} + E_{sat}}{\frac{V_{gs} - V_{TSC}}{L} + E_{sat}} \right] = 0.793$$

$$\frac{I_D}{I'_D} = 1 + \lambda(V_{ds} - V_{ds_{sat}})$$

$$\lambda = \frac{0.793 - 1}{5 - 2.4} = -0.0796$$

$$V_A = \frac{1}{\lambda} - V_{ds_{sat}} = -14.96 \text{ volts}$$

The Early voltage is exactly three times the rail voltage. This enables the transistor to deliver close to a constant amount of current while varying the V_{ds} potential, in the saturation region of operation.

4. PROCESS DEVELOPMENT

The process development for the RIT's Sub-micron CMOS was divided into 2 main sections:

- I. Chip Layout - Generation of the chip layout using the CAD software available and fabrication of masks with dual fiducial marks for the GCA g-line Stepper and the Canon i-line Stepper.
- II. Process Flow - Detailed steps in fabricating the CMOS devices.

4.1 Chip Layout

The chip was designed using ICGraph (by Mentor Graphics), which runs on an HP-UNIX based machine. The design rule used was $0.5\mu\text{m}$ (λ). This smallest channel length on the die is $0.5\mu\text{m}$. The maximum channel length was chosen to be $10\mu\text{m}$. Large channel lengths will compensate for overlay errors when the same mask set is used in the GCA 6700 Stepper. Two gate widths were used; $8\mu\text{m}$ and $16\mu\text{m}$. Some of the test structures such as the Van-der Pauw's and CBKR's were copied from the current CMOS test-chip layout. Other structures include the ring oscillator and Op-amps.

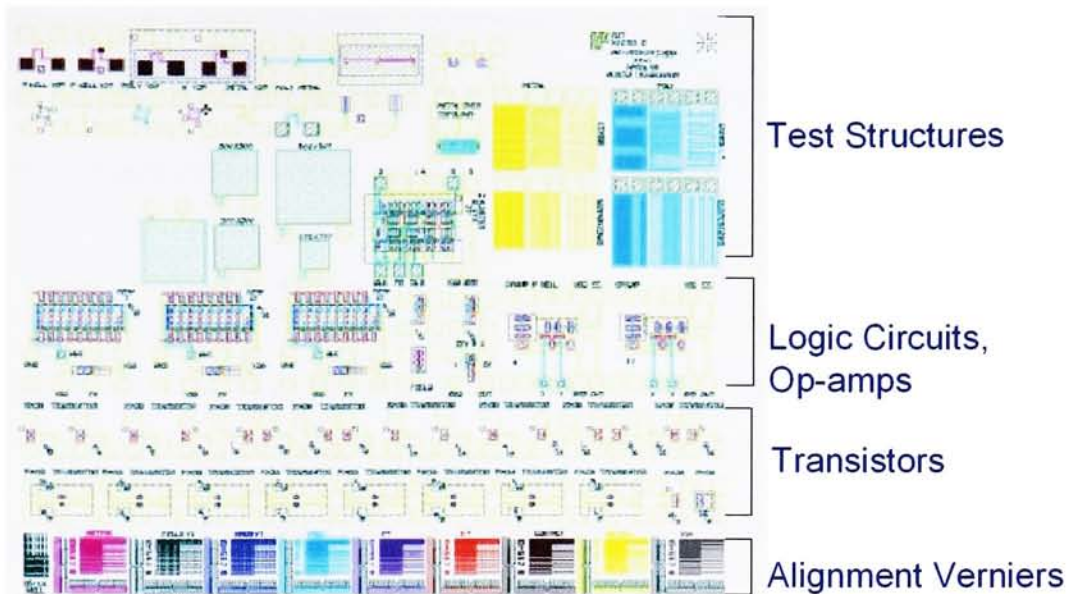


Fig 4.1 The Sub-micron CMOS chip layout

The masks were designed with the intention of using them in either the GCA or the Canon Stepper. This also means that the devices can be fabricated on 4" wafers.

4.2 Process Flow

The Sub-micron CMOS process shares few of the processing steps with the current PW-3 CMOS Process^[5], namely the LOCOS process and some of the oxide growths (500Å pad oxide, 1000Å Kooi oxide and 5000Å Field Oxide). Since it's a new process developed for 6" wafer, and it involves the usage of new equipment, new processes have to be developed mainly for diffusion and dry etching. In

addition to this, the equipment and the defining factors have to be characterized and optimized for uniformity, etch rate, deposition rate and film quality.

The key step in achieving the sub-micron channel lengths is in the dry-etch process. It has to be optimized for anisotropy with accurate end-point detection. The following steps outline the sub-micron CMOS process.

4.2.1 Substrate

The substrate is Boron doped, p-type wafer, 15-20 Ω -cm. It would be ideal to begin the device processing on a wafer with an epitaxial layer. The wafers are scribed on the backside of the wafers followed by an RCA clean. Megasonics cleaning should be incorporated with the RCA clean to remove particles from the wafer surface.

4.2.2 The Twin Well

LOCOS process is used for defining the twin-well. The first step in LOCOS is to grow the 500Å stress relief pad oxide. The oxide is grown at 1000°C in oxygen ambient for 48 minutes. The following step is a deposition of 1500Å of

silicon nitride. The deposition is performed in the ASM LPCVD at a temperature of 900°C. Being a standard deposition step used in PW-3 CMOS, the recipe should already be available for use.

The first lithography step defines the n-Well windows. Resist will be spin-coated on the SSI 6" Track, using a standard coat program for the i-line resist. The wafers will then be exposed using Level 1 mask on the Canon FPA 2000I i-line stepper, followed by the develop process on the SSI Track. Prior to the first lithography step, an optimized resist process for obtaining features 0.5µm or less should be developed. This is not required for the first level, however it will be an issue for the gate lithography.

Dry-etch the nitride in the Drytek Quad, stopping at the pad oxide. The gas, power and pressure settings are the same as those used in the Factory CMOS Process, and can be found outlined in MESA (work-in-progress tracking software from Camstar Systems). The pad oxide acts as a buffer zone for the high-energy n-well implant.

The p-well is formed by implanting phosphorous (P_{31}) at a dose of $2 \times 10^{12} \text{ cm}^{-2}$ with energy of 150 KeV. To prevent polymerization of the resist, the implant current should not exceed $25\mu\text{A}$.

Plasma strip the photoresist, followed by an RCA clean. Grow 5000\AA oxide in the Bruce furnace using Recipe 350. This is done at 1100°C in steam for 48 minutes. This oxide will also mask the n-well implant. Dry etch the nitride layer in the DryTek Quad. The underlying oxide layer is the pad oxide, through which the boron is implanted. The gas used is BF_3 , and the species is B_{11} , implanted at a dose of $2.5 \times 10^{13} \text{ cm}^{-2}$ at 50 KeV.

Finally, the well drive in performed at 1100°C for 210 minutes in nitrogen ambient. A new recipe needs to be written and verified on the Bruce furnace. Figures 3, 4 and 5 shows the wafer crossection and the simulation results for p-well and n-well, respectively.

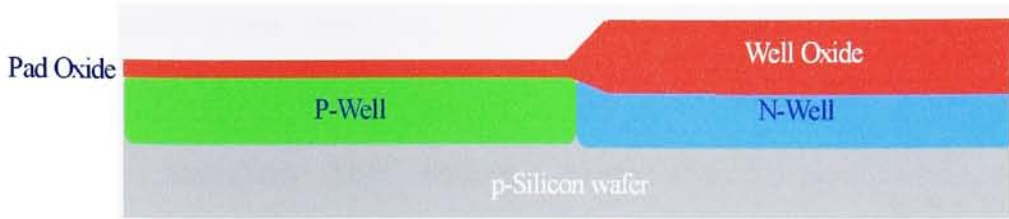


Fig 4.2 Crossection after the Well drive-in

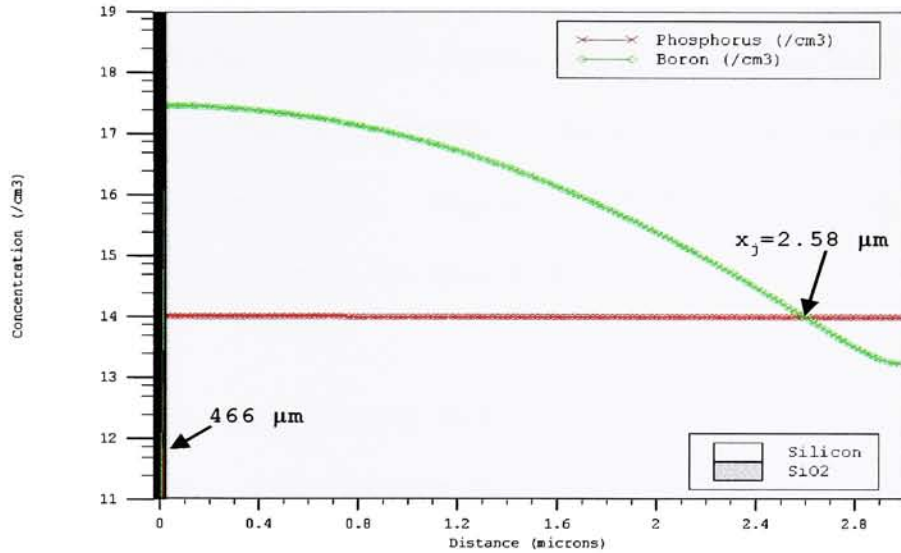


Fig 4.3 N-Well junction depth after drive-in

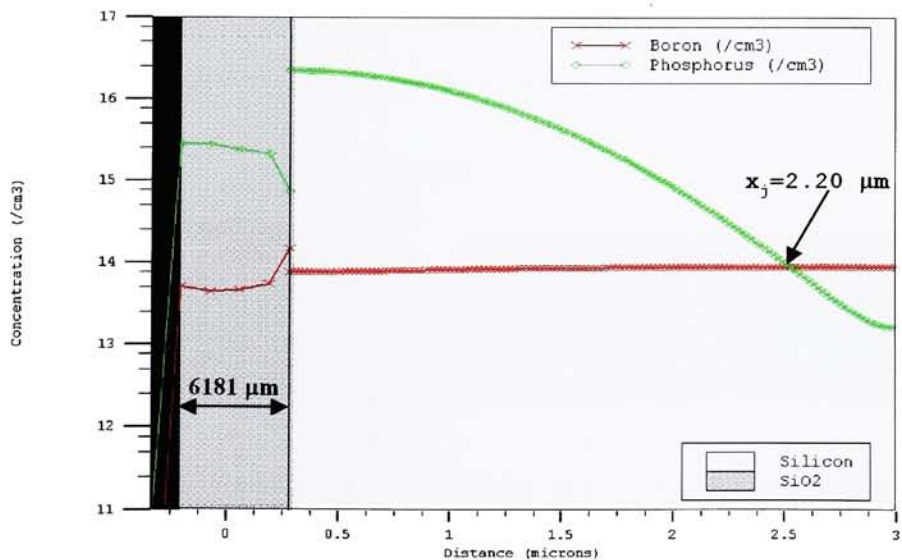


Fig 4.4 P-Well junction depth after drive-in

4.2.3 Channel Stop Implant

After forming the wells, completely etch the 5000Å oxide in BOE for approximately 6 minutes. Ensure that all the oxide is removed by measuring the oxide thickness over the n-well regions. An RCA clean should be performed prior to growing the 500Å pad oxide. This is the beginning of the second LOCOS process. Deposit 1500Å of Si₃N₄ using the standard Nitride process on the ASM 6" CVD.

The second lithography defines windows for etching the silicon nitride. The lithography process is similar to the one outlined in the previous section. Silicon nitride is then etched in the DryTek quad using the Factory recipe. A third lithography steps defines the active area. The crosssection is shown in figure 4.4.

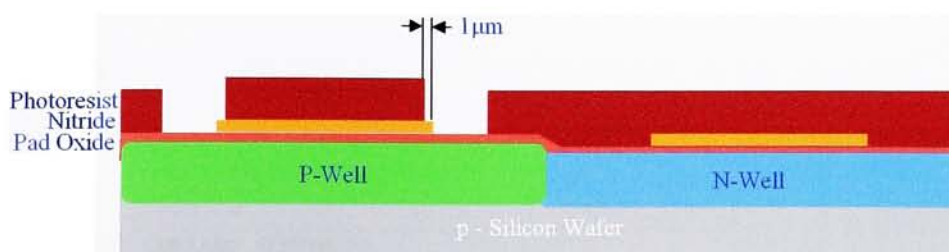


Fig. 4.5 Crosssection after active lithography

In order to prevent depletion of active boron in the well during the field oxide growth caused due to the boron segregation, a channel stop implant is performed. It's also referred to as the guard ring, because the implant is around the NMOS device. The B₁₁ implant is done at 100 KeV with a dose of $8e13 \text{ cm}^{-2}$. The peak of the implant is at $0.3\mu\text{m}$, which is approximately 44% of the FOX thickness.

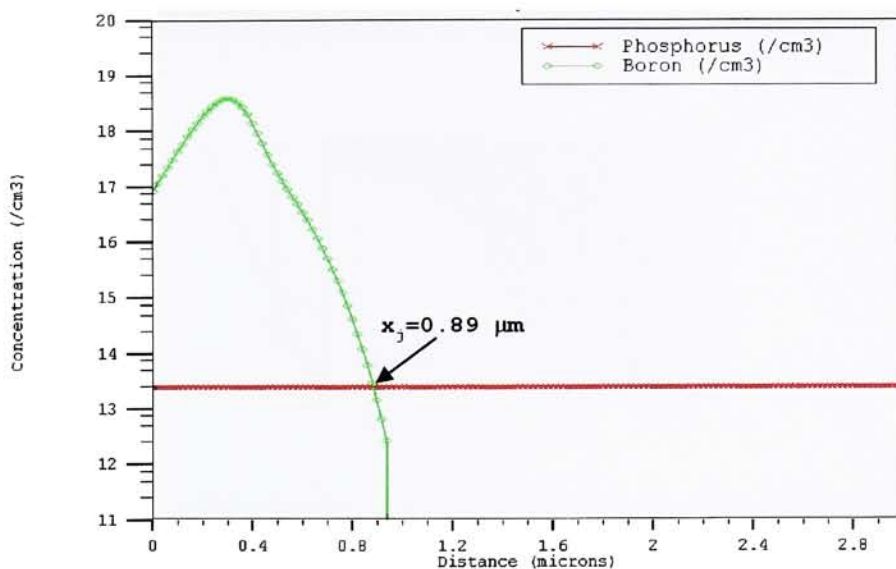


Fig 4.6 Simulation of the channel stop implant

4.2.4 Field Oxide Growth

Field oxide was used as the isolation method. There currently exists a good process for growing field oxide, which will require slight modification to the soak time so

as to obtain the target thickness of 6500Å. Prior to the field oxide growth, the photoresist is stripped in the Asher followed by an advanced cleaning procedure combining RCA and Megasonic cleaning. The wafers are then loaded into Tube 1 of Bruce furnace, for wet oxidation.

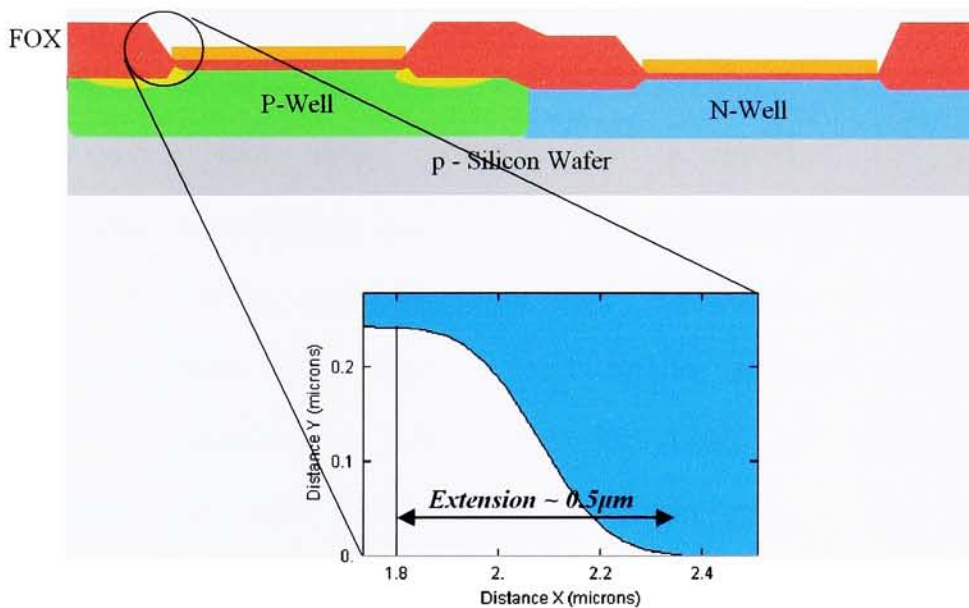


Fig 4.7 'Bird's Beak' Extension After Field Oxidation

4.2.5 Gate Oxide

The most critical oxide in the process is the gate oxide. The quality and the thickness of this oxide will determine the final behavior of the device. The IC Industry spends endless effort in growing very high quality gate oxide. As the thickness keeps decreasing to few

atoms, the purity and thickness control becomes an issue. The gate oxide thickness in this process is 150Å. However, a clean oxidation step is still required. TCA clean is commonly used in the gate oxide growth here at RIT to remove metallic contamination impregnated in the quartz furnace tube.

Before growing the gate oxide, silicon nitride is dry-etched using the same process as described in section 4.2.2. The underlying pad oxide is etched away in buffered oxide etch (BOE) for 60 seconds, followed by the Kooi oxidation. This is a sacrificial oxide used to remove the Nitride contamination (which could lead to thinning of gate-oxide) at the FOX to Well interface. The target thickness for the Kooi oxide is 1000Å and the Bruce furnace recipe is that will be used is 310. The oxide is grown at 1000°C, and the soak time is 45 minutes.

Remove the Kooi oxide in BOE (~60 seconds), followed by an RCA and Megasonics clean. While the wafers are going through the cleaning process, prepare Tube 4 on the Bruce furnace for gate oxidation. The tube must be cleaned using TCA for 20 (or even longer) minutes prior to gate-oxide growth. The tube clean should be performed with the paddle

and the wafer boat inside the tube. A new Bruce furnace recipe needs to be created with ramp up from 800°C to 1000°C in dry-O₂ and 40-minute soak time in oxygen ambient.

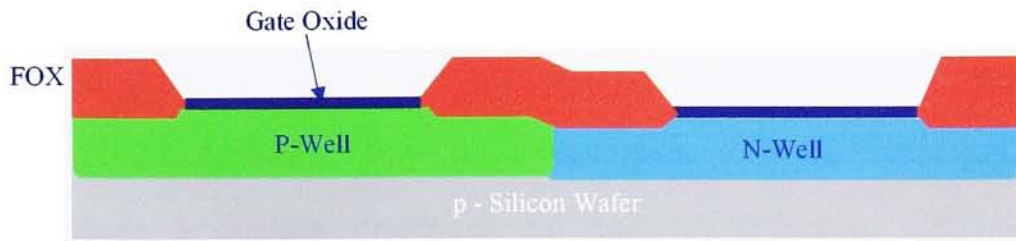


Fig 4.8 Crossection after gate-oxidation

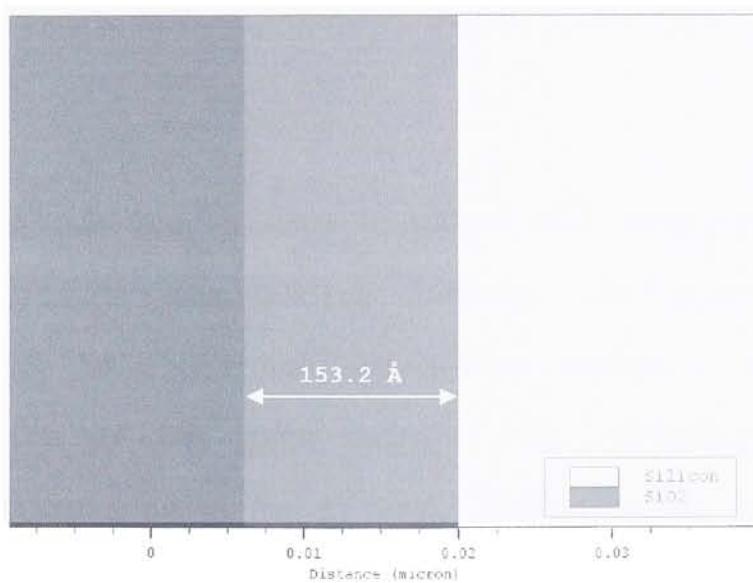


Fig 4.9 Simulation of the gate oxide growth

4.2.6 Polysilicon Deposition

Polysilicon is commonly used as the conductive material for the gate. The greatest advantage attained by using polysilicon, is the ability to control the metal work function of the device. By doping the poly with either boron or phosphorus, the work function can be changed. It has become a common practice in the IC industry to use n+ poly for the NMOS device and p+ poly for the PMOS device. The advantage of using p+ poly over n+ poly for the PMOS device is discussed in Section 6 as a process improvement suggestion.

In the sub-micron CMOS process, the poly thickness is 4200Å, and is n+ (phosphorus) doped. The poly should be thick enough to block the subsequent implants, to prevent contamination of the gate oxide. The thickness selected will block implants up to 95 KeV. Polysilicon is deposited in the ASM CVD at a temperature of 610°C. The gas used in this process is Silane. As Silane breaks down at this temperature, it coats the tube and any material in it with silicon. Deposition time should be calculated from the control charts in MESA. Since the PW-3 CMOS Process calls for 6000Å, the time required for the poly deposition would

be half that. It is also recommended to include few control wafers with 1000Å oxide so as to measure the poly thickness on the Tencor Nanospec.

4.2.7 Doping the Polysilicon

The polysilicon is phosphorus doped, making it n+. Due to the unavailability of in-situ doping and a 6" Ion-implanter, a simpler method, although primitive by standards, is used. Spin-on dopant, N-250 from Allied Signal, is used to dope the poly. This method is used in the current PW-3 CMOS Process.

The spin-on dopant is applied onto the wafers at 3000 RPM, followed by an oven bake (solvent bake), in the Blue-M Oven, at 200°C. The wafers are then annealed in the Bruce Furnace at 1000°C for 7.5 minutes. The wafers should not be soaked for a long time due to the possibility of contaminating the gate-oxide.

The thermal process forms a thin layer of Phospho-Silicate Glass, which needs to be removed before the next step. The wafers are placed in the BOE bath for a minute to etch away the 'skin'.

4.2.8 Gate Lithography

This is the most critical lithography in the CMOS process. The smallest feature is 0.5 microns, which calls for an optimized lithography process. The wafers should be primed with HMDS and then baked at 100°C in the Blue-M oven, prior to sending them through the Track. The SSI 6" Coating track will be used to apply a uniform coating of the i-line resist, with the primer dispense turned off. The wafers will then be exposed using the gate mask. SSI Track will again be used for developing.

4.2.9 Defining the Gate

Polysilicon can be etched either in the GEC Cell or the DryTek Quad. Both tools accept 6" wafers. If the GEC tool is used for etching the poly gate, use SF6 and CHF3 gases at a pressure of 50 mTorr and a power of 40 watts. The etch rate on a 4" wafer with these settings was determined to be 300 Å/min. However, if the Drytek Quad is to be used, the pressure, power and ratio of the gas composition needs to be determined from the log sheets or MESA. It is very important to stop at the gate oxide, as it acts as the buffer zone for the n- LDD implant. Use the

dummy wafers from the poly deposition step to calculate the etch rate of polysilicon. In addition to this, the plasma etch should be anisotropic, producing near-vertical sidewalls. Figure 4.9 shows the crosssection expected after the polysilicon etch.

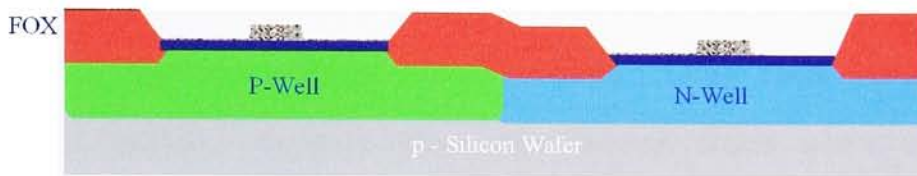


Fig 4.10 Crosssection after polysilicon etch

4.2.10 N- and P- Source/Drain Implant

The Sub-micron CMOS process uses lightly doped drain/source (LDD) regions to minimize hot carrier effects. Hot carriers affect the device performance over time, the most important being the shift in threshold voltage. In NMOS transistors, LDD's are used for devices smaller than 1 μm , and for 0.8 μm or smaller in PMOS transistors.

The S/D lithography mask is same as the p-well mask. The lithography is performed on the 5X Canon i-line

stepper. The wafers undergo a phosphorus implant with a dose of $5 \times 10^{13} \text{ cm}^{-2}$ at energy of 65 KeV.

The wafers are then ashed and send through the resist coating line on the SSI track, preparing them for the next lithography step. The mask used is the inverse of the n-LDD. The implant species for forming the P- LDD is BF_2 . The main reason behind this being the fact that the resulting implant energy that the boron atom gets is ~23% of the total energy. Using BF_2 is an advantage where low energy implants are not possible. The dose for this implant is $4 \times 10^{13} \text{ cm}^{-2}$ at an energy of 75 KeV. Finally, plasma strip the photoresist and perform an RCA and Megasonics clean. The anticipated crossection will look as follows.

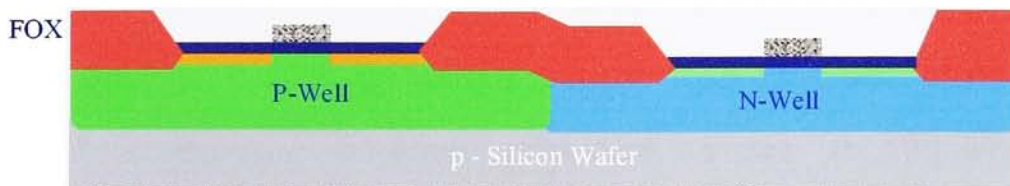


Fig. 4.11 Crossection showing the LDD's

4.2.11 Formation of the Source & Drain

The final implants are the source and drain implants. These will be at a higher concentration than the n- and the p- implants. The first step in the sequence for forming the n+ and the p+ region is the deposition of low temperature oxide (LTO). This will be performed in the ASM CVD. The gases used for LTO deposition is silane and oxygen and the deposition temperature is 400°C. The target thickness is 6500Å, resulting a fairly planar surface. Deposition time has to be calculated from the SPC charts in MESA or from the log sheets.

Next step calls for an etch-back of the LTO. Anisotropy is the key at achieving sidewall spacers. The pressure and time were determined in a previous project by the author, which has to be verified before performing the etch on the device wafers. The optimized recipe for the GEC Cell is: CF₄ = 25 sccm, H₂ = 5 sccm, pressure is set at 100 mTorr, the RF power is 60 watts and the platen temperature is 19.2°C. After a successful etch-back, the crossection should be identical to figure 4.11. The SEM crossection (figure 4.12) clearly illustrates the sidewalls along the poly line.

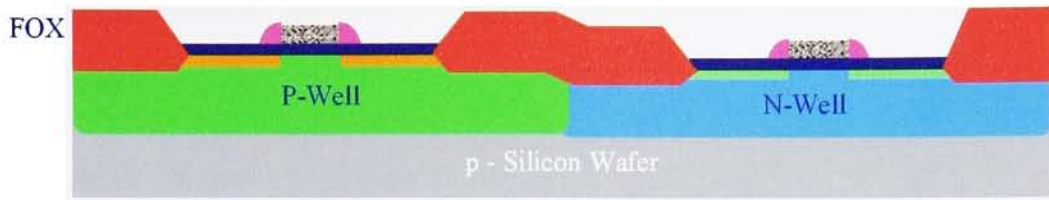


Fig. 4.12 Crosssection after LTO etch-back

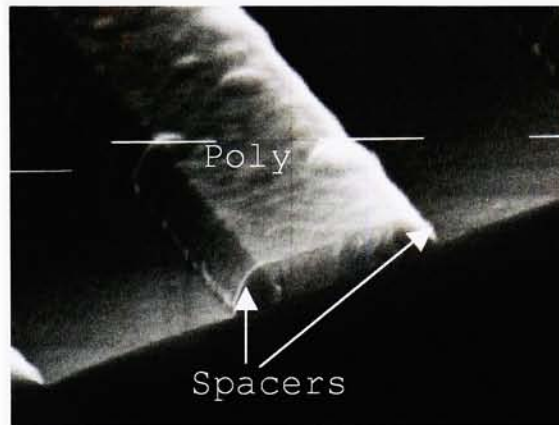


Fig. 4.13 SEM micrograph of sidewall spacers

After forming the spacers a lithograph step, using the same mask for n- LDD, opens windows for the NMOS S/D high dose implant. This phosphorous implant is $3.25 \times 10^{15} \text{ cm}^{-2}$ with an energy of 85 KeV. After removing the photoresist, another lithography using the p- LDD mask defines areas for the PMOS S/D implant. This implant uses BF₂, which can produce shallow junctions. The dose is $6.0 \times 10^{15} \text{ cm}^{-2}$, and the energy is 120 KeV. The implant current should not exceed 30 μA , as this will cause polymerization of the photoresist that cannot be removed by any means, even in

the well known piranha etch (Sulfuric acid + Hydrogen Peroxide)!

The next step involves a dry etch. This is the removal of the 150Å over the S/D regions of the devices. To prevent lateral etching, leading to the thinning or loss of the sidewalls, an anisotropic etch is required.

After RCA clean, the wafers will need to be annealed. The annealing step is performed in the Bruce Furnace at 900°C, for 10 minutes in an inert ambient. The crosssection and simulation results are shown in figures 4.13, 4.14 and 4.15, respectively. The expected junction depths are shown on the simulation graphs. It's highly recommended to have a high flow of nitrogen to prevent oxidation of the polysilicon or the source/drain regions. Any oxide present will affect the silicide process later on.

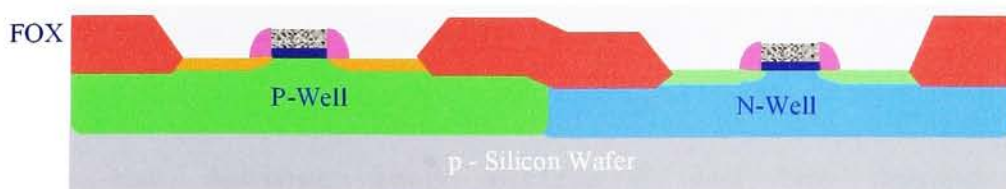


Fig 4.14 Crosssection after S/D implant and anneal

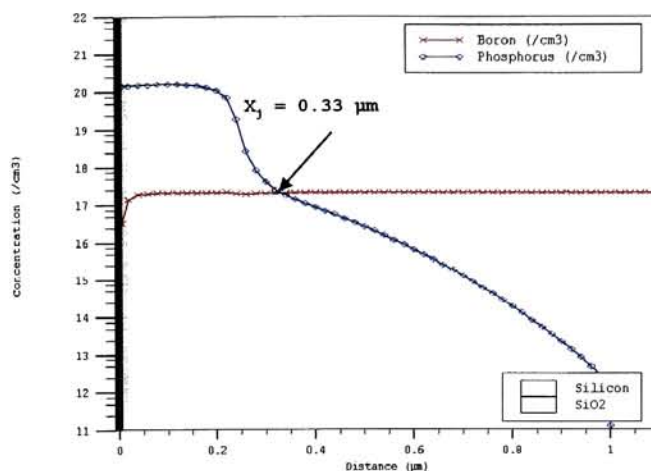


Fig 4.15 Simulation of NMOS S/D implant and anneal

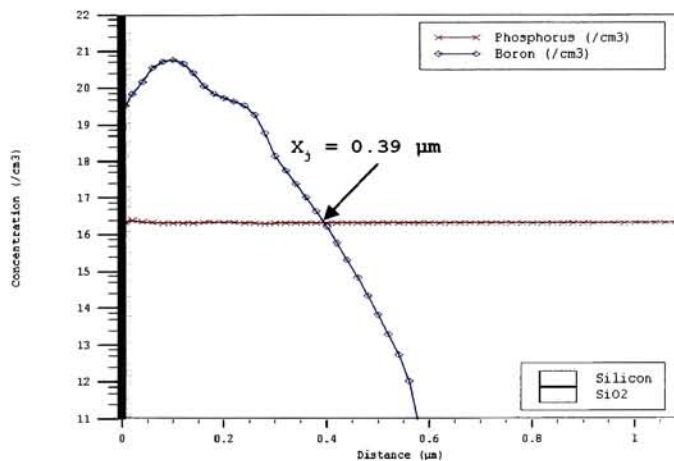


Fig 4.16 Simulation of PMOS S/D implant and anneal

4.2.12 Titanium (Self Aligned) Silicide

As the devices keep shrinking and the demand for faster devices keep rising, the contact technology becomes more challenging. Contact resistance can cause a hindrance to achieving faster devices. Silicides are therefore

commonly used by the IC industry to reduce the contact resistance. Some of the most common silicides are tungsten silicide (WSi_2), cobalt silicide (CoSi_2) and titanium silicide (TiSi_2). This process uses titanium silicide, due to its process simplicity. Previous studies carried out by the author showed that better results are obtained when an RTP is used for the thermal steps in the formation of the silicide^[4].

The formation of titanium silicide is a three-step sinter process using the RTP. During the thermal steps, titanium chemically reacts with silicon to produce the very low resistive alloy (TiSi_2). The process of forming the silicide begins with deposition of titanium. 1100Å of titanium metal is sputtered at a pressure 5 mTorr in Argon ambient, with a pre-sputter time of 10 minutes. The pre-sputter time should be longer if the target hasn't been used for a while. The DC power depends on the size of the target used, which could be either 4" or 8". The actual deposition time has to be calculated from the log sheets.

Titanium di-silicide, also called titanium silicide, cannot be patterned using conventional etch techniques, whereas Titanium can easily be etched in a hot ammonium

hydroxide and peroxide solution. Taking this into account, the formation of $TiSi_2$ is broken down into 3 main parts. A study here at RIT has shown that RTP annealing produces good results for the formation of the silicide. First thermal phase (700°C, 30 seconds in N₂ ambient) forms Titanium mono-silicide, a high resistive material, compared to its latter, the disilicide. Since titanium only reacts with silicon, the presence of the oxide sidewall spacers will inhibit the formation of silicide. This selective silicidation is also referred to as **self aligned silicide** or Salicide.

The second step, which is a wet etch, removes any unreacted titanium. The chemical solution consists of ammonium hydroxide (NH₄OH), hydrogen peroxide (H₂O₂) and DI water in a ratio of 1:1:5, respectively. The final thermal step (800°C, 30 seconds in N₂ ambient) forms titanium disilicide. During this thermal step, silicon is consumed and it is able to determine the thickness of the silicide using the Tencor Alphastep.

The graphical cross-section and a SEM cross-section are shown in figures 4.16 and 4.17.

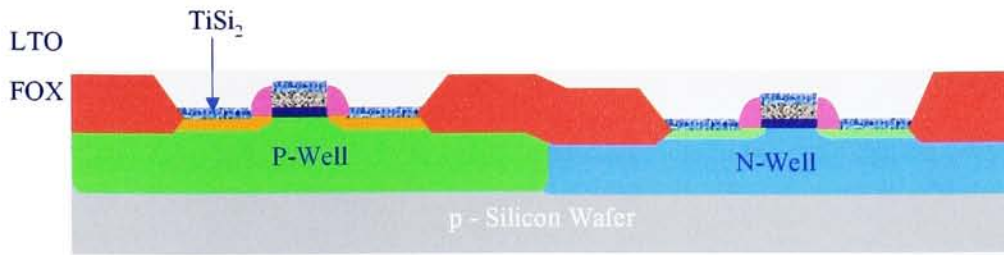


Fig. 4.17 Formation of Titanium Silicide

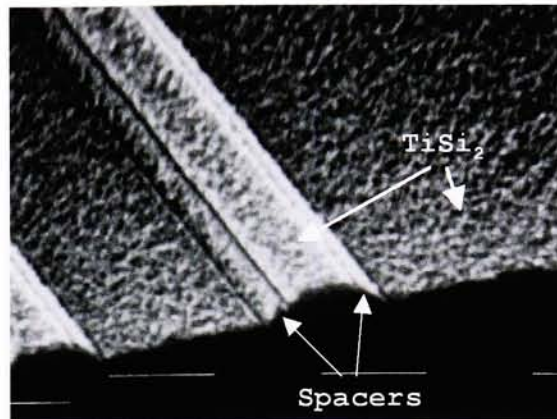


Fig. 4.18 SEM Micrograph of TiSi_2

4.2.13 Contact Cuts

After the formation of titanium silicide, 4000\AA of LTO is deposited. This is done in the ASM CVD at deposition temperature of 400°C . The gases used are silane and oxygen. At this temperature, silane and oxygen chemically reacts forming silicon dioxide as a by-product. An optional densification of LTO can be performed after the deposition. The contact cut lithography opens windows where aluminum

has to make contact with the underlying material. The overlay for contact cut, as in all previous lithography steps, is critical. Misalignment could lead to open circuits.

The wafers are then dry etched in the DryTek Quad. There currently exists a process for LTO etch, which is used in the Factory CMOS process. The gases used are CHF_3 and SF_6 . A little over-etch is recommended to guarantee that the LTO has been etched all the way down.

4.2.14 Metallization

Aluminum is still the choice of metal in the IC industry due to its process simplicity and fairly low sheet resistance (copper being the lower, hence becoming more popular in the recent years). This CMOS process utilizes aluminum due to the presence of a robust metallization process, migrated from the current CMOS PW-3 process.

Aluminum is DC sputtered in the CVC 601 Sputterer. The sputter pressure is 5 mTorr and the gas used is argon. The target material is an aluminum/silicon alloy (99% Al, and 1% Si). The presence of silicon greatly reduces

'spiking' of aluminum, leading to shorting within the devices. The pre-sputtering for 10 minutes will remove any contaminants present on the target surface. The target thickness for aluminum is 5000Å. The sputter time needs to be determined from the SPC charts or the log sheets.

The final lithography step defines the metal contacts. While coating Photoresist, it is not necessary to use HMDS, as it has good adhesion to metal surfaces. Better resolution can be attained if an Anti-Reflective Coating (ARC) is used. The metal mask defines region where aluminum will be etched. The exposure time needs to be reduced to compensate for the highly reflective surface.

As of now, there is no dry-etch process for aluminum here at RIT, but there exists a possibility in the near future. At that point, plasma etching should be used for etching the aluminum. Currently, wet etching of aluminum using a mixture of phosphoric acid and nitric acid at 50-55°C, is used. It will be undesirable for sub-micron features due to its isotropic etching.

After the wafers are thoroughly rinsed, they go through the final thermal step. Sintering is performed at

400°C in forming gas (H_2N_2) for 20 minutes. This ensures a very good contact to the underlying material, by chemically removing the native oxide found at the interface of aluminum and silicon. The final crosssection of the device is shown below.

The final step called Sintering will reduce the interface charges and contact resistance. This is performed in Bruce Furnace Tube 1 at 400°C in forming gas (H_2N_2) for 20 minutes.

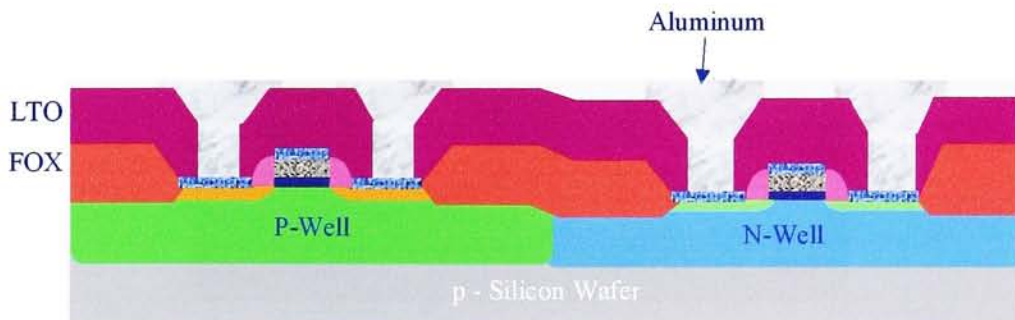


Fig 4.19 Crosssection of the Finished Product

5. PROCESS & DEVICE SIMULATION

MicroTec by Siborg Systems was the software used to simulate the process as well as extract device characteristics. MicroTec uses the diffusion-drift model for simulation of the thermal and implant steps. It is optimized to run on a 386-based machine running Microsoft Windows 3.1/95/98/NT/2000. The following window will appear when the program is launched.

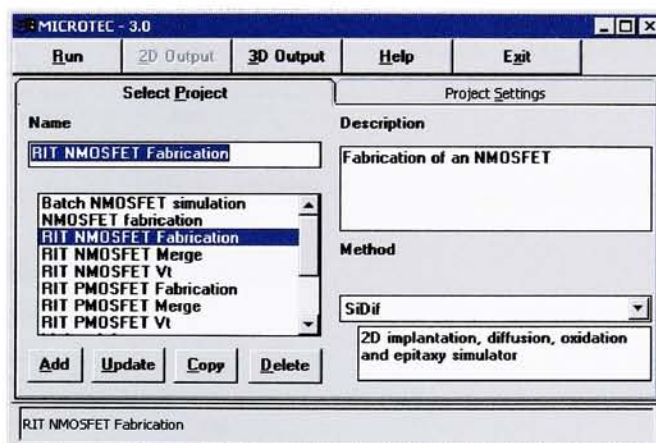
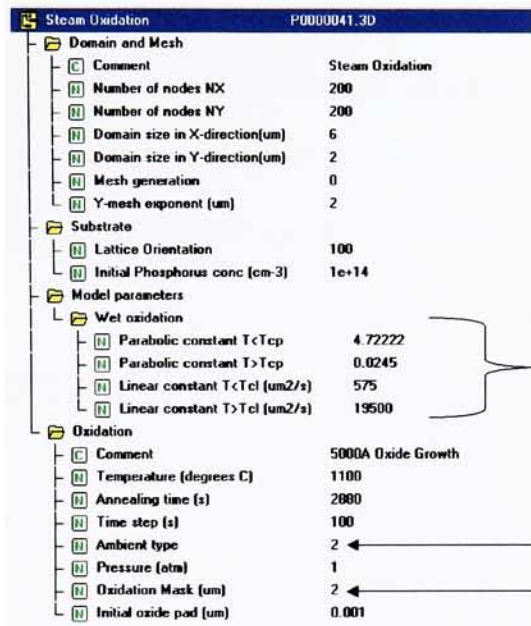


Fig 5.1 MicroTec's user interface

Examples of the input deck for MicroTec are shown in figures 5.2 and 5.3.

Silvaco's SUPREM3 simulation package was also used to simulate certain diffusion and oxide growths. Unlike MicroTec, the Silvaco package can perform multiple

oxidation steps and etches, and therefore is considered as an advanced simulator.



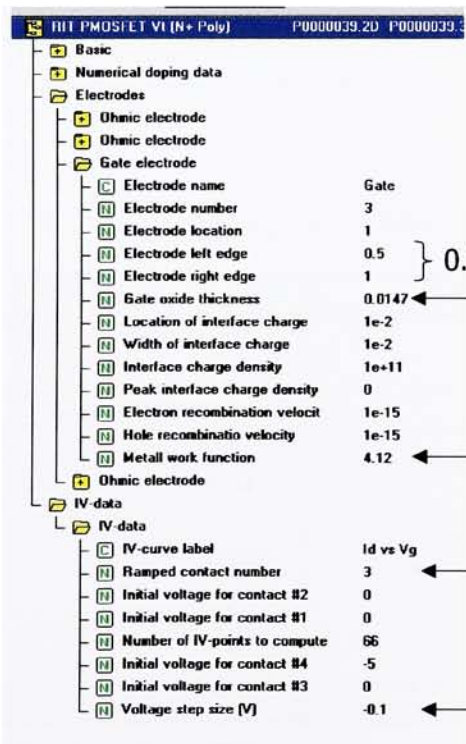
Parameter	Value
Comment	Steam Oxidation
Number of nodes NX	200
Number of nodes NY	200
Domain size in X-direction(um)	6
Domain size in Y-direction(um)	2
Mesh generation	0
Y-mesh exponent (um)	2
Lattice Orientation	100
Initial Phosphorus conc [cm-3]	1e+14
Parabolic constant T<T _{cp}	4.72222
Parabolic constant T>T _{cp}	0.0245
Linear constant T<T _{cl} (um ² /s)	575
Linear constant T>T _{cl} (um ² /s)	19500
Comment	5000A Oxide Growth
Temperature (degrees C)	1100
Annealing time (s)	2880
Time step (s)	100
Ambient type	2
Pressure (atm)	1
Oxidation Mask (um)	2
Initial oxide pad (um)	0.001

These values have been calculated to match the oxide growth chart. This is for steam oxidation only

Ambient 1=Dry, 2=Wet

Region of Oxide Growth

Fig 5.2 Input steps for steam oxidation



Parameter	Value
Electrode name	Gate
Electrode number	3
Electrode location	1
Electrode left edge	0.5
Electrode right edge	1
Gate oxide thickness	0.0147
Location of interface charge	1e-2
Width of interface charge	1e-2
Interface charge density	1e+11
Peak interface charge density	0
Electron recombination velocity	1e-15
Hole recombination velocity	1e-15
Metall work function	4.12
IV-curve label	Id vs Vg
Ramped contact number	3
Initial voltage for contact #2	0
Initial voltage for contact #1	0
Number of IV-points to compute	66
Initial voltage for contact #4	-5
Initial voltage for contact #3	0
Voltage step size [V]	-0.1

0.5μm Gate Length

Gate oxide thickness in microns

N+ poly work Function

Gate electrode ramped

Initial gate potential

Fig 5.3 Device simulation input file for a PMOSFET

5.1 Simulation Results and Discussion

The NMOS and the PMOS devices were simulated separately. The results were charted and verified with the target values. Charts 5.4, 5.5 and table 5.1 summarize the results generated by MicroTec.

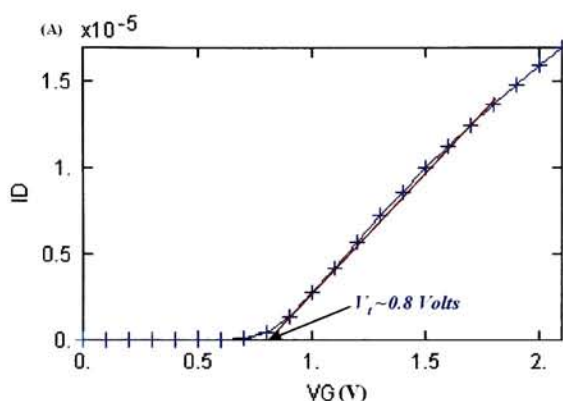


Fig 5.4 V_t extrapolation graph for the NMOS

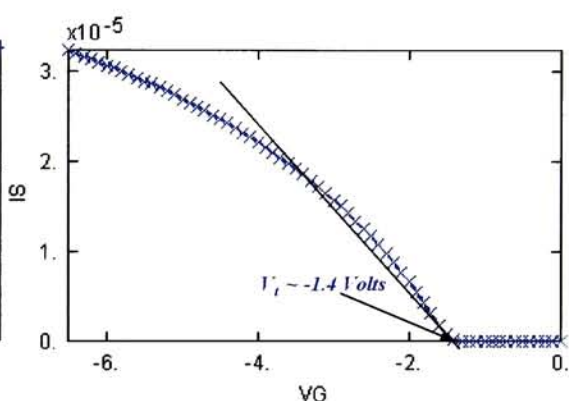


Fig 5.5 PMOS V_t extrapolation graph

Table 5.1 Summary of simulation results for 0.5 μ m devices

Parameter	NMOSFET	PMOSFET (n+ poly)
Threshold Voltage (V)	0.8	-1.4
L_{eff} (μ m)	0.4	0.41
Early Voltage (V)	16	6
Subthreshold swing (mV/decade)	90	100
Off-state current (A)	$\sim 10^{-14}$	$\sim 10^{-17}$
Max Drive Current (mA) *	0.5	-
Max Vdd (V) *	8.4	-

* Before breakdown

The NMOS simulation verified that this process is capable of attaining the target, which was 0.8 volts. The PMOS device displayed a higher threshold voltage, which is due to the n+ polysilicon gate. The solution to this is to use p+ polysilicon, which can easily lower the threshold voltage. The IC Industry implements dual work functions for better control of the device characteristics.

The Early voltage was measured by extrapolating the curve in the saturation region until it intersected the x-axis. Decreasing the doping will reduce the Early voltage, but it will also increase the threshold voltage. The trade-off will be poor subthreshold characteristics, but the FET will be a good current source.

The correlation between the calculated values from Section 2 to the simulated values for the 0.5 μ m transistor is shown Table 5.2. Please refer to the Simulation section in Appendix 1 for the detailed charts on how the values were extracted.

Table 5.2 Comparison table for NMOS

Parameter	Calculated	Simulated	Comments
Threshold Voltage (V)	0.83	0.8	-
Early Voltage (V)	14.96	16	Better
Subthreshold swing (mV/decade)	93	90	Better
Off-state current (A)	$\sim 10^{-13}$	$\sim 10^{-14}$	Better
Max Drive Current (mA)	0.69	0.5	Acceptable

Hand-calculations were not performed for the PFET devices, hence omitted from the table above. Almost in all cases, the simulated transistor is better than the 'theoretical' one. The simulated transistor showed better subthreshold swing (S). The off-state current, ideally, should be as small as possible. This determines whether the transistor can be used in logic circuits. If there is any leakage current, the transistor will never be off, and therefore will consume power.

Figures 5.6 and 5.7 shows the family of curves for the NMOS and the PMOS transistors, respectively. For both devices, the gate voltage increased by 0.25 volts increments, while varying the drain voltage from 0 to 5 volts. The values for the source current versus drain potential were used to plot the chart for the PMOS

transistor, hence the vertically flipped chart. Both devices clearly display channel length modulation, depicted by the positive slope of the lines in the saturation region as the drain voltage is increased. The slope is a combination of other effects such as drain induced barrier lowering (DIBL)^[1], and therefore is not wholly due to the channel length modulation. In simple terms, DIBL is the increase in drain current as the drain voltage is increased. This is a well-explained phenomenon and is clearly shown in figures 5.8 and 5.9 (junction leakage is ignored) for both devices.

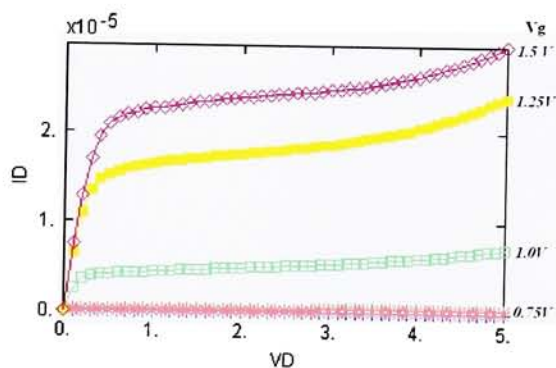


Fig 5.6 NMOS Family of curves

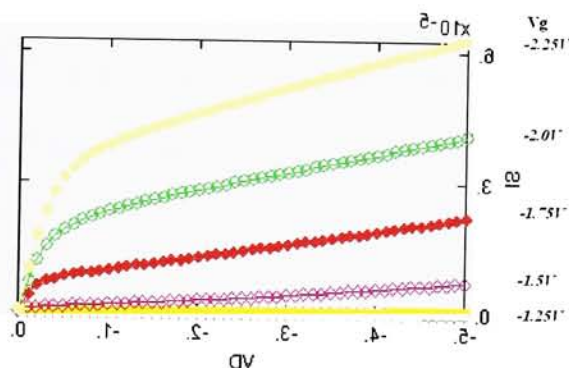


Fig 5.7 PMOS family of curves

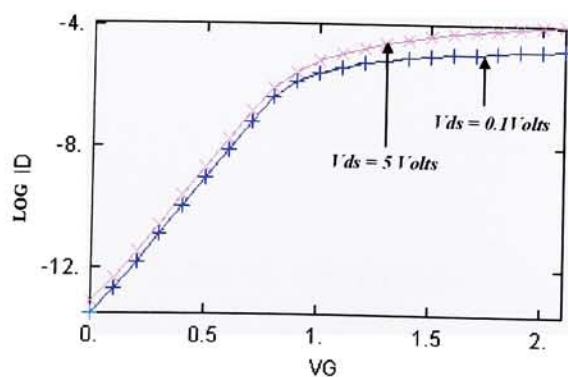


Fig 5.8 Log Id versus gate voltage for the NMOS

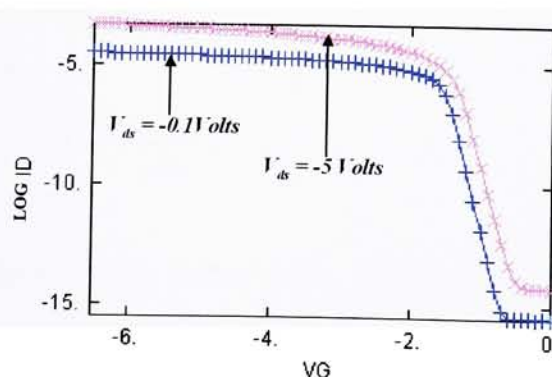


Fig 5.9 Log Id versus gate voltage for the PMOS

Using p+ poly for the PMOS transistor has its advantages, the main one being the control of the threshold voltage. In-situ doping is the most desired method of depositing polysilicon with different work functions. The conventional method of doping by spin-on-dopant or the ion implanter adds complexity and multiple mask levels to the process. P+ poly increases the metal work function, Φ_{ms} , by 1.12eV, resulting in a lower threshold voltage. The higher metal work function also improves subthreshold characteristics of the device. Using MicroTec, this same process with p+ poly was simulated. The chart below clearly shows the threshold voltage as -0.88 volts, which is significantly better than the PMOS device with n+ polysilicon. The target for the PMOS transistor is -0.8 volts.

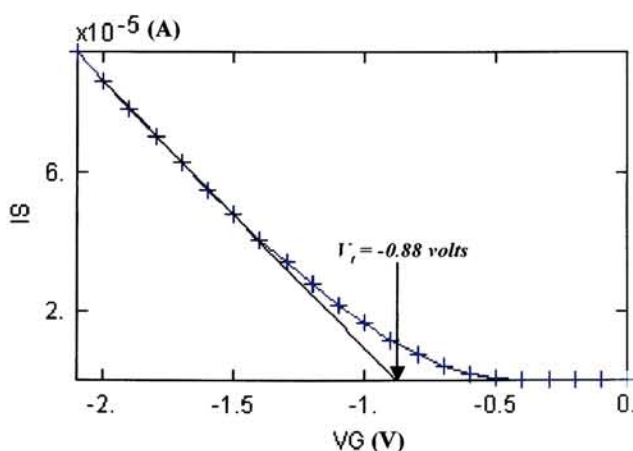


Fig 5.10 V_t extrapolation chart for PMOS with p+ poly

6. CONCLUSIONS AND FUTURE WORK

Creation of the sub-micron process for RIT involves the development of various steps. Most of the current steps used in the P-well CMOS, will require modification and optimization, as any process migration would. An easier way to approach this would be to employ Design of Experiments (DOE). The ultimate goal here is to use the sub-micron CMOS Process as a teaching tool. Some of the recent studies have been successful in characterizing certain dry-etching processes, which needs to be verified before students in the Factory class can use it.

Simulation of the process revealed that the new process is capable of going down to $0.5\mu\text{m}$ channel lengths. The use n^+ polysilicon retards the threshold voltage for the PMOS devices. However, the NMOS devices display great potential as a very good current source. The threshold voltage, both calculated and simulated, for the $0.5\mu\text{m}$ device was found to be 0.8 volts, which was the target V_t also.

Devices with channel lengths as small as $1\mu\text{m}$ are now being fabricated using this process. These wafers will be

on the test bench by the end of November 2000, barring unforeseen circumstances.

Future predictions for RIT's CMOS technology, as predicted by the author, are as follows:

Table 6.1 RIT's CMOS road-map

Name	Advancements
RIT's Advanced CMOS	STI, W Plugs, CMP
MEMS + CMOS	On board CMOS+Sensors
'Metal-less' CMOS	Silicon based Optoelectronics, III-V Semi + Silicon CMOS, retro-grade wells

7. REFERENCES

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2. J.R. Brews, W. Fitchner, E.H. Nicollian, "Generalised Guide for MOSFET Miniaturization," IEEE Electron Device Letters, Vol. EDL-1, No.1, pp. 2-4, January 1980
3. G.E. Rittenhouse, W.M. Mansfield, A. Kornbilt, "Sub-0.1 μ m NMOS Transistors Fabricated Using Laser-Plasma Point Source X-Ray Lithography," IEEE Electron Device Letters, Vol. 16, No. 7, July 1995
4. S. Bhaskaran, "Formation of Sidewall Spacers and Titanium Salicide for RIT's Sub-micron CMOS," 14th Annual Microelectronic Engineering Conference, Rochester, NY (1996)
5. Lynn F Fuller, "CMOS PW-3 MESA Process Details - Lab Notes," Rochester Institute of Technology, Rochester, NY (1999)
6. Lynn F Fuller, "RIT P-Well-3 CMOS Process Crosssections - Lab Notes," Rochester Institute of Technology, Rochester, NY (1999)
7. Ton Mouthaan, Semiconductor Devices Explained Using Active Simulation," John Wiley & Sons Ltd., New York, NY, pp. 256-293 (1999)

8. Yannis P. Tsividis, "Operation and Modeling of The MOS Transistor," McGraw-Hill Inc., New York, NY

9. Dieter k. Schroder, "Semiconductor Material and Device Characterization," Wiley-Interscience, New York, NY, pp. 394-396 (1998)

APPENDIX A - DETAILED PROCESS FLOW

Scribe

- Boron doped P-type wafer
 - Four Point Probe to calculate ρ

$$\rho = \frac{\Pi}{\ln 2} \times \text{Wafer Thickness} \times \frac{V}{I}$$

- Scribe wafers D1-D3
- RCA Clean
 - Equipment: RCA Wet Bench
 - HPM (10 min), HF (1min), APM (10 mins), HF (1min), with 5min DI Rinse in between each bath.



Pad Oxide Growth

- Begin LOCOS process
- Grow 500A Pad Oxide
 - Equipment: Bruce Furnace
 - Recipe: 250
 - Ambient: Dry O₂, Temperature: 1000°C, Time: 48 minutes



Deposit Nitride

- Deposit 1500A Nitride
 - Equipment: ASM 6” CVD
 - Use recipe for Factory nitride deposition, include a control wafer
 - Measure thickness on control wafer

Nitride
Pad Oxide



Ist Level Lithography

- P-Well lithography
 - Equipment: SSI Track, Canon I-line
 - 1st Level mask (N-Well Mask)
 - Develop on SSI Track



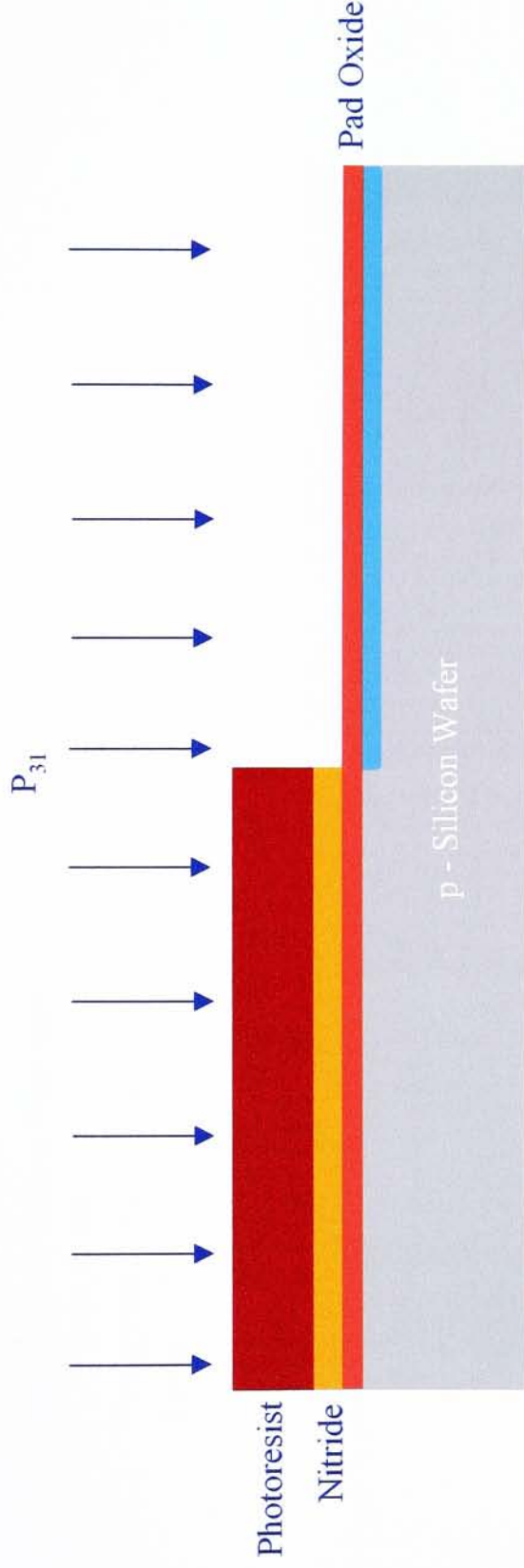
Nitride Etch

- Etch Nitride
 - Equipment: DryTek Quad
 - Gases: SF_6 , 250mTorr



N-Well Ion Implant

- Implant P_{31}
 - Equipment: Varian 120 Ion Implanter
 - Species= P_{31} , Dose = 2×10^{12} ions/cm² (peak conc. = 1.5×10^{17} cm⁻³)
 - Energy = 150 KeV



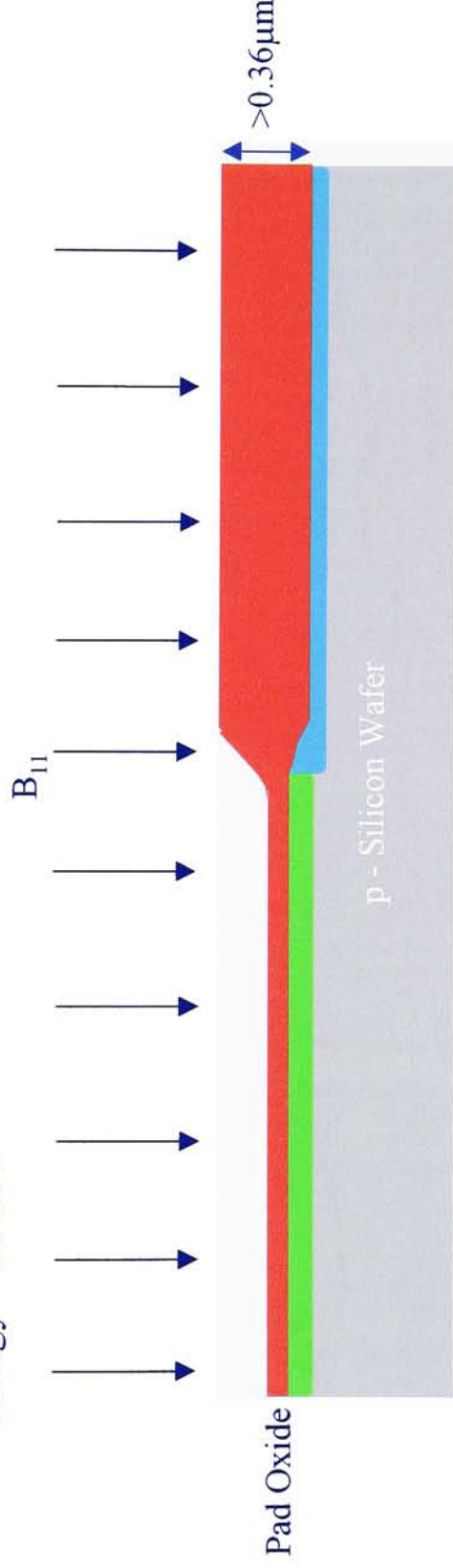
N-Well Oxidation

- Plasma strip the Photoresist
 - Equipment: DryTek quad or Branson Asher
- RCA clean
 - Equipment: RCA Wet Bench
- Grow 5000 Å oxide
 - Equipment: Bruce Furnace
 - Recipe 350
 - Pyrogenic Steam ambient
 - Temp = 1100°C, time = 48 minutes



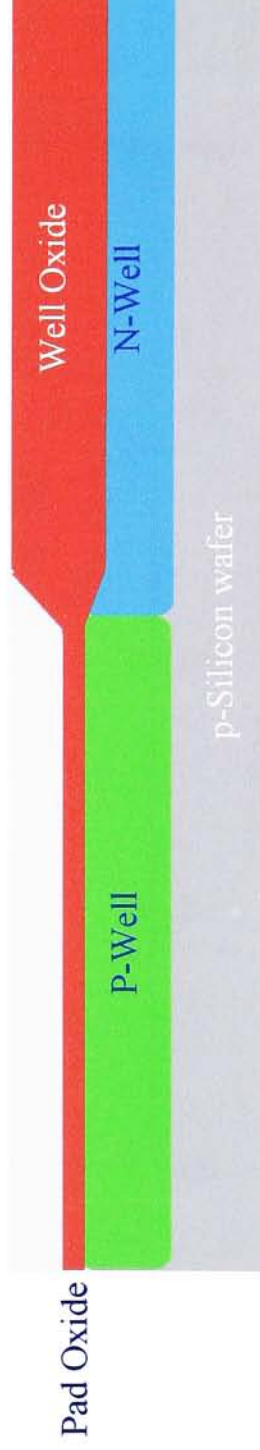
P-Well Implant

- Complete etch of Nitride layer
 - Equipment: DryTek Quad
- Implant B_{11}
 - Equipment: Varian 120 Ion Implanter
 - Species = B_{11} , Dose = 2.5×10^{13} ions/cm²
 - results in surface concentration of $\sim 2.5 \times 10^{17}$ cm⁻³
 - Energy = 50 keV



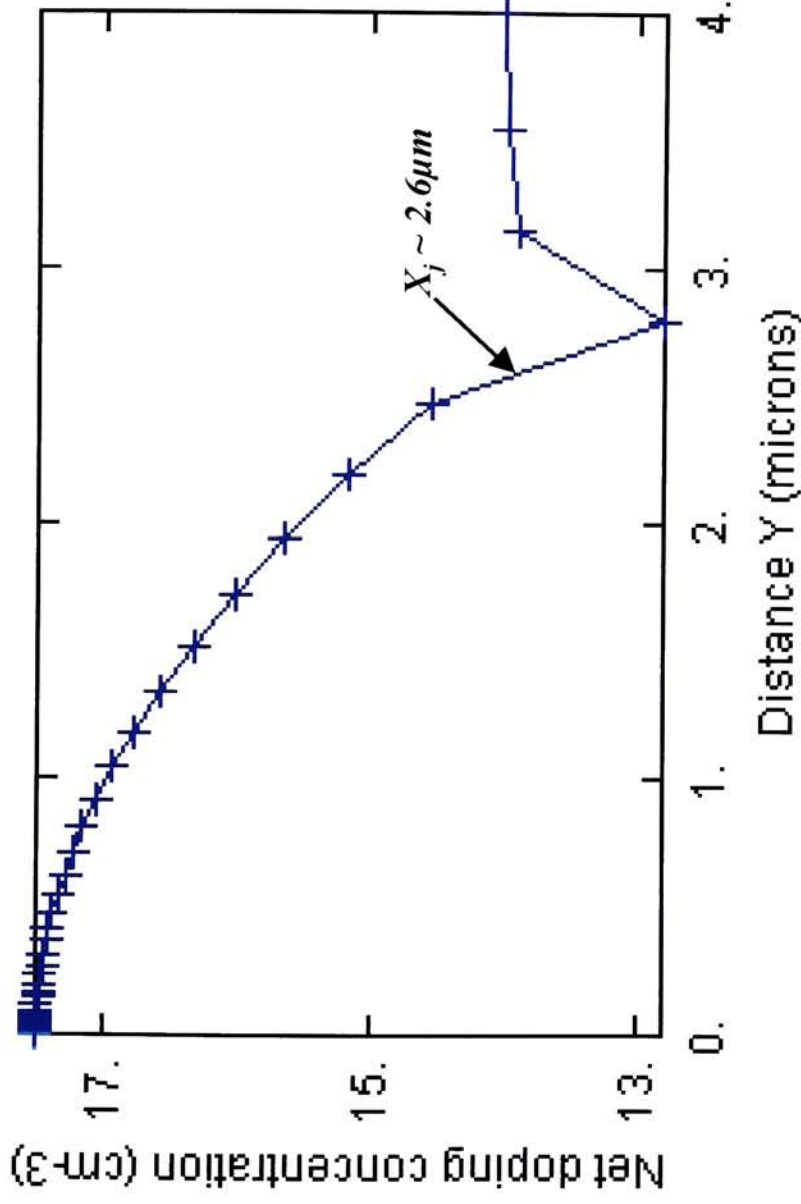
P-Well Drive-in

- Well Drive-in
 - Equipment: Bruce Furnace Tube 01
 - Recipe: Create a new one
 - Soak in N_2 for 210 min, $T = 1100^\circ C$
- Measure junction depth
 - Equipment: Groove and Stain Lapper
 - Approximate depth for P-Well = $2.5 \pm 0.5 \mu m$
 - Approximate Depth for N-Well = $3.2 \pm 0.5 \mu m$



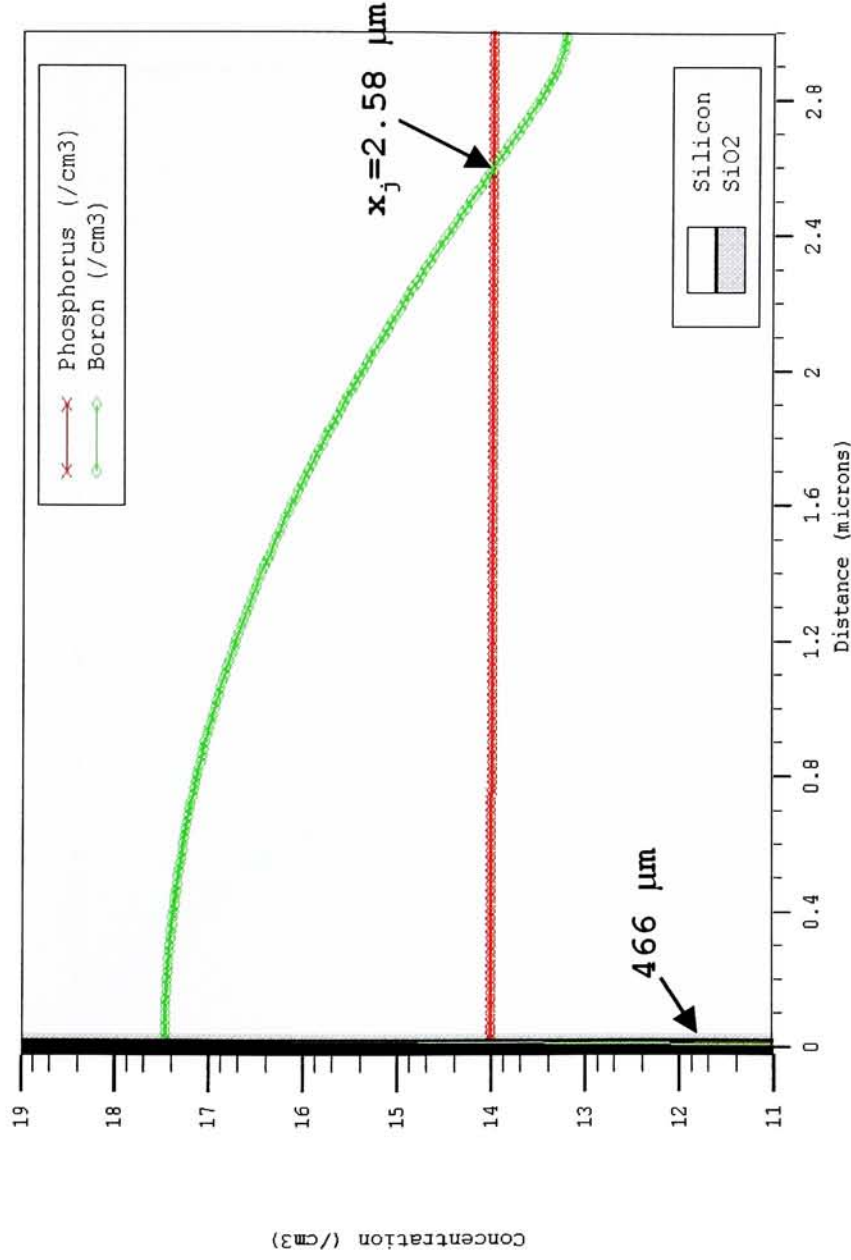
After Drive-in (P-Well)

- MicroTec Simulation Output after drive-in (Net Doping Profiles)



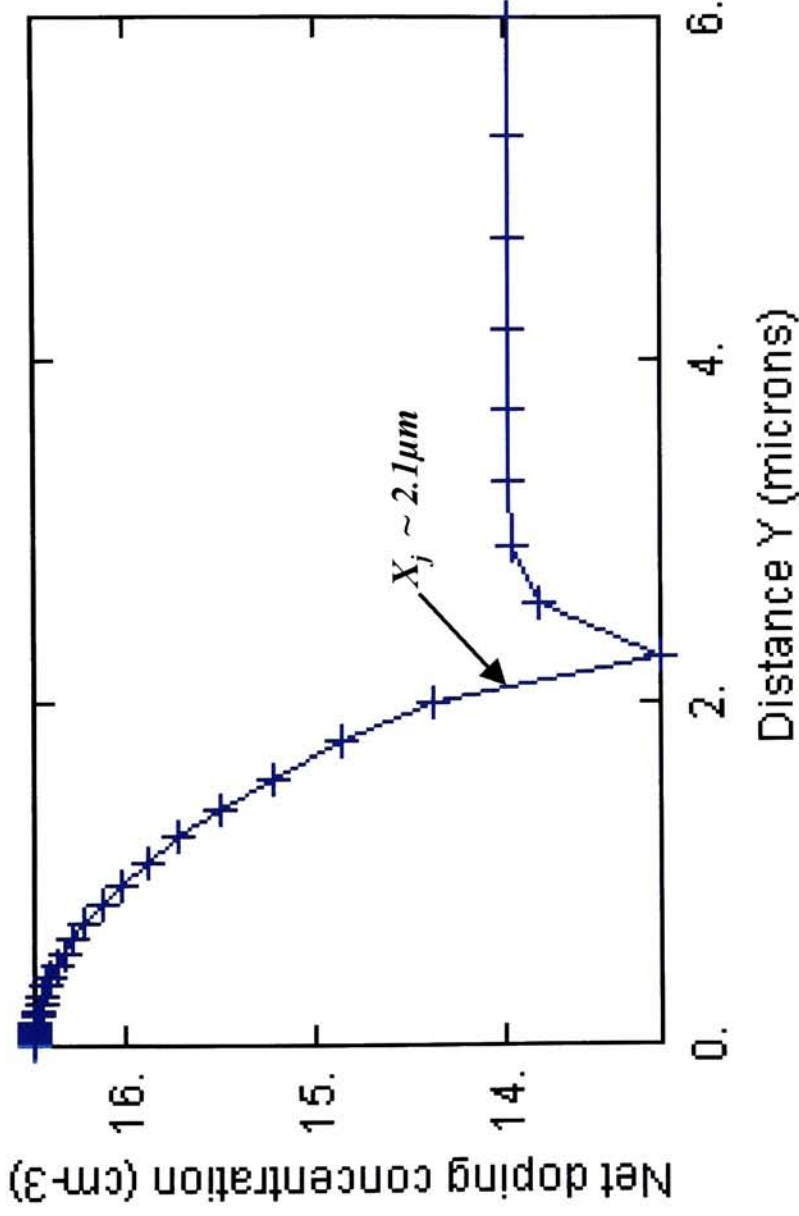
After Drive-in (P-Well)

- SILVACO Simulation Output after drive-in (Net Doping Profiles)



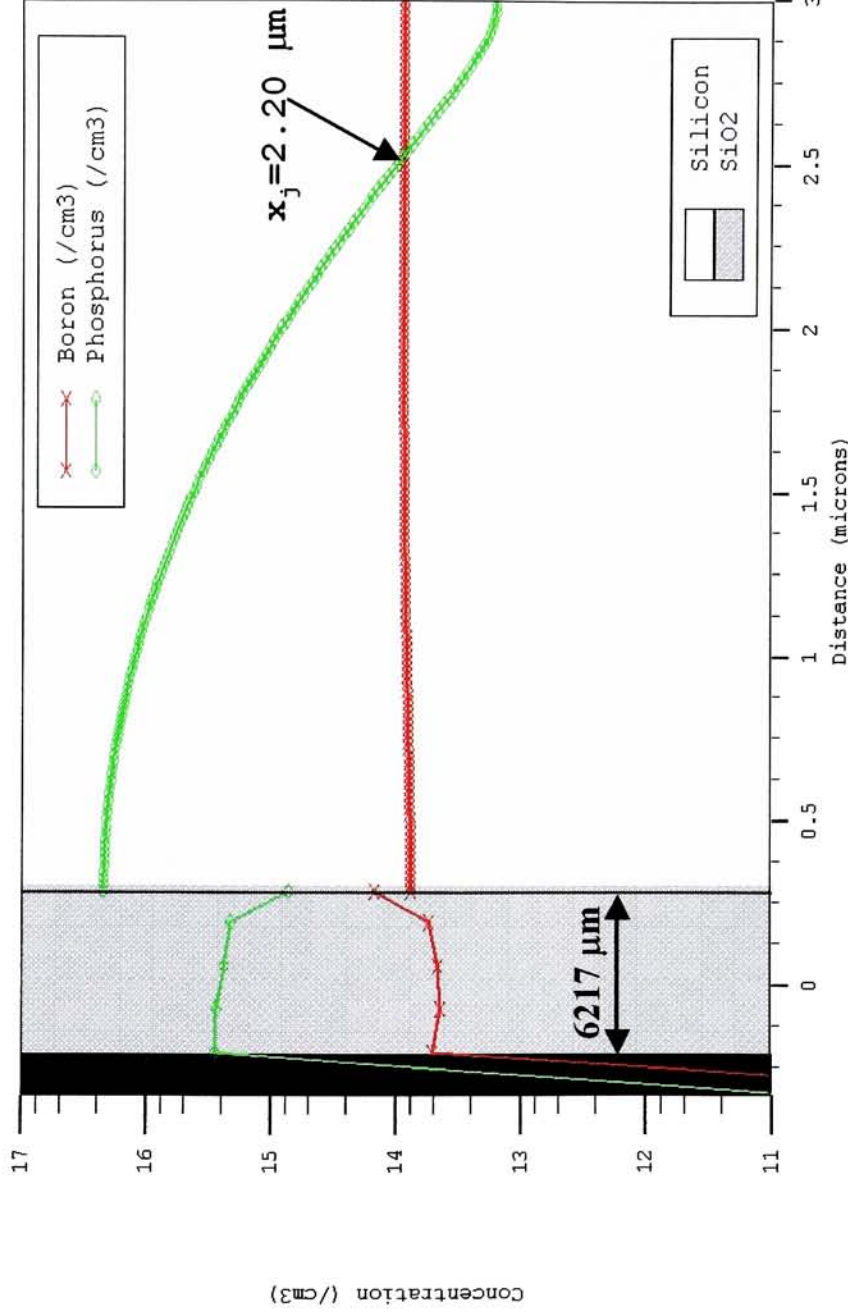
After Drive-in (N-Well)

- MicroTec Simulation Output after drive-in (Net Doping Profiles)



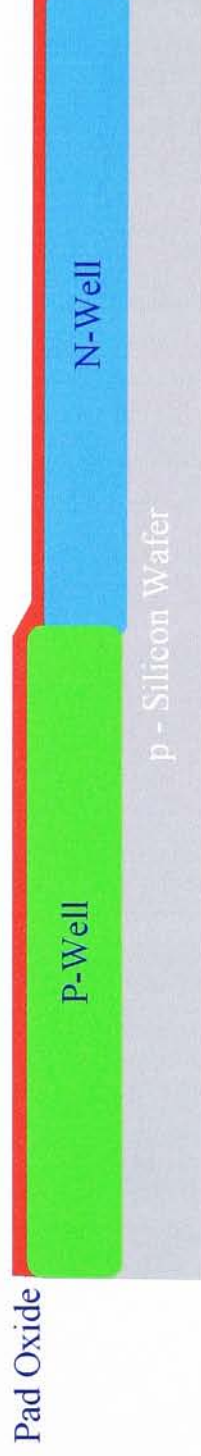
After Drive-in (N-Well)

- Silvaco Simulation Output after drive-in (Net Doping Profiles)



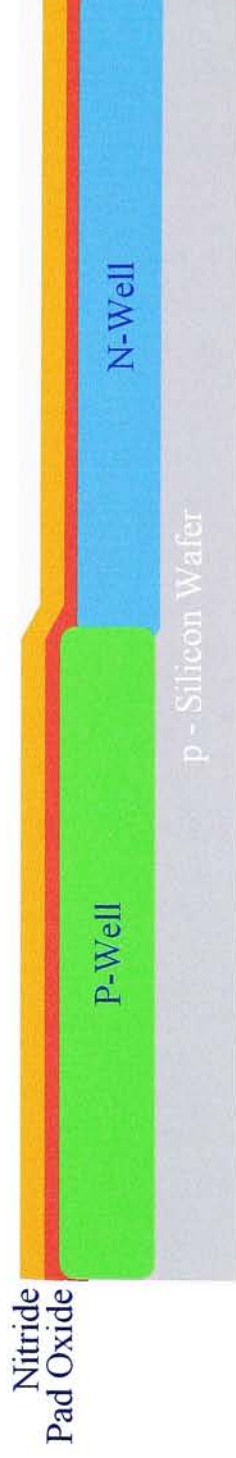
Grow Pad-Ox

- Etch thick oxide, 10 min in BOE
 - Equipment: Wet BOE Bench
- RCA Clean
 - Equipment: RCA Wet Bench
- Grow 500Å Pad Oxide (Beginning of second LOCOS)
 - Equipment: Bruce Furnace
 - Recipe: 250
 - Ambient: Dry O₂, Temperature: 1000°C, Time: 48 minutes



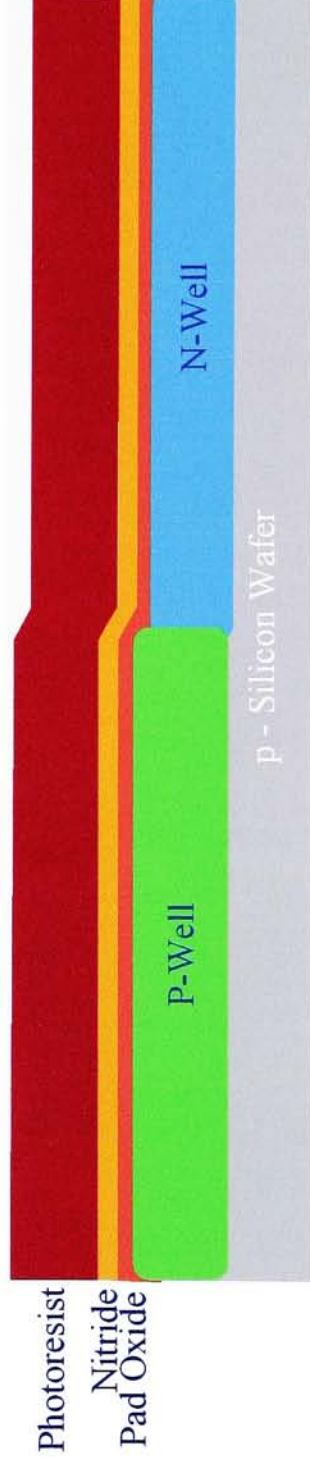
Deposit Nitride

- Deposit 1500A Nitride
 - Equipment: ASM 6” CVD Furnace
 - Gases: DCS + NH₃
 - Time: Calculate time from Control Charts



Active Lithography

- Coat Photoresist
 - Equipment: SSI Track
 - Use factory standard recipe



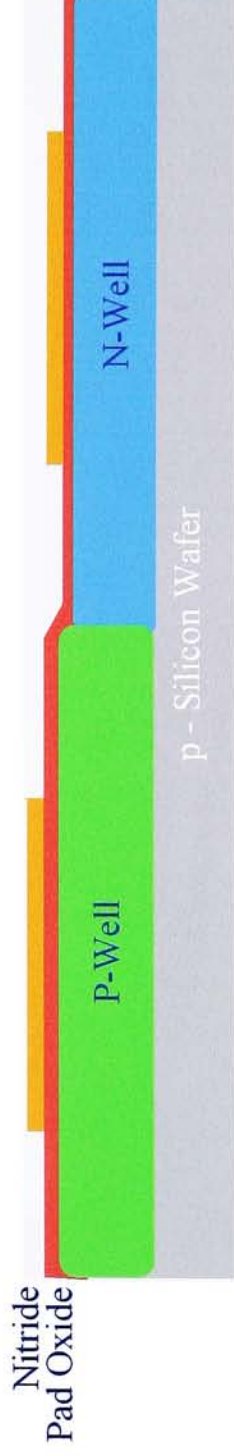
Active Lithography Contd.

- Expose using Level 2 mask
 - Equipment: Canon i-line Stepper
 - 2nd Level mask (Active Mask)
 - Develop on SSI Track
- Etch Nitride
 - Equipment: DryTek Quad
 - Gases: SF_6 , 250mTorr



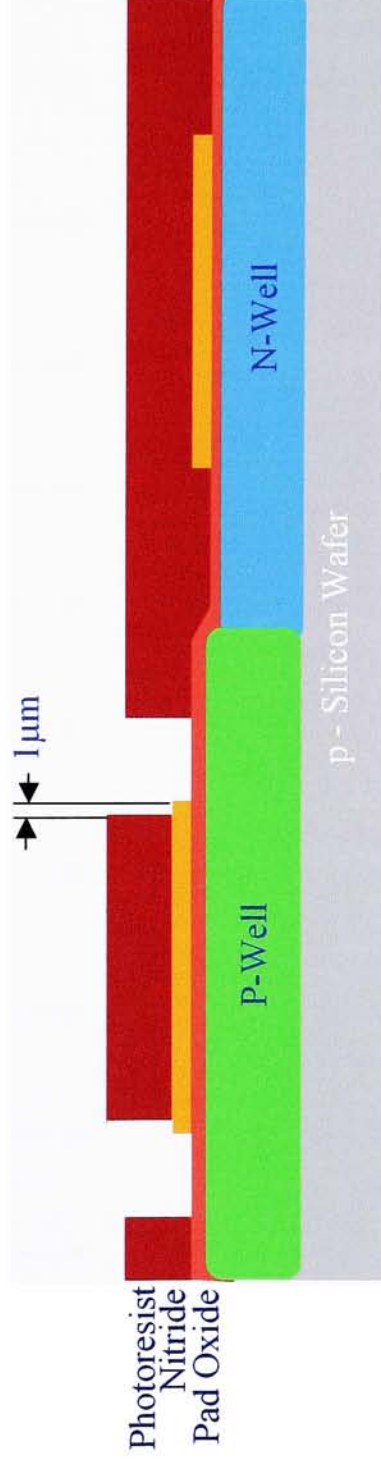
Strip Resist

- Plasma strip resist
 - Equipment: DryTek Quad (Chamber 3) or GaSonics Asher
 - Time: TBA



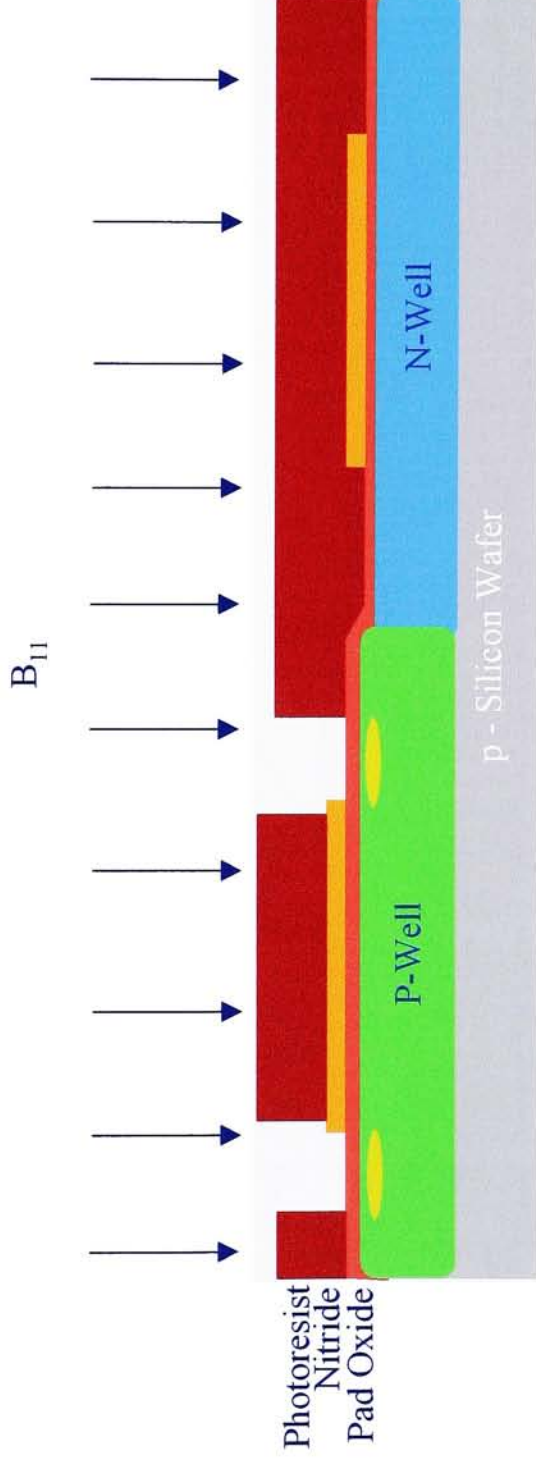
Field VT Lithography

- Coat Photoresist on Trac
 - Equipment: SSI Track
 - Use factory standard recipe
- Level 3 Photolithography
 - Equipment: Canon i-line Stepper
 - 3rd Level mask (Field V_t ; (inverse n-well mask ored with active shrunk ($1 \mu\text{m}$)))
 - Develop on SSI Track



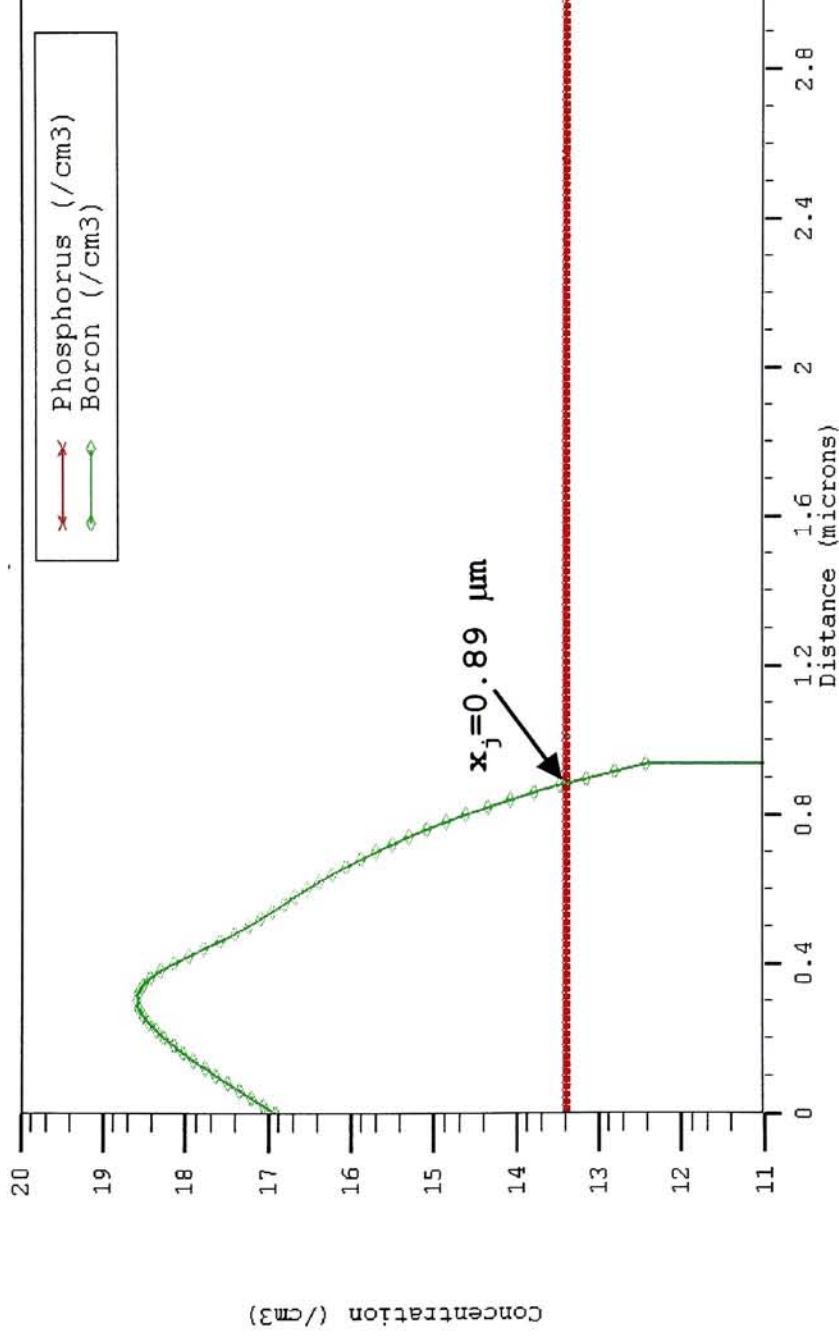
Channel Stop Implant

- Channel Stop Implant
 - Equipment: Varian 120 Ion Implanter
 - Species = B_{11} , Dose = 8×10^{13} ions/cm²
 - Energy = 100 keV



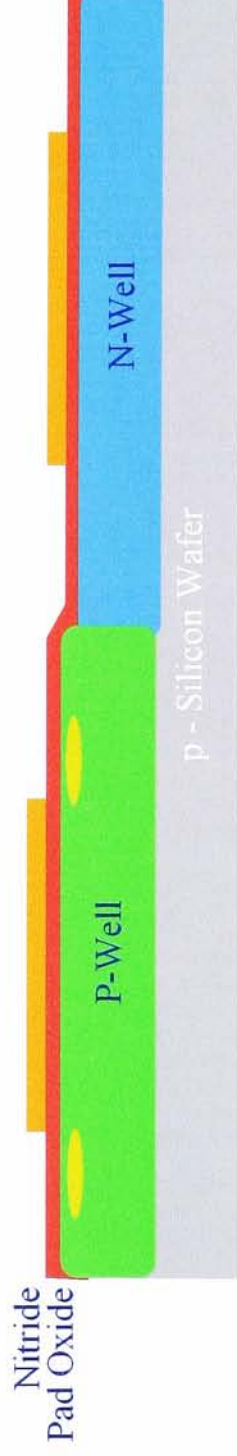
Channel Stop Implant

- Junction depth from simulation (SILVACO)



Strip Photoresist

- Plasma strip photoresist
 - Equipment: DryTek Quad (Chamber 3) or GaSonics Asher
 - Time: TBA

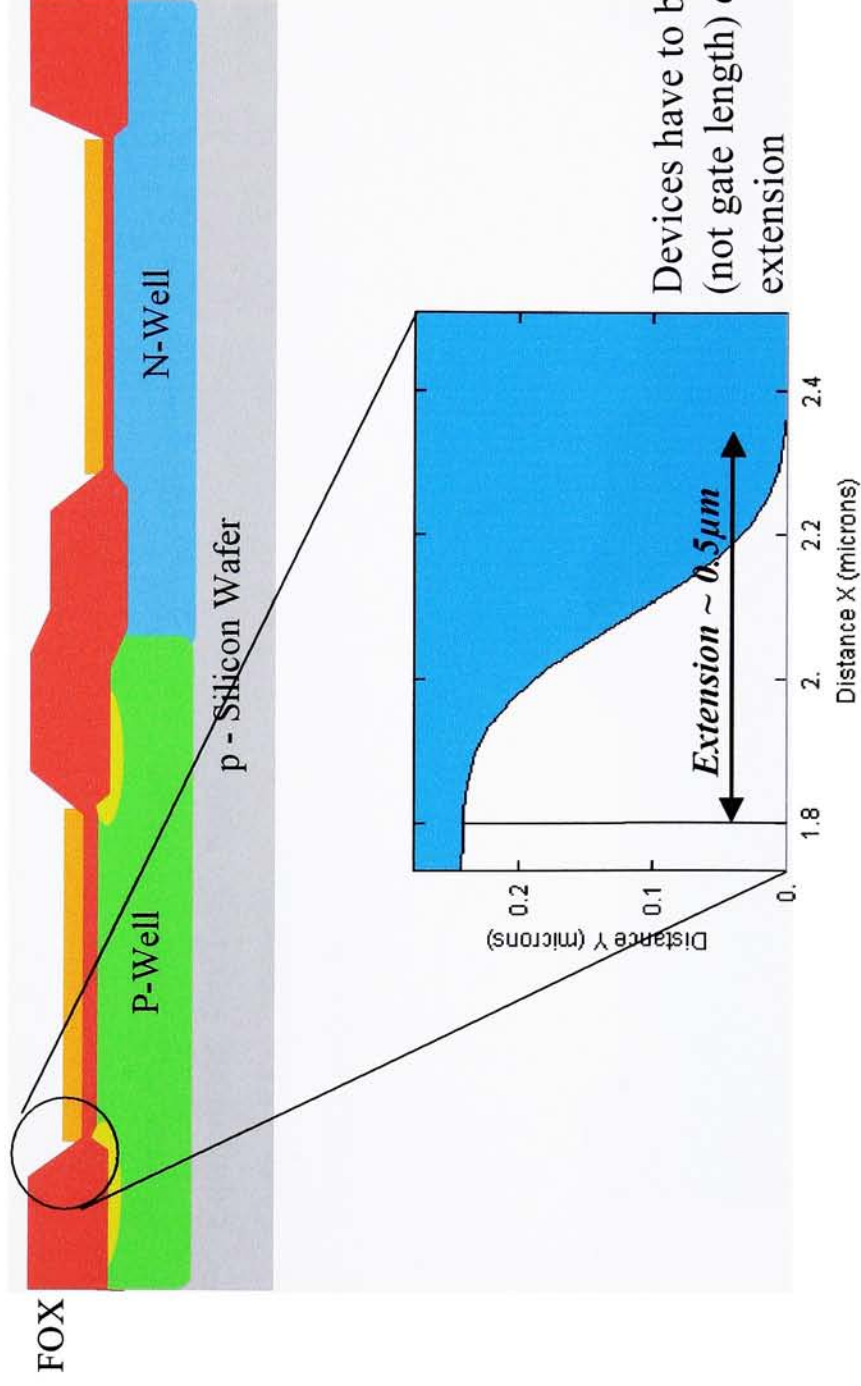


FOX Growth

- RCA Clean
 - Megasonic cleaning recommended
- FOX growth
 - Equipment: Bruce Furnace
 - Recipe: Create a new process
 - Desired thickness = 6500Å
 - Ambient = Steam, Temp = 1100°C, time = 60 minutes



FOX Growth – ‘Bird’s Beak’ Simulation



Remove Silicon Nitride

- Etch Silicon Nitride
 - Plasma etch Silicon Nitride
 - Equipment: DryTeK Quad
 - Gases: SF6, 250mTorr
 - **Process under development**



Etch Pad Oxide

- Etch pad oxide in BOE
 - Equipment: Wet BOE bench
 - Time: 60 seconds
- RCA Clean



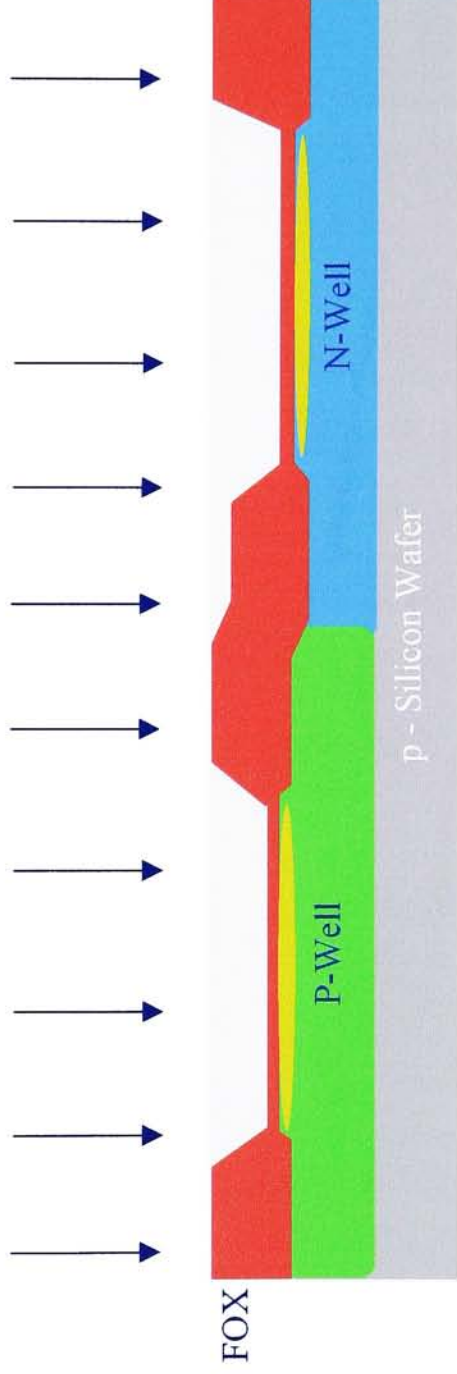
Kooi Oxide Growth

- Grow 1000Å Kooi Oxide
 - Equipment: Bruce Furnace
 - Recipe: 310
 - Ambient = Steam, Temp = 900°C, time = 45 minutes



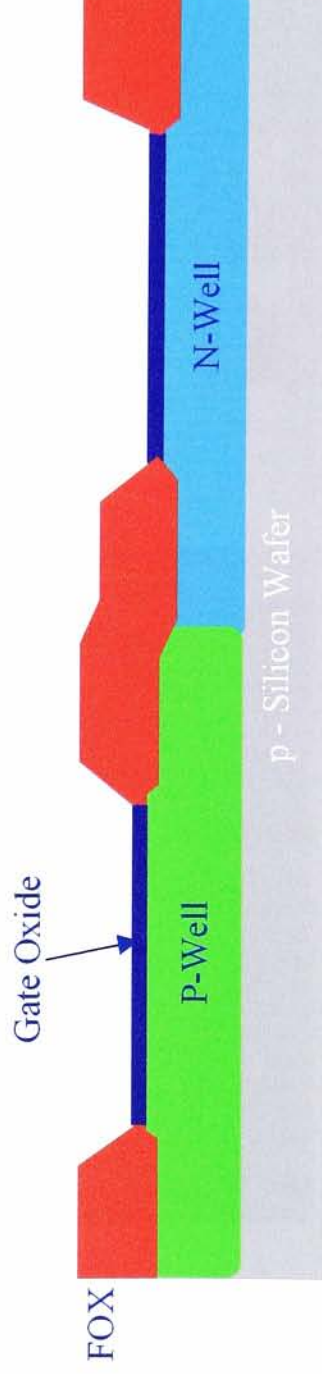
Blanket V_t Adjust Implant - Optional

- Implant B_{11}
 - Equipment: Varian 120 Ion Implanter
 - Species = B_{11} , Dose = 1×10^{12} ions/cm²
 - Energy = 40 keV
 - Peak of implant to be below Kooi oxide



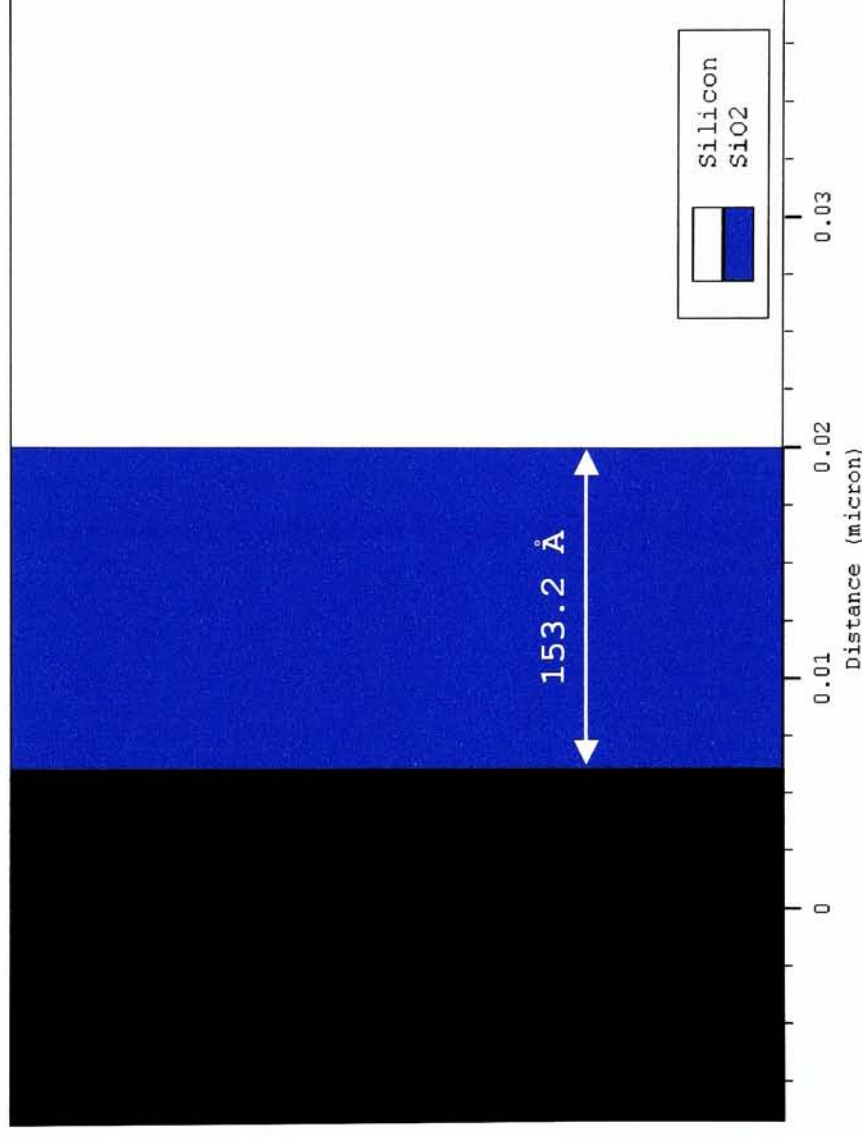
Gate-Ox Growth

- Etch Kool Oxide
 - Equipment: Wet BOE Bench
 - Time: 90 Seconds
- RCA Clean
- Grow Gate Oxide
 - Equipment: Bruce Furnace
 - Recipe: Create new Recipe
 - Ambient = Dry O₂, Temp = 900°C, time = 40 minutes



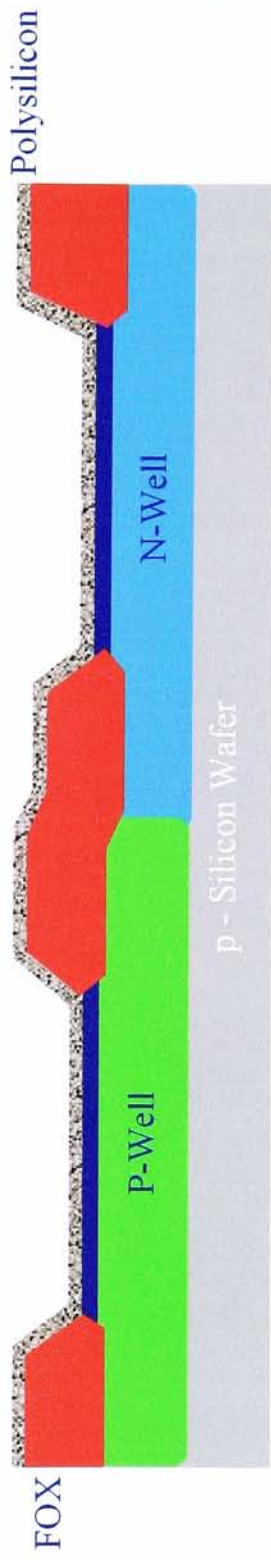
Gate-Ox Growth Simulation

- Oxide growth simulated using SILVACO



Polysilicon Deposition

- Deposit Polysilicon
 - Equipment: ASM CVD
 - Gas: Silane
 - Thickness = 4200Å (Use the log sheets to calculate deposition time)
- Dope Poly n-type using Spin-on-dopant
 - Follow the processing procedure for N-250 Spin-on-Dopant
 - Spin at 3000 RPM for 20 seconds
 - Prebake N-250 at 200°C for 15 min in the Blue-M Oven
 - Create a Bruce Furnace recipe similar to Recipe 120
 - Soak at 1000°C, 7.5 minutes, nitrogen ambient



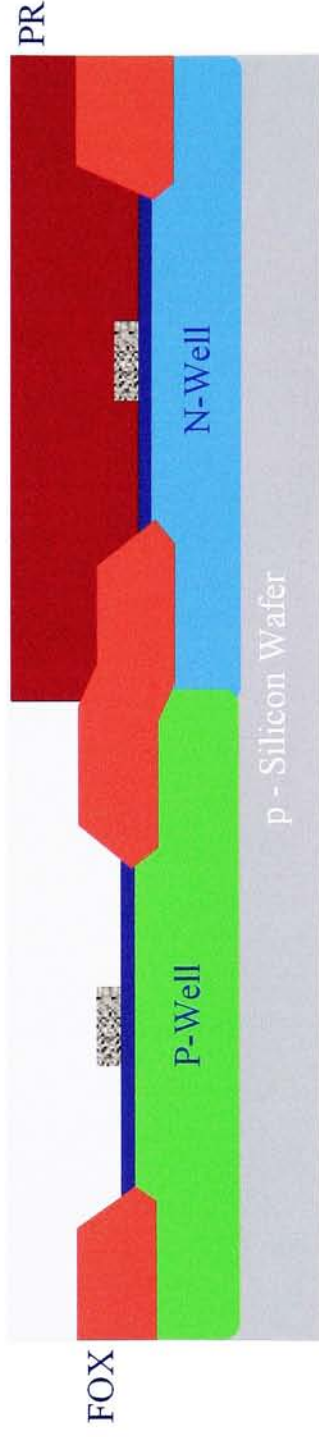
Gate Lithography

- Gate Lithography
- Poly Etch
 - 1 minute Wet-etch in BOE to remove Phospho-Silicate Glass
 - Dry etch poly
 - Equipment: DryTek Quad
 - Gase: $\text{SF}_6 + \text{O}_2$
 - Time: To be determined from SPC Charts



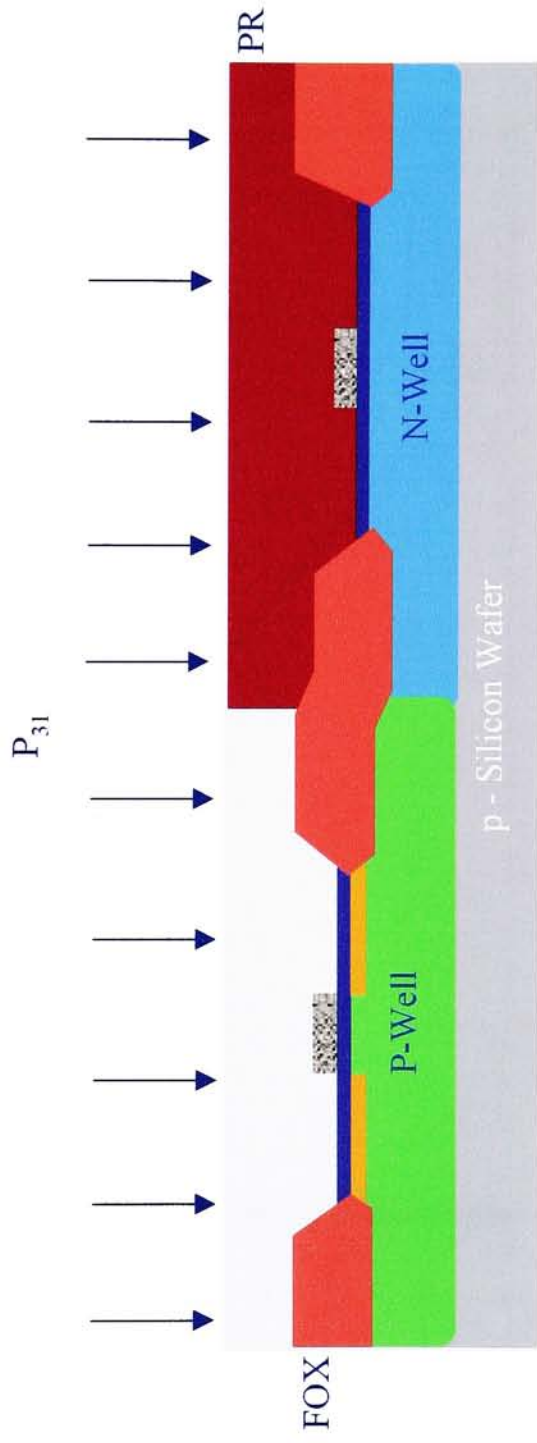
N- S/D Lithography

- Expose wafers using inverse of N-well Mask



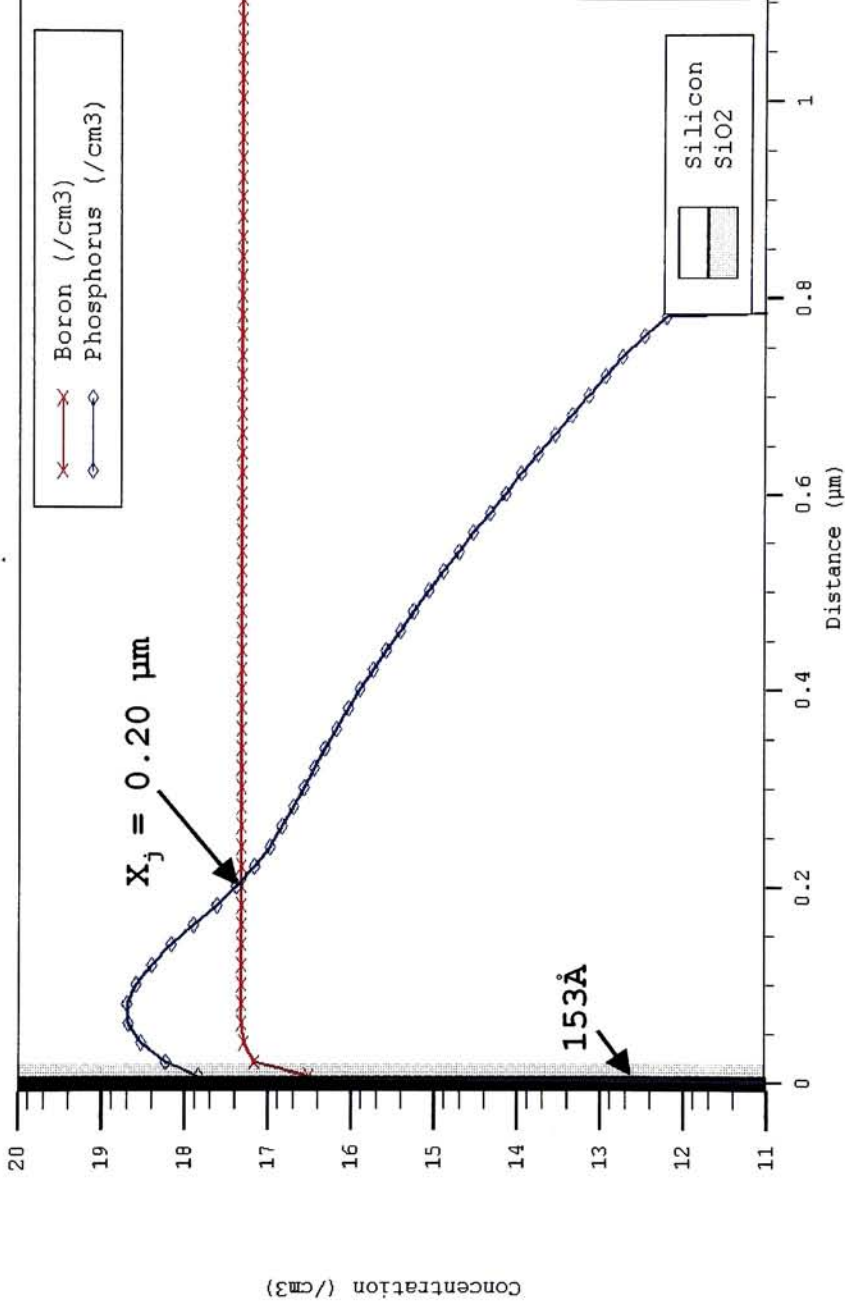
LDD Implant

- Implant P_{31}
 - Dose 5×10^{13} , energy = 65 KeV



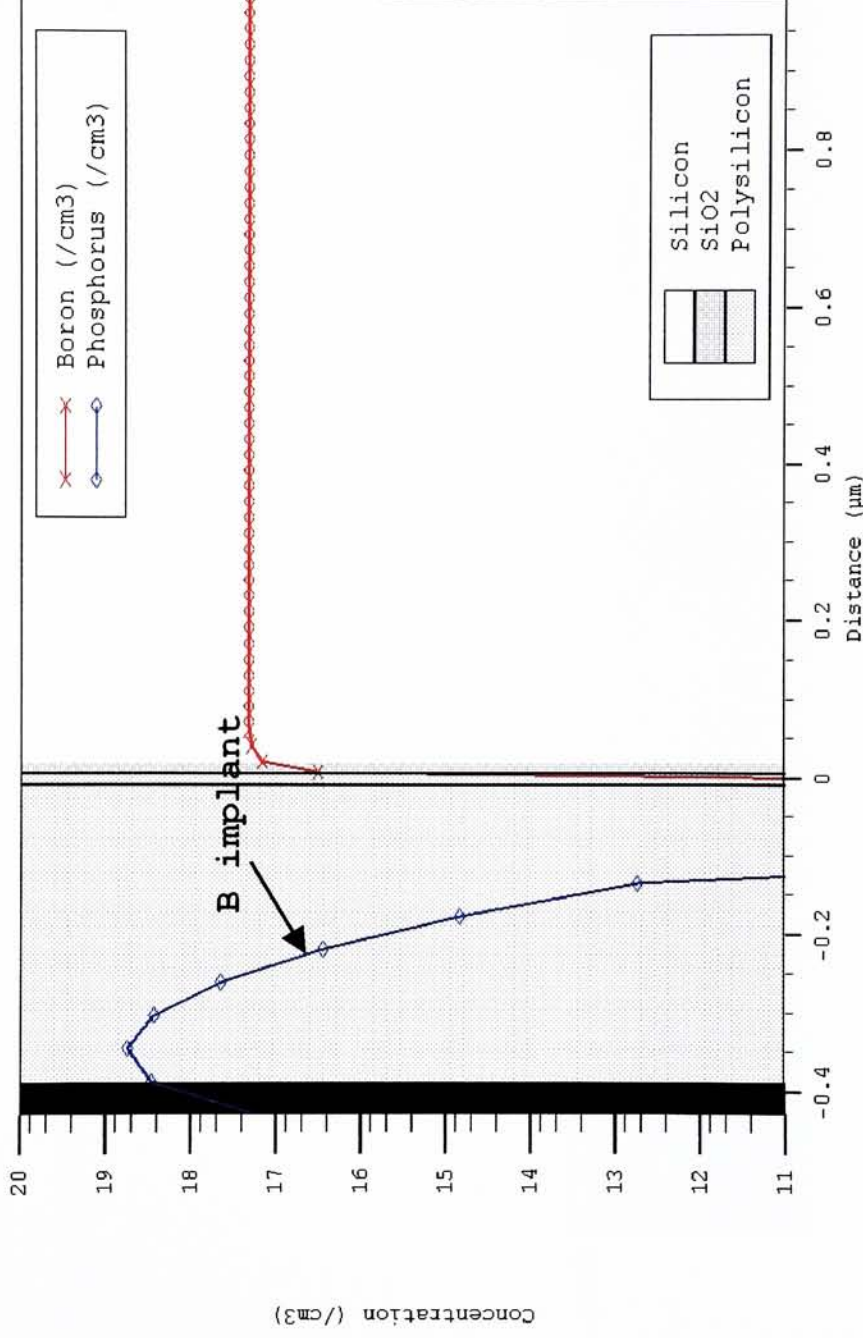
Simulation of n- LDD Implant

- Simulation of the implant in to the S/D region



Poly as a Mask

- The 4200Å Polysilicon is adequate for blocking the n- LDD implant



Strip Photoresist

- Strip resist in the asher



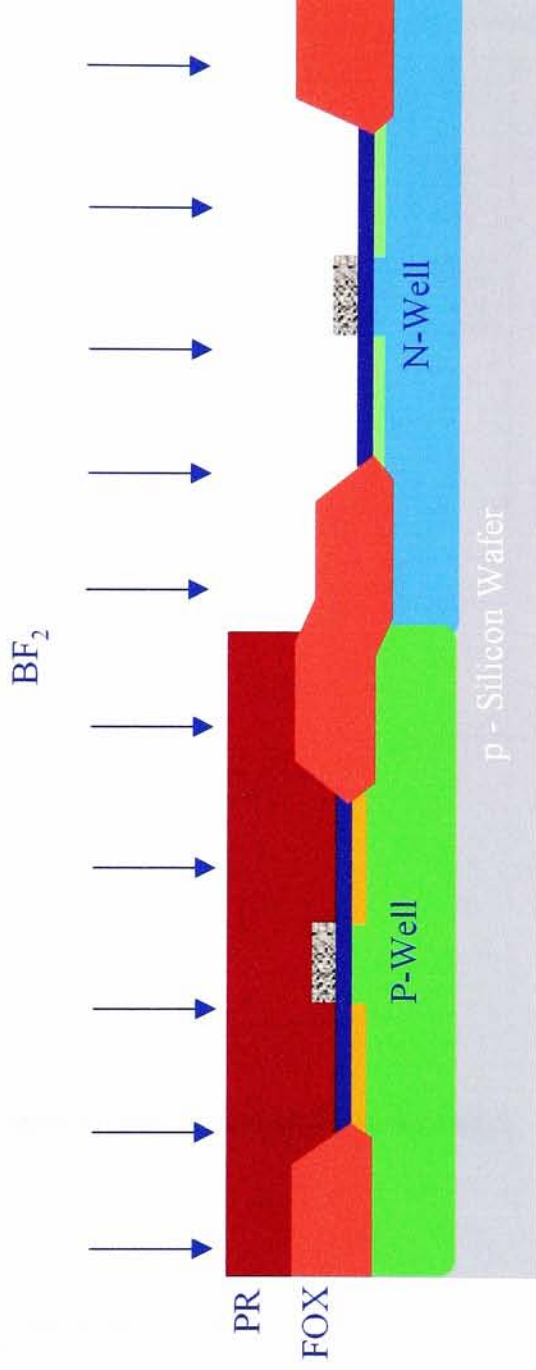
PMOS P- S/D Lithography

- Photolithography for defining PMOS S/D implant
 - Mask is same as level 1 (N-Well Mask)



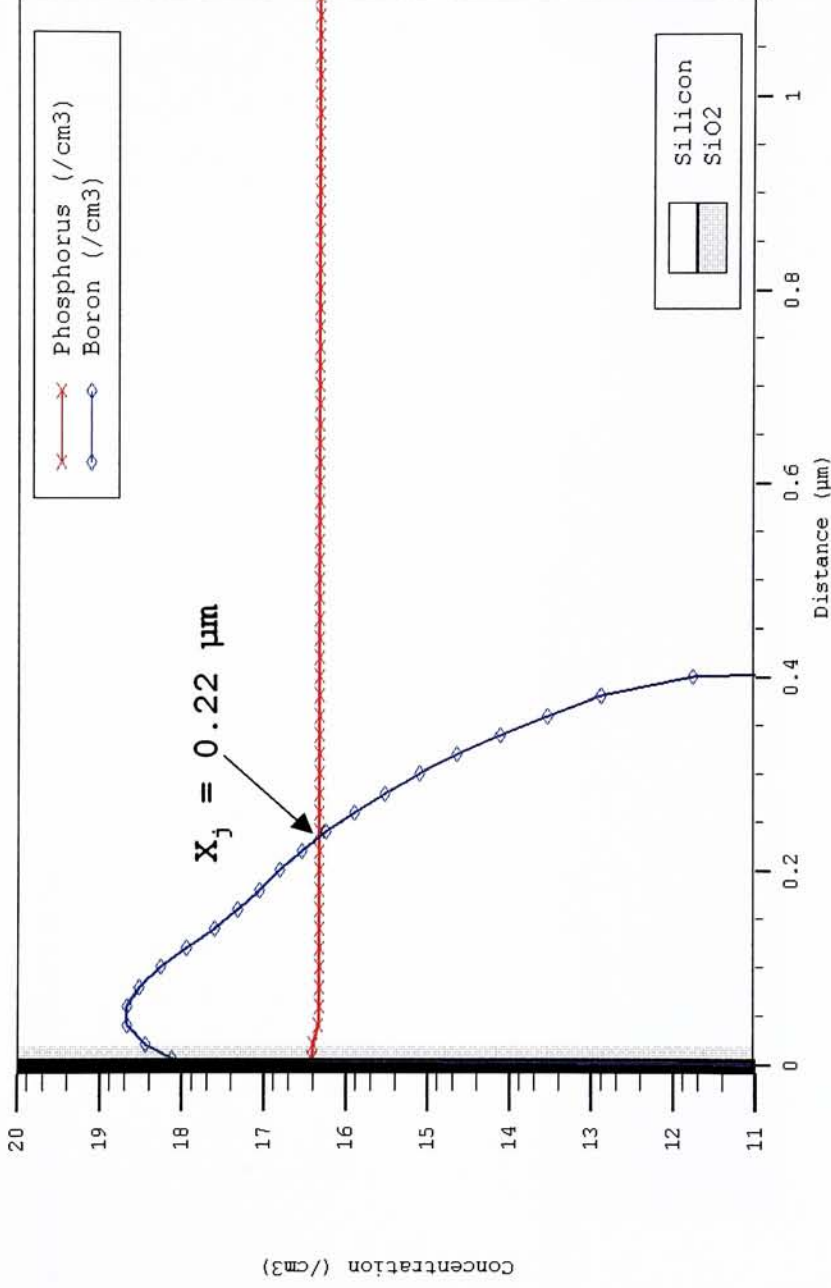
PMOS P- LDD Implant

- Implant BF_2
 - Dose 4.0×10^{13} , energy = 75 KeV
 - Use peak at AMU=49



Simulation of p- LDD Implant

- Silvaco simulation of the p- LDD implant



Strip Resist

- Plasma strip photoresist



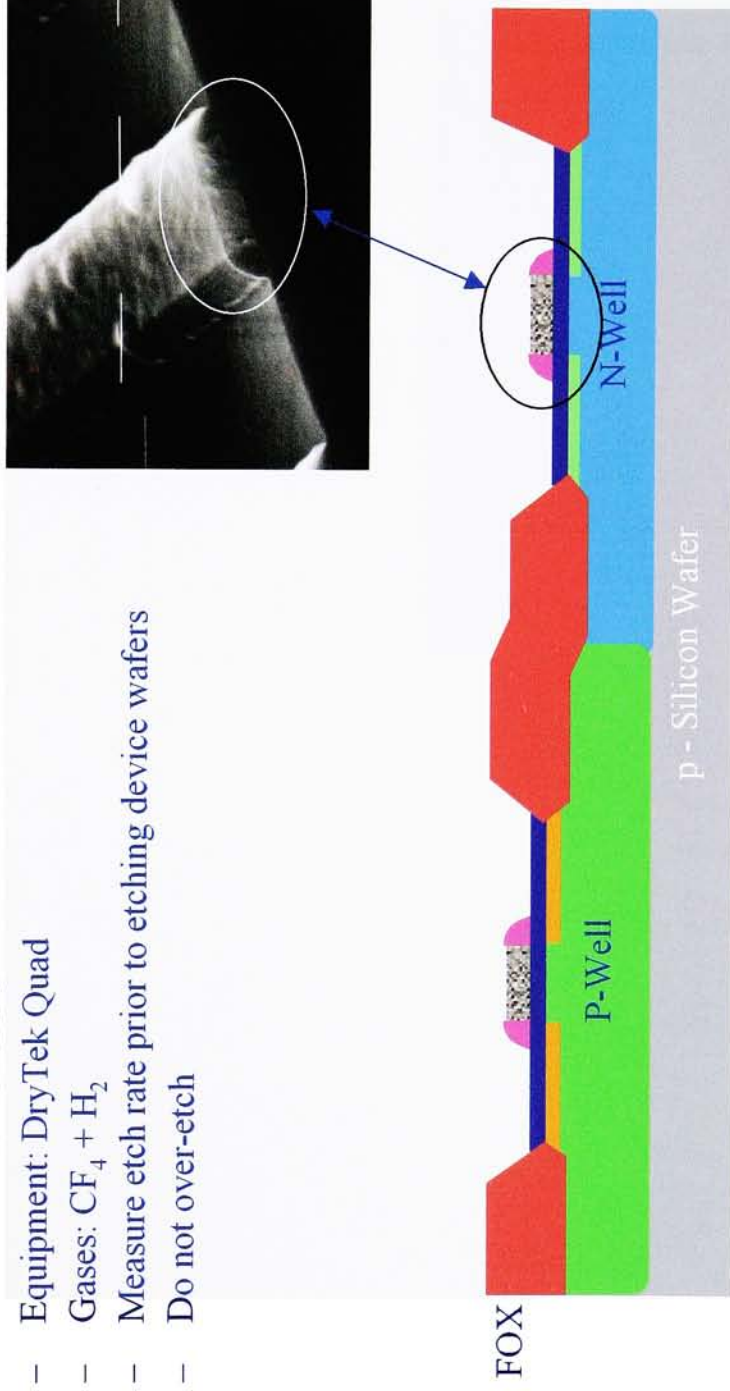
LTO Deposition

- Deposit LTO
 - Equipment: ASM CVD
 - Gases: Silane + Oxygen
 - Temperature: 400°C
 - Time: Calculated from log sheets
 - Target = 4000A



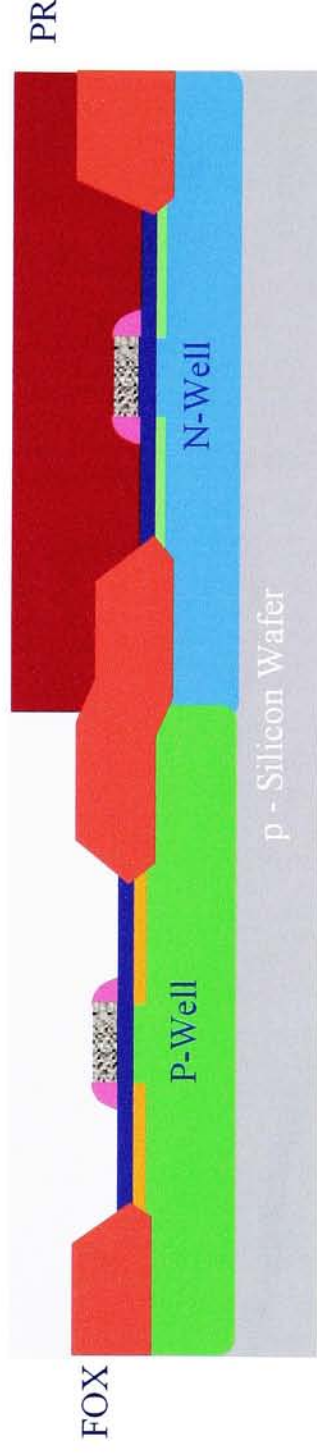
Sidewall Formation

- Plasma etch-back of LTO
 - Equipment: DryTek Quad
 - Gases: $\text{CF}_4 + \text{H}_2$
 - Measure etch rate prior to etching device wafers
 - Do not over-etch



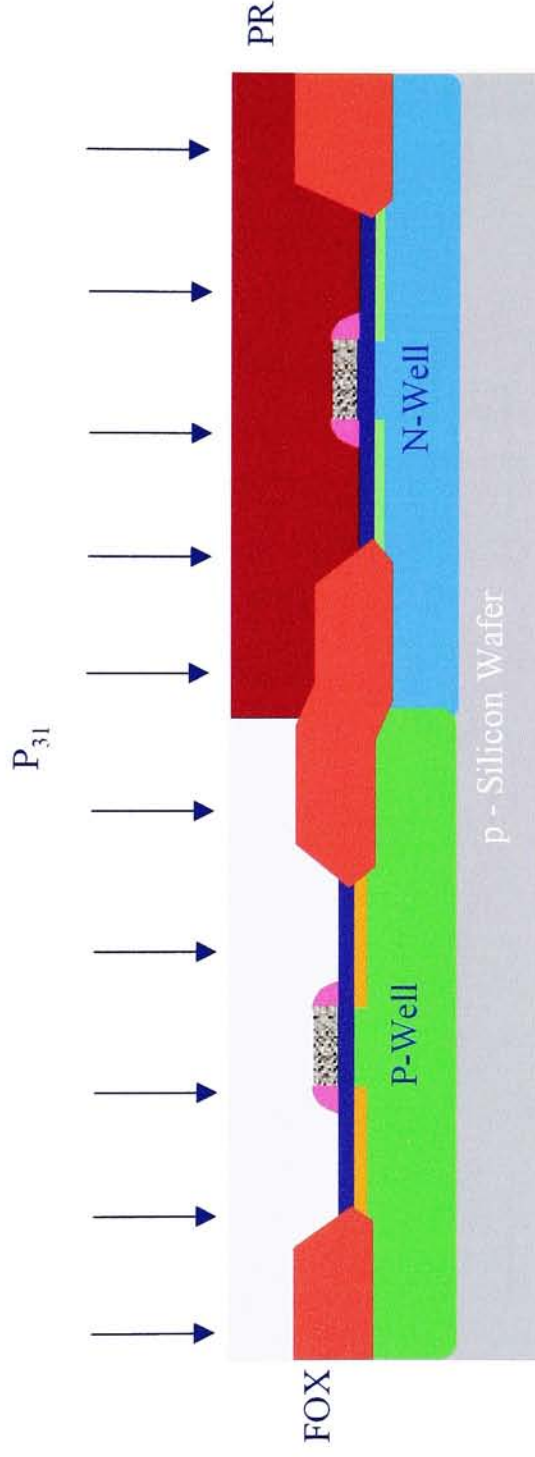
NMOS S/D Lithography

- Coat and expose using inverse of N-well mask



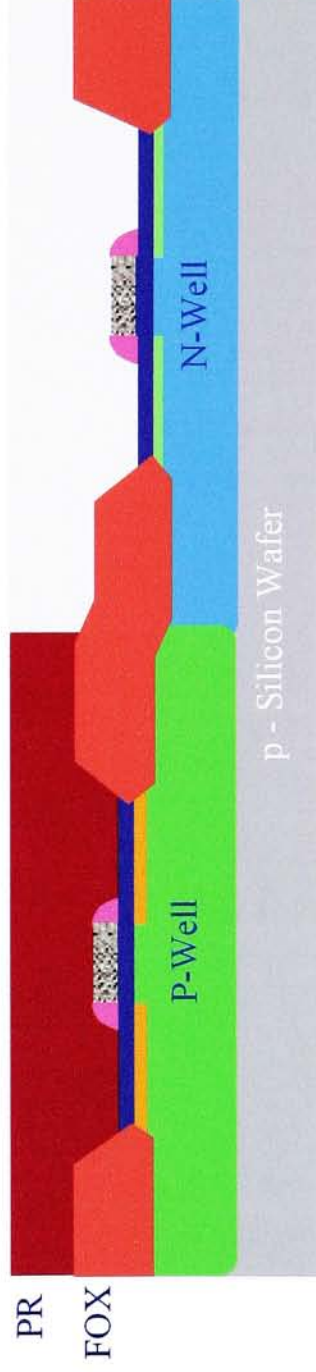
NMOS S/D Implant

- Implant P_{31}
 - Dose 3.25×10^{15} , energy = 85 KeV



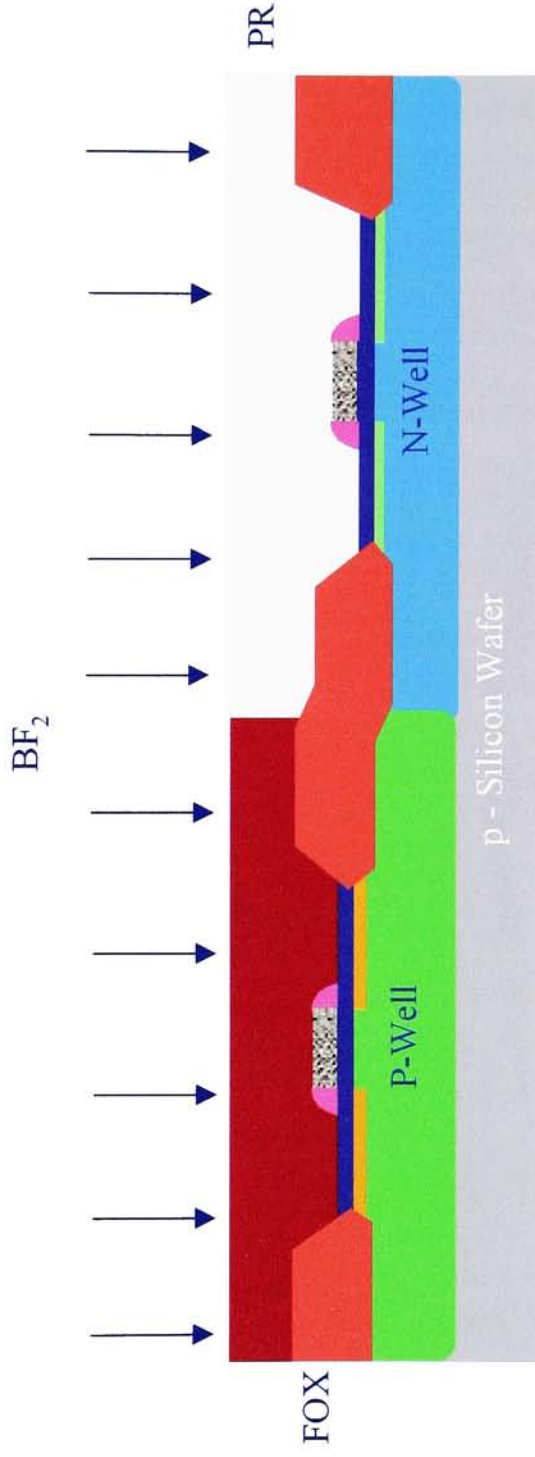
PMOS S/D Lithography

- Coat and expose using N-well mask



PMOS S/D Implant

- Implant BF_2
 - Dose 6.0×10^{15} , energy = 120 KeV

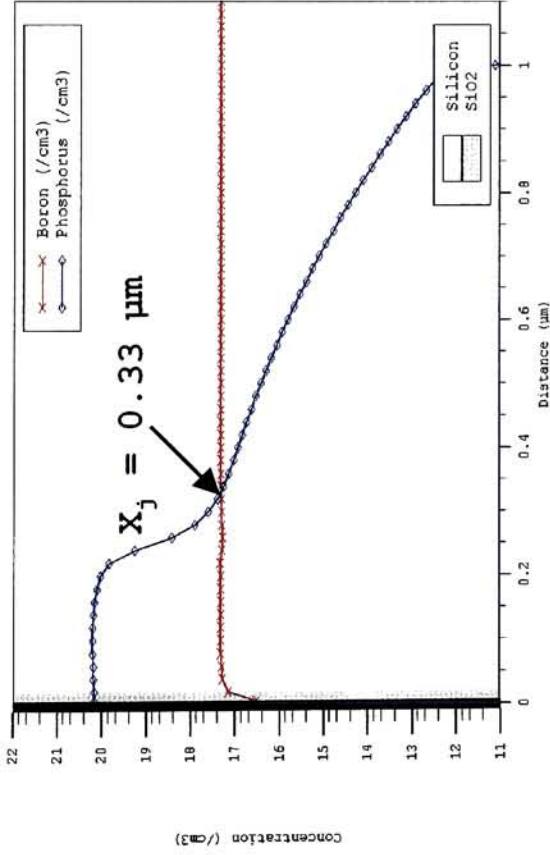


S/D Anneal

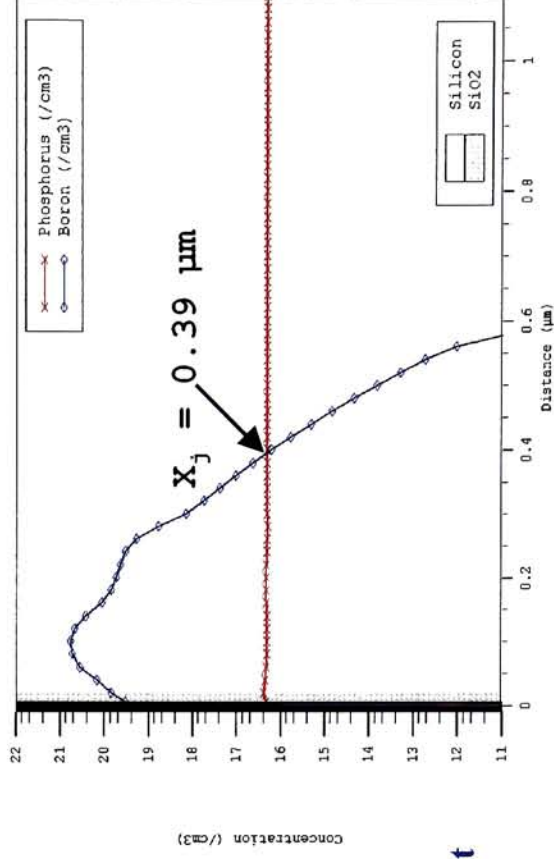
- Ash photoresist
- Plasma etch the 150Å gate oxide
- RCA clean
- S/D anneal
 - Temp = 900°C, time = 10 minutes



Simulation After S/D Anneal



NMOS S/D Implant



PMOS S/D Implant



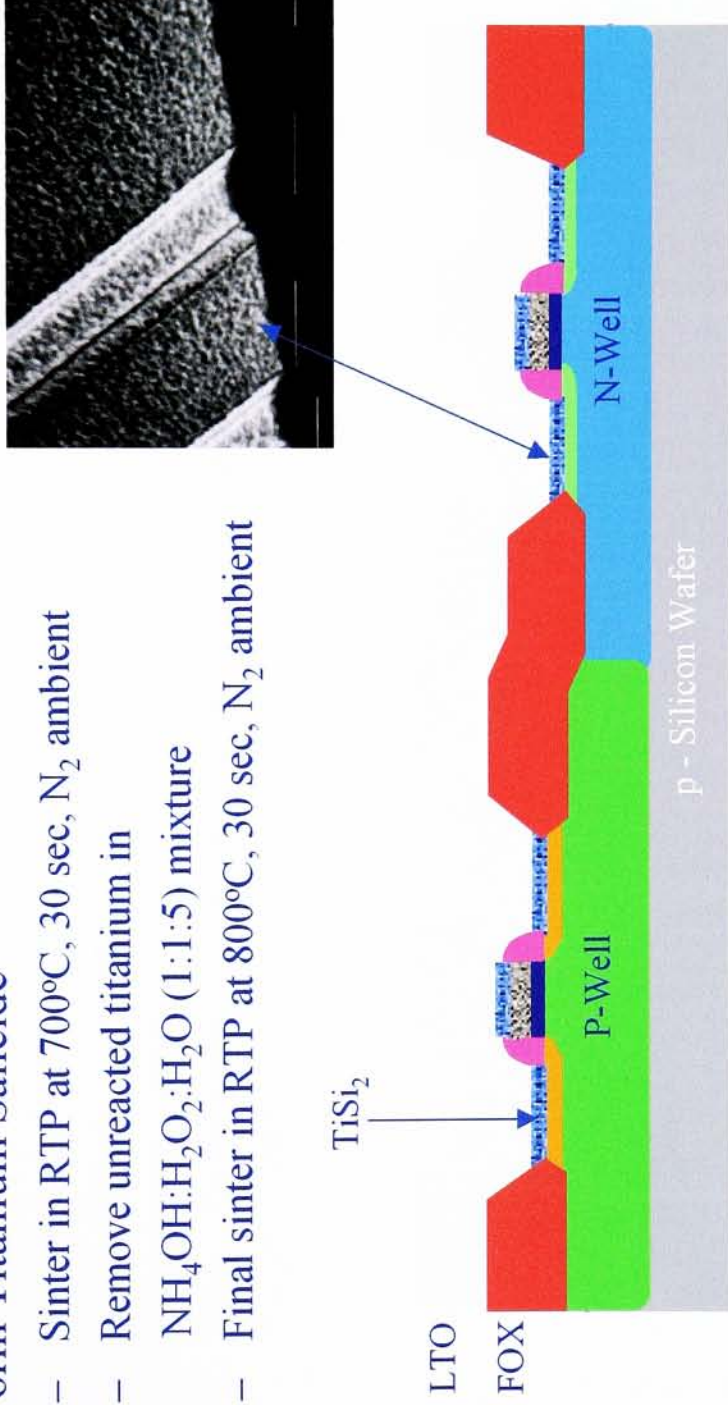
Deposit Titanium

- Sputter Titanium
 - Pressure = 5 mTorr, presputter = 10 min
 - Target = 1100 A



TiSi₂ Formation

- Form Titanium Salicide
 - Sinter in RTP at 700°C, 30 sec, N₂ ambient
 - Remove unreacted titanium in NH₄OH:H₂O₂:H₂O (1:1:5) mixture
 - Final sinter in RTP at 800°C, 30 sec, N₂ ambient



LTO Deposition

- Deposit LTO
 - Equipment: ASM CVD
 - Gases: Silane + Oxygen
 - Temperature: 400°C
 - Time: To be determined from SPC charts or log sheets
 - Target = 4000 Å



Contact Cut Lithography

- Contact cut lithography
 - Equipment: DryTek Quad
 - Gases: CHF₃ + SF₆
 - Etch rate: To be determined using control wafers
 - Etch time: To be calculated from etch rate



Metal Deposition/Lithography

- Deposit Aluminum
 - Equipment: CVC 601 Sputterer
 - Gas/Pressure: Argon/5 mTorr
 - Pre-sputter: 10 minutes
 - Sputter time: Calculate from SPC charts or log sheets
 - Target thickness = 5000 Å
- Metal Lithography
- Etch Aluminum
 - Dry/Wet Chemical etch



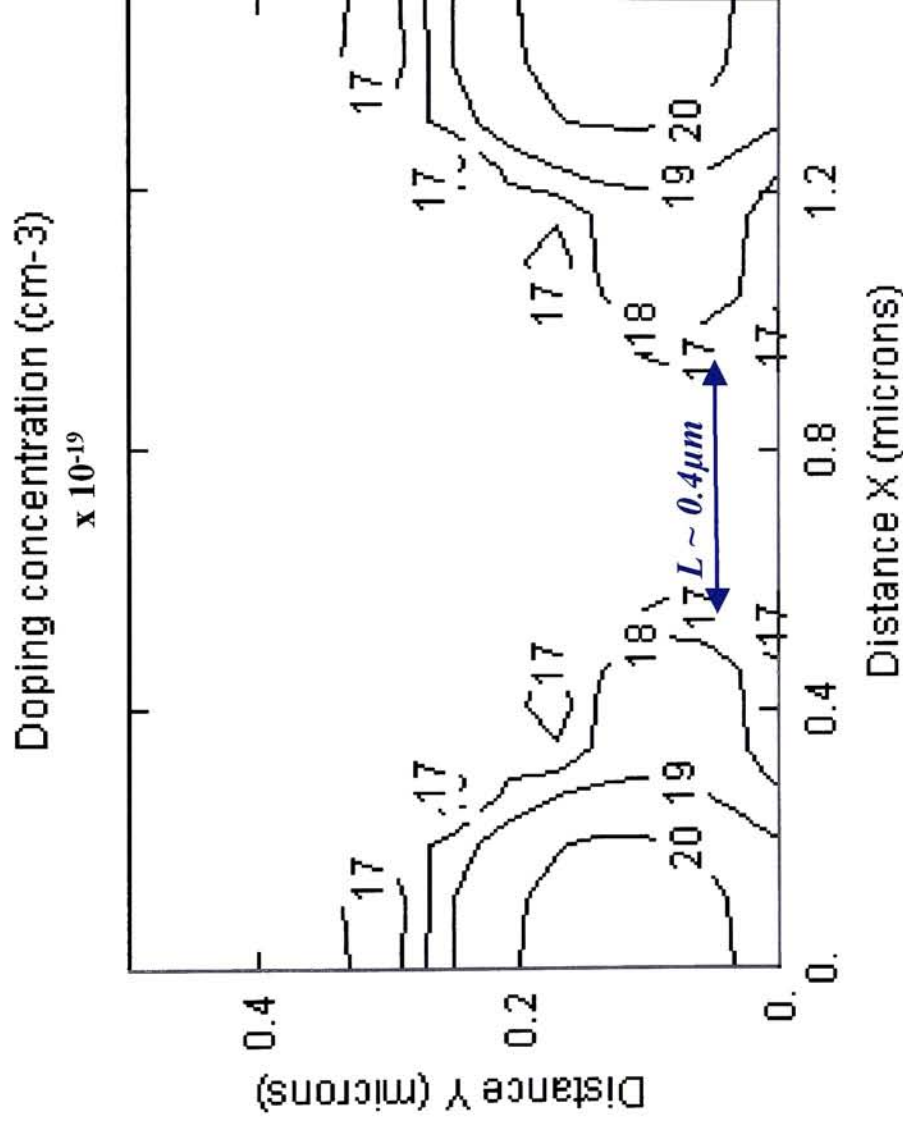
Sintering

- Sinter (to reduce contact resistance)
 - Equipment: Bruce Furnace
 - Gas: Forming gas H_2N_2
 - Temperature: 400°C
 - Time: 20 minutes

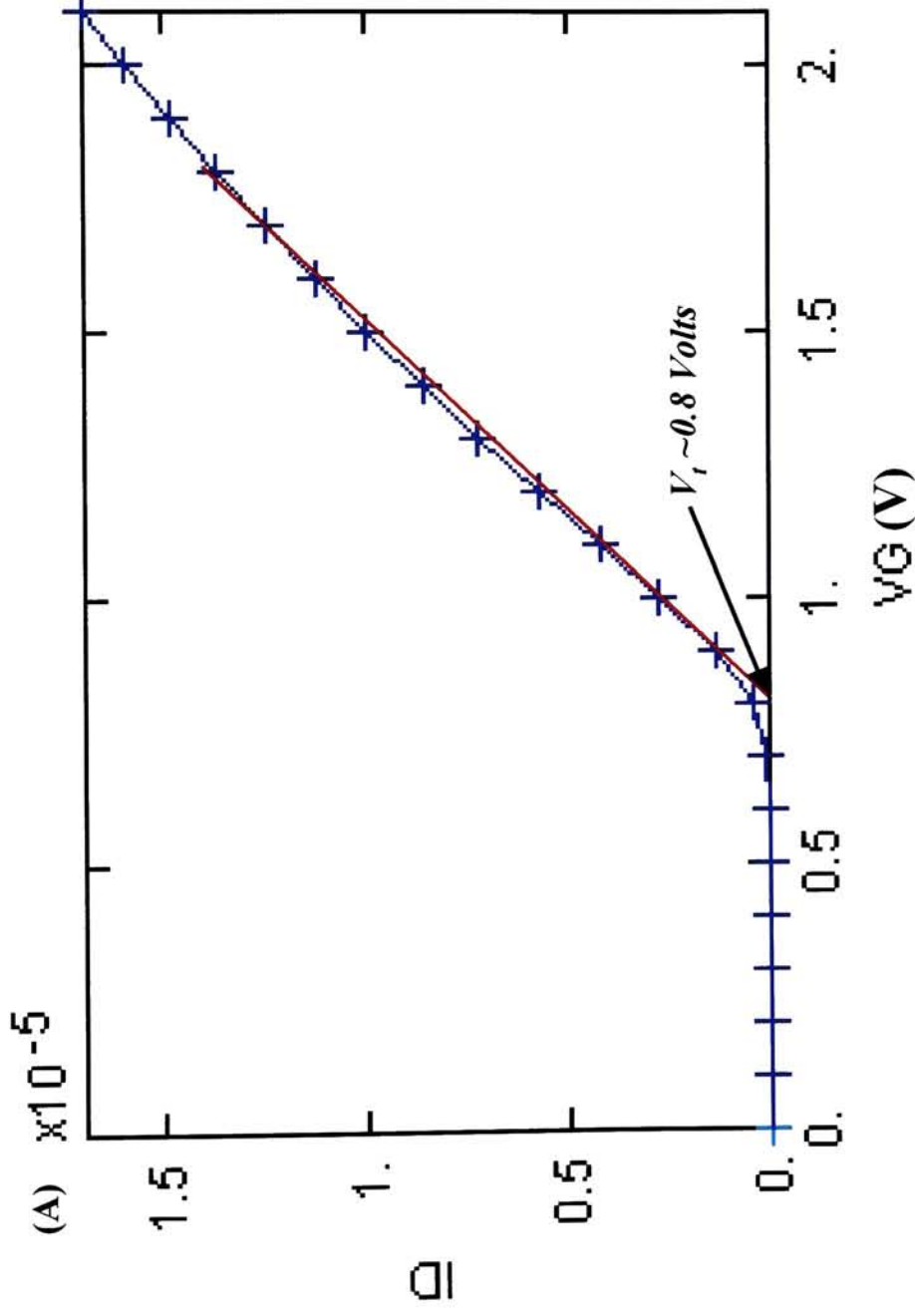


APPENDIX B - SIMULATION RESULTS

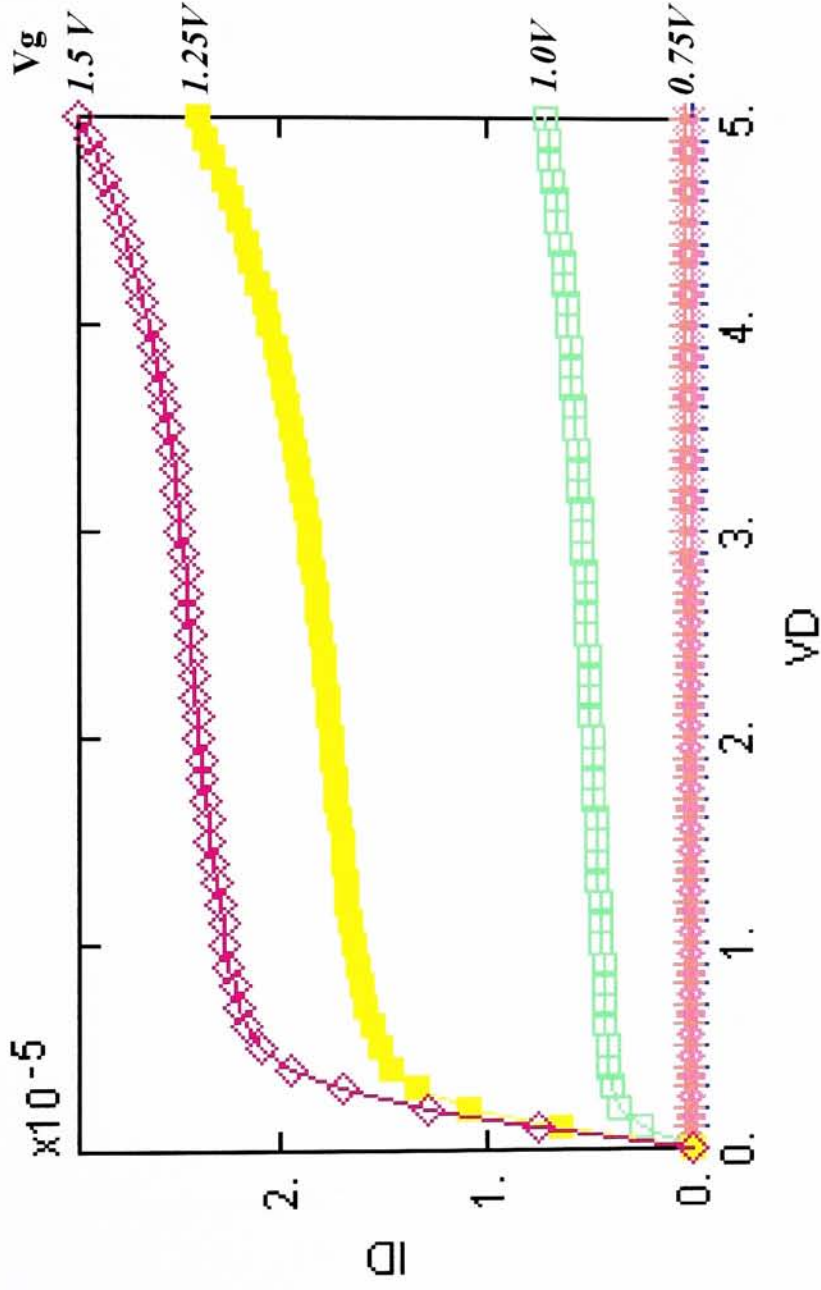
NMOS – Final Crossection



NMOS I_d vs V_g (V_t Curve)

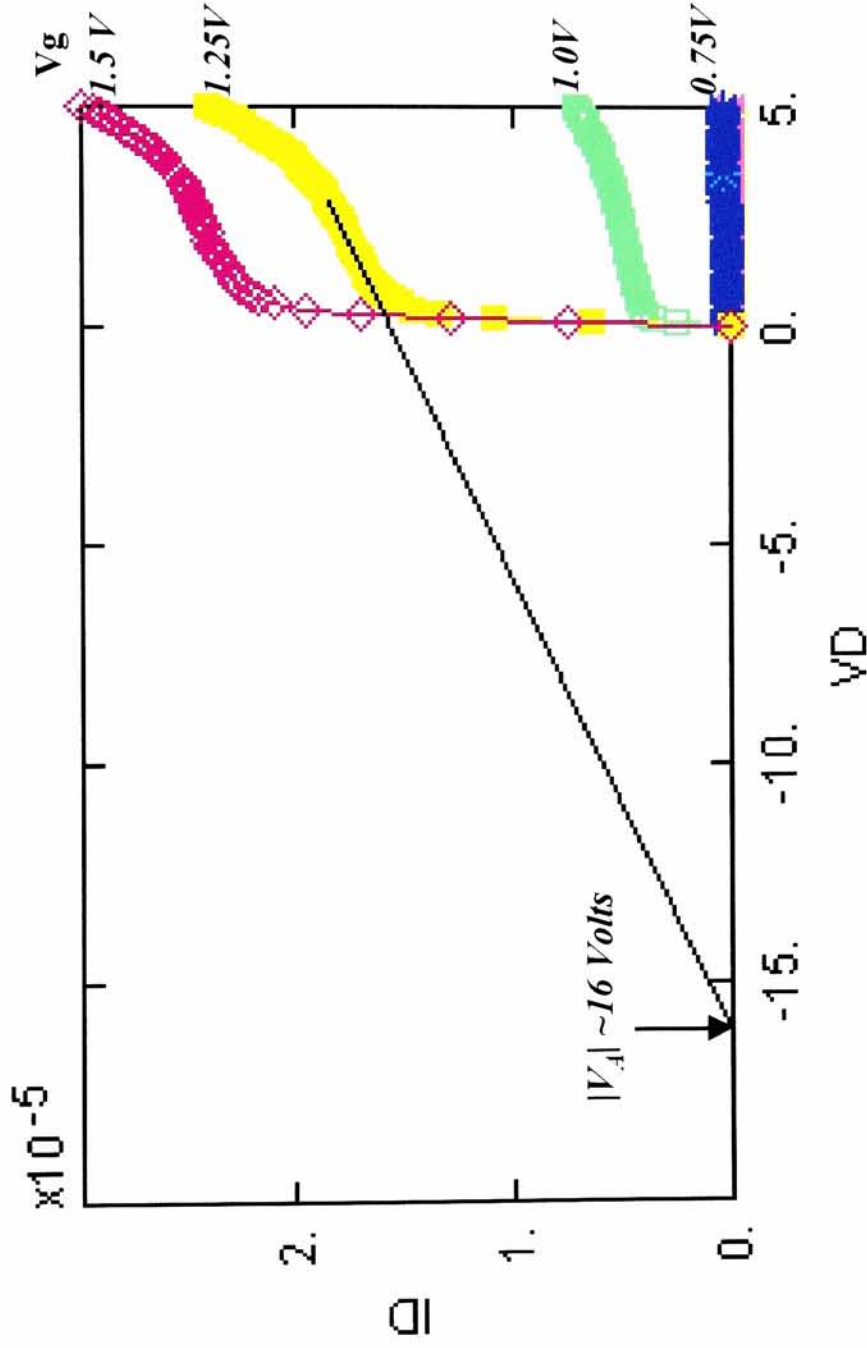


NMOS Family of Curves

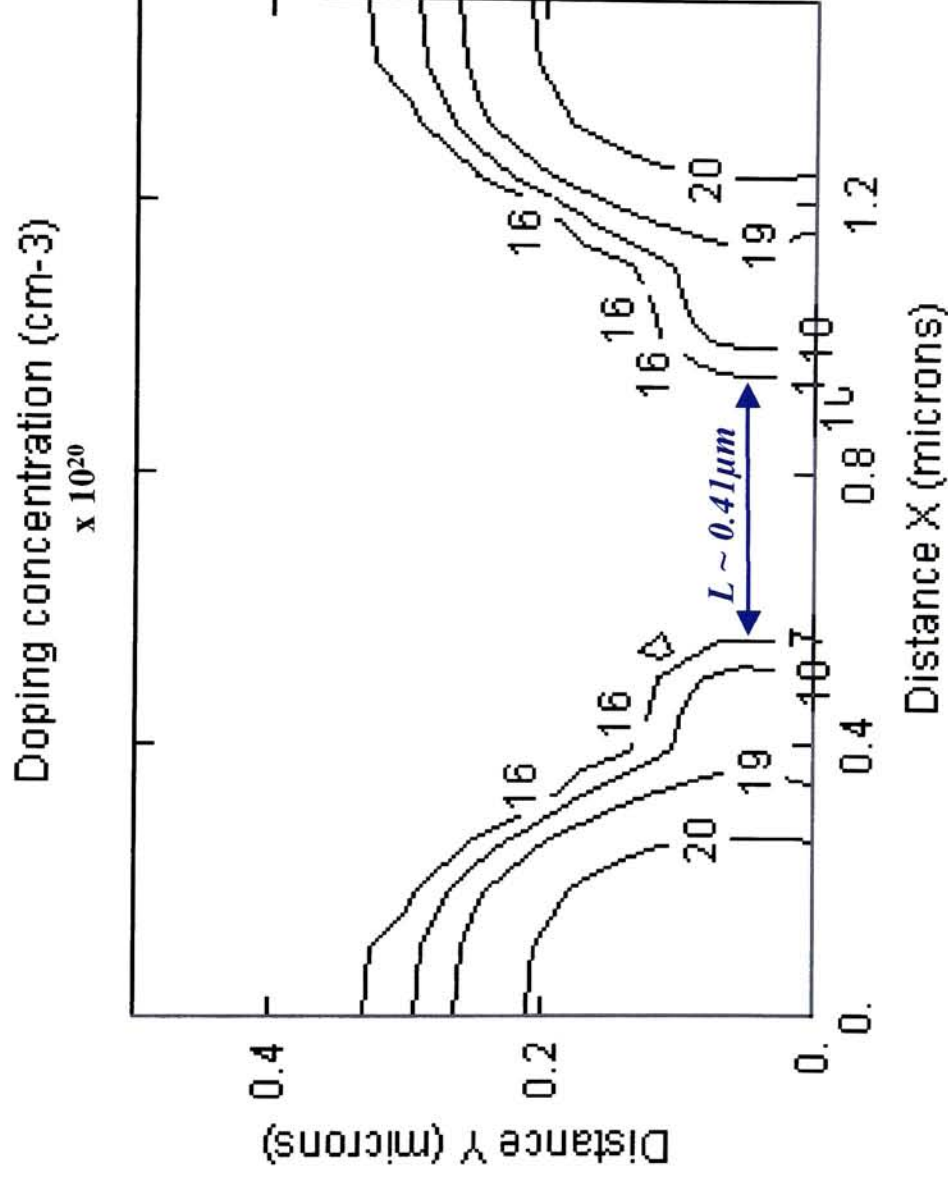


* V_g Varied from 0 Volts to 1.5 Volts with increments of 0.25 Volts
 $V_{dd} = 0.1$ Volts, $V_{sub} = 0$ Volts, $V_s = 0$ Volts

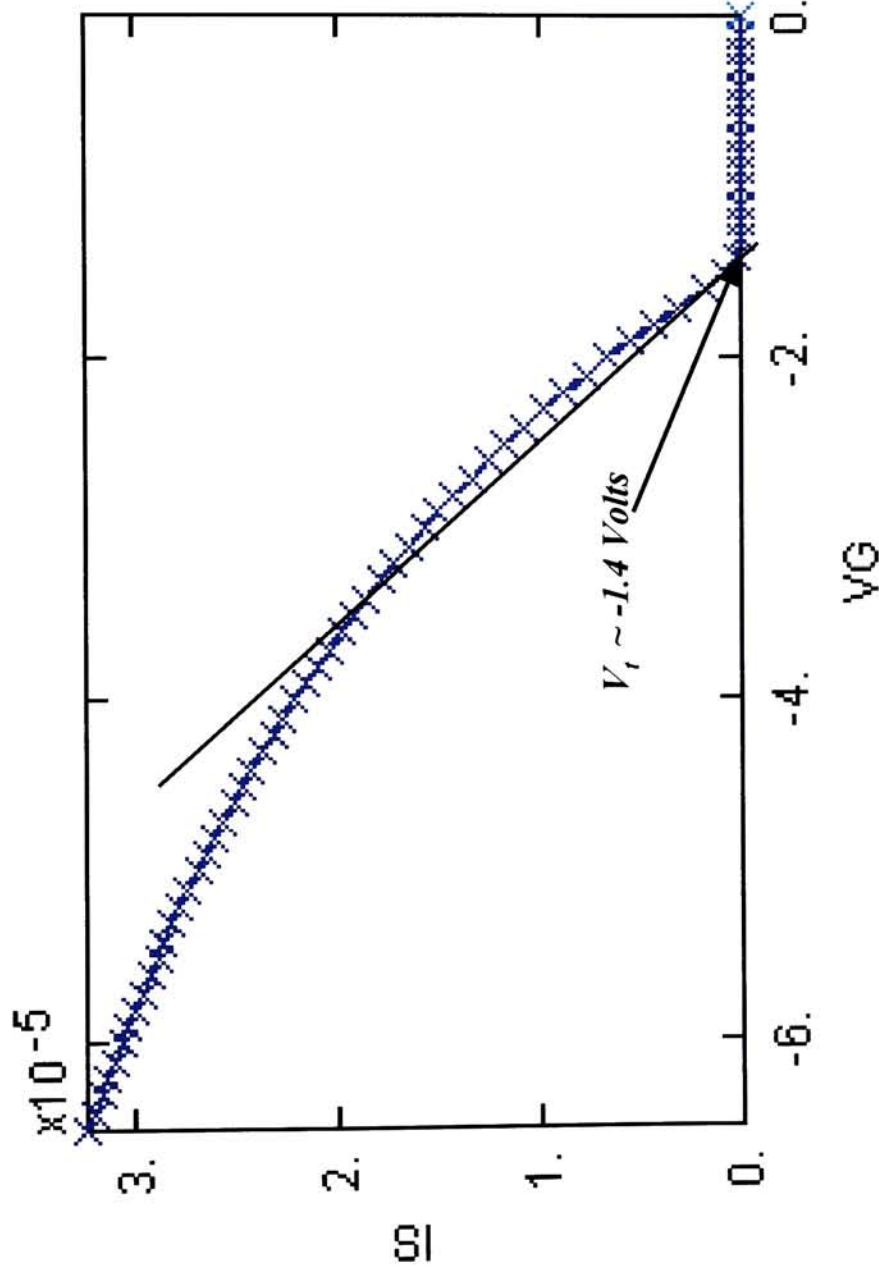
NMOS Early Voltage Extraction



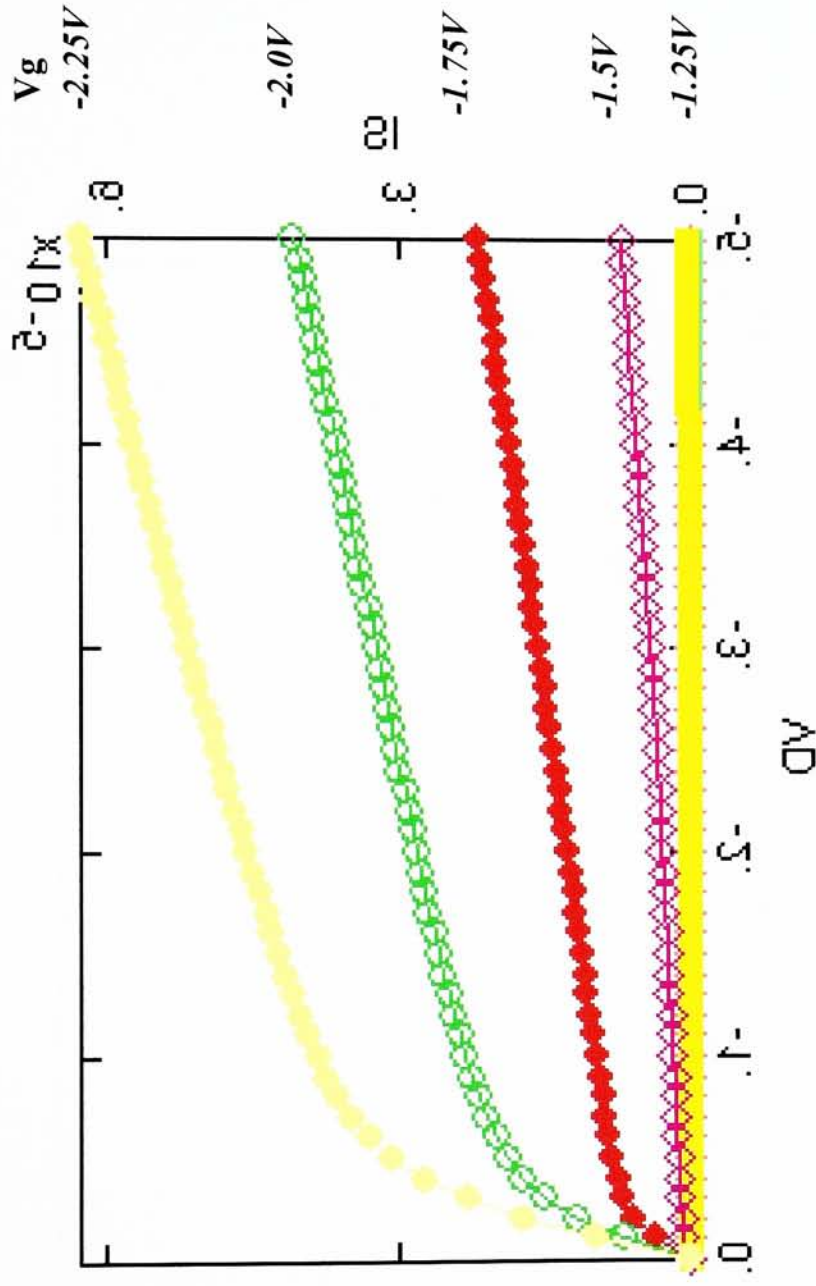
PMOS Final Crossection



PMOS I_S vs V_g (V_t Curve)

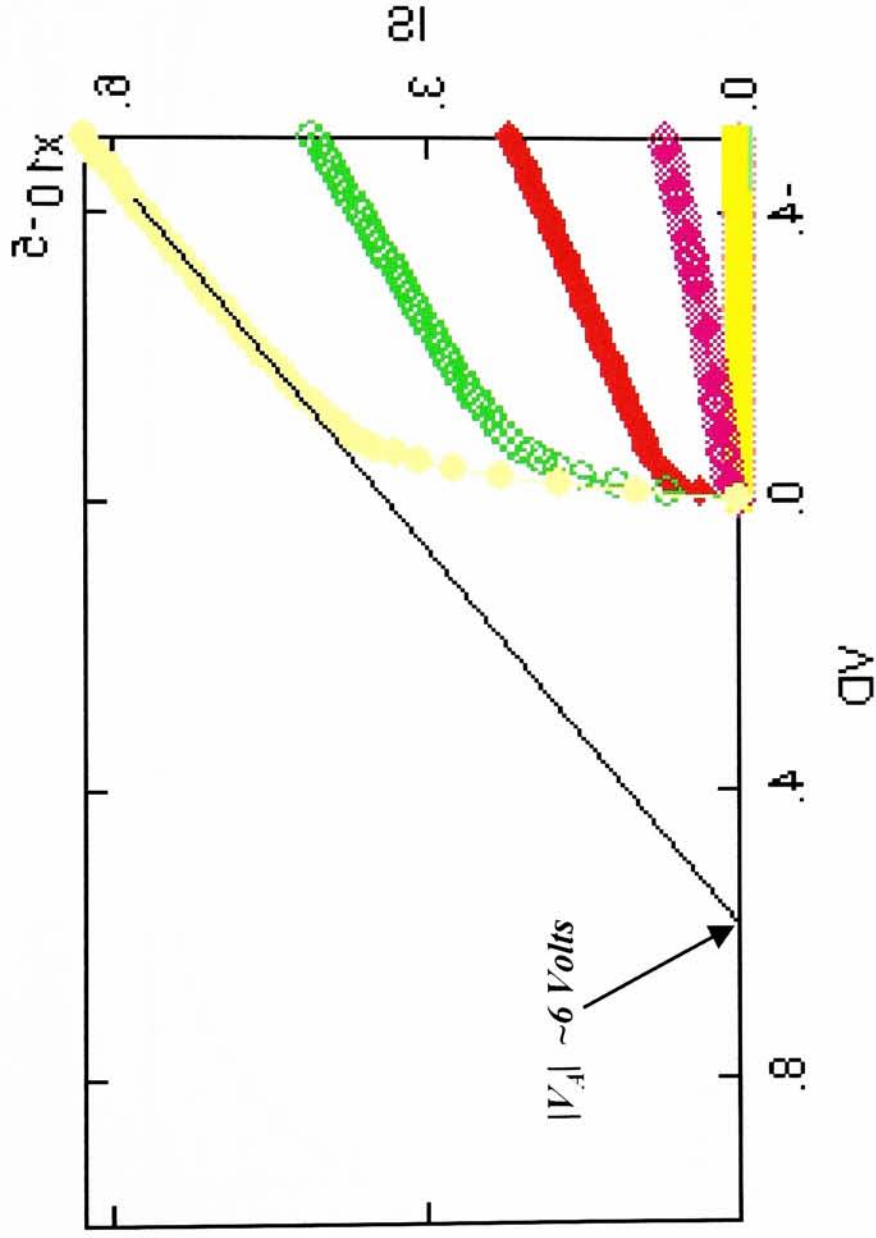


PMOS Family of Curves



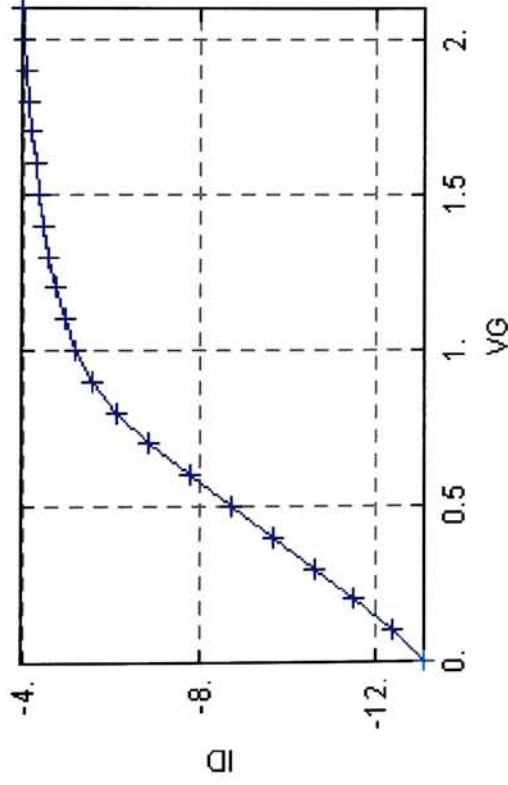
* V_g Varied from 0 Volts to -2.25 Volts with increments of -0.25 Volts
 $V_{dd} = -0.1$ Volts, $V_{sub} = 0$ Volts, $V_s = 0$ Volts

PMOS Early Voltage Extraction



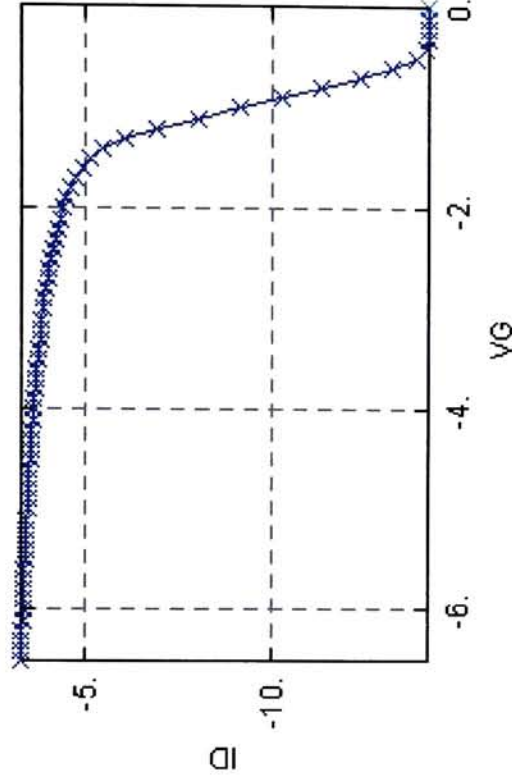
Subthreshold Simulation Results

NMOSFET



Swing ~ 90 mV/decade
Off-state Current ~ 10^{-14} A

PMOSFET



Swing ~ 100 mV/decade
Off-state Current ~ 10^{-17} A



Recommendations/Future Work



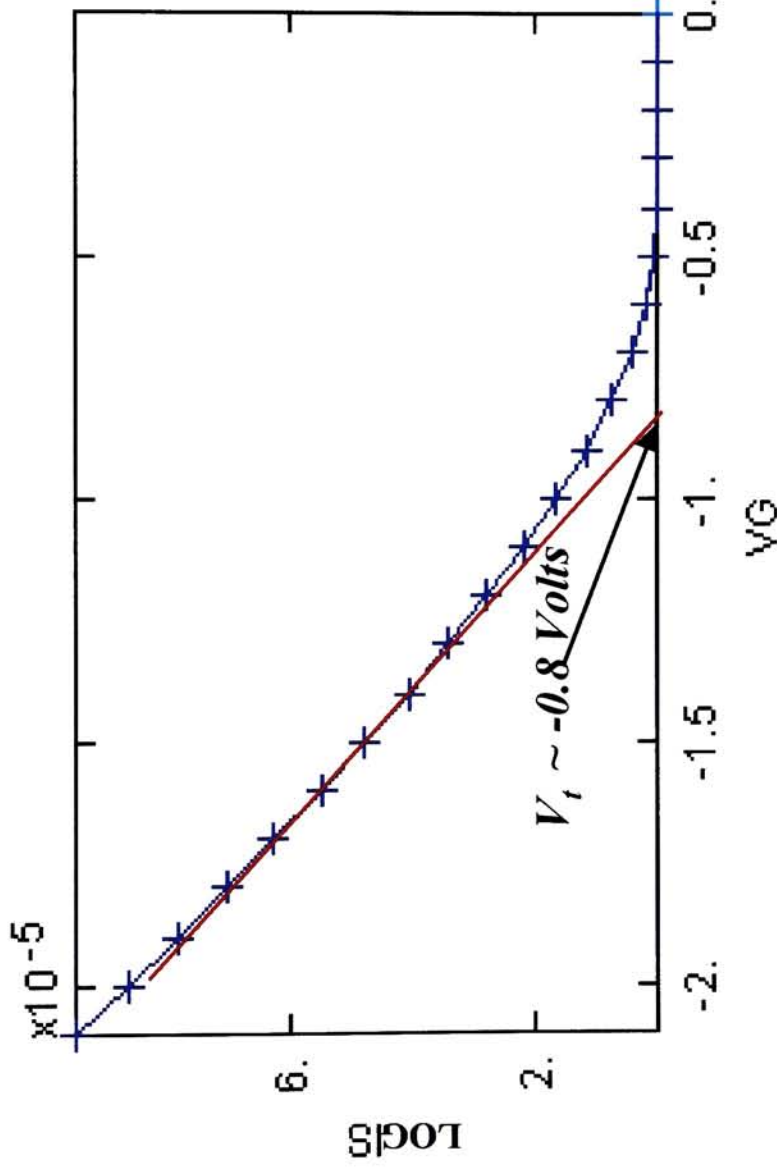
Upgrade the PMOS!

- Use of p+ poly gate
 - Better control of the threshold voltage
 - $\phi_{ms} = 5.33$ Volts
- Will require changes to the layout
 - Extra masking steps
 - Change in implant dose



V_t for PMOS (p+ Poly) – 0.5 μm FET

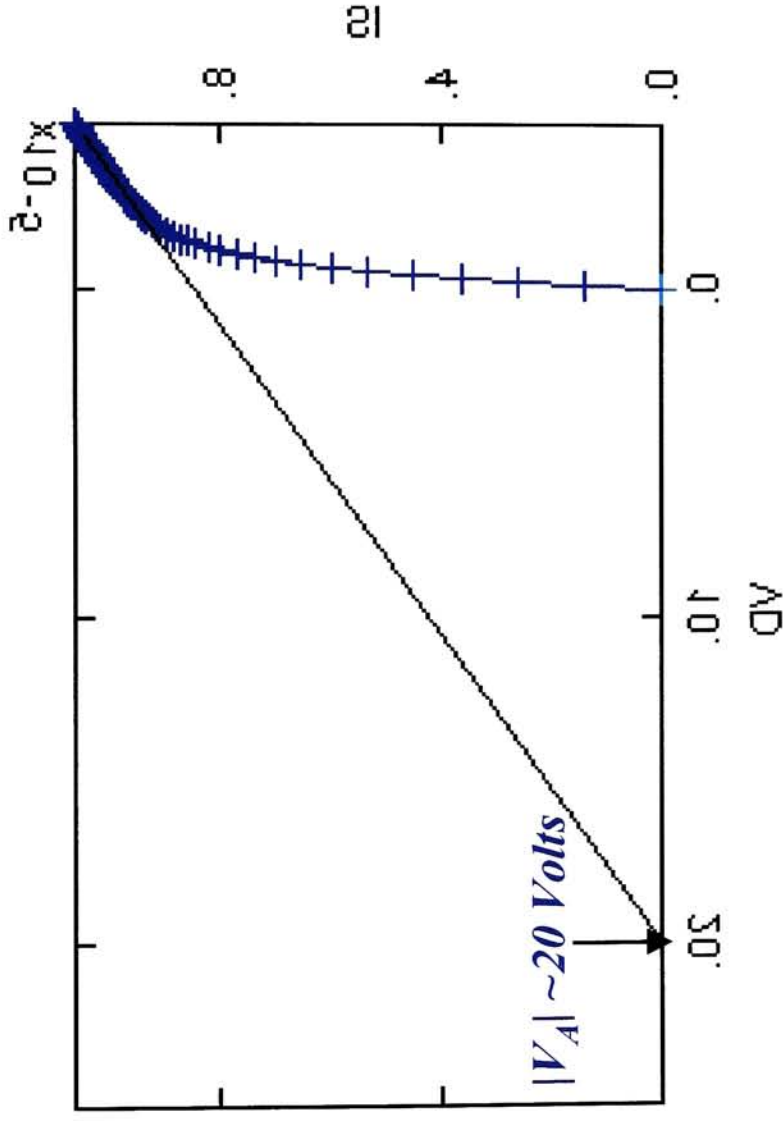
- N-well implant dose increased to $9 \times 10^{12} \text{ cm}^{-2}$
- D/S implant decreased to $4.5 \times 10^{15} \text{ cm}^{-2}$



Lower threshold voltage than n+ poly gate



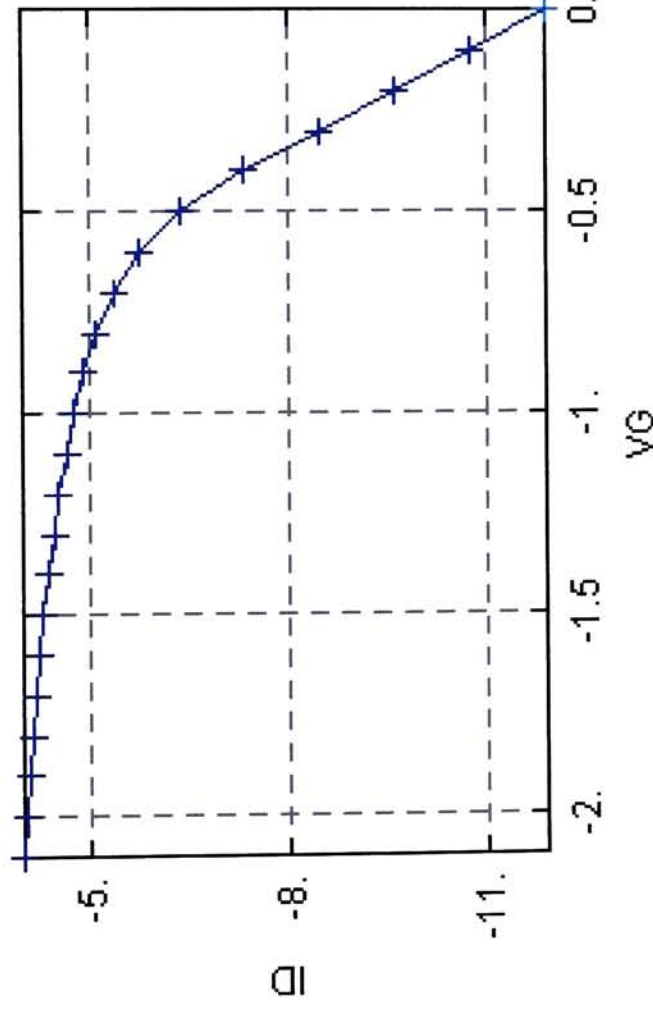
Early Voltage



Channel length modulation has been lowered, leading to a higher Early voltage (~ 20 volts)



Subthreshold Characteristics



*Swing = 93mV/decade = Better subthreshold swing
Off-State current $\sim 10^{-14}A$, but a leakier transistor*



APPENDIX C - INPUT FILES FOR MICROTEC

NMOSFET Fabrication		P0000030_3D
Domain and Mesh		
Comment		NMOSFET fabrication
Number of nodes NX		100
Number of nodes NY		200
Domain size in X-direction(um)		0.75
Domain size in Y-direction(um)		3
Mesh generation		0
Y-mesh exponent (um)		4
Substrate		
Lattice Orientation		100
Initial Boron conc (cm-3)		1e+14
Boron implant		
Comment		P-well implant
Boron implant mask (um)		0.75
Boron implant dose (cm-2)		2.5e+13
Boron implant energy (KeV)		50
Annealing		
Comment		Ramp up
Temperature (degrees C)		800
Annealing time (s)		300
Time step		100
Annealing		
Comment		Twin-well drive-in
Temperature (degrees C)		1100
Annealing time (s)		12600
Time step		100
Annealing		
Comment		Second Pad Oxide
Temperature (degrees C)		1000
Annealing time (s)		2880
Time step		100
Annealing		
Comment		Field Oxide Growth
Temperature (degrees C)		1100
Annealing time (s)		2880
Time step		100
Annealing		
Comment		KOO1 Oxidation
Temperature (degrees C)		900
Annealing time (s)		2700
Time step		100
Oxidation		
Comment		Gate oxide growth
Temperature (degrees C)		900
Annealing time (s)		2880
Time step (s)		100
Ambient type		1
Pressure (atm)		1
Oxidation Mask (um)		1000
Initial oxide pad (um)		0.001
Annealing		
Comment		Poly doping
Temperature (degrees C)		1000
Annealing time (s)		450
Time step		200
Phosphorus implant		
Comment		NMOS LDD N- Implant
Phosphorus implant mask		0.5
Phosphorus implant dose (cm-2)		4e+13
Phosphorus implant energy(KeV)		65
Phosphorus implant		
Comment		NMOS S/D Implant
Phosphorus implant mask		0.2
Phosphorus implant dose (cm-2)		3.25e+15
Phosphorus implant energy(KeV)		85
Annealing		
Comment		LDD annealing
Temperature (degrees C)		900
Annealing time (s)		600
Time step		200

Input Parameters for NMOS Electrical Simulation

NMOSFET Vt		P0000032.2D P0000032.3D
Numerical doping data		
Basic		
Physical models		
<input type="checkbox"/>	Impact ionization	1
Mesh		
<input type="checkbox"/>	Number of X-nodes	51
<input type="checkbox"/>	Number of Y-nodes	50
<input type="checkbox"/>	Domain X size	1.5
<input type="checkbox"/>	Domain Y size (um)	2
<input type="checkbox"/>	Domain Z size (um)	1
<input type="checkbox"/>	First Y mesh step size (um)	0.01
<input type="checkbox"/>	Remesh	3
Numerical solution parameters		
<input type="checkbox"/>	Comment line	Subthreshold
<input type="checkbox"/>	Batch mode	1
Electrodes		
Ohmic electrode		
<input type="checkbox"/>	Electrode name	Bulk
<input type="checkbox"/>	Electrode number	1
<input type="checkbox"/>	Electrode location	2
<input type="checkbox"/>	Electrode left edge (um)	0
<input type="checkbox"/>	Electrode right edge (um)	1.5
Ohmic electrode		
<input type="checkbox"/>	Electrode name	Source
<input type="checkbox"/>	Electrode number	2
<input type="checkbox"/>	Electrode location	1
<input type="checkbox"/>	Electrode left edge (um)	0
<input type="checkbox"/>	Electrode right edge (um)	0.2
Gate electrode		
<input type="checkbox"/>	Electrode name	Gate
<input type="checkbox"/>	Electrode number	3
<input type="checkbox"/>	Electrode location	1
<input type="checkbox"/>	Electrode left edge	0.5
<input type="checkbox"/>	Electrode right edge	1
<input type="checkbox"/>	Gate oxide thickness	0.015
<input type="checkbox"/>	Location of interface charge	1e-2
<input type="checkbox"/>	Width of interface charge	1e-2
<input type="checkbox"/>	Interface charge density	2e+11
<input type="checkbox"/>	Peak interface charge density	0
<input type="checkbox"/>	Electron recombination velocity	1e-15
<input type="checkbox"/>	Hole recombination velocity	1e-15
<input type="checkbox"/>	Metal work function	4.12
Ohmic electrode		
<input type="checkbox"/>	Electrode name	Drain
<input type="checkbox"/>	Electrode number	4
<input type="checkbox"/>	Electrode location	1
<input type="checkbox"/>	Electrode left edge (um)	1.3
<input type="checkbox"/>	Electrode right edge (um)	1.5
IV-data		
IV-data		
<input type="checkbox"/>	IV-curve label	IV-curve
<input type="checkbox"/>	Ramped contact number	3
<input type="checkbox"/>	Number of IV-points to compute	51
<input type="checkbox"/>	Voltage step size (V)	0.1
<input type="checkbox"/>	Initial voltage for contact #4	0.1
<input type="checkbox"/>	Initial voltage for contact #1	0
<input type="checkbox"/>	Initial voltage for contact #3	0
<input type="checkbox"/>	Initial voltage for contact #2	0

Input Parameters for PMOS Process Simulation

PMOSFET Fabrication		P0000033 3D
Domain and Mesh		
Comment		PMOSFET fabrication
Number of nodes NX		100
Number of nodes NY		200
Domain size in X-direction(um)		0.75
Domain size in Y-direction(um)		3
Mesh generation		0
Y-mesh exponent (um)		4
Substrate		
Lattice Orientation		100
Initial Boron conc (cm-3)		1e+14
Phosphorus implant		
Comment		N-Well Implant
Phosphorus implant mask		1000
Phosphorus implant dose (cm-2)		9e+12
Phosphorus implant energy(KeV)		150
Annealing		
Comment		N-well drive-in
Temperature (degrees C)		1100
Annealing time (s)		2880
Time step		200
Annealing		
Comment		Twin-well drive-in
Temperature (degrees C)		1100
Annealing time (s)		12600
Time step		100
Annealing		
Comment		Second LOCOS start
Temperature (degrees C)		1000
Annealing time (s)		2880
Time step		100
Annealing		
Comment		Field Oxide Growth
Temperature (degrees C)		1100
Annealing time (s)		2880
Time step		100
Annealing		
Comment		KOOI Oxidation
Temperature (degrees C)		900
Annealing time (s)		2700
Time step		200
Oxidation		
Comment		Gate oxide growth
Temperature (degrees C)		900
Annealing time (s)		2880
Time step (s)		200
Ambient type		1
Pressure (atm)		1
Oxidation Mask (um)		1000
Initial oxide pad (um)		0.001
Annealing		
Comment		Poly doping
Temperature (degrees C)		1000
Annealing time (s)		450
Time step		200
Boron implant		
Comment		P- LDD Implant
Boron implant mask (um)		0.5
Boron implant dose (cm-2)		4e+13
Boron implant energy (KeV)		17
Boron implant		
Comment		Comment
Boron implant mask (um)		0.2
Boron implant dose (cm-2)		4.5e+15
Boron implant energy (KeV)		27
Annealing		
Comment		LDD annealing
Temperature (degrees C)		900
Annealing time (s)		600
Time step		200

PMOSFET Vt (N+ Poly)		P0000039.2D	P0000039.3D
Basic			
Mesh			
Number of X-nodes		51	
Number of Y-nodes		50	
Domain X size		1.5	
Domain Y size (um)		2	
Domain Z size (um)		1	
First Y mesh step size (um)		0.01	
Remesh		3	
Numerical solution parameters			
Numerical doping data			
Numerical doping data		P0000050.3D	
Electrodes			
Ohmic electrode			
Electrode name		Bulk	
Electrode number		1	
Electrode location		2	
Electrode left edge (um)		0	
Electrode right edge (um)		1.5	
Ohmic electrode			
Electrode name		Source	
Electrode number		2	
Electrode location		1	
Electrode left edge (um)		0	
Electrode right edge (um)		0.2	
Gate electrode			
Electrode name		Gate	
Electrode number		3	
Electrode location		1	
Electrode left edge		0.5	
Electrode right edge		1	
Gate oxide thickness		0.015	
Location of interface charge		1e-2	
Width of interface charge		1e-2	
Interface charge density		2e+11	
Peak interface charge density		0	
Electron recombination velocity		1e-15	
Hole recombination velocity		1e-15	
Metal work function		4.12	
Ohmic electrode			
Electrode name		Drain	
Electrode number		4	
Electrode location		1	
Electrode left edge (um)		1.3	
Electrode right edge (um)		1.5	
IV-data			
IV-data			
IV-curve label		Id vs Vg	
Ramped contact number		4	
Initial voltage for contact #2		0	
Initial voltage for contact #1		0	
Number of IV-points to compute		50	
Initial voltage for contact #4		0	
Initial voltage for contact #3		-5	
Voltage step size [V]		-5	

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