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Development and modeling of a low temperature thin-film CMOS on glass

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DEVELOPMENT AND MODELING OF A LOW TEMPERATURE THIN-FILM CMOS ON GLASS

By

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ABSTRACT

The push to develop integrated systems using thin-film transistors (TFT) on insulating substrates (i.e. glass) has always been limited due to low-mobility semiconducting films such as amorphous and polycrystalline silicon. Corning Incorporated is developing a new substrate material known as silicon-on-glass (SiOG). It is intrinsically better than amorphous and polycrystalline silicon materials due to its single crystal nature of the silicon film. This however does not mitigate the challenges associated with low-temperature CMOS process and fabrication.

The first generation of TFTs fabricated at RIT showed the potential of SiOG as a viable substrate material, but were plagued by considerable short comings such as high leakage and low transconductance. As part of this study, refinements to TFT processing on SiOG have demonstrated significant improvement to TFT performance and uniformity, showing increase transconductanace/mobility, lower subthreshold swing, tighter V_T distributions, and near symmetrical NFET and PFET operation about 0 V. With these improvements minimal steps have been added to the manufacturing process, keeping simple and adoptable by the flat panel display (FPD) industry. Device modeling clearly demonstrates the key areas important to electrical operation, such as dopant activation, interface charge/trap reduction, and workfunction engineering. It addition, modeling and simulation have helped to explain the governing physics of device operation explaining non-ideal effects such as gate induced drain leakage (GIDL) and various mobility degradation mechanism. An overview of device design, process refinements and device operation is presented. Process modifications and resulting benefits are discussed along with CMOS integration on SiOG.

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CHAPTER 1

INTRODUCTION

1.1 Motivation for TFT Advancement

In the past decade an increased use of thin-film transistors (TFTs) has orcured in display applications. TFT liquid crystal displays (LCD) and organic light emitting diodes (OLED) are now found in a variety of fields ranging from large format applications for televisions and monitors to portable applications for cells phones and digital cameras.

In early LCD technology, passive matrix addressing was used to address each segment or pixel of the display. These displays were small and low resolution. In the late 1980s attempts to make higher resolution displays were made, however these displays were plagued by a slow response time and poor contrast. To further increase the contrast, resolution and size of LCD displays, active matrix addressing was implemented to address pixels more quickly without the sacrifice of image quality. Active matrix LCD (AMLCD) and Active Matrix OLED (AMOLED) displays utilize transistors fabricated in a semiconductor material on the backplane of a flat panel display (FPD). Thus, addressing is done to each pixel transistor rather than to pixel capacitors directly, drastically decreasing response time, especially in larger format displays [1].

Today in active matrix displays, the pixels themselves consist of the pixel capacitor, color filters and pixel driving transistor. All of the driving electronics are off panel and

are fabricated in traditional bulk silicon CMOS technologies. The dominant TFT transistor technologies today are based in either amorphous silicon (a-Si) or polycrystalline silicon (poly-Si). The transistor performance characteristics of these technologies are such that they can easily meet the requirements for controlling pixels [2], however, they do not deliver acceptable performance for addressing and image processing. A push is being made to further integrate electronics on FPDs. The poor performance of devices fabricated in a-Si does not allow for any integrated electronics. Lower level integration of electronics using long grain polysilicon films has shown some success. However, the integration using poly-Si has been limited to simple circuits such as row and column drivers and some small timing circuits [3].

1.2 Systems-on-Glass Technology Today

In FPD industry, there is a push to integrate more circuitry on the display itself, particularly for small format displays. The goal of system on panel is to develop a fully integrated display with all required circuitry on the display substrate; data and power being the only external connections. Technologies utilizing a-Si and poly-Si do not offer acceptable transistor performance for complex circuitry.

Transistors fabricated in a-Si are plagued by low mobility due to the non-crystalline nature of the film. Though high device uniformity can be fabricated with this film, the device performance basically limits the use of transistor fabricated to pixel drivers. On the other hand, low temperature polysilicon (LTPS) material does offer potentially higher performing transistor that could be use for advanced integrated circuitry, however the benefit of this added performance is limited to poor uniformity. By using SiOG material

technology, where the silicon layer is single crystal, transistor performing close to that fabricated in bulk silicon can be fabricated, offering greater potential for integration.

1.3 Thin-film Transistor Designs and Material Systems

The development of thin-film transistor technology has been around since the early 1960s. The first TFT was fabricated using a CdS semiconductor film and gold contacts on glass [4]. Since that time many material systems have been developed, including organic semiconductors. However, TFT technology is currently dominated by a few material systems: amorphous and polycrystalline silicon, which are currently used in the FPD industry, and organics which is currently a popular area of research. A brief overview of these systems is given in Chapter 2 along with background done at work at RIT on a new crystalline silicon-on-glass material system.

1.4 Partnership with Corning

Thin film display is an area where research activities are rapidly advancing the technology. The process development and characterization work required for this project match exceedingly well with the teaching and research interests of the Microelectronic Engineering Department.

In addition to being a leader in the telecommunication industry, Corning leads the industry in providing high quality glass to flat panel display manufacturers. Corning has expressed an interest in researching the capabilities of their semiconductor on glass substrate. With RIT's current tooling and CMOS process experience, a process will be engineered for Corning's substrate. Corning's new substrate material consists of a single crystalline silicon film on a alkaline earth boro-aluminosilicate glass substrate. The

silicon film is bonded to the glass substrate using proprietary techniques and is of extremely low defect level. Such material is targeted for applications requiring larger area electronics, particularly the FPD industry.

Corning is interested in investigating the influence of thermal processing effects on the substrate. The devices will be processed within the material's thermal strain limit beyond which the glass structure changes. However, temperature cycles will cause changes in dimensions of the substrate, affecting global and local registration. Proprietary details of Corning's substrate are not public knowledge and will not be discussed in this document.

1.5 Work Covered by This Document

The primary focus of this study was to investigate potential improvements to NFET and PFET devices fabricated in the SiOG material system with minimal increase in fabrication complexity. Along with this, a more complete description of SiOG TFT operation is given, a continuation from that in reference [5]. Finally, a potential process is discussed, designed to help advanced channel length scaling on SiOG.

CHAPTER 2

MATERIAL SYSTEMS FOR SILICON-BASED TRANSISTORS ON GLASS

2.1 Material Systems

Since the 1970's amorphous silicon has been used for FPD displays on glass, and has remained the dominate choice for larger format displays due to its uniform performance and the low cost of transistor fabrication. Throughout the 1980's and 1990's significant development in low temperature polysilicon (LTPS) films on glass had been made. In the late 1990's to present, LTPS has become more commonly found in small format displays. LTPS has allowed for higher integration and the implementation of CMOS. However, issues with uniformity still do remain and more complex processing to improve off-state conditions is required [1].

Silicon-on-glass (SiOG) substrates, being a single crystalline silicon (c-Si) film should offer higher performance than a-Si and LTPS materials and provide good uniformity and simpler transistor fabrication. A schematic comparing the transfer characteristics of transistors from each thin-film silicon material system is shown Figure 1. The on-state of c-Si on glass is better than both a-Si and LTPS due to the single crystalline nature of the film. The subthreshold region is characterized as having a very steep slope and the off-state region has very low level leakage level, comparable to a-Si, if not better.

Subthreshold I_D-V_G
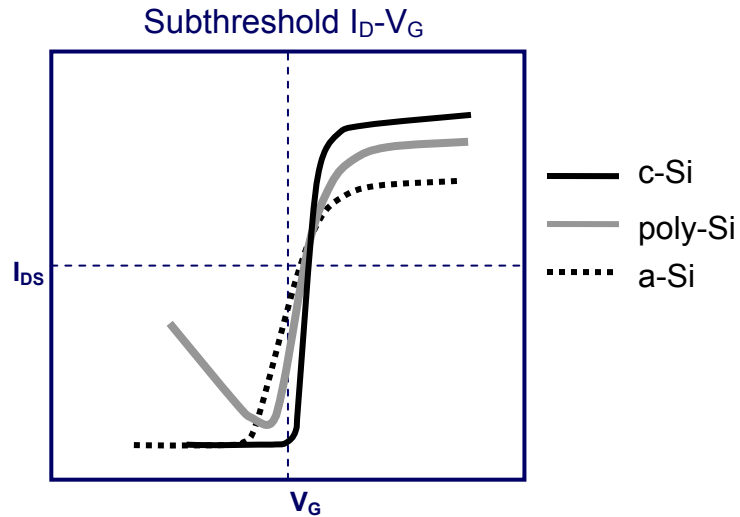
Figure 1. Schematic of the transfer characteristic for a-Si, poly-Si and crystalline silicon thin-film material systems. SiOG could potentially off higher current drive and less leakage for transistor of the same geometry.

The benefits of having c-Si TFTs on glass as opposed to other material systems is that transistors of smaller geometry can offer the same or better performance. Smaller transistor allow for displays with higher pixel aperture ratios, which leads to a host of other improved viewing characteristics. The benefits of a smaller transistor also allow for high integration; moving more circuitry onto the glass.

2.2 Amorphous Silicon

In the mid to late 1970's amorphous silicon became a viable option for the development of thin-film transistors on glass. It had been know that amorphous silicon could be deposited at low temperatures via chemical vapor deposition techniques. It was not until a method for doping a-Si via glow discharge did its use for thin-film devices take off [6]. Hydrogen passivated amorphous silicon could be doped; the hydrogen can tie up dangling bonds which are associated with high densities of mid-gap states.

Though other materials at the time of the introduction a-Si for TFTs were showing more promise, such as higher mobilities and better I_{on}/I_{off} ratios, refinements in processing device structure and layout led to more efficient production of a-Si TFTs. These refinements led to excellent off-sate current characteristics with adequate on-state drive current and switching capabilities for pixel drivers despite its very low carrier mobility ($\sim$1cm^2/V-sec or less) [7]. A significant advantage with amorphous silicon is that it can be easily deposited on larger area substrates with superb uniformity. This makes it very attractive from an industrial investment point of view as almost any company could setup a production line for a-Si and have working, reproducible devices in very few processing steps.

Devices fabricated in a-Si are typically bottom gate structures as seen in Figure 2. A gate material, such as Al or ITO, is first deposited and patterned. A gate dielectric is deposited, such as SiO_2 or Si_xN_y, via PECVD or LPCVD at relatively low temperatures (*i.e.* below 550ºC). Silicon is deposited via LPCVD or PECVD at low temperatures, ranging from anywhere between 150ºC to 550ºC. This is often done in the same chamber as the gate dielectric deposition without breaking vacuum. Another layer of in-situ doped silicon follows which is for the source and drain region. Finally, a layer of metal is deposited to make contact to the source and drain. The metal is then patterned and used as etch mask for the pattering of the channel region (the doped silicon). Figure 2 shows an example of a complete structure, [8],[9],[10].

Since there is no structure to a-Si film, many of the silicon atoms have dangling bonds. The performance of a-Si films can be improved through hydrogenation of the film. By subjecting the amorphous film to a hydrogen plasma, or a lower temperature anneal in

hydrogen, many of the dangling bonds can be passivated by forming a H-Si bond. This changes the effective band gap of the material and reduces the number of defect states in the film, particularly between the effective valance and conduction bands [11].
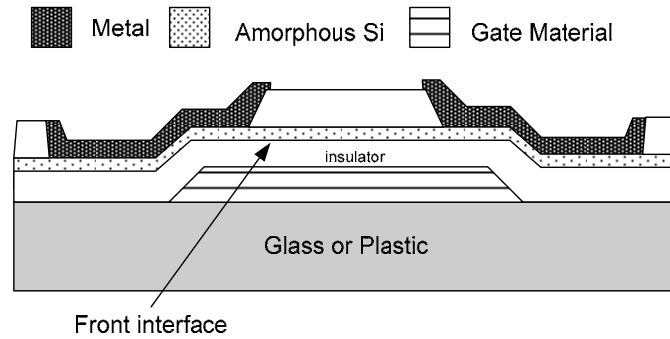
Figure 2. Cross-section of a typical bottom gate amorphous thin film transistor.

2.3 Polycrystalline Silicon

Poly-Si TFT devices are often seen in both top gate and bottom gate configurations. Top gate fabrication is a process very similar to that of conventional lateral MOSFET devices in Figure 3 whereas bottom gate processing is similar to what was described above for the amorphous silicon TFTs. The advantage of poly-Si TFTs fabrication is that grain engineering is possible. To further enhance the performance of poly-Si TFTs, the reduction of grain boundaries is necessary in the active film layer. This can be done using one of the following techniques: solid-phase crystallization (SPC), metal induced lateral crystallization (MILC) [12] or Excimer laser crystallization (ELC) [13]. For SPC, first an amorphous silicon film is deposited via CVD, below 600ºC. The film then can be converted to a polycrystalline structure by annealing it in an inert ambient for a prolong period of time, 10-100 hours, around 530ºC to 600ºC [12]. Depending on deposition

chemistries, temperature, and annealing temperature, grain sizes upwards of 3-5 μm have been reported [13]. Though the grain size is fairly large, a high density of localized states is not only present at the grain boundaries, but also within the grains themselves. Thus the electron field-effect mobility of 40-70 cm^2/V-s is the upper limit that has been achieved with this method.

An alternative for further enhancement of poly-Si performance is ELC. Excimer lasers output UV radiation wavelengths (XeCl lasers output at 308 nm) for which silicon has high absorption. This allows the silicon to be melted without significant heating of the substrate. Thus re-crystallization at temperatures below 400ºC can be accomplished [14]. Because the process is a melt-and-re-growth, there are few defects within the grains themselves. ELC allows for super lateral growth (SLG) to occur; this occurs when all of the silicon is melted excepted for a few small crystals clusters. Thus these clusters act as crystal seeds and crystalline re-growth occurs laterally around the clusters. The growth continues until neighboring grains impinge on each other. Gain sizes >1μm have been achieved with field effect mobilities above 200 cm^2/V-s [14].

The best performance increase out of all the crystallization techniques has been reported for MILC. Field effect electron mobilities as high as 430 cm^2/V-s have been achieved [15]. MILC is done by patterning "seeding" areas on top of an amorphous silicon film. A thin metal layer, such as Ni, is then deposited over the seeding windows. MILC is then carried out in a furnace between 500ºC and 600ºC for a long period of time (>10 hours) in an inert ambient. Nickel silicide is formed when Ni contacts the silicon. This acts as a seed and the surrounding silicon can orient itself to it. Long grains can be achieved with this process; however the width can be somewhat narrow. To increase the

width of the grains as well and length, once the initial MILC has occurred, a post high temperature anneal (>900ºC) can be performed. This will help to increase the width of the poly-Si grains. However, because this is a high temperature process is not very compatible with many glass or plastic substrates.

2.4 SOI Technology

While silicon on insulator (SOI) technology is technically a thin film platform, it does offer a major advantage over conventional TFT technologies in that processing temperature is not limited by a glass substrate. The semiconductor industry has adopted SOI technology in production for many microelectronic applications because of its advantages over bulk processing.   The reduced junction capacitance, from reduced source/drain junction area, increases the maximum frequency of operation while in turn help to reduce power consumption.   CMOS latch-up is eliminated with SOI, as each device is totally isolated.   Improved isolation also enables the integration of high frequency passive components.
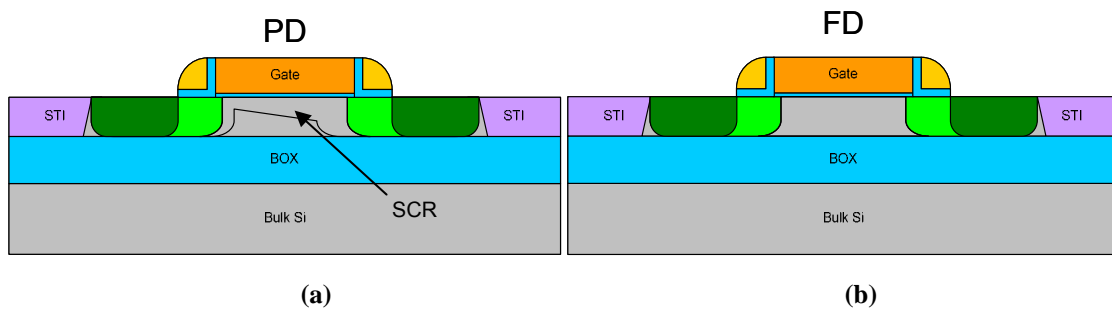
Figure 3. Schematic of SOI device showing (a) partially depleted device and (b) a fully depleted device

With SOI, depending on the silicon thickness the body regions of these devices can be either partially depleted (PD) or fully depleted (FD). An SOI device is fully depleted

when the entire body thickness is depleted of carriers, and the depletion charge is constant and will not extend further. Partially depleted devices are similar to bulk silicon devices in that there is body under the gate that is not depleted [5]. Figure 3 portrays cross-sectional vies of (a) a partially depleted and (b) a fully depleted transistor.

An advantage of PD devices is that well established techniques such as retrograde wells, halo implants, and S/D extensions can be used to control short channel effects. However without a body contact, the body of a PD device is electrically floating. Body contacts are not desirable as they take up valuable real-estate. During normal operation the body will charge and discharge, which occurs by generation and recombination of carriers created via impact ionization at the drain end of the channel. This sets the body at a particular voltage, thus V_{BS} and V_{BD} will not be the expected values; this is known as the history effect [16]. Several adverse effects on device behavior can occur. The history effect causes a variation in gate delay. Body charging can forward bias the body-source pn junction resulting in a parasitic shunt bipolar transistor. The parasitic BJT effectively lowers the SOI device threshold voltage. The floating body also causes drain induced barrier lowering (DIBL) to increase; as the body charge increases, V_T decreases causing additional barrier lowering. Body charging can also be attributed to gate induced drain leakage (GIDL); band to band tunneling between the body and drain in the off state [17].

FD SOI devices offer several advantages over PD SOI devices, including steeper subthreshold slope (better off-state characteristics), larger saturation current at the same applied bias, reduced power consumption at a lower operating voltage, and no floating body effects. Fully depleted SOI transistors do exhibit increased short channel effects,

however these can be suppressed if the silicon film thickness is much smaller than the depletion depth [18].

2.5 SiOG Material Technology

The potential of SiOG substrates is that they contain a thin, single crystalline silicon film similar to that found in SOI. The application of SiOG is in large area electronics which is typically the realm of a-Si and polycrystalline silicon technologies. It offers a very high quality silicon semiconductor, but is constrained in processing ability due to temperature limitations of the glass. This combination of properties makes designing MOSFET transistors in SiOG different from both traditional TFT and SOI material systems. The following chapters discuss design options for incorporating MOSFETs on SiOG that have high performance but can be process within the thermal constraints of the glass substrate. Implementation and fabrication of transistor on SiOG is first discussed in Chapter 3 followed by design aspects in Chapter 4.

CHAPTER 3

SiOG TFT DESIGN AND LOW-TEMPERATURE CMOS

3.1 Transistor Device Design

To date, thin-film transistors built on SiOG substrates have been done so in P-type silicon films. Because of low temperature constraints set forth by the glass substrate, traditional bulk CMOS processing technologies such as LOCOS, single or twin-wells processes, etc., are very difficult to integrate and are not compatible with conventional FPD industry processing techniques. However, even with these constraints, CMOS on SiOG substrates is possible using relatively simple processing techniques common in both IC and FPD micro-fabrication.

Bulk silicon MOS field-effect transistors typically consist of four terminals: source, drain, gate, and substrate/well electrodes. A four terminal transistor can be designed and fabricated on SiOG, however it is not necessarily practical because the silicon film is so thin. For a one-to-one transfer of a process technology from a bulk IC CMOS to a thin-film SOI or SiOG substrate, the transistor would have to be designed such that it operated as partially a depleted device [19]. If the device is designed to operate with the body region partially depleted, floating body effects become an issue [20], especially at high switching speeds, if no body contact terminal is established. The body contact terminal is needed to define the body potential as seen in Figure 4A. In bulk silicon, this terminal is

well defined, and the associated penalty is relatively small in comparison to the benefits. However, as the body of the silicon film becomes thin, the parasitic resistance and capacitance contributed by the body terminal start to become significant. As the silicon and body region become thinner and thinner, the resistance of the body contact terminal goes up. This increase in resistance increases the RC delay and thus the switching speed at which the transistor operates. Eventually the body contact can not move charge out of the body region effectively and parasitic bipolar effects can become an issue in the operation of the partially depleted transistor [21].
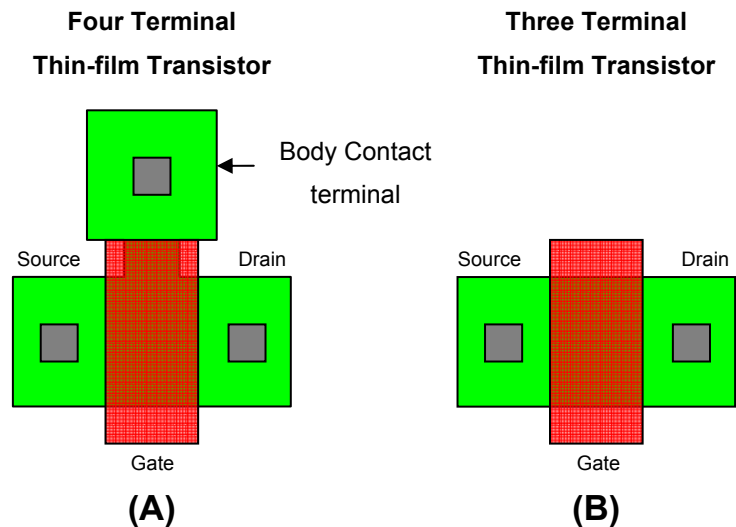
Figure 4. Schematic representation of a (A) four terminal and (B) three terminal thin-film transistor layouts. The body contact of the four terminal transistor is of the same type of dopant as the body of the transistor. Because of the thin film nature of the substrate, the body contact needs to be made laterally on the surface with a terminal that connects the contact and the body region and is protect from any implants that would change its type. By comparison, the three terminal transistor is much simpler and compact.

To reduced and/or eliminate the possibly of floating effects in a thin-film MOS transistor, a three terminal transistor design (Figure 4B) can be used such that the body of the transistor becomes fully depleted. This helps to eliminate the floating body effects

and there are no added parasitics associated with a body terminal. To design such a transistor, appropriate gate dielectric thickness, gate workfunction silicon thickness and body dopant concentration are required. Specific details about these parameters will be discussed in Chapter 4.

Without using wells or other counter doping techniques, NFETs and PFETs can be fabricated. The NFET is of the traditional sort; having degenerately doped N-type source and drain regions in a P-type film. It is an inversion mode device, forming an N-channel when a positive bias is applied to the gate electrode. Its threshold voltage is such that it is consistent with enhancement mode operation. The NFET on SiOG could be designed to operate as either a partially depleted or a fully depleted device. Because the silicon film used for this study was ≤ 200 nm, and lightly doped, the body contact on a four terminal transistor design was essentially useless and a three terminal fully-depleted design was pursued.

The PFET is an accumulation mode device. It is built in a P-type film with degenerately doped P-type source and drain regions. A comparison of an inversion mode and an accumulation mode transistor are shown in Figure 5. The accumulation mode transistor conducts current when a negative bias is applied to the gate electrode, forming an accumulation channel of majority carriers. The device is off when the body region of the transistor is fully depleted, of free carriers, impeding conduction from the source to drain. The bias conditions at which the device turns on and off is a function of many parameters and will be explained further in Chapter 4.
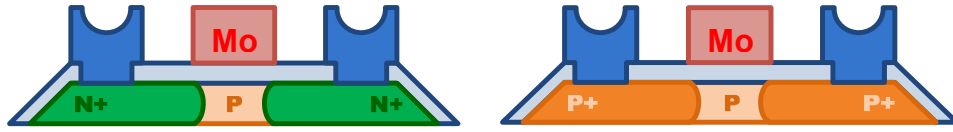
Figure 5. Cross-section schematics of SiOG NFET and PFET devices

3.2 SiOG Transistor Fabrication Process

Both NFET and PFET devices have been fabricated on SiOG, SOI and bulk substrates. Because of temperature constraints of the glass [22] all processing was done at temperatures ≤ 600 °C. The original process stated in [23] was modified for improved transistor performance by adding several cleaning steps and refinements in material deposition and etching steps; the effects on device performance will be discussed in Chapter 5.

To monitor the fabrication process, SOI and bulk silicon wafers were used with known material parameters (resistivity, crystallinity, thickness, etc.). These wafers were processed using the exact same steps as the SiOG substrates. Because of the well understood nature of these substrates, any process flaws could be extracted independent of the substrate material without being confounded with the substrate fabrication conditions of SiOG. Also the SOI substrate was used as a "best-case" example of thin-film CMOS fabricated at low temperatures in a crystalline film. The SOI substrate is known to be of high single crystal quality with exceeding low defect conditions. The following paragraphs provide a description of the low-temperature CMOS fabrication process used to make transistors and other semiconductor devices on SiOG substrates. A full step-by-step process description is listed in Appendix A.

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Prior to fabrication, the SiOG substrates are cleaned in a 50:1 H_2O:H_2SO_4 piranha bath for ten minutes at 130 ºC. The piranha bath is excellent for removal of organic material and also removes metal contaminates [24, 25]. Many micro-fabrication tools are not equipped to handle transparent substrates. To prepare SiOG for tool handling, a protective SiO_2 film of 1000 Å was first deposited over the Si film via LPCVD. Then a 5000 Å molybdenum film was put on the backside of the SiOG substrate to make it opaque and to enable capacitive signal detection for tool handling systems. Molybdenum was chosen for this purpose because of its ability to withstand subsequent process at temperatures $\geq$ 600 °C via PECVD. To protect this molybdenum film from wet chemical processing, 2 μm SiO_2 were deposited over it. Instead of backside metallization, the SOI and bulk wafers received backside implants to allow for ohmic contact formation; important for electrical characteization.

Active level lithography was done and Si mesas were etched using a DC plasma with SF_6 chemistry. All silicon was etched between the mesas down to the glass substrate. The etch was engineered such that the edge of the mesas had a tapper of 60º helping to ensure conformal step coverage for subsequently deposited films. The substrates were then cleaned in preparation for the gate dielectric deposition. Cleaning consists of a 10 minute immersion in a 50:1 H_2O:H_2SO_4 piranha bath followed by a 10 minute immersion in 5:1:1 H_2O:H_2O_2:HCl bath. The importance of this cleaning process is discussed in Chapter 5. A SiO_2 film was used the gate dielectric for both the NFETs and PFETs. It was deposited via LPCVD at 425 °C at a target thickness of 500 Å. A molybdenum film was then deposited over this, via RF sputtering, patterned and reactive-ion etched to form the gate electrode.

To allow for a self-aligned process the molybdenum gate blocks the source/drain implant. Phosphorus was used for the NFET source drain implants. At high doses phosphorus will self-amorphize the silicon lattice, allowing for reasonable levels of activation at 600°C [26]. To achieve highly doped n+ source/drain regions, a 4×10^{15}cm^{-2} ^{31}P dose was implanted at 110 keV. To achieve sufficiently doped PFET source/drain regions, a ^{19}F & ^{11}B co-implant was required. A fluorine dose of 3×10^{15} cm^{-2} was implanted at 70 keV to cause pre-amorphization, followed by a 4×10^{15} cm^{-2} boron implant at 35 keV. All implants were done through the 100 nm screening SiO_2 layer which spread the implant profile throughout the entire thickness of the silicon film; allowing the source and drain regions to be more uniformly doped from the front surface to the back interface.

Following the n$^+$ and p$^+$ implants, an LPCVD SiO_2 inter-level dielectric (ILD) was deposited. An anneal at 600 °C for two hours in a N_2 ambient was performed to activate the source drain regions as well as improve the insulating characteristics of the ILD and gate dielectric. Contacts were then patterned and etched, followed by aluminum deposition, pattern and etch. Finally, a sinter at 425 °C in forming gas (5% H_2 in N_2) was done for 15 minutes to complete the fabrication process. A representative profile of a completed transistor is shown in Figure 6.
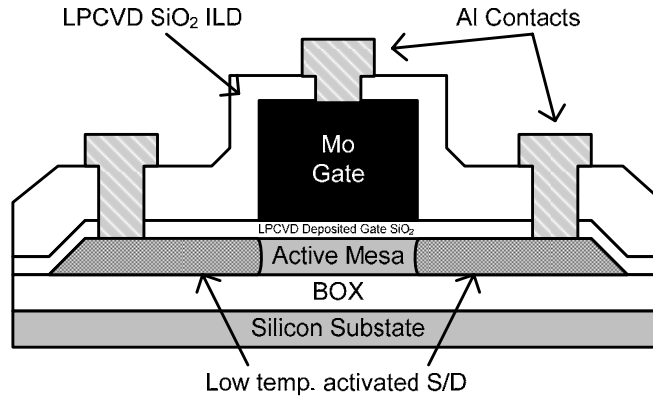
Figure 6. Cross-section of a low temperature fabricated SOI FET using deposited dielectric films. For CMOS operation, the NFET and PFET were isolated via a Si mesa etch.

3.3 SiOG Transistor Operation

This section offers a brief summary of the operation of the NFET and PFET devices on SiOG with a full description of device behavior and the corresponding physics given in Chapters 4 and 6. The described low-temperature CMOS process has been verified on both SiOG and SIMOX SOI substrates, with both NFETs and PFETs demonstrating enhancement mode threshold voltages [5]. Device isolation is provided by silicon mesa active regions. The NFET is a surface channel device. SiOG NFETs exhibit excellent characteristics with a low subthreshold swing of ~100 mV/dec and a high electron field effect mobility of >500 cm^2/Vsec. In the saturation mode of operation some gate induced leakage is observed, which may be enhanced by possible low junction integrity. SOI NFETs fabricated in conjunction with SiOG show subthreshold swings around 85 mV/dec and field effect mobilities >700 cm^2/Vsec.

The PFET is fabricated in a p-type substrate, and thus operates as an accumulation mode device with turn-on characteristic similar to that found in buried channel transistors

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[27]. When the device is off, the gate must deplete the body region of carriers in order for no current to flow. The SiOG PFET field-effect hole mobility extracted was 220 cm^2/Vsec on SOI wafers. The device shows a drain bias dependant subthreshold swing; 100 mV/dec in the linear regime and ~150 mV/dec in the saturation regime of operation. The reason for the large discrepancy is due to limited gate control at biases around 0V. The larger bias on the drain changes how the body region of the device depletes, causing it to turn of more gradually. Similar SOI PFETs show field effect mobilities of 290 cm^2/Vsec and subthreshold swings on the order of 100 mV/dec.

Fabrication work at RIT has led to the development of high performance thin-film transistors on glass. Fabrication and process development has given a competent understating of the both limitations and potential of the SiOG substrate. This understanding aids in designing transistor on SiOG and is discussed in the next chapter.

CHAPTER 4

MODELING & SIMULATION OF SIOG THIN-FILM TRANSISTOR CURRENT-VOLTAGE BEHAVIOR

4.1 Design Space

There are many parameters for consideration when designing thin-film transistors on SiOG substrates. Parameters used in the design and engineering of conventional bulk transistors apply with the addition of several others due to the thin-film and low temperature regimes. This chapter discusses the thin-film transistor design space using modeling and numerical simulation. These tools are used to further enhanced the physical understanding of the operation of the NFET and PFET devices on SiOG substrates.

Table 1 list several basic design parameters for NFET and PFET transistors. These design parameters define the transistor operating characteristics. This includes things such as threshold voltage, drive current, off-state leakage current, subthreshold swing, transconductance, etc. While many similarities do exist between bulk and crystalline thin-film transistor design, there are slight differences that can have a significant impact on how the device operates in either regime. The added challenges when designing MOSFETs on SiOG are that silicon thickness needs to be taken into consideration as well as the potential lack of a body contact resulting in a floating body potential.

	Parameter	Material System
1.	Body / Well Doping Concentration	Bulk, SiOG, SOI
2.	Gate insulator type and thickness	Bulk, SiOG, SOI
3.	Source/Drain doping concentration	Bulk, SiOG, SOI
4.	Source/Drain Junction Depth	Bulk, SiOG, SOI
5.	Channel Length and Width	Bulk, SiOG, SOI
6.	Gate Metal Work Function	Bulk, SiOG, SOI
7.	Source/Drain Contact Metal	Bulk, SiOG, SOI
8.	Body Potential	Bulk, SOI (cap.)
9.	Silicon Thickness	SiOG, SOI

Table 1. Basic Design parameters for NMOSFETs and PMOSFETs

One of the most fundamental parameters in any MOSFET design is the workfunction of the of the gate material. When designing a thin film transistor that is fully depleted versus partially depleted, an understanding of what the depletion width induced by the gate is necessary for a particular bias and doping scheme as well as a maximum silicon thickness. Designing a process to fabricate thin-film CMOS on SiOG substrates with self-aligned source and drain regions requires, a gate material that is able to block boron and phosphorus implants, and is compatible with subsequent processing at 600 °C. Doped polycrystalline silicon would be the first choice as a material that can meet these needs. Using polycrystalline silicon would allow for a dual workfunction process allowing maximum tunability for both the NFET and PFET threshold voltages independent of each other. However, to dope polysilicon via implant and anneal it at ≤600 °C does not allow for efficient activation. Only a few percent of the dopant introduced will fill lattice sites and the other will segregate at grain boundaries creating a high resistance material and a possible non-uniform workfunction across the substrate [**Error! Bookmark not**

defined.]. In situ doped polycrystalline silicon is an option to avoid this, but was not available and it was not considered a practical option for TFTs.

To overcome the problems associated with polycrystalline silicon, a molybdenum gate metal was chosen instead. It is thermally stable at temperatures greater than 900 °C [28] and has a near mid-gap work function 4.53 eV [29] (mid-gap is 4.6 eV). Tunability of the molybdenum metal work function has been reported in [30] but was not explored in this study. Having a mid-gap metal work function allows for the design of symmetric CMOS about a 0 V (V_{GS}) operating point without adding significant extra processing steps to compensate the complementary device.

For the thin-film CMOS transistors, a gate oxide thickness of 500 Å was used [5]. Designing a fully depleted or partially depleted TFT requires a good understanding of how the gate electrode depletes the body region. Figure 7 show the simulation of the depletion width caused by a zero-bias gate electrode at various body doping and metal workfunction levels for an SiO_2 gate dielectric 500 Å thick. The depletion width shown is that which would occur in a bulk silicon film. For a TFT to be fully depleted, the silicon film thickness would have to be equal to or less than the bulk depletion with induced by the gate electrode at 0 V.

As shown in Figure 7 a maximum depletion width occurs between $1 \times 10^{14} \, cm^{-3}$ and $2 \times 10^{14} \, cm^{-3}$ for a workfunction value of 4.5 eV. This maximum and reduction of the depletion width for dopant concentrations less than $1 \times 10^{14} \, cm^{-3}$ is non-intuitive and can be explained by the dependence of surface potential with transistor body doping concentration. For a mathematical explanation refer to Appendix B.

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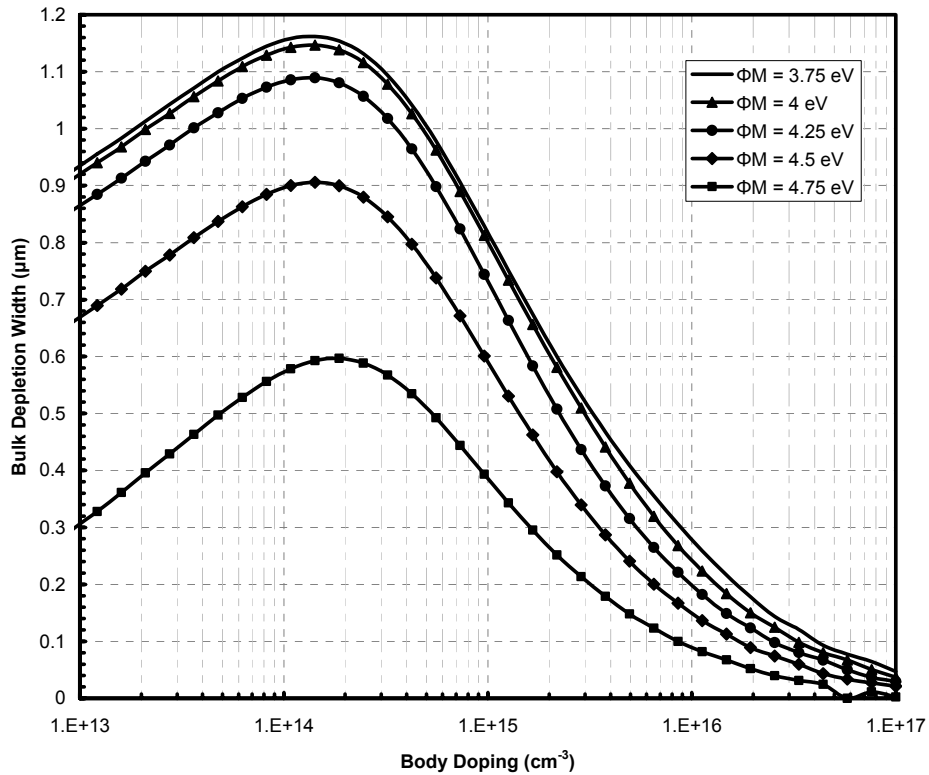
Figure 7. The effect on body doping and gate metal workfunction on the induced depletion width at $V_{GS} = 0$ V. The maximum depletion with occurs between 1×10^{14} and 2×10^{14} cm^{-3}. Boron concentrations above or below this point cause the depletion width to decrease. At higher boron concentrations there are more dopant ions per unit volume to match charge on the gate and thus the field effect does not need to reach as far. For lower dopant concentrations

A practical range of doping considered for CMOS TFT fabrication on SiOG substrates is between 1×10^{15} and 5×10^{15} cm^{-3}. This allows for theoretical maximum silicon film thickness of between 0.25 and 0.6 μm respectively, and still supports a fully depleted body at 0 V gate bias. The majority of transistors in this study were fabricated on films of 0.2 μm, sufficiently thin to ensure fully depleted operation. Instances where this was not the case are indicated.

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4.2 Thin-Film SiOG NFET design

The thin-film NFET transistor design is similar to those found on a bulk or SOI substrate. Slight deviation from a bulk device design will be discussed. For a full description of conventional bulk, inversion mode NMOSFET transistor design, see reference [31].

The SiOG NFET is a top gate design utilizing an inversion channel and N-type source drain regions. While similar to that of NFETs found in bulk silicon process, extra consideration must be taken when designing a threshold voltage. As indicated in Figure 7, the depletion width induced by the gate field-effect can far exceed the thickness of the silicon film.

$$W_d = \sqrt{\frac{2\varepsilon_s\psi_{sa}}{qN_A}} \tag{1}$$

For the semiconductor to match the charge on the gate, inversion will occur earlier. Thus for a given gate dielectric thickness and body doping, the threshold voltage of a thin-film NFET will be lower than one on bulk silicon.

4.3 Thin-Film SiOG PFET design

There are many ways to implement a hole carrier transistor device on SiOG; some implementations require more design and process complexity than others. Keeping in mind that the development of SiOG is primarily for the FDP industry, an implementation of the PFET was designed such that the processing needed for it to operate was kept to a minimum. Thus an accumulation mode PFET (AMPFET) was designed and incorporated

into SiOG CMOS. Such a device cannot be fabricated in a bulk silicon wafer and requires a thin silicon film for it to operate as a field-effect transistor.

An accumulation mode transistor is one such that the source and drain regions are of the same type of semiconductor as the body region, and an accumulation of majority carriers form a low resistance layer connecting the source and drain. The accumulation mode transistor is characterized by having an enhancement mode biasing scheme to control both on and off-state current conduction. The semiconducting film needs to be sufficiently thin enough such that the gate electrode can fully deplete the body of the transistor, severing conduction between the source and drain. In the case of the SiOG PFET fabricated in this study, for this thesis, a P-type silicon film on glass was used with p^+ source and drain regions. With a negative V_{GS} the device is on; with a positive V_{GS} the device is considered off. Determining when the device on or off is controlled by the flatband voltage as in a conventional inversion mode transistor.

To ensure that the AM PFET is off with 0 V on the gate electrode, the body of the transistor must be fully depleted. The depletion width induced by the gate electrode is a function of several factors including body dopant concentration, gate dielectric permittivity and thickness, and metal gate workfunction as mentioned earlier. Figure 8 shows the simulated band diagrams for an AMPFET. In this case, a 200 nm silicon film doped 3×10^{15} cm^{-3} was used with a 50 nm SiO_2 gate dielectric and Molybdenum gate. With $V_G = 0$ V, the silicon film is fully depleted, with surface of the film slightly inverted. As the magnitude of V_G is increased such, that it is greater than the threshold voltage (*i.e.* $V_G > V_T = V_{FB}$), the bands shift and the film appears to be more p-type. As holes

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replenish the body region at the surface of the silicon film, an accumulation layer is formed as indicated by the increased band bending.
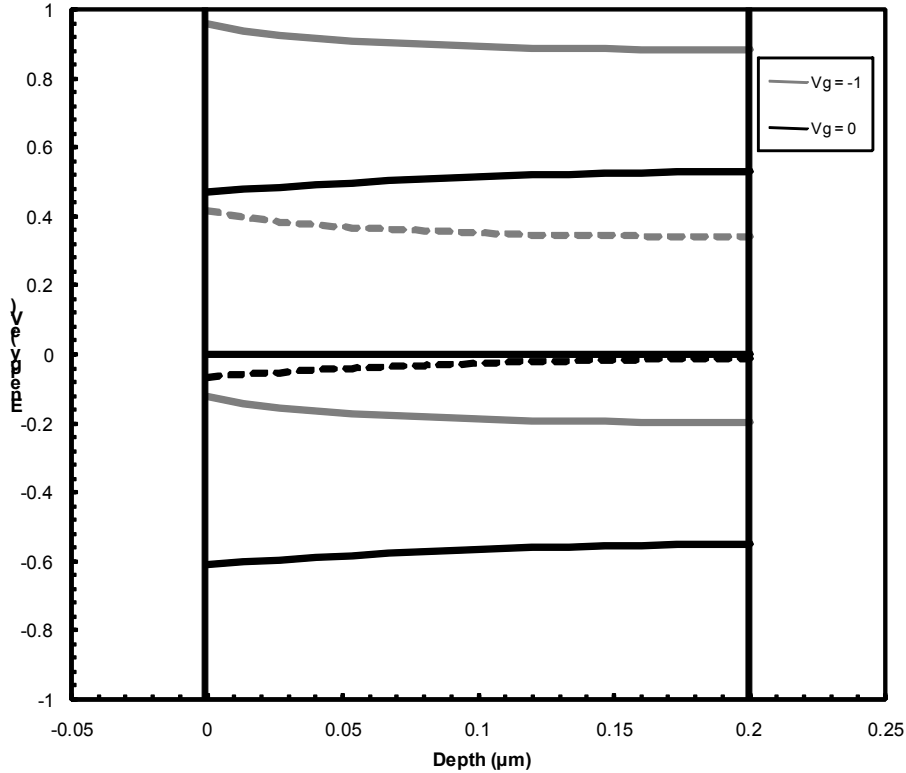
Figure 8. Band Diagrams for Thin-Film PFET on 200 nm p-type Silicon Film Gate Oxide: 50 nm, Molybdenum Gate ($\Phi_M = 4.53$ V), N_A: 3×10^{15} cm^{-3}

4.4 Thin-Film Transistors Designed on SiOG for CMOS

While modern CMOS manufacturing technology routinely produces transistors at critical dimensions below 100 nm, with ultra-thin gate oxide layers scaled well below 10 nm, TFT dimensions are usually more than an order of magnitude higher due to product needs, manufacturing limitations and yield-associated costs. In addition, a traditional CMOS process may easily exceed 25 photolithography steps, while TFT processes typically use 4–6 mask levels. Since fabrication process simplicity was a

primary design consideration, constraints imposed on CMOS TFT designs for SiOG substrates include employing a relatively thick deposited gate oxide thickness (50 nm), and the avoidance of threshold-voltage adjustment implants.

Since the devices are being built in a p-type silicon layer, the structural design of an NFET alone would normally be considered quite straightforward. The remaining design parameters include silicon film doping concentration (N_A), silicon film thickness (X_{Si}), and gate metal workfunction (Φ_M). The PFET has design considerations which impose specific constraints on these choices. The details of the PFET design and associated effects on the NFET operation are next discussed in order to clarify the choices for the remaining design parameters.
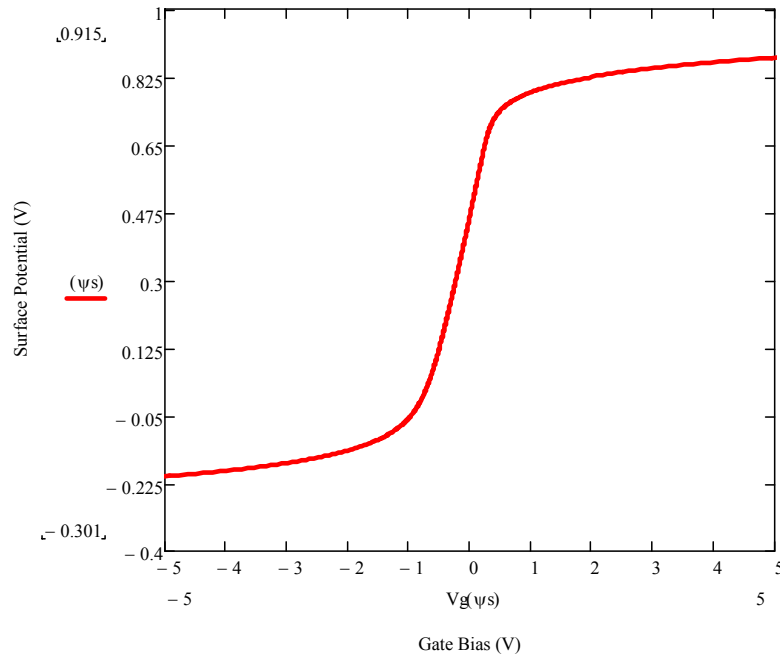
Figure 9. Silicon surface potential as a function of applied gate bias for p-type silicion, $N_A = 1 \times 10^{15}$ cm^{-3}, oxide thickness of 50 nm and a Mo gate (Φ_{MS}).

The NFET device currently implemented on SiOG substrates are similar to those designed in other material systems such as SOI. The transistor design consists of heavily doped n-type source/drain regions and a lightly doped p-type body region. Application of a positive gate bias will form an electron inversion layer, establishing a conductive pathway between the source and drain. The threshold voltage (V_T) is the gate bias which represents the onset of this inversion layer, and is established as the point at which the transistor is considered "on". An enhancement-mode NFET ($V_T > 0$) is achieved using an appropriate choice of N_A (boron) and Φ_M. The PFET device designed for SiOG CMOS implementation operates by depleting hole carriers in the off-state and accumulating hole carriers in the on-state in the p-type silicon layer. An accumulation-mode transistor has source and drain regions defined as the same electrical type as the body region; an accumulation of majority carriers forms a highly conductive region connecting the source and drain. Such a device requires a thin-film silicon device layer, and cannot be realized in a bulk silicon wafer due to lack of electrical isolation. The operation of an accumulation-mode PFET (AMPFET) has been previously described for SOI applications [32], however not in the context of CMOS integration.

In addition to being fabricated in the same p-type silicon layer, the same gate metal is used on SiOG PFETs and NFETs to avoid complex integration schemes. While the design window for N_A, Φ_M and X_{Si} is quite large for the NFET, the choice of an appropriate combination that will result in an enhancement-mode threshold ($V_T < 0$) with acceptable off-state performance is quite limited. For the AMPFET to be off with the gate electrode at zero-bias, a full depletion of hole carriers in the body region is required. The depletion width induced through a field-effect by the gate electrode at zero-bias is a

function of several factors including N_A, Φ_M, gate dielectric properties (permittivity and thickness), and charge that may exist at both the oxide-silicon and silicon-glass interfaces.

Choosing a silicon film doping to satisfy both the NFET and PFET in an SiOG CMOS, is not without its compromise. Figure 10 shows the range of silicon film thickness and doping at which both the NFET and PFET still have enhancement mode threshold voltages ($V_{Tn} > 0$ and $V_{Tp} < 0$), assuming no fixed or trap charge. For most of the devices considered in this work, a dopant concentration range between 1×10^{15} cm^{-3} and 3×10^{15} cm^{-3} was used as indicated by the boxed region in Figure 10. This favors a higher magnitude PFET threshold voltage than the NFET. This dopant range allows room for the NFET to be further adjusted with the addition of more dopant to increase the magnitude of the threshold voltage without influencing the PFET. Compensating the NFET device is more favorable because excess dopant would have lower impact on the electron mobility than the hole mobility.

Figure 11 shows the dependence of the extracted V_T of a simulated AMPFET with varying N_A at different values of X_{Si}, assuming a gate metal workfunction of molybdenum ($\Phi_M = 4.53$ eV), a gate oxide thickness of 50 nm, and neglecting interface charge. The AMPFET VT is most sensitive to changes in X_{Si} at higher doping concentrations, where operation is depletion mode. At N_A values below 10^{15} cm^{-3} the threshold voltage becomes relatively constant, converging towards the metal-semiconductor workfunction difference (Φ_{MS}) in order to establish a flatband condition, which can be considered analogous to the onset of inversion in the accumulation-mode device.
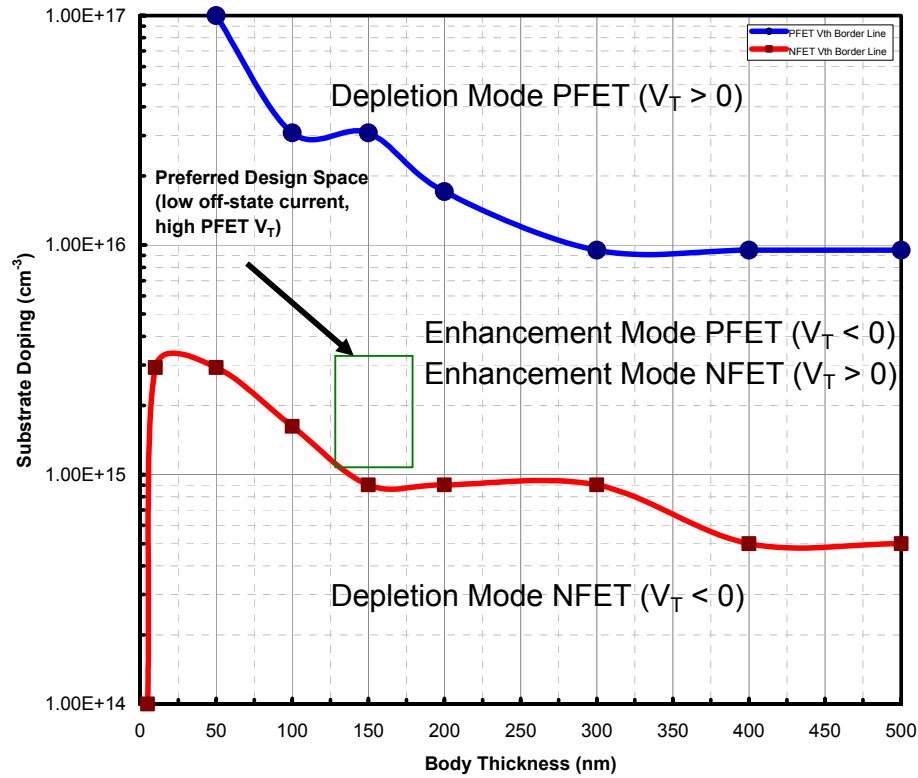
Figure 10. The delineation between enhancement and depletion mode threshold voltages for SiOG NFETs and PFETs. The region in the center of the plot indicated ranges of siliocon body thickness and substrate doping applicable for fabricating SiOG CMOS with enhancement mode threshold voltages on both Devices. The square indicates the preferred design space for CMOS utilizing a inversion mode NFET and an accumulation mode PFET. Working in this design space would increase the magnitude of the PFET threshold voltage and lower the NFET's. This is such that compensation could be considered later in processing to help raise the threshold voltage with a minimal impact on mobility lowering.. (For both devices: $X_{OX} = 50$ nm and $\Phi_M = 4.53$ eV)
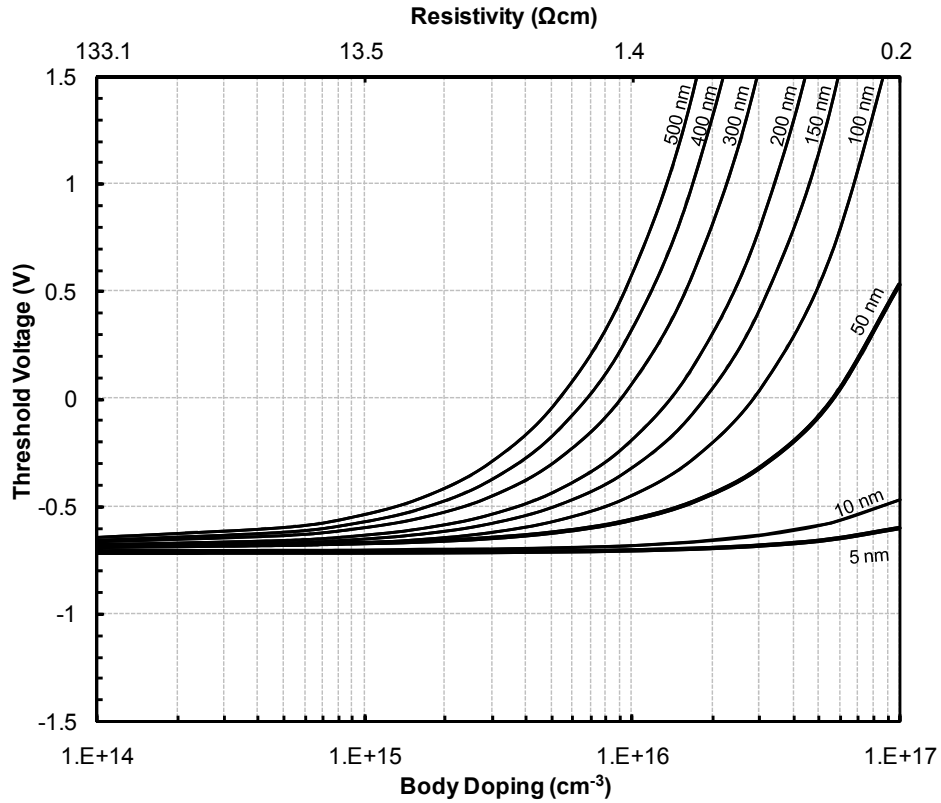
Figure 11 Simulation of the effects of body doping concentration and silicon film thickness on the linearly extroplated threshold voltage of a thin-film accumulation-mode PFET on glass. The threshold voltage is that from a linear extrapolation on an IDS vs. VGS plot. A negative (positive) threshold voltage denotes an enhancement (depletion) mode biasing scheme. A 50 nm gate oxide and molybdenum workfunction of 4.53 eV were used.

An enhancement-mode V_T by itself does not guarantee adequate subthreshold characteristics and off-state leakage current. The 2D numerical simulation of minimum current of an AMPFET transistor is show in Figure 12 with enhancement and depletion mode regions indicated. For a given film thickness and dopant concentration, the threshold voltage may appear to be enhancement mode, but the off-state characteristics would suggest that it is not functioning well. Obviously at high doping and high thickness the off-state leakage current should be relatively high; for thin thickness and low doping levels, the leakage should be low.

Minimum Off-State Current for Thin-Film PFET on P-type Silicon Film
Gate Oxide: 500Å, Molybdenum Gate (Φ_M = 4.53V), Linear Regime
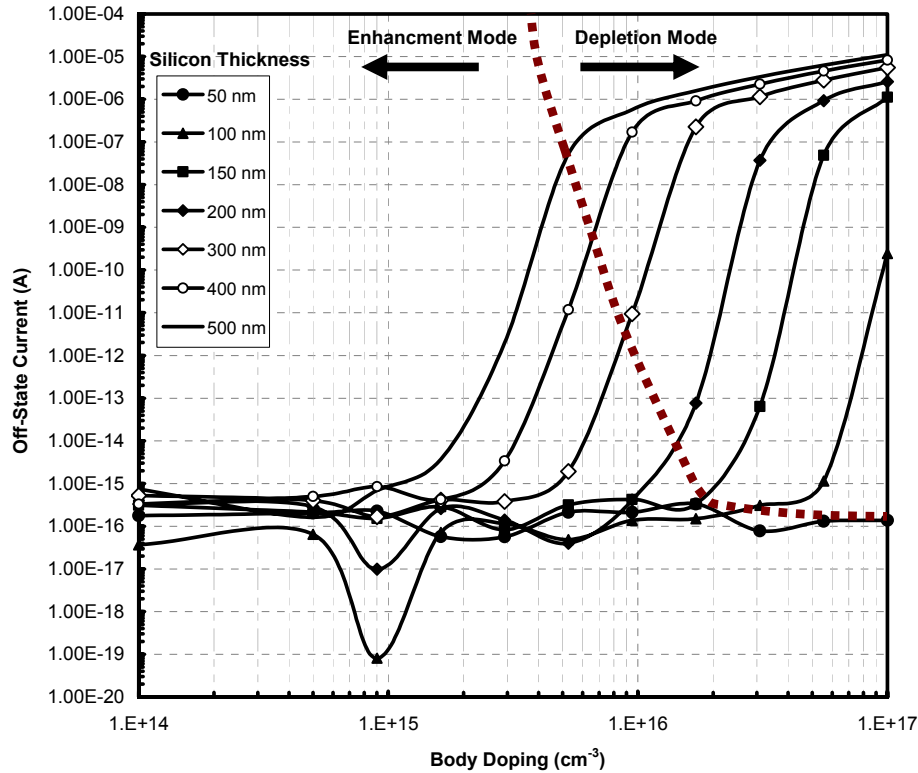
Figure 12. Simulation of the minimum off-state current of the thin-film PFET on glass. The dotted line denotes whether the transistor is operating as an enhancement mode or a depletion mode device *(i.e* it represents the current at the extracted threshold voltage). Even if a transistor has an enhancement mode threshold voltage is still may not have adequate off-state characteristics. If the silicon film is too thick, or the body dopant concentration is too high, there will be a significant amount of leakage current. Current values $< 10^{-15}$ A are subject to numerical error from the simulation software.

Considering a very thin film or a very lightly doped film would be the best choice to main low leakage current levels and an enhancement mode threshold voltage. In this range, there is leeway to allow for slight variation in these factors without seeing a significant increase in the leakage current.

A metric was developed to maintain specific off-state characteristics while adjusting device design parameters. This metric is derived from the ratio of current at the threshold voltage (I_{VT}) and the current with the gate at zero-bias (I_o); the logarithmic value of this ratio indicates drop of current in decades as the gate voltage changes from V_T to 0 V.

The number of decades required for adequate transistor performance is an engineering decision and is chosen based on the device application. Figure 13 is plot of the design metric $Log(I_{VT}/I_o)$ vs. p-type dopant concentration for various silicon film thicknesses.
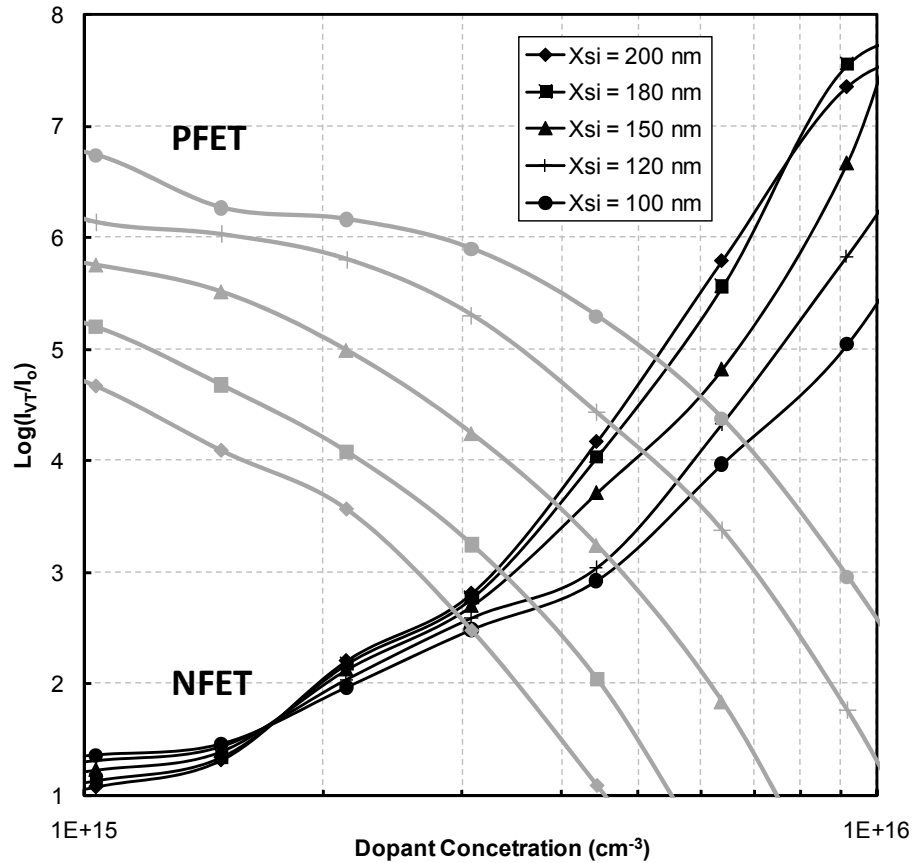
Figure 13. Numerical modeling of design space for NFET and AMPFET transistors on SiOG under ideal conditions; considering no interface charge or trap states. The off-state metric is $Log(I_{VT}/I_o)$, described in the text. Devices with a channel length of 2 μm and a gate oxide thickness of 50 nm were simulated using a molybdenum gate workfunction. Intersecting points of same film thickness represents symmetric operation of both the NFET and AMPFET transistors with threshold voltages of the same magnitude.

Figure 13 provides a comprehensive assessment of both the NFET and PFET off-state performance achievable at different values of NA and X_{Si}. A value of 6 for the off-state metric would represent an excellent discrimination between on-state and off-state current. Either the PFET or NFET can meet this criterion individually with appropriate parameter

values, however a compromise is required to provide equivalent off-state performance. The intersecting points of matched X_{Si} characteristics in Figure 13 define the performance of NFETs and PFETs with the same body doping level. As shown in the figure, the highest span of current drop is about 4.25 at X_{Si} of 100 nm and N_A of 6.7×10^{15} cm^{-3}. Note that interface charge or trap states that may exist at either the top or bottom silicon layer interface has not been considered. The presence of charge states can have a significant influence on subthreshold behavior, yielding results which may be interpreted as either better or worse than this ideal scenario.

While the explanation of ideal SiOG TFT behavior is easily discussed by parameters which that can directly control, real devices are affected by non-idealities such as surface finish and contamination. In Chapters 5 and 6, a discussion of SiOG TFT performance will be conducted in the context of fabricated devices. The impact of non-ideal effects will be discussed and explained through numerical modeling where appropriate.

CHAPTER 5

PROCESS REFINEMENT TOWARDS IMPROVED DEVICE PERFORMANCE

5.1 Introduction

In this chapter, a discussion of changes to substrate preparation and processing along with their effects on device performance is given. Small refinements in the substrate preparation before and during process can and do have a substantial impact on the final electrical characteristics of the fabricated transistors. Because of the subtleness of some of these refinements, their implementation and impact can be easily overlooked. Identifying and employing these modifications can be quite involved at best. Impact of these changes is not well captured in physical models and their effectiveness typically can only be quantified through experimentation.

Independent of work at RIT, Corning Incorporated has made refinements to the SiOG substrate manufacturing process, in areas such as implant and bonding conditions, to help improve starting film quality and lead to enhanced electron device performance. Along with the manufacturing of SiOG, preparation of the substrate for device and transistor fabrication is of great importance as well. Experimentation at RIT has assessed the impact that surface preparation and cleaning before and during fabrication have on final device characteristics. While these are simplistic changes, their improvements have lead enormous improvements in TFT function in all operating regimes as well as

reproducibility. The following sections identify these changes as show the influence on the final fabricated TFTs.

5.2 Surface Finish

One of the parameters that need to be addressed during the fabrication of SiOG substrates is the quality of the surface finish. The surface quality of the silicon film on SiOG can affect mobility, threshold voltage and uniformity across a substrate. Due to the proprietary nature of the SiOG fabrication process, some parameters described in this analysis will be treated as categorical or reported as relative results as opposed to quantitative quantities.

One of the primary electrical response metrics for quantifying the quality of the surface finish was the field-effect mobility. All surface finish experiments were done on bulk p-type silicon substrates on which surface channel NFETs were fabricated. From the measured I_D-V_G characteristics, the electron field-effect mobility was extracted from the maximum transconductance from the curve [33, 34].

In Figure 14 the surface finish treatment condition and the corresponding mobility values are shown; nine sample sites were measured in all cases. Considering the electron field-effect mobility extracted in the linear mode of operation (*i.e.* neglecting lateral field effects), the standard finish treatment shows the lowest mobility value. Both Alternative (Alt.) #1 finish and Alt. #2 finish treatments demonstrated improvements over the standard finish at the time of the experiment, however the Alt. #2 finish was much more comparable to the ideal (vendor prepared) bulk wafer finish condition. This result demonstrated that the SiOG surface finish, prepared by Corning Incorporated, had a direct influence on the field-effect mobility response.
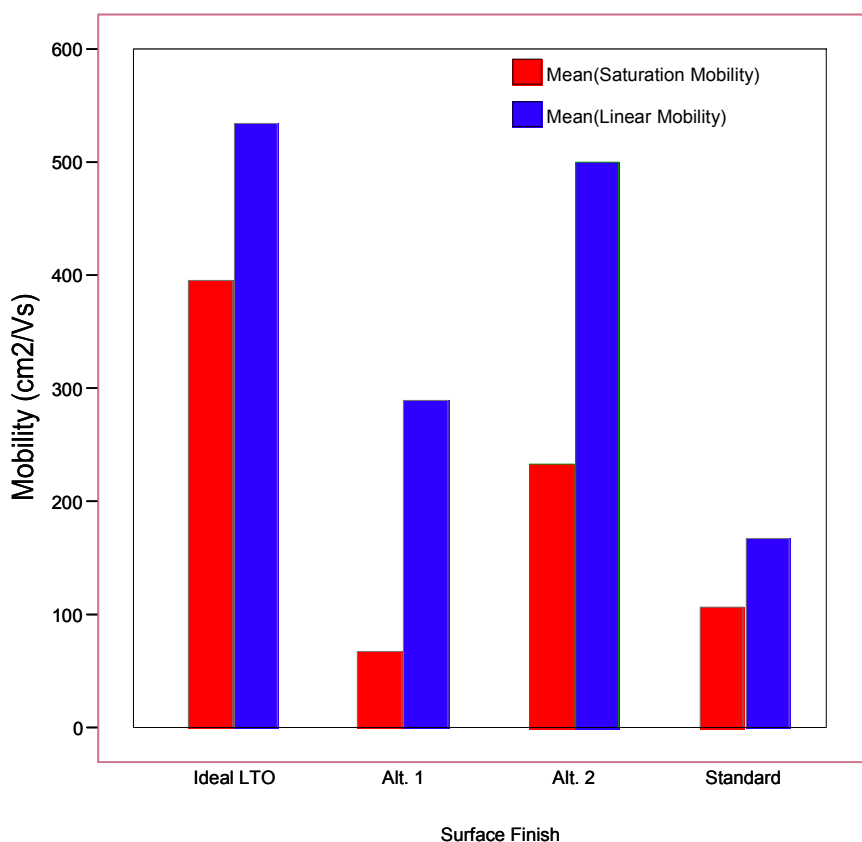
Figure 14. Electron field-effect mobility with varying surface conditions on bulk substrates. The field-effect mobility was extracted from the maximum transconductance from an NFET transistor fabricated on bulk Si with the substrate temperature not exceeding 600 °C. The Alt. #2 finish showed to be far superior to the then standard finish. The ideal surface is resulting from a prime-grade bulk silicon wafer, direct from the manufacturer.

While the on-state results of Alt. #2 surface finish appeared encouraging, the off-state behavior required further investigation. Figure 15 shows C-V characteristics of the ideal surface finish treatment compared to the Alt. #2 finish. While mobility values are similar as shown in Figure 14, the C-V curves of Alt. #2 finish are significantly degraded by comparison. The improved (smoother) surface quality does seem to offer reduce mobility degradation due to surface roughness and normal electric fields; however, it does not seem to alleviate any issues with fixed charge or interface traps at the silicon / SiO_2 interface. The Alt. #2 finish curves are significantly stretched in the depletion and weak

inversion region of the C-V plot. Note that a higher threshold voltage is observed even though both wafers treatments were of the same dopant concentration.
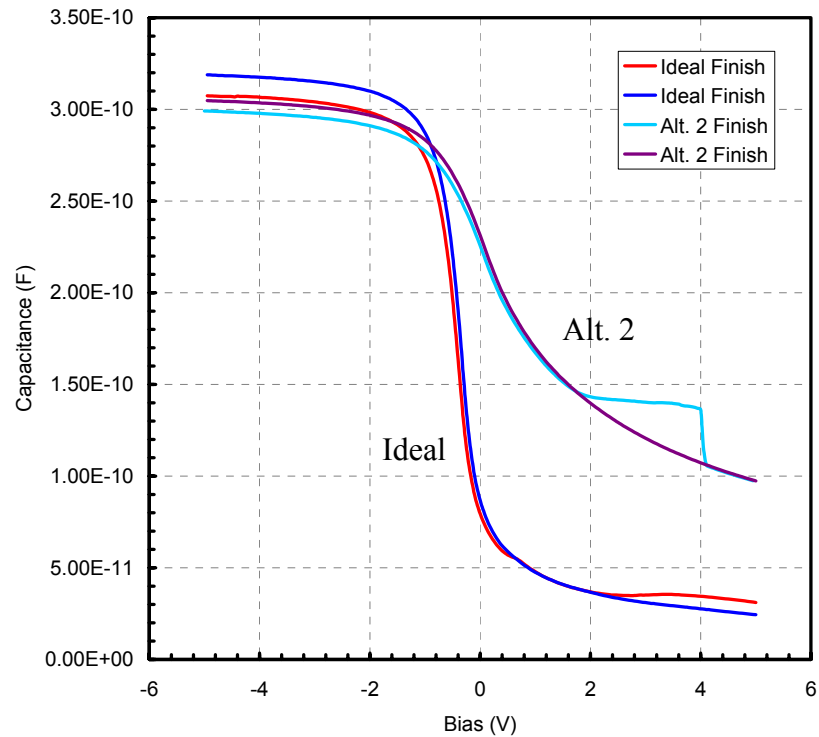
Figure 15. CV measurement of bulk wafers with different surface finished. Surface finish Alt. #1 is not shown because it did not yield interpretable MOS C-V curves.

While improving the surface finish did offer some benefits, there were still large discrepancies between the ideal and "improved" Alt. #2 surface finish. Thus, these discrepancies must be due to another effect other than the surface quality of the silicon wafer, which is a representation of the surface quality of the SiOG silicon layer. Figure 16 shows a comparison of gate-swept I-V characteristics. In this case, an alternative cleaning process was implemented (HCl / H_2O_2 mixture). Both curves show very similar trends, particularly in the sub-threshold region. There is a slight offset in the curves, however the left-to-right offset can be attributed to minor dopant concentration difference between the two substrates. The ideal finished wafer does show higher on-state current,

and appears to exhibit a higher level of leakage current in the overdriven off-state. However the apparent difference in leakage is within the sample variation; there were Alt. #2 finish samples that exhibited higher leakage, along with more noticeable sub-threshold distortion. The results shown nonetheless demonstrated the potential of an improved cleaning procedure.
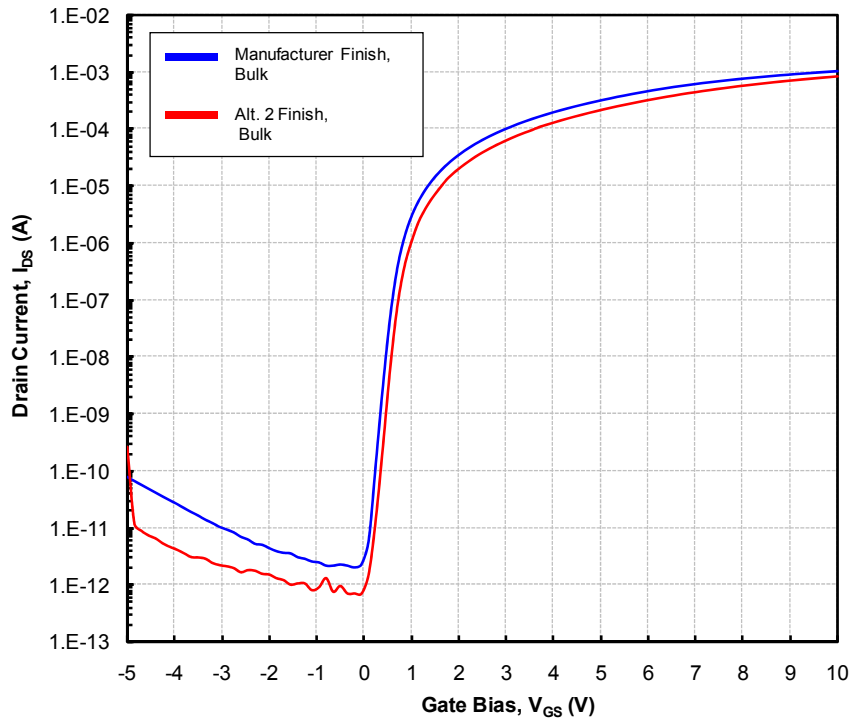
Figure 16. Improved I-V characteristics with Alt. 2 surface finish and improved cleaning process for transistor (L = 6μm, W = 24μm) fabricated in bulk substrates at temperatures ≤600 °C. The characteristics show the same trend, but are slightly offset. Note that the Alt. #2 characteristic presented is a best-case device sample.

5.3 Cleaning Process Improvements

One of the major efforts in device performance improvement was the implementation of a more stringent cleaning process. This improved process was particularly effective when implemented before the gate dielectric deposition. The prior version of this

cleaning step consisted of submerging the substrates in a 50:1 H_2SO_4:H_2O_2 piranha bath heated to 130 °C. In order to reduce the need for heated chemical processes to maintain compatibility with FPD manufacturing, traditional RCA cleaning processes [1] were not originally implemented, as found in conventional CMOS manufacturing. The piranha bath was chosen for its effectiveness in organic particulate and residue removal as well as the ability to remove inorganic contaminants [35, 36]. However device performance improvements were realized by using a modified RCA clean [37] prior to the gate dielectric LPCVD deposition process. This 4-step cleaning process started with the same 50:1 H_2SO_4:H_2O_2 piranha bath heated to 130 °C for 10 minutes followed by a 50:1 H_2O:HF dip for 20 seconds. This was then followed by 1:1:5 H_2O:H_2O_2:HCl soak for 15 minutes at 75 °C and a final dip in the 50:1 H_2O:HF dip for 20 seconds. Between each chemistry transition, the wafers were rinsed in de-ionized water for five minutes.

The addition of an HCl bath was implemented to aid in the removal a possible metal/inorganic contaminates on the surface of the SiOG substrate [37, 38]. The SiOG substrate fabrication process does contain steps that are mechanical in nature which could be possible sources inorganic contaminations. Also, it is known that the glass portion of the SiOG substrate does contain inorganic materials (alkaline earth elements) that could out diffuse during some processing steps, though this is highly unlikely as mentioned in [39]. Metals such as Fe and Ni are known to be deep trap levels within the silicon bandgap, and HCl has been proven to remove such contaminates [37].

The HF dips were implemented into the process to remove any chemically formed oxide (Si_xO_y) during the cleaning process due to the H_2O_2 [38]. In a conventional CMOS process, where a thermally grown gate SiO_2 layer used, this chemical Si_xO_y layer formed

during an RCA cleaning process is consumed and pushed away from the silicon, leaving a high quality interface. In the SiOG TFT process, the gate dielectric is a deposited SiO_2 layer; thus an interface with a high level of fixed charge and traps will result if the chemically formed SiO_x layer is not removed.

The I_D-V_G characteristics shown in Figure 17 illustrates the profound difference in SiOG TFT performance due to the improved cleaning process. The devices that went through the piranha-only cleaning process (without an HF chemical oxide removal) show signs of elevated fixed charge levels, resulting in lateral shifting of the of I-V characteristics. Enhanced interface trap levels are also indicated through the degraded sub-threshold swing. The kink observed in the NFET curves that only has the piranha clean has been associated with silicon dangling bonds through numerical modeling as shown in Figure 18. The removal of the chemically induced oxide layer is shown to reduce the level fixed interface charge and dangling bonds at the silicon/gate SiO_2 interface significantly.
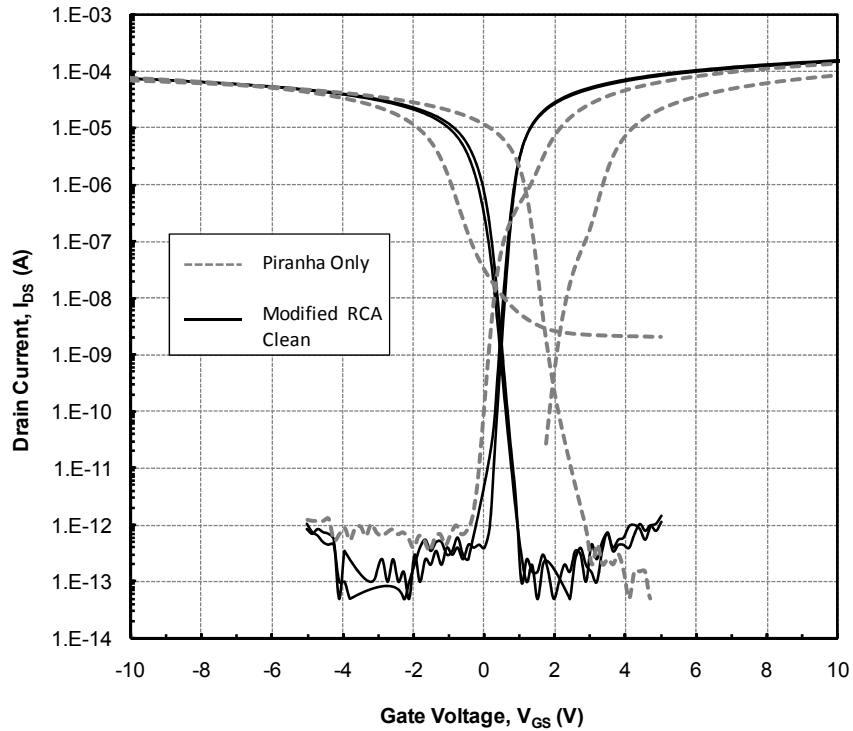
Figure 17. SiOG TFT I_D-V_G characteristics (L = 3µm and W = 24µm) with two different cleaning processes prior to the gate SiO_2 dielectric deposition. Each cleaning process is represented by measurements taken from two devices. The SiOG substrate cleaned only with the piranha shows evidence of threshold voltage shifting due to fixed interface charge and changes in the sub-threshold swing due to interface traps. The kink observed in the piranha-only NFET transistors has been linked to silicon dangling bonds at the interface through numerical modeling. Implementing the modified RCA clean resulted in a significant reduction in both fixed interface charge and interface trap levels.

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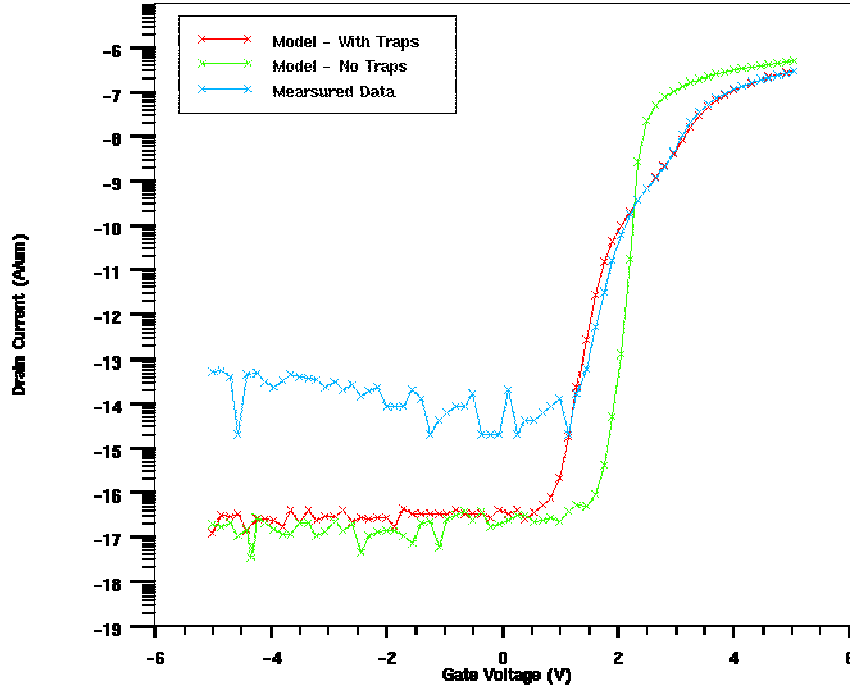
Figure 18. Numerical modeling of SiOG NFEF I_D-V_G characteristics for devices that saw the piranha-only cleaning process. Excellent overlay of between the measured and modeled devices is shown. The kink in the characteristics corresponds to a donor-like interface trap 0.8 eV from the conduction band edge. This has been found to correspond to a possible trap state for a silicon dangling bond [40]. An ideal NFET I-V characteristic is also shown for comparison without any interface traps.

5.4 Silicon Layer Design Tradeoffs in SiOG CMOS TFT Performance

The effect of silicon film thickness on the performance of TFT transistor is of great importance from both an electrical and manufacturing perspective. Silicon film thickness affects almost all device performance parameters directly, including threshold voltage, current drive, and off-state leakage. Ideally a thinner semiconducting film offers better transistor control; however achieving a thin crystalline silicon film (thickness $\leq$ 100nm) is difficult from a manufacturing prospective. Thus understanding the influence that the silicon film thickness has on SiOG TFTs is essential to realize an optimized CMOS device design that is manufacturable.

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To study the impact of SiOG silicon thickness, various SiOG substrates were fabricated with film thicknesses between 80 nm and 350 nm.

Table 2 summarizes the silicon layer thicknesses investigated in TFTs fabricated using the standard fabrication process. The implant process used was the same regardless of the thickness of the silicon film; designed such that the peak of the implant profile was approximately 20 nm below the surface of the silicon.

Film Thickness (nm)	Dopant Concentration (cm^{-3})
81	9×10^{14}
151	9×10^{14}
202	9×10^{14}
251	9×10^{14}
350	9×10^{14}
201	1.3×10^{15}

Table 2. Summary of SiOG silicon film thicknesses and corresponding dopant concentration. A duplicate wafer at 200 nm thickness was created but had a slightly higher dopant concentration.

Changes in the silicon thickness should result in a proportional change in both the NFET and PFET threshold voltages, as observed in Figure 19. In both cases, as the film becomes thinner, the V_T values shift to the left (less positive, more negative); consistent with the discussion in Chapter 4. A thinner film has an overall lower total depletion charge, and establishes the onset of inversion at a lower NFET threshold voltage. For the PFET, a lower amount of acceptor ions requires a larger negative gate potential to form an accumulation layer and establish on-state current.
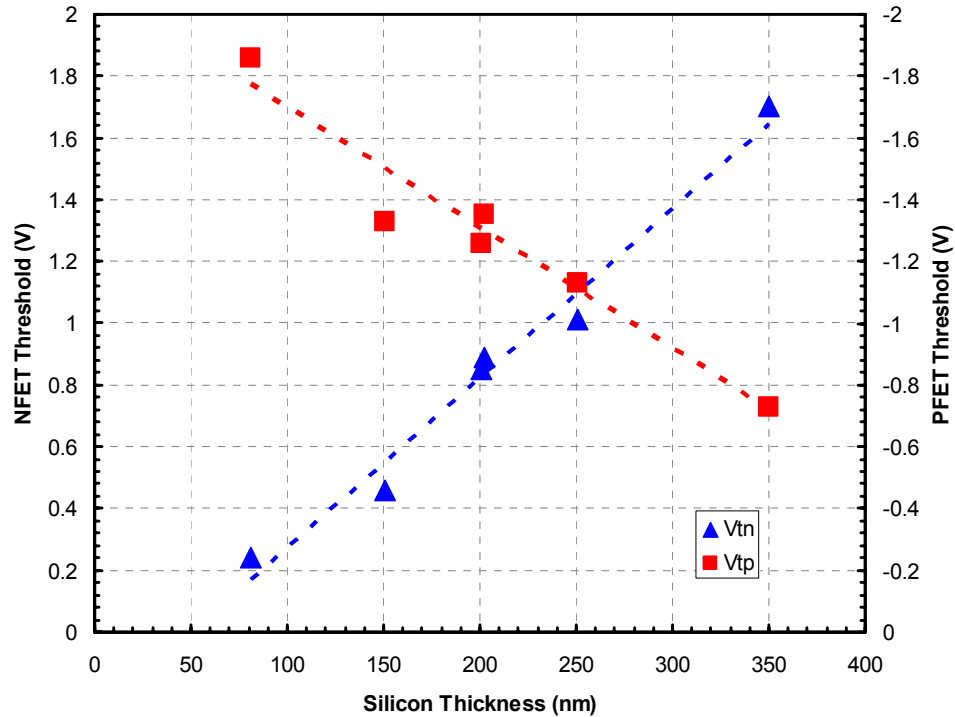
Figure 19. MOSFET threshold voltage as a function of SiOG silicon thickness. A linear trend should be observed. At the 150 nm thickness treatment, a slight deviation from the trend is observed, both the NFET and PFET threshold voltage have a lower magnitude threshold voltage. This is consistent with a lower P-type film dopant concentration.

Figure 20 shows how the maximum drive current of the transistor varies with silicon thickness. For a surface channel device, as in the case of the NFET, as the film becomes thinner a higher level of inversion should be achieved thus provide higher current drive. Results where the silicon thickness was scaled from 350 nm to 200 nm appears to follow this trend, however as the thickness is scaled below 200 nm the current drive begins to drop. This reduction in current can be attributed to a reduction in surface quality due to the SiOG manufacturing process. Surface roughness on the silicon film, coupled with a higher normal field will lead to increased mobility degradation.

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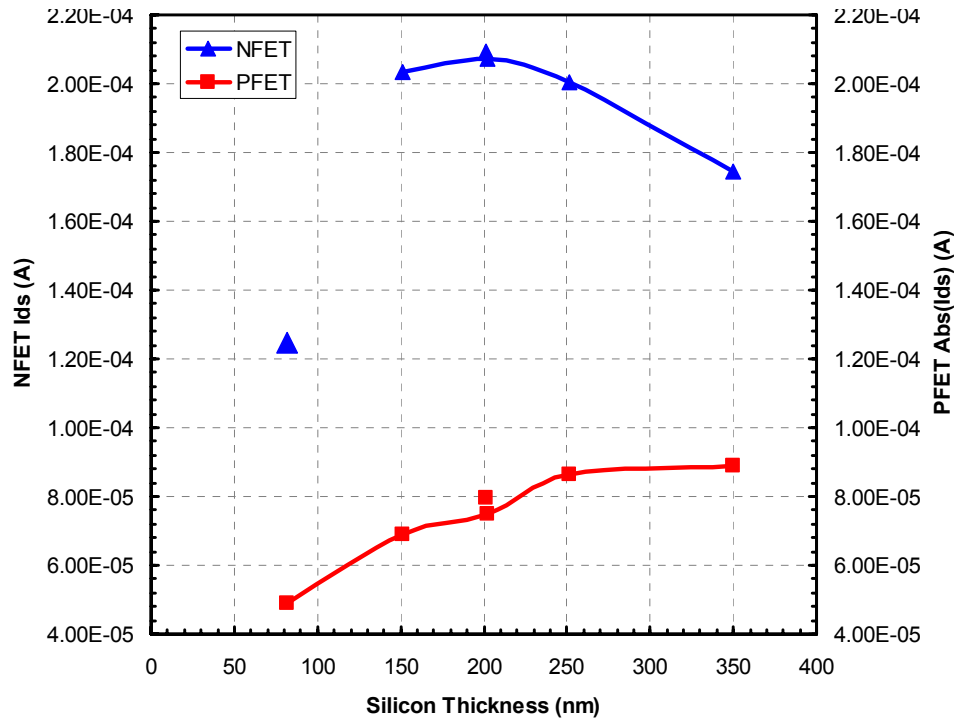
Figure 20. NFET and PFET current drive as a function of silicon thickness. The PFET trend follows expected behavior, showing more current as the p-type silicon layer thickness is increased. The NFET demonstrates a peak current drive at a p-type silicon film thickness of 200nm, with an apparent compromise in carrier mobility as the film thickness is decreased further due to the thinning process.

For the PFET, the opposite current trend is observed. As the silicon film is made thicker, the current level is higher at an equivalent biasing scheme. Because the PFET is an accumulation mode device, it has conduction both through the accumulation layer and the body of the transistor. As the film becomes thicker, there is an increase in the body current. At the same time, the magnitude of the potential required to form an accumulation layer also decreases, causing an increase in current drive. This result also suggests that the effective channel mobility of hole carriers in the AMPFET is not as sensitive to normal-field degradation.

5.5 Enhanced SiOG TFT Performance

By implementing an improved SiOG silicon finish (Section 5.2) and an improved substrate cleaning process, particularly before the gate dielectric deposition (Section 5.3), a step-function improvement in the SiOG TFT performance was achieved. This improvement was observed both in the performance in the TFTs and the uniformity of operational parameters across a four-inch substrate. Figure 21 shows a comparison of transistors fabricated on SiOG and SOI substrates. Substantial improvement can be seen in the SiOG NFET and PFET characteristics, especially when compared to those from initial process runs [5].
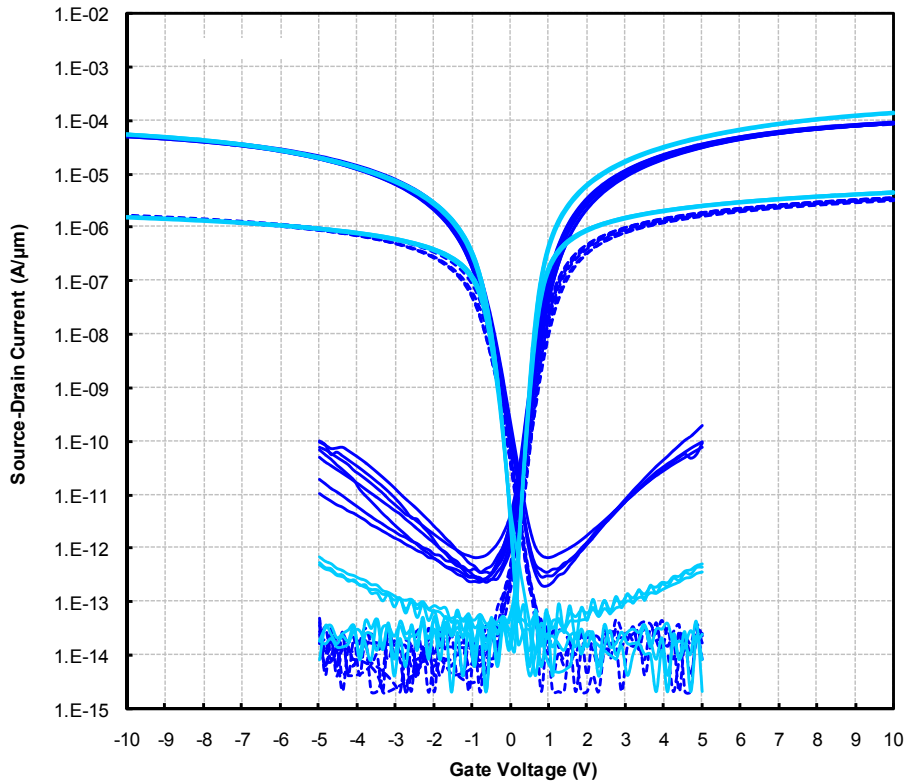
Figure 21. A comparison of SiOG and SOI TFTs fabricated at low temperature. Multiple devices are shown (n = 9) to give an indication of uniformity. Implementing surface finish and cleaning improves allowed for a considerable improvement in SiOG NFET and PFET I-V performance and uniformity across a 4-inch substrate. Transistor operation at V_{DS} = 0.1 V and 5 V are shown. L=6 μm, W=24 μm, and the gate SiO_2 thickness was 50 nm. A further discussion on device characteristics is presented in Chapter 6.

CHAPTER 6

ADVANCED DEVICE MODELING AND SUBMICRON SCALING

6.1 Introduction

The follow section describes the process of modeling transfer (I_D-V_G) characteristics on the described SiOG AMPFET and NFET devices. These transistors show more similarities to SOI FETs than to TFTs. Because of the high quality silicon layer, carrier hopping transport mechanisms (as in a-Si) or grain boundary effects (as in LTPS) are not applicable. Model development can be separated into two main domains: on-state and off-state. Modeling the on-state characteristics gives insight into how the transistor will perform in circuit applications. Extracted parameters such as V_T, carrier mobility, and transconductance can provide an excellent fit to measured data, however parasitic series resistance and mobility degradation mechanisms must be considered to provide consistent model accuracy over different bias conditions.

To model and simulated both the NFET and PFET I-V characteristics the software package Atlas, a commercial version of SPICES produced by Silvaco Data Systems Inc., was used [41]. To represent carrier transport degradation the Lombardi-Darwish numerical mobility model implemented [42,43]. Off-state behavior, including GIDL current, was modeled the numerical method described in [44]. Assembling the these

models and proper calibration, through iterative methods, allowed for accurate simulation of the SiOG devices.

6.2 Electrical Characteristics of TFTs Fabricated on SiOG and SOI

While the performance of SiOG CMOS TFTs was markedly improved through process refinements, there were noted discrepancies compared to TFTs fabricated on SOI, considered to be a performance benchmark. Figure 22 (replicate of Figure 21) shows these differences in both the on- and off-states; the off-state being emphasized with current presented on a log-scale.
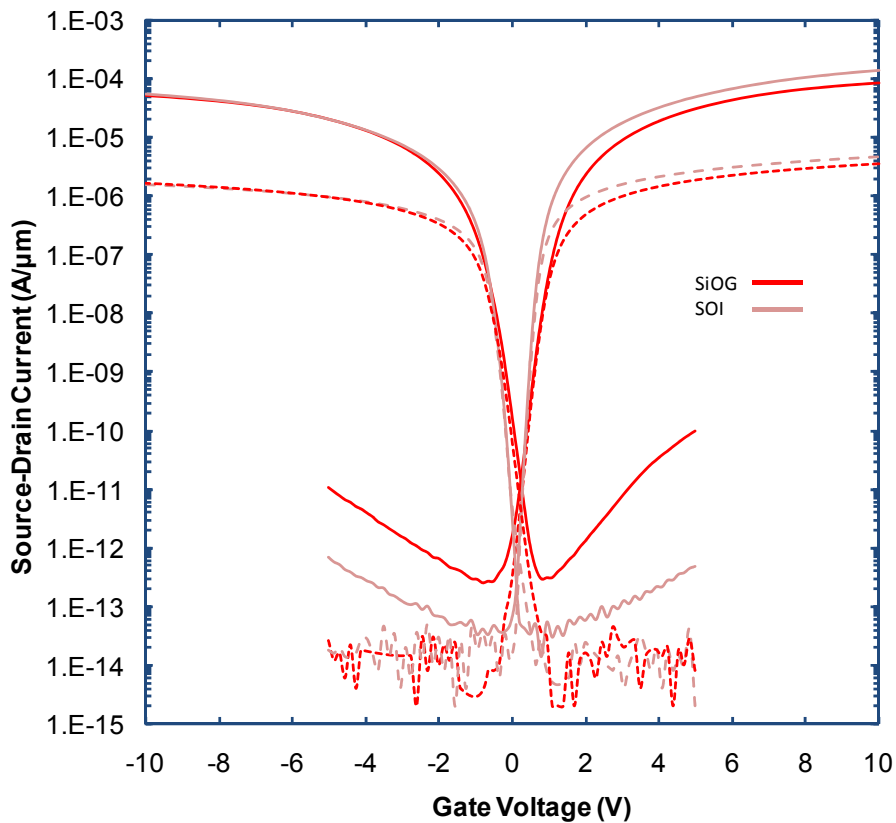
Figure 22. A comparison I-V characteristics of TFTs fabricated on SiOG and SOI for $|V_{DS}| = 0.1V$ and $|V_{DS}| = 5$ V. Both substrates show GIDL at the higher drain bias condition; however it is considerably higher with the SiOG transistors.

The SiOG NFETs in Figure 22 have a slightly lower transconductance than their SOI counter parts at lower gate voltages. This in turn means than the SiOG NFET does have a lower electron field-effect mobility of around $450 - 510 \text{ cm}^2/\text{Vs}$ compared to the SOI's of $600 - 630 \text{ cm}^2/\text{Vs}$. A similar assessment can be made for the PFETs. While the discrepancy between the two devices is not as large, the SiOG PFET does have a lower hole field-effect mobility of around $250 - 280 \text{ cm}^2/\text{Vs}$ where as the SOI is about $300 \text{ cm}^2/\text{Vs}$. While in both cases the SiOG TFTs do have lower field-effect mobilities than the ideal case of the SOI devices fabricated a low temperature, they are much higher than those reported for current LTPS technologies when carrier transport across grain boundaries is considered [45, 46].

In observing the off-state characteristics, the leakage current is observed to increase when the gate bias is over-driven. This is evident both on the SiOG and SOI substrates, however to a lesser degree on the latter. The high magnitude of Gate-Induced Drain Leakage (GIDL) on the SiOG TFTs has to do with a fundamental difference in the device structure. While the SOI substrate is supposed to mimic the SiOG substrate but contain an ideal silicon film, its buried oxide (BOX) layer is of finite thickness and the mechanical silicon substrate does influence transistor operating characteristics. Fringing electric field lines in the SOI transistor can impinge on the mechanical silicon substrate. This leaves less stray fields to impinge on the body of the transistor and reduce the amount of GIDL; a thinner BOX supports a reduction in the amount of GIDL. In the SiOG transistor, the entire substrate is glass. Any fringing fields from the electrodes can terminate only on area within the transistor. This increased stray field impacts the SiOG

DC characteristics; primarily in the off-state, observed through enhanced GIDL and short-channel behavior.

6.3 Overlay of Measured and Modeled data

Modeling the off-state behavior of SiOG transistors provides a yet deeper understanding on the fundamental operation of the device. Through careful interpretation, using a non-automated and highly iterative process, models have been developed that account for the variety of irregularities often observed in subthreshold characteristics. Interface charge and trap densities, and associated energy distribution, are key factors. Device modeling has revealed the properties of the operative interface traps (i.e. type, location, energy level) and how they affect both the NFET and AMPFET operation. These non-ideal centers have influence at both the oxide/silicon and silicon/glass interfaces. The AMPFET seems to be influenced by acceptor-like states at the silicon/glass interface. These states cause the subthreshold region to be extended and can ultimately limit the minimum off-state leakage current. While these states do have a minor effect on the inversion-mode NFET transistor characteristics, donor-like states at the silicon/gate dielectric interface have a larger impact. These donor-like states control both the subthreshold slope of the NFET and can cause shifts in the threshold voltage. A realistic and comprehensive trap model has been iteratively derived for selected SiOG devices, showing full consistency on local NFET and AMPFET device pairs.

A model-calibrated trap-state energy distribution was used in the fit to measured data, with integrated acceptor-like and donor-like state densities around 2×10^{11} cm^{-2}. Discrete traps states were used initially to provide a close fit to measured SiOG transistor I-V data.

An exponential fit was then applied to the discrete trap densities to provide a smoother distribution and is shown in Figure 23.
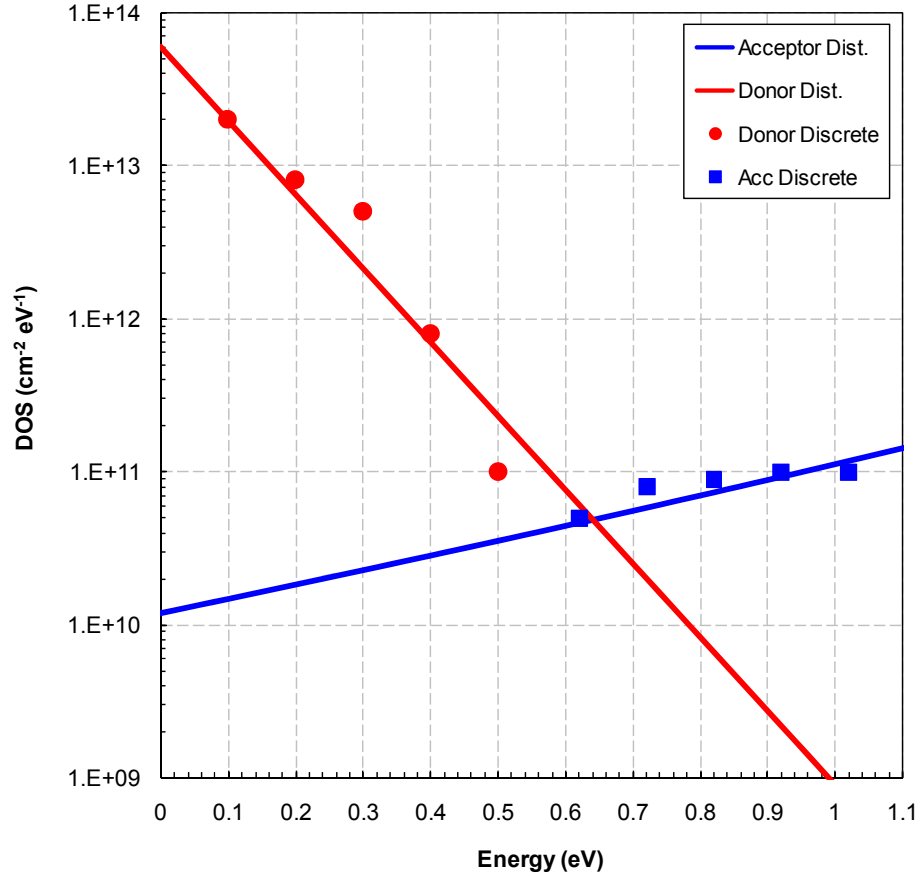
Figure 23. Distributions of interface charge at the silicon/glass interface as derived through numerical modeling and simulation. Through this analysis, it appears that the backside interface is dominated by acceptor-like trap states in the off-state where E_F is moving towards E_C.

The on-state model was enhanced with mobility degradation parameters that account for scattering events (carrier-carrier, carrier-ion, carrier-phonon and carrier-surface) as well as the effects of normal field degradation and velocity saturation. Finally, tunneling parameters that account for the observed GIDL in the overdriven off-state were

implemented in order to provide a remarkable fit to the full transfer characteristic, shown

in Figure 24 (linear scale) and Figure 25 (log scale).
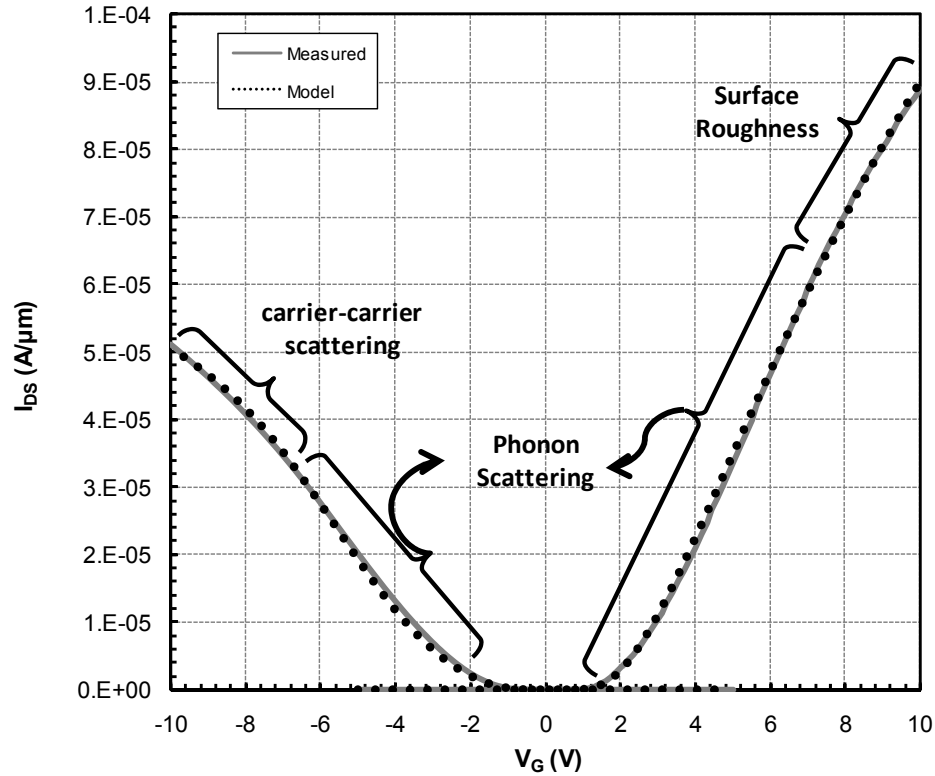
Figure 24. Overlay of modeled characteristics with measured SiOG transistor data. on a linear current scale. $|V_{DS}| = 5$ V and $L = 6$ μm to ensure long-channel behavior. The following primitive device parameter values were used: $\Phi_{MS} = 4.53$ eV, $X_{ox} = 48$ nm (measured optically), $X_{Si} = 200$ nm, $N_A = 3 \times 10^{15}$ cm^{-3}. Low-field (SPICE equivalent) channel mobility values are μ_n @ 450 cm^2/V-sec and μ_p @ 280 cm^2/V-sec for the NFET and AMPFET, respectively. See the text for additional details on numerical model enhancements.

Several mobility degradation mechanisms contribute to both the NFET and AMPFET

final on-state I-V characteristics as shown in Figure 24. Regions of the curves where

particular mobility degradation mechanisms are dominant are indicated. Phonon and

inter-valley scattering at lower normal fields are similar in both the NFET and APMFET.

At high normal fields, these mechanism manifest differently in the NFET and the

AMPFET. It should be noted that at high normal fields (e.g. high gate bias) the TFT

transitions from the saturation mode of operation to the linear mode; the current dependence on V_G would ideally transition from quadratic to linear behavior. The surface channel of the NFET is strongly affected by the surface quality of the SiOG film, whereas increased surface roughness can enhance mobility degradation. Because of the two conduction paths present in the AMPFET, adjusting the level of the surface roughness parameter did not produce the observed mobility degradation. However, the degradation is well modeled by increased carrier-carrier interactions. Both of these mobility degradation mechanisms result in the observed sub-linear characteristics at higher V_G values.

Matching the modeled with the measured subthreshold I-V characteristics in Figure 25 was primarily done through assumption of particular interface trap distributions at the silicon/gate dielectric and silicon/glass interfaces. Two possible mechanisms were considered for the observed GIDL current; band-to-band tunneling and trap-assisted tunneling. It was found that pure band-to-band tunneling alone models this increased gate-overdrive leakage current; which is identical behavior in both the NFET and AMPFT. If trap-assisted tunneling were significant, characteristics associated with the n+ and p+ implanted regions would be expected to exhibit somewhat different results.
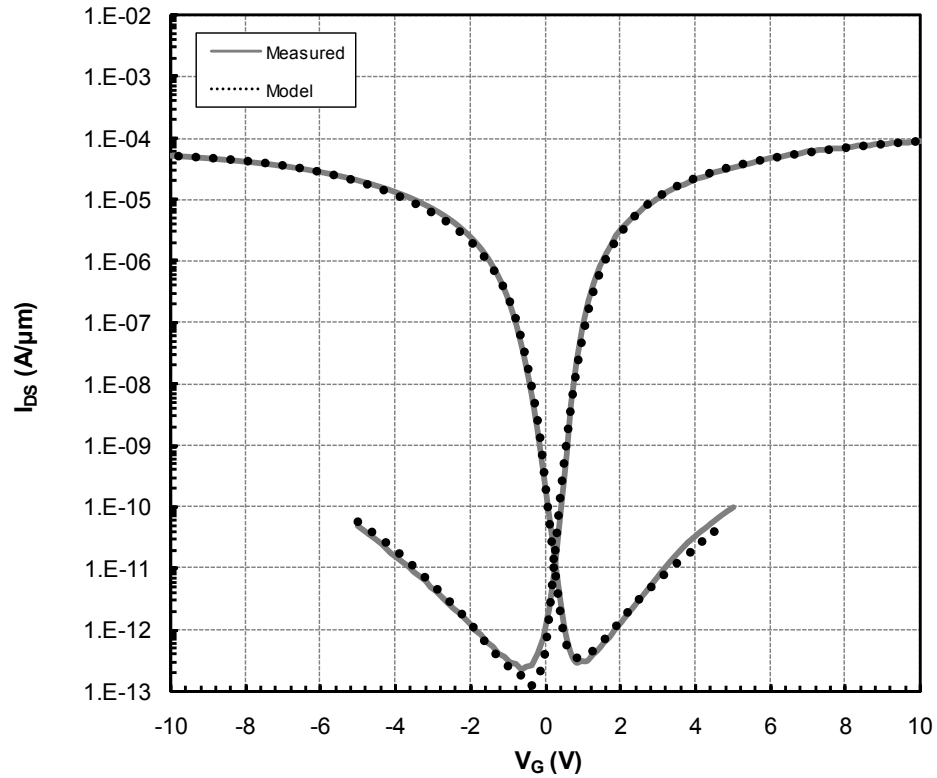
Figure 25. Overlay of modeled characteristics with measured SiOG transistor data with $|V_{DS}| = 5$ V and $L = 6$ μm to ensure long-channel behavior.

6.4 Steps toward submicron SiOG TFT scaling

One of the promising qualities of SiOG substrates is its potential for scaling CMOS TFTs into the submicron regime. As with bulk silicon and SOI material systems, overcoming short-channel effects is necessary in SiOG, as well as the challenge of additional non-ideal behavior (i.e. trap effects, pronounced GIDL) that must be suppressed. Since the NFET and PFET TFTs operate quite differently, the scaling of each presents their own set of challenges. Unfortunately the compensation for short-channel effects and non-ideal device behavior usually involves additional complexity in device design and processing procedures; highly undesirable in developing a FDP-compatible process. It is well established that the addition of lightly-doped drain

(LDD) structures can help reduce GIDL by lowering the peak E-field and degree of band-bending near the drain end of the device. As the NFET is an inversion-mode device, the scaling trends are predictable. Short-channel effects can be improved primarily through scaling the gate oxide and channel doping. Scaling the silicon layer thickness could also be considered, however due to SiOG manufacturing constraints this option is not feasible.

The AMPFET demonstrates limitations in device scaling, beyond which an inversion-mode device is required. Design and simulation work in presented in Chapter 4 showed that the AMPFET has considerable scaling issues, particularly when the silicon thickness & dielectric thickness is not scaled with length. DIBL-like short channel effects become very intolerable at channel lengths just below 2 μm. The NFET, utilizing a surface channel, does scale better, but begins to reach its limits of acceptable short channel effects at around 1 μm channel length. The transistors described in Chapters 3 and 4 where never intended to operate at channel lengths less than 2 μm.

One of the main reasons for the onset of short channel effects, in particular channel length modulation and DIBL, is the fact that body doping is relatively light. The transistors in this study were fabricated using P-type body regions of $\sim 1 \times 10^{15}$ cm^{-3} doping concentration. As mentioned earlier this lightly doped body region allow for the fabrication NFET and AMPFET device with threshold voltages symmetric around $V_G = 0$ V. However as the channel length is reduced, the high lateral field extending from the drain across the body of the transistor allows for the quick onset of short channel effects.
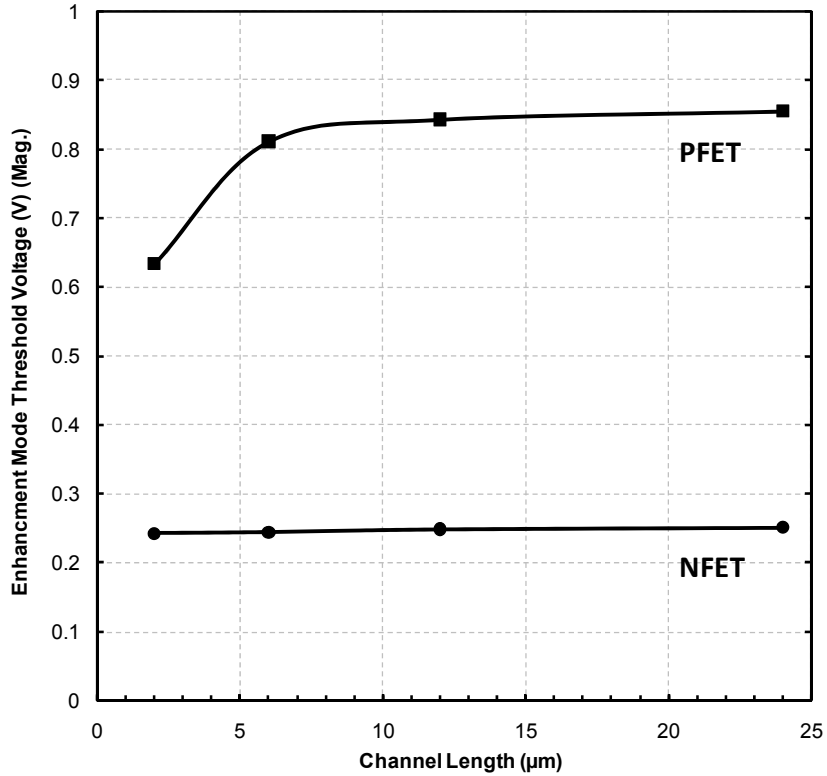
Figure 26. Measured saturation-mode (V_{DS} = -5.0 V) V_T roll-off characteristic of the SiOG AMPFET. The relatively small V_T offset at L = 2 μm is expected due to the device parameters chosen based on the design tradeoffs involved in the NFET and AMPFET for CMOS operation.

The AMPFET has demonstrated reasonable off-state performance. Figure 26 shows V_T roll-off behavior for the AMPFET under saturation conditions, with a relatively small shift at L = 2 μm   The V_T roll-off represents a characteristic on the device design of this particular accumulation-mode PFET. If the AMPFET design parameters (e.g. N_A, X_{Si}, Φ_{MS}) were chosen independently from the NFET, subthreshold characteristics could be optimized with additional process complexity. Note that the inversion-mode NFET V_T (not shown) is unaffected at these dimensions. The sensitivity of the AMPFET V_T is primarily due to the reduction of the depletion region induced by the gate field-effect as the source and drain regions are closer in proximity, and the lack of a physical p-n junction to establish a hole-carrier energy barrier at the source/drain ends of the transistor.

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To allow for transistor channel length scaling to take place while keeping in mind the limitation of fabrication in the FPD industry the best approach is to implement a body adjustment implant. In a conventional bulk CMOS process this would be analogous to threshold adjustment implant. By implementing such an implant, the SiOG CMOS performance is no longer a careful balance between the starting silicon film doping concentration, the gate dielectric thickness and the gate metal workfunction in order to achieve a balanced NFET and PFET. Using a body-adjust implant, the operation of the NFET and PFET can be independently regulated.

A body-adjust implant accomplishes several things. First, it can be used to raise or compensate the dopant concentration in the body region. This will directly affect the threshold voltage of the transistor and can be optimized to meet design specifications independently on each transistor type. The body-adjust implant can also help manage short-channel effects such as channel length modulation, DIBL, and ultimately punchthrough, due to narrower depletion widths and a relative increase in gate control on the channel. The final benefit of a body adjust implant is that it can be used to change the majority dopant type, analogous to a well implant. The body of the AMPFET can be counter doped n-type, thus changing the device to a surface-channel or inversion-mode PFET.

Implanting dopants into semiconductors to adjust transistor behavior is a relatively common technique, particularly in the IC industry. In fact, it would seem quite obvious to implement this right away on any SiOG CMOS design. However it does need to be engineered differently in the SiOG material system, in addition to considering the process

complexity associated with the added lithography and implant steps that can be quite costly in the FDP industry.

A primary technical concern is the fact that any body-adjust implant must be annealed at temperatures ≤ 600 °C. As discussed in [26], dopant activation is not 100% at these temperatures and moreover is highly dose dependent. This makes it impossible to predict active dose values without an experimental investigation. Perhaps of larger concern is how implant damage will be healed during any subsequent annealing at 600 °C. One of the major highlights of SiOG is the fact that the silicon is crystalline. Implantation in the body region of the transistor creates damage to the silicon lattice. If this damage cannot be annealed out, it could lead to a polycrystalline channel region or remaining defects and/or amorphous regions which would render the advantage of the starting single crystalline film moot. Grains and/or defects in the body and channel region of the transistor could degrade mobility. In addition, these defects could introduce trap energy level with in the band gap further degrading threshold voltage and subthreshold transistor characteristics.

The possibility of implementing a body adjust implant was investigated on TFTs fabricated on an SOI wafer. The body adjust implant was integrated into standard low-temperature TFT fabrication process flow, following active (mesa) definition and etch as a blanket implant through 100 nm of SiO_2. It was activated during the source/drain anneal at 600 °C for 2 hours in a N_2 ambient. A boron dose of 5.5×10^{11} cm^{-2} on selected transistors (NFET & PFET) while a phosphorous dose of 6.5×10^{11} cm^{-2} on others. The characteristics of these transistors were then compared to transistors without the body-adjust implant. All transistors were fabricated on the same SOI substrate with a 200 nm

p-type silicon layer with a doping of 3×10^{15} cm^{-3}; different regions receiving a different implant. For the NFET, the boron implant dose was designed to provide a +2 V threshold, and the phosphorus implant dose was designed to provide a -1.5 V threshold (depletion-mode). For the PFET, the boron implant dose was designed to provide +0.3 V threshold (depletion-mode), and the phosphorus implant dose was designed to provide a -2.5 V threshold. The V_T targets assumed 100% dopant activation during the 600 °C anneal.

The linear-mode transfer characteristics for thin-film NFETs are shown in Figure 27. Without a body-adjust implant the extracted threshold voltage was 0.33 V. The boron implant increased the threshold voltage to 1.15 volts. The phosphorous implant lowered the V_T to -1.33 V.
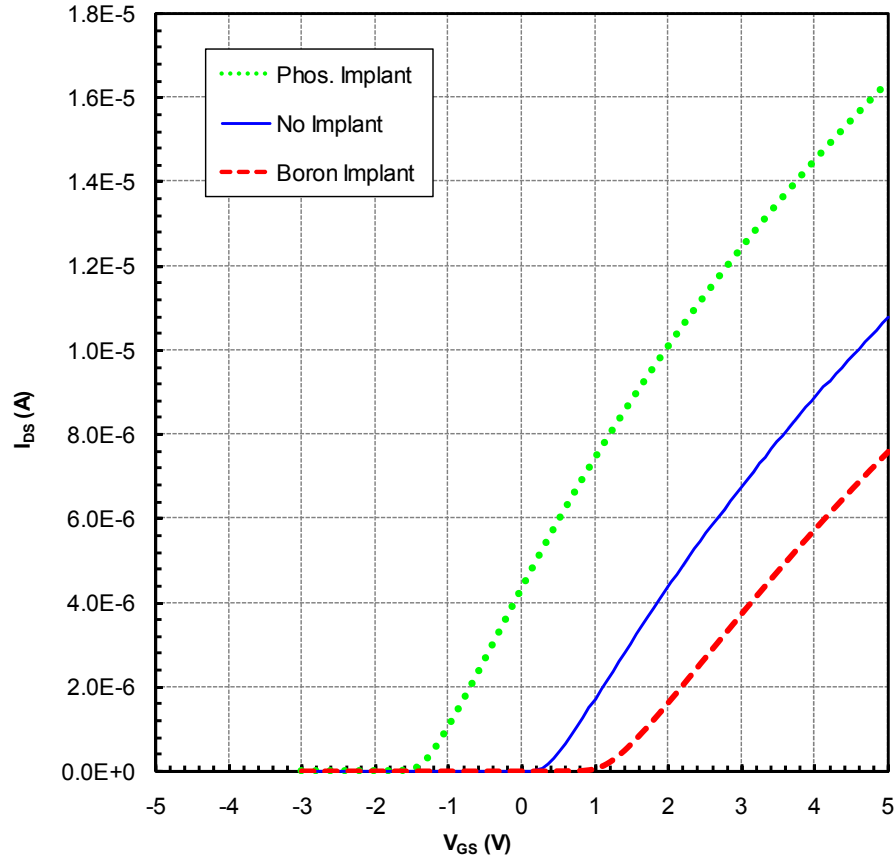
Figure 27. Body adjust implant implemented on a thin-film NFET transistors. A 5.5×10^{11} cm^{-2} boron dose, a 6.5×10^{11} cm^{-2} phosphorus does we performed and compared to an NFET transistor that did not receive any body adjust implant. With no implant and a P-type substrate dopant concentration of 3×10^{15} cm^{-3} resulted in a 0.3 V threshold voltage. The boron implant increase the threshold voltage to 1.15 V while the phosphorus implanted lowered it to -1.33 V.

For the phosphorus implant, the difference between the designed and measured threshold voltage is 0.2 V. The equivalent dose is 6.35×10^{11} cm^{-2} which equates to 98% dopant activation which is higher than what the trends predict in [26]. The boron implant show a threshold difference between the design and measured to be about 0.85 V. The equivalent implant dose for this threshold voltage is 3.17×10^{11} cm^{-2}. This is only 58% boron activation which is in very good agreement with the trends predicted in [26] without preamorphization.

Examining the electron field-effect mobility as extracted from the maximum transconductance, the transistor the than with no implants was around 500 cm^2/Vs. The phosphorous body adjust implant transistor showed a mobility of 510 cm^2/Vs, in good agreement with the reference device. However, the boron body adjust implant seems to lower the electron field-effect mobility. And mobility of 390 cm^2/Vs was extracted. Reason for this is not clear and is somewhat counter intuitive. Examining the subthreshold characteristics in Figure 28, is seen that the phosphorus implant cause a left shift in the I-V curves. However, for the boron implanted case, there is a right shift present but also a change in the subthreshold slope. In fact, a clear kink in present in the curve. This suggests that there are defects/trap states in the channel and body region of the transistor. These defects/trap states cause degradation in carrier transport and thus lower the electron mobility.
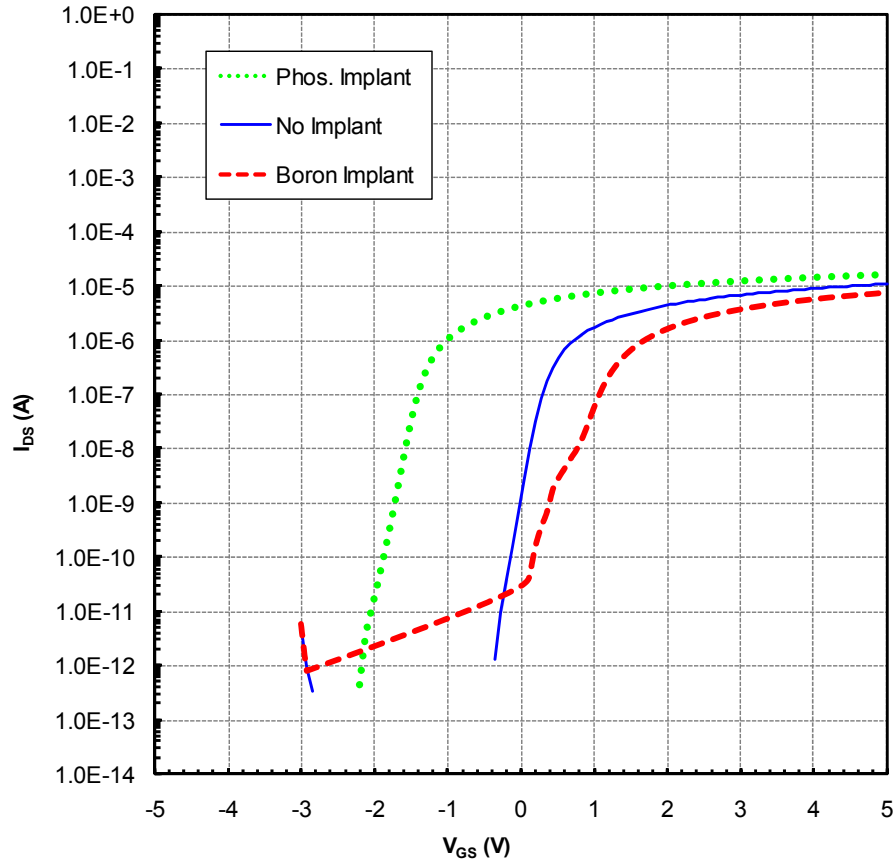
Figure 28. Subthreshold characteristics of those shown in Figure 27. The phosphorous body adjust implant caused a linear left shift in the I-V characteristics. The boron body adjust implant caused a right shift and also degraded the subthreshold slope. A kink in this curve is also present. The degradation of the this curve suggests the implant caused damage that could not be repaired by the low temperature anneal.

As with the thin-film NFET a similar analysis can be performed with the thin-film PFET. As mentioned earlier, the PFET is an accumulation mode device. The 6.5×10^{11} cm^{-2} phosphorus dose is enough to counter dope the p-type silicon film to make it n-type. With no implant, the accumulation mode PFET had a threshold voltage of -0.91 V. Using a phosphorous body-adjust implant of 6.5×10^{11} cm^{-2}, the same as for the NFET, the threshold voltage was shifted lower to -2.38 volts. This corresponds to an effective implanted dose of 6.32×10^{11} cm^{-2} or 97% dopant activation, consistent with that of the NFET. Using a boron body-adjust implant dose of 5.5×10^{11} cm^{-2} the threshold

voltage was shift lower to -0.05 V. This is equivalent to a effective dose of

3.71×10^{11} cm^{-2} or 67% dopant activation; higher than the NFET interpreted result (58%)

which may be related to the mode of device operation. This appearance of higher boron

activation may be due to the nature of the accumulation mode PFET structure. The p$^+$

source and drain regions, having only a small potential barrier to the body of the

transistor, promotes a lower threshold voltage. This 2-D V_T roll-off effect may become

further enhanced by added boron in the body, creating the appearance of higher dopant

activation.
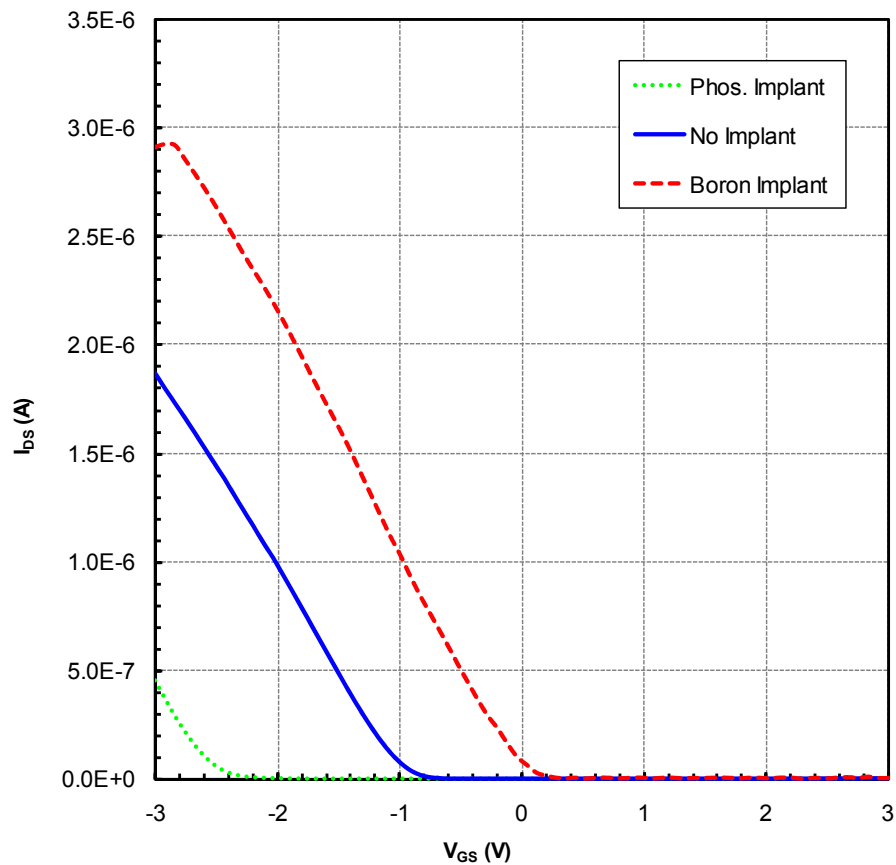
Figure 29. Body adjust implant implemented on a thin-film PFET. A 5.5×10^{11} cm^{-2} boron dose, a 6.5×10^{11} cm^{-2} phosphorous does we performed and compared to an PFET transistor that did not receive any body adjust implant. With no implant and a P-type substrate dopant concentration of 3×10^{15} cm^{-3} resulted in a -0.91 V threshold voltage. The boron implant increase the threshold voltage to -0.05 V while the phosphorous implanted lowered it to -2.38 V.

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The subthreshold characteristics of the PFET are shown in Figure 30. The boron body adjust implant increased the threshold, causing a linear shift in the I-V characteristics. However, the minimum off-state of the PFET is now much higher because the increased boron in the body region of the devices makes it harder for the gate to fully deplete this region.
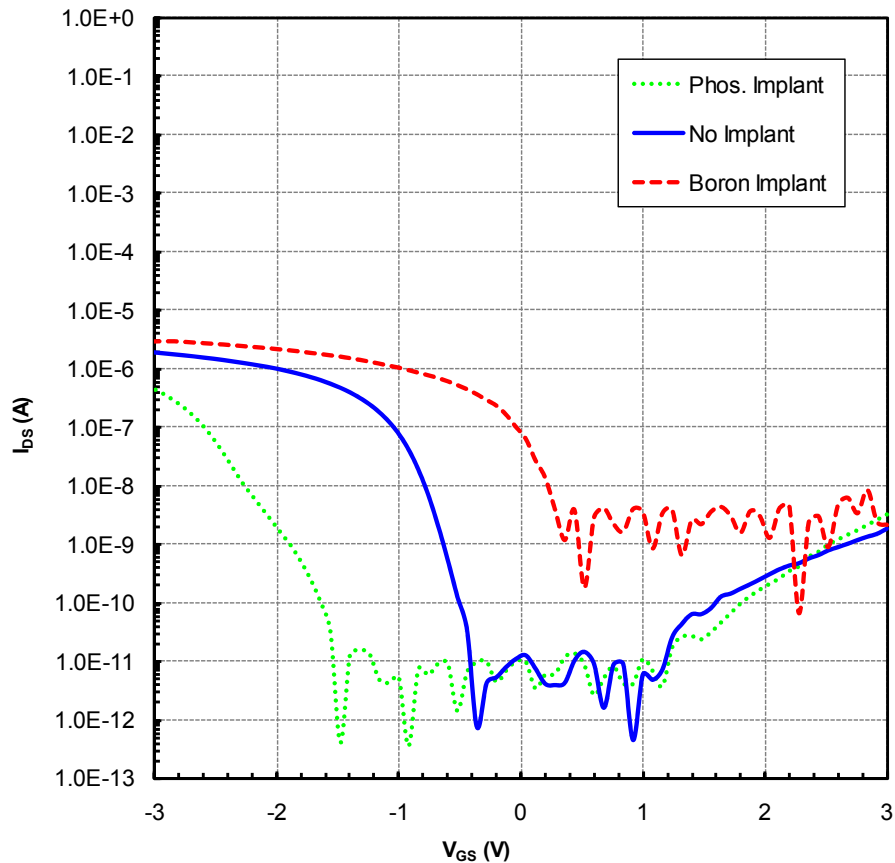
Figure 30. Subthreshold I-V characteristics of the thin-film PFET. The boron implant increased the threshold voltage causing a linear shift in the characteristics. However, the minimum off-state is lower because the added boron in the body regions does not allow the gate to deplete this region and effectively. The phosphorous implant lowered the threshold voltage and degraded the subthreshold swing.

For the phosphorus body-adjusted implanted PFET, the threshold was moved further negative as expected. However the characteristic was degraded in the subthreshold

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region; the mechanism of which has not been well established. Comparing the field-effect hole mobility, both the boron and phosphorus body-adjusted PFETs demonstrated values that were consistent with the non-adjusted device, $\mu_{eff} \sim 150$ cm^2/Vs.

In further examination of the effectiveness of the body-adjust implant, the C-V characteristics of implanted body regions were compared to a non-implanted body. For the analysis, a two-dimensional thin-film capacitor was used consisting of a molybdenum gate, a 50 nm SiO$_2$ gate dielectric, and a p$^+$ or n$^+$ border around the capacitor for the bottom semiconductor electrode. For further specification of the capacitor, see Appendix C. Table 3 shows the nominal flat band and onset of full depletion voltages. For a non-implanted capacitor a shift can be induced by either the phosphorous or boron implant. Figure 31 shows the C-V characteristics for a p$^+$ contact thin-film capacitor and n$^+$ thin-film capacitor respectively.

	P+ Contact			N+ Contact		
	Phos. Implant (ΔV)	No Implant (V)	Boron Implant (ΔV)	Phos. Implant (ΔV)	No Implant (V)	Boron Implant (ΔV)
Fully Depleted	-1.5	-0.75	1.11	-1.2	-0.8	1
Flat Band	-1.8	-1.65	0.73	-1	0	1.3

Table 3. Flatband and fully depleted voltage shift observed with phosphorous or boron body adjust implants.

Through C-V analysis the boron body adjust implant seems to just cause a lateral shift in the characteristics for both the p$^+$ and n$^+$ contact cases with little or no change is the slope. Also, the accumulation mode capacitance is in good agreement with that of the non-implant capacitor. The phosphorous body adjust implant not only causes a lateral shift in the C-V characteristics, but also a change in slope potentially due to interface traps.
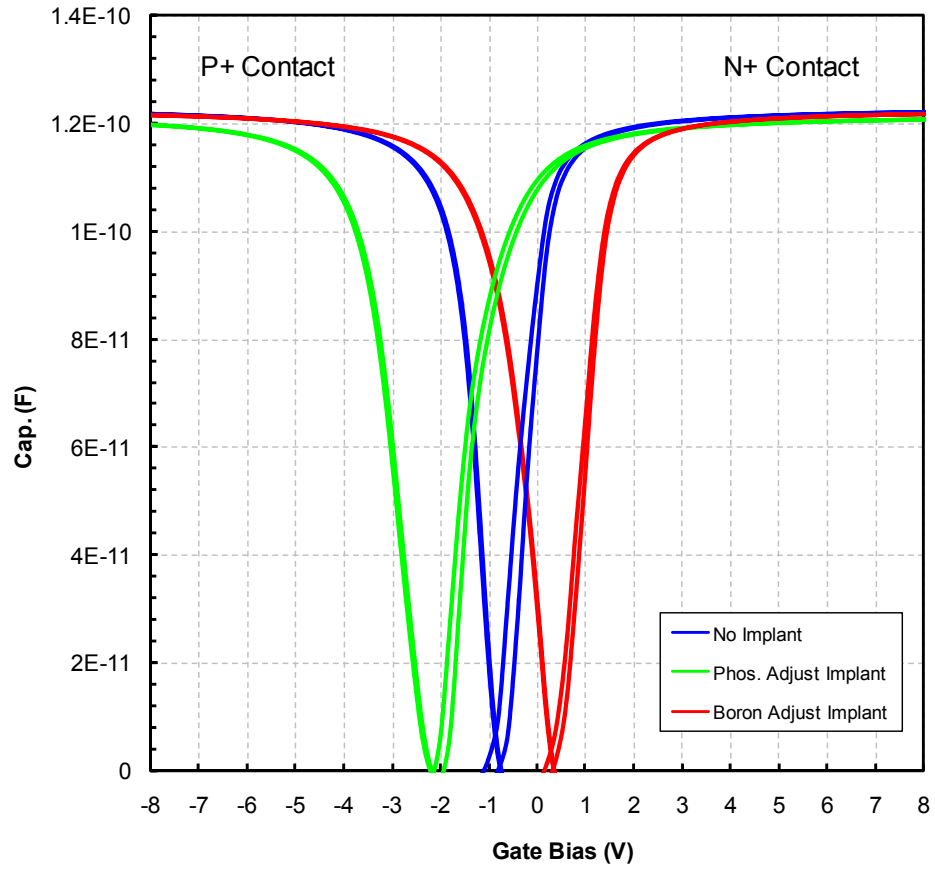
Figure 31. Comparison of C-V characteristics for a thin-film (two dimensional) capacitor on p-type SiOG at 100 kHz with a P+ contacts and N+ contacts. Because of the thin film nature the capacitance quickly goes to zero once the film is fully depleted.

CHAPTER 7

CONCLUSION

7.1 Introduction

Subtle yet significant improvements to fabrication of TFTs on SiOG substrates at RIT have led to much improved NFET and PFET electrical characteristics. This, coupled with advanced modeling and simulation, has led to a much stronger understanding of the physics and electron device design considerations involved in the SiOG material system. In this chapter, a review of the significant developments and findings throughout the parts of this study are presented.

7.2 SiOG Device Design and Simulation

There are many possibilities and parameter choices for implementing thin-film transistors on SiOG substrates. An overview of the design space for both the on-state and off-state characteristics of NFETs and PFETs was given with consideration of the processing constraints associated with SiOG. An inversion-mode NFET and an accumulation-mode PFET were implemented to allow for a CMOS technology on SiOG using a single metal-semiconductor workfunction difference (Φ_{MS}). The gate workfunction (Molybdenum, $\Phi_M = 4.53$ eV) was such that it is nearly a midway compromise between n+ polysilicon (4.1 eV) and p+ polysilicon (5.3 eV). This provided a nearly symmetrical CMOS operation about $V_{GS} = 0$ V for p-type silicon film, boron concentration of approximately 1×10^{15} cm^{-3} and 200 nm thick.

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The consideration of the off-state design of both types of devices was given with emphasis on the differences in channel formation and conduction mechanisms. A design metric of the logarithm of the current ratio at V_T and 0 V ($Log_{10}[I_{VT}/I_o]$) was use to help ensure the proper performance of both devices while still maintaining symmetric operation. Figure 32, reproduced from Chapter 4, again shows this metric plotted for both the NFET and PFET considering various silicon doping concentrations and thicknesses.
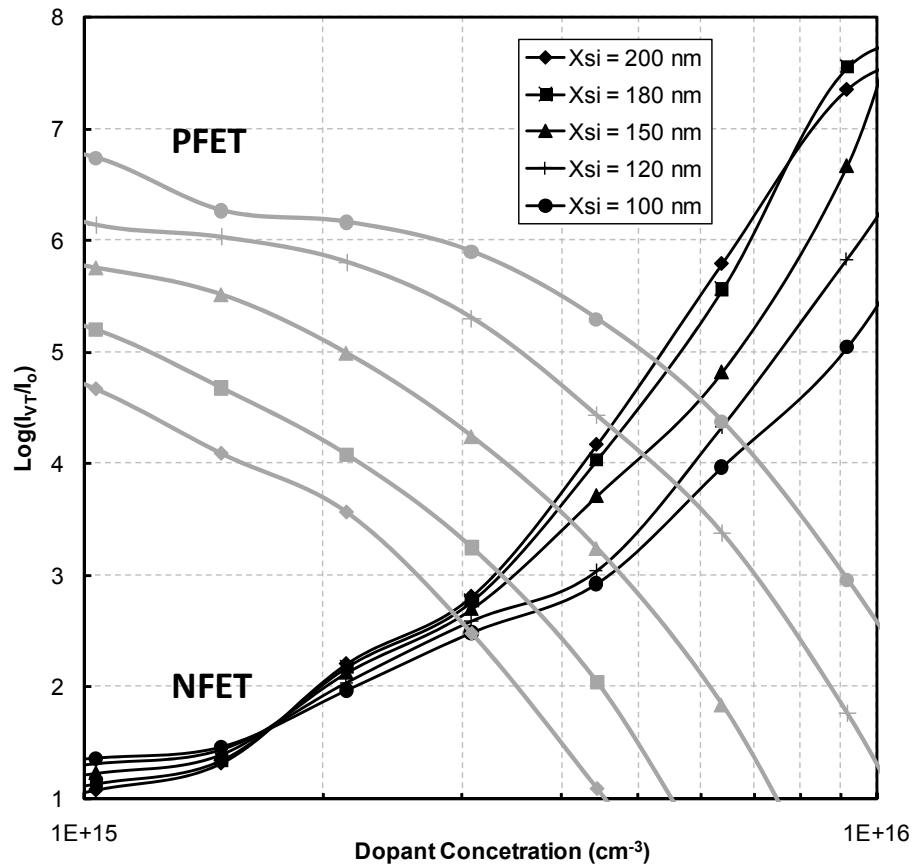
Figure 32: Design space for NFET and AMPFET transistors on SiOG under ideal conditions; considering no interface charge or trap states. Reproduced from Figure 13 for convenience.

While the limitation of any accumulation mode transistor are known and well understood, its integration in CMOS on SiOG allows for a very simple process which

would be easily adaptable by the FPD industry. Also, the accumulation mode PFET allows for more in-depth understanding of the SiOG material system due to the increase sensitivity to the silicon/glass interface.

7.3 Refinement in SiOG processing and improved TFT performance

Small modification to the SiOG substrate preparation with improved in-process cleaning have shown to dramatically improve the TFT I-V characteristics both in the on- and off-state regimes, while also improving uniformity. The impact of Corning Incorporated's proprietary SiOG surface preparation methods on TFTs was experimentally investigated. It was found that the Alternate #2 finish (anticipating a smoother surface) yielded higher performance TFTs than the current standard SiOG finish; although inferior in comparison to standard IC wafer manufacture.

The modification of cleaning processes during SiOG TFT fabrication has shown vast I-V performance gains. The addition of $HCl:H_2O_2$ immersion step following the $H_2SO_4:H_2O_2$ bath, along with dilute HF immersions after each peroxide mixture is believed to help removed additional metallic contaminates along remnants of any chemical Si_xO_y formation. This cleaning process done in particular before the gate SiO_2 deposition has shown dramatic improvement in TFT operation and is captured in Figure 33.
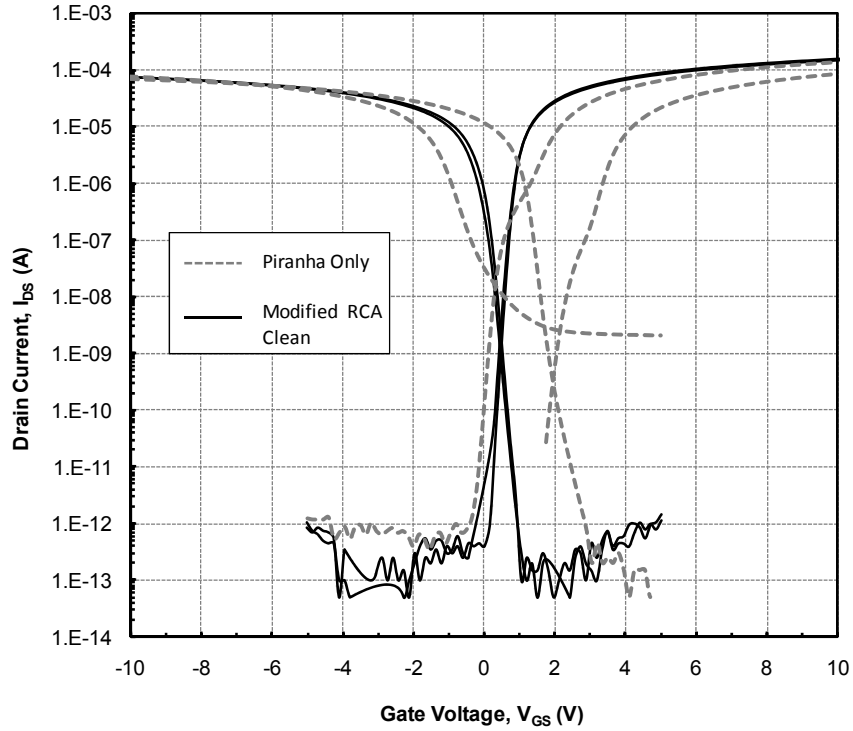
Figure 33. SiOG TFT I_D-V_G characteristics (L = 3µm and W = 24µm) with two different cleaning processes prior to the gate SiO$_2$ dielectric deposition. Each cleaning process is represented by measurements taken from two devices. The SiOG substrate cleaned only with the piranha shows evidence of threshold voltage shifting due to fixed interface charge and changes in the sub-threshold swing due to interface traps. Reproduced from Figure 17.

The enhancement offered by both the surface preparation and cleans has led the fabrication of devices on the SiOG material system comparable to those on the SOI material, keeping within the same processing constrains. This comparison is shown in Figure 34.
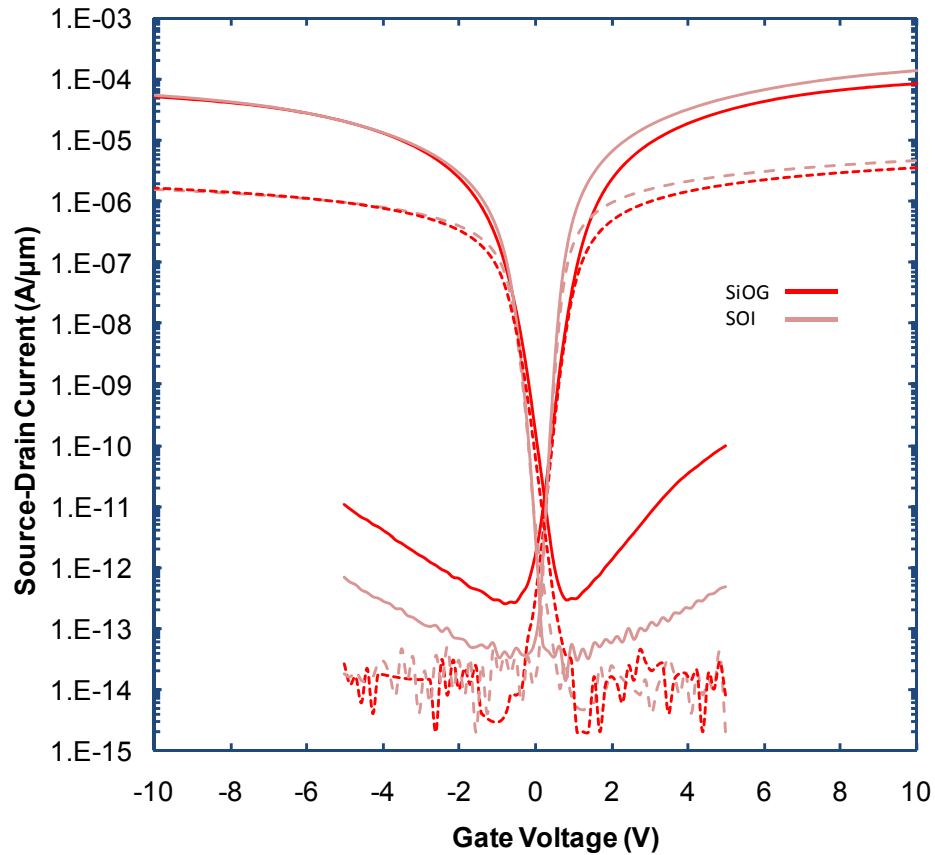
Figure 34. Enhanced TFT performance on SiOG compared to equivalent transistor fabricated on SOI at low temperatures. Reproduced from data in Figure 21.

7.4 Device Modeling and Understanding

Much effort has been put towards to understanding the physical operation of transistors is the SiOG material system. The use of numerical modeling and simulation tools have aided greatly in this effort. Numerical models for the NFET and accumulation mode PFET have been developed and are continuous overall all practical regimes of operation. In the on-state, the effects of mobility degradation have been accounted for and show up differently in the NFET and AMPEFT due to their disparity conduction

between the source and drain. Normal field mobility degradation appears in the NFET and is virtually lacking the AMPFET. In the AMPFET, this degradation mechanism is replaced by increased carrier-carrier interaction.

In the off-state regime, the degradation in the subthreshold swing has been modeled by proposed interface trap distribution of both acceptor- and donor-like states. These distributions were found through an iterative process and show excellent agreement with the measured I-V characteristics. The GILD current for the NFET and AMPFET manifest itself through pure band-to-band tunneling. Contribution to this current through trap-assisted tunneling was considered but could not be modeled with success. The mechanism for the GIDL current was found to be same for both flavors of devices. The model characteristics overlaid with the measured are shown in Figure 35.
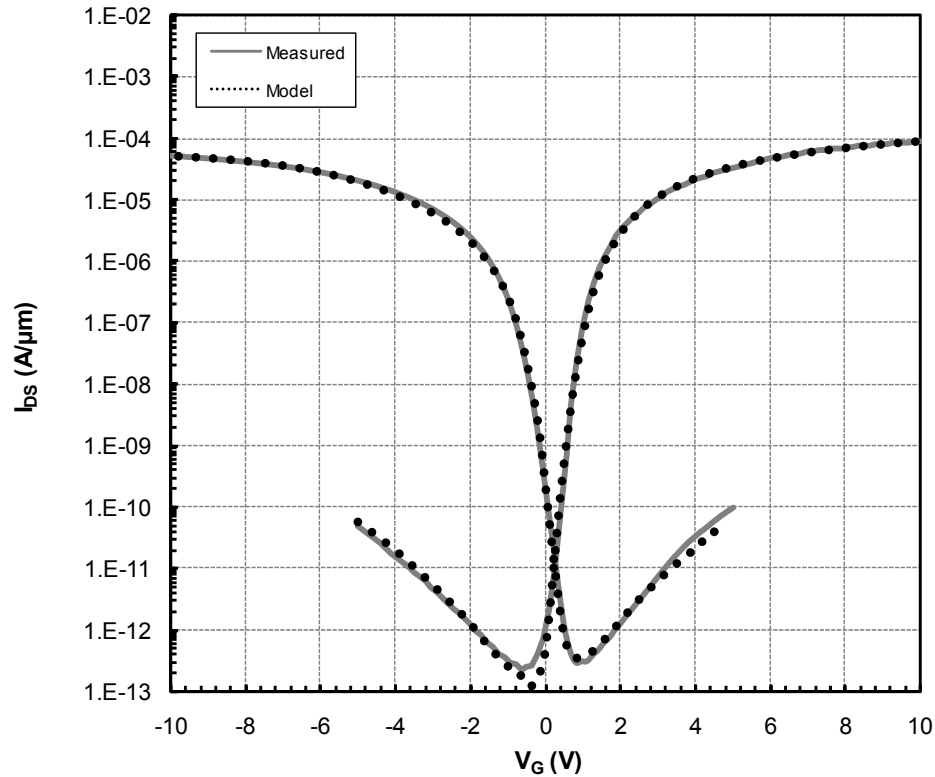
Figure 35: Modeled SiOG TFT characteristics overlaid measured data

7.5 Towards SiOG TFT submicron scaling

The limitations of the current process and device designs in scaling the channel length below 1 μm were discussed. A body-adjust implant was introduced as one possible means towards advancement in channel length scaling. Several benefits of the body-adjust implant include the reduction of channel-length modulation, V_T stability, and counter doping effects for surface channel operation of both NFET and PFET devices. The feasibility of a body-adjust implant was implemented on TFTs fabricated in the SOI material system processed at low temperatures. A phosphorus body-adjust implant was shown to have near 100% activation, while a boron body-adjust implant showed between 60-70% activation. In both cases there were no significant mobility degradation issues

associated with lattice defects, thus suggesting that either strategy could be used for CMOS implementation.

7.6 Closing Remarks

The primary focus of this study was to investigate potential improvements to NFET and PFET devices fabricated in the SiOG material system with minimal increase in fabrication complexity. These improvements have been made with the increased understanding of the governing physics of both NFET and accumulation-mode PFET operation. The implementation of a body-adjust implant was also investigated and shows potential in the channel length scaling of TFTs fabricated on SiOG.

This work has lead to several investigations that look to improve the performance of TFTs fabricated in the SiOG material system. Improvement to the silicon/gate dialectic interface is being investigated by looking at different gate insulating materials. These include deposited films via LPCVD and PECVD and low temperature oxidation of silicon. A second investigation poised to understand the activation of implanted dopant species and their activation a low temperatures and the repair of the damaged silicon lattice.

APPENDIX A

Step-by-step process flow for fabricating TFTs on SiOG at low temperatures.

#	Step	Process Parameters
1	Piranha Clean	Piranha Bath 10 min @ 130C Approx. 50:1 H2SO4:H2O2 (Spike if old) H2SO4: 5000mL H2O2: 100mL
2	LTO Dep Protective surface	Deposit 1000A of LTO in 6" LPCVD (top) tube Time ~4min Include monitor wafer during dep
3	Backside Moly	Tool: PE2400 Moly Dep Ar Flow: 15sccm (on flow, 21.6 sccm actual) Pressure: ~14mTorr Power: 700W Presputter ~ 300 sec (no shutter, place wafers oposite target in chamber, and do not rotate) Dep. Time: ~72 minutes
4	Backside TEOS	Deposit 2um TEOS oxide on backside to protect Mo *A6-2M TEOS LS*
5	Backside pre-amorphization	Varian 350D Dose - 3E15 Energy - 60Kev Species - F
6	P+ Backside Implant	Varian 350D Dose - 2e15 cm^-2 Energy - 35KeV Species - B11
7	Alignment Litho (Level 0)	SVG - Coat trac, pgrm: 1 GCA - Lithography Job: EAGLEPLG pass: 4 SVG - Develop, pgrm: 1 Time: ~0.64s (Si wafer)
8	Oxide Etch	10:1 BOE 560A/min (thermal ox etch rate) HF. Get etch rate from LTO monitor wafer (M1). Time = ??

9	Si Etch	LAM 490: Target depth ~1000Å Gap - 0.9cm Power: 140W CF4 - 0 sccm Pressure: 325mTorr O2 - 100 sccm Helium - 0 sccm SF6 - 150 sccm O2 - 0 sccm Time: 21sec
10	Resist Strip	Branson - O2 Ash 4" hard Ash recipe
11	Channel stop Litho (Level 0.5)	SVG - Coat trac, pgrm: 1 GCA - Lithography Job: EAGLEPLG Pass: 3 SVG - Develop, pgrm: 1 Time:
12	Channel stop implant	Varian 350D Dose = 5E12 cm-2 Energy = 35KeV Species - B11
13	Resist Strip	Branson - O2 Ash 4" hard Ash recipe
14	Dep LTO Field	Deposit 4000Å of LTO in 6" LPCVD (top) tube 425°C Calculate dep time from previous run
15	Active Litho (Level 1 BLK)	SVG - Coat trac, pgrm: 1 GCA - Lithography Device Job: EAGLEPLG PASS: 3 Cap Job: EAGLEPLG PASS: 1 SVG - Develop, pgrm: 1 Time: *~0.64s (Si wafer)*
16	Active Oxide Etch	10:1 BOE 560A/min (thermal ox etch rate) HF. Get etch rate from TEOS monitor wafer (M1). Time = TBD
17	VT Adjust Litho	SVG - Coat trac, pgrm: 1 GCA - Lithography Device Job: EAGLEPLG PASS: 5 SVG - Develop, pgrm: 1 Time: ~0.64s (Si wafer)
18	Phos VT Adjust	Varian 350D Dose - 2e11 Energy – 110 Kev Species - P31
19	Resist Strip	Branson - O2 Ash 4" hard Ash recipe

20	VT Adjust Litho	SVG - Coat trac, pgrm: 1 GCA - Lithography Device Job: EAGLEPLG PASS: 6 SVG - Develop, pgrm: 1 Time: ~0.64s (Si wafer)
21	Boron VT Adjust	Varian 350D Dose - 2e11 Energy – 35 Kev Species - B11
22	Resist Strip	Branson - O2 Ash 4" hard Ash recipe
23	HF Dip	10:1 BOE 560A/min (thermal ox etch rate) HF Time = 1:00 m:s
24	Active Litho (Level 1 SiOG)	SVG - Coat trac, pgrm: 1 GCA - Lithography SVG - Develop, pgrm: 1 Job: eagle1 PASS: 3 (SiOG) Time: 0.53s (SiOG Wafer) Focus: 0 (SiOG Wafer)
25	Silicon Etch	LAM490 - Silicon Etch Pressure: 325mTorr Power: 140W Gap - 0.9 (SiOG) CF4 - 0 sccm O2 - 100 sccm Helium - 0 sccm SF6 - 150 sccm O2 - 0 sccm Time: TBD
26	Resist Strip	PRS1000 - PRS2000 10min in each bath
27	Piranah	Piranha Bath 10 min @ 130C Approx. 50:1 H2SO4:H2O2 (Spike if old) H2SO4: 5000mL H2O2: 100mL
28	Gate Oxide Dep	Deposit 500A of LTO in 6" LPCVD (top) tube 2 runs back to back - first run verify dep rate (on M1) Time ~4min Include monitor wafer during dep

29	Gate Metal Dep	Tool: PE2400 Ar Flow: 15sccm (on flow, 21.6 sccm actual) Pressure: ~14mTorr Power: 700W Presputter ~ 300 sec (no shutter, place wafers oposite target in chamber, and do not rotate) Dep. Time: ~72 minutes
30	Gate Litho (Level 2)	SVG - Coat trac, pgrm: 1 GCA - Lithography SVG - Develop, pgrm 1 Job: EAGLEPLG PASS: 3 (Bulk) Job: EAGLE1 Pass: 3 (SiOG) Time: ~0.7s
31	Gate Etch	Drytec Quad - Moly Etch, Recipe: Moly Chamber #2 - Quartz carrier Power: 250W Pressure: 150mT SF6: 50sccm Time: 1:10 m:s !!!Check!!!
32	Resist Strip	PRS1000 - PRS2000 10min in each bath
33	Screen Ox	Deposit <u>600Å</u> of LTO in 6" LPCVD (top) tube Time ~4min Include monitor wafer during dep
34	N+ Litho (Level 3)	SVG - Coat trac, pgrm: 1 GCA - Lithography SVG - Develop pgm: 1 Job: EAGLE1 PASS: 3 (SiOG) Job: EAGLEPLG PASS: 3 (Bulk Si, SOI) Time: ~0.6s
35	N+ S/D Implant	Varian 350D Dose - 4E15 Energy - 110Kev Species - P31
36	Resist Strip	Branson - O2 Ash 4" hard Ash recipe
37	P+ Litho (Level 4)	SVG - Coat trac pgrm: 1 GCA - Lithography SVG - Develop, pgrm: 1 Job: EAGLE1 PASS: 3 (SiOG) Job: EAGLEPLG PASS: 3 (Bulk Si, SOI) Time: ~0.6s

38	P+ S/D pre-amorphization Implant	Varian 350D Dose - 3E15 Energy - 60Kev Species - F
39	P+ S/D Implant	Varian 350D Dose - 4E15 Energy - 35Kev Species - B11
40	Resist Strip	Branson - O2 Ash 4" hard ash recipe
41	Clean	Piranha Bath 10 min @ 130C Approx. 50:1 H2SO4:H2O2 (Spike if old) H2SO4: 5000mL H2O2: 100mL
42	ILD	4000Å LTO Recipe: 425°C LTO Tool: 6" ASM LPCVD
43	Anneal	Bruce Tube - 07 Recipe 735 2 hour Anneal in N2 @600C
44	Anneal	Bruce Tube - 07 Recipe 735 2 hour Anneal in N2 @650C
45	Anneal	Bruce Tube - 07 Recipe 735 2 hour Anneal in N2 @700C
46	Anneal	RTA-B 1 min Anneal in N2 @700C
47	Contact Cut Litho (Level 5)	SVG - Coat trac pgrm: 1 GCA - Lithography SVG - Develop pgrm: 1 Job: EAGLE1 PASS: 3 (SiOG) EAGLEPLG PASS: 3 (Si, SOI) Time: ~1.0s
48	Contact Cut Etch	10:1 BOE 560A/min HF *Get etch time from M3* Time: TBD????
49	Resist Strip	PRS1000 - PRS2000 10min in each bath

50	Metal Deposition	CVC601 - Aluminum Deposition 2000W ~20 sccms Argon 5.0 mtorr dep pressure 20 min for ~7500Å
51	Metal Litho (Level 6)	SVG - Coat trac pgrm: 1 GCA - Lithography SVG - Developpgrm: 1 Job: EAGLE1 PASS: 3 (SiOG) Job: EAGLEPLG PASS: 3 (Si, SOI) Time: ~0.87s
52	Metal Etch	Wet Aluminum Etchant (50°C) Use M3 as a monitor wafer Time: ~1:25 m:s
53	Resist Strip	PRS1000 - PRS2000 10min in each bath
54	Cap Litho (Level 7)	SVG - Coat trac pgrm: 1 GCA - Lithography SVG - Developpgrm: 1 Job: EAGLE1 PASS: 3 (SiOG) Job: EAGLEPLG PASS: 3 (Si SOI) Time: ~0.87s
55	Metal Cap Etch	Wet Aluminum Etchant (50°C)
56	Resist Strip	PRS1000 - PRS2000 10min in each bath
57	Backside Metal	CVC601 - Aluminum Deposition 2000W ~20 sccms Argon 5.0 mtorr dep pressure 20 min for ~7500Å
58	Sinter	Bruce Tube - 07 Recipe 41 425C H2/N2 30min

APPENDIX B

The following shows the determination of the maximum depletion width (W_d) as a function of p-type dopant concentration for a bulk silicon substrate with consideration of the metal-semiconductor workfunction difference (Φ_{MS}).

Starting substrate parameters

$$N_A = p_o - n_o \text{ and } N_D = 0$$

where

$$n(y) = n_o e^{\frac{\psi(y)}{\phi_t}} \text{ and } p(y) = n_o e^{\frac{-\psi(y)}{\phi_t}}$$

From Poisson's equation

$$\rho(y) = q(p(y) - n(y) + N_D - N_A)$$

and

$$\frac{d^2\psi}{dy^2} = -\frac{q}{\varepsilon_{Si}}\left[p_o\left(e^{-\psi(y)/\phi_t} - 1\right) - n_o\left(e^{\psi(y)/\phi_t} - 1\right)\right]$$

Knowing for a p-type material

$$p_o \approx N_A, n_o \approx \frac{n_i^2}{N_A}, \text{ and } \phi_F \approx \phi_t \ln\left(\frac{N_A}{n_i}\right)$$

Thus substituting into Poisson's equation:

$$\frac{d^2\psi}{dy^2} = -\frac{qN_A}{\varepsilon_{Si}}\left[e^{-\psi(y)/\phi_t} - 1 - e^{-2\phi_F/\phi_t}\left(e^{\psi(y)/\phi_t} - 1\right)\right]$$

Integrating

$$\mathcal{E}(y) = -\frac{d\psi}{dy} = \pm\frac{\sqrt{2q\varepsilon_{Si}N_A}}{\varepsilon_{Si}}\sqrt{\phi_t e^{-\psi/\phi_t} + \psi - \phi_t + e^{-2\phi_F/\phi_t}\left(\phi_t e^{\psi/\phi_t} - \psi - \phi_t\right)}$$

Let $\psi = \psi(y)$

Integrate from surface to bulk of silicon where the electric field is zero:

$$Q_C = -\int \frac{d\psi}{dy} = \int_0^{\psi_s} \pm \frac{\sqrt{2q\varepsilon_{Si}N_A}}{\varepsilon_{Si}} \sqrt{\phi_t e^{-\psi(y)/\phi_t} + \psi(y) - \phi_t + e^{-2\phi_F/\phi_t}\left(\phi_t e^{\psi(y)/\phi_t} - \psi(y) - \phi_t\right)}$$

Total charge (When inverted)

$$Q_C = \pm\sqrt{2q\varepsilon_{Si}N_A} \sqrt{\phi_t e^{-\psi_s/\phi_t} + \psi_s - \phi_t + e^{-2\phi_F/\phi_t}\left(\phi_t e^{\psi_s/\phi_t} - \psi_s - \phi_t\right)}$$

For practical dopant ranges Q_C can be approximated to be [31]

$$Q_C = -\sqrt{2q\varepsilon_{Si}N_A}\sqrt{\psi_s + \phi_t e^{(\psi_s - 2\phi_F)/\phi_t}}$$

Where

$$Q_C = Q_I + Q_B$$

The depletion charge is:

$$Q_B = -\sqrt{2q\varepsilon_{Si}N_A}\sqrt{\psi_s}$$

Solving for the inversion charge:

$$Q_I = -\sqrt{2q\varepsilon_{Si}N_A}\left(\sqrt{\psi_s + \phi_t e^{(\psi_s - 2\phi_F)/\phi_t}} - \sqrt{\psi_s}\right)$$

For weak inversion define [31]:

$$\xi = \phi_t e^{(\psi_s + 2\phi_F)/\phi_t}$$

Taylor Series expansion

$$\sqrt{\psi_s + \xi} = \sqrt{\psi_s} + \frac{\xi}{2\sqrt{\psi_s}} + \dots$$

And

$$\gamma \equiv \frac{\sqrt{2q\varepsilon_s N_A}}{C_{OX}}$$

Substituting in the approximation the inversion charge becomes:

$$Q_I \approx -\frac{\sqrt{2q\varepsilon_{Si}N_A}}{2\sqrt{\psi_s}}\phi_t e^{(\psi_s - 2\phi_F)/\phi_t}$$

And

$$V_{GB} \approx V_{FB} + \psi_s - \frac{Q_I(\psi_s) + Q_B(\psi_s)}{C_{OX}}$$

where $Q_I(\psi_s) << Q_B(\psi_s)$ in week inversion

$$V_{GB} \approx V_{FB} + \psi_s - \frac{Q_B(\psi_s)}{C_{OX}}$$

Solve for the surface potential from V_{GB}

$$\psi_{sa} \approx \psi_s \approx \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{GB} - V_{FB}} \right)^2$$

Knowing that [40]

$$\psi_{sa} = \frac{qN_A}{2\varepsilon_s} W_d^2$$

Solving for W_d and substituting in the surface potential approximation:

$$W_d = -\frac{t_{OX}\sqrt{qN_A\varepsilon_s} - \sqrt{2}\varepsilon_s\sqrt{\dfrac{qN_A t_{OX}^2 - 2V_{FB}\varepsilon_s + 2V_{GB}\varepsilon_s}{\varepsilon_s}}}{\sqrt{qN_A\varepsilon_s}}$$

Solving for the maximum depletion width at N_A

$$\frac{dW_d}{dN_A} = \frac{\left(V_{GB} - V_{FB} + N_A\left[\dfrac{d}{dN_A}V_{FB} \right] \right)\sqrt{\varepsilon_{Si}}}{N_A^{3/2}\sqrt{q}\sqrt{2V_{GB} - 2V_{FB} + \dfrac{N_A q t_{OX}^2}{\varepsilon_{Si}}}} = 0$$
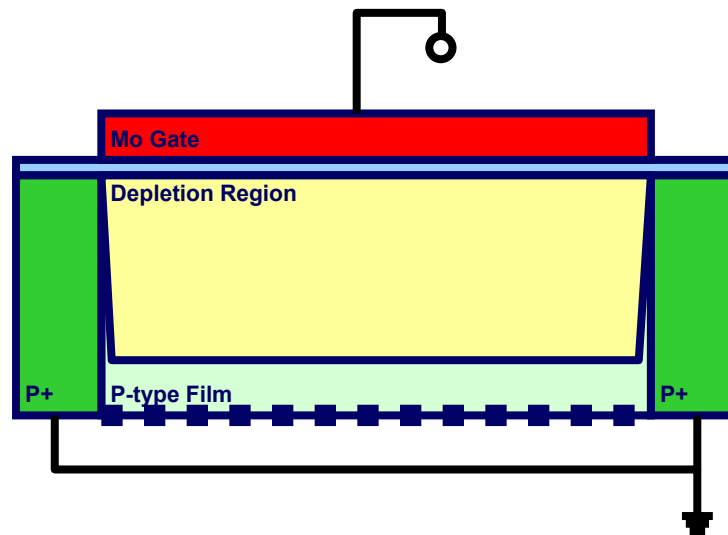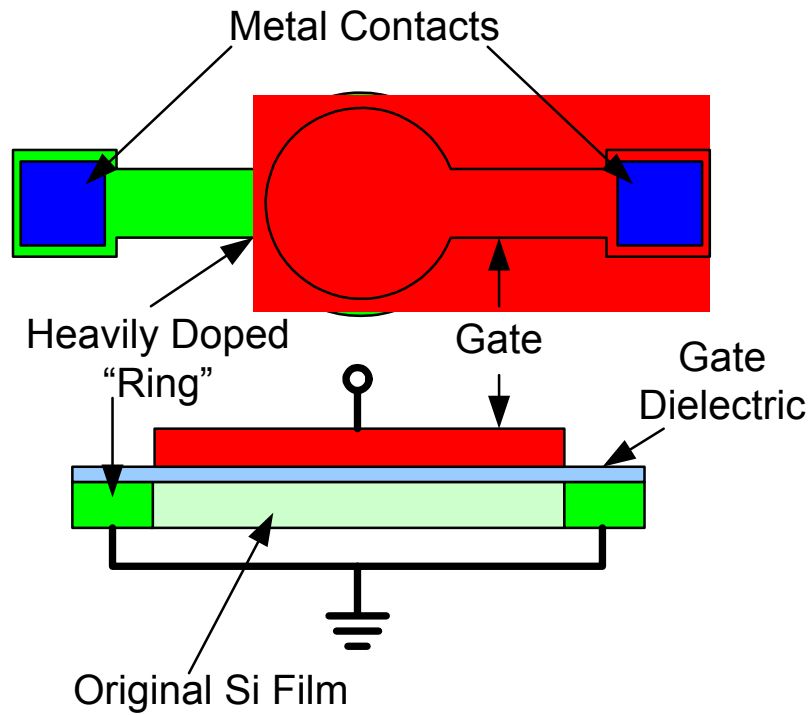
Simplifying

$$V_{GB} - V_{FB} + N_A\left[\frac{d}{dN_A}V_{FB} \right] = 0$$

The maximum depletion width occurs at:

$$\frac{V_{FB} - V_{GB}}{\dfrac{d}{dN_A}V_{FB}} = N_{AMaxWd}$$

Two dimensional MOS capacitor used in body-adjust implant studies.

Metal Contacts

Heavily Doped "Ring"

Gate

Gate Dielectric

Original Si Film

Mo Gate

Depletion Region

P+

P-type Film

P+

REFERENCES

[1] W. den Boer, Active Matrix Liquid Crystal Displays Fundamentals and Applications, Newnes, 2005

[2] A. Kumar, A. Nathan, G. Jabbour, "Does TFT Mobility Impact Pixel Size in AMOLED Backplanes?," IEEE Trans. Elec. Devices, vol. 52, No. 11, pp. 2386-2394, 2005

[3] Y. Matsueda, Y. Park, S. Choi, H. Chung, "Trends of System on Panel," IMID '05 Digest, pp. 1-4, 2005

[4] P. K. Weimer, "The TFT – A New Thin-Film Transistor," Proc. IEEE Vol 51., pp. 1462, 1962

[5] R. L. Saxer, Development and Characterization of High Performance Transistors on Glass, RIT M.S. Thesis, 2006

[6] W. E. Spear, P. G. LeComber, "Substitutional Doping of Amorphous Silicon," Solid State Comm., Vol. 17, pp. 1193, 1975

[7] C. R. Kagan, P. Andry, Thin-Film Transistors, Marcel Dekker, Inc., 2003

[8] L. Wang, T Fjeldly, B. Iniguez, H. Slade and M. Shur, "Self-Heating and Kink Effects in a-Si:H Thin Film Transistors," IEEE Trans. Electron Devices, Vol. 47, no. 2 pp. 387-397, 2000

[9] A. Natthan, P. Servati, K. Karim, D. Striakhilev, and A. Sazonov, "Thin film transistor integration on glass and plastic substrates in amorphous silicon technology," IEE Proc.-Circuits Devices Syst. Vol. 150, No. 4, pp. 329-338, 2003

[10] P. Servati and A. Nathan, "Modeling of the static and dynamic behavior of hydrogenated amorphous silicon thin film transistors," J. Vac. Sci. Technol. A, Vol. 20, No. 3, pp. 1038-1042, 2002.

[11] R. A. Street, *Hydrogenated Amorphous Silicon,* Cambridge University Press, 1991

[12] S. Jagar, M. Chan, M. Poon, H. Wang, M. Qin, P. Ko, Y. Wang, "Single Grain Thin-Film Transistor (TFT) with SOI CMOS Performance Formed by Metal-Induced-Lateral-Crystallizatoin," Conc. Rec., IEDM, pp. 293-296, 1999

[13] G.A. Bhat, Z. Jin, H.S. Kwok, M. Wong, "Efects of longitudinal grain boundaries on the perforamance of MILC-TFT's," *IEEE Elec. Dev. Let.* Vol. 20, No. 2, pp. 97-99, 1999

[14] G. Giust and T. Sigmon, "Hihg-performance thin-film transistors fabricated using excimer laser processing and grain engineering," IEEE, Trans. Electron Devices, Vol. 45, No. 4, pp. 925-932, 1998

[15] H. Wang, M. Chan, S. Jagar, V. Poon, M. Qin, Y. Wang, P. Ko, "Super thin-film transistors with SOI CMOS performance formed by a novel grain enhancement method," IEEE Trans. Electron Devices, Vol. 47, No. 8, pp. 1580-1586, 2000

[16] Shahidi, G. G., "SOI Technology for the GHz era," IBM J. Res. & Dev., Vol. 46, No. 2/3 2002

[17] K. Brenstein, N. Rohrer, *SOI Circuit design concepts,* Kluwer Academic Publishers, Boston, MA 2000

[18] Hanajiri, T., "Scaling rules for SOI MOSFETs operating in the fully inverted mode," Solid State Electronics, Vol. 48, pp 1943-1946, 2004

[19] G. K. Celler and S. Cristoloveanu, "Frontiers of silicon-on-insulator," *Journal of Applied Physics*, Vol. 93, No. 9, pp. 4955-4978, 2003

[20] J. Colinge, *Silicon-on-Insulator Technology,*3rd ed. Springer, New York City, New York 2004

[21] S. Krishnan and J. Fossum, "Grasping SOI Floating-Body Effects," *IEEE Cir. And Dev. Mag.*, Vol. 14, No. 4, pp. 32-37, 1998

[22] *Corning®EAGLE²⁰⁰⁰™ AMLCD Glass Substrates*, Product information brochure, 2003, http://www.corning.com

[23] Saxer, Robert L., Development and *Characterization of High Performance Transistors on Glass.* Master of Science Thesis, 2005, Chapter 4

[24] W. Kern and D. A. Puotinen, "Cleaning solutions based on hydrogen for use in silicon semiconductor technology," *RCA Rev.* Vol. 31, No. 2, pp. 187-206, 1970

[25] K. J. Seu, A. P. Pandey, F. Haque, E. A. Proctor, A. E. Ribbe, and J. S. Hovis, "Effect of surface treatment on diffusion and domain formation in suppored lipid bilayer," *Biophys. J.* 2007

[26] E. Woodard *et. al.*, *IEEE UGIM Proc.* Vol. 16 (2006)

[27] B.M. Wilamowski, R.C. Jaeger, and J.N. Fordemwalt, "Buried-channel MOS transistor with punch-through," *Solid-State Electronics,* Vol. 27, No. 8-9, pp. 811-815, 1984

[28] T. Nozaki, H. Okabayashi, and K. Higuchi, "Ion Implantation masking ability degradation in high temperature annealed Mo films [MOSFET]," *Jap. Journal of Applied Physics*, Vol. 20, No. 6, pp. 1121-1127, 1981

[29] J.M. Bernhard, A. Rouse, E.D. Sosa, D.E. Golden, B.R. Chalamala, S. Aggarwal, B.E. Gnade, R. Ramesh, "Photoelectric workfunctions of metals oxide films and emission characteristics of molybdenum emitter tips with oxide coatings," *Proceedings of the IEEE International Vacuum Microelectronics Conference, IVMC*, p 32-33, 1998

[30] M.H. Juang, T.Y. Lin, and S.L. Jang, "Formation of Mo gate electrode with adjustable work function on thin Ta_2O_5 high-k dielectric films, *Solid-State Electronics* Vol. 50, No. 2 pp. 114-118, 2006

[31] Y. Tsividis, *Operation and Modeling of The MOS Transistor,* 2nd ed. Oxford University Press, Oxford, New York, 1999

[32] J. Colinge, *IEEE Trans. Elec. Dev.* No. 37, p. 718 (1990)

[33] J.R. Hauser, "Extraction of Experimental Mobility Data for MOS Devices," *IEEE Trans. on Elec. Dev.,* Vol. 43, No. 11, pp. 1981-1988, 1996

[34] N. Lifshitz and S. Luryi, "Enhanced channel mobility in polysilicon thin film transistors," *IEEE Elec. Dev. Let.,* Vol. 15, No. 18, pp. 274-276, 1994

[35] Park, Jin-Goo, "Hydrophilization of process wafers in dilute hydrogen peroxide solution and ozonzated dionized water and its effects on defects and gate oxide integrity." *Japanese Journal of Applied Physics*, Vol. 36, No. 9A, pp 5416-5420, 1997

[36] Kalani J. Seu, Anjan P. Pandey, Farzin Haque, Elizabeth A. Proctor, Alexander E. Ribbe and Jennifer S. Hovis, "Effect of Surface Treatment on Diffusion and Domain Formation in Supported Lipid Bilayers." *Biophysical Journal*, Vol. 92, pp. 2445-2450, 2007

[37] Kern, W., Poutinen, D.A., "Cleaning solutions based on hydrogen for usi in silicon semiconductor tenoclogy." *RCA.* Vol. 31, No. 2, pp. 187-206, 1970

[38] Glick, Jeffrey S., "Characterization of deposition and removal of metallic impurities of the RCA standard clean." *Conference Proceedings – Annual Semiconductor Pure Water and Chemicals Conference.* No pt 2, pp. 93-102, 1993

[39] Ramkumar, J., Sudarsan, V., Chandramouleeswaran, S., Shrikhande, V., Ravindran, P., Kulshreshtha, S., Makherjee, T., "Structural studies on boroaluminosilicate glasses", *Journal of Non-Cystalline Solids.* Vol. 354, No. 15-16, pp. 1591-1597, 2007

[40] S.M. Sze and K.K. NG, *Physics of Semiconductor Devices,* 3rd Ed., John Wiley & Sons, Hoboken, New Jersey, 2007

[41] Atlas User's Manual, Silvaco Data Systems, Inc., Santa Clara, CA, 2007

[42] Lombardi, C., Manzini, S., Saporito, A., Vanzi, M., "A Physically Based Mobility Model for Numerical Simulation of Nonplanar Devices," *IEEE Trans. On Elec. Dev.,* Vol. 7, No. 11, pp. 1164-1171, 1988

[43] Darwish, M., Lentz, J., Pinto, M., Zeitzoff, P., Krutsick, T., Vuong, H., "An Improved Electron and Hole Mobility Model for General Purpose Devices Simulation," *IEEE Trans. on Elec. Dev.,* Vol. 44, No. 9, pp. 1529-1538, 1997

[44] Keeney, S., Piccinini, F., Morelli, M., Mathewson, A., Lombardi, C., Beg, R., Ravazzi, L., Cantarelli, D., "Complete Transient Simulation of Flash EEPROM Devices," *IEEE IEDM Conference Proc.*, pp. 201-204, 1990

[45] G.K. Giust and T.W. Sigmon, "High-performance thin-film transistors fabricated using excimer laser processing and grain engineering," *IEEE. Trans. on Elec. Dev.* Vol. 45, No. 4, pp. 925-932, 1998

[46] R. Paetzel, L. Herbst, F. Simon, "Laser annealing of LTPS," *Proceedings of the SPIE - The International Society for Optical Engineering*, Vol. 6106, 2006