Ferroelectric HfO_2 Thin Films for FeFET Memory Devices

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Outline

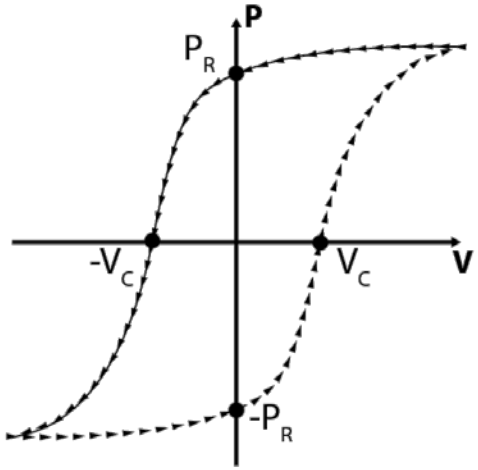
- Introduction and Background
- Project Objectives
- Process Design
- Mask Design
- Process Development
- Final Devices and Testing
- Conclusions and Future Work

Introduction

- Big Data and Data Analytics are increasingly important.
  - Requires more storage, and with more data comes more power consumption.
- FeFETs offer advantages over conventional non-volatile memory such as Flash or Phase Change Memory.
  - Reduced operating voltages for low-power operation.
  - Faster read and write speeds in the ~100 ns range and lower. [2]

Background on Ferroelectrics

- Ferroelectricity is a material property where the material has the ability to have reversible spontaneous polarization from an applied electric field.
- Characteristic Parameters:
  - Remnant Polarization (P_R): The amount of polarization charge with no applied electric field
  - Coercive Voltage or Field (V_C/E_C): The amount of applied voltage or field that results in no polarization.



Representative polarization charge [µC/cm^2] vs. applied voltage [V].

Challenges with Traditional FE Materials

- Common FE materials: Lead Zirconate Titanate (PZT) and Strontium Bismuth Tantalate (SBT)
  - Incompatibility with CMOS technology due to inter-diffusion of silicon and FE components.
  - Increased interface trap charges, so severe it can mask the ferroelectric effect.
  - Traditional FE materials have much lower coercive fields on the order of 50-100 kV/cm. Requires thicker FE layer to achieve sufficiently large memory window.

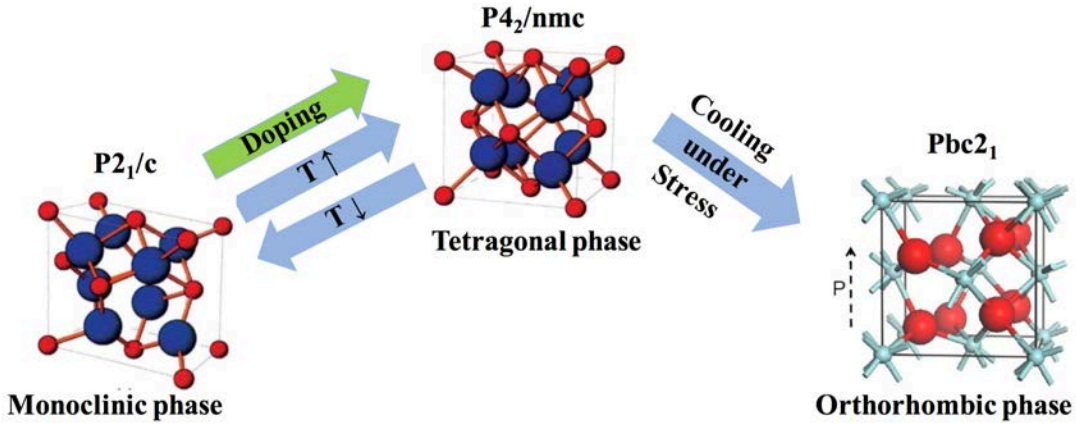
$$Memory\ Window = V_{T,OFF} - V_{T,ON}$$

$$MW_{max} = 2E_c \times t_{FE}$$

$$V_c = E_c \times t_{FE}$$

Doped HfO_2

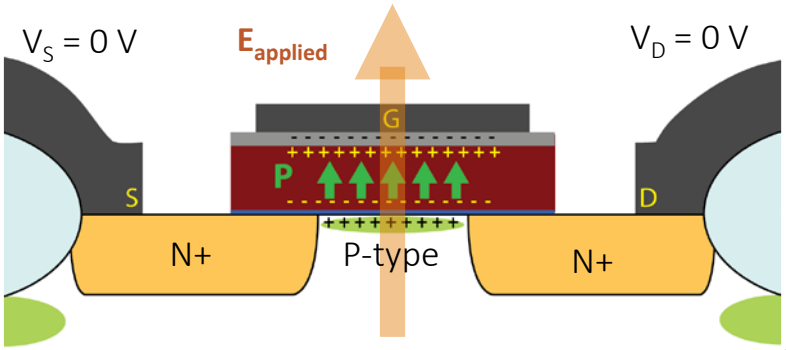
- Benefit of high process compatibility in CMOS processing.
- Standard bulk and thin film hafnium oxide is centrosymmetric and doesn't exhibit ferroelectric behavior.
- Thin film (~30 nm or less) doped HfO_2 can be induced into the non-centrosymmetric orthorhombic phase which is ferroelectric (FE)
  - Via incorporation stress from cation dopants such as silicon and capping layers. [1,2]

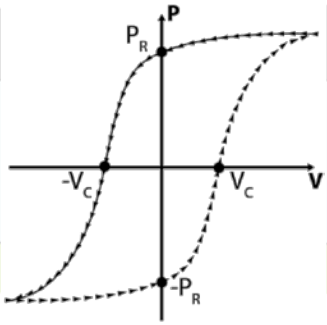


Relationship between HfO_2 crystalline phases. [2]

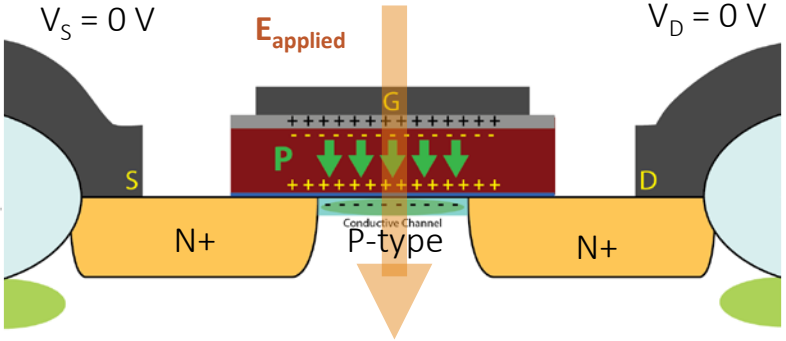
NMOS FeFET Device Operation:

OFF State: $V_G < -V_C$





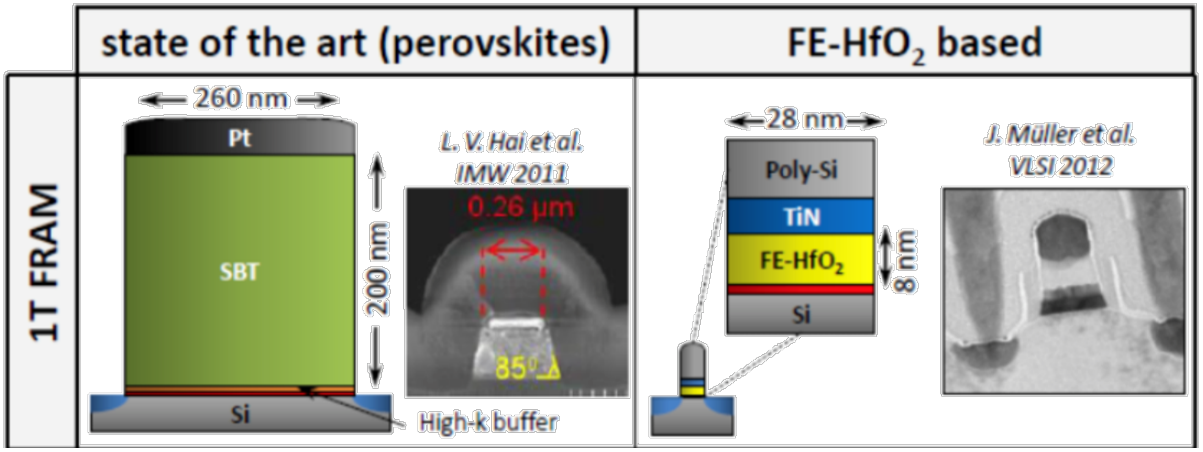
ON State: $V_G > V_C$

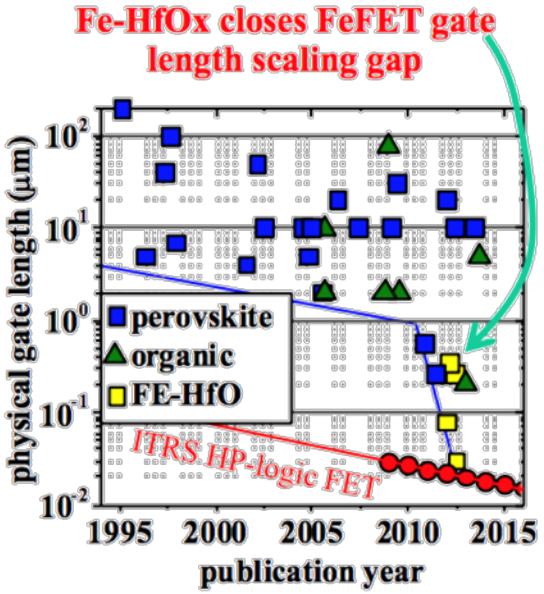


- Negative surface charge in FE layer enhances the positive charge in the channel, increasing V_T.
- Positive surface charge in FE layer depletes the positive charge in the channel, decreasing V_T.

HfO_2 Based FeFET Memory Technology Advantages

- Uses a 1-T design like flash – enables high density
  - Higher coercive fields enables more scalable devices.
  - Traditional FeRAM uses 1T-1C





ITRS Summer Meeting, Palo Alto, CA, July 11-12, 2015

Project Objectives

- Design NMOS FeFET Process
  - Develop Mask Set
    - 4–Level mask design inspired by RIT PMOS metal gate and sub-CMOS processes.
  - Develop Process Flow
    - Si:HfO_2 deposition and anneal done at NaMLab in Dresden, Germany using atomic layer deposition (ALD).
    - Enable etching of ALD Si:HfO_2 in the SMFL.
  - Fabricate FeFET devices
- Demonstrate a memory device

Process Design

- The process was designed to be robust and enable the highest probability to realize devices using a conservative mask design.
  - 39-step process

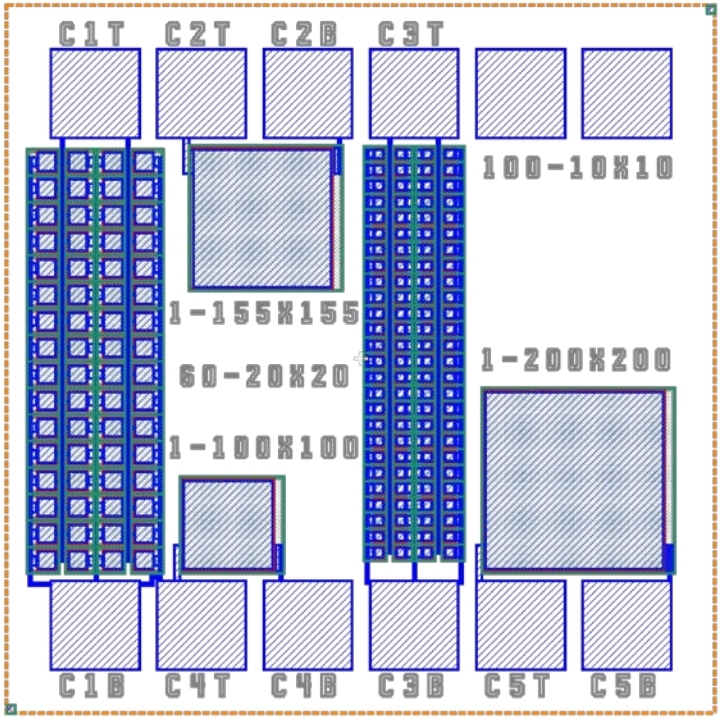
- Requires a low thermal budget (< 600 ^{o}C) after the Si:HfO2 deposition. This restriction led to:
  - Non-self-aligned process.
  - No ability to use silicide S/D.
  - No inter-level-dielectric to reduce charges from low-temperature oxides

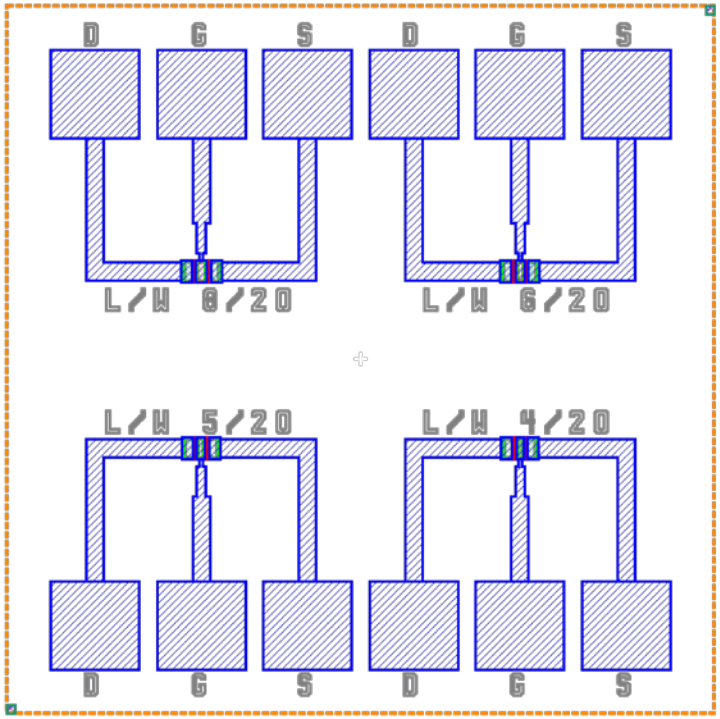
Mask Design

- 4-Levels for FeFET process flow.
- The full chip layout includes a variety of test structures:
  - Array of FeFETs with varying dimensions,
  - MFIS capacitors
  - TLMs
  - CBKRs
  - Van Der Pauw's structures
  - Resolution and alignment marks

Mask Design

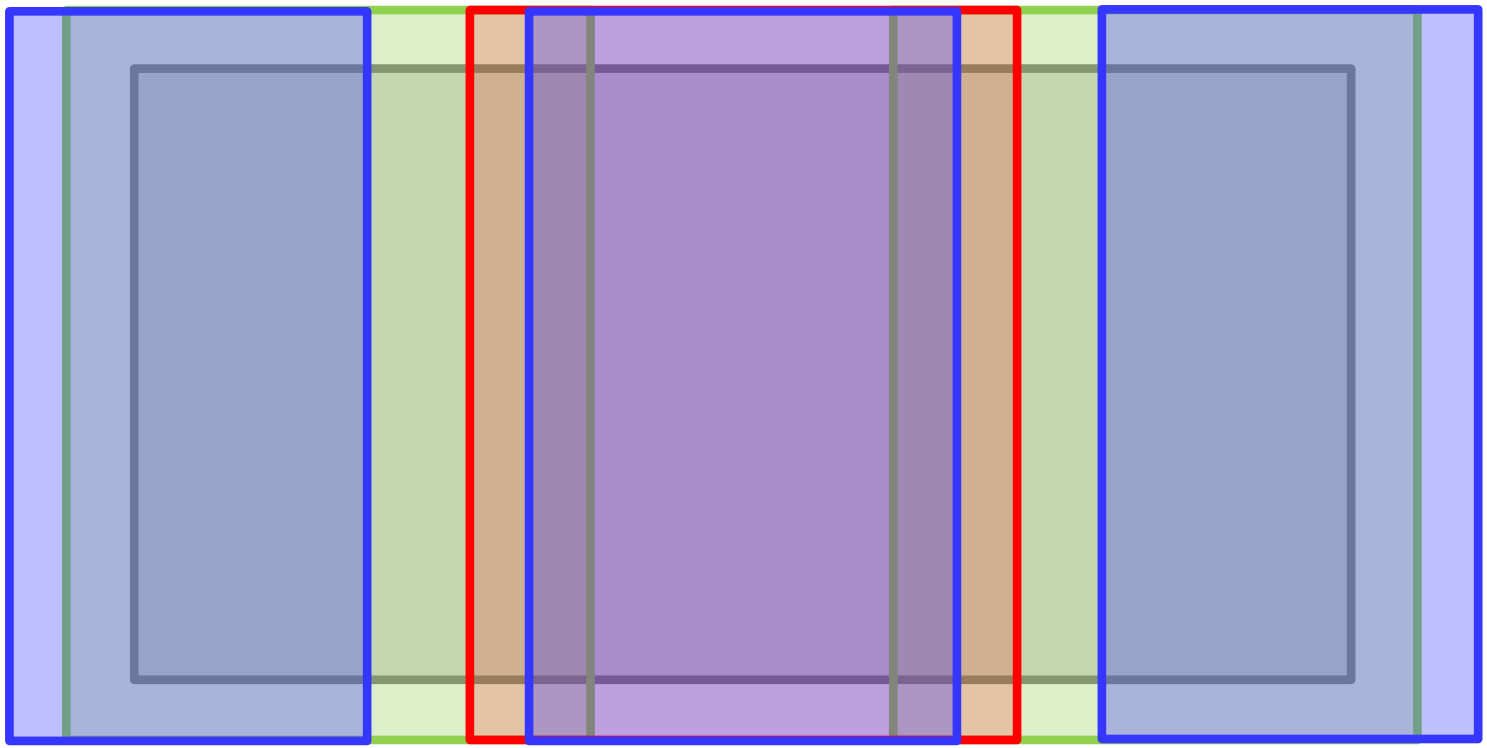
- An MFIS capacitor array is used to test the FE film without influence from the semiconductor depletion.
- Various FeFET dimensions were created.



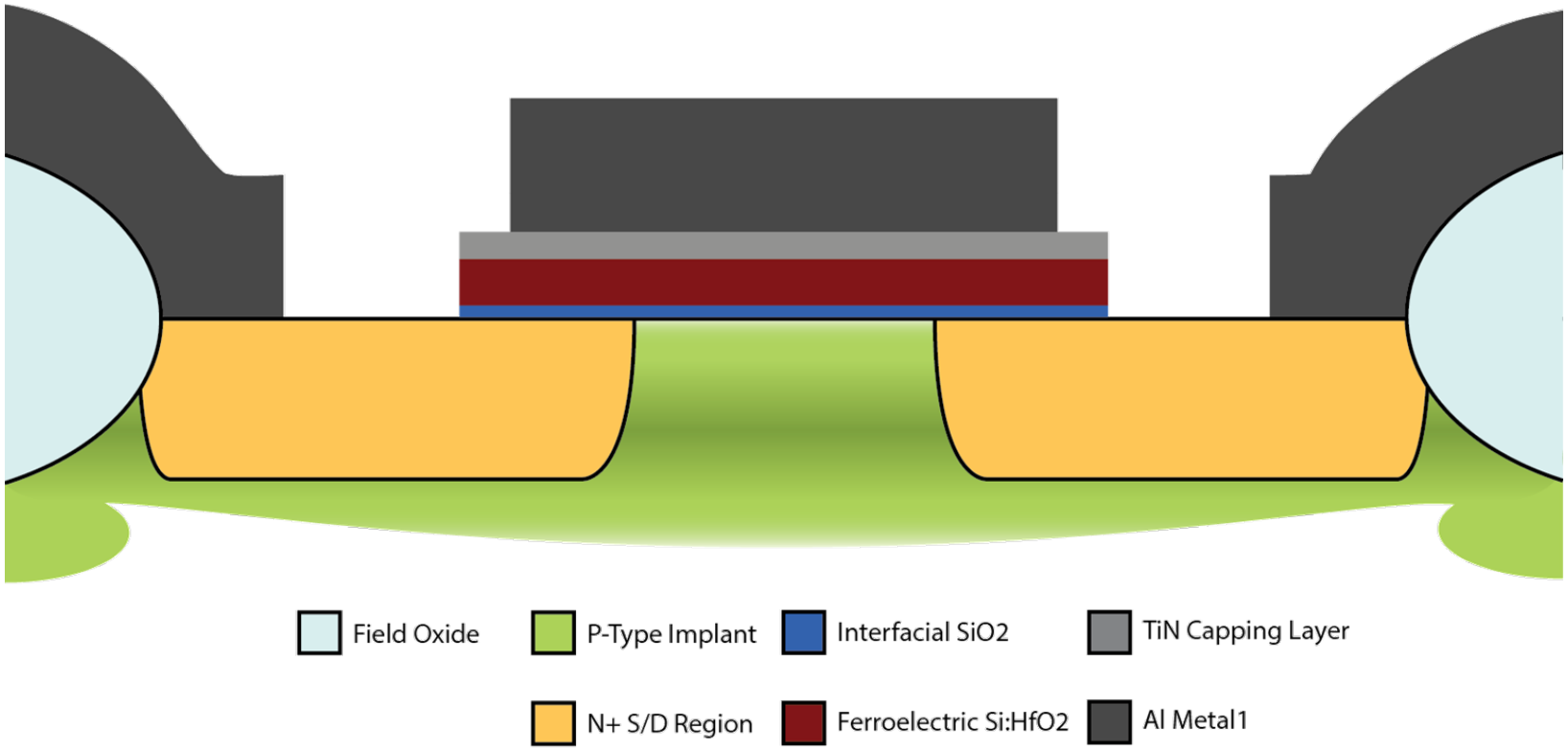


Mask Design FeFET

- A closer look at the FeFET layout.
  - **Active**, **S/D**, **Gate**, **M1**



Final Device Cross-Section



Process Development

- There was no reliable etch process at RIT for HfO2.
- A process was developed using the LAM 4600 and N_2, BCl_3, CL_2, and Ar to get an etch rate of 5.3 nm/min. The flow ratios were defined to be the same as [3].

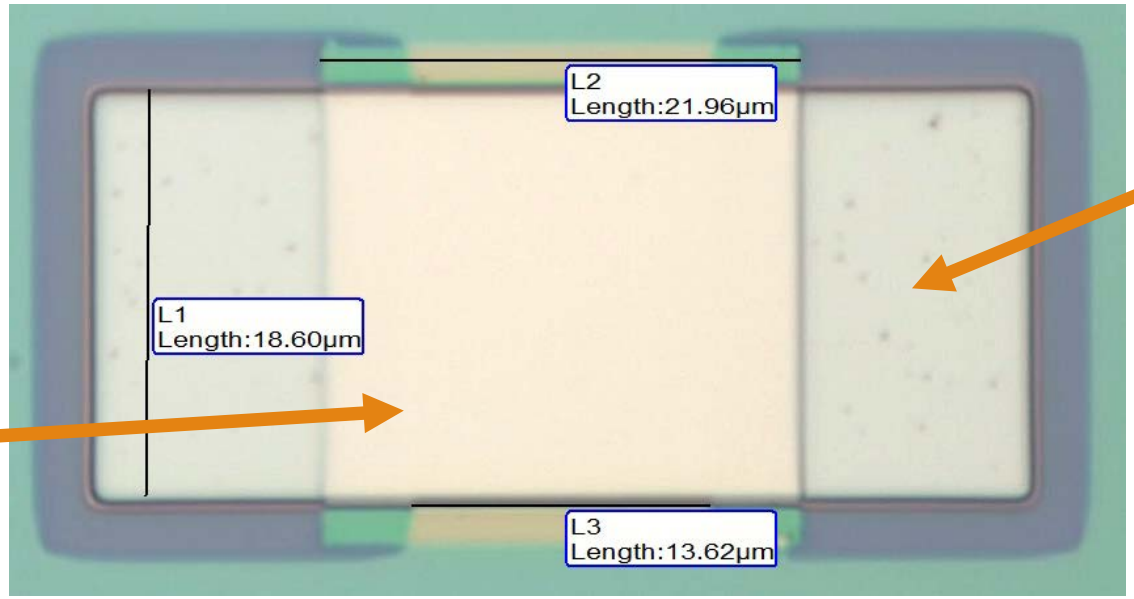
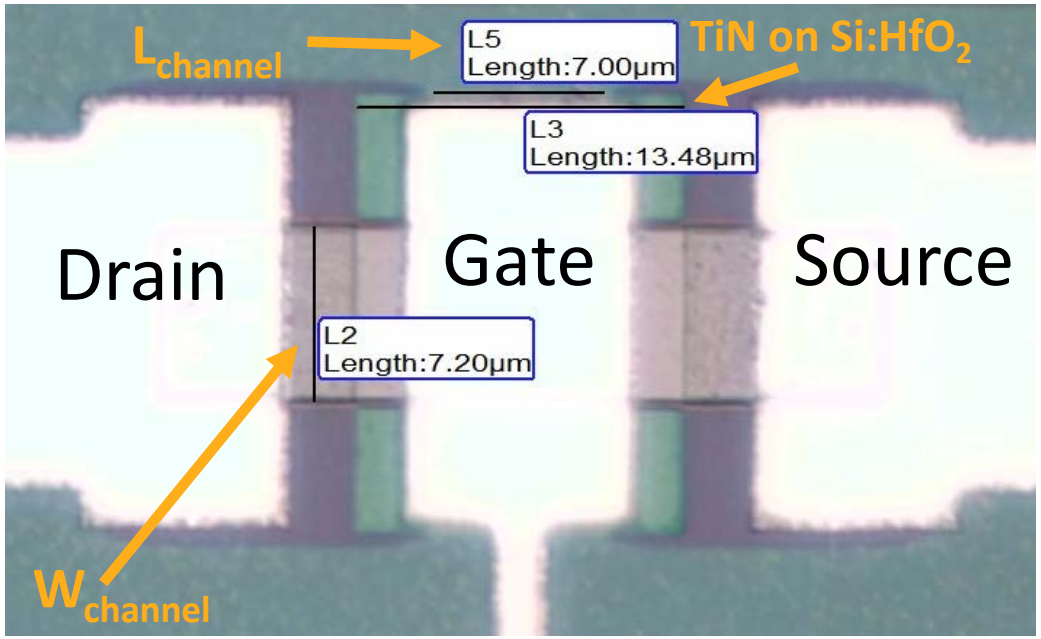


Image of FeFET device after the TiN and Si:HfO_2 stack has been etched.

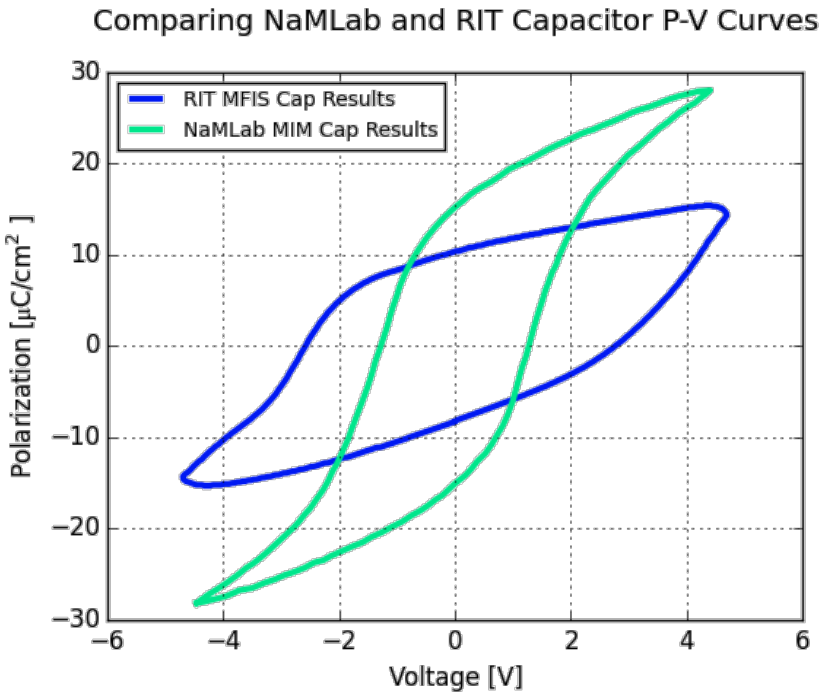
Final Device

- Capture of a L=10µm and W=10µm FeFET completed device. Some loss in W due to LOCOS and loss in L due to diffusion of carriers and variation in lithography.



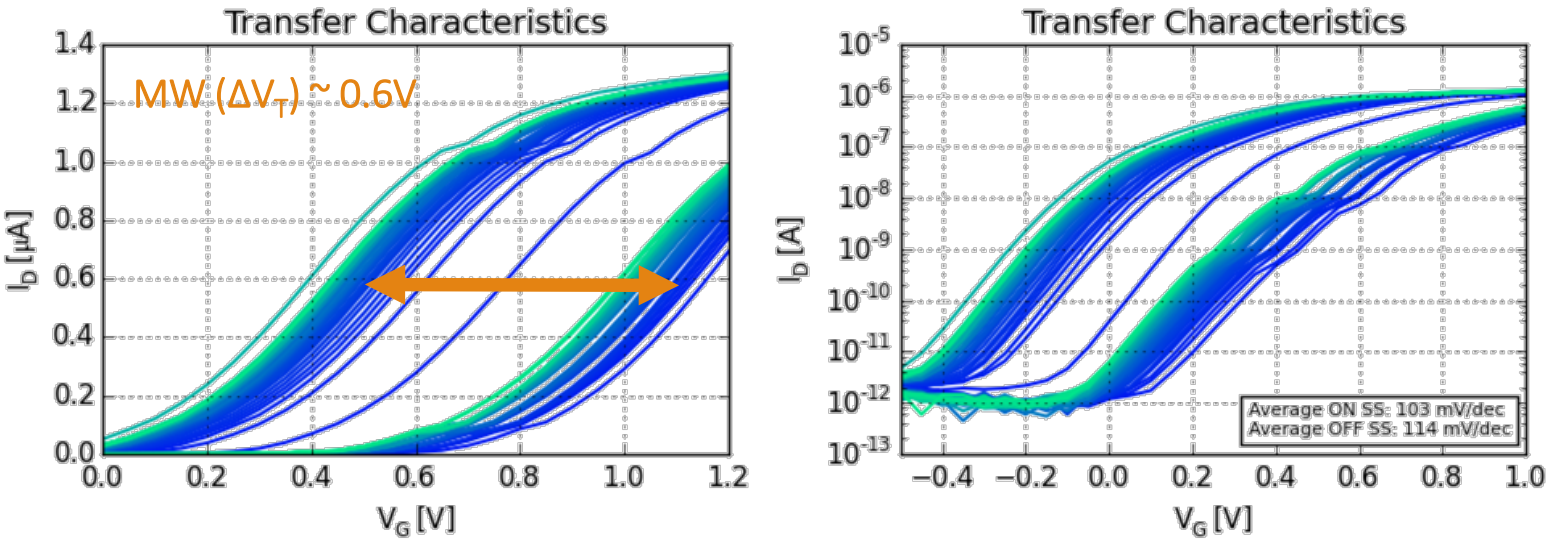
FE Capacitor Results

- Confirmation of FE Si:HfO2 using the aixACCT TF1000 FE Tester on capacitors.
- The differences can be attributed to the difference in material stack and the process variation.
- Degradation due to many factors such as non-switching domains, depolarization fields, and interface charges.



FeFET Transfer Characteristics

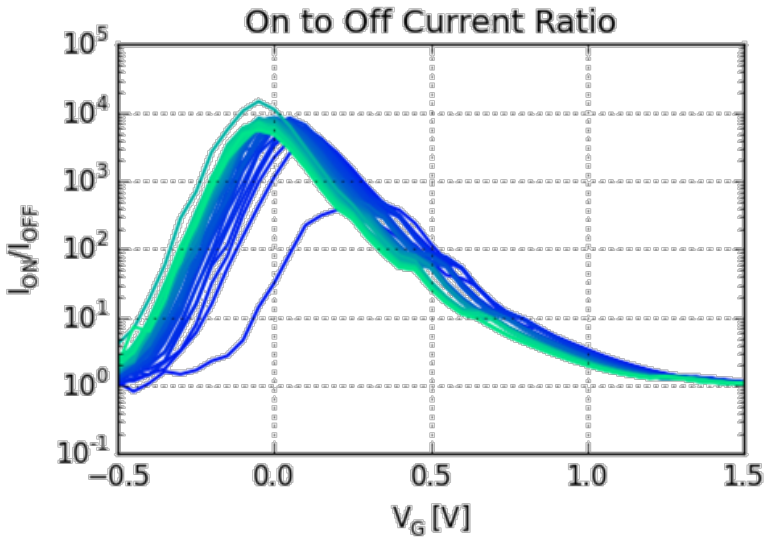
L = 5 µm, W = 15 µm

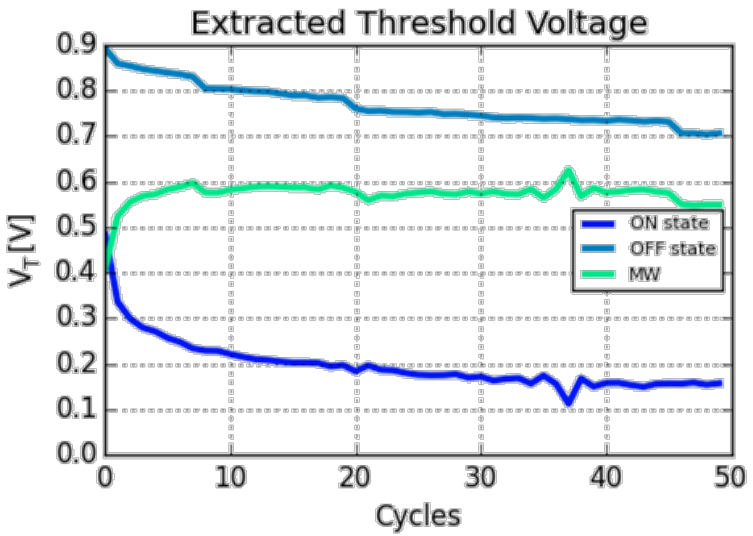


- Cycling the FE layer helps to allow domains to move more freely for full switching.
  - 50 cycles, blue is the starting cycle the plot trends toward light green as the number of cycles increases.
- Device shows a memory window and obvious shift in threshold voltage, indicating the FE Si:HfO_2 is actually switching as designed.

Memory Window

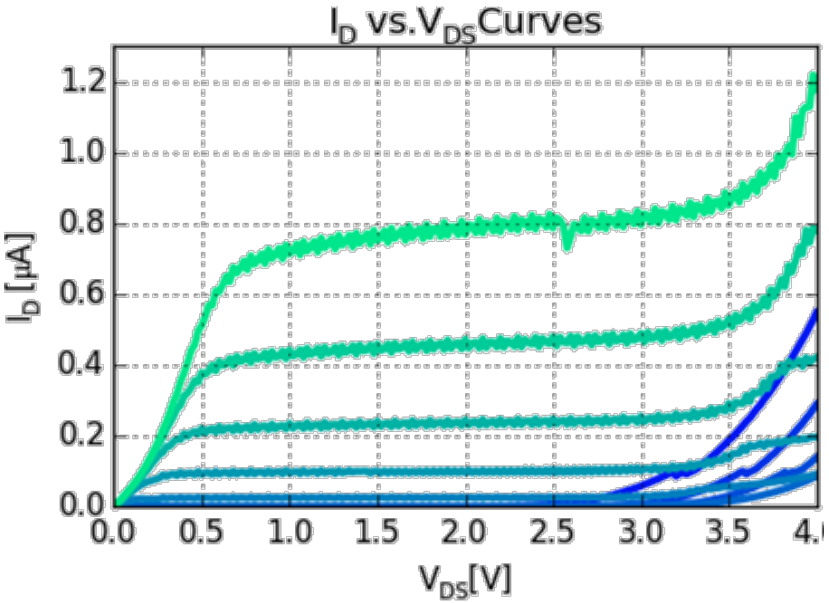
L = 5 µm, W = 15 µm





- The largest difference in the ON and OFF current will give the best read out of the current state of the device. Four orders of magnitude difference at ~0.0 V.
- Steady decrease in V_T for both states indicate trapping mechanisms

I_D vs. V_{DS} Characteristics



- L=20 µm and W= 15 µm device with V_G increasing from 0.0 V to 2.25 V in 0.25 V steps.
- Device shows punch through at high V_{DS}.
- Punch through occurs at lower V_G due to less gate influence on the channel.

Conclusions

- The process that was developed, demonstrates functioning n-channel FeFET for use as a memory device with standard CMOS compatible Si:HfO2.
  - ALD Si:HfO_2 was etched using chlorine based gases with an etch rate of 5.3 nm/min
  - The MFIS capacitors:
    - Remnant polarization: ~10 µC/cm^2
    - Coercive voltage: ~2.5 V
- FeFET demonstrated a memory window of ~0.6 V, independent of the transistor dimensions.

Future Work

- Further understanding memory window
  - Understanding parameters that influence memory window.
- Optimization of process flow to improve ferroelectric behavior
- Avoid high contact resistance:
  - Incorporate silicided S/D regions before ALD
  - Additional HF dip should be used before Al sputter.

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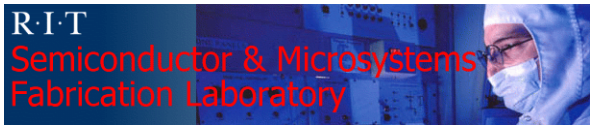

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References

[1] T. S. Boscke, J. Muller, D. Brauhaus, U. Schroder, and U. Bottger, “Ferroelectricity in hafnium oxide thin films,” *Applied Physics Letters*, vol. 99, no. 10, 2011.

[2] E. Yurchuk, *Electrical Characterisation of Ferroelectric Field Effect Transistors based on Ferroelectric HfO2 Thin Films*. Logos Verlag Berlin GmbH, 2015.

[3] Y. H. Joo, J. C. Woo, X. Yang, and C. I. Kim, "Temperature Dependence on Dry Etching of Hafnium Oxide Using an Inductively Coupled Plasma," Ferroelectrics, vol. 406, pp. 176-184, 2010.