

# **Silicon Photonic Devices Manufactured using Double- Patterned i-Line Lithography**

Patsy Cadareanu

Advisors: Drs. Stefan Preble, Robert Pearson, Dale Ewbank



# Presentation Overview

1. Project Goals
2. Photonics Overview
  - A. Waveguides
  - B. Ring Resonators
3. Process
4. Results
5. Acknowledgements

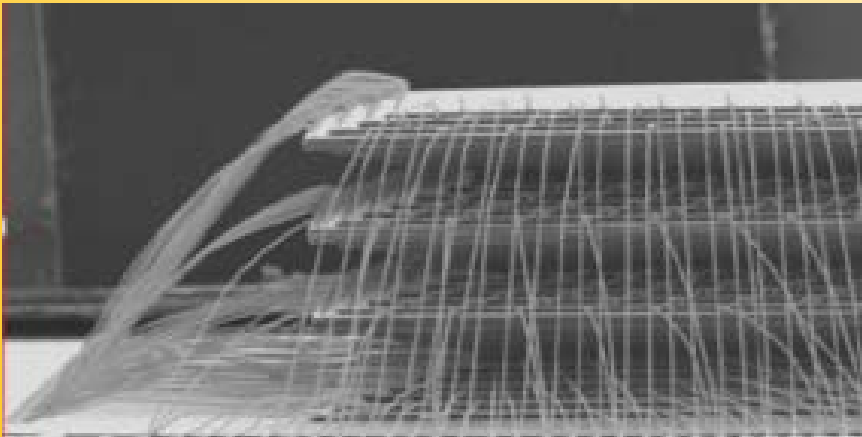
# Project Goals

**Primary Goal: To create working photonic waveguides on a-Si in the RIT SMFL**

- Characterize a double patterned i-line lithography process for sub-300nm waveguide spacings
- Develop a silicon etch process optimized for sidewall angle and smoothness
- Demonstrate working waveguides and ring resonators

# What is “photonics”?

- Study of the transmission and detection of photons
- Integrated photonics is the intersection of photonics and microelectronics
- A necessary next step



Densely integrated metal interconnects



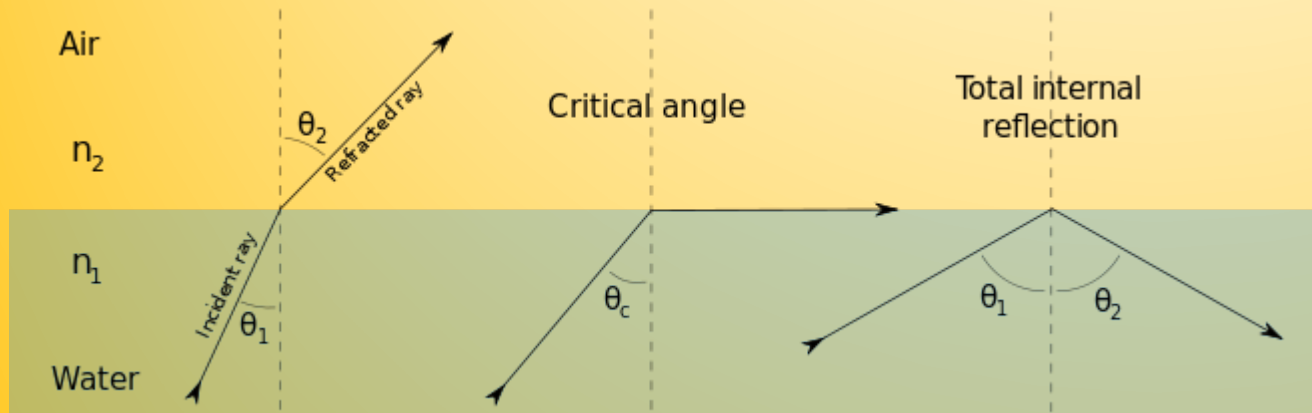
Fiber Optics

# Total Internal Reflection

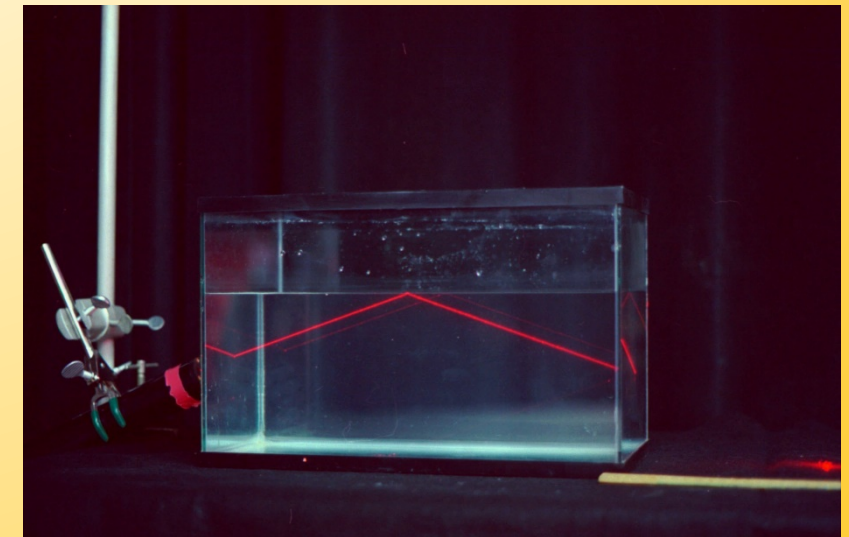
Consider the example of water and air:

$$n_{\text{water}} = n_1 = 1.33$$
$$n_{\text{air}} = n_2 = 1$$

$$n_1 > n_2$$



$$\theta_c = \theta_i = \arcsin\left(\frac{n_2}{n_1}\right) \rightarrow \theta_c = 49.76^\circ$$



Visual representation of total internal reflection

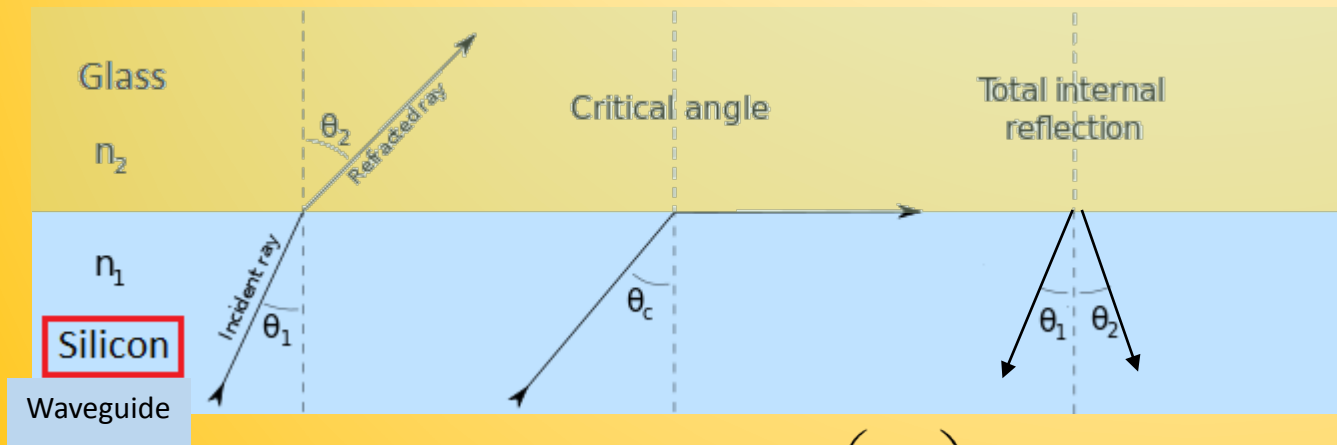


# Total Internal Reflection: Silicon edition!

What if silicon was used with oxide (glass) as cladding?

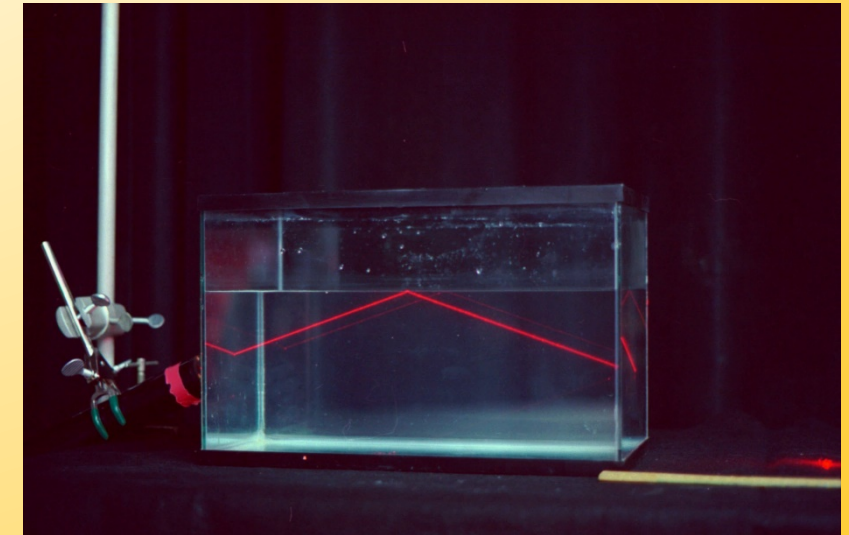
$$n_{\text{silicon}} = n_1 = 3.44$$
$$n_{\text{glass}} = n_2 = 1.45$$

$$n_1 > n_2$$



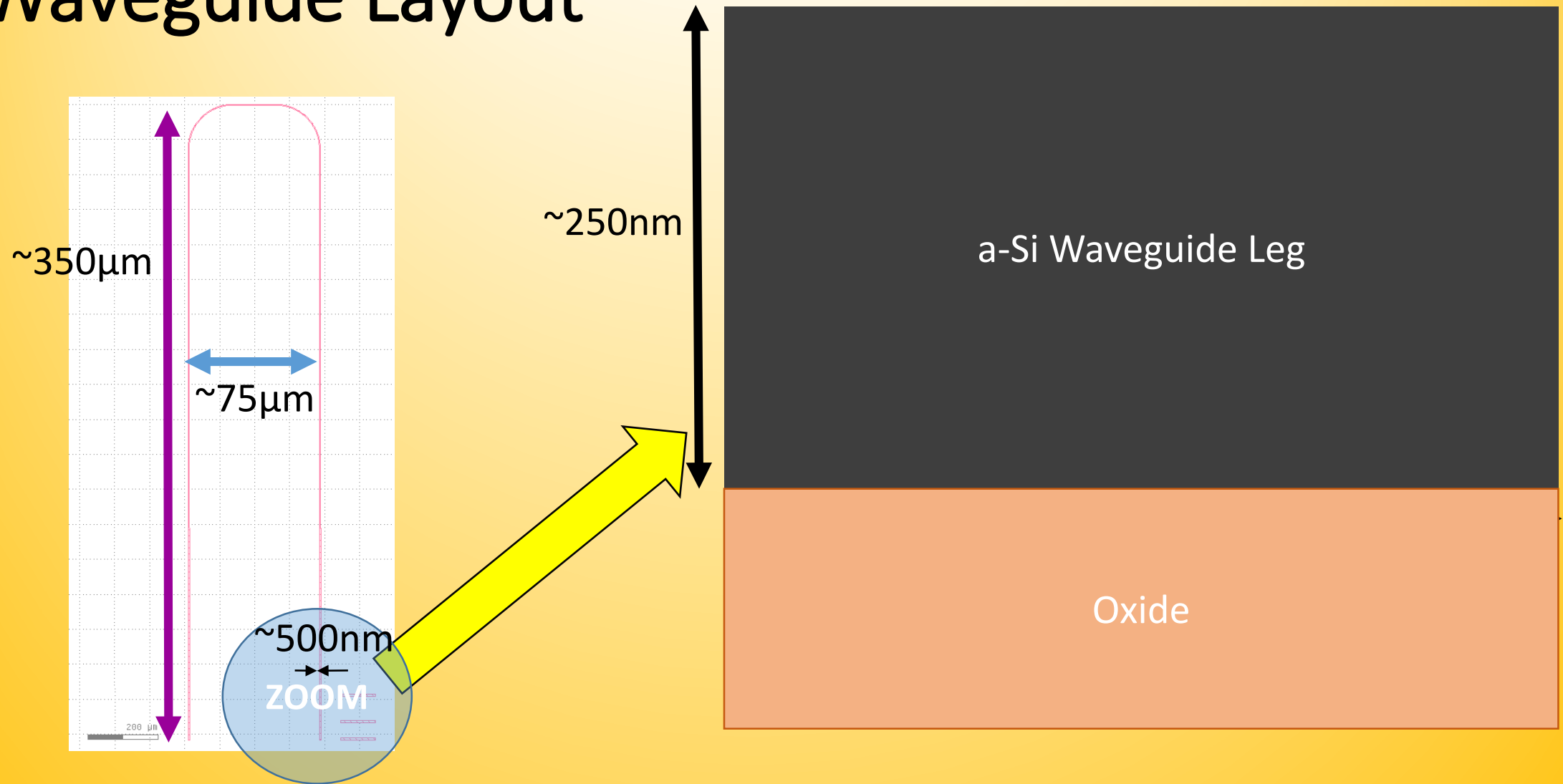
$$\theta_c = \theta_i = \arcsin\left(\frac{n_2}{n_1}\right)$$

$$\rightarrow \theta_c = 24.93^\circ$$

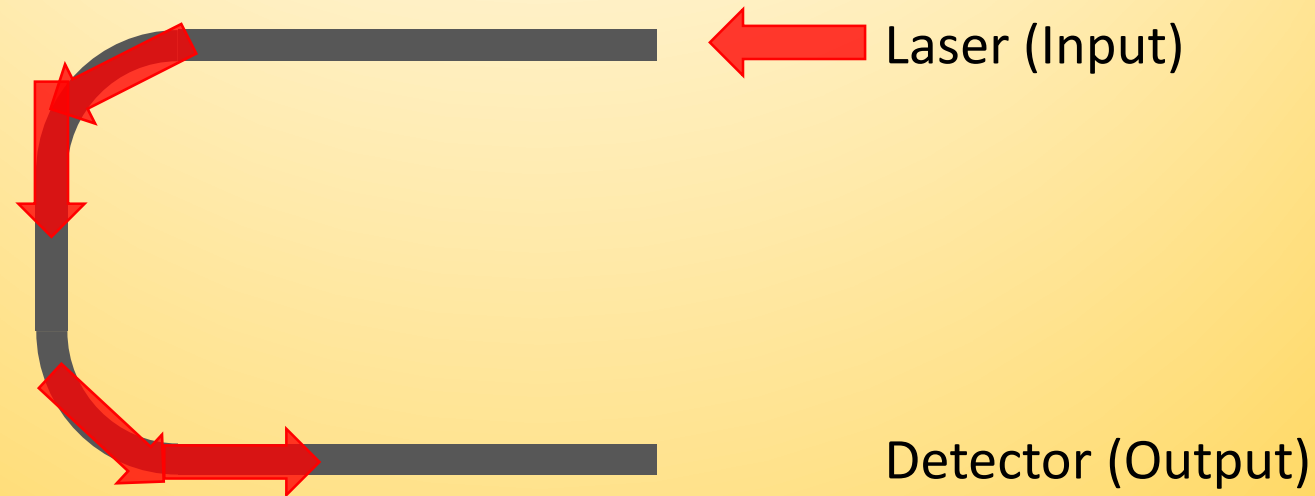


Visual representation of total internal reflection

# Waveguide Layout



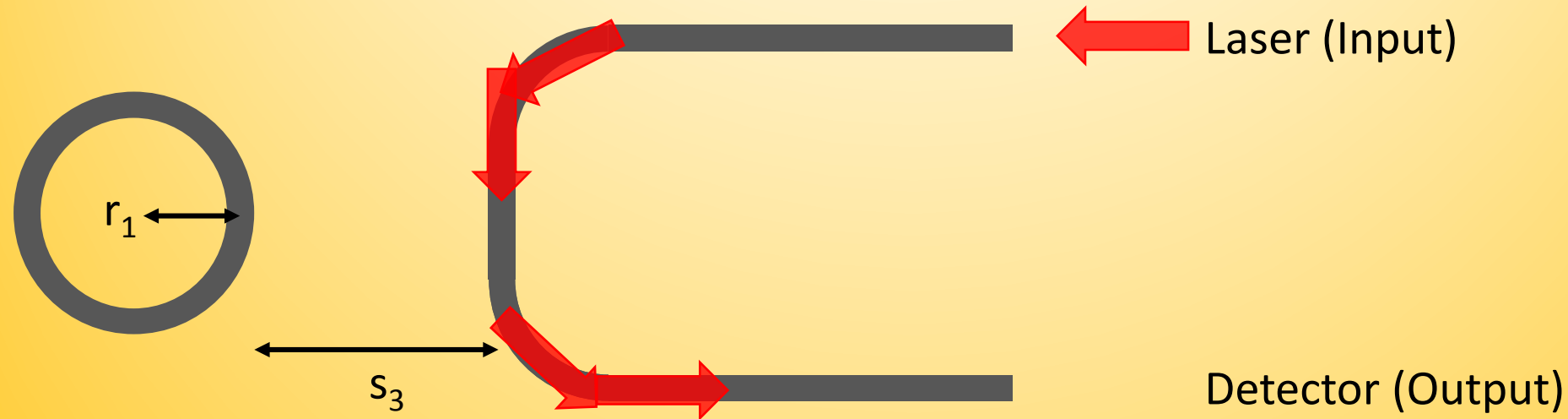
# How does a waveguide work?



**High transmission will occur in this case because the light has nowhere else to go but to the detector**

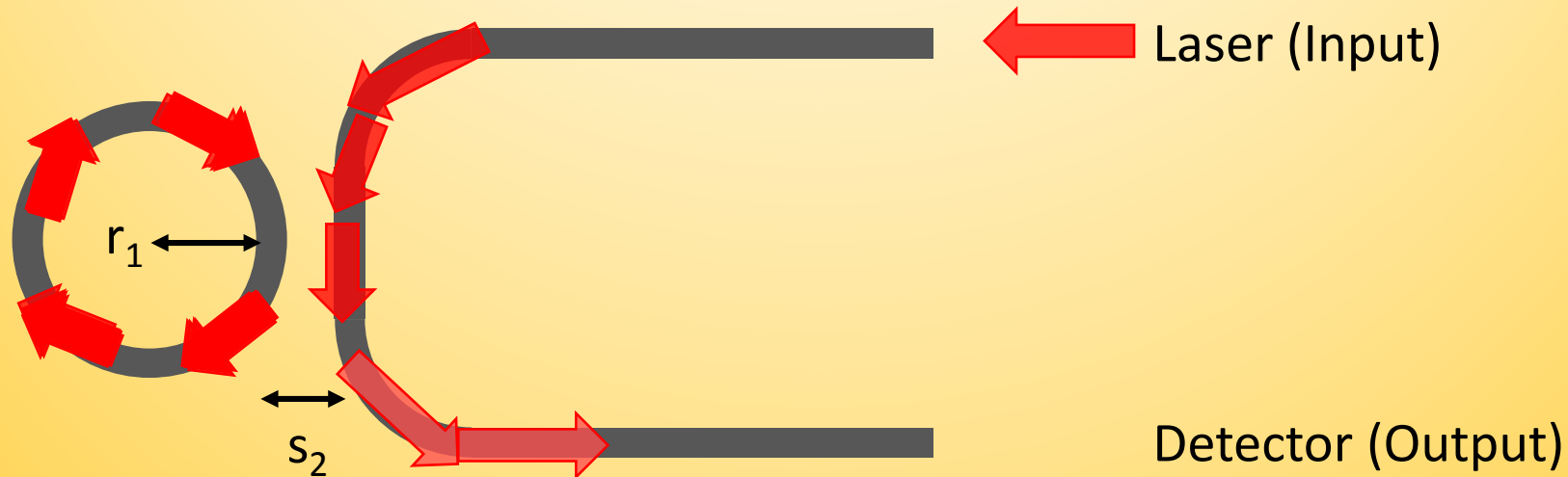


This is the same instance as when a ring resonator is added that is too far away



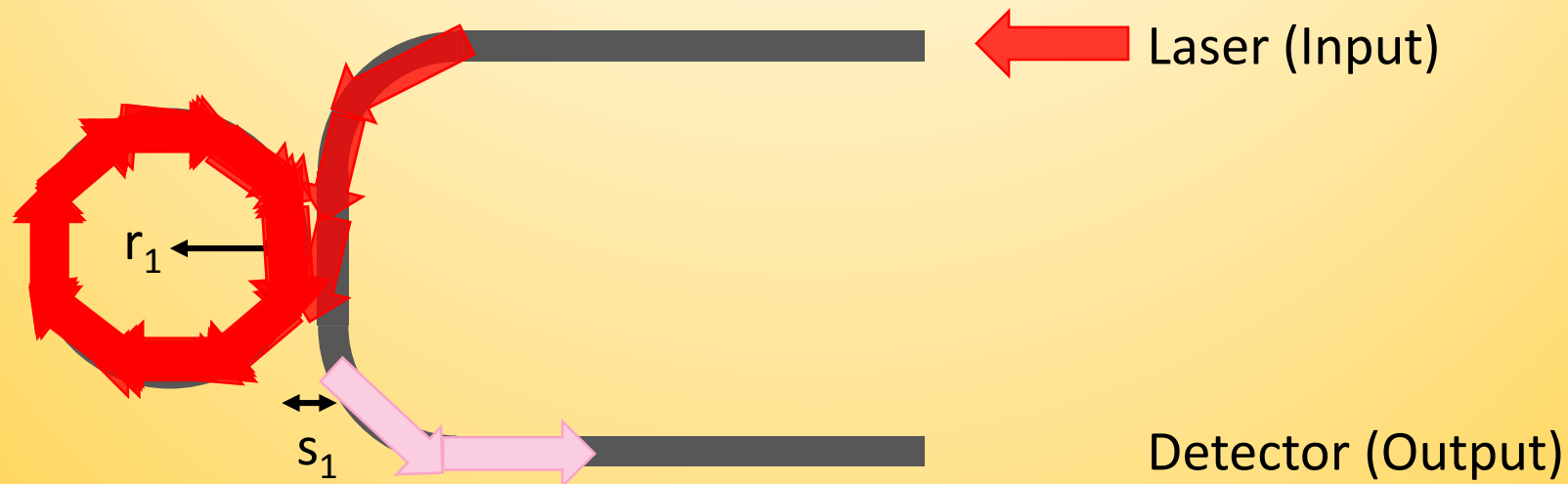
If the spacing increases past the maximum allowable spacing ( $s_3 > s_{MAX}$ ) and  $r_1$  is kept the same, there will be no coupling so transmission will be high

# What happens if the ring is moved closer?



**If the spacing decreases ( $s_2 > s_1$ ) and  $r_1$  is kept the same ,  
there will be less transmission than before because more  
light will enter the ring**

# Now bring the ring resonator even closer...



If  $s_1$  is sufficiently small and  $r_1$  is sufficiently big, low transmission will occur

# How do we make waveguides?

1. Grow oxide
2. Deposit a-Si
3. Pattern the a-Si
4. Etch waveguides out of the a-Si
5. Deposit TEOS for cladding

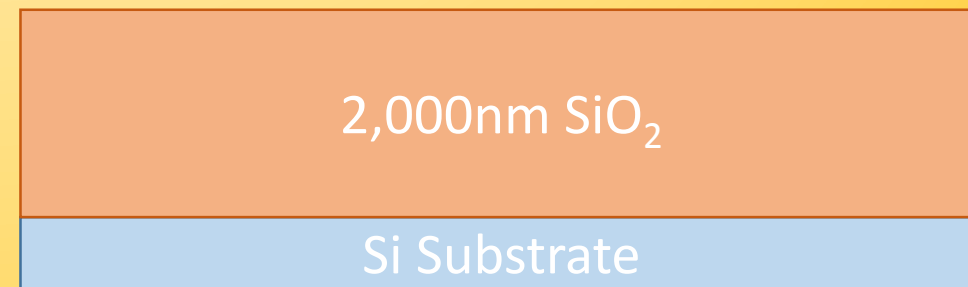
# Process Overview (1/10)

Top-Down Wafer View:



**Grow  $2\mu\text{m SiO}_2$  in the  
SMFL Bruce Furnace**

Layer Wafer View:

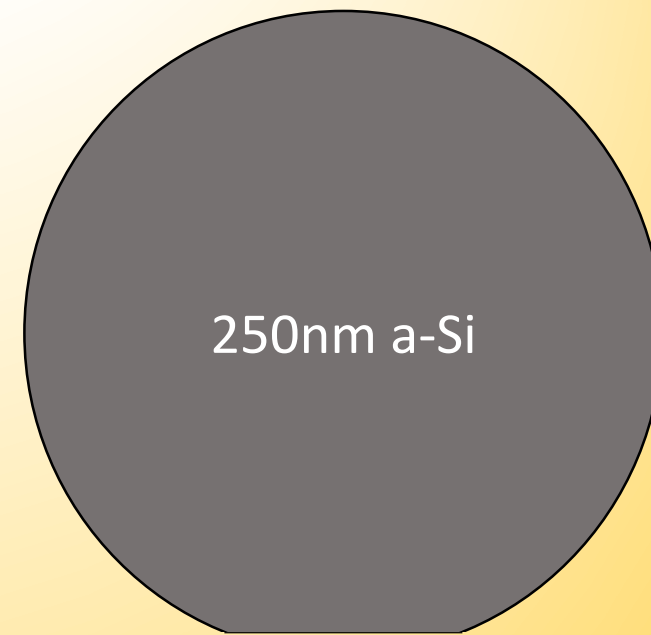


Not to scale



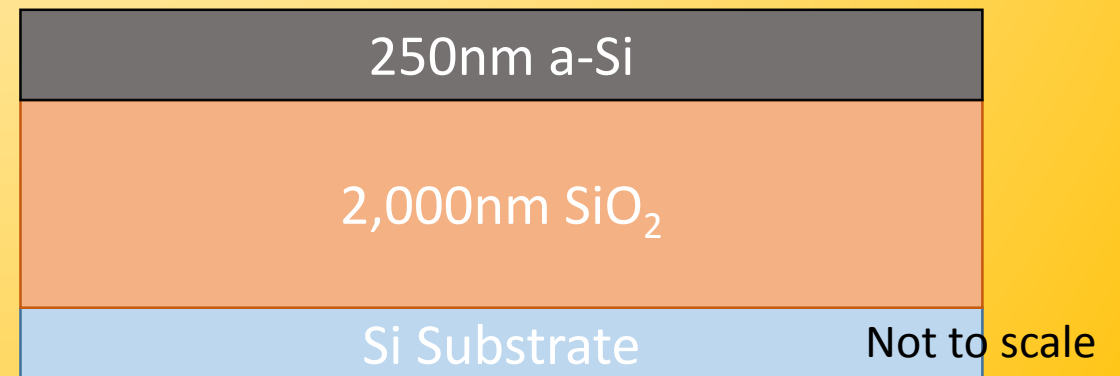
# Process Overview (2/10)

Top-Down Wafer View:



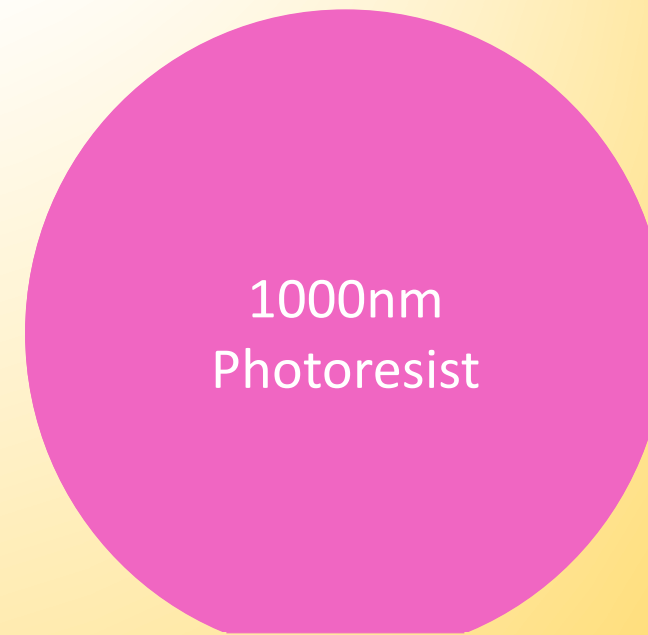
**Deposit 250nm  
amorphous silicon at  
Corning**

Layer Wafer View:



# Process Overview (3/10)

Top-Down Wafer View:



Before Develop  
After Develop

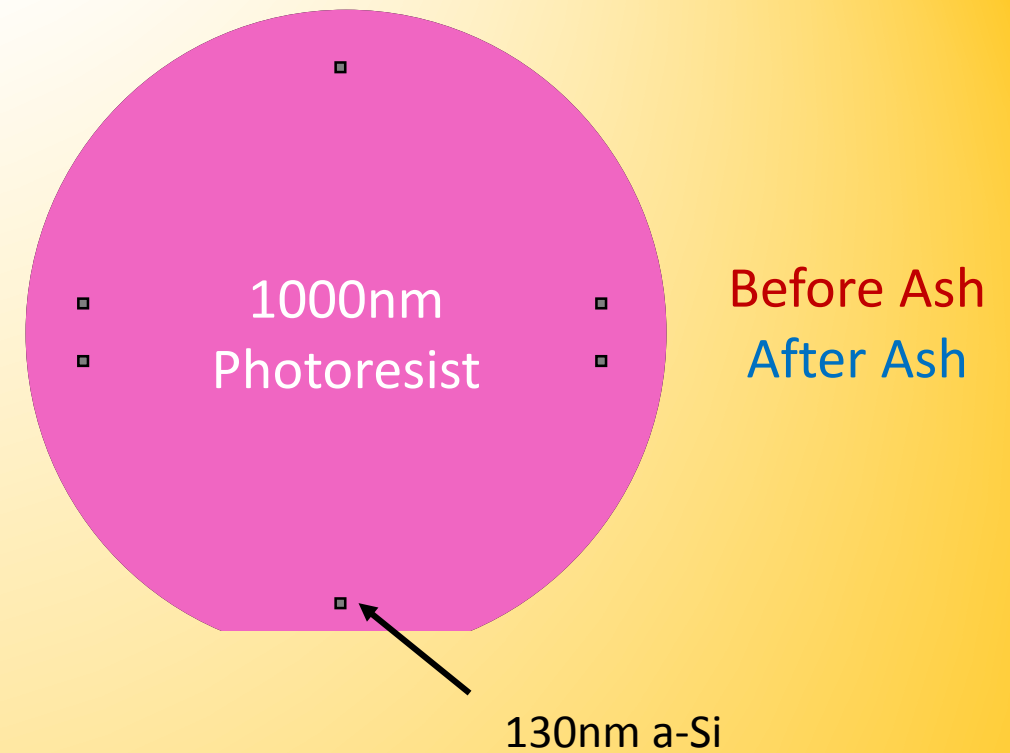
**Pattern a-Si w positive-  
tone resist (OIR-620) for  
alignment marks**

Layer Wafer View:



# Process Overview (4/10)

Top-Down Wafer View:

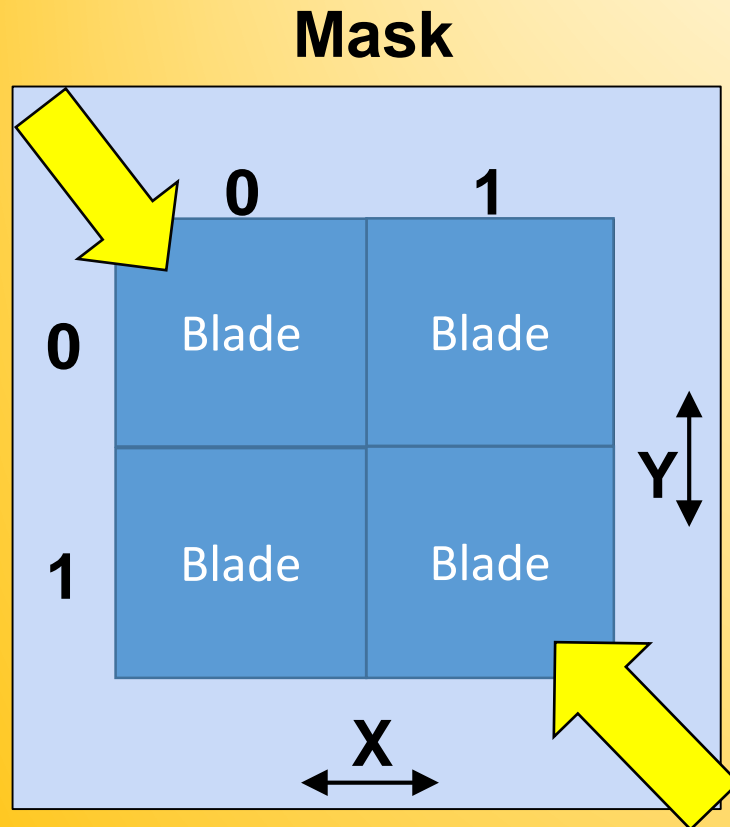


**Etch alignment marks in  
the SMFL DryTek  
Quad Etcher**

Layer Wafer View:



# Creating the ASML Stepper Job



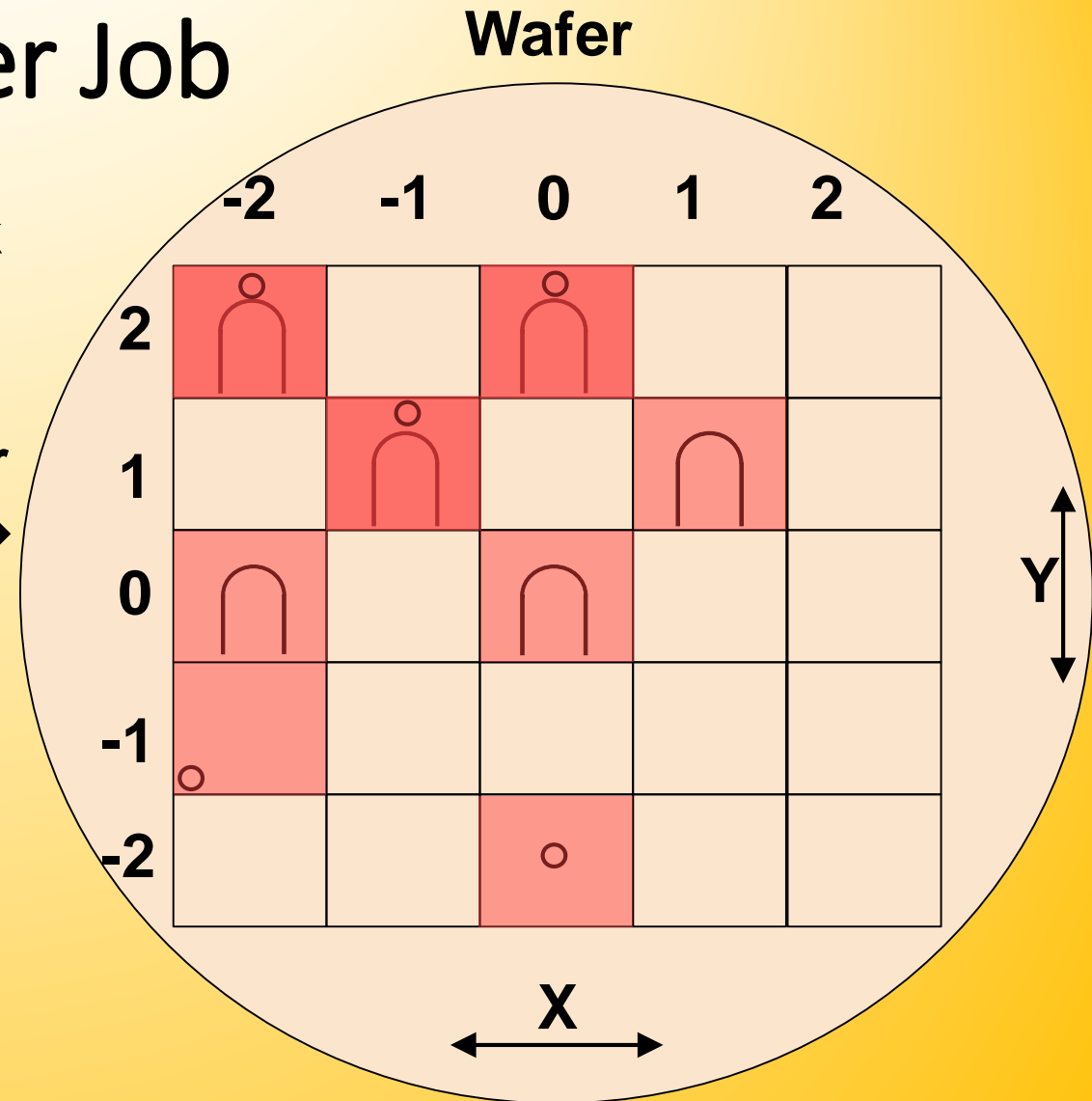
**Locations on mask**  
(x,y):

Waferguide = (0,0)

**Locations on wafer**  
**Finished pattern →**

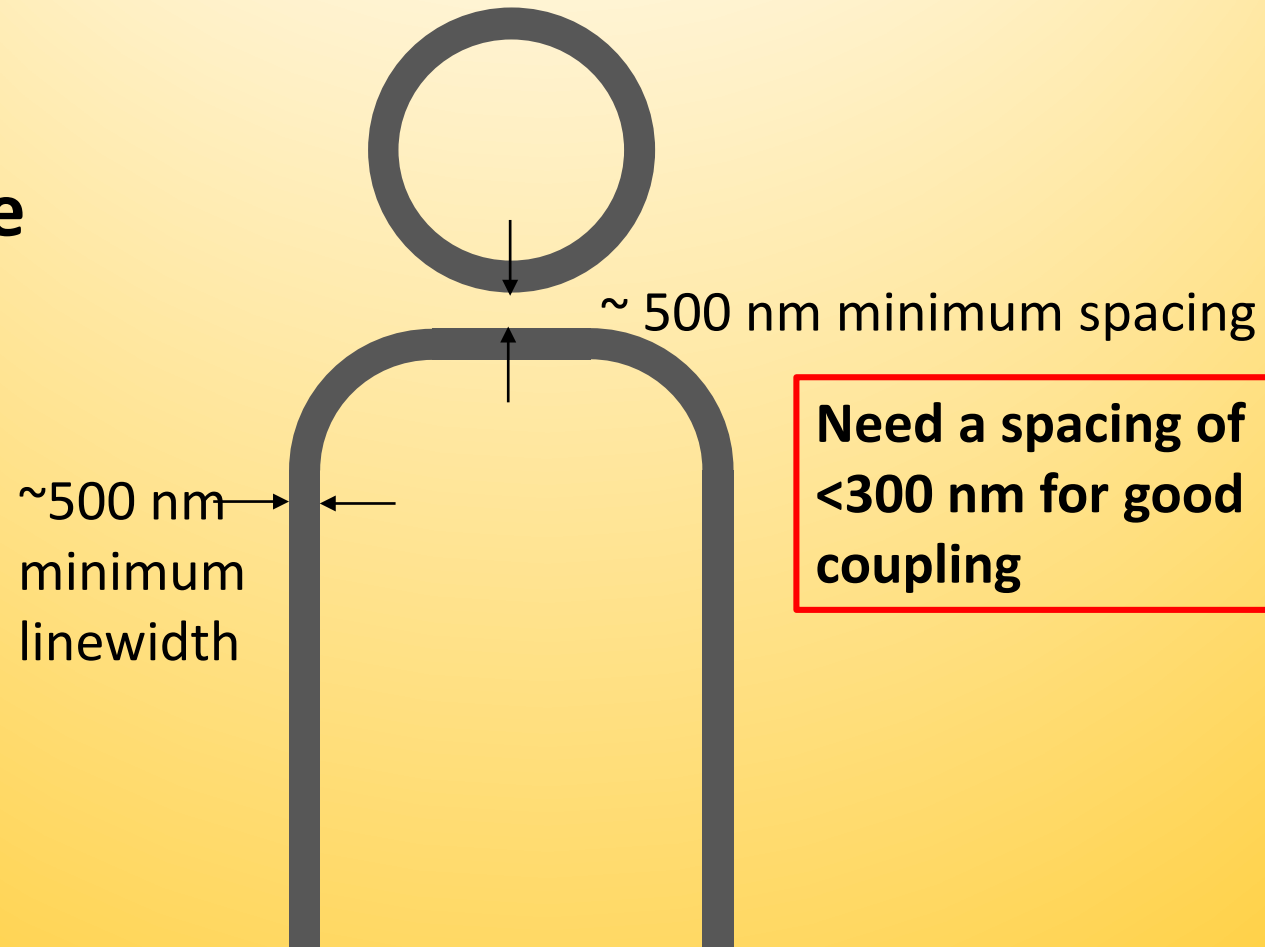
Waferguide

(-2,2)  
(0,2)  
(-2,1)  
(0,1)  
(-2,0)  
(0,0)



# The Spacing Problem

Using a single exposure on RIT's ASML i-line stepper:

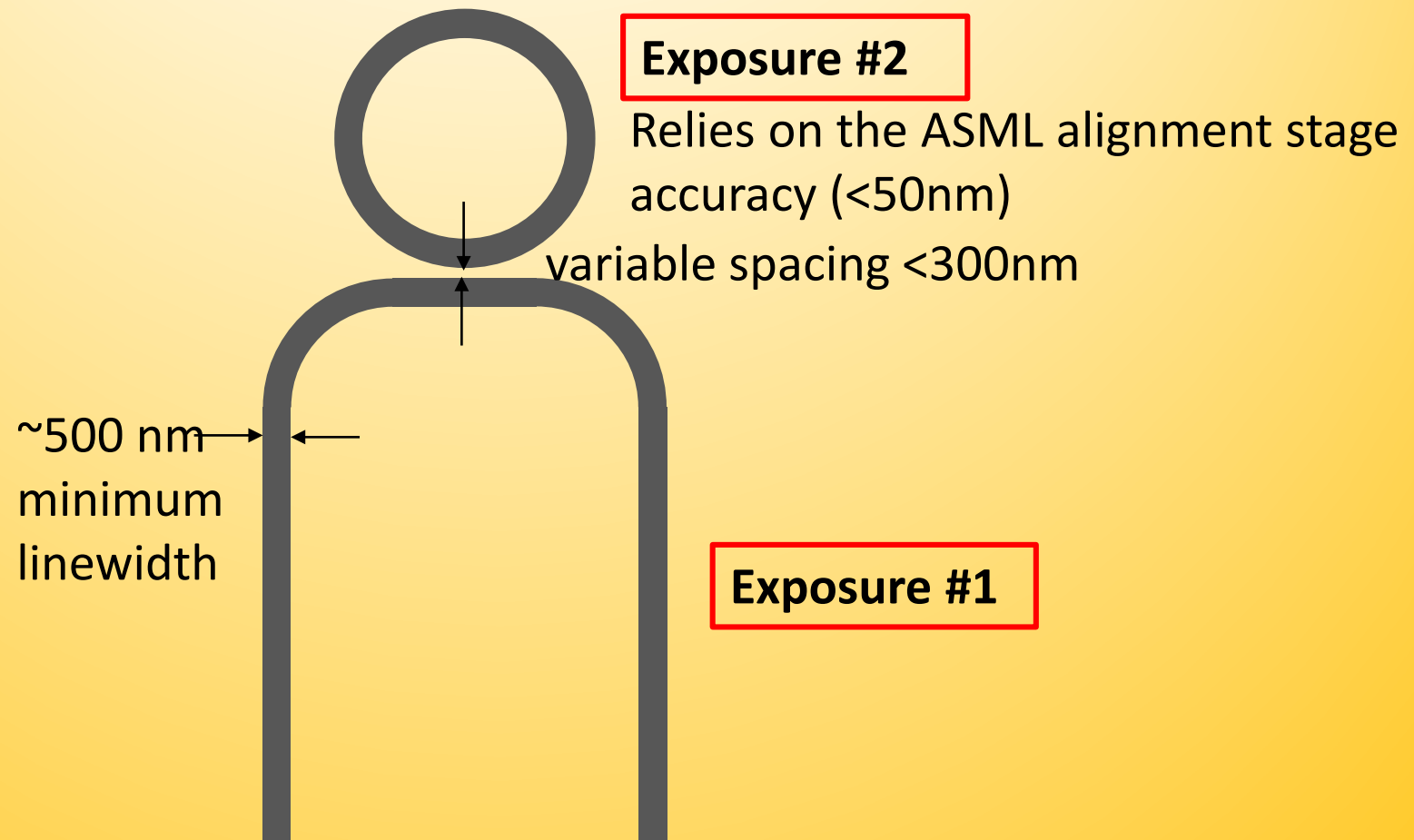


**Need a spacing of <300 nm for good coupling**



# The Solution to the Spacing Problem

Using negative resist and two exposures on RIT's ASML i-line stepper:



# Process Overview (5/10)

Top-Down Wafer View:

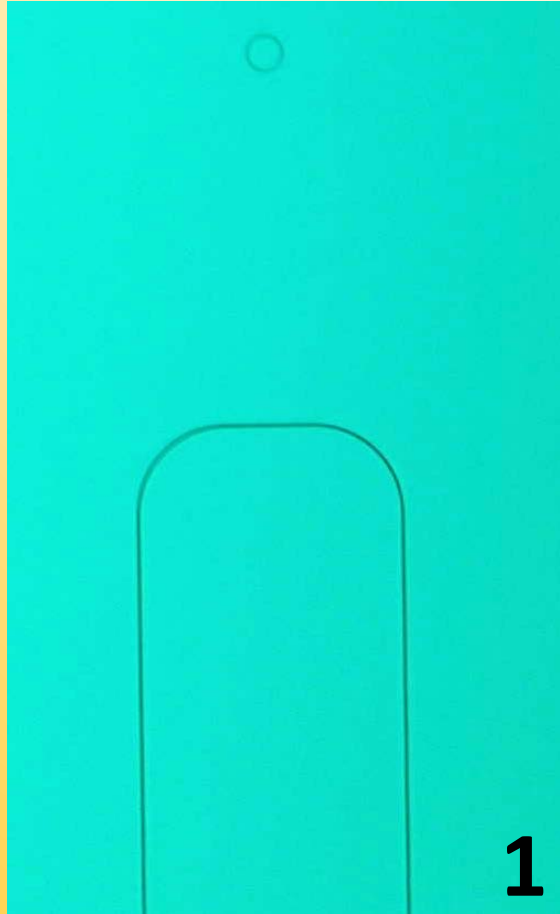


**Pattern a-Si with negative resist (nLOF 2020 dilution) for waveguide and ring pattern**

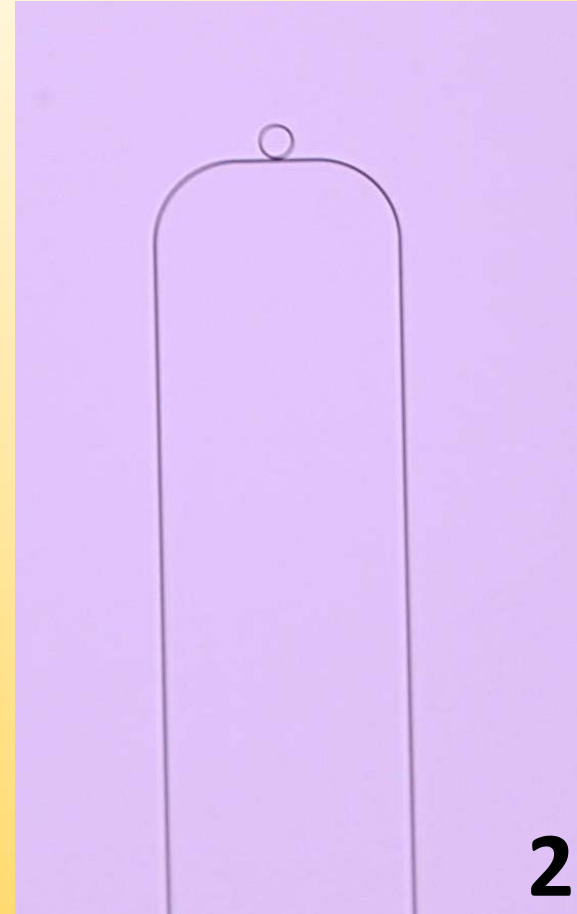
Layer Wafer View:



# Waveguide and Ring Lithography Results

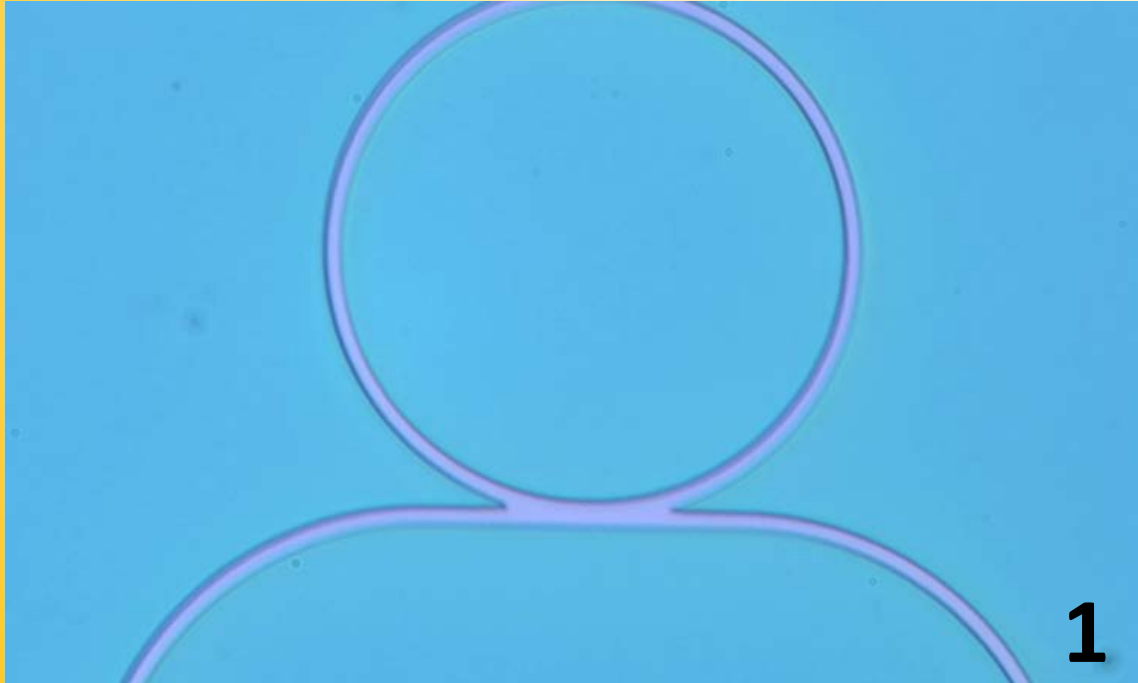


Extremely large offset

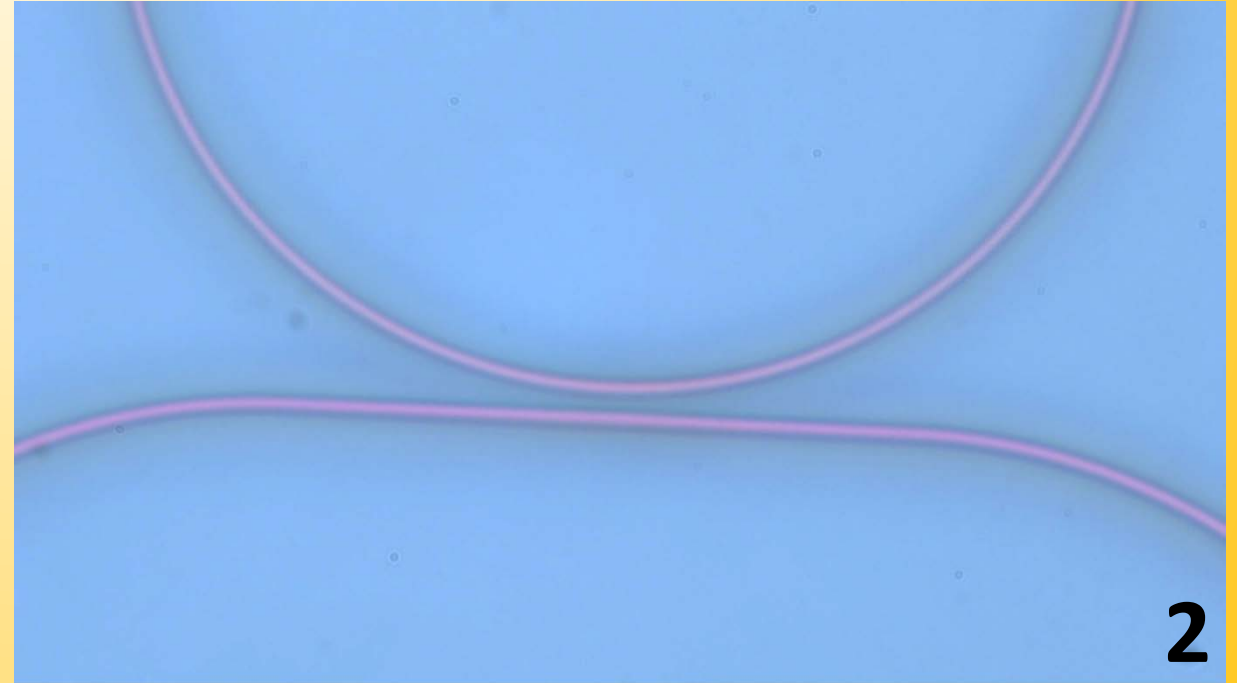


No offset

# Waveguide and Ring Lithography Results



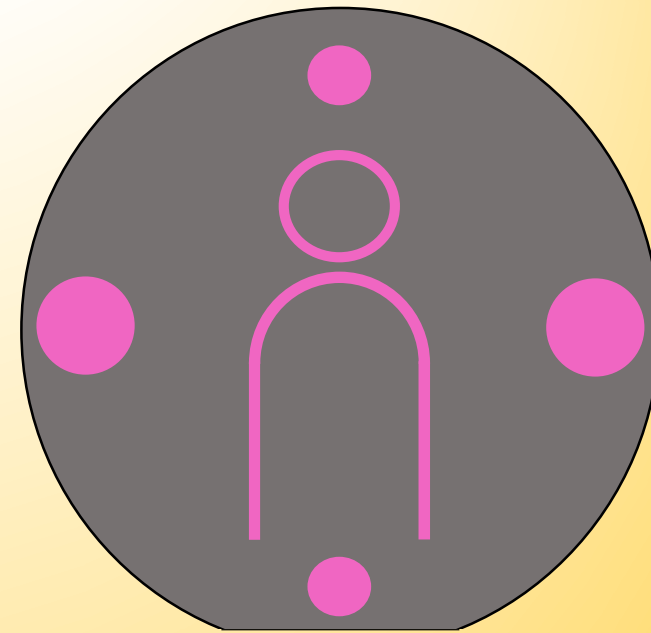
Under-developed or over-exposed → merged



Ring and waveguide offset has not merged

# Process Overview (6/10)

Top-Down Wafer View:



**Protect the alignment marks with positive-tone photoresist**

Layer Wafer View:





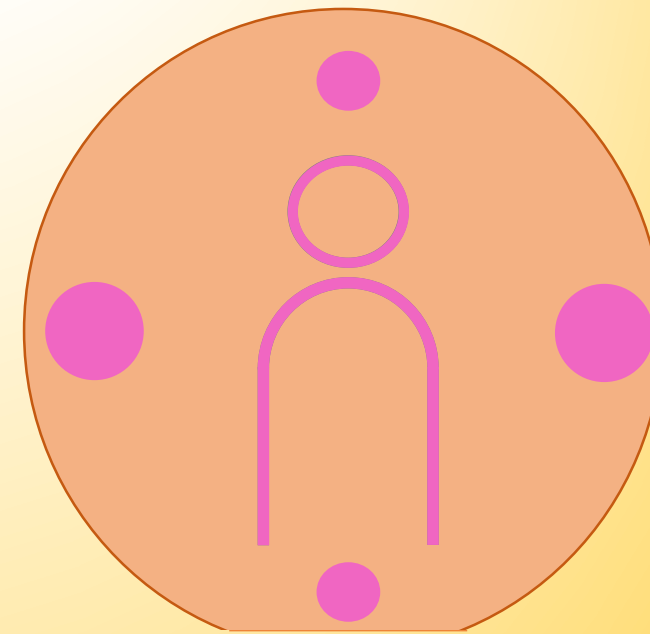
# Etching basics

- STS ASE Deep Etcher is a deep silicon etcher
- Uses the gases  $C_4F_8$ ,  $SF_6$ ,  $O_2$  and Ar
- Single silicon etch cycle
- Developed by Ankur Lamoria and Patricia Meller



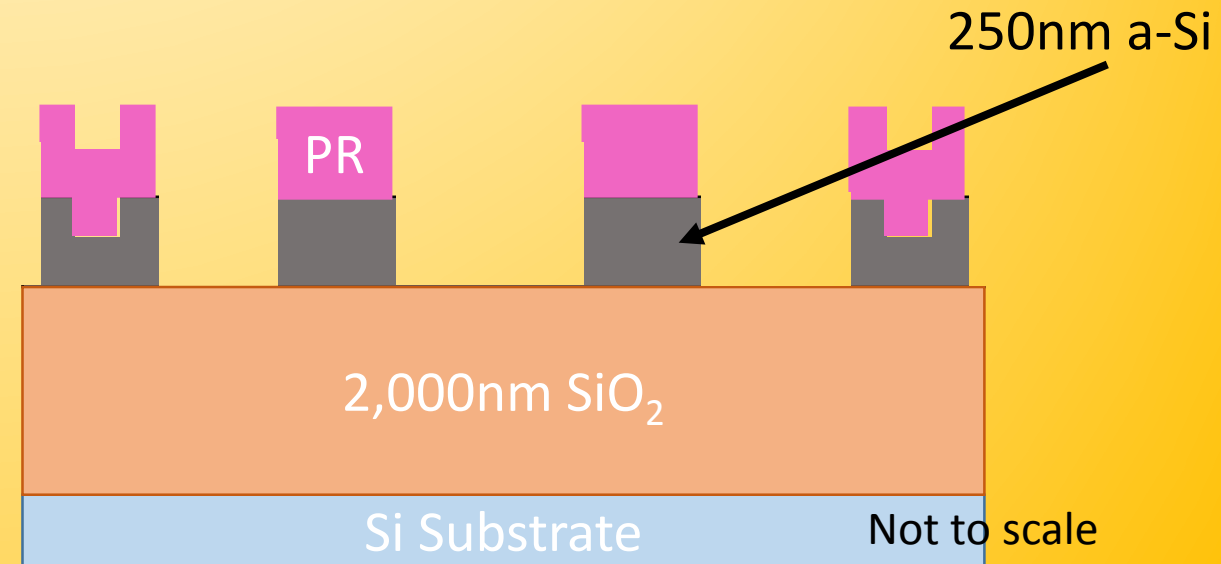
# Process Overview (7/10)

Top-Down Wafer View:

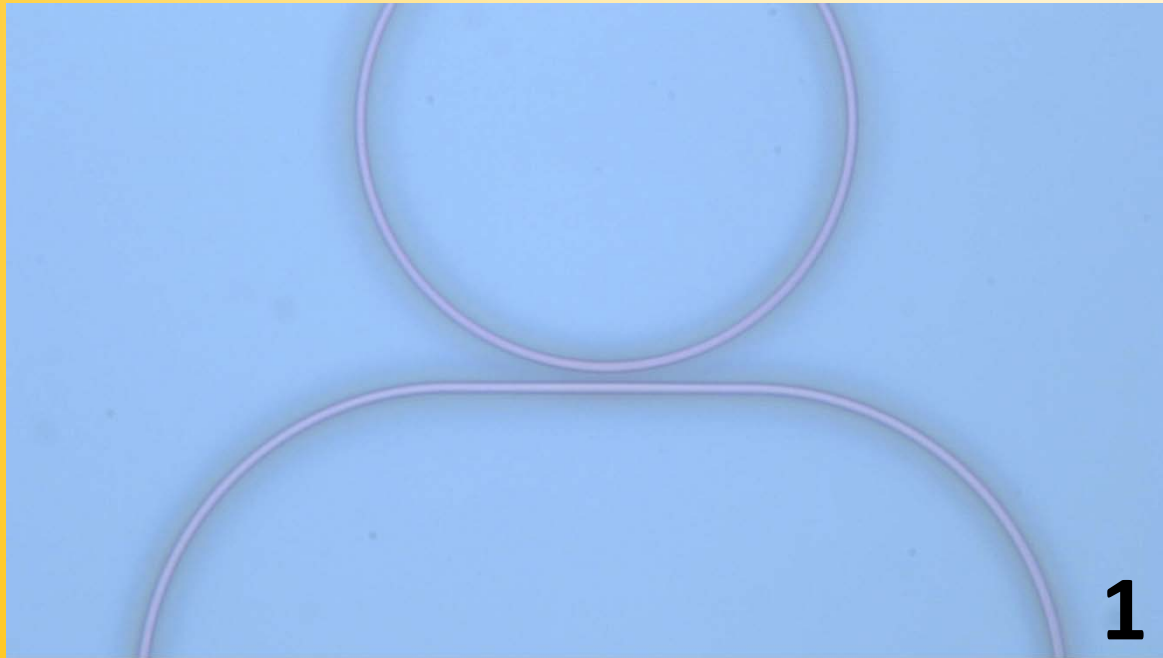


**Etch a-Si in the SMFL  
STS Deep Etcher**

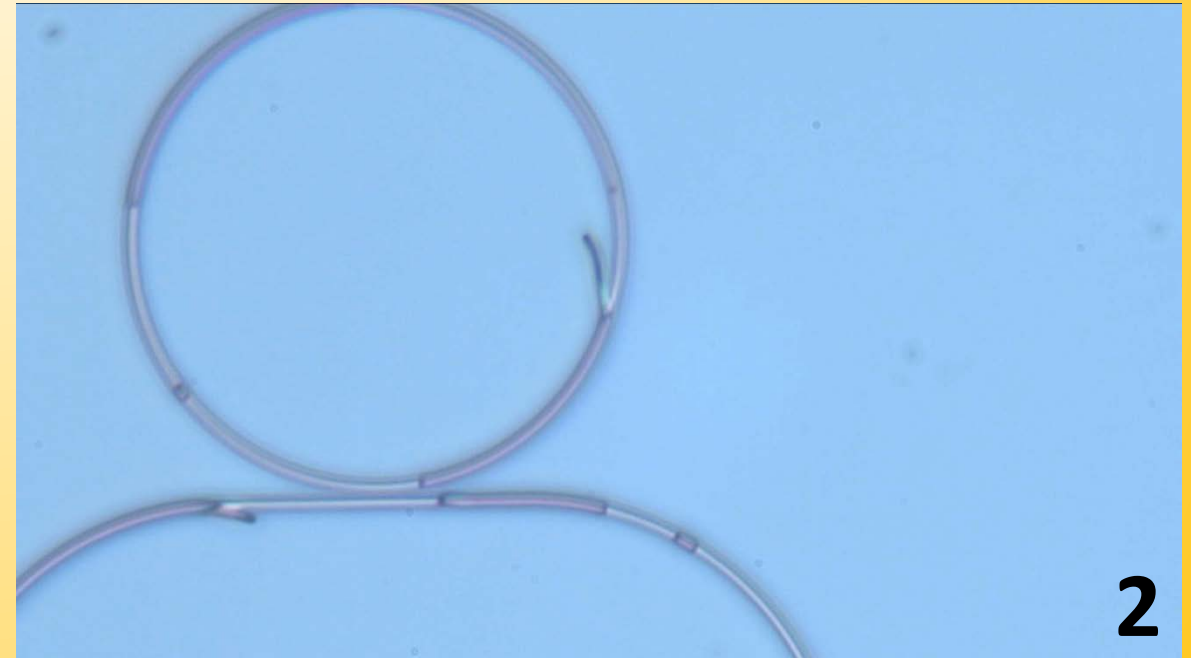
Layer Wafer View:



# Waveguide and Ring Etch Results

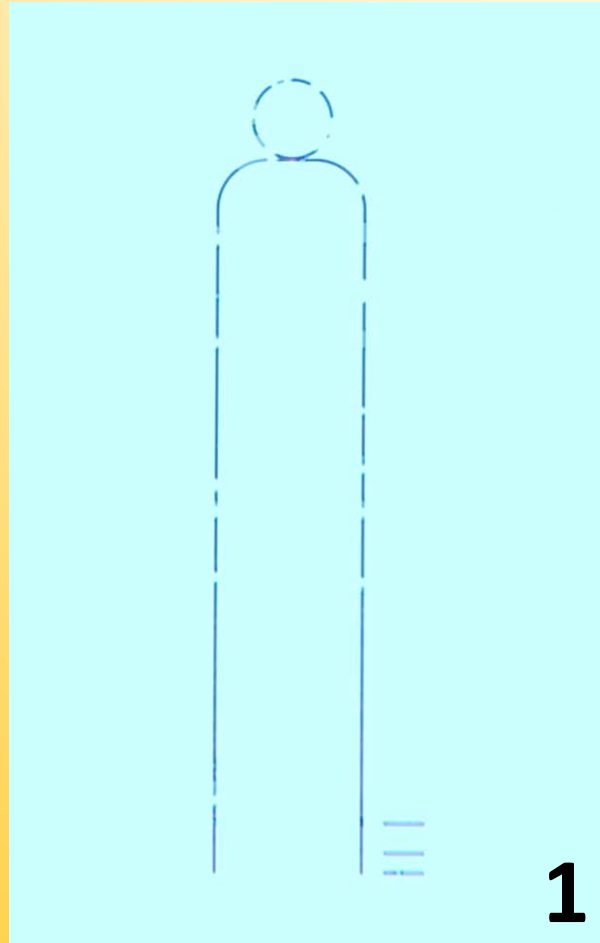


Pre-ash

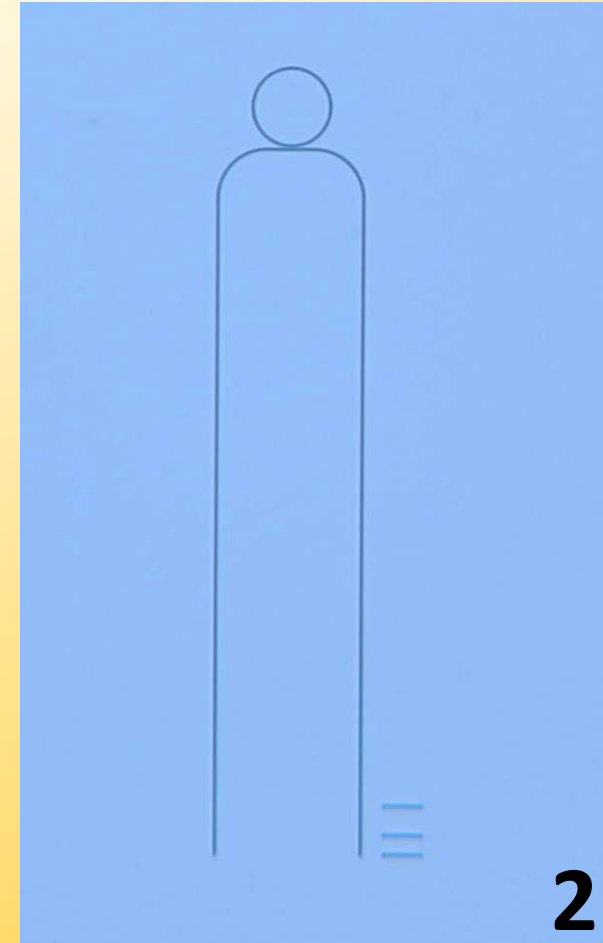


Post-ash; some photoresist still present

# Waveguide and Ring Etch Results

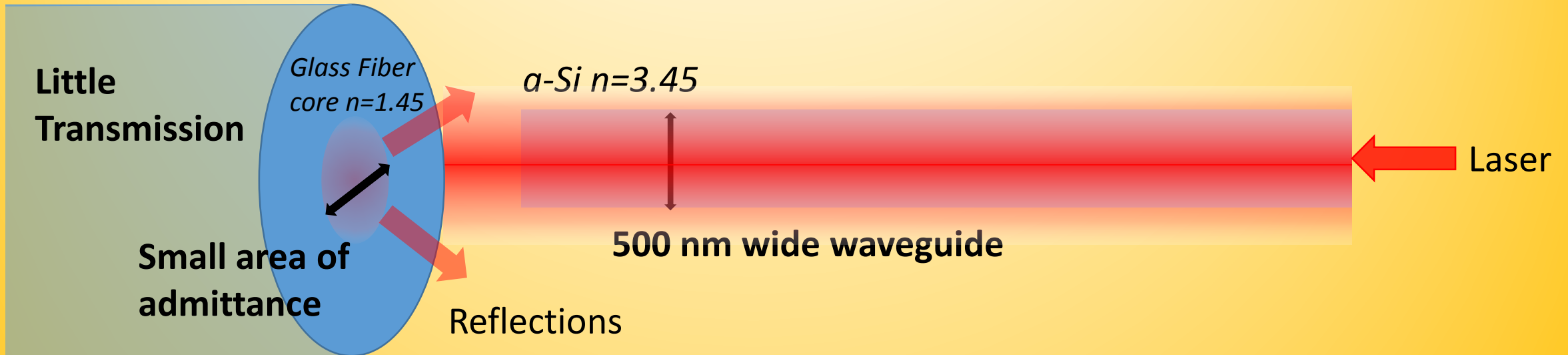


Over-etched



Modified etch

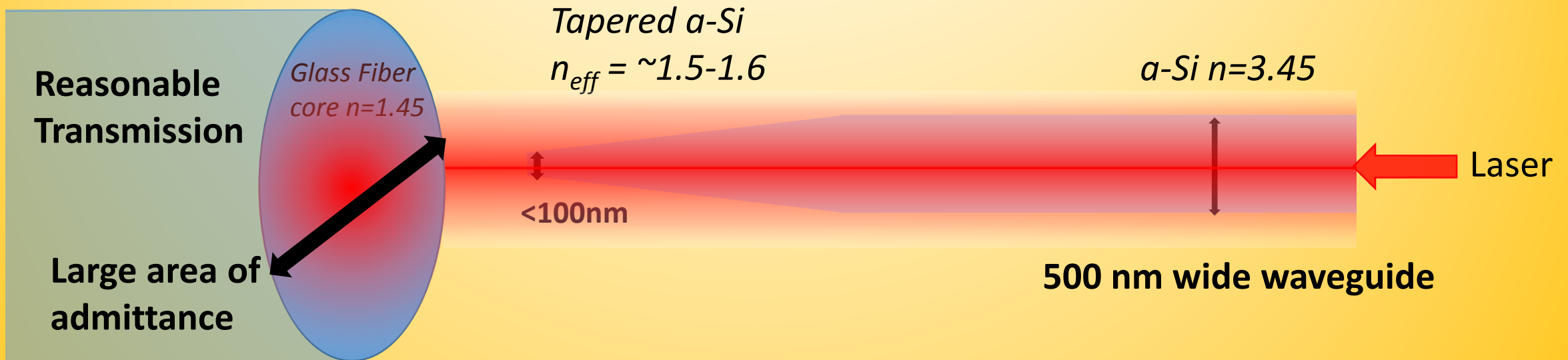
# Waveguide Tapered to Enhance Light Coupling



Reference: Dr. Pearson

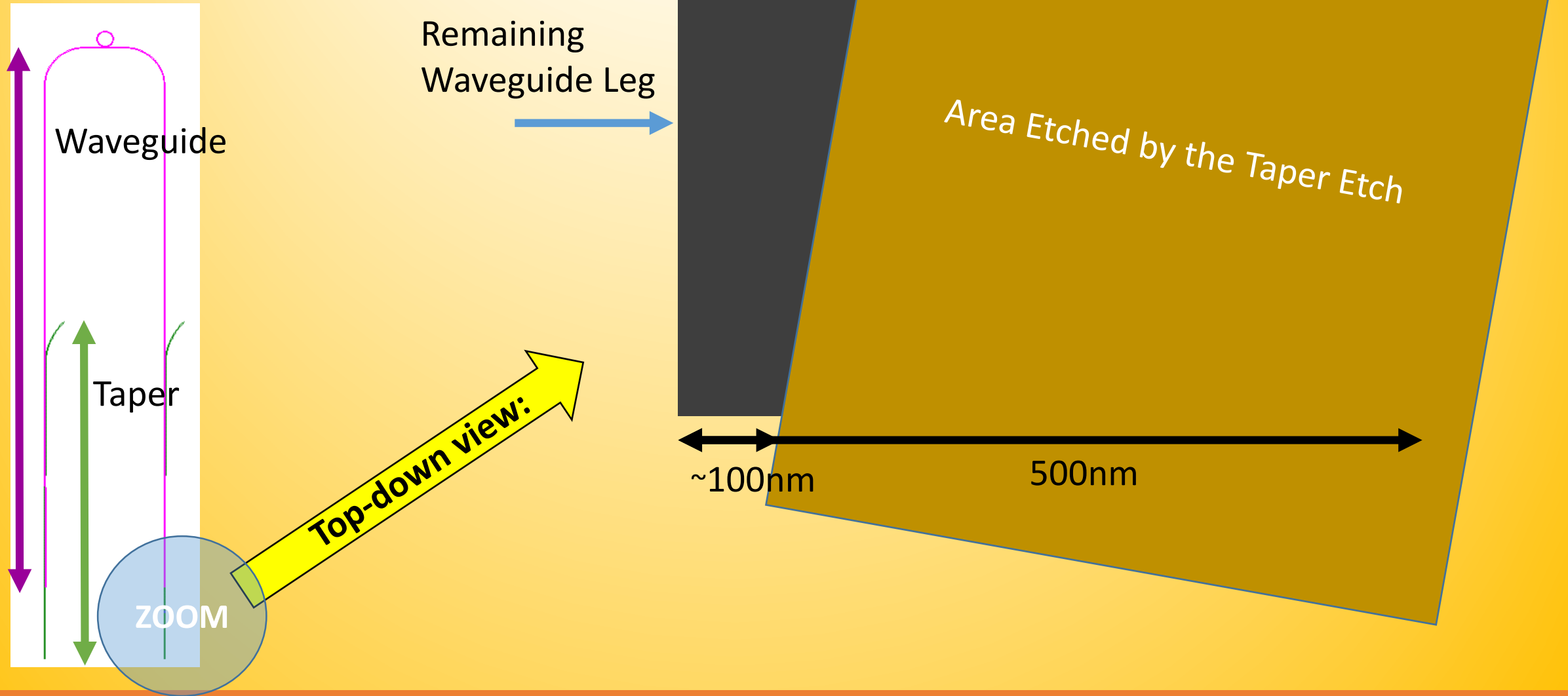


# Waveguide Tapered to Enhance Light Coupling

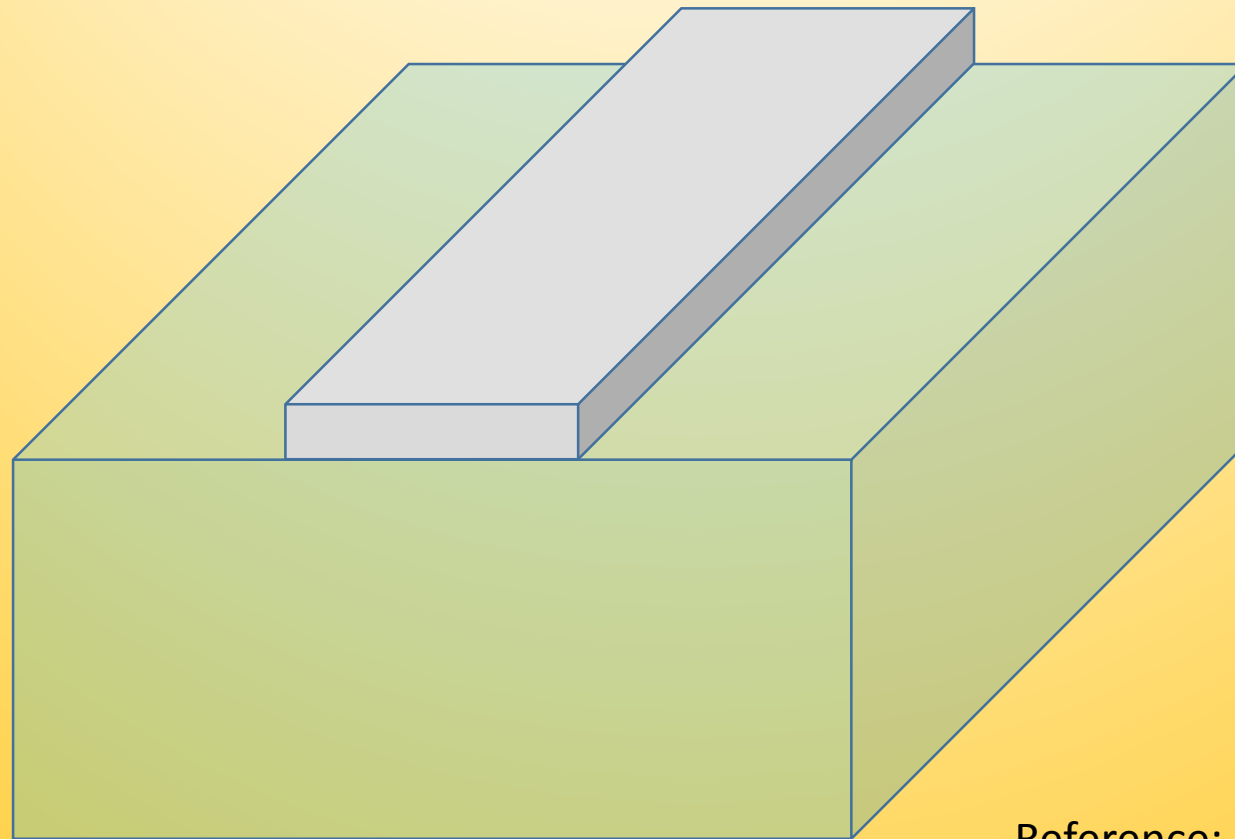


Reference: Dr. Pearson

# Taper layout

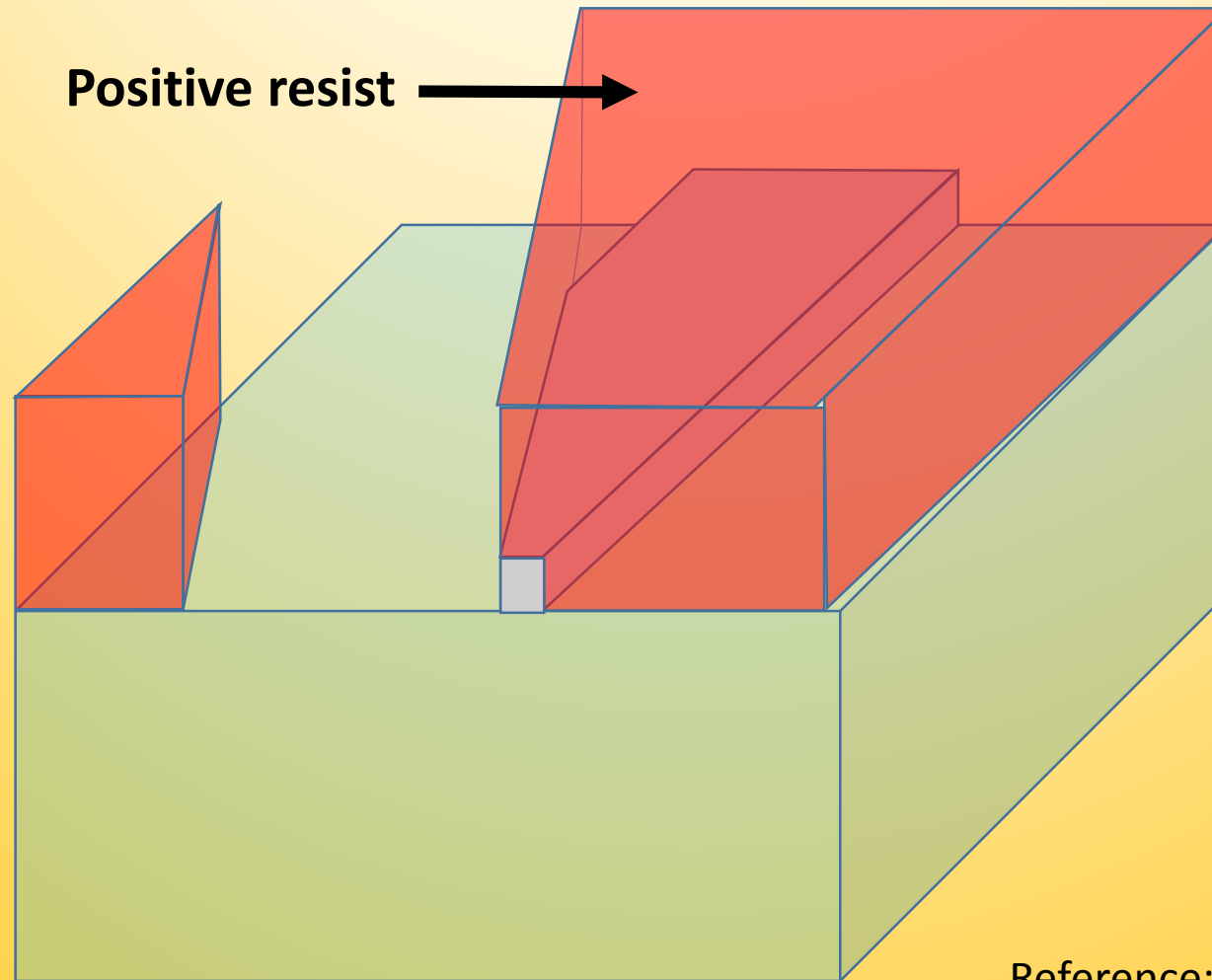


# Formation of a Tapered Waveguide



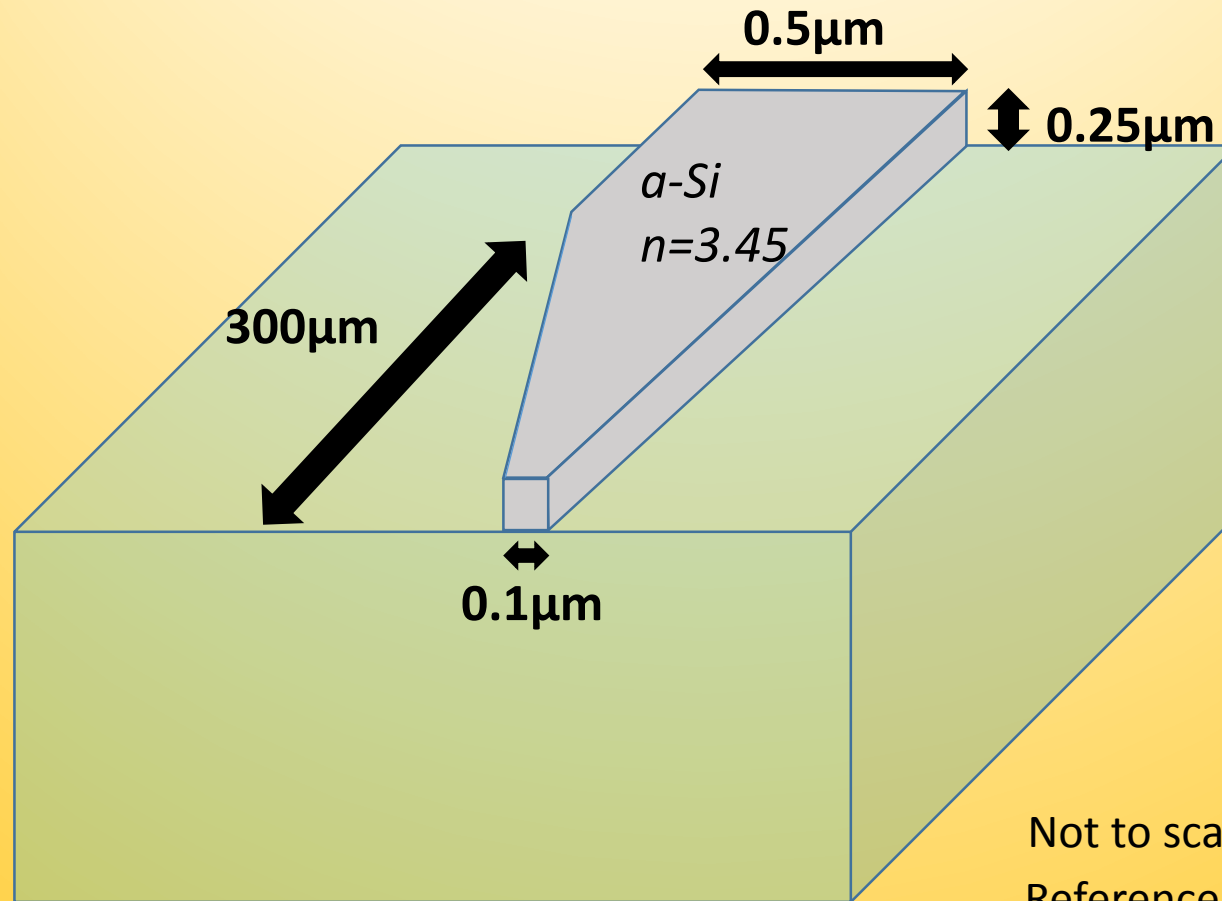
Reference: Dr. Pearson

# Formation of a Tapered Waveguide



Reference: Dr. Pearson

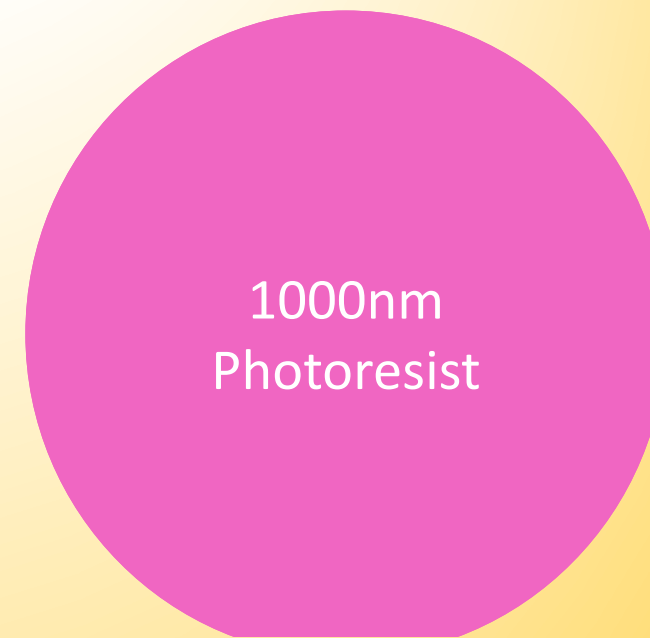
# Formation of a Tapered Waveguide



Not to scale in X and Y  
Reference: Dr. Pearson

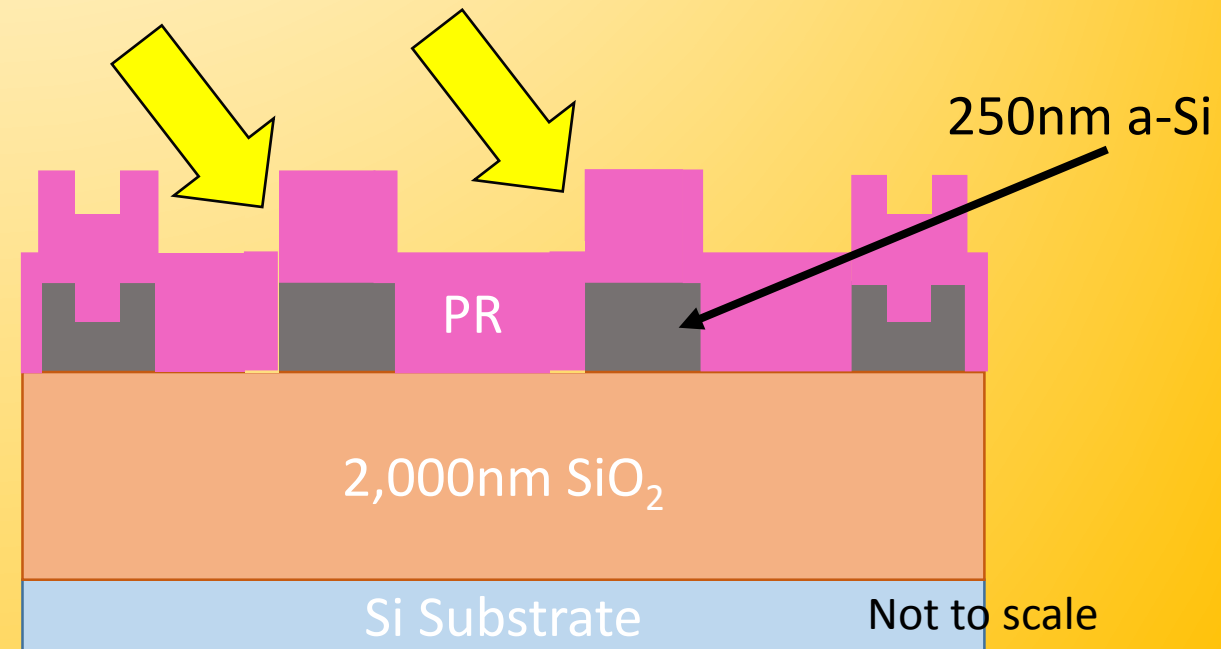
# Process Overview (8/10)

Top-Down Wafer View:



Pattern a-Si w positive-tone resist (OIR-620) for waveguide taper etch

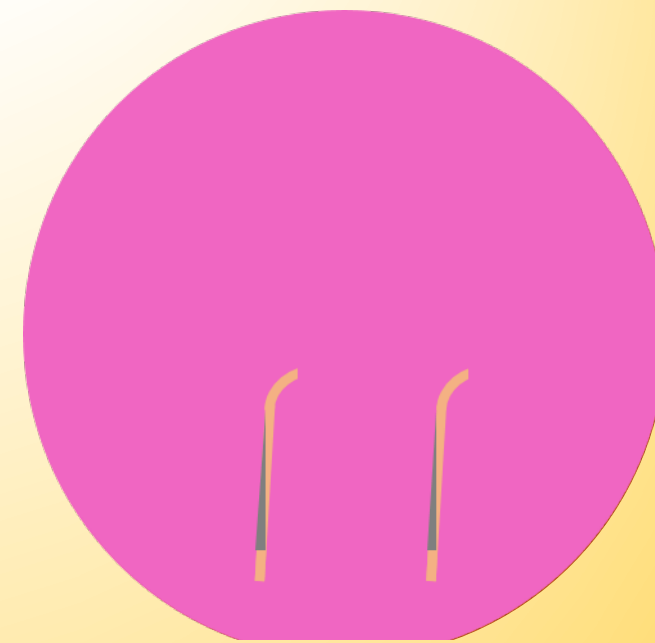
Layer Wafer View:





# Process Overview (9/10)

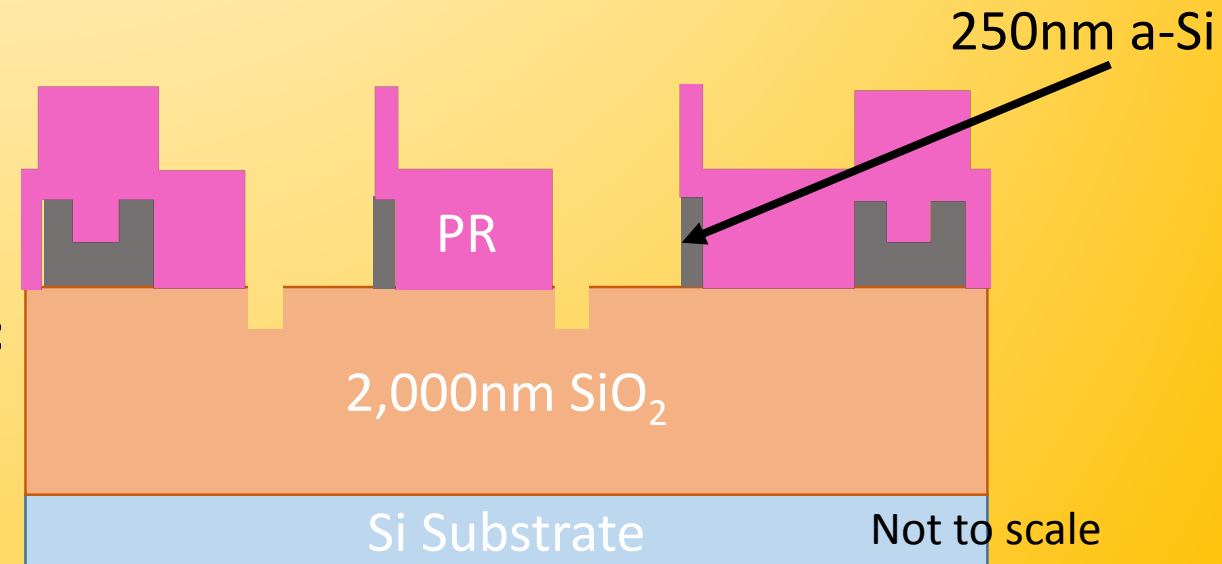
Top-Down Wafer View:



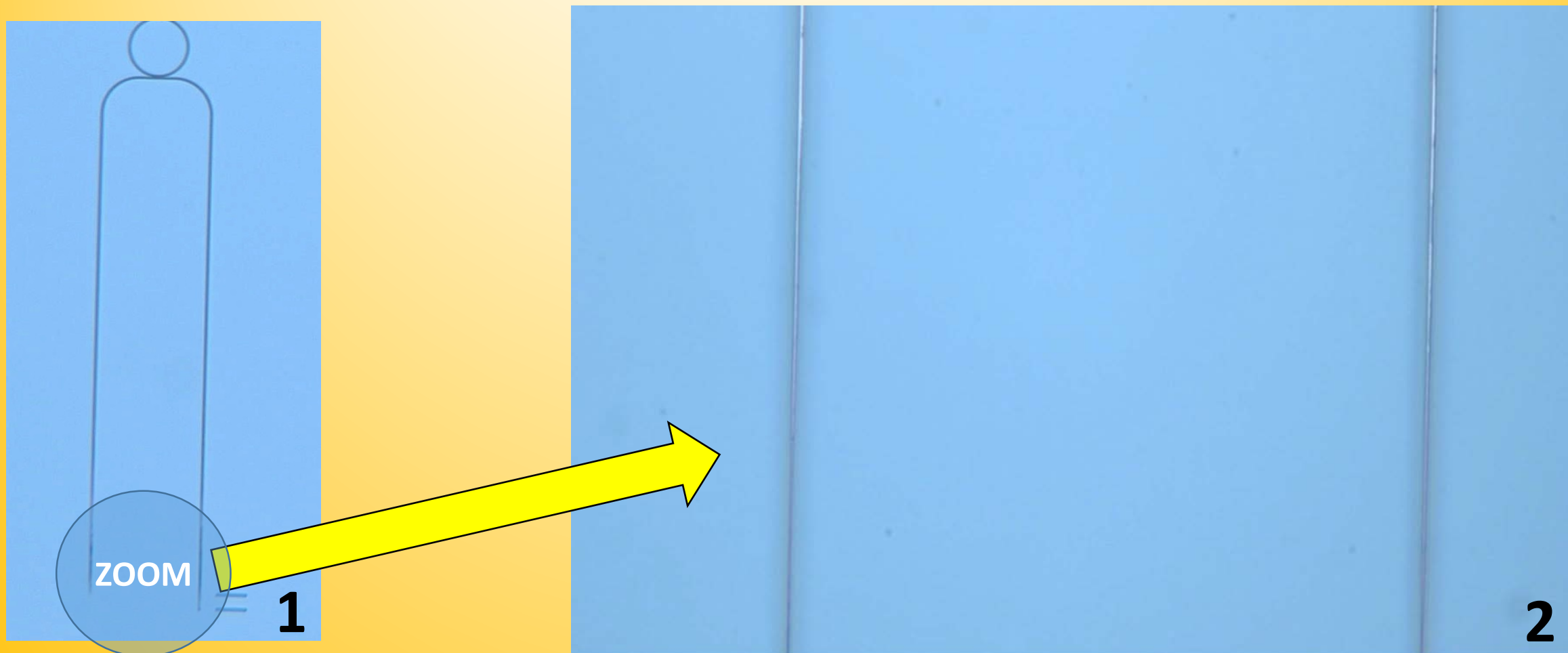
Before Ash  
After Ash

**Etch a-Si in the SMFL  
STS Deep Etcher**

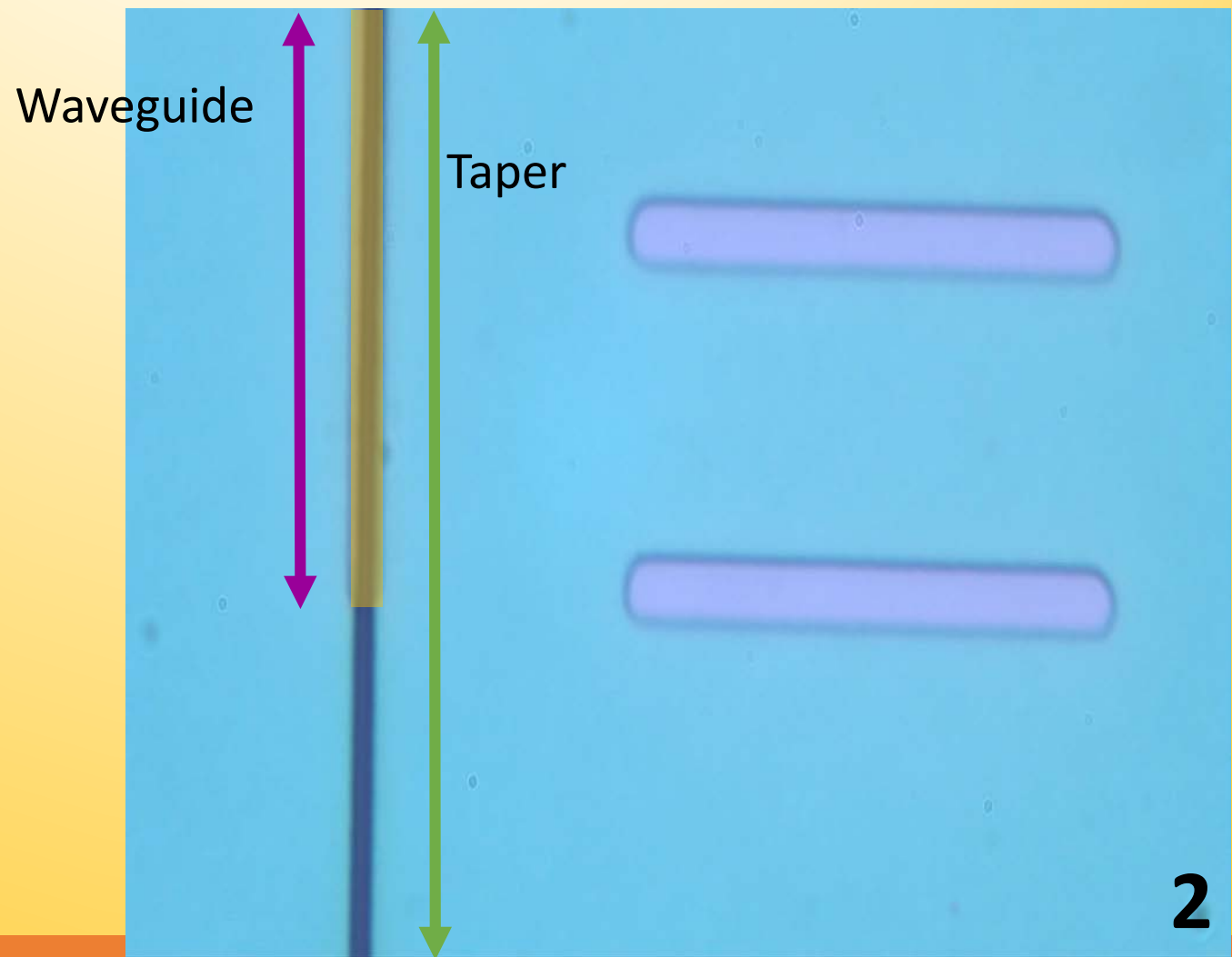
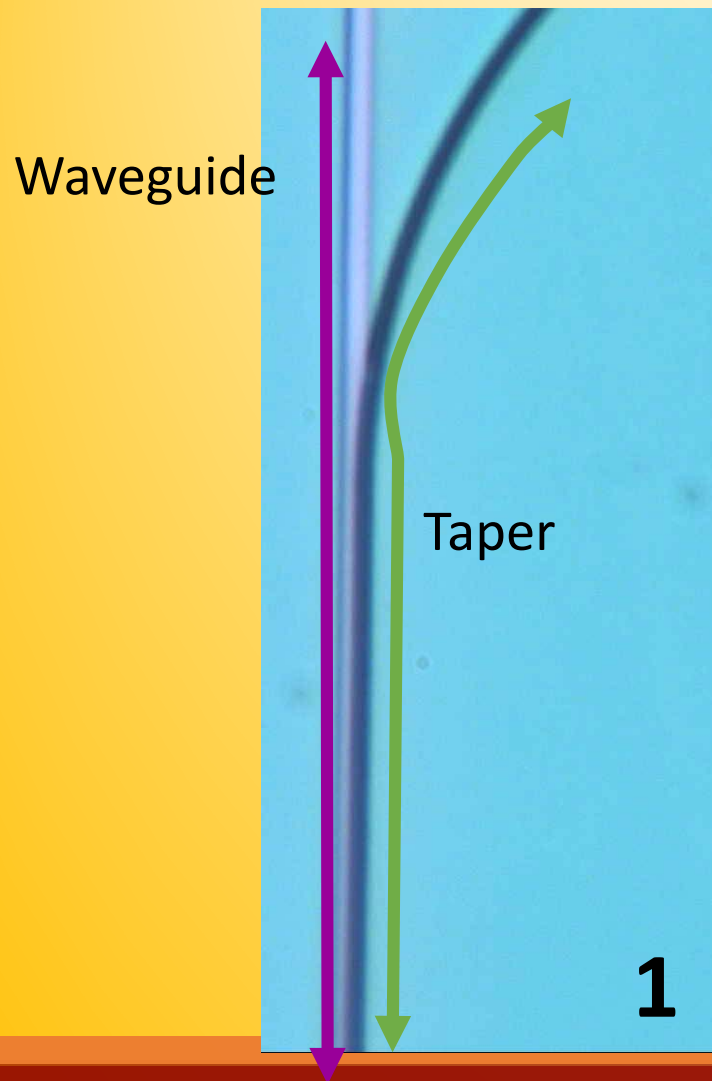
Layer Wafer View:



# Taper Etch Results



# Taper Etch Results



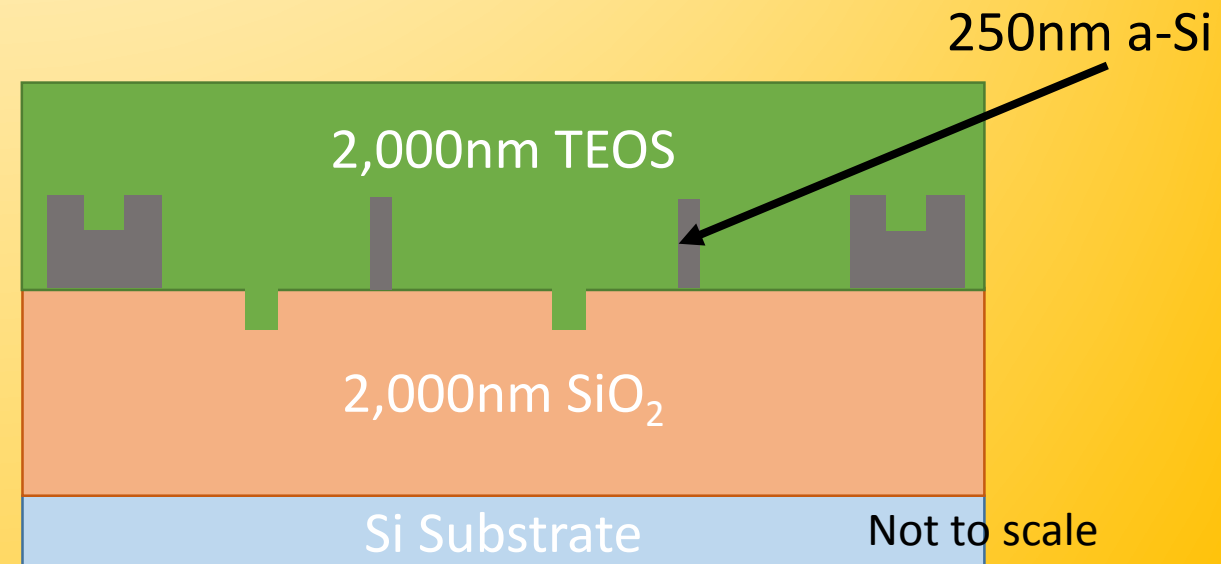
# Process Overview (10/10)

Top-Down Wafer View:

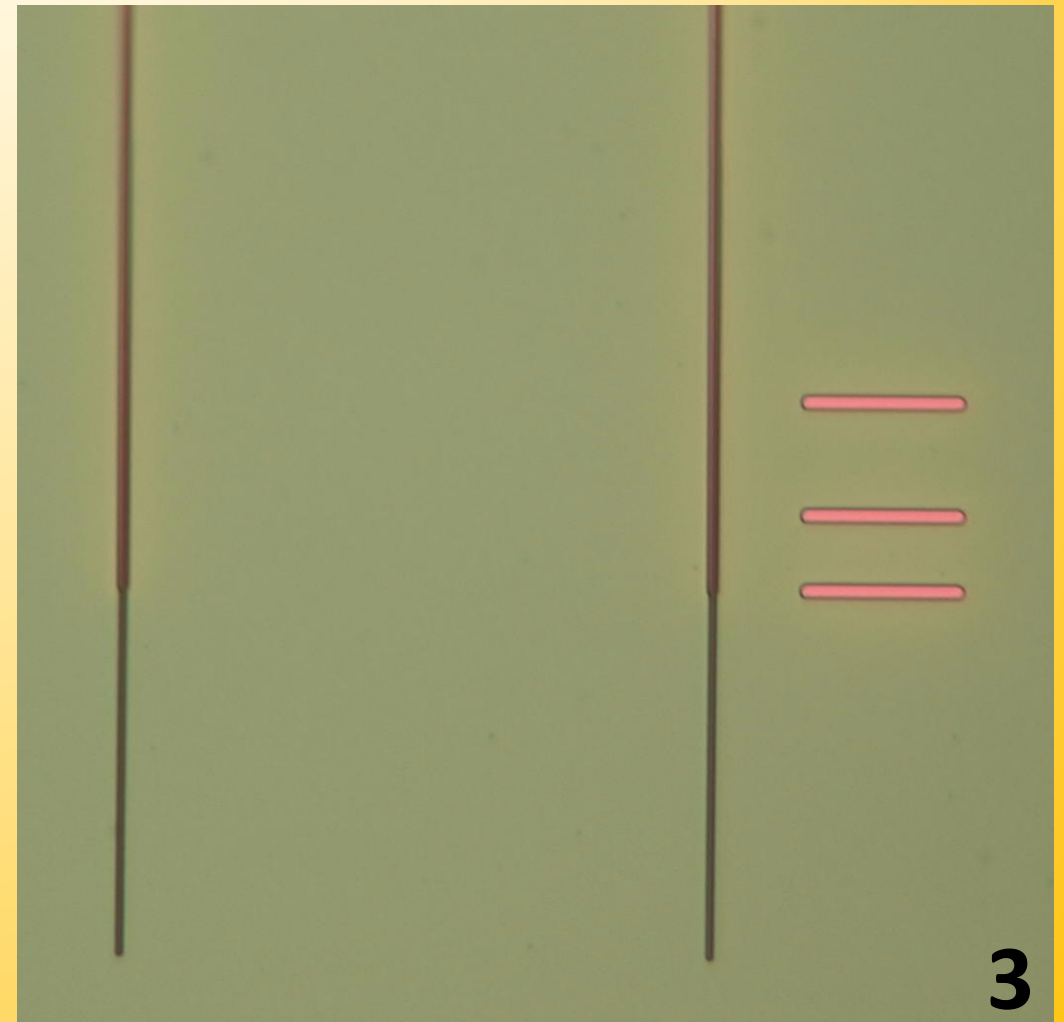
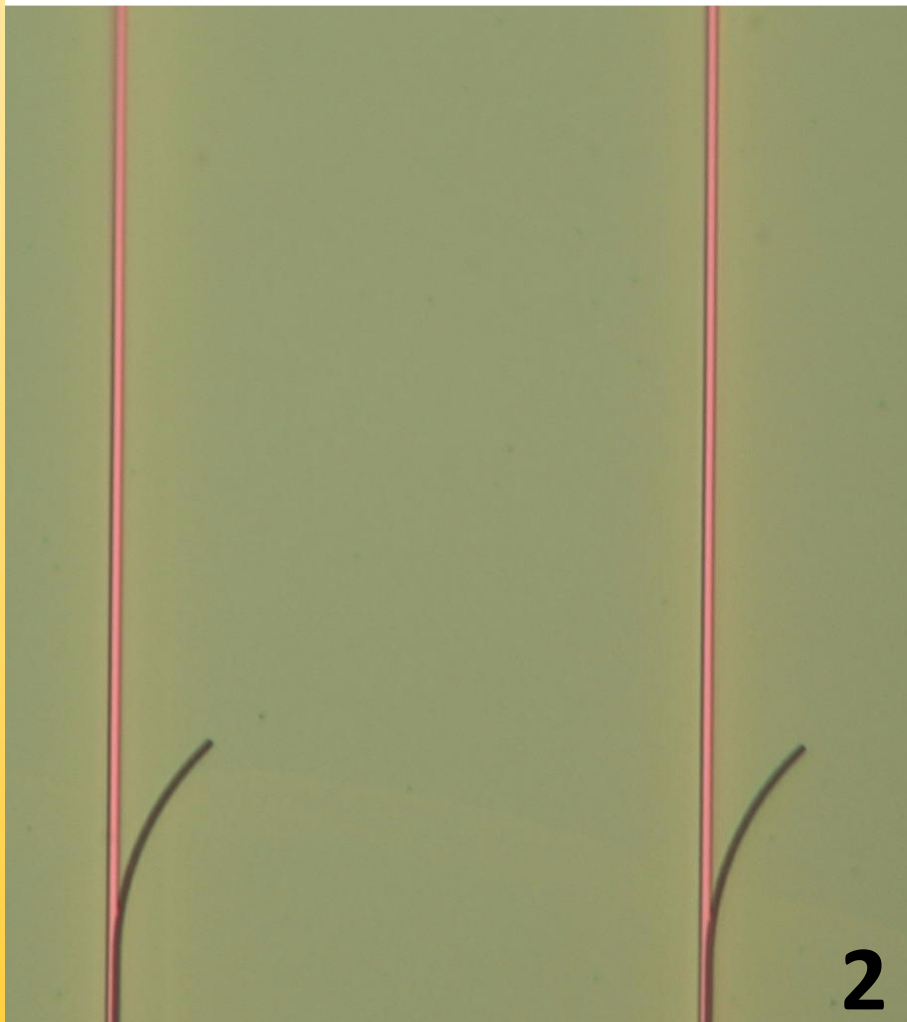
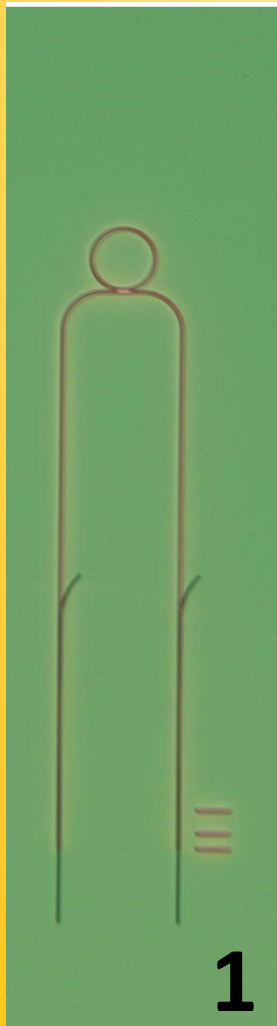


**Deposit 2 $\mu$ m TEOS in  
the SMFL P5000 for  
cladding**

Layer Wafer View:

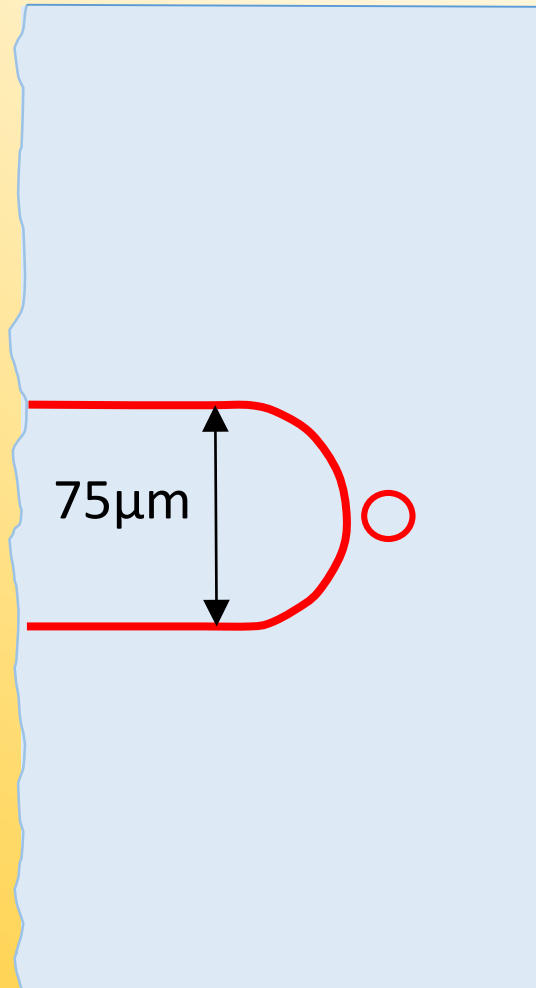


# After TEOS Deposition

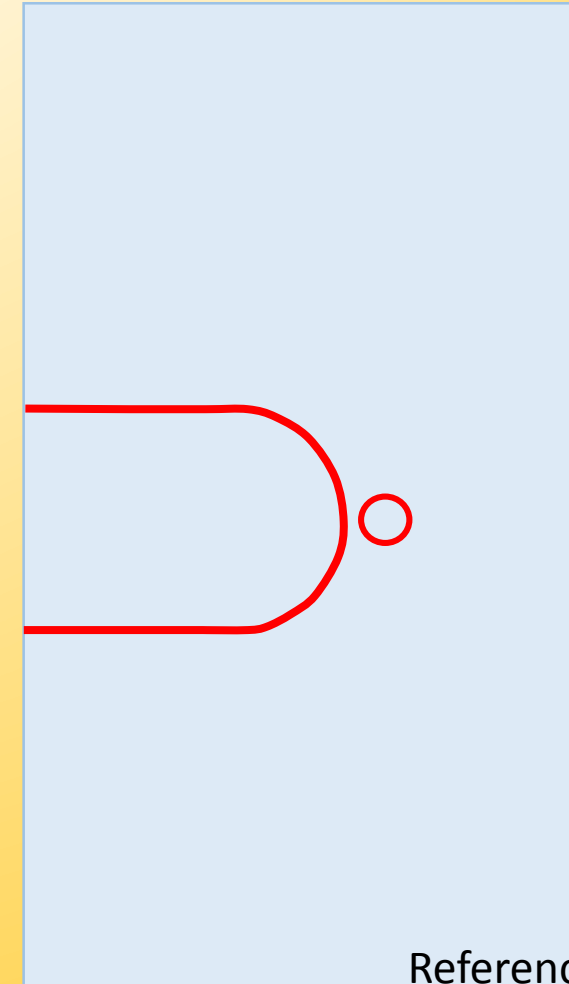


# Sawing and Polishing

Rough edge  
from diamond  
saw



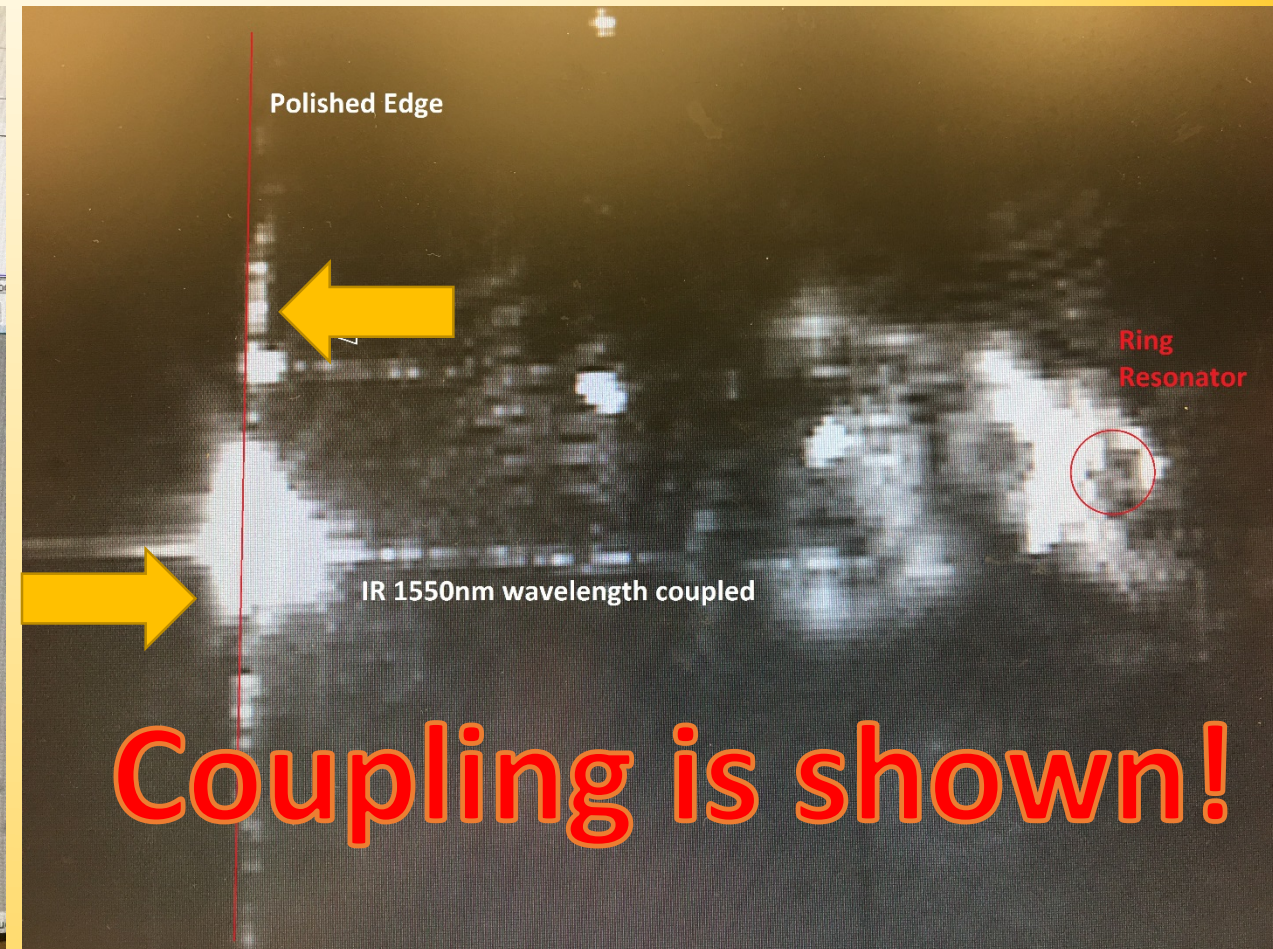
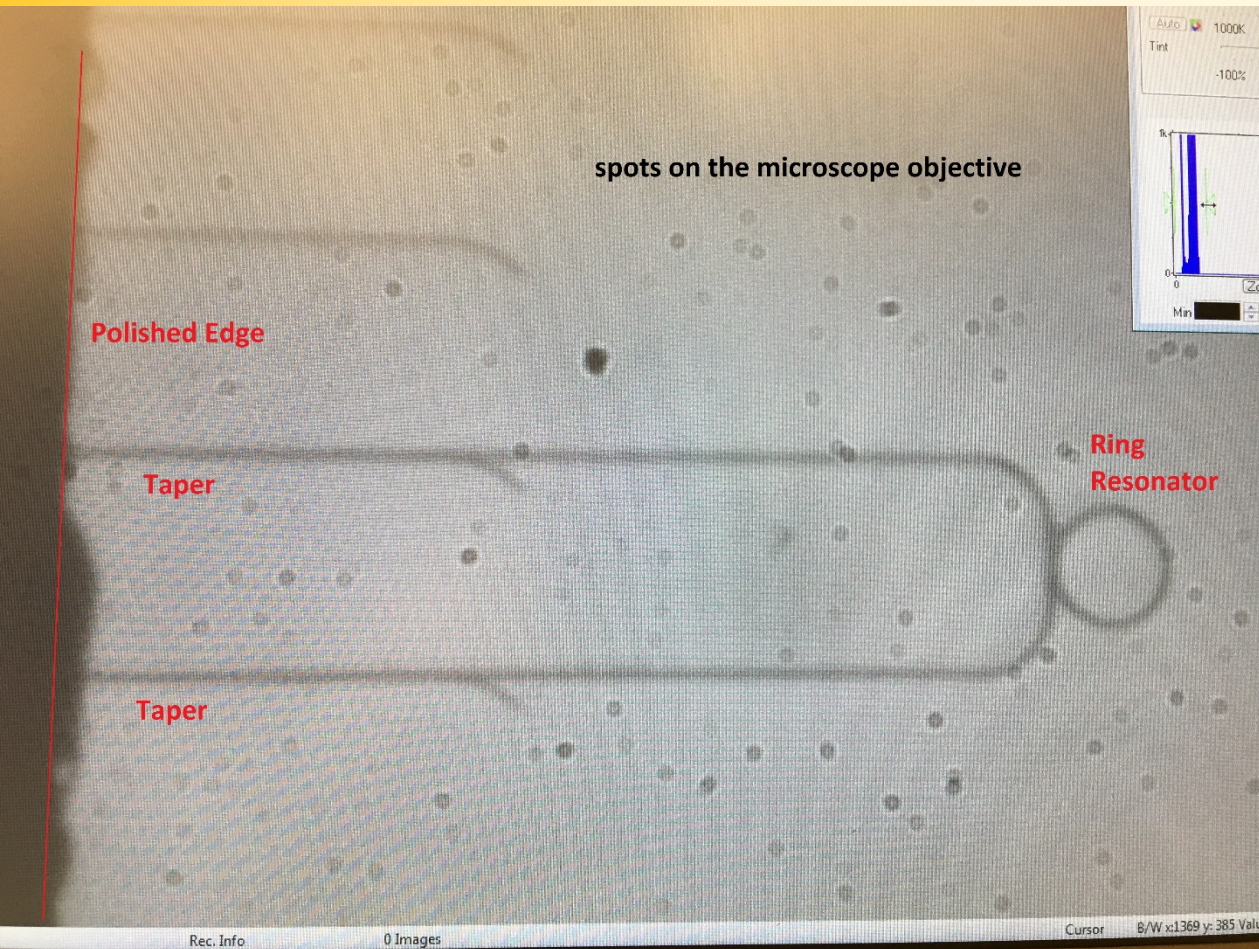
Edge  
polished



Reference: Dr. Pearson



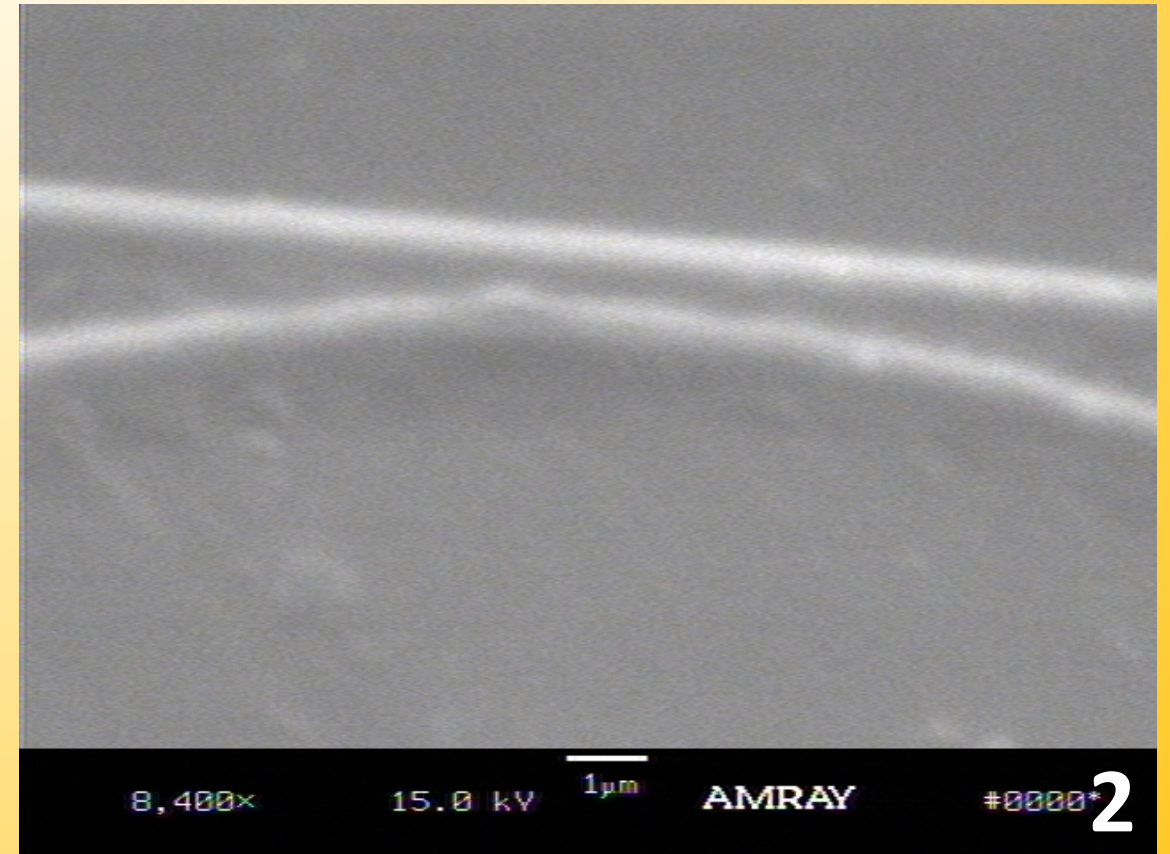
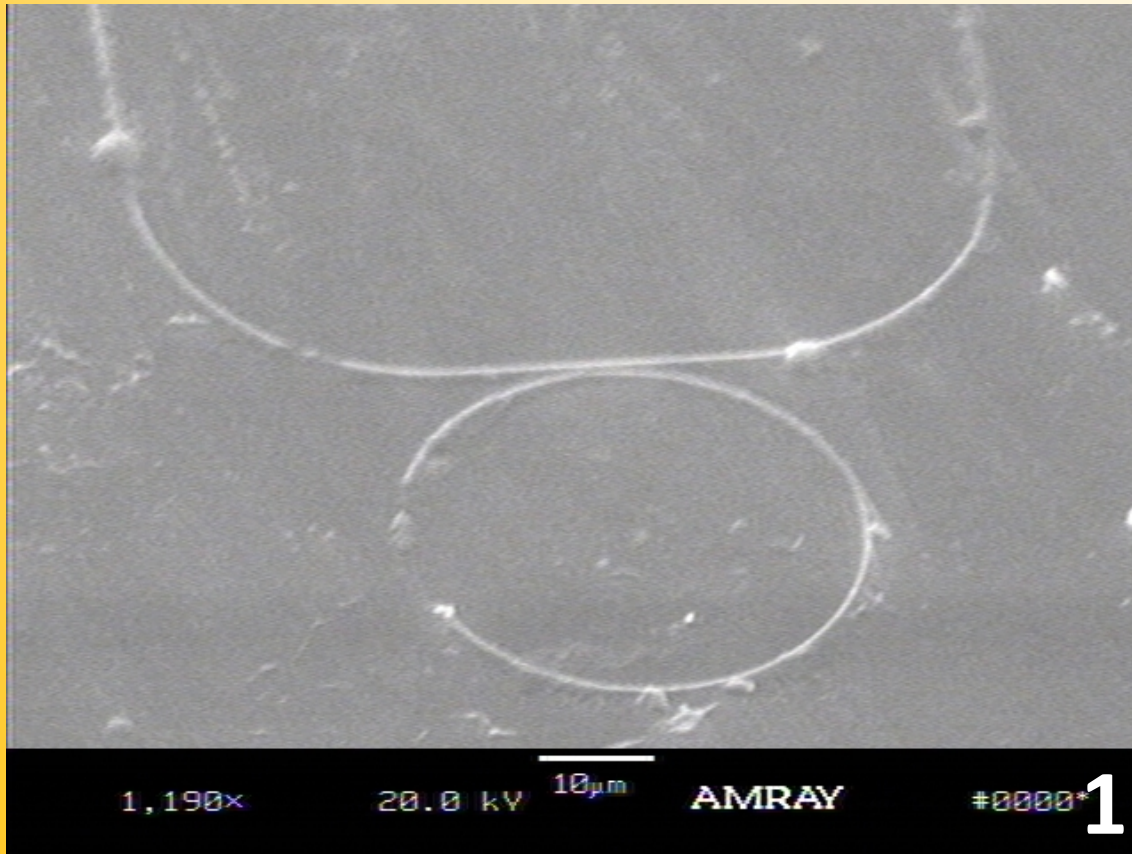
# Testing Results



Thanks to Michael Fanto and Jeffrey Steidle for testing



# SEM pictures



Thanks to Sean O'Brien for these pictures

# Conclusions

- A process for realizing waveguides on a-Si was developed
  - The process only takes one week to fabricate
  - Future short course could be designed around fabricating and testing waveguides
- Finished waveguides demonstrated coupling during testing
  - There is a chance some will show resonance as well but testing is slow
- Thus, the project was a success 😊

# There's still work that needs to be done...

- Characterizing a more stable etch process
- DRM for the nLOF dilution
- Longer waveguides with more waveguides per cell

# Acknowledgements

- My advisors, Drs. Preble, Pearson and Ewbank, for their guidance
- Patricia Meller and Sean O'Brien for all their processing help and knowledge
- The SMFL staff for fixing everything I broke
- Dr. Fuller for the steam oxide growth recipe
- Dr. Hirschman and Corning Inc. for the a-Si deposition
- Frank Byrne and Orthogonal Inc. for the negative-tone resist
- Stephanie Bolster for assistance with the ASML stepper
- Ankur Lamoria for help with etching
- Corey Shay and Eric Evangelou for miscellaneous processing help
- Michael Fanto and Jeffrey Steidle of the RIT Integrated Photonics Group for testing