Ferroelectric HfO_2 Thin Films for FeFET Memory Devices

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Project Objectives

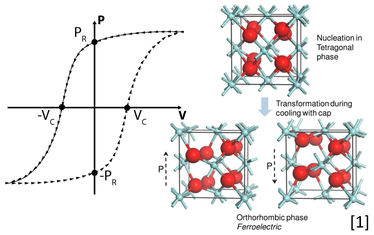
Goal: To demonstrate a functioning ferroelectric field-effect transistor (NMOS FeFET) for use as an inherent memory device. This is a proof of concept for ferroelectric hafnium-based device fabrication at RIT.

1. **Design Process Flow**
2. **Develop Mask**
3. **Develop Process Flow**
4. **Fabricate Devices**
5. **Electrical Testing**

Background and Device Operation

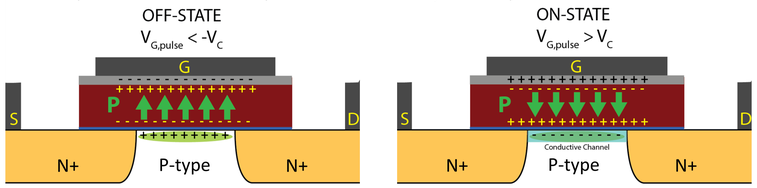
Ferroelectricity is a material property where the material has the ability to have spontaneous polarization from an applied electric field.

An HfO_2 based film for a ferroelectric layer is beneficial for integration into standard CMOS due to the maturity of HfO_2 as a high-k dielectric in modern process technology.



[1]

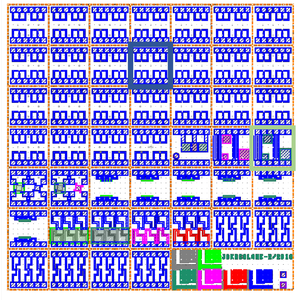
Through the use of dopants, a capping layer for stress, and annealing conditions ferroelectric HfO_2 can be fabricated. [1] This project focuses on silicon doped HfO_2 with a TiN capping layer that is deposited and annealed by NaMLab in Dresden, Germany.



FeFETs have advantages such as a simple one-transistor (1T) memory cell design with a read and write latency in the nanosecond range [2]. In the ON state, there is an effective shift lowering of the threshold voltage. In the OFF state, there is an increase in V_T.

When a voltage greater than V_C (coercive voltage) is applied to the gate, causing negative charge in the substrate, the device is shifted into the ON state. Voltage on the gate is returned to 0V, there is a positive remnant polarization charge ($+P_R$). The OFF state is the opposite.

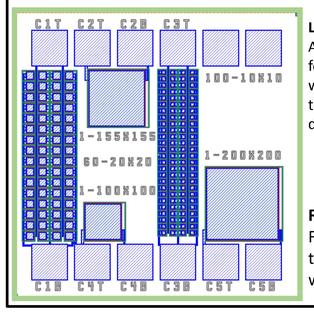
Mask Design



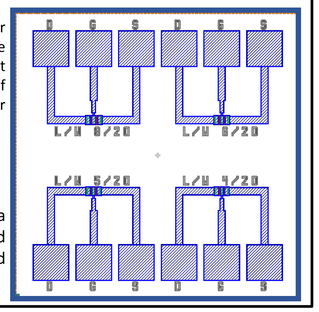
Design Considerations: 4-Levels for FeFET process flow. The mask is conservative with overlap of the gate dielectric and the metal gate contact to ensure control of the channel.

The full chip layout is shown on the left which includes a variety of test structures:

- Array of FeFETs with varying dimensions,
- MFIS capacitors
- TLMs
- CBKRs
- Van Der Pauw's structures
- Resolution and alignment marks



Left: MFIS Capacitor Array used to test the ferroelectric effect without the influence of the semiconductor depletion.



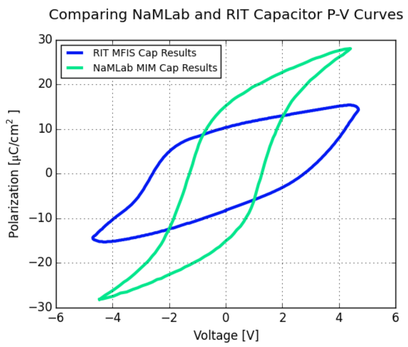
Right: Example of a FeFET cell layout used to test lengths and widths.

Experimental Results

Confirmation of ferroelectric Si:HfO_2 using the aixACCT TF1000 Ferroelectric Tester on capacitors compared with reference MIM capacitor data from NaMLab.

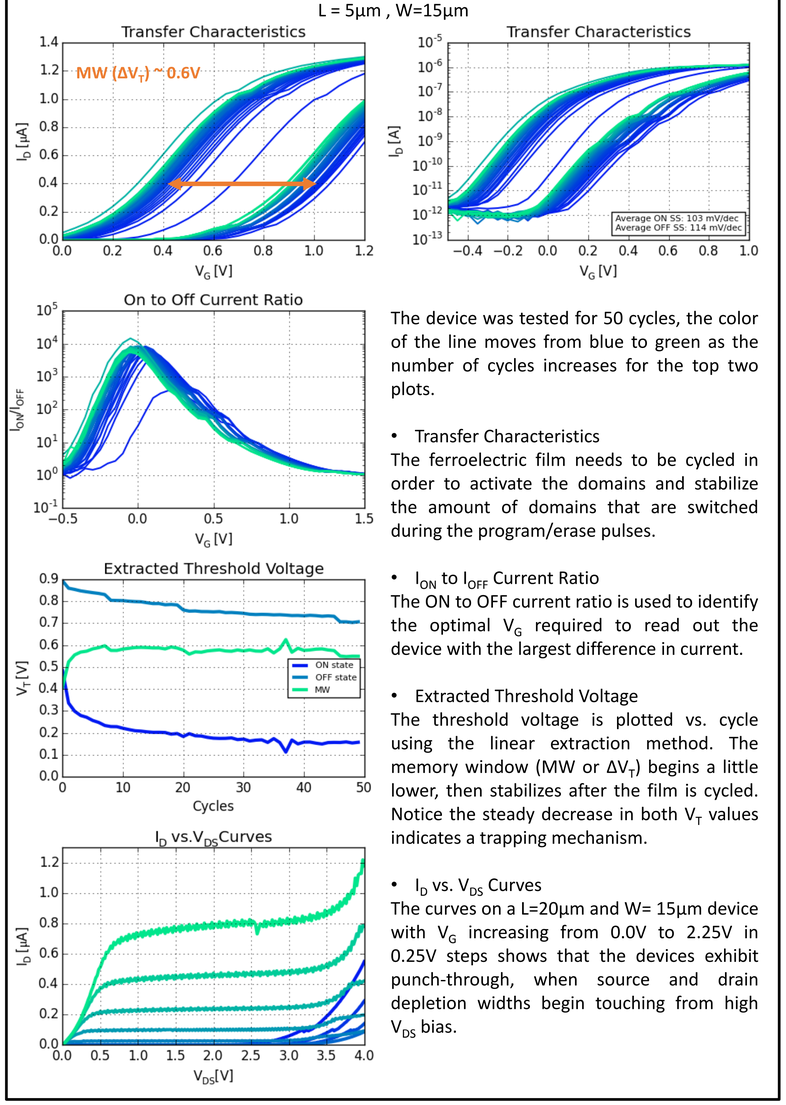
The differences can be attributed to the difference in material stack and the process variation. The film is identical, but it was pattered differently and the NaMLab sample is an MIM stack while the RIT stack is MFIS (N+ Si).

Degradation due to many factors such as non-switching domains, depolarization fields, and interface charges.



I-V Characteristics

FeFET Memory and Cycling Characteristics
L = 5μm , W=15μm



The device was tested for 50 cycles, the color of the line moves from blue to green as the number of cycles increases for the top two plots.

- Transfer Characteristics

The ferroelectric film needs to be cycled in order to activate the domains and stabilize the amount of domains that are switched during the program/erase pulses.

- I_{ON} to I_{OFF} Current Ratio

The ON to OFF current ratio is used to identify the optimal V_G required to read out the device with the largest difference in current.

- Extracted Threshold Voltage

The threshold voltage is plotted vs. cycle using the linear extraction method. The memory window (MW or ΔV_T) begins a little lower, then stabilizes after the film is cycled. Notice the steady decrease in both V_T values indicates a trapping mechanism.

- I_D vs. V_{DS} Curves

The curves on a L=20μm and W= 15μm device with V_G increasing from 0.0V to 2.25V in 0.25V steps shows that the devices exhibit punch-through, when source and drain depletion widths begin touching from high V_{DS} bias.

Processing and Captures

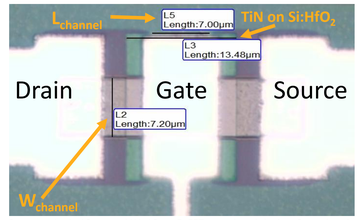
The process was designed to be robust and enable the highest probability to realize devices.

The main processing constraint came from a low thermal budget after the Si:HfO_2 was deposited and annealed as to not change the crystalline structure. This restriction led to:

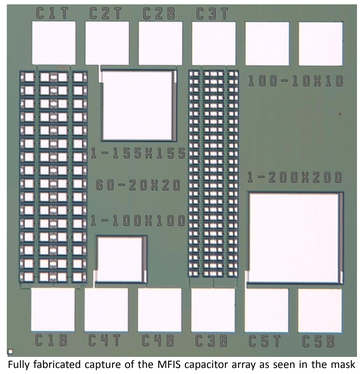
- Gate last process with larger designed overlap of gate on the channel to ensure control of the channel.
- Source/Drain pattern and anneal done before Si:HfO_2 deposition
- No ability to use silicide S/D contacts due to high temperature.
- No inter-level-dielectric to reduce charges from low-temperature oxides

The main road block for processing at RIT was etching the Si:HfO2 film. A process was developed using the LAM 4600 and N_2, BCl_3, CL_2, and Ar to get an etch rate of 5.3 nm/min. The flow ratios were defined to be the same as [3].

- There is a dependence on the etch rate from cycling and leaving the chamber, so a delay in N_2 should be used to reduce damage of photoresist from overheating.



Capture of a L=10μm and W=10μm FeFET completed device. Some loss in W due to LOCOS and loss in L due to diffusion of carriers and variation in lithography.



Fully fabricated capture of the MFIS capacitor array as seen in the mask design section. Array wiring was too aggressive and some were lost.

Conclusions and Future Work

The process that is developed, demonstrates functioning n-channel FeFET for use as a memory device with standard CMOS compatible Si:HfO_2.

- The Si:HfO_2 film that was deposited using atomic layer deposition was etched using chlorine based gases with an etch rate of 5.3 nm/min
- The MFIS capacitors demonstrated a remnant polarization of ~10μC/cm_2 with a coercive voltages of ~2.5V with a 10.0 nm ferroelectric layer.
- The MFIS stack using Si:HfO_2 deposited by NaMLab demonstrates a shift in threshold voltage, or memory window, of ~0.6V which is independent of the transistor dimensions.

Future work can be done with this process flow to optimize device performance. Additionally, an investigation and demonstration can be done of a negative-capacitance FET that utilizes an anti-ferroelectric or ferroelectric film to increase the sub-threshold slope beyond the theoretical limit of 60 mV/dec.

References

[1] T. S. Boscke, J. Muller, D. Brauhaus, U. Schroder, and U. Bottger, "Ferroelectricity in hafnium oxide thin films," *Applied Physics Letters*, vol. 99, no. 10, 2011.

[2] E. Yurchuk, *Electrical Characterisation of Ferroelectric Field Effect Transistors based on Ferroelectric HfO2 Thin Films*. Logos Verlag Berlin GmbH, 2015.

[3] Y. H. Joo, J. C. Woo, X. Yang, and C. I. Kim, "Temperature Dependence on Dry Etching of Hafnium Oxide Using an Inductively Coupled Plasma," Ferroelectrics, vol. 406, pp. 176-184, 2010.

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