

## I. Project Objectives

**Goal:** To develop reliable, in-house solutions to the processing challenges associated with GaN materials. In particular:

- To develop a coating procedure for OiR-620 photoresist on GaN.
- To develop a GaN etch recipe on the LAM4600 reactive ion etcher.
- To develop a coating procedure for LOR-5A resist on GaN.

## II. Motivation

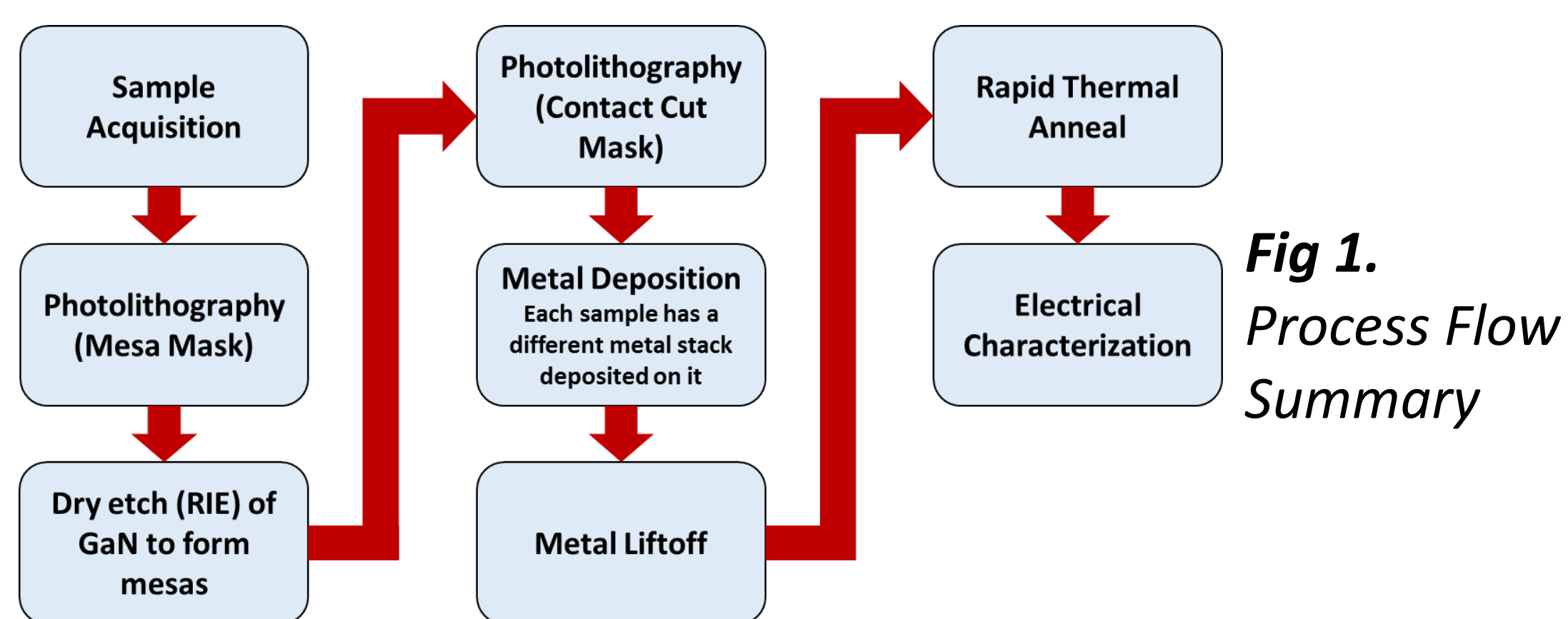
For decades silicon has been the semiconductor of choice used in the manufacturing of integrated transistors. As the scaling of Si-based devices begins to near its physical limit alternative materials with superior electrical performance need to be considered if the development of new and improved transistors is to be maintained for future device generations. To this end, there has recently been an increased effort in the development of production-ready III-V compound semiconductors.

GaN is one such semiconductor that is an appealing alternative to Si. GaN has higher bulk mobility than Si, higher on-currents and lower off-currents, and has better thermal stability, making it a great choice for high power FETs and high frequency applications.

This project was originally centered around the fabrication of low resistance Ohmic contact to n-GaN and AlGaIn materials, but due to setbacks became focused on the development of new processing solutions.

## III. Procedure

Transfer Length Method (TLM) structures were to be used to characterize the contact resistance of different metal stacks. The process outline of their fabrication can be seen below in Fig 1.



The mesa etch was performed on the SMFL's LAM4600 Reactive Ion Etcher. This was the first time GaN was etched using this tool, and as such a new etch procedure needed to be developed to perform the etch.

## IV. Sample Acquisition

Samples were acquired from Texas Instruments (TI), Veeco, and RIT alumnus Brian Romanczyk.

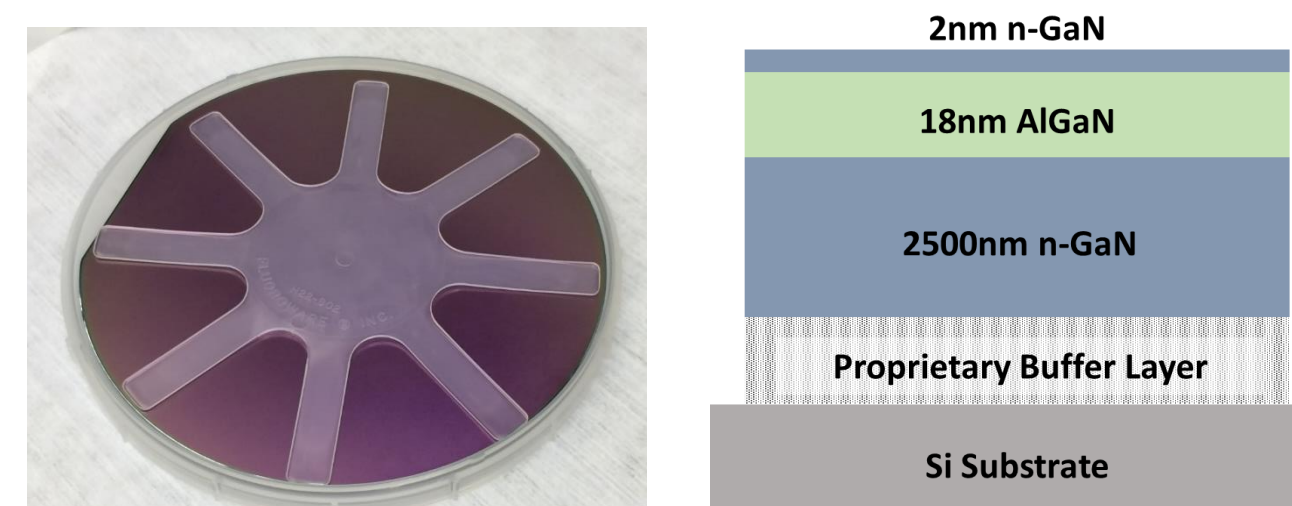


Fig. 2. Texas Instruments provided 6" GaN-on-Si Wafer.

The majority of the subsequent processing occurred on the cleaved pieces of the 6" GaN-on-Si wafer provided by TI.

## V. OiR-620 Coating Procedure

OiR-620 was coated onto GaN pieces. The optimal coating procedure was determined iteratively and was found to be:

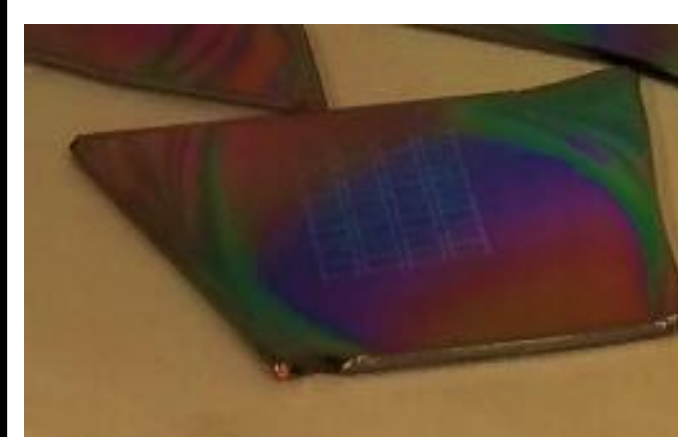


Fig 3. OiR-620 on a GaN piece, mesas patterned.

Puddle Coat,  
Step 1: 1500 RPM, 1s  
Step 2: 3500 RPM, 40s  
Step 3: Ramp down, 10s

99% of die were usable, and resist coated uniformly over the piece.

## VI. LAM4600 Etch Results

BCl<sub>3</sub>, Cl<sub>2</sub>, CHCl<sub>3</sub>, and Ar were used to produce a stable, uniform reactive ion etch of the GaN material. Low power was used so as to not burn the photoresist onto the wafer, and profilometry was used to verify the etch rate and mesa depth resulting from the etch.

### Etch Recipe

Pressure (mTorr)	100
RF Top (W)	0
RF Bottom (W)	125
Gap (cm)	3
O <sub>2</sub> flow (sccm)	0
N <sub>2</sub> flow (sccm)	0
BCl <sub>3</sub> flow (sccm)	25
Cl <sub>2</sub> flow (sccm)	30
Ar flow (sccm)	20
CHCl <sub>3</sub> flow (sccm)	8

### Etch Results

GaN Etch Rate (Å/s)	3.12
Photoresist Etch Rate (Å/s)	7.65
GaN / PR Selectivity	1 / 2.45

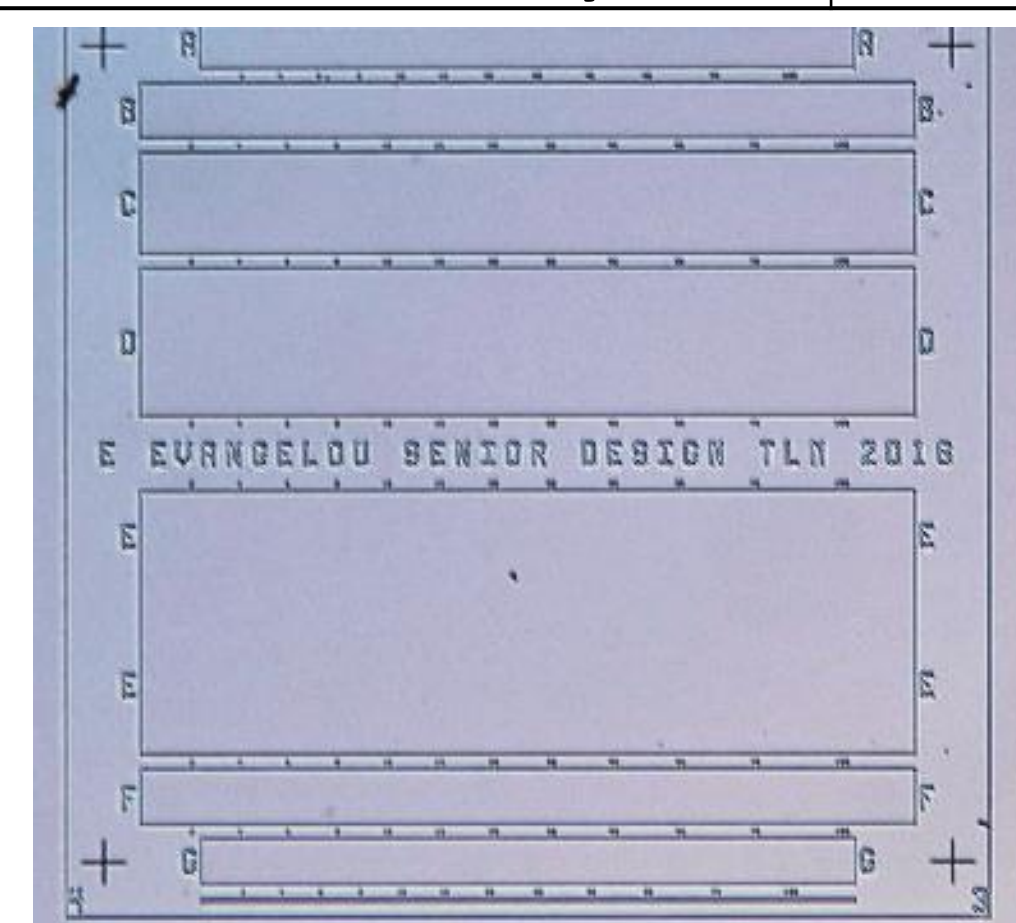


Fig 4. LAM4600 RIE etch results and an image of mesas in a GaN piece.

The low etch rate required that the mesa structures remain fairly shallow at just 100-110nm. The etch was fairly uniform across the 2cm<sup>2</sup> GaN pieces, and was also very anisotropic.

## VII. LOR-5A Coating Procedure

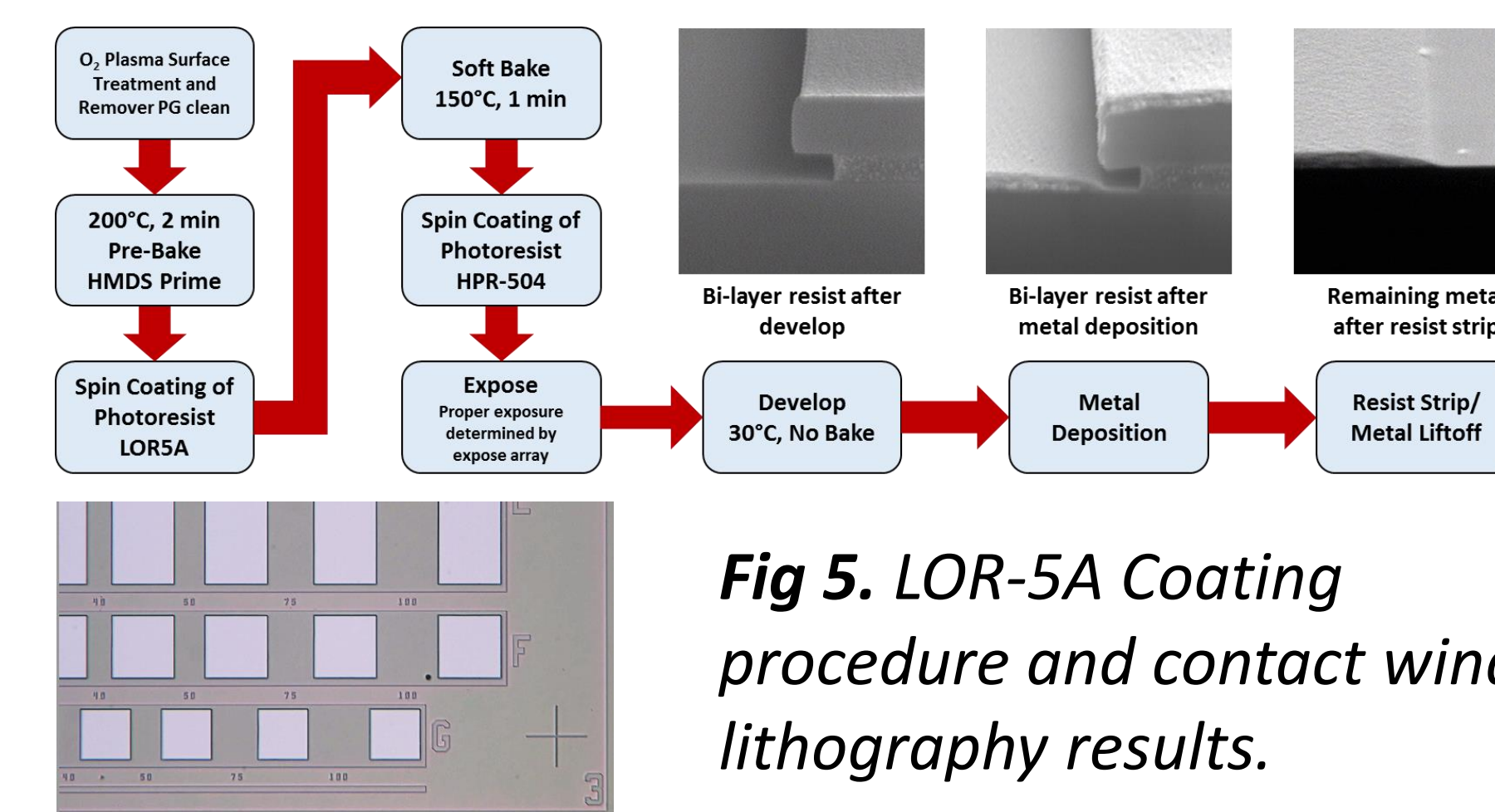


Fig 5. LOR-5A Coating procedure and contact window lithography results.

LOR-5A resist would not adhere to the GaN pieces. An O<sub>2</sub> plasma surface treatment was also performed to help clean the surface, as well as a Remover PG clean. The addition of an HMDS prime and an extended, hotter pre-bake significantly improved the adhesion of the LOR5A to the GaN substrate. Contact windows were defined. An alignment offset of +/-10μm in both the x and y directions was allowable to make processing on pieces easier.

## VIII. Conclusions

- GaN samples were acquired from TI, Veeco, and an RIT alumnus.
- A successful etch recipe was developed for the etching of GaN on RIT's LAM4600 RIE tool.
- Coating procedures were developed for the application of LOR-5A liftoff resist and OiR620 positive photoresist on GaN substrates.
- The procedures developed during this project will assist future GaN-focused projects in the SMFL, which will allow for the development of new and exciting opto-electronic and power-electronic devices.
- **The original project objective was partially met: a contact to n-GaN was fabricated, it was just never optimized for low resistance.**

## References

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## Acknowledgements

- **My sincerest thanks to the entire staff of the SMFL. Patricia Meller, Sean O'Brien, and John Nash in particular have been tremendously supportive of my work.**
- Drs. Zhang, Pearson, and Ewbank for all of their advice.
- Cheng Liu and Yukee Ooi, for their help with photoluminescent characterization of samples.
- Texas Instruments for its generous donation, and in particular Joe Williams for his help arranging it.
- Brian Romanczyk, for the supplied materials.
- Dr. Rommel, for his reassuring reminders.