Silicon Photonic Devices Manufactured Using Double-Patterned i-Line Lithography

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I. Project Objectives

Goal: To create working photonic waveguides on a-Si in the RIT SMFL

- Characterize a double-patterned i-line lithography process and associated stepper job for sub-300nm waveguide spacings
- Develop a silicon etch process optimized for sidewall angle and smoothness
- Demonstrate working waveguides and ring resonators

II. Motivation

- Due to power issues, the fundamental limits of voltage and frequency in electrical interconnects are nearing
- Intricate electrical interconnects are not scalable because the maximum bandwidth is limited by the available area
- Optical interconnects are the best solution because they operate with ultra-high bandwidth (>100THz) and are very low power
- Thus, integrated photonics—the intersection of microelectronics and photonics—is necessary to continue advancing technologically

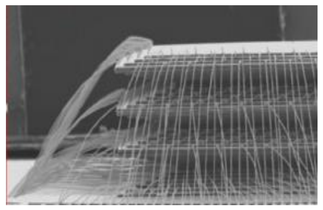

Fig. 1: *Densely integrated metal interconnects.*

III. Background

Waveguide Theory

- Waveguides use total internal reflection to guide photons
- Total internal reflection occurs when a wave hits an interface at an angle larger than the critical angle of the interface

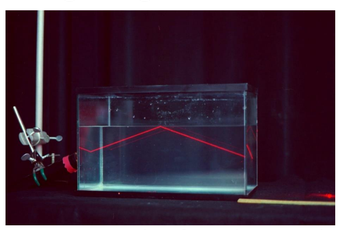

Fig. 2 *Example of total internal reflectance.*

- The critical angle of the Si-SiO_2 interface is:

$$\text{asin}(n_{Ox}/n_{Si})=\text{asin}(1.5/3.5)=\theta_C=24.93°$$

- Therefore, bends of <1.5µm can be achieved, resulting in very compact devices
- Silicon is transparent in the infrared; this confines the light

III. Background contd.

Ring Resonator Theory

- A ring resonator is like a switch; it is often used in conjunction with waveguides to manipulate transmission losses through coupling
- If the spacing increases past its allowable maximum, there will be no coupling so transmission will be high
- Resonance occurs when the wavelength is an integer multiple of the ring's circumference:

$$m(\lambda/n)=2\pi R$$

IV. Proposed Work

The intended waveguides can be achieved through the growth, deposition and etching of oxide and amorphous silicon

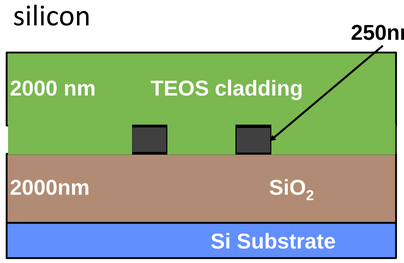

Fig. 3: *Side-view (not to scale).*

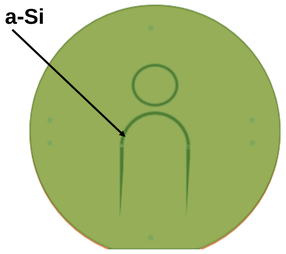

Fig. 4: *Top-view (not to scale).*

V. Results

Oxide Growth

- 2µm of oxide was grown on RCA-cleaned silicon substrates using Dr. Fuller's 410 Recipe in the Bruce Furnace [1]
- The average thickness of the grown oxide was 2.18µm

a-Si Deposition

- 250nm of a-Si was deposited at Corning, Inc.
- These thicknesses were very difficult to verify

Double Exposure Lithography

- The a-Si was patterned with the RIT_Preble2014 mask on the ASML 5500 with diluted nLOF 20-20, a negative resist provided by Orthogonal, Inc.
- The lithography required a double pass:
  - First for the waveguide,
  - Then for the ring resonator at spacings ranging from 200-1000nm
- This is required to feature the sub-300nm waveguide-to-ring spacings necessary for successful coupling

V. Results contd.

Etching

- The etch recipe for the STS ASE Deep Silicon Etcher was developed by Patricia Meller and Ankur Lamoria
- The etch rate was calculated to be 300nm/min

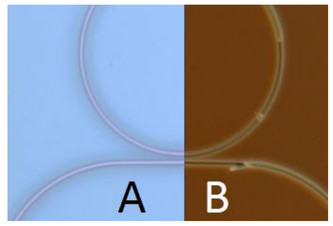

Fig. 5: *The same waveguide after etch. "A" is the waveguide pre-ash, and "B" is post-ash.*

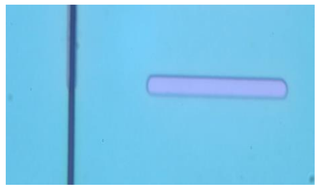

Fig. 6: A successful taper etch. The horizontal line represents the end of the waveguide material.

TEOS Cladding Deposition

- 2µm of TEOS was deposited in Chamber A of the AME P5000 using two iterations of the 1M_TEOS_LS recipe

Fig. 7: *A waveguide after TEOS deposition.*

SEM Images

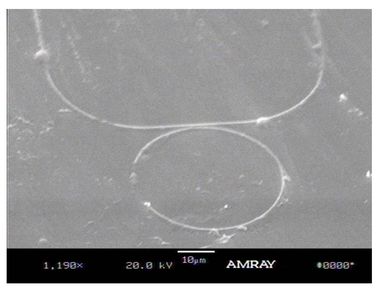

Fig. 8: *SEM of waveguide taken by Sean O'Brien.*

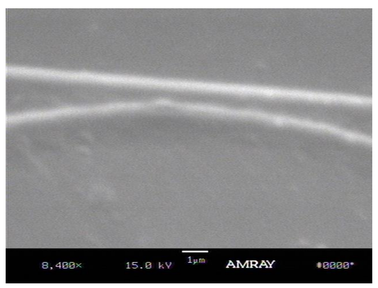

Fig. 9: *Close-up of Fig. 7's waveguide-to-ring spacing.*

VI. Conclusions

All of the primary objectives were met and working devices (that is, tested waveguides showed coupling) were demonstrated. Though more work is required to further optimize the process and increase the waveguide yields, this project has successfully established a baseline for future a-Si waveguide processing in the RIT SMFL.

VII. References

[1] https://people.rit.edu/lffeee/Bruce_Furnace.pdf.