Silicon Photonic Devices Manufactured Using Double-Patterned i-Line Lithography

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ABSTRACT

The purpose of this project is to realize infrared photonic waveguides and ring resonators from hydrogenated amorphous silicon (a-Si) in the Rochester Institute of Technology Semiconductor & Microsystems Fabrication Laboratory (SMFL). The waveguides are intended to be 250 nm thick; the guide-width goal is 500nm at its widest, tapered to 100 nm at the ends for boosting coupling success during testing. The waveguide is arranged in a symmetrical U-shape configuration with the guide-legs designed to be approximately 75μm away from each other and 365μm long on each side. The ring is intended to be 40μm in diameter. This paper covers the critical stages of process development which are categorized as follows: 1) the characterization of the double-patterned i-line lithography process required for sub-300 nm waveguide-to-ring spacings on the ASML PAS 5500 stepper, 2) the development of a silicon etch process designed for straight and smooth a-Si sidewalls in the STS ASE Deep Silicon etcher, and 3) the testing of the finished devices. Though more process optimization is required, initial testing of the devices showed coupling, which denotes this project to have been a success.

Keywords: silicon photonics, integrated photonic waveguides, process development

1. INTRODUCTION

The electronics industry necessitates continual increase in device complexity: the drive is always for smaller, faster devices operated at lower power. This is exemplified by Moore's law, the idea that every two years the number of transistors in an integrated circuit should be doubled. In a playful sense, this is often idiomatically labeled the mantra of the industry. The true force of Moore's law is not, however, either whimsical or dogmatic; ingrained in Moore's law is the electronic industry's innate commitment to the betterment of society. Moore's law provides real product benefits which enable innovation in the more socially pertinent fields of education and healthcare.

Due to power issues, the fundamental limits of voltage and frequency in electrical interconnects are being reached. One potential solution is multi-core computing, but connecting between parallel cores requires intricate electrical interconnects and these are not scalable because the maximum bandwidth is limited by the available area. However, as the physical limits of the contemporary manufacturable transistors are reached, so too do the doors to completely new avenues for further development in electronics unlatch. One such path is that of integrated photonics which implements the manufacturing processes developed for electronic integrated circuits for photonic applications.

As opposed to electron transport, photons move at the speed of light in vacuum and their propagation does not require the consumption of more energy than is used to generate them. These properties imply that photonic circuits could be free from heating effects as well as made smaller, faster, and more power efficient in comparison to conventional electronic circuits. Because not all applications for photonics are practical, the idea is not to replace all electron-based technology with photonics but instead to integrate the two and enable new applications in both industries.

Photonic technologies are just emerging and are where microelectronics were in the 1970's, so there is significant capacity for advancements in this field. The benefits of integrated photonics devices are primarily in encoding data at speeds of Terabytes/second, which is useful in high speed communication. Modern applications include weather

modeling, LiDAR, optical routers, RF photonics, quantum communication and bio-chemical sensing.

In a sense, a waveguide is a "photonic wire" which uses the physics of frustrated internal reflection to guide photons along its path. If spaced close enough to a waveguide, a ring resonator can operate as a switch or modulator using the physics of resonance to control transmission. The substrate most often used in infrared waveguide development is silicon due to its high refractive index which allows it to confine light to a sub-micron area and because it is transparent to infrared light. This is especially fortuitous because silicon is the dominant substrate used in CMOS processing, and thus current CMOS processing technologies could be used in the development of silicon photonic devices. This ease in integration of silicon photonic devices with existing electronic processes makes photonic devices decidedly more appealing to manufacturers.

The primary problem in the field of integrated photonics is not the demonstration of low-loss components such as waveguides, but instead with their packaging. If packaging constraints are addressed and rectified, a device as simple as a waveguide with a ring resonator would be sustainable in a manufacturing environment.

2. THEORY

2.1 The physics of photons

The photoelectric effect for which Einstein was awarded the Nobel Prize in Physics in 1921 showed that light is not only an electromagnetic wave, but also a particle. The experiment is as follows: two metal plates are situated in a vacuum with an adjustable voltage between them; light is shined on one of the plates so as to excite electrons out of the it and the current between the two plates is measured. If light is a classical wave the expectation is that current will increase with increased intensity of the light source and the frequency of the light will not affect anything. The actual observations from this experiment are:

1. The current is observed to be linearly proportional to intensity.
2. The current appears with no delay. (The plate does not need to heat up; the electrons will be emitted immediately).
3. Electrons are only emitted when the frequency exceeds a certain frequency, referred to as the cutoff frequency.
4. The cutoff frequency is determined by the type of metal.
5. The maximum kinetic energy is proportional to frequency once the cutoff frequency is exceeded.

From these observations, Einstein made the following conclusions:

1. Light comes in "particle-like" chunks of energy called photons.
2. Each photon will only interact with a single electron.
3. The energy of a photon depends on the frequency of light so that below certain frequencies a photon will not excite an electron; the energy of a photon is given by equation 1:

$$E=hv \tag{1}$$

where E is energy, h is Planck's constant, and v is frequency.

Photonics is the study of the transmission and detection of light and the main take-away from the photoelectric effect in regards to this is the idea that light can be thought of as both a wave and a particle.

2.2 Total internal reflection

Silicon is the primary chosen substrate for use in integrated photonics largely due to its high refractive index of approximately 3.45. This is because waveguides operate using the concept of total internal reflection (TIR), and silicon's high refractive index, especially in contrast with the insulating oxide both underneath and above whose refractive index

is approximately 1.45, makes for better TIR. Briefly, TIR, which is based on Snell's law, can be visualized as follows:

1. Imagine two mediums with different refractive indices, n_1 and n_2, on top of each other.
2. A wave is sent through the first medium and hits the interface between the two materials at an angle called the incident angle.
    - The critical angle is defined as being the smallest angle at which TIR will occur. See equation 2.

$$\theta_c = arcsin\frac{n_2}{n_1} \quad (2)$$

3. If the material on the other side of the interface has a lower refractive index than the first side, its incident angle is said to be greater than the critical angle, and the wave will be completely reflected and not leave the first medium.

This phenomenon occurs with silicon and oxide. The critical angle of the silicon/ oxide interface is 24.93°; this means that photons going into a waveguide made of silicon and hitting the oxide sidewalls will not escape if the incident angle of the sidewall collision is greater than 24.93°. Because the effective wavelength reduces with higher refractive index material, the silicon substrate can confine the light to a submicron area (for a silicon waveguide, the turn radius can be as small as 3-4μm).

Besides this, silicon is also used because, due to its bonding properties, it is transparent in the infrared but opaque in the visible. This means that any infrared light that is sent through it will be transmitted with little change.

2.3 Waveguide basics

An optical waveguide is, as per its name, a simple device which guides photons with minimal loss into the surrounding cladding using TIR. Figure 1 shows the intended top-down structure and associated dimensions of the waveguides created for this project.

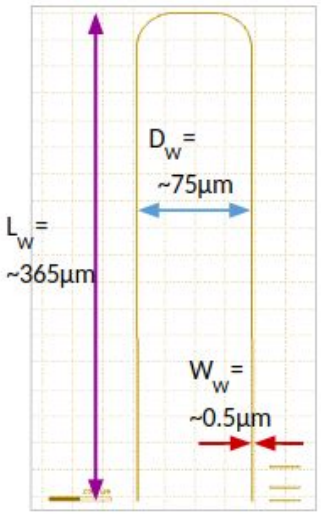


Figure 1. The layout of the waveguide and its associated dimensions.

Figure 2 shows the view if one were to flip Figure 1 *up* and look *into* the waveguide.

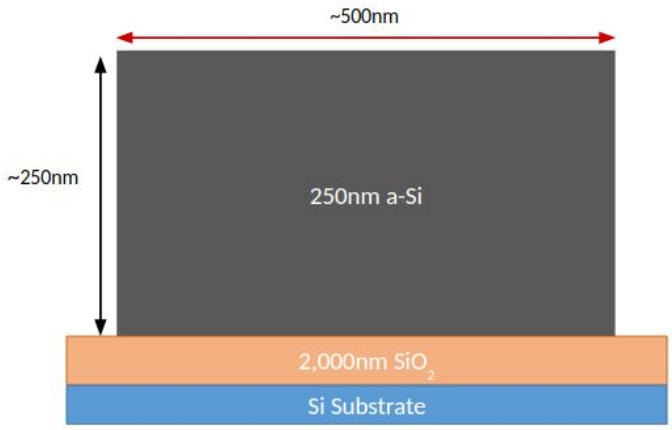


Figure 2. Intended waveguide side view. *Not to scale.*

Throughout this paper, L_W= the length of the waveguide leg, D_W= the distance between the two waveguide legs, W_W= the width of the waveguide leg; meanwhile, L_T= the length of the taper etch opening, D_T= the distance between the two taper etch openings, and W_T= the width of the taper etch opening.

2.4 Ring resonator

As stated briefly in the Introduction, a ring resonator is like a switch or filter. It is often used in conjunction with a waveguide to manipulate transmission losses through coupling. This works as follows: for the same refractive index and ring radius, when the rings are too far apart there is no coupling and so the energy that enters the waveguide will remain in the waveguide, resulting in a high transmission. Meanwhile, closer spacing will result in coupling, which is when some light will enter the ring and remain, and thus the transmission will be lower. Figures 3 through 6 illustrate this.

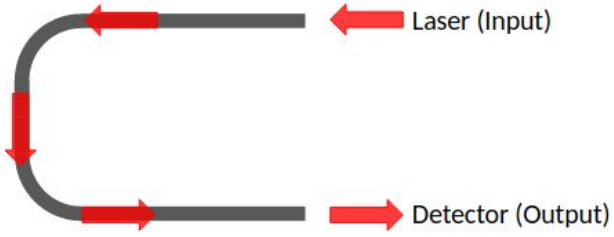


Figure 3. Waveguide with no ring to couple to. Transmission is theoretically 100%. *Not to scale.*

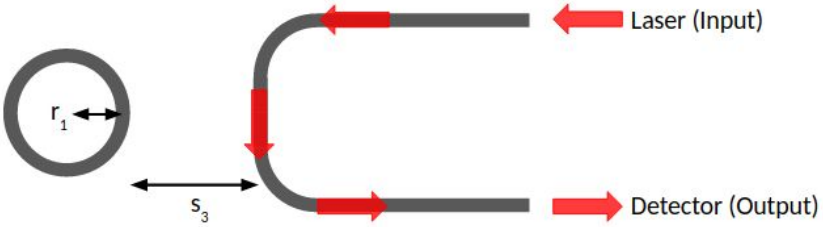


Figure 4. Waveguide with a ring of radius r_1 that are a distance s_3 apart; s_3 is too large, so the ring is too far away to couple to. Thus, again, theoretical transmission is 100%. *Not to scale.*

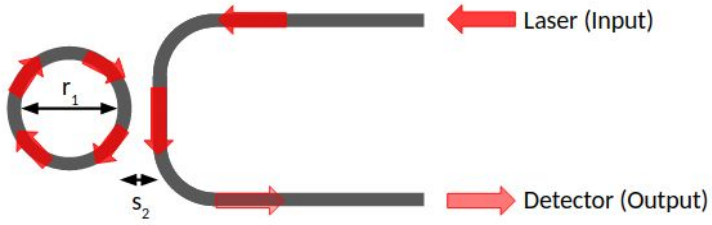


Figure 5. Waveguide with a ring of radius r_1 that are a distance s_2 apart; s_2 is at a distance close enough for coupling to occur. Transmission is therefore <100%. *Not to scale.*

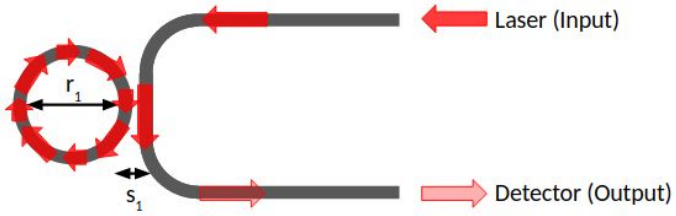


Figure 6. Waveguide with a ring of radius r_1 that are a distance s_1 apart; s_1 is at a distance close enough for coupling to occur that is less than s_2 from Figure 5. Transmission is therefore <100% and also less than when the distance between the two components was s_2. *Not to scale.*

Resonance occurs when the wavelength is an integer multiple of the ring's circumference, and this can be determined by equation 3:

$$m(\lambda/n) = 2\pi R \tag{3}$$

The transmission is 0 when loss around the ring is equal to waveguide-ring power transfer. This is called impedance matching and can be designed for.

2.5 Tapering for improved transmission

For the waveguide to be successfully optically evaluated, not only must the laser and detector (both can be taken to be glass fibers) be placed directly on opposing waveguide ends, but the refractive indices of the waveguide and test materials must be close together so as to limit transmission losses from occurring at these interfaces. One method for doing this is by tapering the ends of the waveguide. As the taper gets smaller the silicon effective index more closely matches the glass fiber and the coupling efficiency gets better. Without the taper it would be difficult to get a significant amount of light into or out of the waveguide. Figures 7 and 8 show the expected transmission differences between a non-tapered and a tapered waveguide.

Figure 7. The refractive index of the glass fiber and the a-Si do not match and so there are multiple reflections at the interface which causes the area of admittance to be small. Therefore, the transmission is low. *Not to scale.*

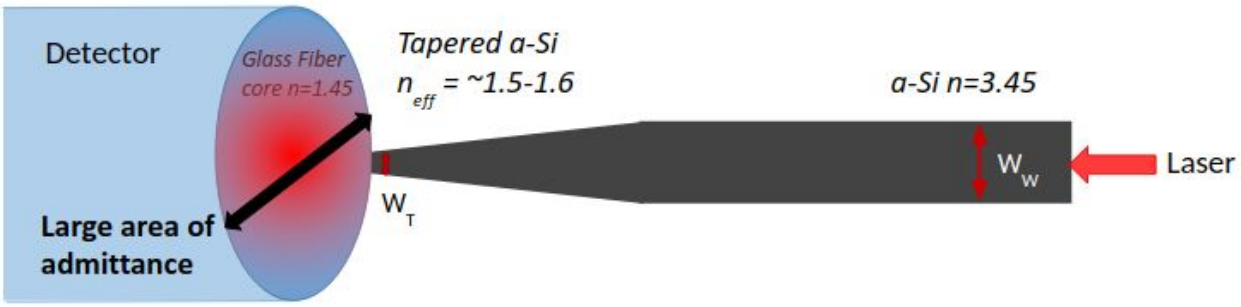


Figure 8. The refractive index of the glass fiber and the effective refractive index of the tapered a-Si are close together and so the area of admittance is large and the transmission is high. W_T, the width of the taper, must be <100 nm for this to occur. *Not to scale.*

2.6 Double-Patterning

The process for forming the tapers is a bit convoluted; due to the small dimensions required (that is, <100 nm), the tapers cannot be exposed simultaneously with the waveguides.

Figures 9 and 10 shows the intended top-down structure and associated dimensions of the waveguide tapers.

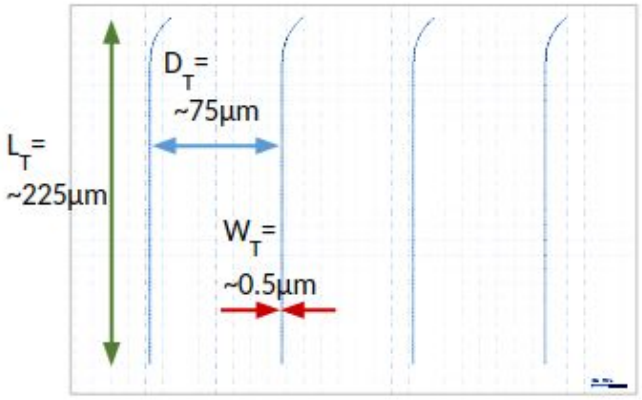


Figure 9. The layout of the tapers and their associated dimensions. The important thing to note here in comparison to Figure 1 is that the use of positive-tone resist means that everything will be protected from the etch, *with the exception* of the area inside the taper-lines.

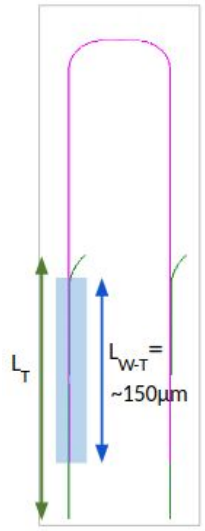


Figure 10. A set of tapers overlaid over a waveguide; the length of the true taper as it appears is approximately 150µm.

Figures 11 through 15 below illustrate the process required for the creation of the tapers.

First, the waveguides are exposed and etched into the a-Si. Figures 11 and 12 are of the starting waveguide and magnified waveguide leg, respectively.

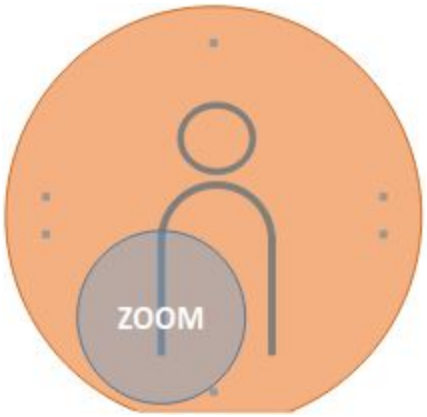


Figure 11. The waveguide prior to tapering. Note that the waveguide is clearly not this big on the wafer; it is magnified here and throughout this paper for clarity.

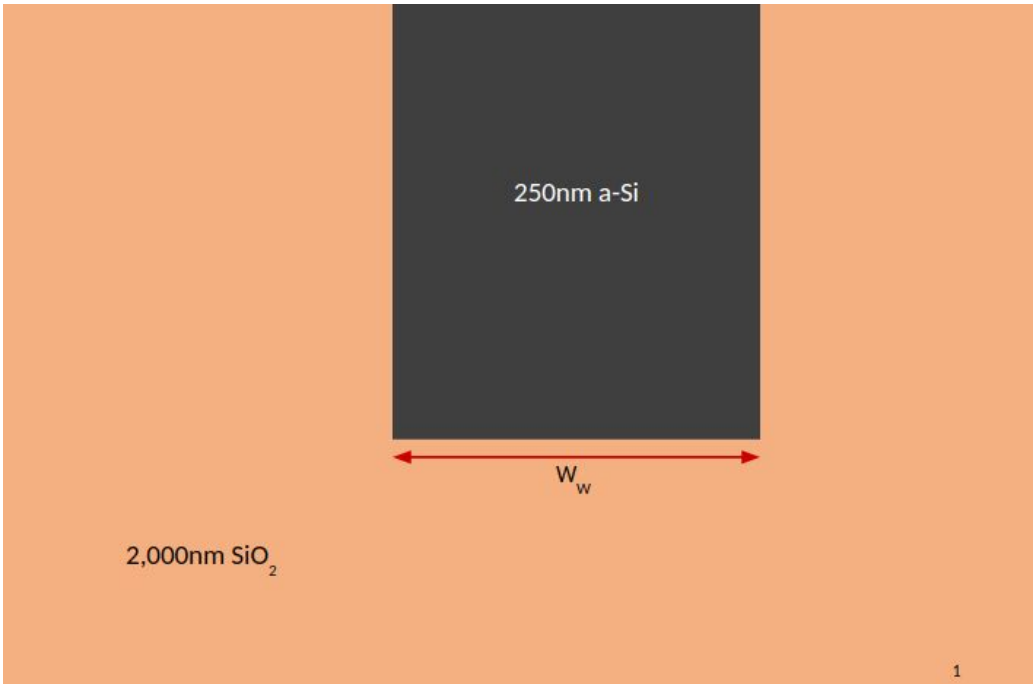


Figure 12. The waveguide end prior to tapering.

After the waveguides have been etched, using positive resist, the area to be etched is exposed. Figure 13 shows where this "cut" will go and Figure 14 shows it in action. This "cut" feature bypasses the SMFL's resolution limits of lithography based on the concept that the ASML's alignment is slightly better than 50nm.

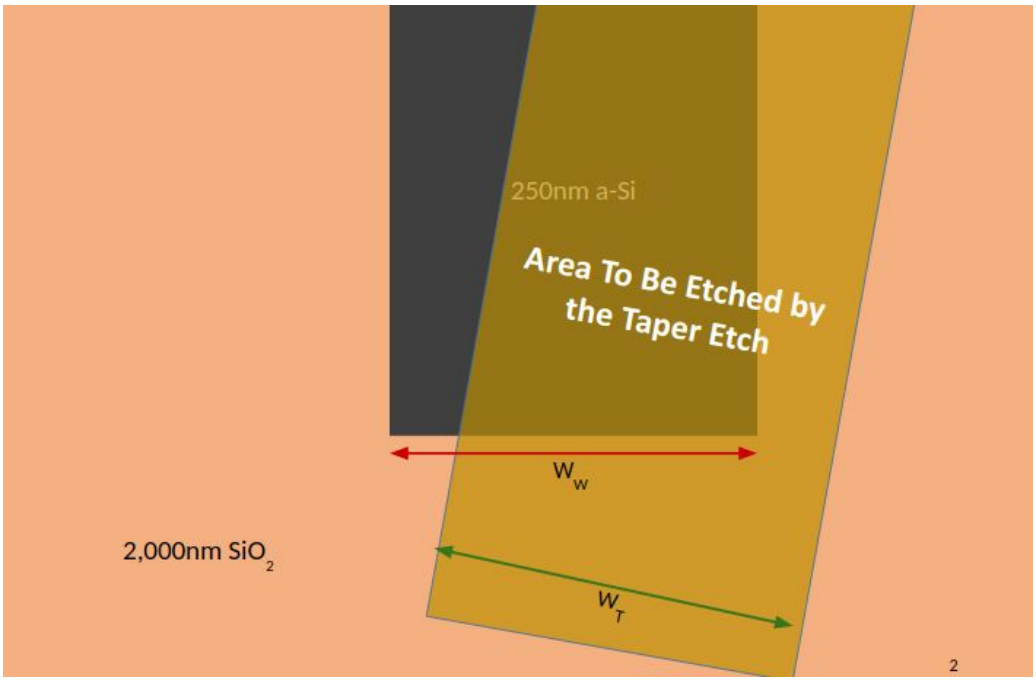


Figure 13. The location of the area to be etched by the taper etch as defined on the mask.

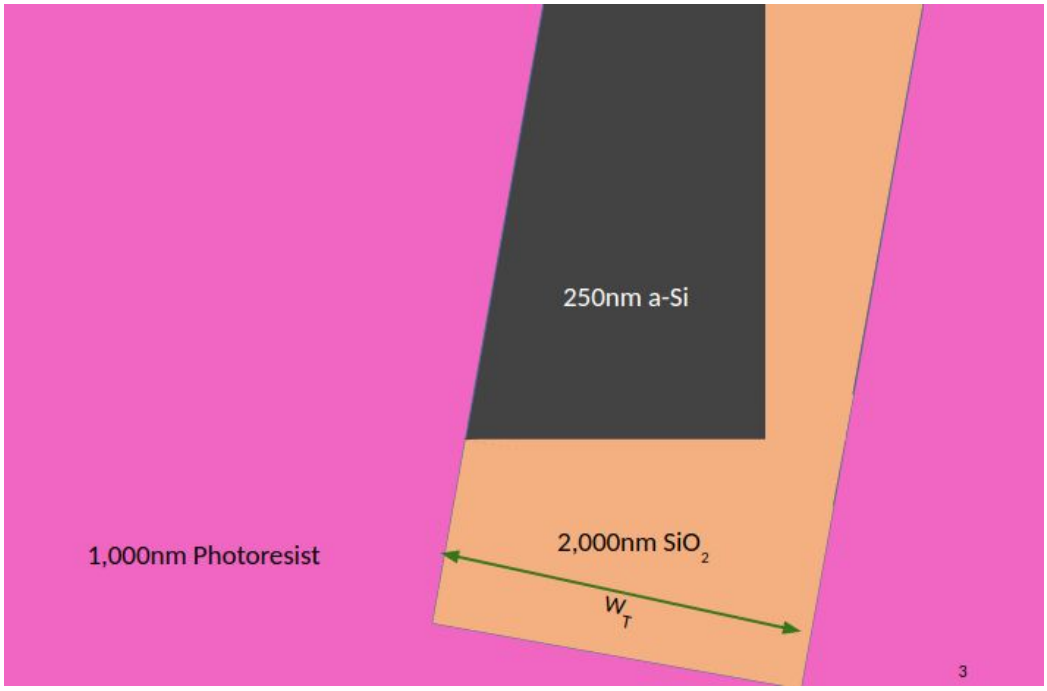


Figure 14. The results of the taper etch exposure.

Finally, the taper cut area is etched, leaving a "tapered" a-Si waveguide end.

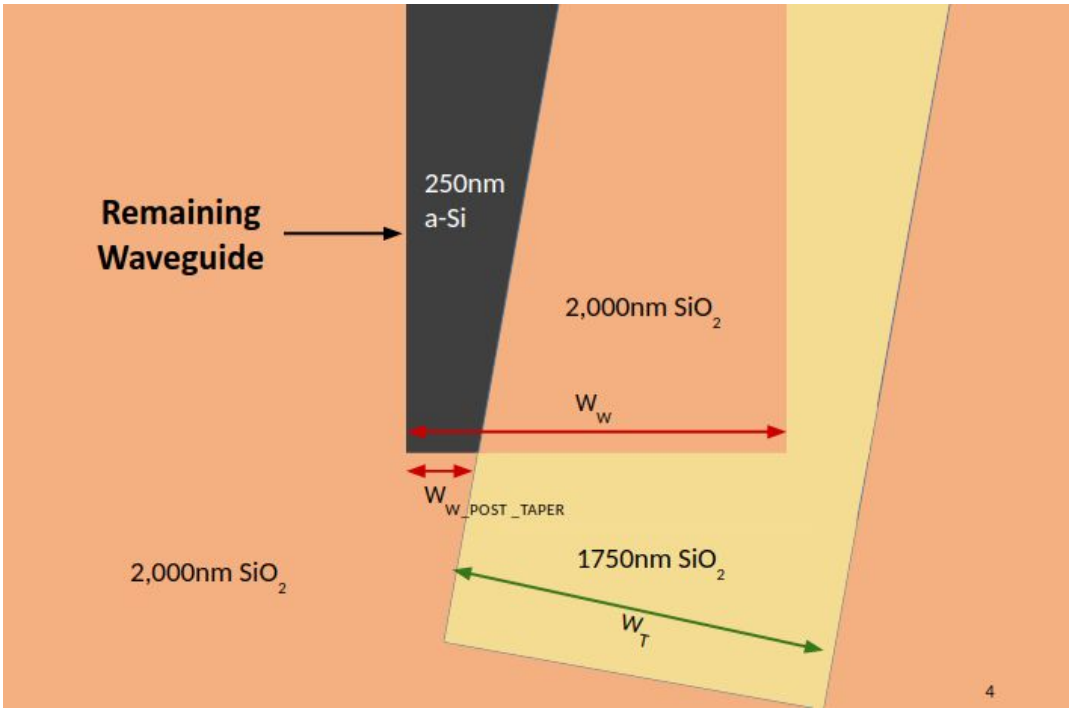


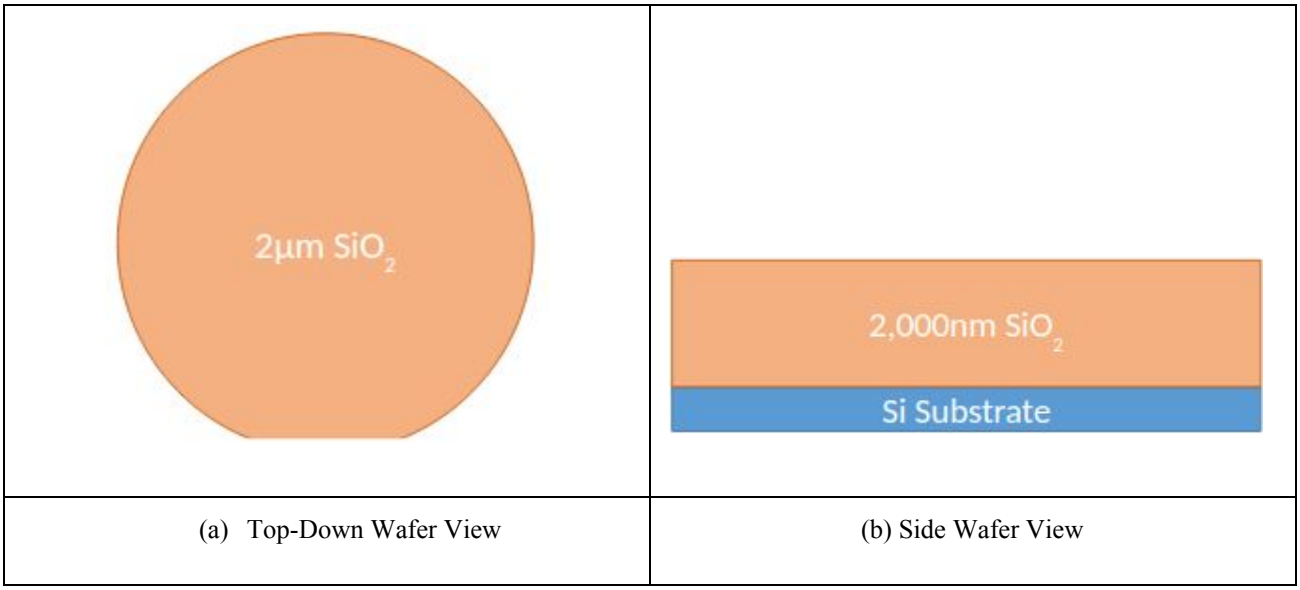
Figure 15. The remaining waveguide after the tapered etch.

Note that this idea of using the ASML's alignment as a tool for achieving better resolution is also used to define the rings in relation to the waveguides so that they have sub 500nm spacings; if the spacings are any bigger, coupling is significantly less likely to occur.

3. EXPERIMENT

A simplified version of the process is as follows: **(1)** a thick layer (2µm) of silicon dioxide (SiO_2, or colloquially 'oxide') is grown on silicon substrates; **(2)** a thin layer (0.25µm) of a-Si is deposited; **(3)** alignment marks are created; **(4)** the a-Si is patterned for the waveguides and rings using double-patterning and negative resist; **(5)** the a-Si is etched so only the waveguide and rings remain; **(6)** the wafers are patterned for the tapering of the waveguide ends using positive resist; **(7)** the ends of the waveguides are etched; **(8)** finally, a thick layer (2µm) of oxide is deposited for cladding. Each of these steps is outlined in more detail below.

3.1 Grow 2µm SiO_2 in Tube #1 of the SMFL Bruce Furnace



(a) Top-Down Wafer View | (b) Side Wafer View

Figure 16. Process views of the first oxide growth step. *Not to scale.*

1. An RCA clean must be performed on the fresh silicon substrates prior to any processing; this is required before the oxidation to keep the tube clean and allow for more uniform growth.
2. Prepare Tube #1 of the Bruce Furnace for oxidation growth as per the manual.
3. Edit Recipe #410 (see Figure 17 below) for an increased hydrogen/ oxygen soak time of 500 minutes. This was calculated using Dr. Lynn Fuller's Excel calculator to result in approximately 20,218 Å of oxide.

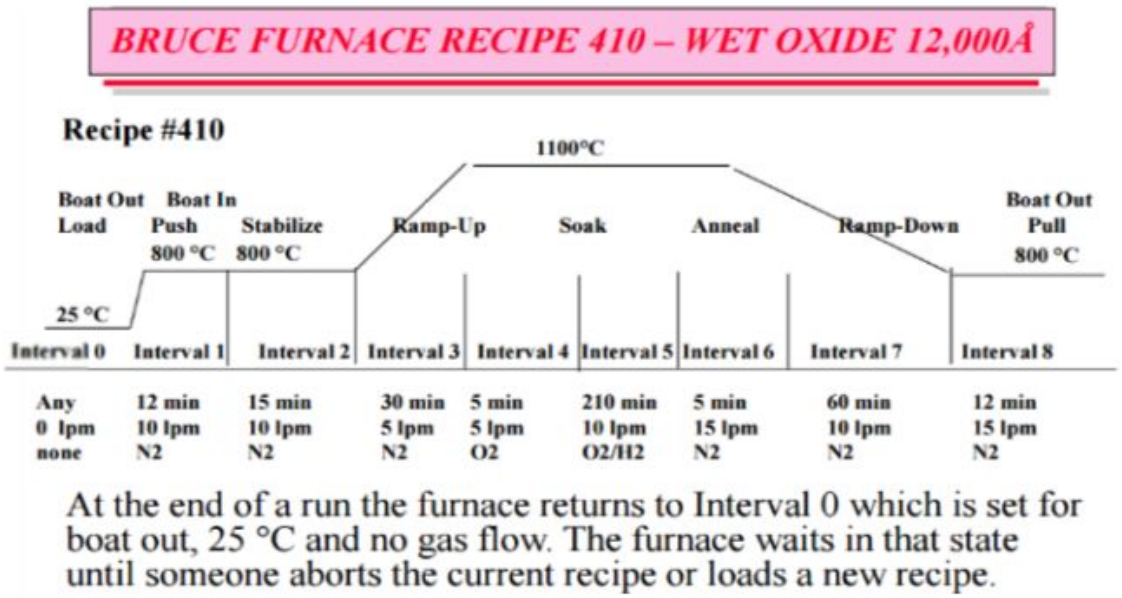
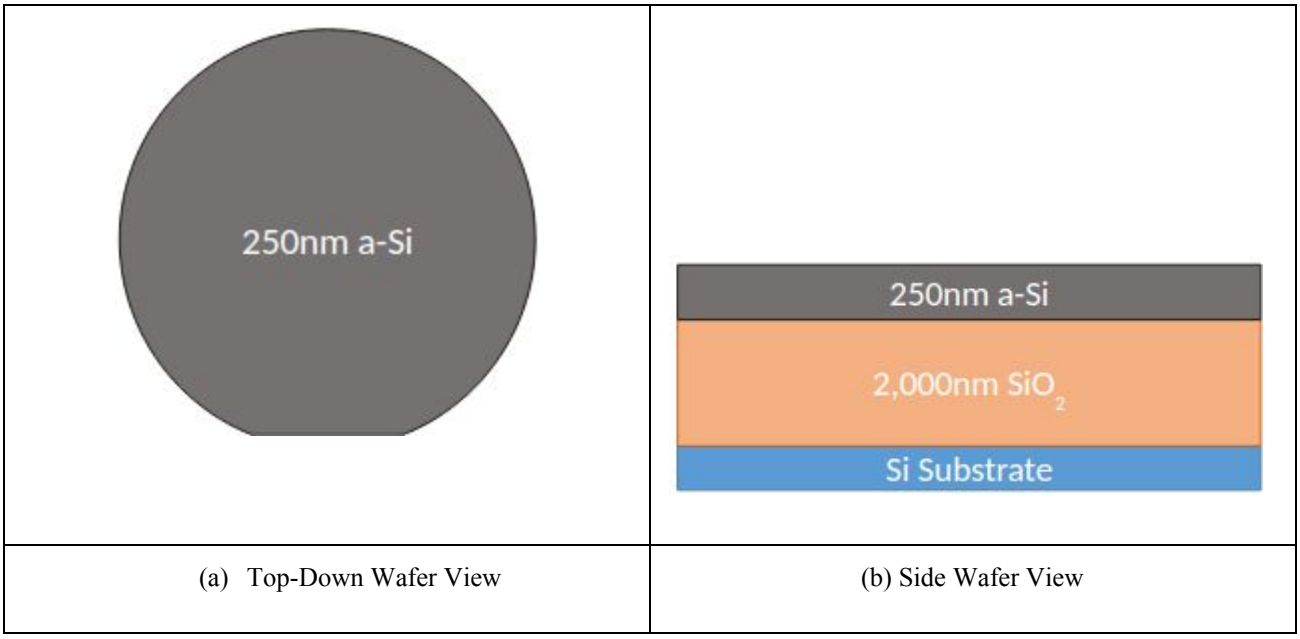


Figure 17. Note that while this figure calls this process 'wet oxide,' the oxidation is technically in steam.[1]

4. Run Recipe #410 edited for the new time.
    - Do not edit any recipes without permission from Dr. Fuller, or relevant SMFL technicians or process engineers.
    - Due to the dangers associated with it, hydrogen is not permitted to run in the SMFL after hours (after 5pm Mon-Fri) without a technician or process engineer present, so for hydrogen to be flowing during the 500 minute soak, the oxidation must be started at 8am for the process to be done in reasonable time.
    - Alert the relevant SMFL technicians and process engineers before running this process in case it will not be done before the SMFL closes or the operator is not able to watch the tool for the full duration of the oxide growth.
5. Once the growth is completed and the wafers are evacuated from the tube.
6. Edit the Recipe #410 hydrogen/oxygen soak time back to 210 minutes, and follow proper shutdown procedure for the tool.
7. Measure the oxide thickness of the wafers using the Spectramap and record the average and standard deviations for each wafer.

3.2 Deposit 250 nm amorphous silicon at Corning Inc.

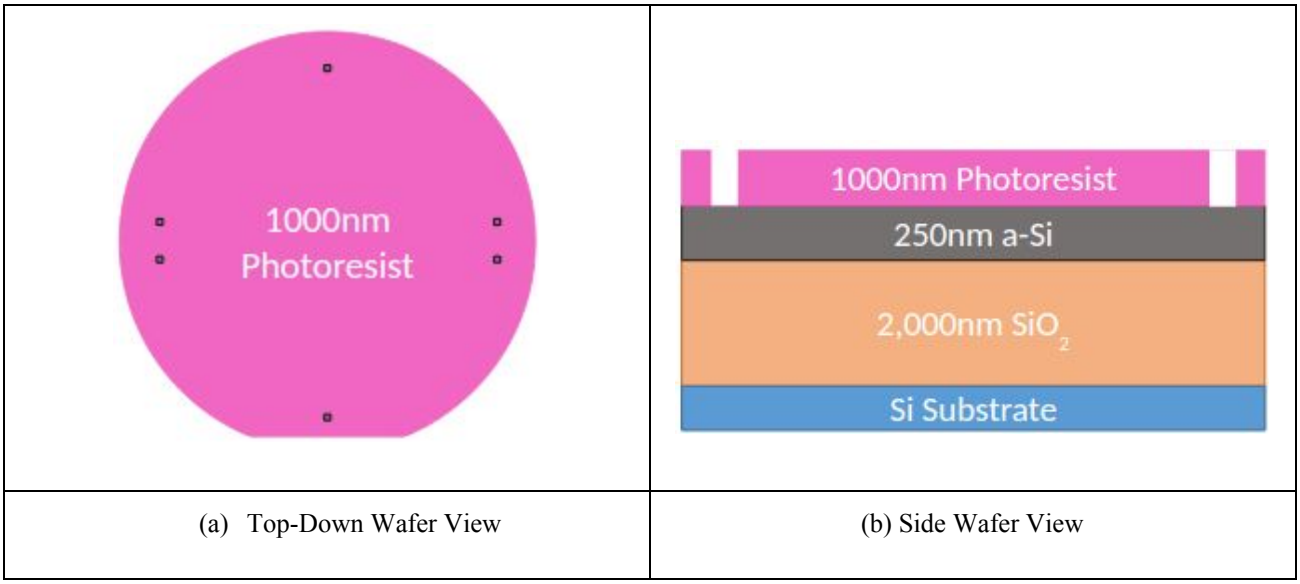


(a) Top-Down Wafer View | (b) Side Wafer View

Figure 18. Process views of the a-Si deposition. *Not to scale.*

While the SMFL is equipped to deposit a-Si using the plasma-enhanced chemical vapor deposition (PECVD) capabilities of Chamber B in the AME P5000, the tool is currently not configured correctly with hydrogen for this to be a safe option. Instead the wafers are taken to Corning, Inc. and 250nm of a-Si is deposited there.

3.3 Pattern a-Si with positive-tone resist for alignment marks



(a) Top-Down Wafer View | (b) Side Wafer View

Figure 19. Process views of the photoresist patterning for the alignment marks.*Not to scale.*

1. On the SSI track edit the NODISPEN recipe for a spin speed of 3400 rpm for 60 seconds, corresponding to an OiR-620 resist thickness of 1000 nm.

2. Verify the resist thickness on the Nanospec.
3. Run the wafers through the SSI coat track and hand-dispense the OiR-620.
4. Load the PREBLEJAN14 mask into the ASML PAS 5500 stepper; it is inside the reticle box labeled SPECTRUM.
5. Expose the wafers on the ASML using LAYER 1 (MARK) of Patsy_Waveguide located in the /0Preble folder.
    - The job is preset with an exposure of 250mJ/cm^2 for each image.
6. Develop the wafers on the SSI develop track.
7. Verify that the lithography is good using an optical microscope prior to the next step.
8. Unload the PREBLEJAN14 mask from the ASML.

3.4 Etch alignment marks in the SMFL DryTek Quad Etcher

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<td>Pre-ash:
 
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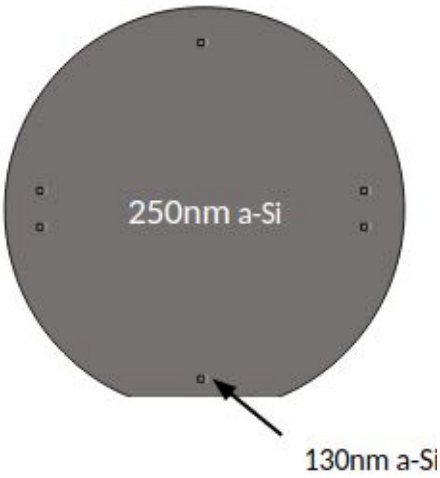
<td>Post-ash:
 
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<td>Post-ash:
 
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(a) Top-Down Wafer View	(b) Side Wafer View

Figure 20. Process views of the alignment mark etching pre- and post-ash. *Not to scale.*

1. The chamber which will be used does not have a required chamber preclean.
2. Verify that the recipe ZEROETCH on the DryTek Quad Etcher is set up with the following parameters:
    - 50 sccm CHF_3
    - 25 sccm CF_4
    - 10 sccm O_2
    - 200 W RF power
    - 100 mT pressure
    - 120 seconds
    - This will result in an etch of 120 nm +/- 20 nm of the alignment marks into the a-Si.
3. Run ZEROETCH.
4. Verify that the etch was successful through optical inspection.
5. Ash the wafers in the GaSonics Aura 1000 Asher.
    - Let them cool for 5 minutes after ashing.
6. Verify that the ash and etch were successful through optical inspection.

3.5 Pattern a-Si with negative resist for waveguide and ring pattern

(a) Top-Down Wafer View	(b) Side Wafer View

Figure 21. Process view of the device patterning. *Not to scale.*

1. Acquire the negative-tone resist nLOF-2020.
    - For this experiment this resist was diluted using PGMEA solvent for conservation purposes. The dilution was 3:5 PGMEA: nLOF. The coating parameters are thus only optimized for this dilution.

2. Create a recipe on the SCS coater with the following parameters:
    - 3200 rpm
    - 45 seconds
    - This will result in resist thicknesses of approximately 600 nm.
3. Hand-dispense the nLOF resist using a pipette and coat the wafer on the SCS coater.
4. Bake immediately after the coating for 1 minute at 110℃.
5. Verify the resist thickness on the Nanospec.
6. Load the PREBLEJAN14 mask into the ASML PAS 5500 stepper.
7. Expose the wafers on the ASML using LAYER 2 (WAVEGUIDE) of Patsy_Waveguide located in the /0Preble folder. Figure 22 below shows the resulting wafer map.
    - The job is preset with an exposure of 85 mJ/cm^2 for each image.

Figure 22. The "Test" cells correspond to test structures and the number cells ("600" etc) correspond to the spacing in nanometer between the ring and the waveguide at that location; "NO" means there is no offset between ring and waveguide. *Not to scale.*

8. Develop the wafers on the SSI develop track.
9. Verify that the lithography is good using an optical microscope prior to the next step.
    - Refer to Figure 23 for the top-down view of the expected sizing of each waveguide.

- The rings are expected to be 40µm in diameter and also 0.5µm in width.

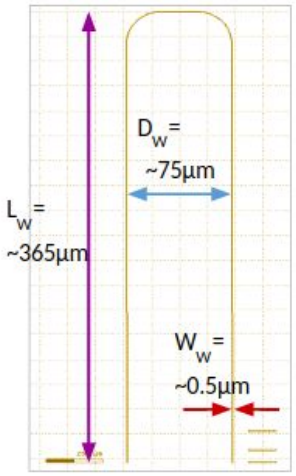
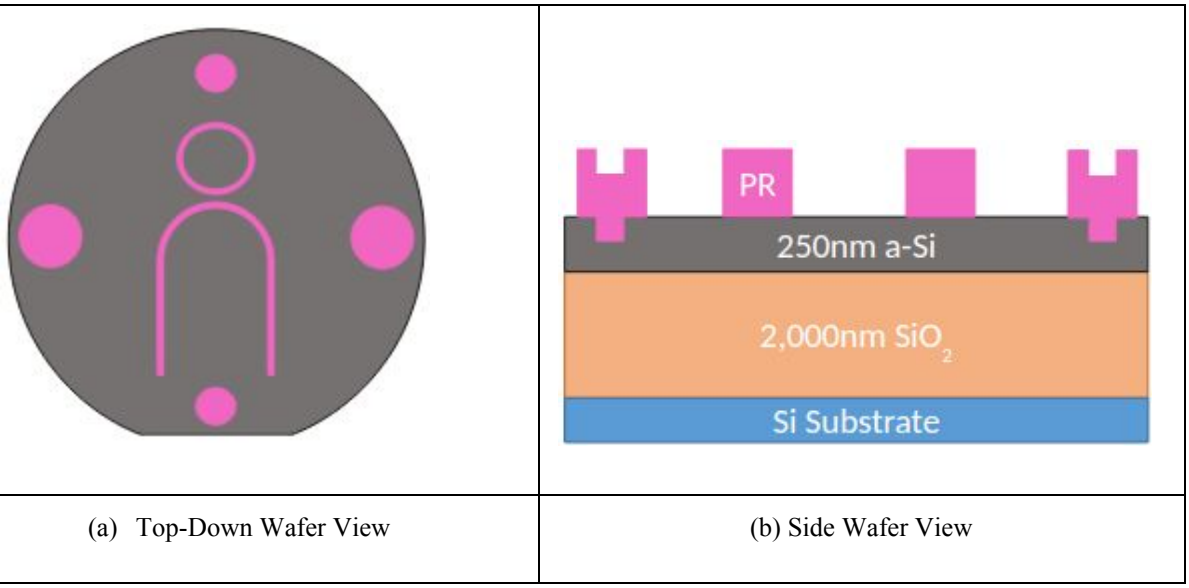


Figure 23. The expected sizing of each waveguide.

10. Unload the PREBLEJAN14 mask from the ASML.

3.6 Protect the alignment marks with positive-tone photoresist



(a) Top-Down Wafer View	(b) Side Wafer View

Figure 24. Process view of the alignment mark masking. *Not to scale.*

1. The alignment marks are only etched ~120nm deep into the a-Si. The next step in the process is to etch 250 nm of a-Si everywhere but on the devices, which includes through the alignment marks needed for the next lithography step. Thus, the alignment marks must be protected from the a-Si etching. In future processing, this protection will be added to LAYER 2 (WAVEGUIDE) of Patsy_Waveguide.

2. Fill a pipette with a very small amount of OiR-620 resist and place globs of resist over the alignment marks.

3. Bake the wafer for 1 minute at 140℃ to harden the resist.

3.7 Etch a-Si in the SMFL STS Deep Etcher

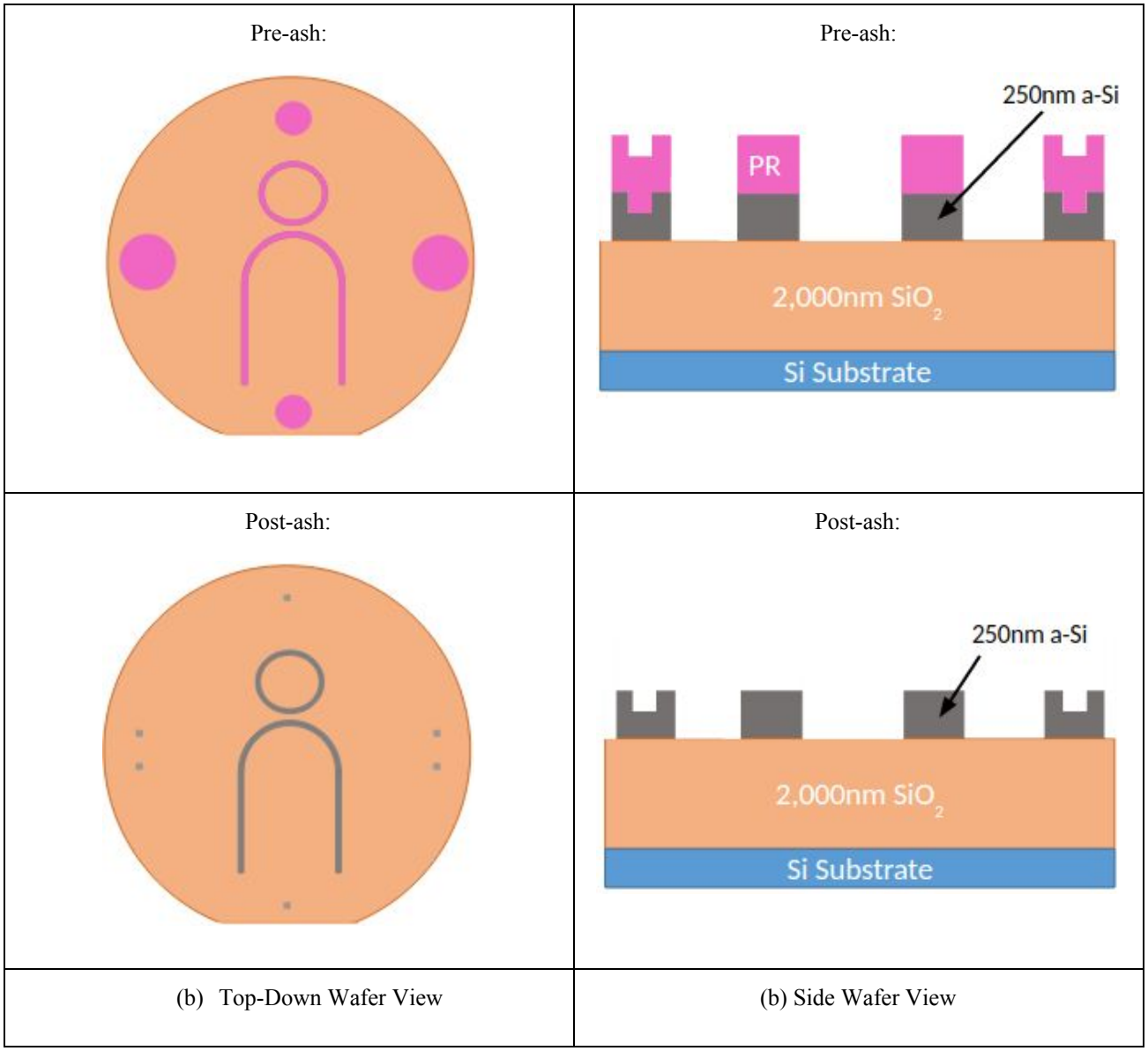
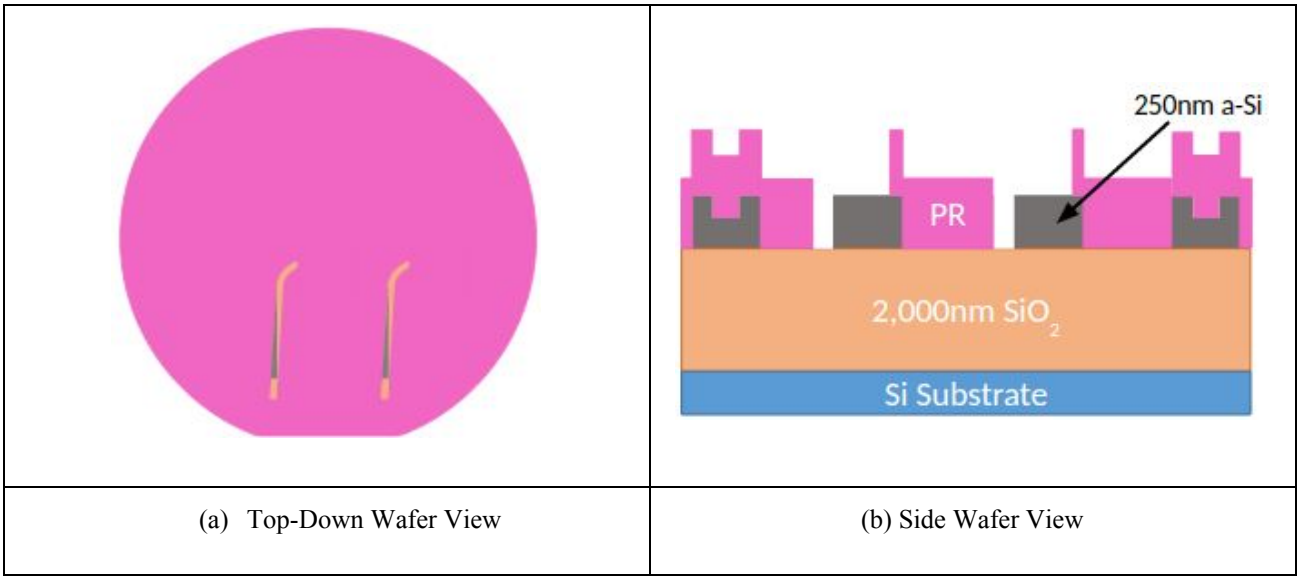


Figure 25. Process view of the waveguide and ring etching pre- and post-ash. *Not to scale.*

1. Etch the a-Si in the STS Deep Etcher using the following parameters:
    - 60 seconds
    - 20 W platen power
    - 700W coil power
    - 56 sccm C_4F_8
    - 10 sccm O_2
    - 40 sccm Ar
    - 24 sccm SF_6
    - Automatic Pre
    - For more details regarding this recipe and its parameters, contact Ankur Lamoria.

2. Verify that the etch has not gone through the photoresist by optical inspection.
3. Etch in the same process as before for 20 seconds.
4. Verify that the etch was successful through optical inspection.
5. Ash the wafers in the GaSonics Aura 1000 Asher.
    - Let them cool for 5 minutes after ashing.
6. Verify that the ash and etch were successful through optical inspection.
    - If there still appears to be scum or leftover resist on the waveguides after ashing, consider ashing again or using a solvent bath.

3.8 Pattern a-Si with positive-tone resist for waveguide taper etch



(a) Top-Down Wafer View | (b) Side Wafer View

Figure 26. Process view of taper cut patterning. *Not to scale.*

1. On the SSI track edit the NODISPEN recipe for a spin speed of 3400 rpm for 60 seconds, corresponding to an OiR-620 resist thickness of 1000 nm.
2. Verify the resist thickness on the Nanospec.
3. Run the wafers through the SSI coat track and hand-dispense the OiR-620.
4. Load the PREBLEJAN14 mask into the ASML PAS 5500 stepper; it is inside the reticle box labeled SPECTRUM.
5. Expose the wafers on the ASML using LAYER 3 (TAPER) of Patsy_Waveguide located in the /0Preble folder.
    - The job is preset with an exposure of 250mJ/cm^2 for each image.
6. Develop the wafers on the SSI develop track.
7. Verify that the lithography is good using an optical microscope prior to the next step.

8. Unload the PREBLEJAN14 mask from the ASML.

3..9 Etch a-Si in the SMFL STS Deep Etcher

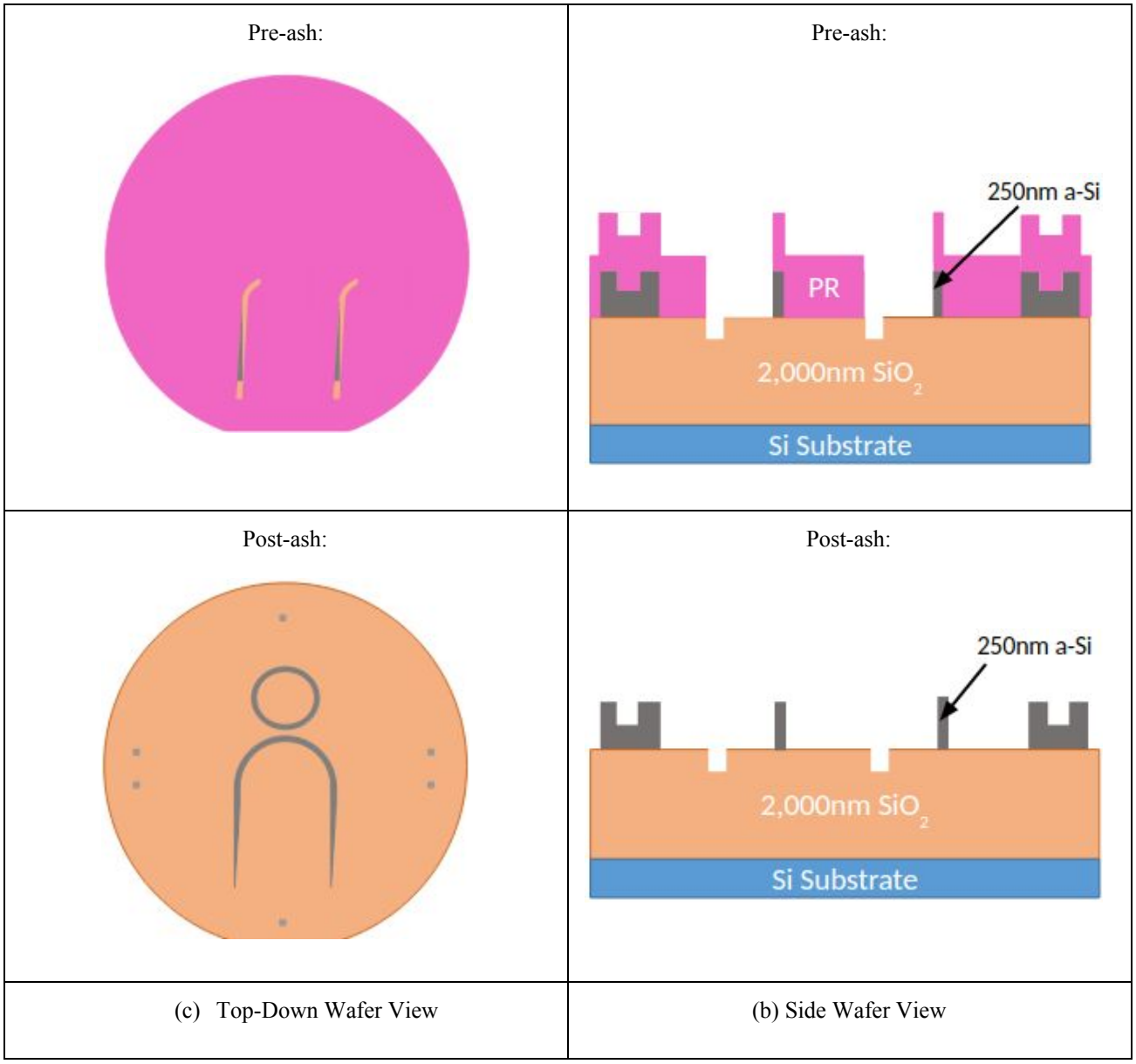


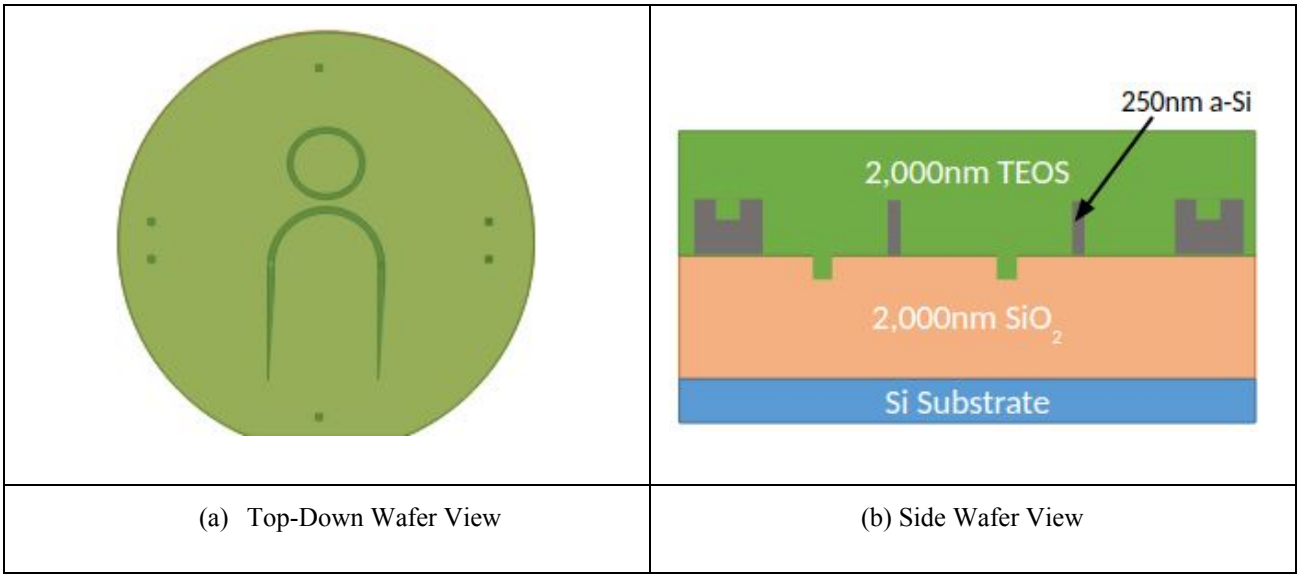
Figure 27. Process view of the waveguide and ring etching pre- and post-ash after the taper etch. Not to scale.

1. Etch the a-Si in the STS Deep Etcher using the following parameters:
    - 60 seconds
    - 20 W platen power
    - 700W coil power
    - 56 sccm C_4F_8
    - 10 sccm O_2
    - 40 sccm Ar
    - 24 sccm SF_6

- Automatic Pressure control
- For more details regarding this recipe and its parameters, contact Ankur Lamoria.

2. Verify that the etch has not gone through the photoresist by optical inspection.
3. Etch in the same process as before for 20 seconds.
4. Verify that the etch was successful through optical inspection.
5. Ash the wafers in the GaSonics Aura 1000 Asher.
    - Let them cool for 5 minutes after ashing.
6. Verify that the ash and etch were successful through optical inspection.
    - If there still appears to be scum or leftover resist on the waveguides after ashing, consider ashing again or using a solvent bath.

3.10 Deposit 2µm TEOS oxide in the SMFL P5000 for cladding



(a) Top-Down Wafer View | (b) Side Wafer View

Figure 28. Process view of the waveguide and ring after cladding. *Not to scale.*

1. Prepare chamber A of the P5000 for TEOS oxide deposition.
    - Wait three hours for the chamber lamps to heat up and stabilize for optimal deposition rate and film stress.
2. Once the lamps have been heated up and the wafer loaded, do a chamber oxygen clean.
3. Run recipe 1M_TEOS_LS on a dummy wafer to measure deposition rate.
4. Using the deposition rate determined, calculate the time required to deposit 1,000nm of TEOS oxide at a time using this recipe and edit the recipe's time accordingly.
5. Run another chamber oxygen clean.
6. Run recipe 1M_TEOS_LS on the wafer with the waveguides and deposit only 1,000nm of TEOS oxide at a

time.

7. Follow the 1,000nm TEOS oxide with an oxygen chamber clean.
8. Deposit the second 1,000nm of TEOS oxide using the same 1M_TEOS_LS recipe for a total of 2,000nm TEOS oxide cladding.
9. Visually inspect the wafer to ensure that the waveguides were not harmed in the cladding deposition.

3.11 Dice, polish and test the waveguides

Testing is performed by Jeffrey Steidle and Michael Fanto of the Nanophotonics Group at RIT and includes dicing the wafers as close to the tapered waveguide legs as possible and polishing evenly along the edge so that the oxide cladding will not peel off.

The source is an infrared laser of 1550 nm wavelength.

4. RESULTS AND DISCUSSION

4.1 Grow 2µm SiO_2 in Tube #1 of the SMFL Bruce Furnace

The recipe used was Recipe #410, with an edited time of 500 minutes. This was calculated using Dr. Lynn Fuller's Excel calculator to result in approximately 20,218 Å of oxide. Dr. Fuller edited and verified the recipe. Because hydrogen is not permitted to run in the SMFL after hours without a technician or process engineer present, Patricia Meller, a process engineer for the SMFL, stayed after hours and assisted with the shutdown of the tool once processing was complete.

The average oxide thickness across all 20 wafers, according to the collected Spectramap data, was 2.12µm.

4.2 Deposit 250 nm amorphous silicon at Corning

The deposition was successfully performed at Corning on 5 wafers. Measuring the a-Si thickness on the Nanospec, Spectramap and Ellipsometer, however, provided varying nonsensical results. Thus, a groove was made in one of the wafers and it was observed under the Laika microscope. Figure 29 is a picture taken of the groove.

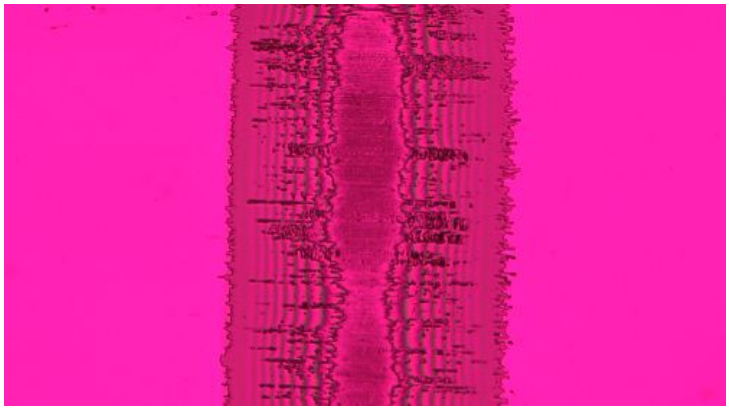


Figure 29. Picture of the middle of the groove in the a-Si.

From Figure 29, 9 fringes were counted from the surface to the silicon substrate and this did not correspond with the expected 250nm of a-Si and 2,000nm of oxide underneath. A wafer with only oxide was then step-etched to verify the oxide thickness; the thickness was confirmed to be approximately 2150 nm, as expected. For this reason, the groove

measurement was determined to be faulty and a set of profilometry readings were taken along the groove to measure the thickness of the a-Si and oxide total stack height. From this and the assumption that the oxide was approximately 2150 nm thick, the a-Si was calculated to be approximately 280 nm.

For future a-Si depositions at Corning Inc., a monitor with 100 nm oxide will be used to eliminate the need for direct measurement of a-Si thickness.

4.3 Alignment marks

The important thing to note about the alignment marks is that with the current process flow they are etched only 120nm +/-20 nm into the a-Si. This means that unless they are otherwise protected, they will be etched away in the STS Deep Etcher.

Another option might be to perform the alignment mark etching into the oxide instead of the a-Si.

4.4 nLOF-2020 resist

More work needs to be done determining the proper development time for the resist. Figure 30 below illustrates an instance where the resist was under-developed. Generally the SSI develop track was used and this gave consistently good results. However, when the SSI develop track was down and hand-developing had to be done in CD-26, the results were unexpected. The developer acted significantly faster during hand-developing than during the puddle develop of the SSI develop track but the cause as yet remains undetermined. Note that the merging of rings and waveguides, could also mean an instance of over-exposure. The optimal exposure was determined based on an FEM, but this might vary with resist dilution, etc. Another idea might be to use HMDS prime before the resist.

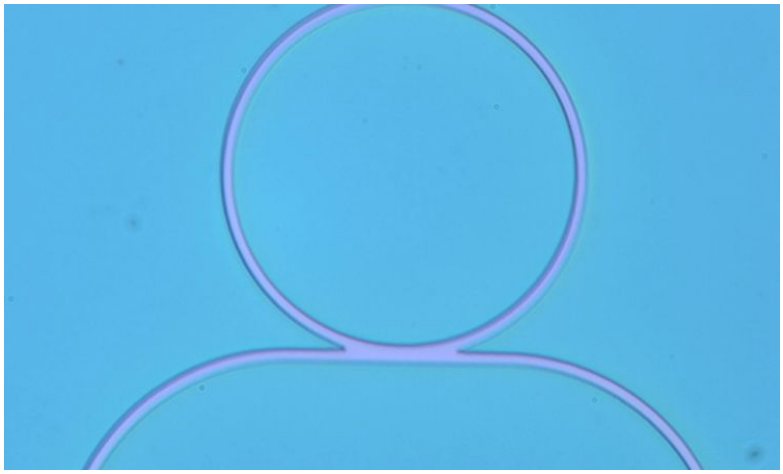


Figure 30. An example of under-development from hand-developing causing the ring and waveguide to merge.

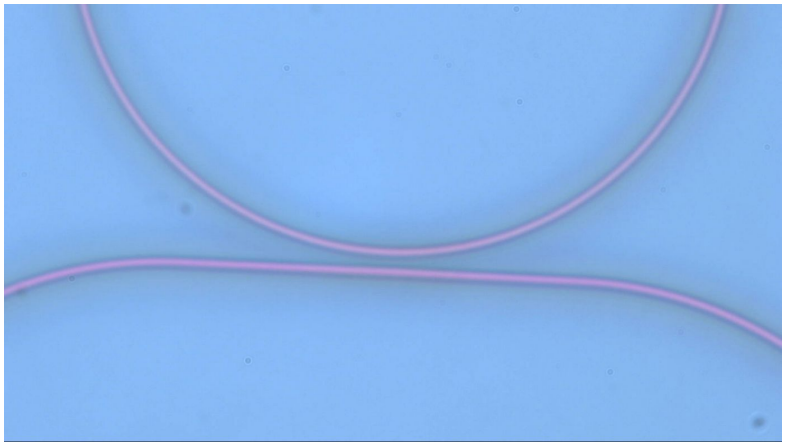


Figure 31. An example of good exposure and development from the SSI track where the ring and waveguide have not merged.

4.5 Writing the ASML matrix/ stepper job

The stepper job required for these waveguides is very different from what is standard in industry. The best way to describe it is that the features to be exposed are like separate building blocks on the mask which must be added together in the proper configuration to create a larger coherent structure on the wafer. To work with such a mask, the following steps must be taken:

1. Notice how the mask can be broken up into an x and y coordinate system and use this to define the mask cells.
2. Similarly, the cells must be defined for the wafer.
3. Define the first object by its location and its required blading size on the mask.
4. Define the instantiations of the objects on the wafer.
5. The stepper will go through each location on the wafer and expose each area separately.
6. Next, define the second object,
7. And define the instantiations of this object on the wafer.
    - Note that the object can be placed at different locations in the cell; this is how the waveguide-ring spacings were made to differ.
8. Once all these features and all other for intended exposure are exposed on the wafer, the stepper job will be finished.

This might seem counterintuitive when one can have a mask printed with the intended image already on the it and do a single-step exposure. And in many ways the process is incredibly cumbersome—for example, the same object cannot be defined multiple times in the same cell—but, this double-patterning process is necessary to resolve features smaller than what the ASML is capable of.

4.5 Etch a-Si in the SMFL STS Deep Etcher

After the lithography, a new shallow etch process was developed using the STS Deep Etcher tool. The tool is designed to etch anywhere from 1µm to hundreds of micrometers of silicon; by those standards, the 250 nm of a-Si that is meant to be etched for the creation of the waveguides is *not* deep. Thus, a single silicon etch cycle is used instead of the usual Bosch process. This can make the run very chaotic, as tuning must be done constantly until the process is terminated.

This part of the project was carried out by Ankur Lamoria, a graduate student in the Microelectronic Engineering program at RIT, with the help of Patricia Meller. The eventual goal is to develop a 100 nm per minute etch that is uniform and can generally tune itself automatically; at the time this paper was authored, this was still in development.

The etch rate was unknown at the time of the first etching, but was determined to be approximately 1.75nm per second. Based on this etch rate, two etching schemes were tried: one for an over-etch and the other for an under-etch of the a-Si.

Figure 32 is a picture of the over-etched waveguide; the etch time for the wafer was 180 seconds. This corresponds to the side wafer view in Figure 34 labeled “Over-etched.”

Figure 33 is a picture of the under-etched waveguide; the etch time for the wafer was 80 seconds. This corresponds to the side wafer view in Figure 34 labeled “Under-etched.”

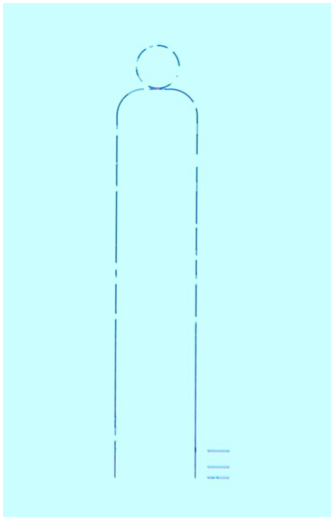


Figure 32. Waveguide etched for 180 seconds.

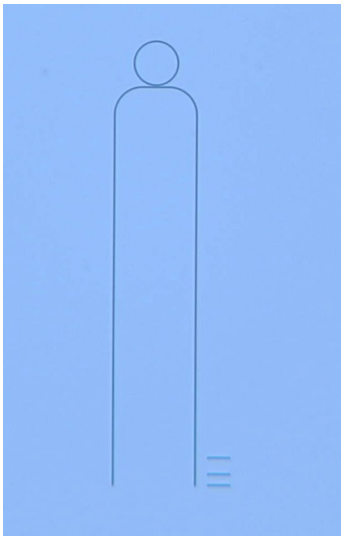
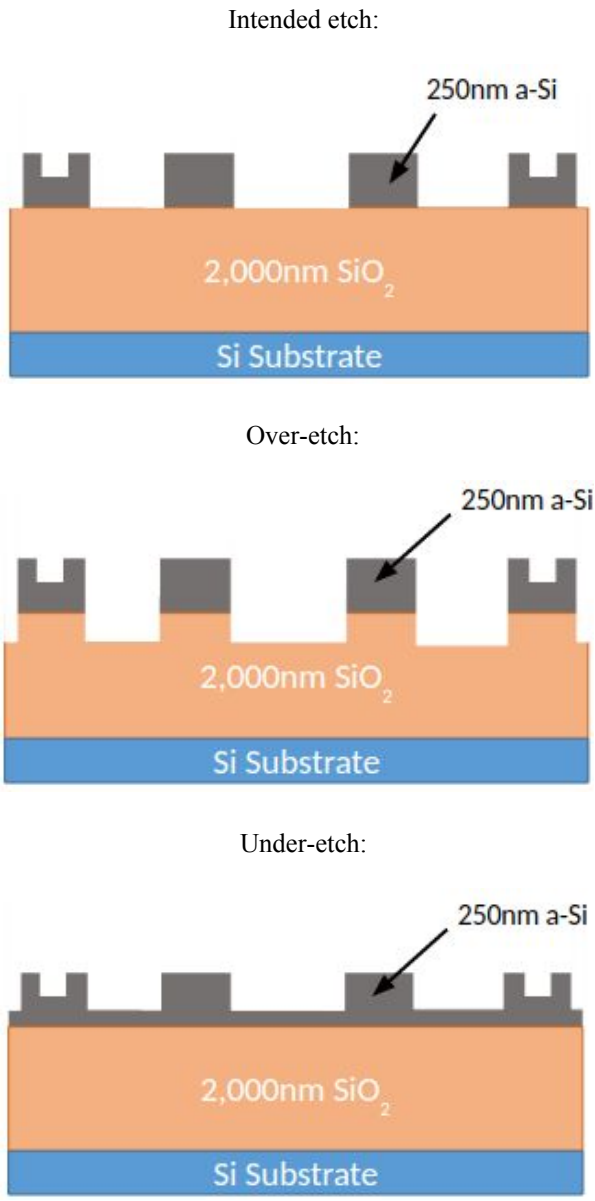


Figure 33. Waveguide etched for 80 seconds.



(d) Top-Down Wafer View

(b) Side Wafer View

Figure 34. Results of various etching schemes. *Not to scale.*

The risk with under-etching is that transmission will be very poor and coupling near-impossible because of the lack of isolation. The risk with over-etching is that the sidewalls will collapse, as clearly happened in Figure 32, as a result of the etchants going through the approximately 600 nm thick layer of photoresist. For more etching details, please refer to Ankur Lamoria.

4.6 Ashing

Scumming was seen after ashing on both wafers. Solutions include either another ashing or using a solvent bath to get rid of the hardened negative resist.

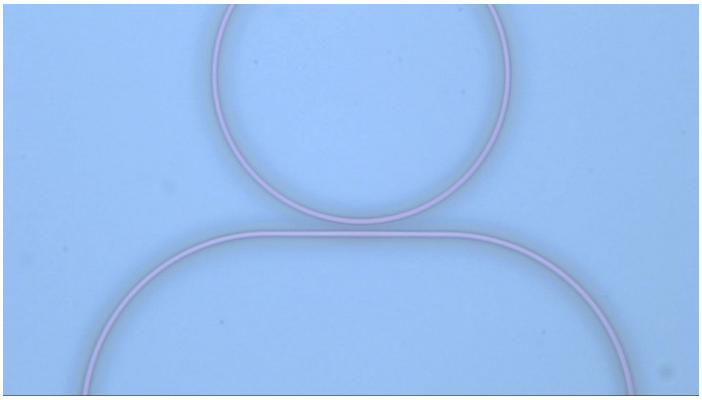


Figure 35. Post-etch and pre-ash.

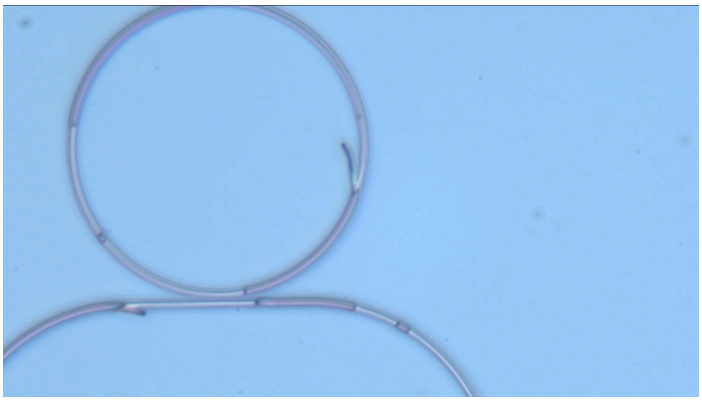


Figure 36. Post-ash with some photoresist still present on the waveguide.

4.7 Taper etch

The taper etch appeared to be successful based on visual inspection. Because the waveguide ends are supposed to be approximately 100 nm wide after the etch, it is hard to determine whether or not this is so with only an optical microscope incapable of directly measuring that small. That being said, both Figures 37 and 38 show the ends of the waveguides getting smaller the further down the waveguide they are, which seems to indicate the success of the taper etch.

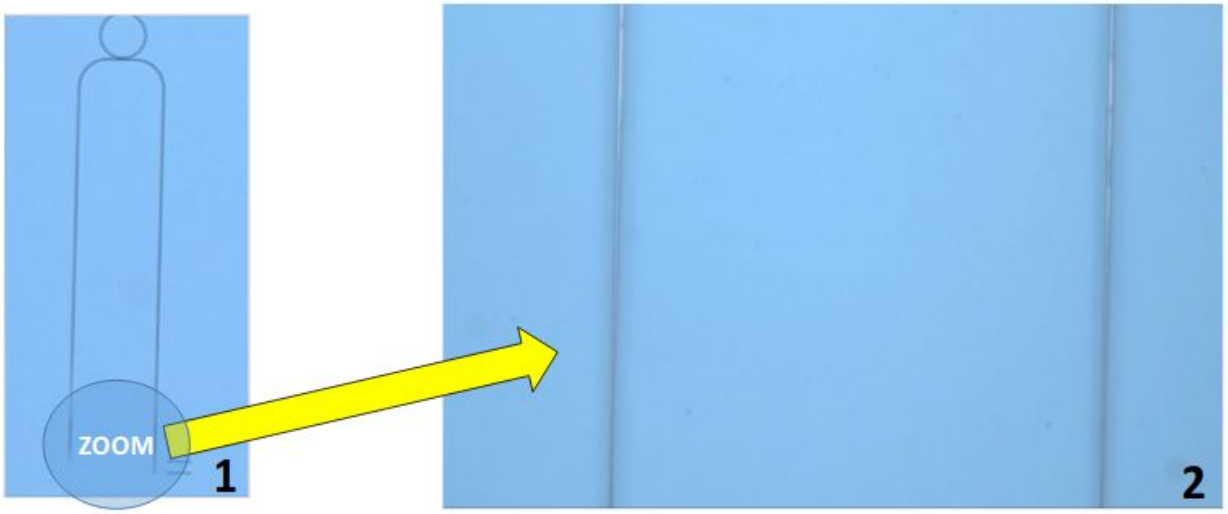


Figure 37. Tapered waveguide ends.

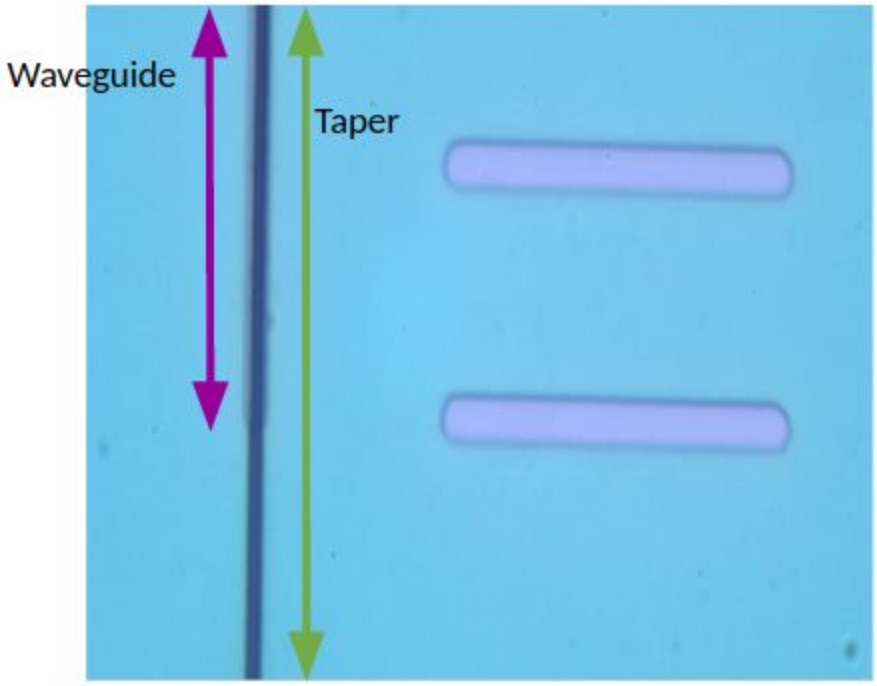


Figure 38. The waveguide and taper can be seen on top of each other in this picture.

4.8 Cladding

More work must be done to determine the best cladding for this material; stress is a huge issue here and the lowest stress films must be realized for successful and easy polishing. Figures 39 and 40 are included to show that the cladding deposited was clear and did not disturb previously-existing waveguides.

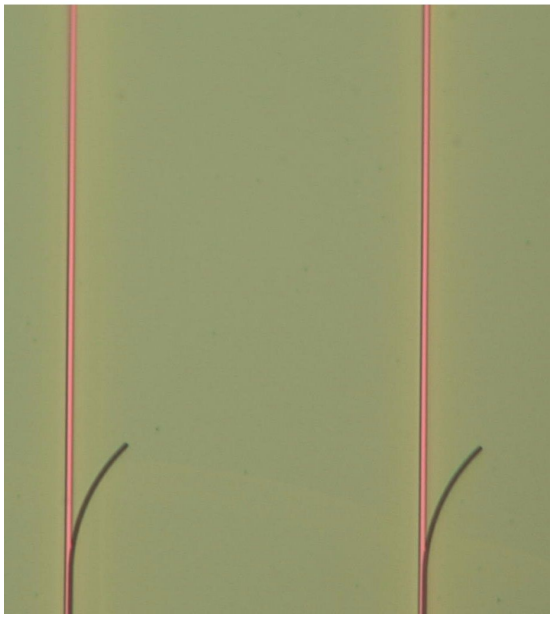


Figure 39. The top part of the waveguide-taper intersection after the TEOS oxide cladding deposition.

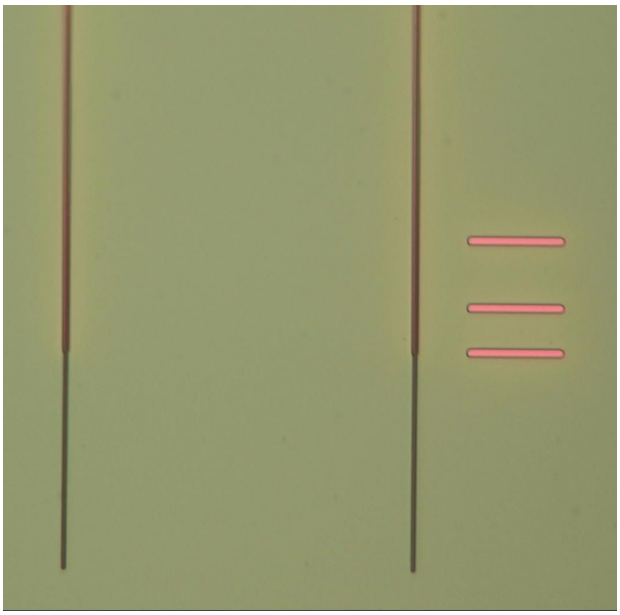


Figure 40. The bottom part of the waveguide-taper intersection after the TEOS oxide cladding deposition.

4.9 Testing

Testing and all of the sample preparation post-cladding was performed by Jeffrey Steidle and Michael Fanto of the Nanophotonics Group at RIT. The source used was an infrared laser of 1550 nm wavelength and the results are below.

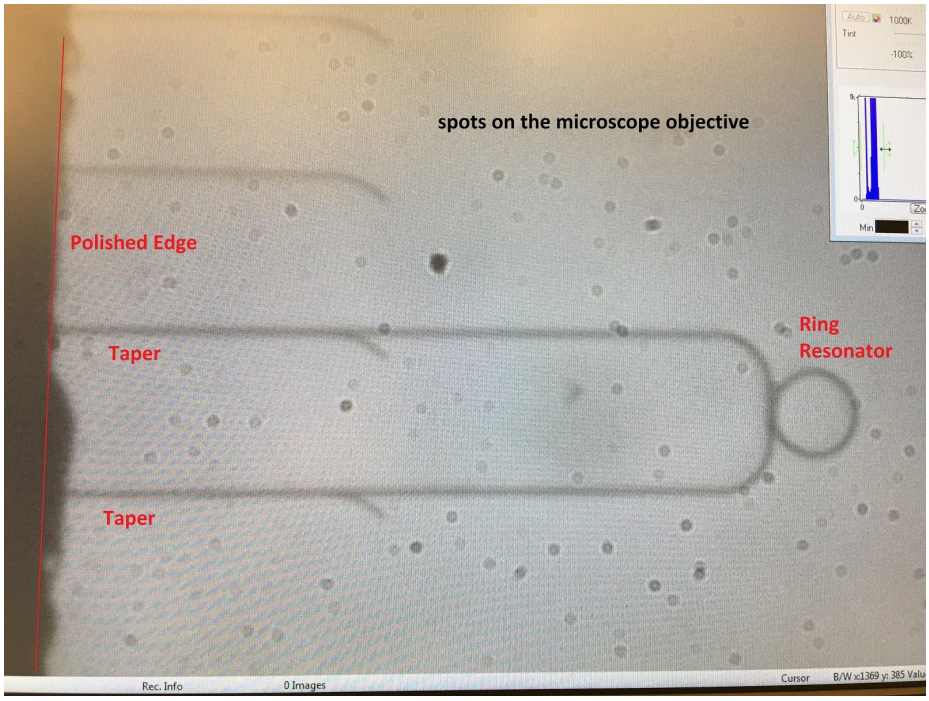


Figure 41. Picture of a diced and polished waveguide and ring awaiting testing taken on an optical microscope.

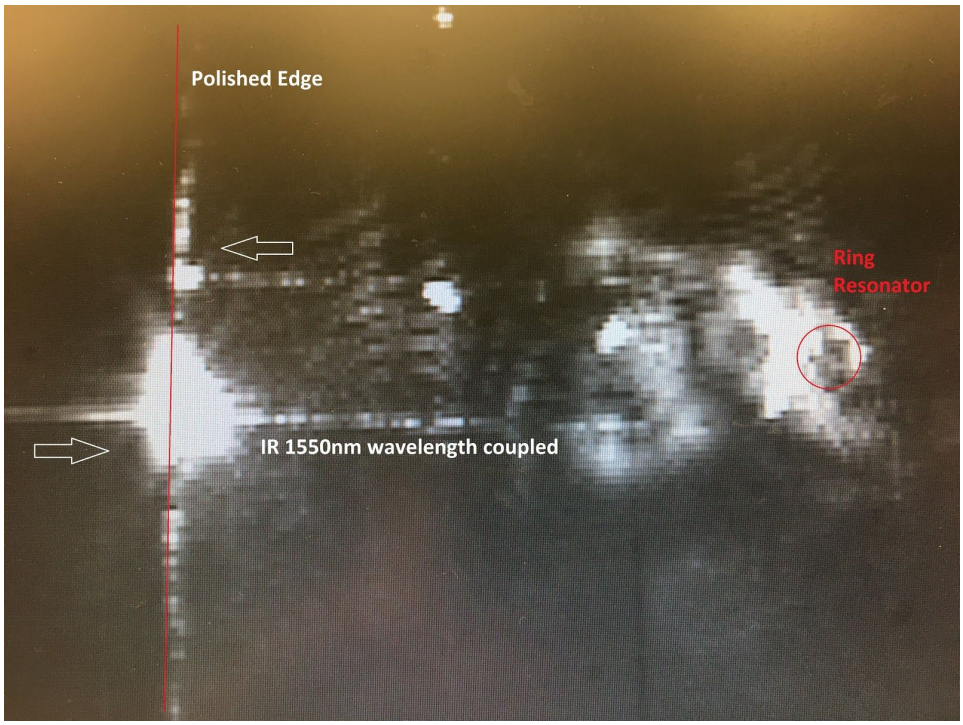


Figure 42. Infrared picture of the same waveguide and ring as in Figure 41, except this time with 1550 nm wavelength light being sent through it. Though the picture isn't the best quality, it can be observed that coupling (that is, light going into the ring from the waveguide) is occurring.

The results shown in Figure 42 serve to classify this project as an overall success.

4.10 SEM pictures

SEM pictures of a waveguide were taken by Sean O'Brien.

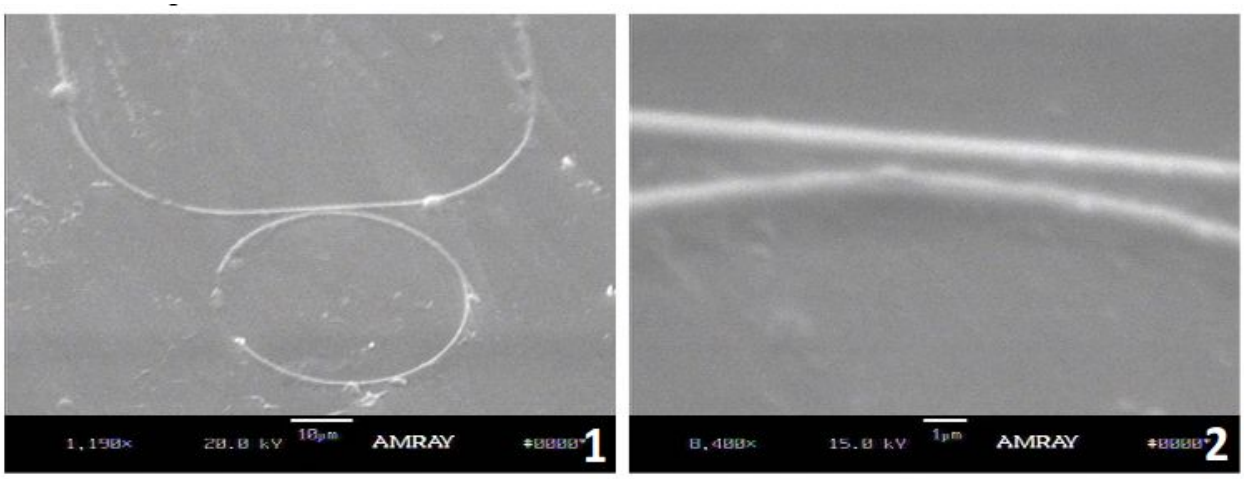


Figure 43. These SEM pictures show that the gap between the ring and the waveguide is in fact present.

5. CONCLUSION

A process for realizing a-Si waveguides on oxide with oxide cladding was developed to be run in the RIT SMFL. Because the process only takes one week to fabricate, it would be easy to implement this into a future short course designed around fabricating and testing waveguides. The finished waveguides demonstrated coupling during testing; there is a chance some will show resonance as well but testing is slow. Overall, however, even with no resonance shown, the project was a success. Future work must be done especially to further characterize the a-Si etch process in the STS Deep Etcher.

ACKNOWLEDGEMENTS

My advisors, Drs. Preble, Pearson and Ewbank, for their guidance. Patricia Meller, Sean O'Brien and the rest of the SMFL staff for all their processing help and knowledge. Dr. Fuller for the steam oxide growth recipe. Dr. Hirschman and Corning Inc. for the a-Si deposition. Frank Byrne and Orthogonal Inc. for providing the negative-tone resist. Stephanie Bolster for assistance with the ASML stepper. Ankur Lamoria for developing the etching recipe used.Corey Shay and Eric Evangelou for miscellaneous processing help. And Michael Fanto and Jeffrey Steidle of the RIT Integrated Photonics Group for testing the devices.

REFERENCES

[1] Fuller, L., "Bruce Furnace Recipes," RIT, 18 May 2016, <https://people.rit.edu/~lffeee/Bruce_Furnace.pdf> (5 July 2014).