Ferroelectric HfO_2 Thin Films for FeFET Memory Devices

Joseph F. McGlone

***Abstract*—Silicon-doped hafnium oxide has been shown to exhibit ferroelectric properties under the certain small thicknesses with appropriate applied stress and annealing conditions. Utilizing Si:HfO_2 as the dielectric with a TiN capping layer in a ferroelectric field-effect-transistor (FeFET) is promising as a potential emerging memory device due to the ease in integration with standard CMOS process flows. The process developed at RIT was successful in fabricating n-channel FeFETs of varying dimensions. The work done here utilizes a 10 nm thick ALD Si:HfO_2 film that has a remnant polarization of 10.34 $\mu C/cm^2$ and an average memory window of 572.3 mV. The subthreshold characteristics were consistent in both the on and off state with a calculated subthreshold swing around 110 mV/dec.**

***Keywords*—Ferroelectric Memory, Hafnium Dioxide, FeFET.**

I. Introduction

BIG Data and data analytics are essential and growing sectors in modern day technology. Millions of users and companies are creating massive amounts of data from personal devices, health trackers, medical sensors, and environmental sensors. The use and correct analysis of this data can have numerous benefits to society, including uncovering important medical trends to help diagnose patients quickly and accurately. With all of this increased data generation comes the need for more storage space; increasing storage space requires more power, which ultimately has a negative effect on the environment. To compensate for these challenges, non-volatile memory devices are being widely studied to evaluate high-density and low-power opportunities in system memory hierarchy for superior system performance.

One promising non-volatile memory device is a ferroelectric field effect transistor (FeFET). A FeFET stores memory through the remnant polarization state of the ferroelectric film in the gate stack, causing shifts in the threshold voltage of the device. This change in threshold voltage is interpreted as different storage values. FeFETs have advantages such as a simple one-transistor (1T) memory cell design with a read and write latency in the nanosecond range [1]. Typical ferroelectric memory devices use lead-based films, but lead-free ferroelectric thin film device design is a growing field and a strong contender in emerging memory technology.

A lead-free option is silicon-doped hafnium oxide (Si:HfO_2) ferroelectric films which have been demonstrated to show excellent potential as a competitive memory technology [2]. Since HfO_2 has already been adopted as a high-k gate dielectric material for state-of-the-art devices currently in mass production, hafnium-based ferroelectric films can be easily integrated into a standard CMOS process flow. In addition to the ease of integration, Si:HfO_2 has higher coercive fields which allows for further scaling of the gate stack compared to conventional ferroelectrics such as strontium bismuth tantalate (SBT) or lead zirconate titanate (PZT).

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II. Theory

A. Ferroelectric Hafnium Dioxide

Ferroelectricity is a material property where the material has the ability to have spontaneous polarization. There are two discrete stable or metastable polarization states in the absence of an applied electric field, and this polarization can be influenced by the the application of an external electric field [3]. The amount of polarization charge in these two states is called the remnant polarization, P_r. The remnant polarization is the property that allows the FeFET to store data via the two polarization states. The device functions as a non-volatile memory device since the lack of an applied electric field does not change the state of the ferroelectric layer in the gate stack.

The ability to use an HfO_2 based film for a ferroelectric layer is hugely beneficial for integration into standard CMOS due to the maturity of HfO_2 as a high-k dielectric in modern process technology. Hafnium oxide has standard bulk and thin film crystalline phases which do not have ferroelectric properties because the structure is centrosymmetric. However, during cooling, thin layers of cation doped HfO_2 under physical stress from a capping layer have been shown to have ferroelectric properties in the resulting orthorhombic non-centrosymmetric crystalline phase [4]. Fig. 1 shows the crystalline transitions required to form ferroelectric hafnium oxide. Since the annealing conditions are critical to inducing the ferroelectric phase, processing once the HfO_2 has been annealed should be kept to a low thermal budget. NaMLab in Dresden, Germany provided the atomic layer deposited (ALD) Si:HfO_2 film, TiN capping layer, and anneal process for this work.

B. FeFET Device and Operation

A FeFET device can be used as a memory device since the polarization state of the ferroelectric film is stored and retains the state after power is removed. The use of the ferroelectric film as the dielectric reduces the complexity of the storage scheme to a 1T design. This reduces the area of the storage cell from the current FeRAM design with an access transistor and a ferroelectric capacitor (1T-1C design). The compatibility with CMOS processing from hafnium based films also reduces the

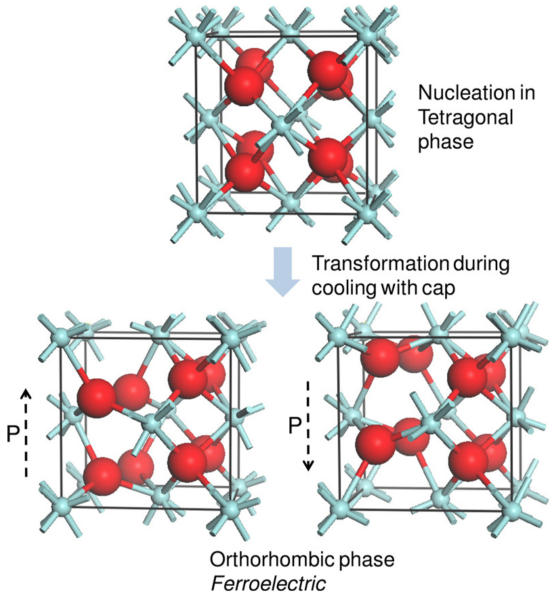

Fig. 1. Shows the tetragonal phase under cooling with a stressing capping layer influences the hafnium oxide crystalline structure toward the orthorhombic phase which is non-centrosymmetric. The two bottom structures show the to stable polarization states.[4]

routing of cells due to isolation of the historical ferroelectric materials from the transistors.

The theoretical maximum memory window is shown in 2. This shows the main scalabiltiy challenge of ferroelectric materials that do not have high coercive fields since a sufficient memory window would require a thicker ferroelectric layer.

$$Memory\ Window = V_{T,OFF} - V_{T,ON} \tag{1}$$

$$MW_{max} = 2E_c \times t_{FE} \tag{2}$$

$$V_c = E_c \times t_{FE} \tag{3}$$

The curve needed to characterize ferroelectric films is the P-V curve shown in Fig. 2. The two labeled points are the remnant polarization, P_r, and the coercive voltage, V_c. The remnant polarization is required for a shift in the apparent threshold voltage seen by the transistor. This polarization charge can shift the threshold voltage higher or lower based on the direction of the polarization vector.

The ON-state, seen in Fig. 3, shows the direction of the polarization vector as pointing toward the substrate inducing the accumulation of electrons to create a conductive channel, in effect, lowering the threshold voltage. The opposite effect is observed when the polarization is in the complementary OFF-state as seen in Fig. 4. In the OFF-state, the polarization vector is pointed away from the substrate and further depletes the electrons in the channel, in effect, increasing the threshold voltage.

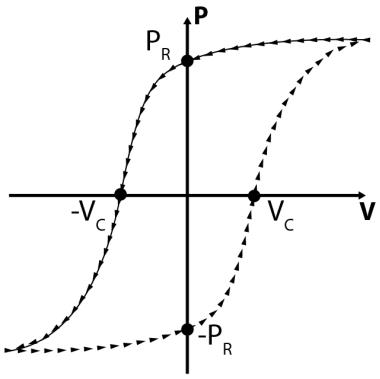

Fig. 2. An example of a ferroelectric polarization vs. voltage curve. The labeled parameters are the remnant polarization and the coercive voltage.

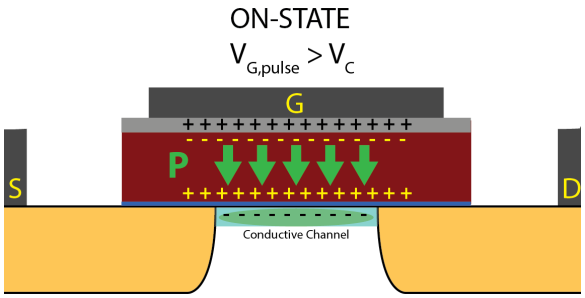

Fig. 3. Example of FeFET in the on-state with a conductive channel induced by the polarization of the ferroelectric film.

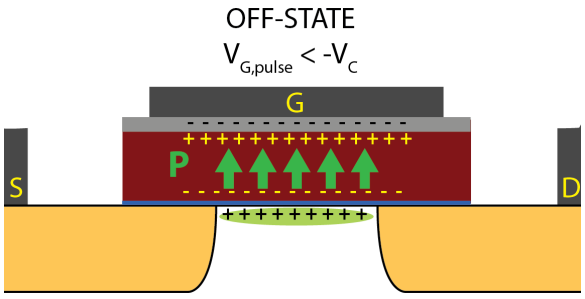

Fig. 4. Example of FeFET in the off-state without a conductive channel induced by the polarization of the ferroelectric film.

III. Experimental Details

A. Mask Design

A full custom mask design was created using four masking levels: active, S/D implant, gate dielectric, and metal. The design consists of an array of FeFETs with varying dimensions, MOS capacitors, TLMs, CBKRs, Van Der Pauw's structures, resolution marks, and alignment marks. This collection of devices and test structures covers a large range of device characteristics from channel length effects to contact resistance measurements.

The capacitor design was done with two designs for the same effective capacitance. Initially, large measurable capaci-

tors were added for a strong signal to noise ratio with parasitic capacitances from wiring but the large capacitor layout has a greater probability of pin holes in the dielectric layer causing shorts. Due to this potential effect, many smaller capacitors were connected in parallel to achieve the same large effective capacitance, but reducing the size reduces the chance that the device will cover a region of the film that has minor defects.

The processing capabilities of the RIT Semiconductor Fabrication Lab (SMFL) are not at the point where state-of-the-art dimensions can be achieved, therefore the mask designs were done to ensure a properly functioning device that has the best chance of demonstrating a memory behavior. The ferroelectric layer must be deposited and annealed after all high temperature steps are completed which rules out a self-aligned process flow. Without having a self-aligned process, larger overlays were incorporated into the mask design to ensure that the gate dielectric and electrode fully covered the channel region. This design will have increased overlap capacitances and slower operation in exchange for a robust process.

B. Process Design

Since this is designed as a two semester project, the process design utilized as many mature RIT sub-CMOS process steps as possible. The active area formation was done using the predetermined LOCOS isolation flow. All implant steps were simulated using SILVACO Athena to ensure the correct profile was achieved after annealing. The channel-stop and source/drain regions were done as done in the standard CMOS flow. The initial design was to forgo a P-well implant but this design would have led to source/drain depletion regions on the order of a few microns leading to severely reduced channel lengths and creating channel shorts at small dimensions. At this discovery, a P-well implant was designed for the substrate doping. A retrograde profile was targeted to reduce the annealing time required as well as reducing the possibility of punch through in the smaller channel devices.

Due to the use of NaMLab's ALD deposition and anneal process, the ferroelectric Si:HfO_2 would be deposited and annealed before it can be pattered. If the film is exposed to temperatures above 550-650 C, the film may be induced back to one of the more stable centrosymmetric phases. This thermal constraint led to a non-self-aligned process, no ability to use a silicide S/D region, and no inter-level-dielectric to reduce charges from low-temperature oxides.

At the time that the project was proposed, there was no reliable etch process at RIT for etching HfO_2, so one of the main challenges to completing this process flow is the ability to design a reactive ion etching recipe using the LAM 4600 and chlorine based gases to etch the ALD Si:HfO_2 film. It has been shown that BCl_n species react with HfO_2, which under ion impact, form volatile etch products such as B_mOCl_n and $HfCl_n$ [5].

IV. Results and Discussion

A. Si:HfO_2 Etching

An etching recipe was created using the same gas ratios as seen in [6] in order to get an acceptable etch rate for the ALD Si:HfO_2 layer. The recipe used is shown in Table I. Since the layer is only approximately 10 nm thick, the etch rate did not need to be that fast for the purpose of this project. There was concern that prolonged time under the plasma would increase the temperature on the wafer to induce photoresist hardening. A difficult to remove resist would be troublesome since the TiN capping layer will oxidize if exposed to an oxygen plasma, therefore ashing is not an option to remove resist. To reduce the possibility of photoresist hardening the wafer was cycled through the tool in 60 second increments and measured after each cycle using the Film Sense FS-1. The device wafers were also processed with the cycling.

TABLE I. Etch recipe used in LAM 4600.

Step	1	2	3
Pressure	120	120	0
RF Top [W]	0	0	0
RF Bottom	0	150	0
Gap [cm]	3.0	3.0	5.3
O2 (111)	0	0	0
N2 (222)	20	20	50
BCl (333)	21	21	0
Cl2 (444)	11	11	0
Ar (555)	84	84	0
CFORM (666)	0	0	0
Complete	Stabl	Time	Time
Time [s]	15	60	15

TABLE II. Data from etching Si:HfO_2 using LAM 4600.

Step Etch Time [sec]	Thickness [nm]	Etch Rate [nm/min]
Initial	9.737	
60.0	4.337	5.401
60.0	2.006	2.330
60.0	0.027	1.979

The etch rate results, shown in Table II, indicate the Si:HfO_2 is actually getting etched with an initial etch rate of about 5.5 nm/min. There is a steady decrease in the etch rate after the initial etching recipe, which is mostly likely due to chlorine corrosion or contamination after being exposed to chlorine and then ambient. The proposed changes to the recipe in Table III are designed to allow the wafer to cool to reduce photoresist hardening, but also keep the wafer under vacuum to avoid contaminants. The cooling step could also be removed completely since the aluminum etch is around 5 minutes and the photoresist was able to be removed with a solvent strip in the PRS-2000. This would need to be tested since the aluminum recipe is different and may have different effects with photoresist.

B. Ferroelectric Capacitor Verification

During the time of the gate stack deposition with a target of 10.0 nm Si:HfO_2 annealed at 1000 C for 1.0 second, NaMLab also deposited the exact same film composition on reference devices that had a metal-ferroelectric-metal film stack. The reference devices were patterned and tested by NaMLab and the results were compared with the RIT fabricated metal-

TABLE III. ETCH RECIPE PROPOSED TO IMPROVE PROCESS IN LAM 4600 THROUGH DELAY IN VACUUM.

Step	1	2	3	4	5
Pressure	120	120	120	120	0
RF Top [W]	0	0	0	0	0
RF Bottom	0	150	0	150	0
Gap [cm]	3.0	3.0	3.0	3.0	5.3
O2 (111)	0	0	0	0	0
N2 (222)	20	20	50	20	50
BCl (333)	21	21	0	21	0
Cl2 (444)	11	11	0	11	0
Ar (555)	84	84	0	84	0
CFORM (666)	0	0	0	0	0
Complete	Stabl	Time	Time	Time	Time
Time [s]	15	75	60	75	15

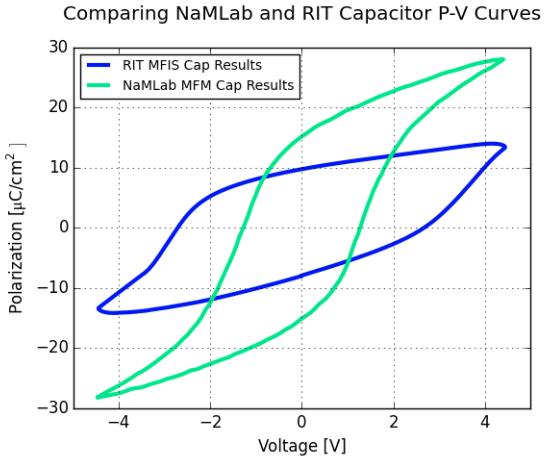

Fig. 5. Comparison between the NaMLab MFM capacitor and the RIT processed MFIS (N+ Si) capacitor. The MFM capacitor has a P_r of $\pm 15.2 \mu C/cm^2$ with a V_c of $\pm 1.2V$. The MFIS capacitor has a P_r of $\pm 9.4 \mu C/cm^2$ with a V_c of $\pm 2.6V$.

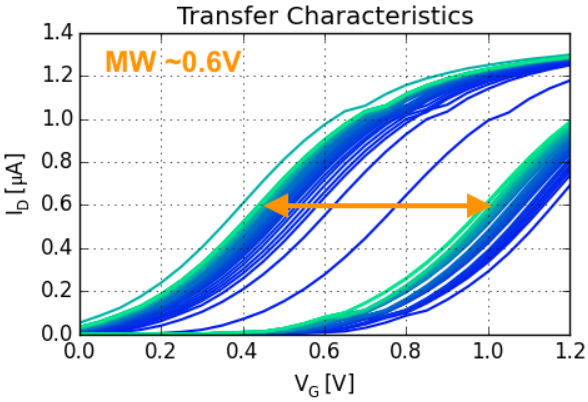

Fig. 6. Linear scale transfer characteristic curve for a L = 5 μm and W = 15 μm. This shows the ON-state which are the curves on the left side, and the OFF-state which are the curves on the right side.

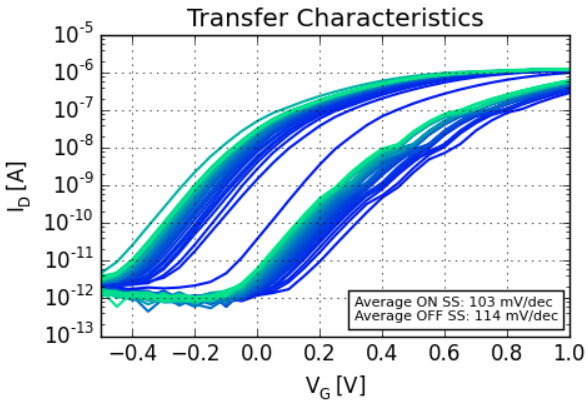

Fig. 7. Log scale transfer characteristic curve for a L = 5 μm and W = 15 μm. This shows the ON-state which are the curves on the left side, and the OFF-state which are the curves on the right side.

ferroelectric-insulator-silicon (n+ doping) or MFIS capacitor with the same annealing conditions.

The polarization vs. voltage curves created using the aixACCT TF1000 FE Tester and shown in Fig. 5, confirm that the RIT processed device exhibits ferroelectric behavior. There is degradation in the curve compared to the reference device due to many reasons. The film stacks are different between the two devices, and the influence of an interfacial oxide in the MFIS stack contributes a linear stretching of the curve due to a series non-ferroelectric capacitance. Other differences in the curve can be attributed to the process variation, potential plasma damage during gate patterning, and parasitics in the final device.

C. FeFET Electrical Testing

To test the functionality of the FeFET devices, the HP 4145 Parameter Analyzer was used to generate the stimuli through the use of the RIT 12 pad probe card. A cycle consists of a gate bias pulse of 4.5 V for 10 ms, a transfer curve sweep, a gate bias pulse of -4.5 V for 10 ms, and another transfer curve. The large pulses on the gate, with the source and drain biased at 0.0 V, are used to change the state of the ferroelectric since the voltage is larger in magnitude than the coercive voltage. The transfer curves were swept to a voltage lower than V_C so as to not change the ferroelectric polarization.

The ferroelectric film needs to be cycled from its initial state. The cycling helps to allow the ferroelectric domains to move more freely and fully switch from the applied field. In the transfer characteristic plots and the current ratio, the dark blue curves are the initial cycles and as the number of cycles increases from 0 to 50, the color becomes more green.

The transfer characteristics in Fig. 6 show a memory window of about 0.6 V using the change in extracted threshold voltage. The curve starts to roll off at higher V_G which is an indication that there is not a perfectly ohmic contact between the source and drain diffusion regions and the metal electrodes. This was most likely result of the missed HF dip before the

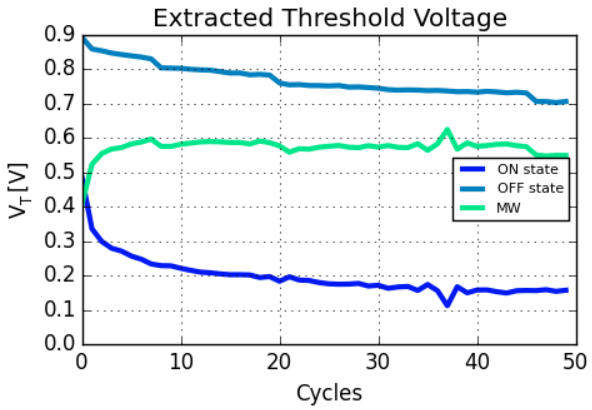

Fig. 8. Threshold voltage change between the ON and OFF state for a L = 5 μm and W = 15 μm. This shows a memory window, or change in V_T to be 0.6 V.

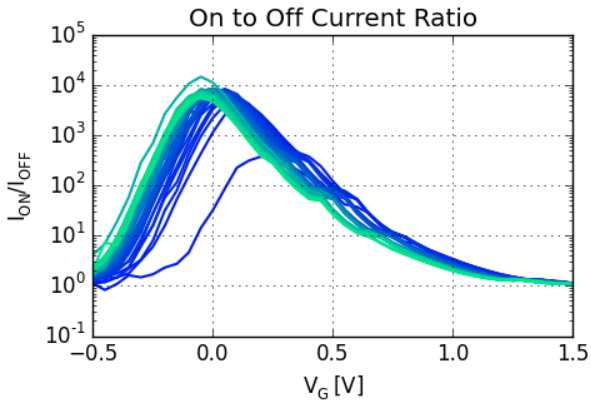

Fig. 9. The ON to OFF current ratio is plotted vs. gate voltage to get an idea of the optimal read voltage. This device is a L = 5 μm and W = 15 μm.

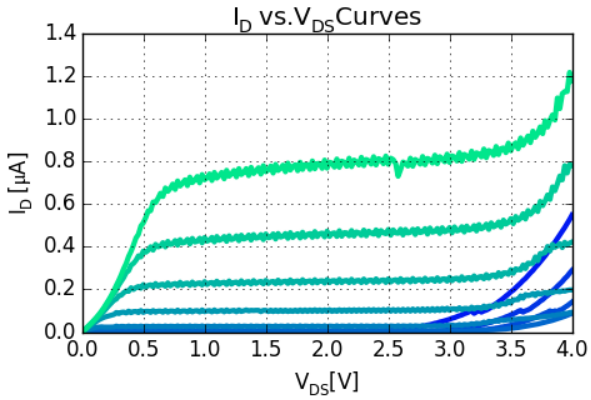

Fig. 10. The I_D vs. V_{DS} curves of a L = 20 μm and W = 15 μm device. The gate voltage ranges from 0.0 V to 2.25 V in steps of 0.25 V.

aluminum sputter deposition which left a thin oxide at the interface between the electrode and diffusion region.

The sub-threshold characteristics are shown in Fig. 7 with a log scale. For both the ON-state and the OFF-state, the sub-threshold swing is around 110 mV/dec. This consistency between the two states allows for a large range of gate voltages that still have a 0.6 V memory window. It is not uncommon for the different states of the device to have different sub-threshold swings which would make the memory window inconsistent. The small changes in the drain current in the OFF-state curve is thought to be due to partial switching of the ferroelectric domains during the sweep.

The change in the threshold voltage between the two states, or the MW, was consistent over the first 50 cycles at 0.6 V shown in Fig. 8. The cycling at the beginning starts to open the memory window (MW) wider from 0.4 V to 0.6 V within 10 cycles. This shows that with a 4.5 V stress for 10 ms, the device is ready quickly. There may be some reduction in cycling stabilization if the pulse to the gate is in the nanosecond range. Testing was done to observe the minimum gate pulse width required to achieve a 0.6 V MW, but the testing setup was limiting the integrity of the pulse from the pulse generator to the actual gate electrode. The steady reduction in the threshold voltage with increasing cycles could be an indication of a trapping mechanism which is a known problem with HfO_2 based devices [1].

The ON-to-OFF current ration is shown in Fig. 9. This ratio can be used to determine the optimal read setting for the device. To sense the state of the device, a large difference between the ON and OFF current needs to be observed by the sensing mechanism for the memory array. The device shows a difference larger than three orders of magnitude for a large range of gate voltages.

The I_D vs. V_{DS} curves shown in Fig. 10 exhibit punch through even though a retrograde substrate well profile was implemented. Punch through is more apparent at lower gate voltages since the gate has less control over the channel and the source and drain depletion regions are larger. As you increase the gate voltage the punch through effect happens at high V_{DS} bias.

V. Conclusion

The process that was developed at RIT was successful in demonstrating a functioning n-channel FeFET for use as a memory device with high compatibility with CMOS technology using Si:HfO_2. The ALD Si:HfO_2 etch recipe was developed using chlorine based gases in the LAM 4600 RIE for an etch rate of 5.4 nm/min. The MFIS capacitors demonstrated ferroelectric behavior similar to the MFM capacitors from NaMLab which confirms the reasoning behind the threshold voltage shift when testing the FeFET device. There was a large contact resistance due to imperfect processing that could be improved on through silicide source and drains potentially. The FeFET demonstrated a memory window of 0.6 V which was independent of the transistor dimensions as it is a charge effect and the polarization charge is measured per unit area.

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