Fabrication of Sub-300 nm Fins at RIT by SADP

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***Abstract*—The goal of fabricating sub-300 nm fins with the implementation of self-aligned double patterning (SADP) at Rochester Institute of Technology's (RIT's) Semiconductor & Microsystems Fabrication Laboratory (SMFL) was not realized completely. An energy dose meander was completed in order to qualify a new resist being used with the fabrication process that Christopher O'Connell developed for his graduate thesis. Manual spin coating of Spin-on-Carbon (SOC), bottom antireflective coating (BARC), and photoresist were all qualified. A 2:1 ratio of AZ MiR 701 photoresist to PGMEA was used to thin the resist for implementation of a 300 nm coat. Low pressure chemical vapor deposition (LPCVD) of silicon nitride as a spacer material was qualified with a ~6.4 nm/s deposition rate and a film etch rate of ~0.3 nm/s. Oxide deposition by in Applied Materials' P5000 TEOS chamber was qualified with an ~8.8 nm/s deposition rate and a ~3.2 nm/s etch rate in the magnetically enhanced reactive ion etch (MERIE) etch chamber of the same P5000 tool cluster. In the RIE chamber, an etch rate of ~0.8 nm/s was qualified for the BARC layer. Ultimately, the oxide mandrels appeared to lack essential vertical sidewalls.**

Keywords—SADP, P5000, oxide mandrel, nitride spacer

I. INTRODUCTION

In 1965, one of the founders of Intel, Gordon Moore, projected that every two years the number of transistors on an integrated circuit (IC) would double. This projection is now known as "Moore's Law." Since then, the semiconductor manufacturing industry has attempted to maintain this predicted trend. However, as technology improves and transistors become smaller and smaller, it becomes more difficult to maintain Moore's Law. One way in which the size of transistors has shrunk is through the development of FinFETs. As opposed to planar FETs, FinFETs have a three-dimensional geometry so there is better gate control, less gate current leakage, and the transistors can be packed more densely.

FinFETs are widely used in the semiconductor industry today in order to create complex and small ICs. Since RIT is a very industry-focused institution that prides itself on readying students to become competent employees, the fabrication of silicon fins in undergraduate RIT labs would be beneficial to the education of students.

SADP is a patterning advancement that allows the lithography pattern to be transferred to a mandrel in order deposit a material over it and create sidewall spacers on either side of the mandrels. The spacers, in turn, are used as an etch mask. The benefit of this is that smaller features may be realized without the implementation of more expensive lithography equipment. At RIT, the i-line ASML stepper has a theoretical lowest limit of 300 nm as the smallest possible feature, which is why this experiment is targeting sub-300 nm fins with SADP.

Figure 1, created by Chris Mack, shows a simple SADP process flow. As the figure shows, a dummy pattern is first created by performing a lithography step and etch step. This "dummy pattern" is the mandrel. A spacer material is then deposited on top of the dummy pattern and etched back. Once the dummy pattern is stripped away, all that remains is the sidewall spacers on top of the underlying film stack. These spacers now act as the etch mask for the final features.

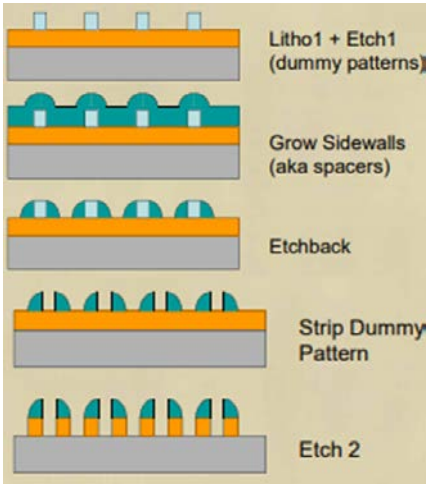

Figure 1: SADP process flow overview [1].

In SADP processing, the uniformity of the film depositions and the etch uniformities are crucial to process control and the integrity of the final features. Highly selective and highly anisotropic etches are required.

II. PROCESS FLOW [2]

Figure 2 lists the process steps for successful fabrication of a silicon fin at RIT. The process was developed by Christopher O'Connell. The only modification from O'Connell's process is a different routine for the mandrel etch. O'Connell developed a more complicated routine than what is described here so that the process would be contained in the P5000 tool cluster, improving manufacturability.

First, an RCA clean is performed on silicon wafers. Then, 80 nm of SOC is deposited as a hardmask for the eventual etch into the silicon for fin formation. 120 nm of oxide is deposited on top of the SOC by chemical vapor deposition (CVD) of tetraethyl orthosilicate (TEOS) as the precursor gas. 65 nm of BARC is deposited next to help with the imaging of small

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features. Then, 300 nm of positive photoresist is deposited. The BARC is etched followed by a trim etch of the remaining BARC/photoresist pattern. The trim etch creates a thinner feature in the subsequent oxide mandrel etch.

Once the mandrel etch has been performed, a solvent strip is implemented in order to remove the photoresist and BARC that are present on top of the oxide mandrels without etching the exposed SOC. Next, 150 nm of silicon nitride is deposited conformally over the oxide mandrels. The silicon nitride spacer etch removes the silicon nitride on top of the oxide mandrels and over the SOC. Silicon nitride only remains on either side of each mandrel; these are the spacers. The exposed oxide mandrel is then stripped, leaving only the silicon nitride spacers on top of the SOC. The exposed SOC is etched and then an anisotropic silicon etch is performed in order to etch the silicon fins. A cross-sectional view of the process is shown in **Figure 3**.

Figure 2: Process flow for fin formation.

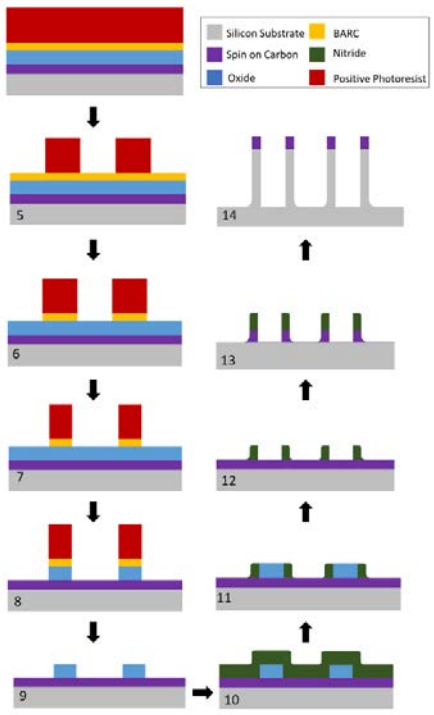

Figure 3: Partial process flow cross sections.

III. EXPERIMENTAL PROCEDURE

First, the bare silicon wafers were cleaned with an RCA clean and the SOC process recipe provided by O'Connell in **Table 1** was verified. This was performed on RIT's SCS spin coater, which is a manual spin coater. Next, spin speeds and coat times were qualified for the 65 nm BARC deposition and the 300 nm photoresist deposition on RIT's SEE spin coater, another manual spin coater. The positive photoresist used was AZ MiR 701. All coat thicknesses and uniformities were determined using RIT's Prometrix SM300 SpectraMap, a spectrophotometer.

Next, an energy dose meander was performed in order to determine the optimal exposure dose for the process. O'Connell's mask was used, as it contains long lines for the formation of fins.

The deposition rates of both the silicon nitride and the oxide were determined next. The silicon nitride was deposited in RIT's LPCVD tool. The oxide, as mentioned previously, was deposited using RIT's Applied Materials P5000 TEOS chamber.

Next, the etch rates were determined for the oxide, the BARC, and the nitride layers. All three materials were deposited onto a bare silicon and etched in the MERIE chamber (chamber C) of the P5000 with their respective etch recipes.

Next, bare silicon wafers were cleaned, deposited with the oxide mandrel layer, coated with BARC and PR, and patterned. The BARC open etch was performed, followed by the mandrel etch. A wafer was cleaved and the oxide mandrels were inspected using scanning electron microscopy (SEM).

Then, a solvent strip was performed on the intact wafers, followed by silicon nitride deposition and the silicon nitride spacer etch. Again, a wafer was cleaved and the integrity of the sidewall spacers was inspected using SEM analysis.

IV. RESULTS AND ANALYSIS

Table 1 details the parameters for coating and hardening of SOC onto a bare silicon wafer. The resulting measurements from the SpectraMap were an average thickness of 70.2 nm and an average standard deviation of 1.1 nm.

Table 1: Spin-On-Carbon deposition and hardening process details.

Spin-On-Carbon Recipe			
100 °C Dehydration Bake for 1 minute			
Step	Ramp Time (s)	Spin Speed (RPM)	Time (s)
1	3	800	20
2	1	2500	60
3	N/A	N/A	N/A
4	15	N/A	N/A
300 °C Cure for 3 minutes			

The AZ MiR 701 resist, in order to be coated at 300 nm, needed to be thinned down. A 2:1 dilution of the 701 photoresist to PGMEA (Propylene glycol methyl ether

acetate), a solvent, was implemented. **Table 2** records the spin speeds and spin durations that were implemented in order to achieve the target thicknesses for both the BARC and the PR. Also included in **Table 2** is the data from the SpectraMap with implementation of an 81-point measurement.

Table 2: SpectraMap data and coater parameters for BARC and PR.

Film Material		BARC	PR
SEE Coater Parameters	Spin Speed (RPM)	2000	2500
	Time (s)	45	30
SpectraMap Data	Mean Thickness (nm)	63.6	312.4
	Standard Deviation (nm)	0.3	3.9

The energy does meander resulted in an optimal dose of 150 mJ/cm^2. This was performed with conventional illumination and RIT's ASML stepper's default NA of 0.48 and default sigma value of 0.625. A focus offset of zero was also implemented.

The silicon nitride deposition was performed using RIT's low-pressure nitride recipe in the LPCVD tool. A 20-minute deposition resulted in a deposition rate of ~6.4 nm/s with a total film thickness of 127.9 nm and a standard deviation of 2.8 nm.

The oxide deposition by CVD with TEOS was performed using RIT's 5 kÅ TEOS low stress recipe ("A6-5KA TEOS LS"), adjusting the deposition time to 15 seconds and resulting in a deposition rate of about 8.8 nm/s. The average thickness was 131.9 nm for a 15 second deposition with a standard deviation of 4.5 nm. This recipe implements 285 sccm of O_2, 400 sccm of TEOS, and a pressure of 9.0 Torr at deposition.

The BARC etch recipe, "C6-BARC," implements a 6 sccm flow of O_2 at 10 mTorr during the 60 second etch step. The resulting etch rate is ~0.8 nm/s. The oxide mandrel etch recipe, "C6-MANDREL-ETCH," performs the etch step with the following gas flows and a 60 second duration:

- CHF3-B: 30 sccm
- CF4-B: 60 sccm
- AR-B 100 sccm
- C2F6: 15 sccm

The resulting etch rate is about ~3.2 nm/s for the mandrel layer.

The silicon nitride etch recipe, "C6-NITSPA," performs the etch step with a pressure of 30 mTorr and the following gas flows:

- CHF3-B: 22 sccm
- CF4-B: 15 sccm
- AR-B 90 sccm
- O2: 4 sccm

The resulting etch rate is about 0.3 nm/s for the silicon nitride film.

The SEM inspection of the oxide mandrels is illustrated in **Figure 4** and **Figure 5**. **Figure 4** shows one of the wider mandrels, while **Figure 5** is a zoomed-in version of that same mandrel. As can be seen in the figures, the sidewall does not look completely vertical.

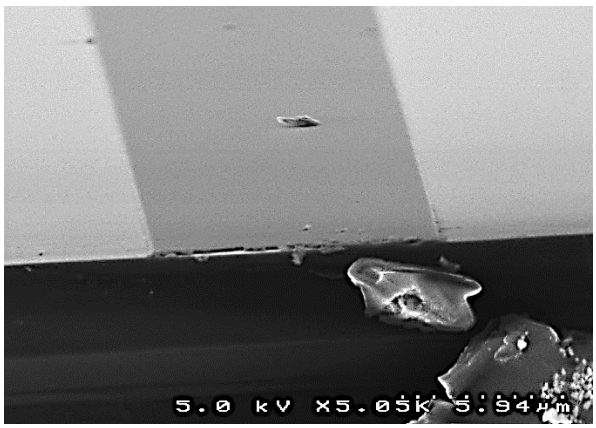

Figure 4: Wide oxide mandrel on silicon substrate.

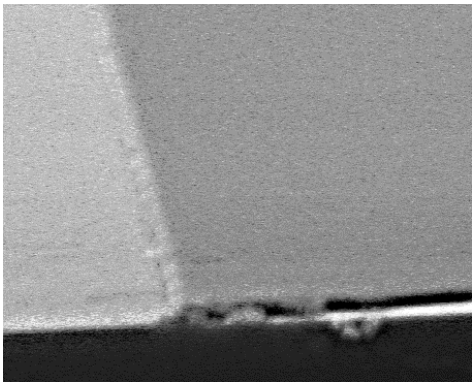

Figure 5: Zoomed-in view of oxide mandrel sidewall.

Figure 6 shows the image from the SEM after the silicon nitride etch was performed for 405 seconds. At this point in the process, the oxide mandrel should be present with nitride spacers only present on either side of the mandrel. However, the image in **Figure 6** shows a disintegrated mandrel. Either the nitride etch was not selective and anisotropic enough or the fault is due to the lack of anisotropy of the oxide mandrel etch. If the oxide mandrel does not have vertical sidewalls then the nitride etch will never result in spacers; all of the nitride will be cleared.

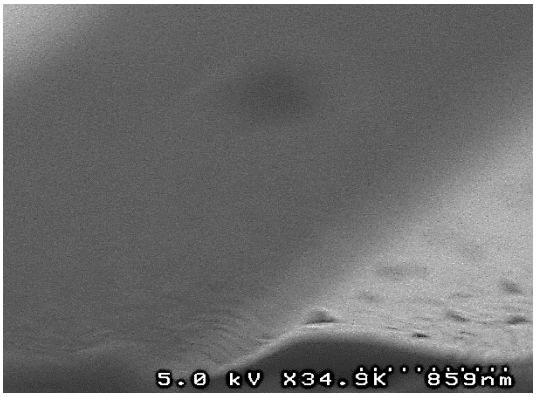

Figure 6: Oxide mandrel post silicon nitride etch.

V. CONCLUSIONS

The fabrication of sub-300 nm silicon fins was ultimately not successful due to the suspected anisotropy of the oxide mandrel. The non-vertical sidewalls did not allow for formation of nitride spacers on either side of the mandrels.

In order to achieve more perfect anisotropy of the oxide mandrel layer, either one or a combination of the following developments needs to be implemented:

- Addition of a hardmask layer on top of the oxide mandrel layer
- More anisotropic oxide mandrel etch
- More controlled and anisotropic nitride spacer etch

Future work will begin with the implementation of a hardmask above the oxide mandrel layer and with the development of RIE/plasma etch process improvements. The eventual implementation of the complete P5000 tool cluster is desired. With a successful fin fabrication process, implementation in undergraduate courses is expected. Furthermore, fabrication of silicon fins could lead to the development of a FinFET process by a PhD candidate.

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