FeFET Fabrication and Characterization at RIT

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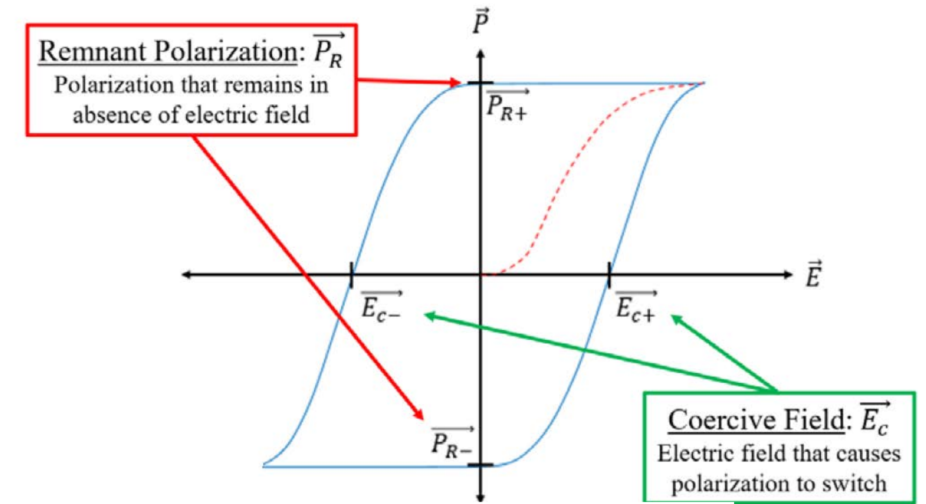
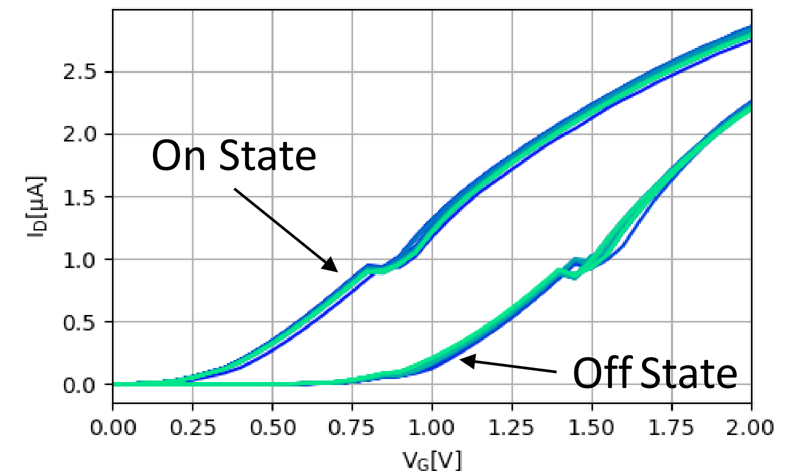
Electrical Characteristics of Ferroelectrics

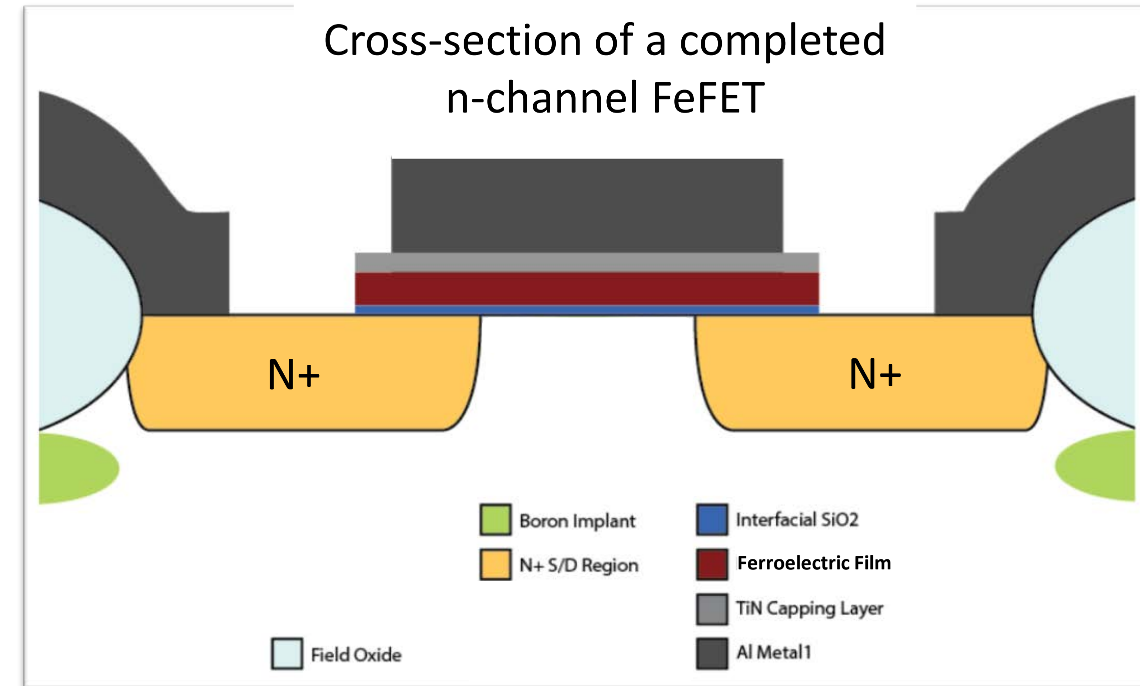
- A hysteresis loop is observed in ferroelectric materials when measuring polarization v. voltage
- Some parameters of interest associated with this loop include:
  - **Coercive voltage or Field (V_C/E_C)**, is the voltage or electric field at which there is 0 polarization
  - **Remnant Polarization (P_{r+} or P_{r-})**, is the positive or negative polarization of the material at 0V bias, ideally they are equal in magnitude
- This observed bi-stability, even after bias is removed, makes these materials a popular candidate for non-volatile memory applications





What are FeFETs?

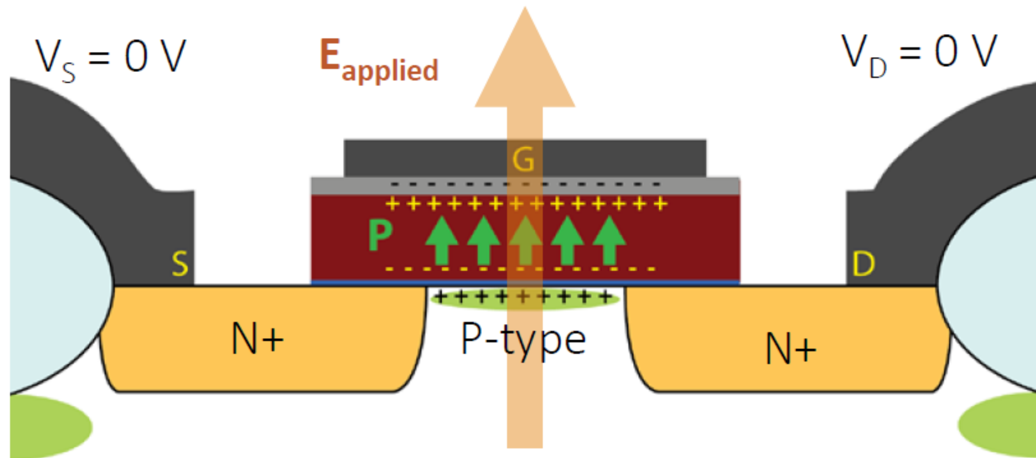
- Ferroelectric field effect transistors (FeFETs), are devices comparable to planar MOSFETs incorporating FE materials
- This material is implemented in place of a traditional gate dielectric (red layer in figure on right)
- State-of-the-art FeFETs utilize doped-hafnium oxide (HfO_2) ferroelectrics for CMOS compatibility

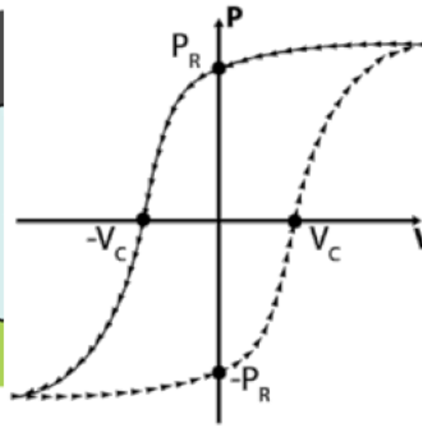


Modified from [1]

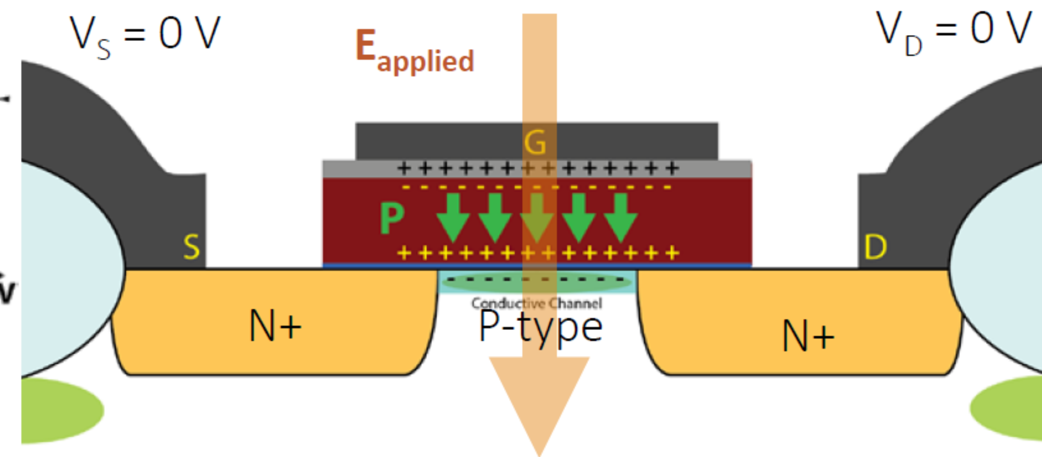
N-channel FeFET Operation

OFF State: $V_G < -V_C$





ON State: $V_G > V_C$



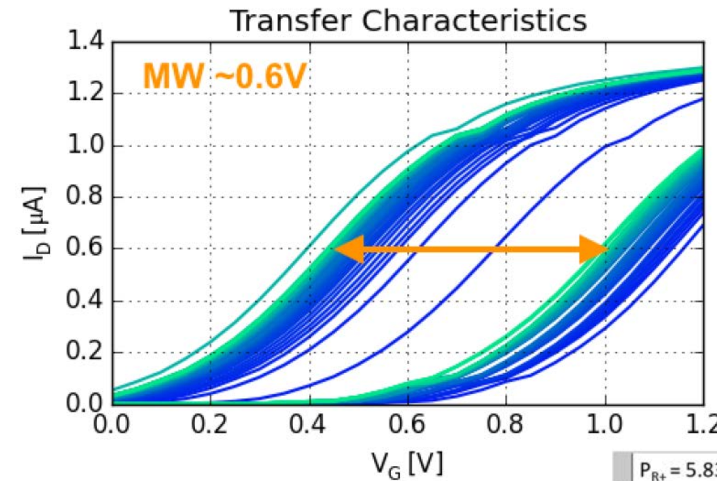
- Positive charge accumulates in channel, raises V_t

- Channel is partially depleted, lowers V_t

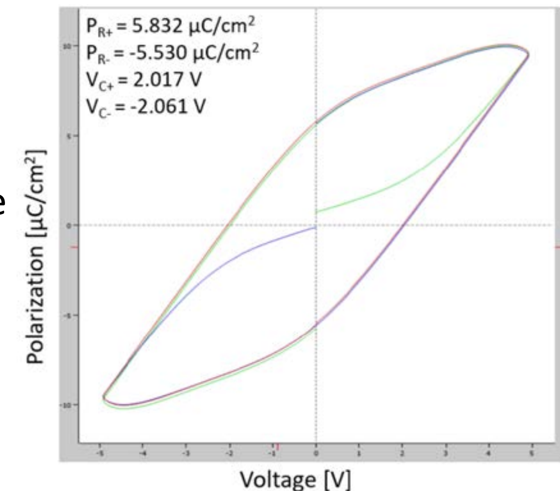
Figure of Merit for FeFET-based Memory:
- Memory Window (MW) = $V_{t,off} - V_{t,on}$
- Max. MW = 2*E_C*FE Thickness
- Larger Memory Window is Desired

Previous work at RIT

- $Si{:}HfO_2$ n-channel FeFETs fabricated by Joe McGlone and NaMLab
- A memory window of ~0.6V was observed; on state showed depletion-mode IV characteristics
- $Al{:}HfO_2$ capacitors with varying aluminum concentrations made by Casey Gonta and Josh Eschle with in-house ALD system
- Hysteresis was observed in resulting devices' PV characteristics



Transfer Characteristics of McGlone FeFETs show MW [1]



PV Characteristics of Eschle FE Capacitors, show hysteretic behavior [3]

Project Objectives

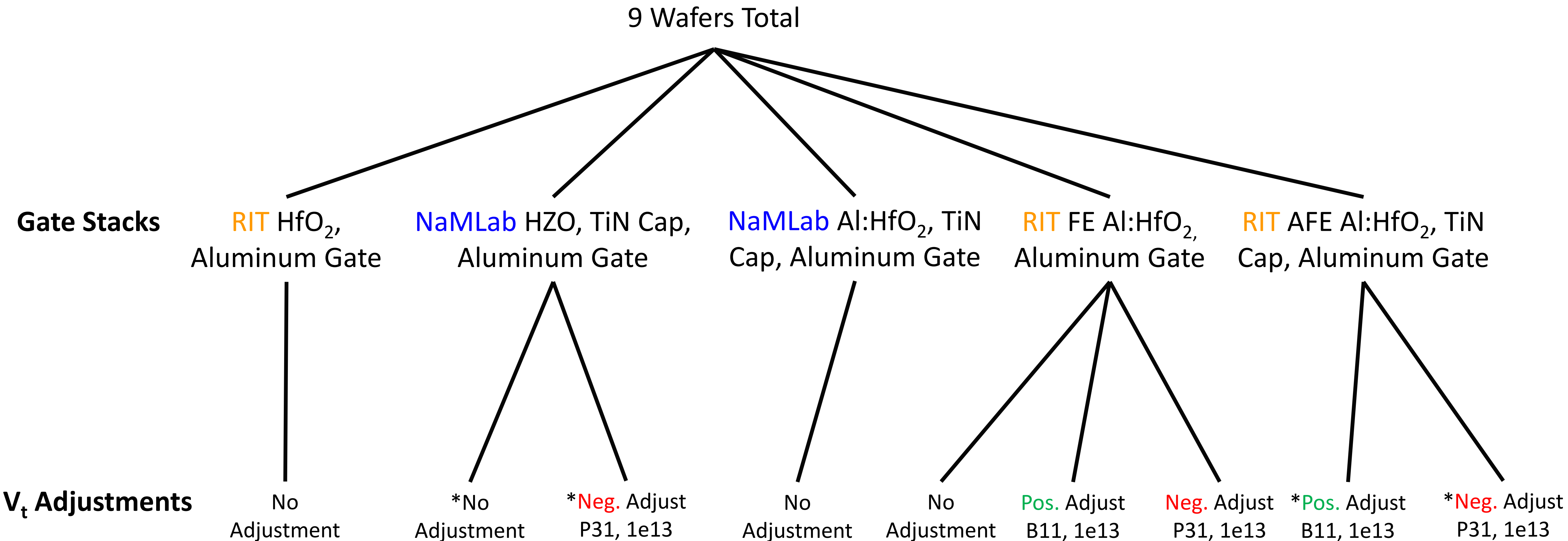
Goal: To fabricate and characterize n-channel ferroelectric field-effect transistors (FeFETs) in-house at RIT

- Integrate McGlone/Anderson’s FeFET process flow with Eschle/Gonta’s Al:HfO_2 ALD studies to make in-house n-channel FeFET process flow/devices
- Measure IV characteristics of fabricated devices
  - Investigate impact of threshold voltage adjustment implants on devices/memory window
- Compare in-house deposited ferroelectric films to those deposited at NaMLab in terms of observed memory window

Proposed n-channel FeFET Process Flow

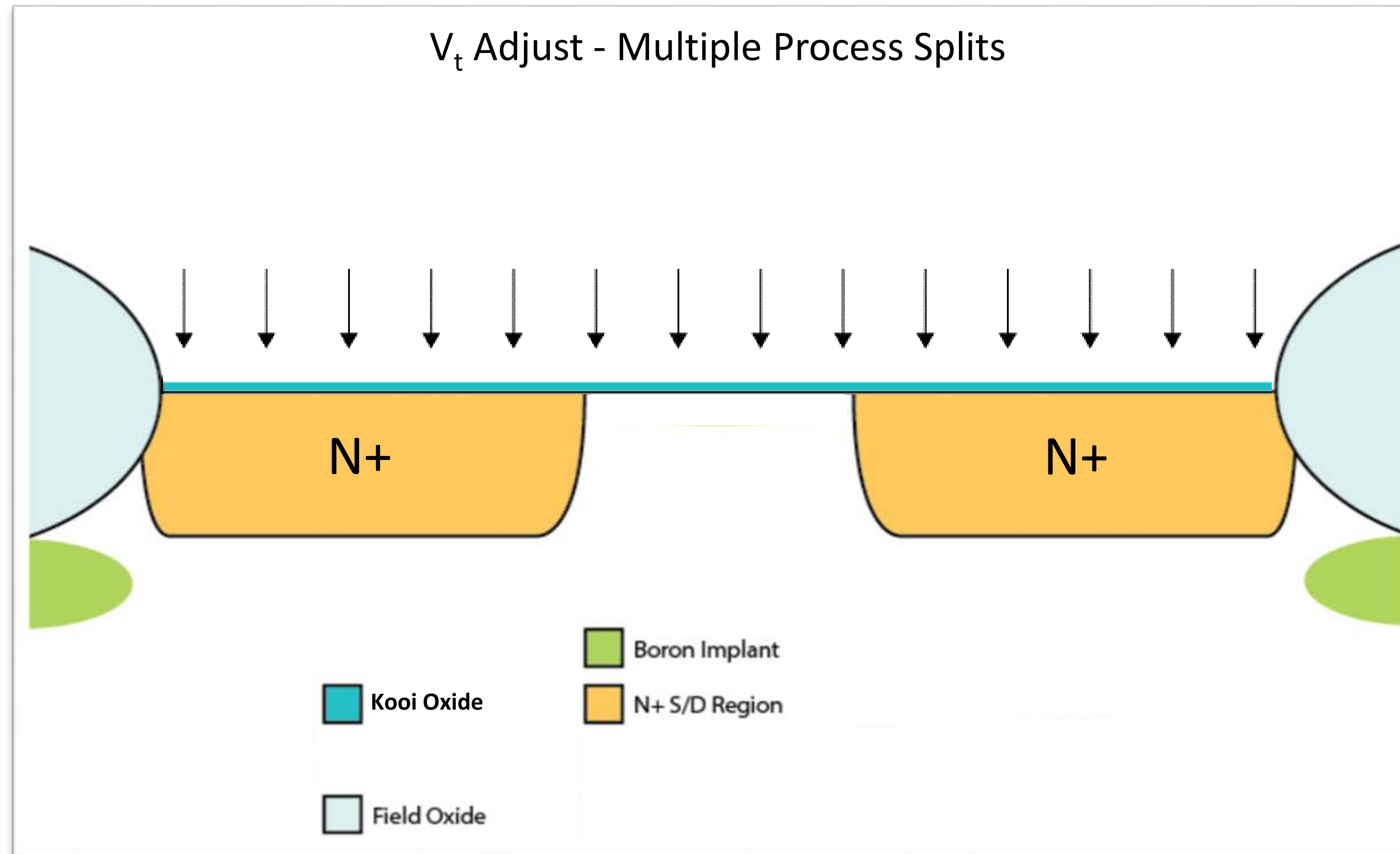
1) RCA Clean
2) Zero Level Lithography
3) 10:1 BOE etch (native oxide)
4) Zero Level Etch (alignment marks)
5) Ash Resist
6) RCA Clean
7) Pad Oxide Growth (50nm)
8) Back Side Implant (B11, 2e15)
9) LPCVD Nitride (150nm)
10) Level 1, “Active” Lithography
11) Dry Etch Nitride
12) Channel Stop Implant (B11, 8e13)
13) Ash Resist
14) RCA Clean
15) Field Oxide Growth (650nm)
16) Hot Phos Nitride Etch
17) 10:1 BOE etch (Pad Oxide)
18) Kooi Oxide Growth (100nm)
19) Level 2+3 “S/D” + “N+” Lithography
20) Source/Drain Implant (P31, 2e15)
21) Ash Resist
22) RCA Clean
23) S/D and backside Anneal
24) Threshold Adjust Implant
25) RTA
26) 10:1 BOE etch (Kooi Oxide)
27) ALD Ferroelectric Material
28) TiN Sputter
29) RTA
30) Level 5 “Gate” Lithography
31) Al:HfO_2/TiN Etch, LAM 4600
32) Resist Strip, Wet Bench
33) 10:1 BOE Dip
34) Aluminum Sputter (750nm)
35) Level 6 “Metal” Lithography
36) Aluminum Etch, LAM 4600
37) Resist Strip, Wet Bench
38) Evaporate Backside Aluminum
39) Sinter Aluminum

FeFET Processing Splits



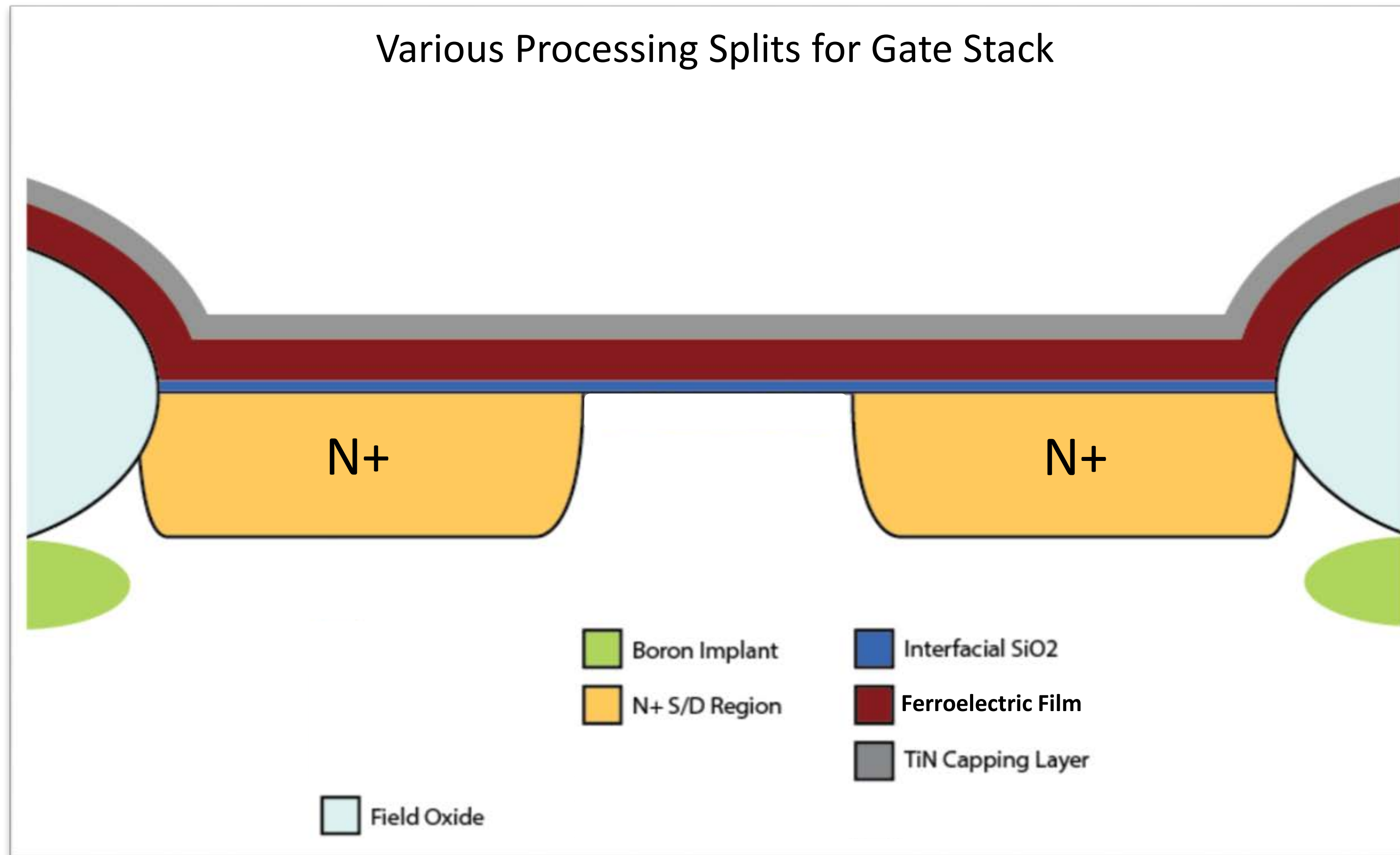
*** Denotes Wafers that are still in process**

Threshold Adjustment Implant, Split Step



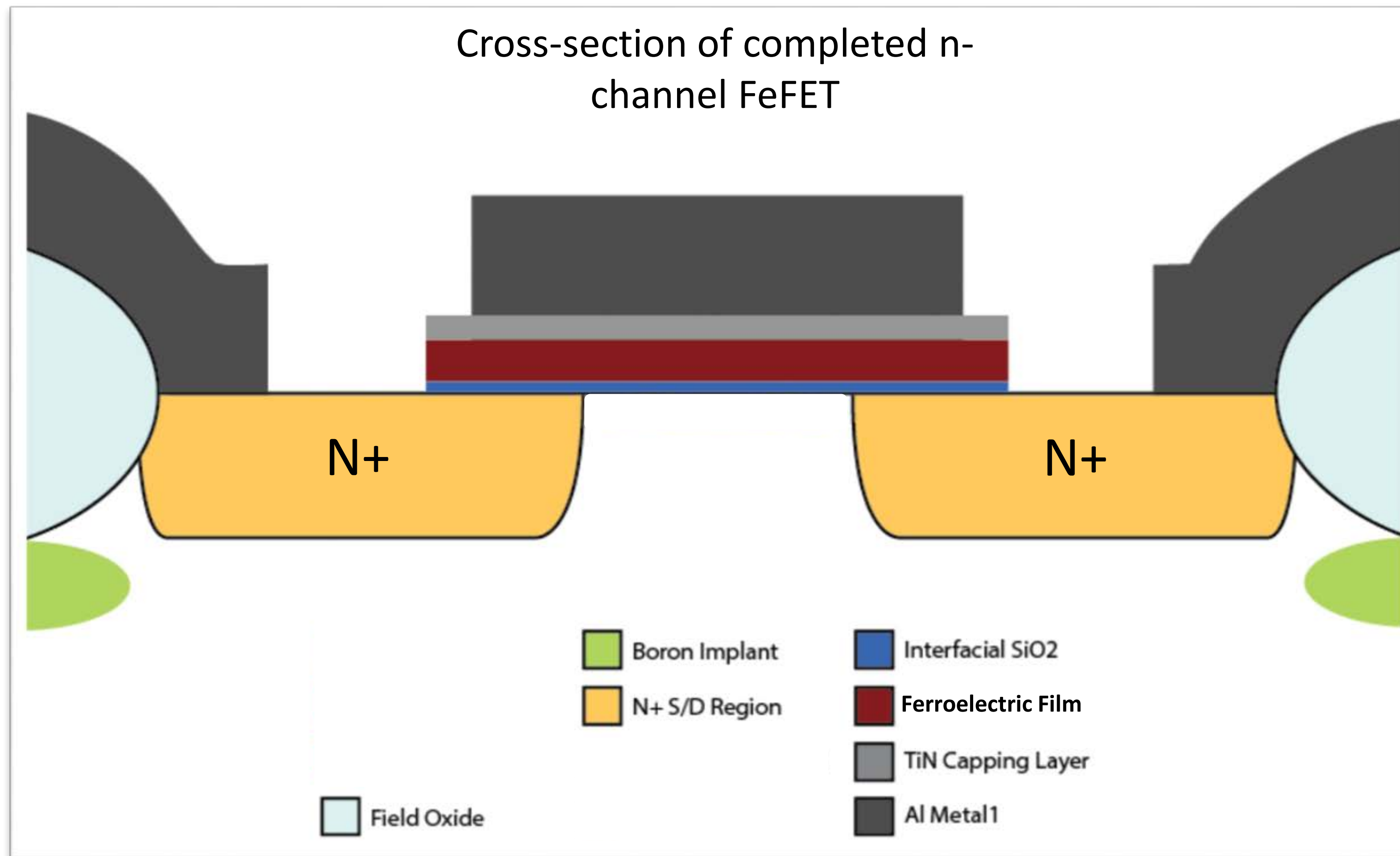
Modified from [1]

Gate Stack Deposition, Split Step



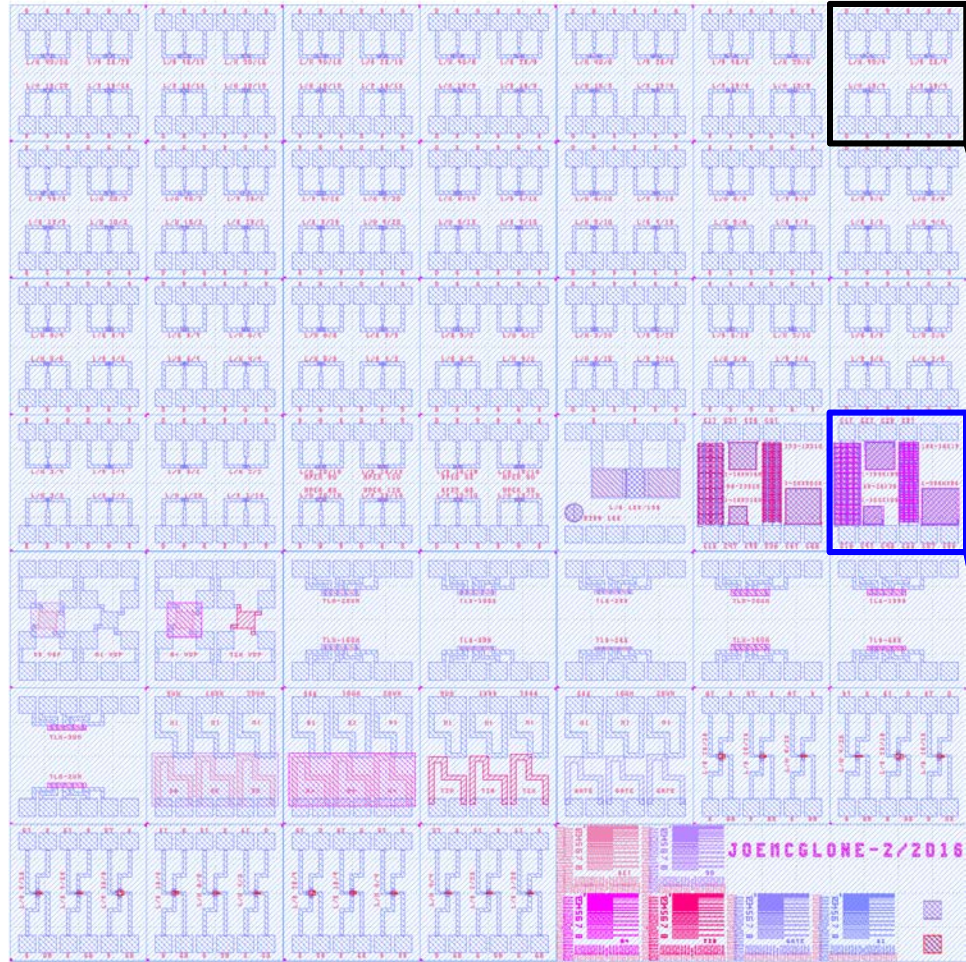
Modified from [1]

Final Device Cross-section

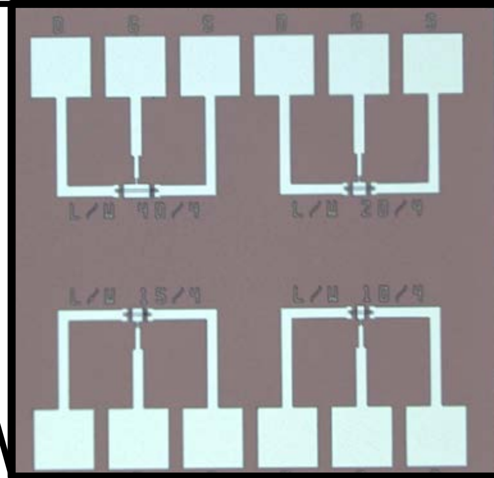


Modified from [1]

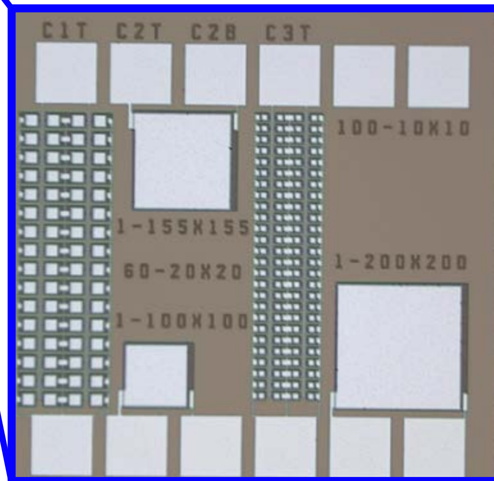
Microscope Images of Fabricated Devices



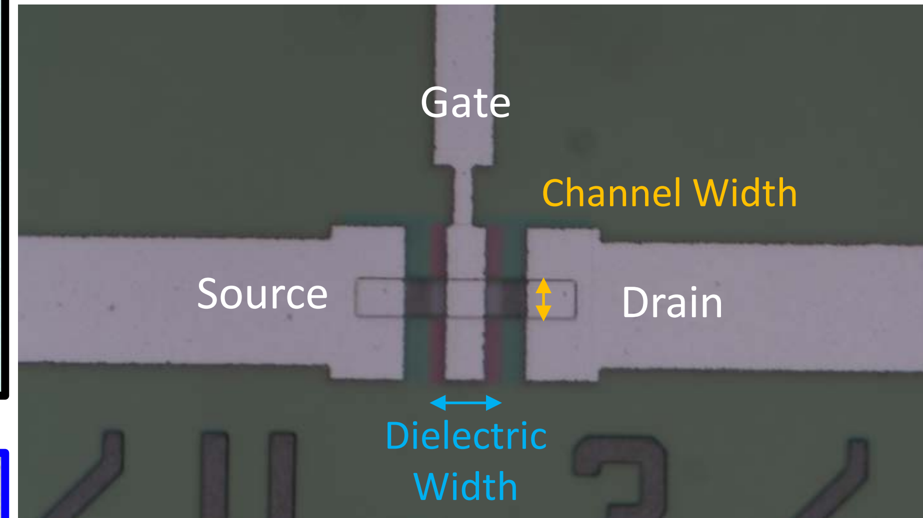
Mask designed by Joe McGlone



Capture of FeFET Array



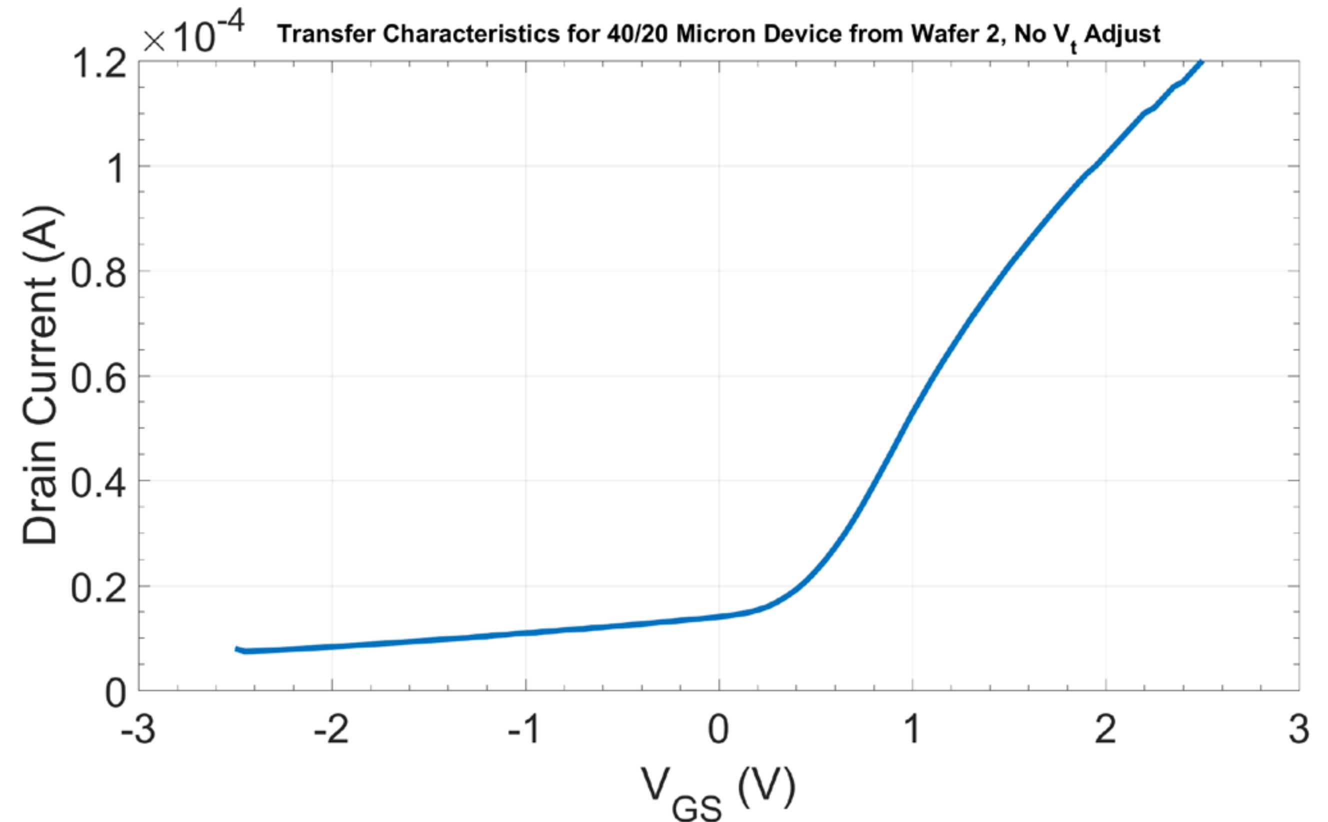
Capture of MFIS Capacitor Array



100X Image of FeFET with channel length and width of 3µm and 6µm, respectively

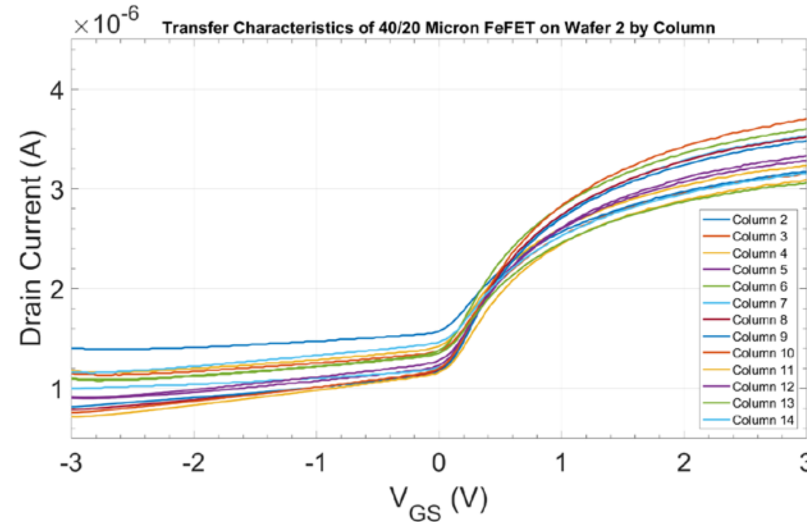
Initial Results, Gate Control with Leakage

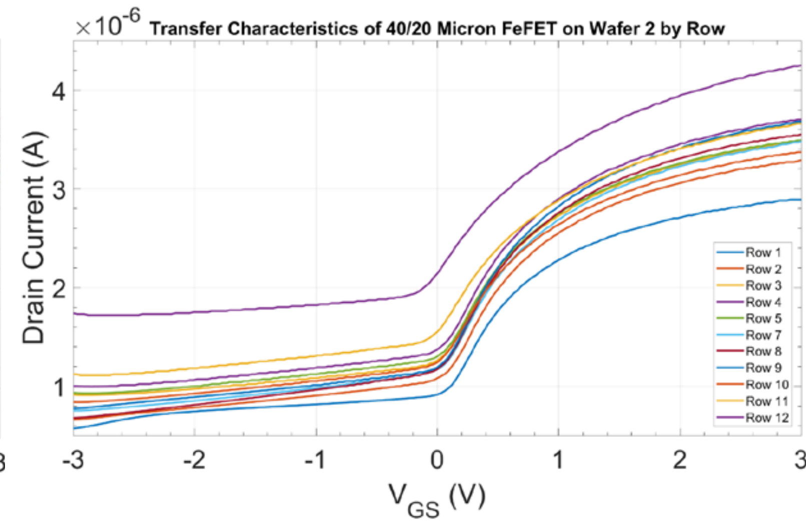
- Transfer curve shows "transistor-like" behavior
- Difference between off- and on-state current levels is only a factor of ~10
- Off-state leakage current is high, µA range
- Channel resistance appears quite large

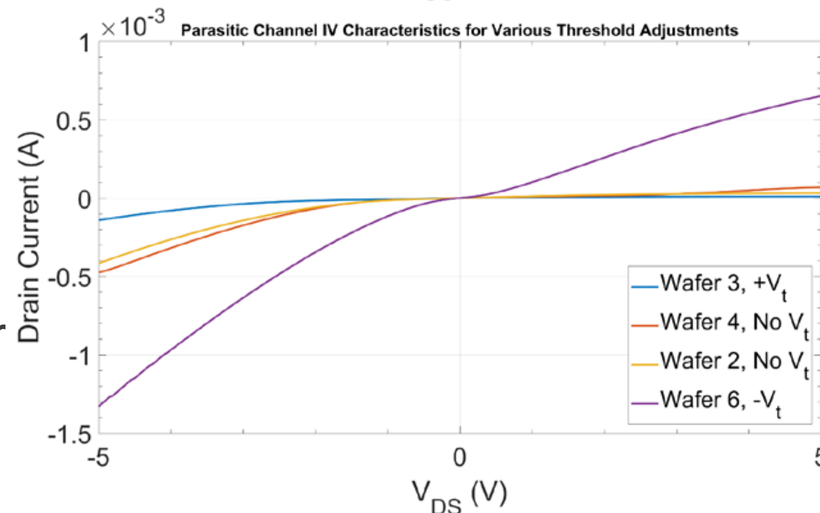


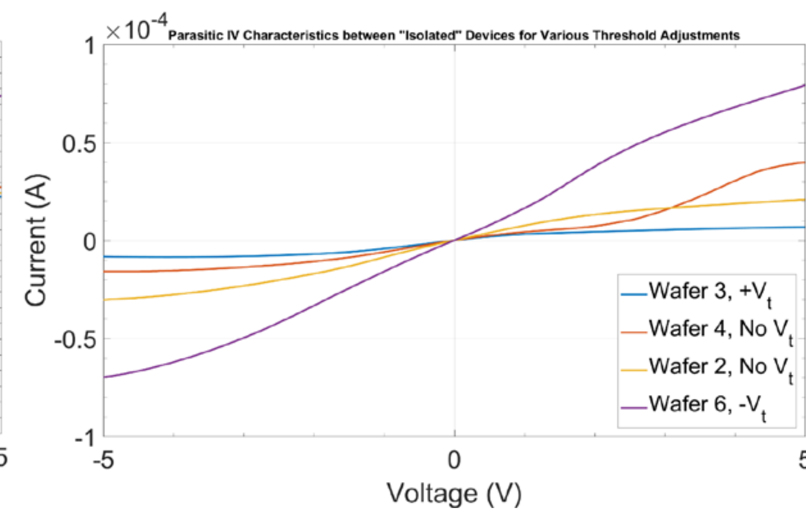
Off-state Leakage Investigation

- Wafer type was first verified using “hot-probe” methodology
- Wafer mapping was performed to determine whether leakage was localized
- Parasitic IV characteristics were measured between drain and source and source/drain terminals of adjacent devices
- The latter suggests improper n-type junction formation in source/drain regions



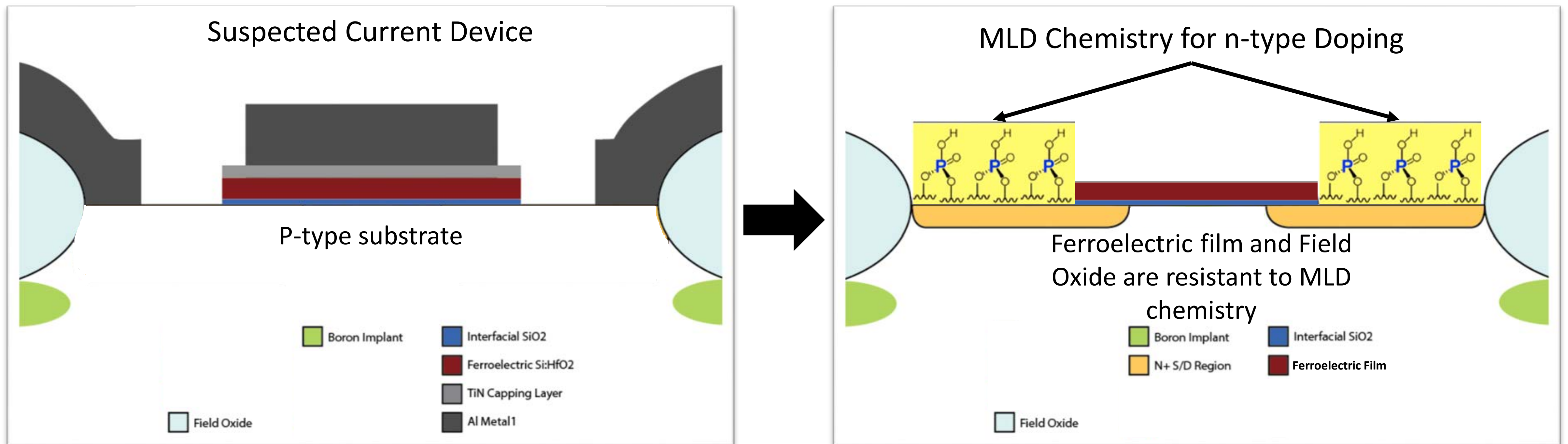






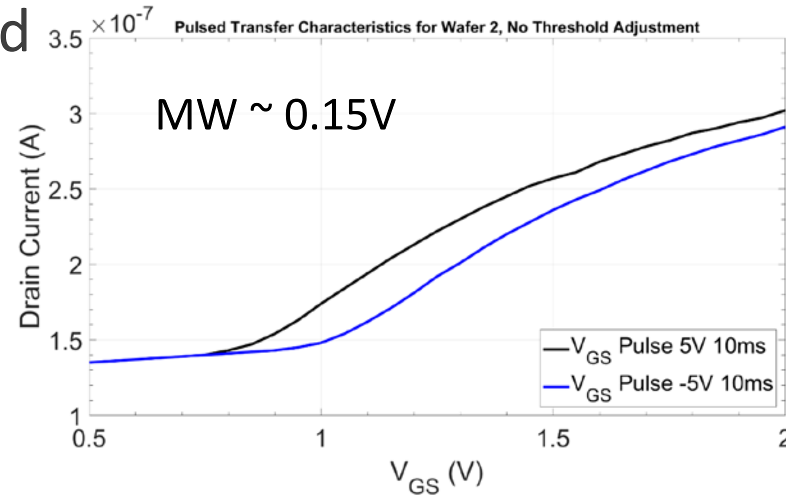
Proposed Plan to Revive Devices

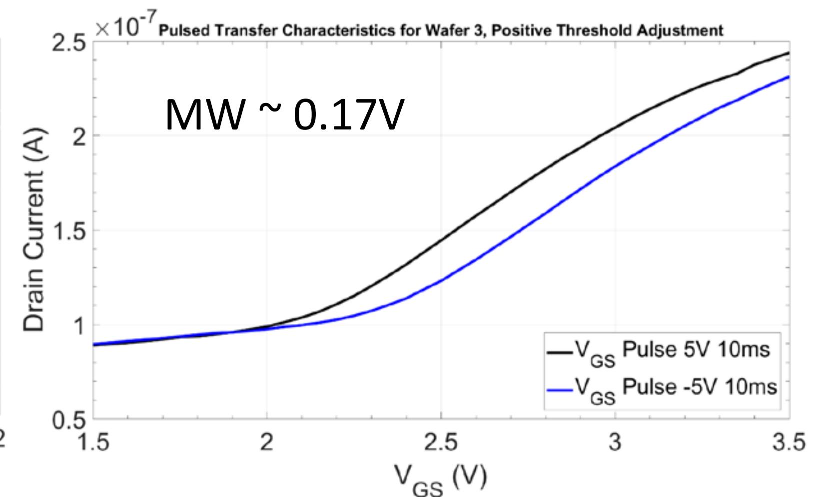
- Etch the aluminum off of one device wafer and expose it to a monolayer doping (MLD) source
- This may provide for a new self-aligned process for doping source/drain regions
- Redeposit aluminum and pattern as before, sinter
- Retest transistors and examine the off-state leakage

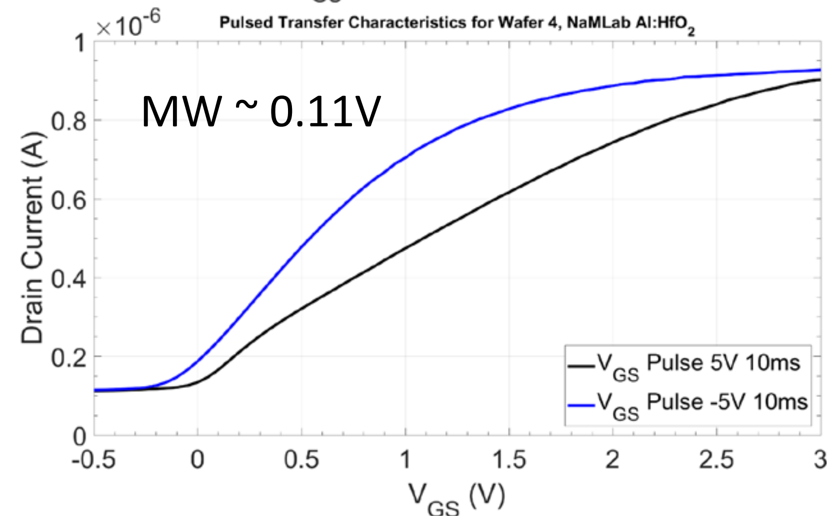


Initial Results, Ferroelectricity

- 2 of 3 FE samples fabricated at RIT demonstrate ferroelectricity in transfer characteristics
- Threshold adjustment implant appears to shift memory window without degrading it
- NaMLab memory window is comparable with opposite charging effects, possibly anti-ferroelectric





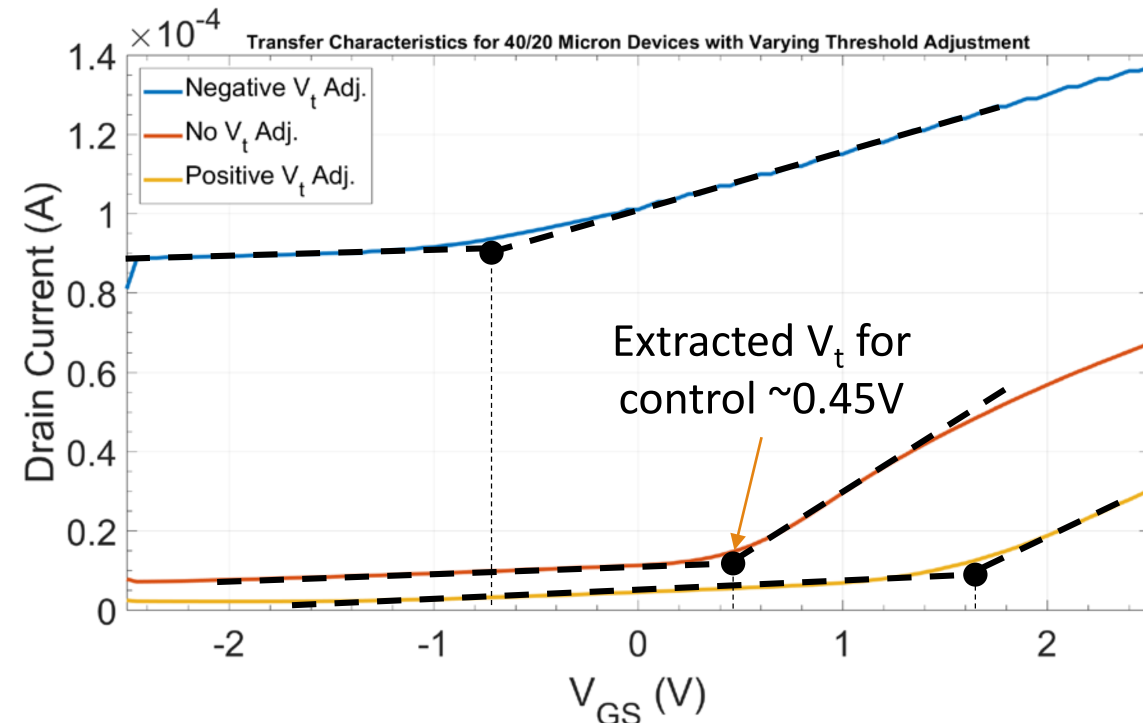


Legend:

= V_{GS} Pulse 5V, 10ms

= V_{GS} Pulse -5V, 10ms

Initial Results, V_t Adjustment Implants



V_t Implant Conditions	*Extracted V_t (V)	Shift from Control (V)	**Theoretical Shift (V)
B11 Implant, 1e13	~+1.65	+1.20	+0.78
P31 Implant, 1e13	~-0.7	-1.15	-0.78

*Threshold Voltage was experimentally extracted by finding the intersection of two extrapolated linear lines for each devices' on- and off-state currents (shown in figure)

**Theoretical threshold shifts were obtained through the following equation:

$$\Delta V_t = \frac{q * Dose}{C_{ox}}$$

- $Al:HfO_2$ relative permittivity from [2] used for computation
- Thickness of deposited $Al:HfO_2$ measured with VASE

Discrepancies in theoretical shifts and experimental shifts can be attributed to:

- Different permittivity of deposited film than that in [2]
- Oxide charges

Conclusions

- Improper source/drain formation is a strong candidate for the off-state leakage observed in fabricated FeFETs
- Improper formation could be the result of:
  - Junction spiking (not likely, but should be confirmed)
  - Improper dose processing (number of ions implanted)
  - Ion interference
- Ferroelectricity has been demonstrated in 2 of 3 samples fabricated at RIT
- Threshold adjustment was observed to have negligible impact on memory window
- Extracted threshold voltage shifts differ from those theoretically predicted on threshold adjusted wafers, but they appear to have worked accordingly

Future Work

- Integration of more advanced CMOS processing techniques such as:
  - Monolayer doping (MLD), process for this has been established at RIT and it would allow for self-aligned gates as well
  - Low-temperature silicide formation, has also been demonstrated at RIT
- Ferroelectric film deposition at RIT paves the way for additional device architectures including:
  - Ferroelectric tunnel junctions (FTJs)
  - Negative-capacitance field-effect transistors (NC-FETs)

Acknowledgments

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