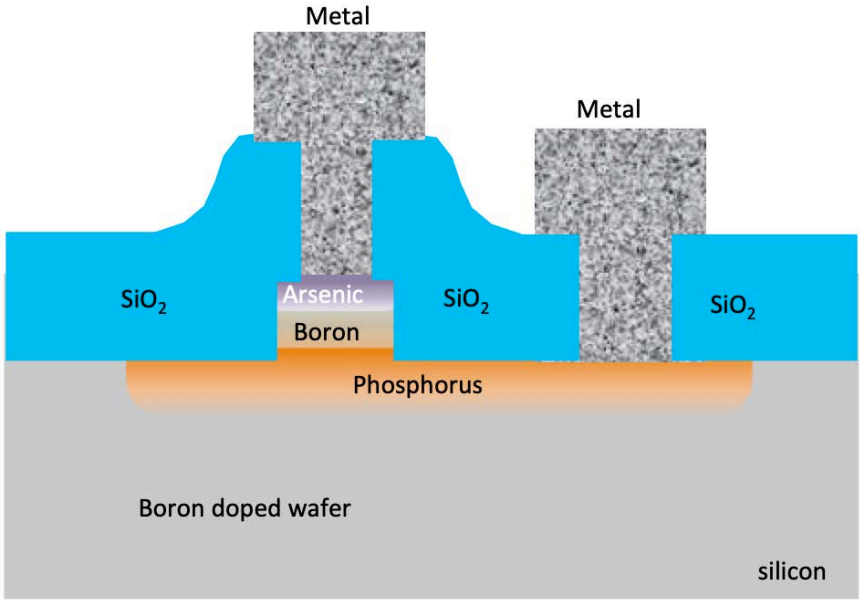
Biristor Array Investigation

By Jeremiah Leit



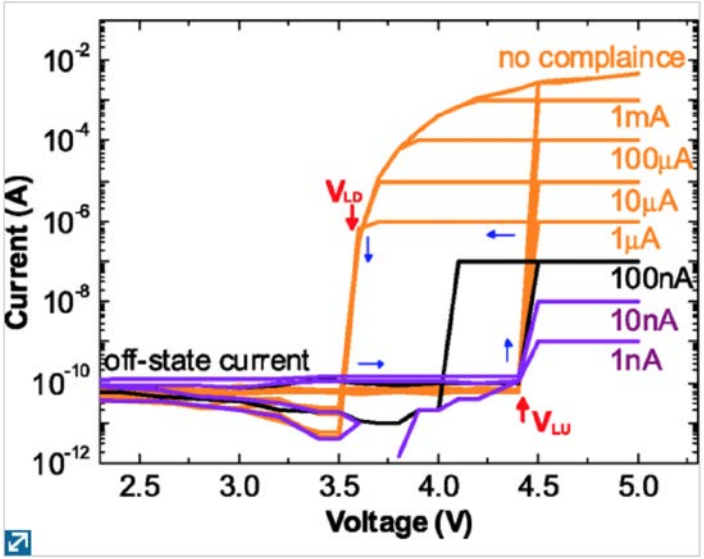
A device that can be used for hardware based encryption and neural network computing

What is a Biristor?

- A biristor is a two terminal device with two different modes of operation.
    1) Silicon Controlled Rectifier Latch
    2) Neuron Fire mode
- It is essentially a floating base Bipolar Junction Transistor.
- The device can be either NPN or PNP however, in this project I am fabricating NPN devices.
- It observes an avalanche effect which changes the internal resistance of the device.
- This makes it essentially a type of resistor with volatile memory or memristor.

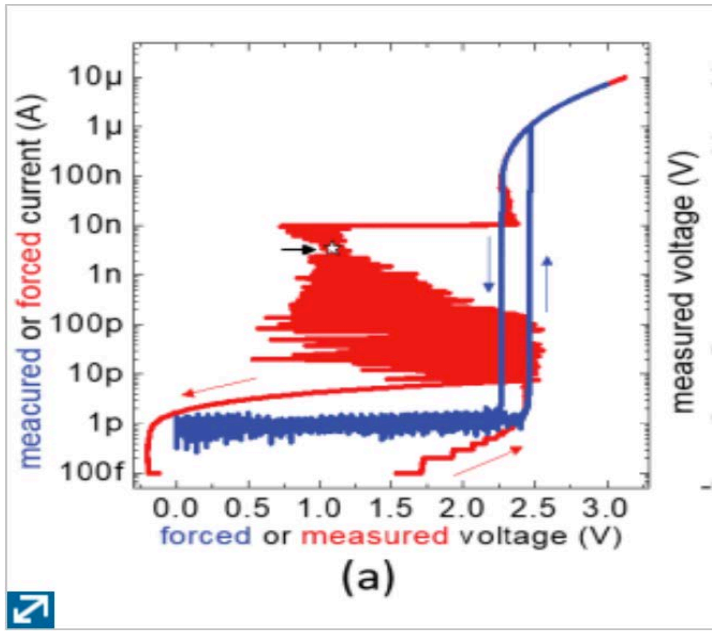
What do the I-V characteristics look like?

Silicon Controlled Rectifier Latch mode of operation



J. Han and M. Meyyappan, "Trigger and Self-Latch Mechanisms of n-p-n Bistable Resistor," *IEEE Electron Device Letters*, vol. 35, no. 3, pp. 387–389, Mar. 2014.

Leaky Latch/Un-latch or Neuron –Fire mode of operation



Jin-Woo Han ; M. Meyyappan

Biristor applications?

- A latching change in the resistance value of the device which would allow it to be used as a memory element.
- The neural spiking method can be used to create neural networks that are designed to compute information more in manner more like a human brain than a microprocessor and possibly use less energy.
- If scaled properly the diode isolation from both directions as well as that caused by the dielectric TEOS around the device could create quantum dots.

What are my project goals?

- Fabrication of Biristors

1. Mask Design
2. Process Design
3. Fabrication
4. Electrical Testing

- Compare Measured Results to Published Results
- Determine Relation Between Scaling and I-V Characteristics

The Ion Implant Steps

- Replicate the device fabricated by Jin-Woo Han.

  Consulted for ion implantation details and other processes.

- Three Implant steps

  Shallow arsenic implant

  $3x10^{15}$ cm^{-3} 80keV

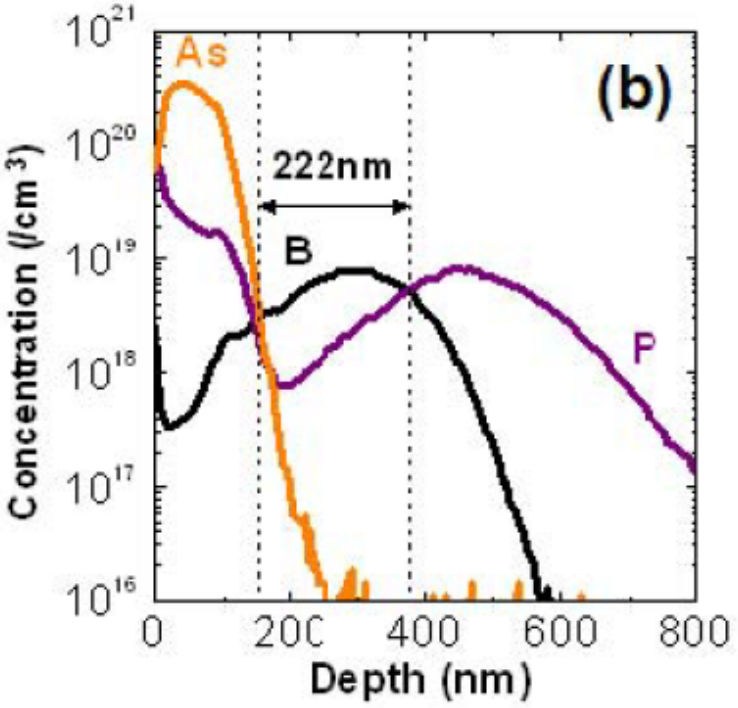
  Boron implant

  $8x10^{13}$ cm^{-3} 100keV

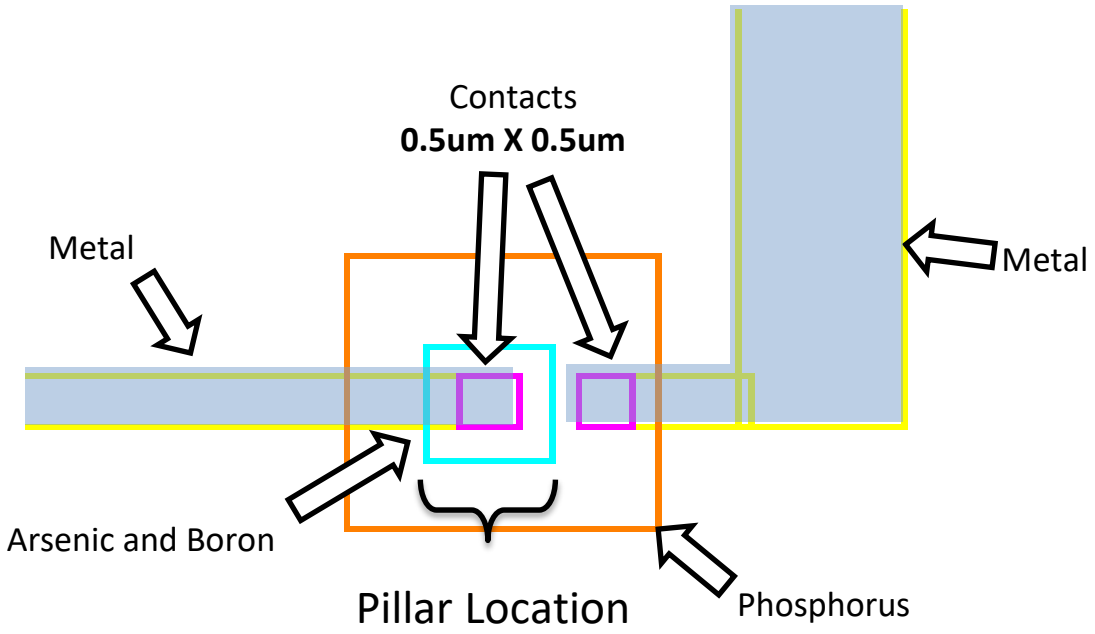
  Deep phosphorous implant

  $1x10^{14}$ cm^{-3} 500keV

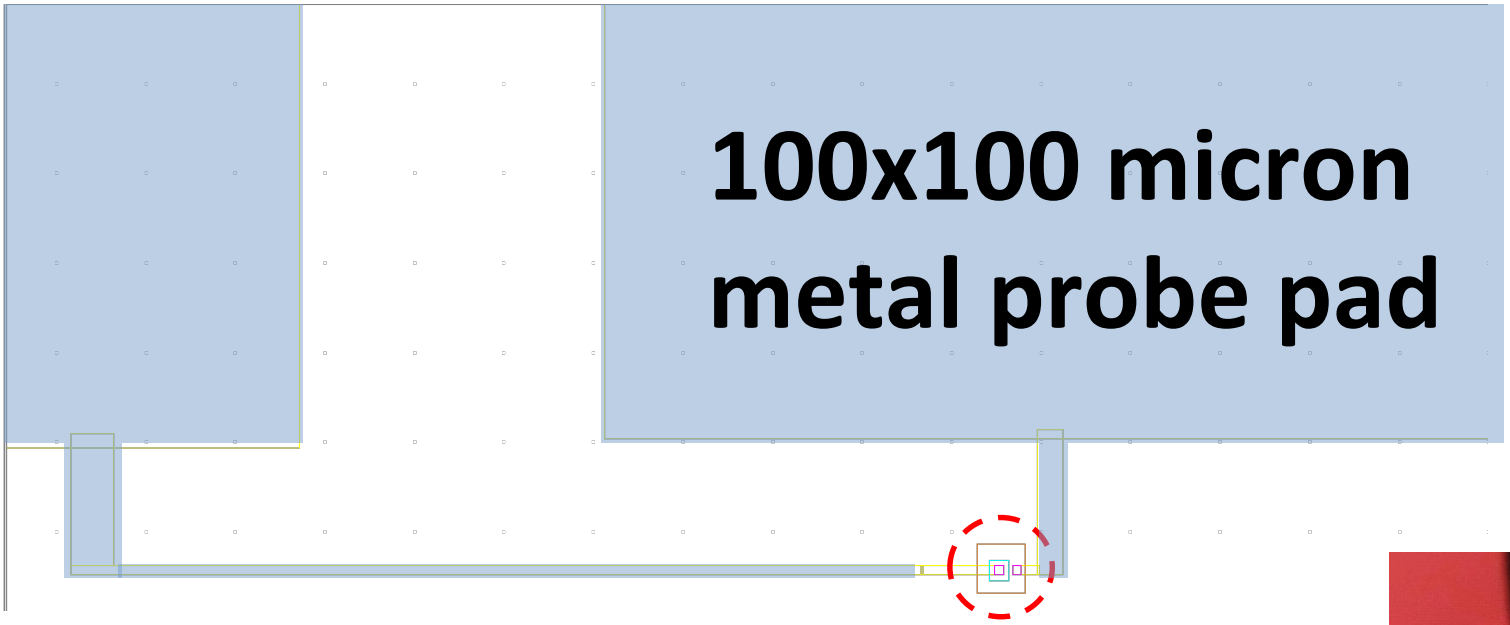
  Implant done by Innovion



Mask Design For Individual Biristor



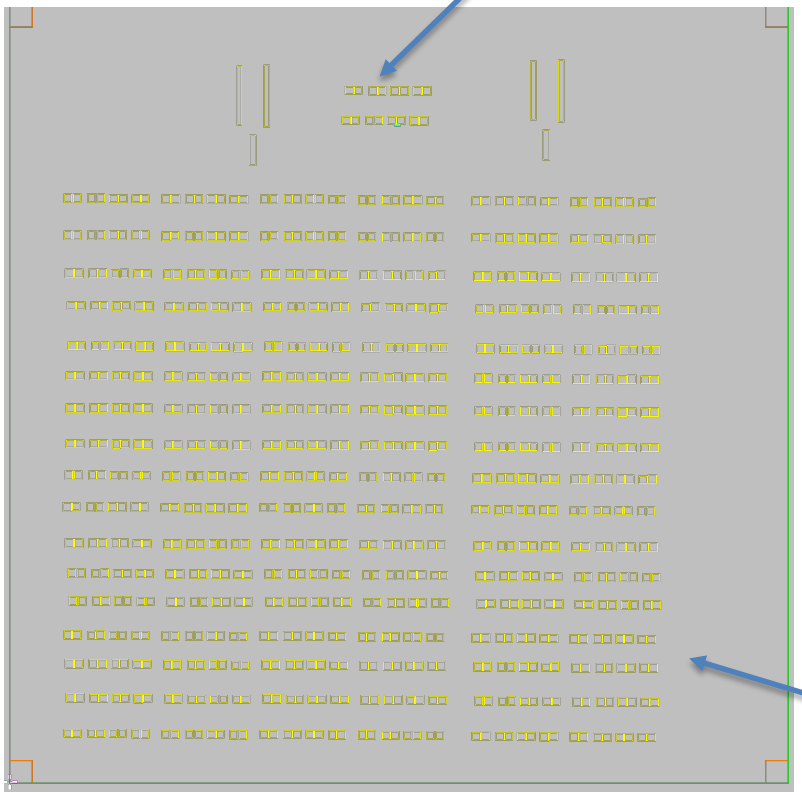
Biristor layout with probe pad



Biristor

Mask Layout of Biristor Array

Resistor testing area

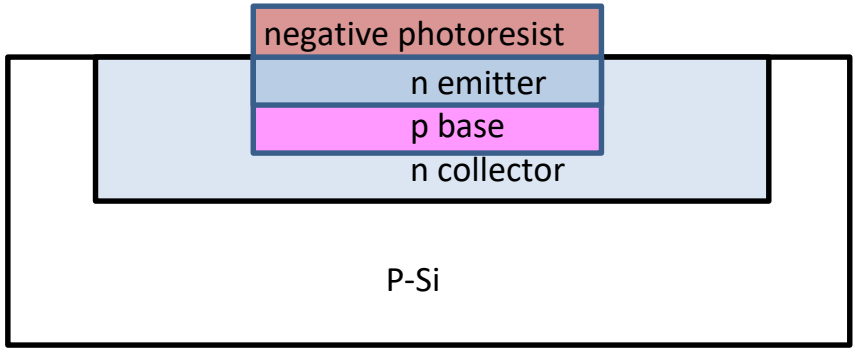


Pillar Dimensions
range from 1.1um to 2.7um

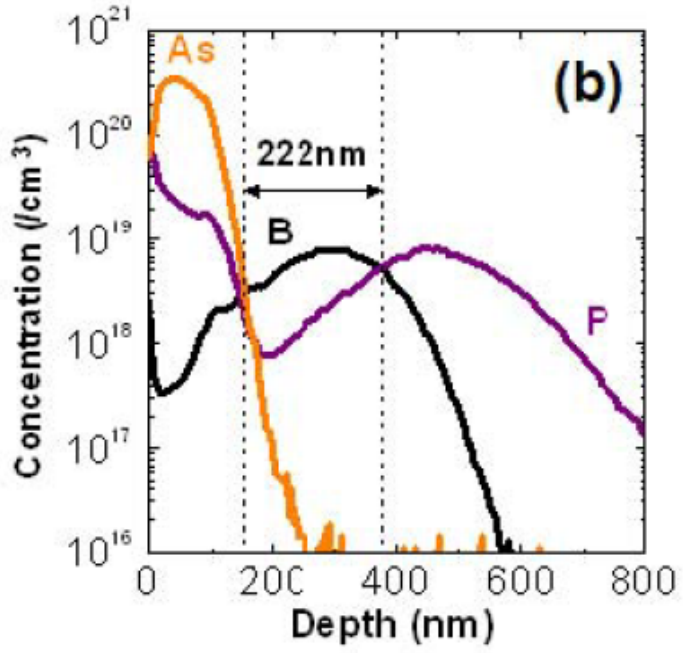
Contact Dimensions are
.5um

Main
Array Area

Ion Implantation Profiles and Etching

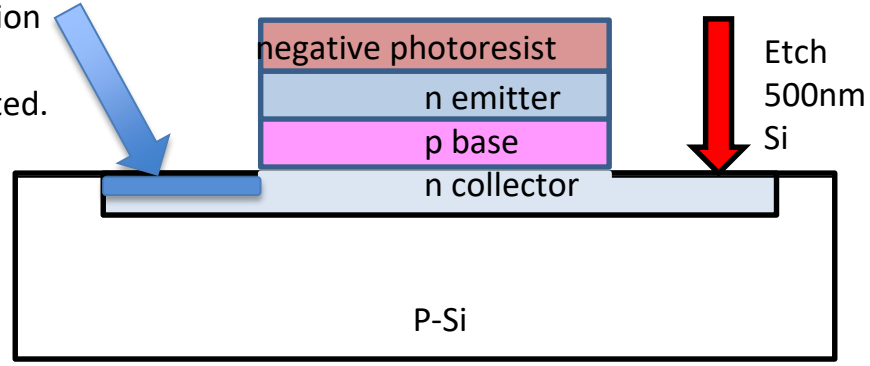


n emitter is Arsenic doped
p base is boron doped
n collector is phosphorus doped



Monolayer Doping was done on two wafers whose fabrication was not completed.

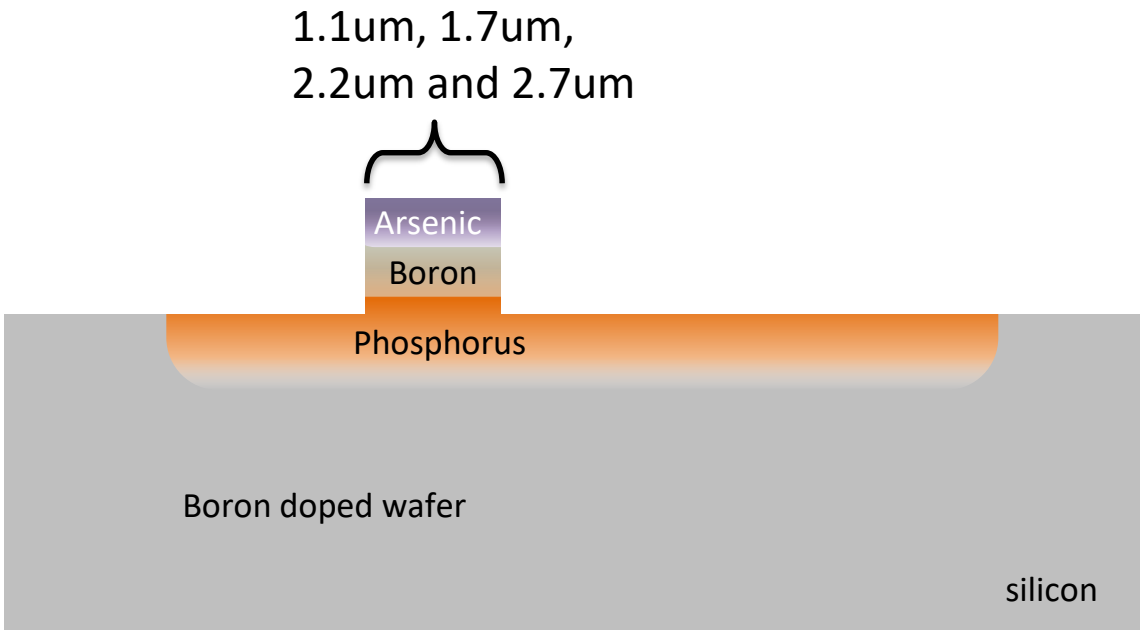
Etch silicon <u>just to reach</u> n type collector ~ 500nm



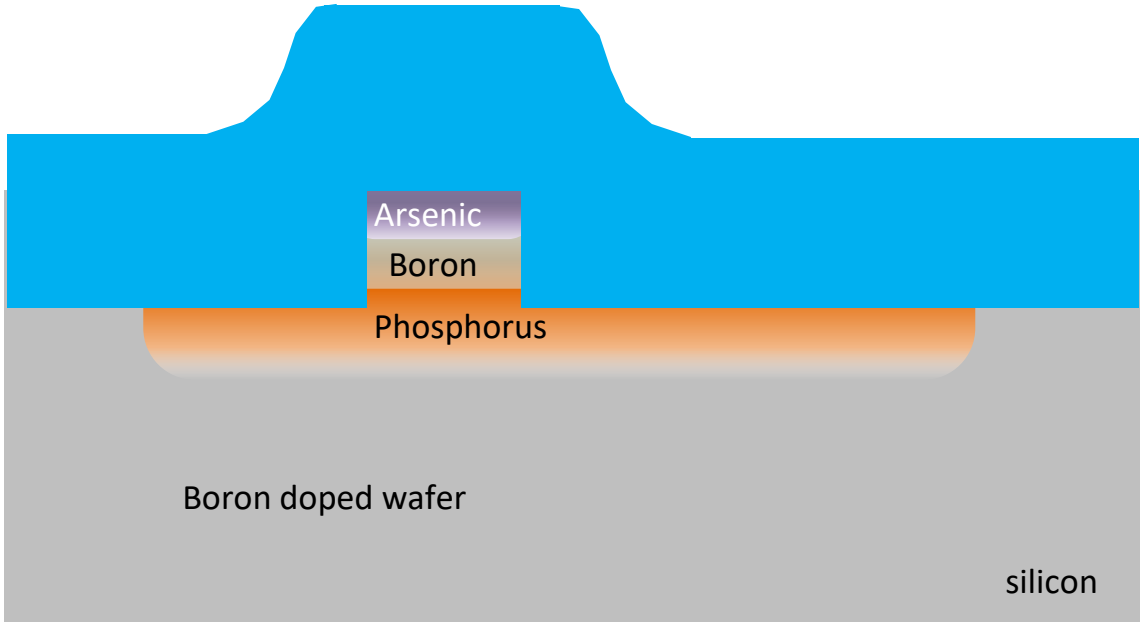
Etch 500nm Si

Etch 500nm Si

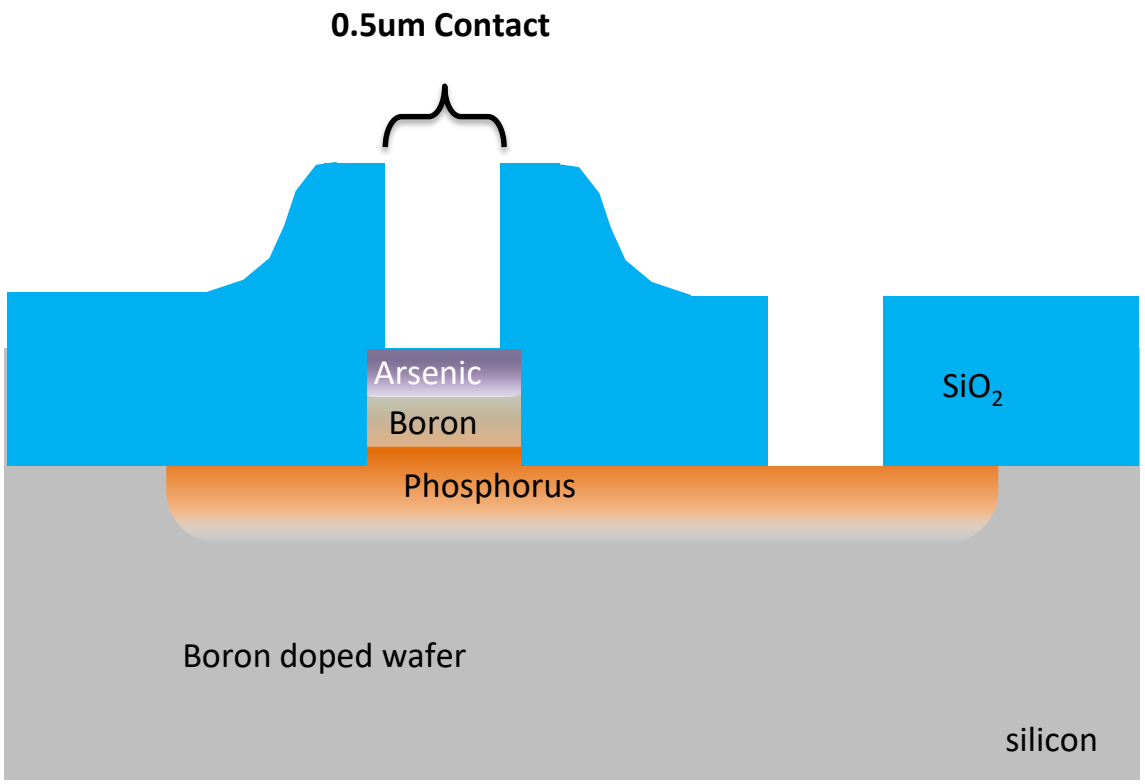
Pillar Structure Formed After Etching



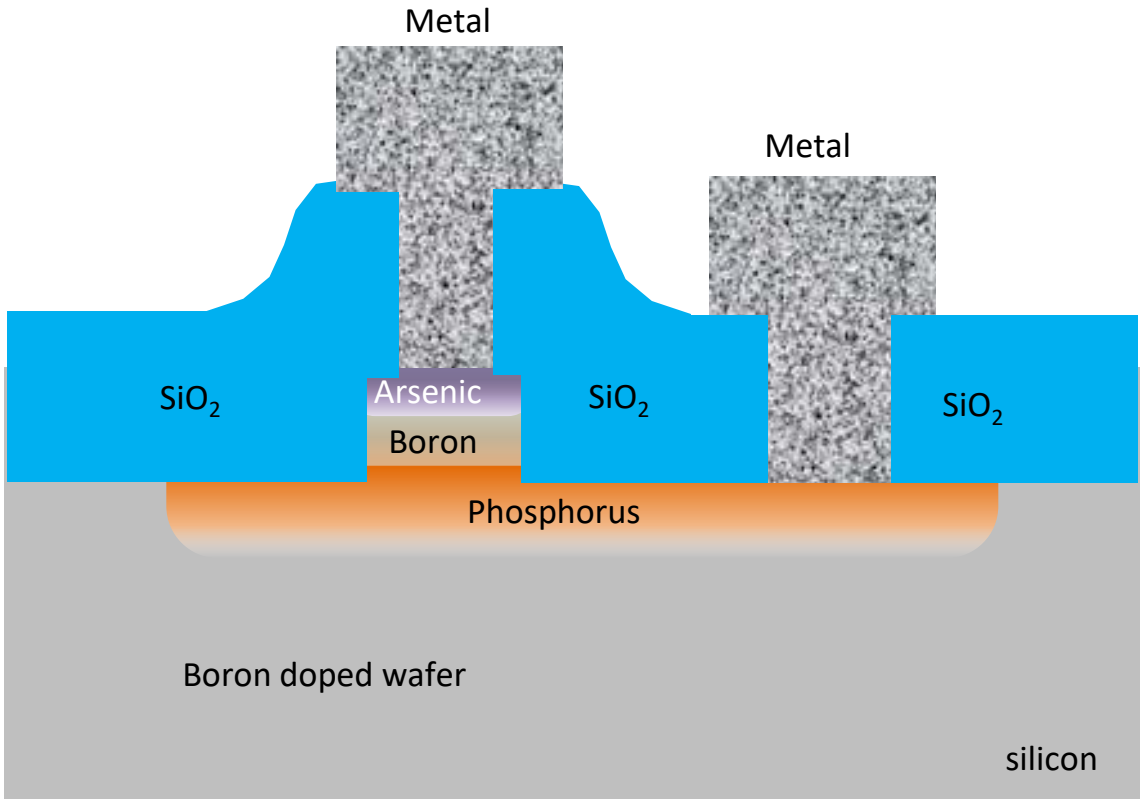
Oxide Deposition Over Pillar



Contact Cuts

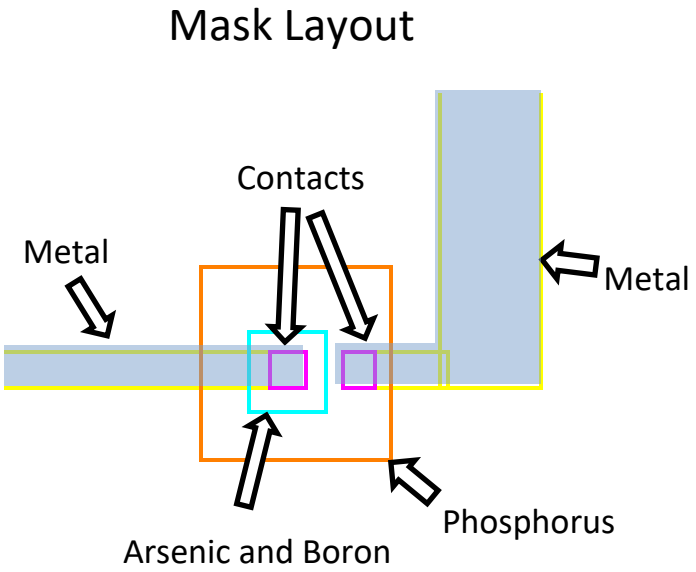


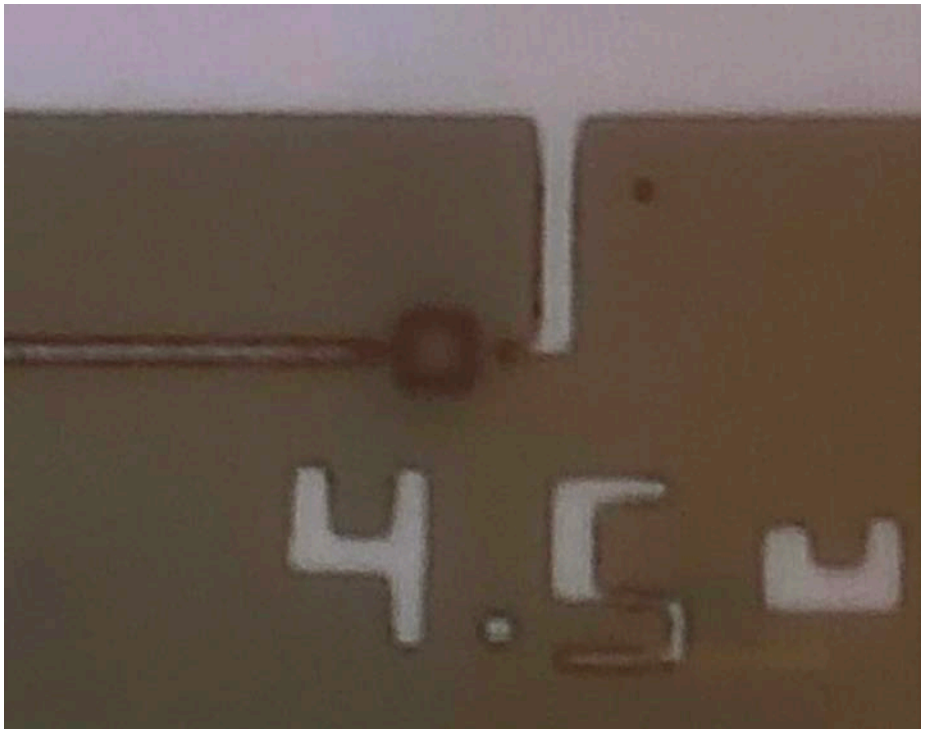
Final Device



Completed Biristor Device

2.7umX2.7um Pillar

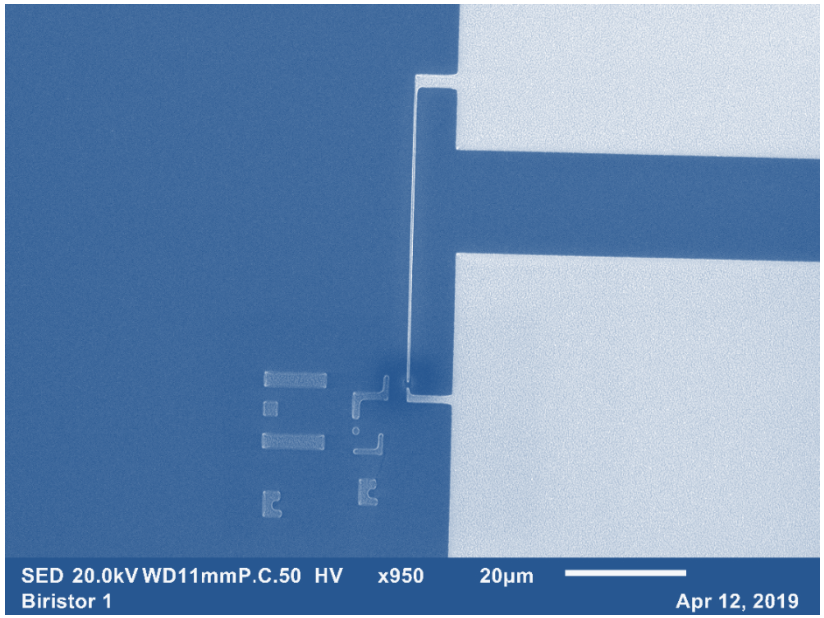


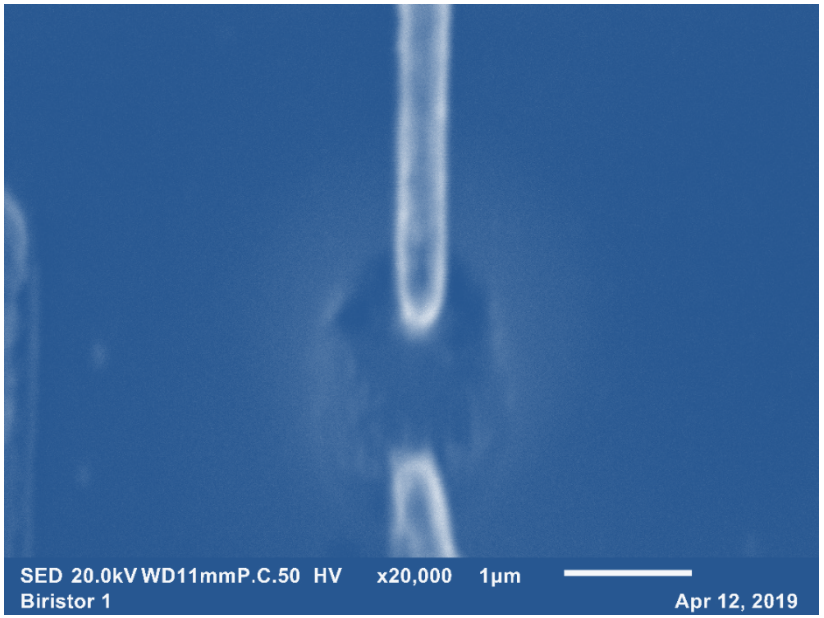


Biristor after the Metal Etch

SEM Micrographs of the Device

1.1um X 1.1um Device

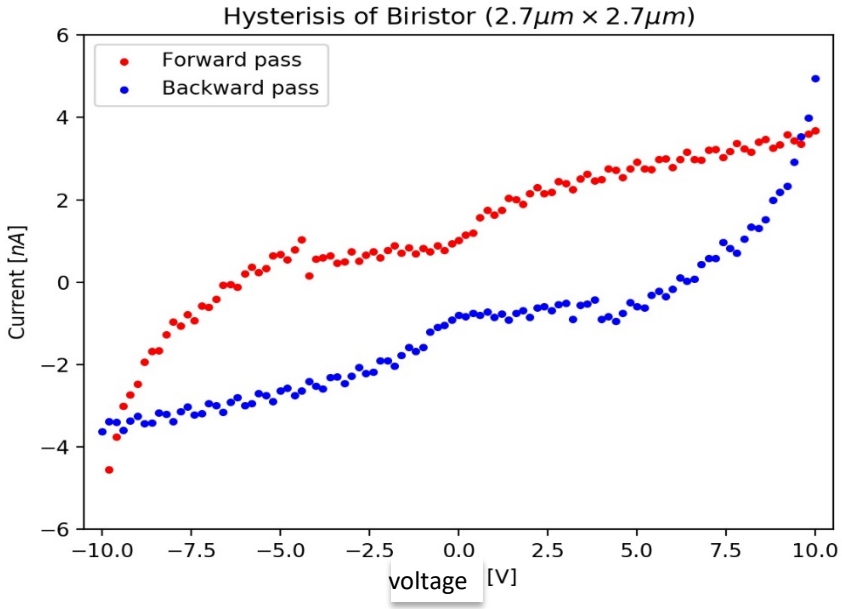


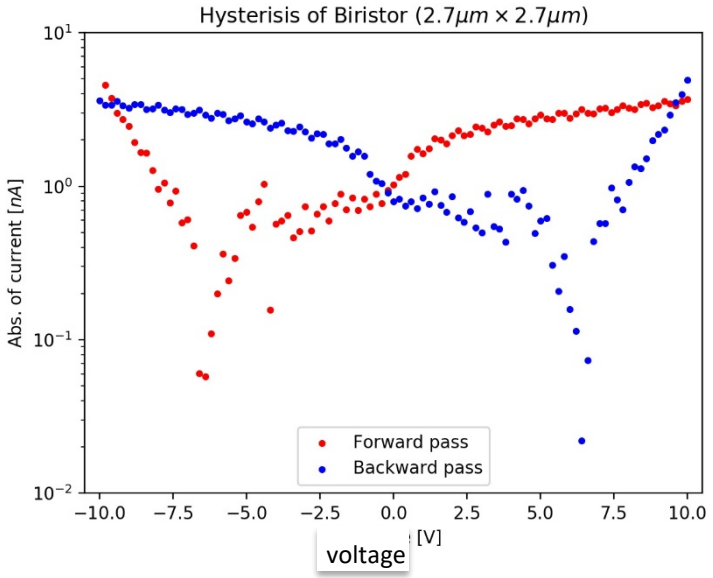


Tool used JEOL JSM-IT100 LA

Courtesy of Bruce E. Kahn, AMPrint Center
Rochester Institute of Technology

Measured I-V Characteristic





Conclusions

- During the process of fabricating the device several obstacles were overcome. Primarily the determination of how to etch the silicon pillars, how to get proper contact cut selectivity when using a dry etch tool and most importantly how to resolve .5um aluminum traces for wires. Additionally the mask design was difficult because design rules had to be determined. Proper probe spacing was achieved without the use of a template.
- Overall, these efforts resulted in a device that exhibited a biristor like I-V curve that displayed path dependent resistance. The reason for this discrepancy is yet to be determined.
- This was the first Biristor made at RIT.

Acknowledgements

- Dr. Kurinec, Dr. Pearson, Dr. Ewbank
- Dr. Jin Woo-Han of NASA AMES (J. Han and M. Meyyappan, "Trigger and Self-Latch Mechanisms of n-p-n Bistable Resistor," *IEEE Electron Device Letters*, vol. 35, no. 3, pp. 387–389, Mar. 2014.)
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