Etching process characterization of Nitride layer and Poly silicon layer using TRION III Etcher

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ABSTRACT

The TRION III etch tool enables us to do a more anisotropic etching of necessary layers such as Nitride and Polysilicon. Therefore proper characterization of the machine is required to be done for better understanding of each parameter and its effect on etching profile.
The characterization of the tool revealed a significant difference in etching performance and parameters compared to our previous established data set from Drytek quad.
It was observed the time for etching for Polysilicon drop by almost 75 percent - which leads us to understand a faster etch rate. In terms of Nitride, it was also seen as better etch uniformity and directionality. The etch selectivity of Nitride test resulted in us understanding how the gas selectively etches the nitride and photoresist. Through this paper better etch recipes can be made for any device fabrication process which will aide in smaller device fabrication and increase in yield across the wafer.

Keywords: TRION, Etching, Selectivity, Etch-Rate

1. INTRODUCTION

As technology is evolving and we are pushing boundaries on how small and efficient our devices get, one of the main challenges that remain is for the technology that enables such process to develop evolves at the same rate. As we are reaching limits on our lithography process, etch recipes become vital and the need of direction Anisotropic etch becomes critical. In this research, the TRION III etcher will be characterized using all of its parameters (gas flow, power, and pressure) to establish recipes for Nitride and Polysilicon layer etch characteristics and profiles.

The key things to consider when doing Characterization of Etcher is to look into the layers Selectivity, etch rate and the pattern. Over the lab process, we were able to change process conditions and get data for etch rate and selectivity. It was seen the power and pressure becomes a key factor when it comes to etching uniformity and profile.

In this research paper Etch selectivity, etch rate and furthermore the combination of factors affecting these parameters for Nitride and Poly-silicon layer will be analyzed for the TRION III etch tool.

2. THEORY

2.1 Etching

Etching in its most basic terms in microelectronic fabrication is a process by which materials selectively removed from the silicon substrate or thin films on the substrate surface.

Etch Parameters
1. Etch rate
2. Etch rate uniformity
3. Etch selectivity
4. Etch profile
5. Etch-Bias

2.1.1 Etch Rate

The rate at which material is removed from the film by an etch process is known as etch rate
The etch-rate is defined by:
Etch rate = thickness-etched/etch-time = ΔT/t

2.1.2 Etch Rate uniformity

This is the measure of the ability of an etch process to etch evenly. It is highly desirable to have highly-uniform etch rates - as this may directly correlate with dying yield in a production operation in a semiconductor Fabrication process.

2.1.3 Etch selectivity

In most Etch process three main materials are being attacked
1. The photoresist mask
2. film being etched
3. the material under the film being etched
Hence during the etch process the difference between how each layer is etched out at which rate under the same Process condition is called selectivity between layers.
S = r1/r2

2.1.4 Etch Profile

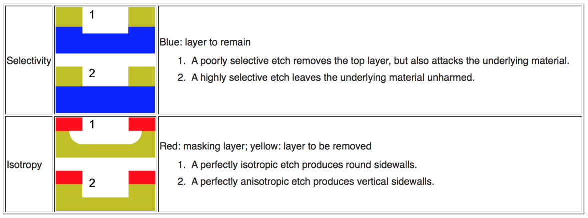
Etching process usually occurs from all direction on a particular film. Therefore the shape at which the process takes place leads to the profile of the layer to differ. When etching process in all directions at that case it is said the process is isotropic on the other hand if the etch process occurs in a unidirectional manner then the

process becomes Anisotropic.
Most wet etch process, and some dry etch process is isotropic while if Anisotropic etch profile is desired its ideal to go with a Dry etch process. Anisotropic etch profiles are becoming highly desirable in the semiconductor industry as the need for smaller nodes and thinner films are desired.

Anisotropy:

$$A = 1 - \frac{\text{Lateral Etch Rate}}{\text{Vertical Etch Rate}}$$

Figure 1. Anisotropy equation



Selectivity	1 2	Blue: layer to remain 1. A poorly selective etch removes the top layer, but also attacks the underlying material. 2. A highly selective etch leaves the underlying material unharmed.
Isotropy	1 2	Red: masking layer; yellow: layer to be removed 1. A perfectly isotropic etch produces round sidewalls. 2. A perfectly anisotropic etch produces vertical sidewalls.

Figure 2. Selectivity and profile

2.1.5 Etch-bias

This is the measure of the Critical Dimension (CD) change after performing a etch process. This is usually caused by isotropic etching and undercutting.

2.1.6 TRION III

In this research we will be using and characterizing the TRION III etcher, This is Dry RIE etching tool which uses RF plasma and gasses to etch target layers selectively. The target layer that will be looked into is the Nitride and Polysilicon layer.
For the Process of plasma etching, an RF glow discharge is created with the power decided. This RF charge created produces chemically reactive species (atoms, ions, etc.) these reactive ions react with the discharged gasses from the inlet and combining react with eh thin film layers to etch them off isotropically or anisotropically.

Figure 3. TRION III RIE Etcher

Figure 4. How Plasma is created for Dry Etching

3. EXPERIMENTAL DETAIL

The experiment setup was divided into two groups based on the Thin Film layer. The first experiment design was designed to characterize the etch process of the nitride layer, and then further testing was done to characterize polysilicon layer.
The process flow setup for the tests was a repeat and learned a method of flow, where after each test was done results were analyzed and understood and further DOE experiments were carried out. The process flow is shown in figure 5 below:

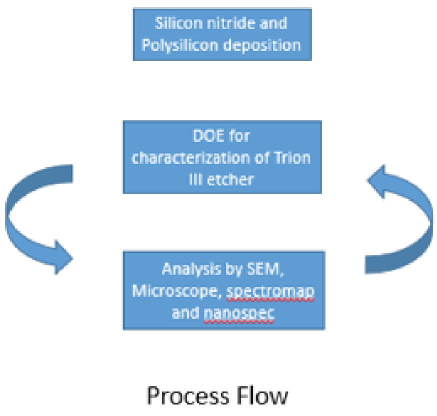


Figure 5. Process flowchart

The substrate stack was similar to both where each wafer was RCA cleaned and oxide layer of around 2500Åwas deposited using the P5000 tool. On top of that 2500Åof nitride was grown and 5000Åof polysilicon was grown using an LPCVD method. Using photoresist and GCA g-Line lithography system some Line space features was exposed and developed and using that line/space was etched into the nitride and polysilicon layer. Figure 6 shows the complete film stack of the process.

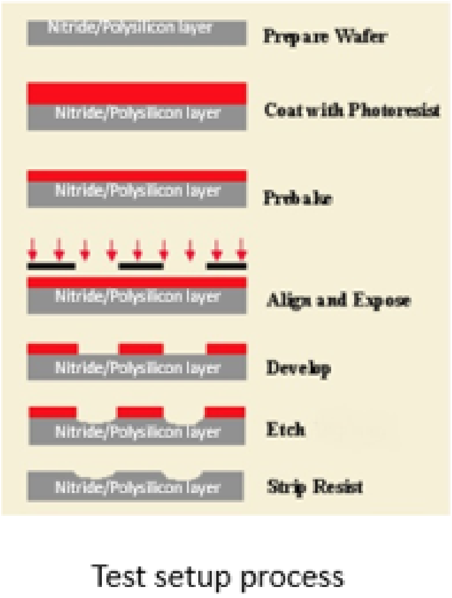
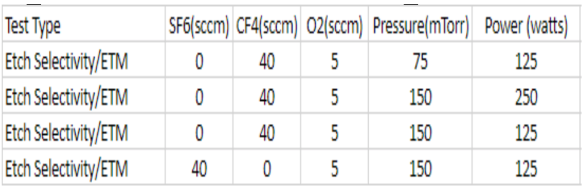


Figure 6. Process layer film stack

3.1 DOE-NITRIDE

One of the central thin film layers in the semiconductor industry for the last decade or so has been Nitride layer on top of oxide. Hence for most general CMOS or device processing, there are many masking layers and nitride layer that requires high degrees of anisotropic and uniform etching. Therefore the main wafer test setup was designed as follows in figure 7. Through these four tests the pressure, power and gas combination was altered to understand the effect of each parameter. The initial recipe was gathered from old SMFL Drytek quad etch tool for these particular layers for baseline recipe. For Nitride test the gases used were CF4, SF6, and O2. while power was varied between 120 to 250 Watts and pressure 75 to 150 mTorrs.

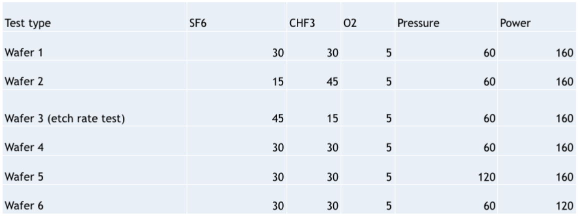


Test Type	SF6(sccm)	CF4(sccm)	O2(sccm)	Pressure(mTorr)	Power (watts)
Etch Selectivity/ETM	0	40	5	75	125
Etch Selectivity/ETM	0	40	5	150	250
Etch Selectivity/ETM	0	40	5	150	125
Etch Selectivity/ETM	40	0	5	150	125

Figure 7. Nitride Test Setup

3.2 DOE-POLYSILICON

Another critical layer in the semiconductor industry for device manufacturing is the Polysilicon layer, and the polysilicon layer has many electrical characteristics that very desirable for device performance. It is also a vital thin film layer for a thin film layer on top of the polysilicon substrate. Therefore the etch process for the Polysilicon layer is also critical in enabling useful device gate contacts and performance.
This process set up the gases used were CHF3, SF6, and O2. The power is ranged from 120 - 160 Watts and pressure 60 - 120 mTorrs.



Test type	SF6	CHF3	O2	Pressure	Power
Wafer 1	30	30	5	60	160
Wafer 2	15	45	5	60	160
Wafer 3 (etch rate test)	45	15	5	60	160
Wafer 4	30	30	5	60	160
Wafer 5	30	30	5	120	160
Wafer 6	30	30	5	60	120

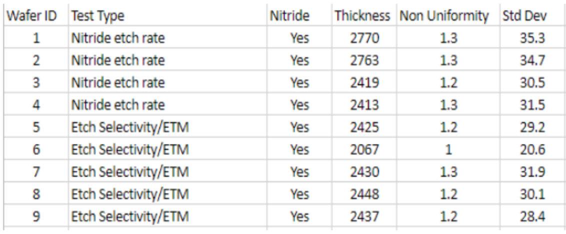
Figure 8. Polysilicon test Setup

4. RESULTS AND DISCUSSION

Initial Deposition data of the layer of interest was measured to check for non-uniformity in thickness. On Top of that, the test was divided between conducting tests of Etch rate, Etch selectivity and further Etch Bias testing.

4.1 NITRIDE DEPOSITION

The nitride Deposition showed good Non-uniformity numbers of around 1.2 percent which is ideal for etching uniformity testing. Nitride was deposited on top of the Oxide layer, and the target thickness was around 2400Å. Below is the table; it shows all the thickness data and per wafer Non-Uniformity Data.



Wafer ID	Test Type	Nitride	Thickness	Non Uniformity	Std Dev
1	Nitride etch rate	Yes	2770	1.3	35.3
2	Nitride etch rate	Yes	2763	1.3	34.7
3	Nitride etch rate	Yes	2419	1.2	30.5
4	Nitride etch rate	Yes	2413	1.3	31.5
5	Etch Selectivity/ETM	Yes	2425	1.2	29.2
6	Etch Selectivity/ETM	Yes	2067	1	20.6
7	Etch Selectivity/ETM	Yes	2430	1.3	31.9
8	Etch Selectivity/ETM	Yes	2448	1.2	30.1
9	Etch Selectivity/ETM	Yes	2437	1.2	28.4

Figure 9. Nitride deposition analysis

4.2 POLYSILICON DEPOSITION

The polysilicon thickness target of 5000Åwas reached for all of the wafers. Therefore the growth using LPCVD recipe was ideal. Although the uniformity between wafers was low, the uniformity in the wafer was not as constant as the growth of our nitride recipe. The Non-Uniformity ranged from 8 percent to 13 percent compared to 1.2 percent of our nitride growth. This is not ideal for Etch rate uniformity test, as the uniformity pattern stays between stacks of a thin film.

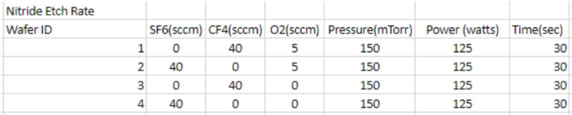
Wafer ID	Test Type	polysilicon	Thickness A	Non Uniformity	Std Dev
1	Etch Selectivity/ETM	Yes	4968	8.84	439
2	Etch Selectivity/ETM	Yes	4805	9.13	439
3	Etch Rate test	Yes	5157	11.5	594
4	Etch Selectivity/ETM	Yes	4830	9.97	481
5	Etch Selectivity/ETM	Yes	4954	10.1	501
6	Etch Selectivity/ETM	Yes	5019	12.59	632

Figure 10. Polysilicon deposition analysis

4.3 ETCH RATE

4.3.1 NITRIDE

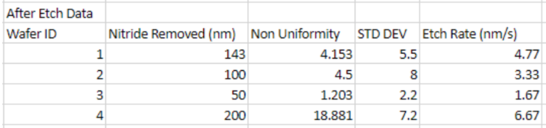
The Etch rate was calculated using the initial thickness data, and the after etching thickness data, using the time of etching we calculated the etch rate for all the conditions. The Etch plan set up for blank wafers is shown in figure 10:



Nitride Etch Rate						
Wafer ID	SF6(sccm)	CF4(sccm)	O2(sccm)	Pressure(mTorr)	Power (watts)	Time(sec)
1	0	40	5	150	125	30
2	40	0	5	150	125	30
3	0	40	0	150	125	30
4	40	0	0	150	125	30

Figure 11. Bare wafer etch plan

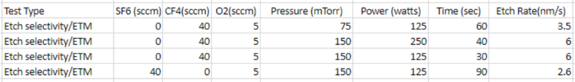
The etch rate that was achieved for bare nitride grown wafer was as follows:



After Etch Data				
Wafer ID	Nitride Removed (nm)	Non Uniformity	STD DEV	Etch Rate (nm/s)
1	143	4.153	5.5	4.77
2	100	4.5	8	3.33
3	50	1.203	2.2	1.67
4	200	18.881	7.2	6.67

Figure 12. Nitride base etch data

The nitride etch was also collected on patterned wafer as shown below:



Test Type	SF6 (sccm)	CF4(sccm)	O2(sccm)	Pressure (mTorr)	Power (watts)	Time (sec)	Etch Rate(nm/s)
Etch selectivity/ETM	0	40	5	75	125	60	3.5
Etch selectivity/ETM	0	40	5	150	250	40	6
Etch selectivity/ETM	0	40	5	150	125	30	6
Etch selectivity/ETM	40	0	5	150	125	90	2.6

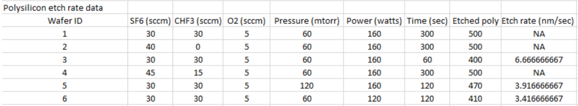
Figure 13. Patterned wafer etch data

The etch data shows how the O2 helps with controlling the etch rate, and the CF4 carbon atoms help with breaking down the nitride layer compare to the SF6 gas combination.
When using O2 uniformity is better allthroughout the wafer. The etch rate is better in both CF4 gas recipes. With SF6 the consistency and etch rate becomes pretty highly uncontrollable.

It can be seen the etch rate differ between unpatterned and patterned wafer. With the patterned wafer, it can also be seen that lower the pressure the more controlled the etch rate is (slower) while power gives more etch rate and directional etch. Overall the etch rate decreases due to the increase in surface area from the patterned features.

4.3.2 POLYSILICON

The polysilicon Etch recipe was established from previously logged data from SMFLs Drytek Quad Etcher. The data showed a considerable difference in ETCH rate in comparison. The Etch rate time changed from the already established time of 5 minutes for 5000Åof polysilicon to around 2 minutes. This could be related to the chamber size and better RIE contacts, etc. Below is shown the data for the etch rates.

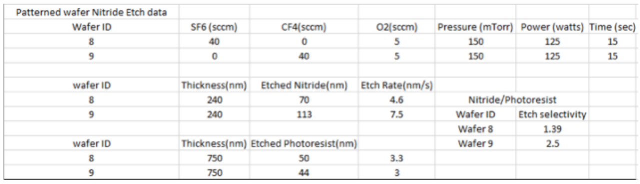


Polysilicon etch rate data								
Wafer ID	SF6 (sccm)	CHF3 (sccm)	O2 (sccm)	Pressure (mtorr)	Power (watts)	Time (sec)	Etched poly	Etch rate (nm/sec)
1	30	30	5	60	160	300	500	NA
2	40	0	5	60	160	300	500	NA
3	30	30	5	60	160	60	400	6.666666667
4	45	15	5	60	160	300	500	NA
5	30	30	5	120	160	120	470	3.916666667
6	30	30	5	60	120	120	410	3.416666667

Figure 14. patterned wafer polysilicon etch rate

4.4 ETCH SELECTIVITY NITRIDE

Etch selectivity test was carried out on the wafer with exposed serpentine motion blocks of clear exposer. This resulted in an open field and close field checkerboard pattern allowing us to analyze photoresist to nitride etch selectivity and rates. Below is shown the data for the etch selectivity between the layers.



Patterned wafer Nitride Etch data						
Wafer ID	SF6 (sccm)	CF4(sccm)	O2(sccm)	Pressure (mTorr)	Power (watts)	Time (sec)
8	40	0	5	150	125	15
9	0	40	5	150	125	15
wafer ID	Thickness(nm)	Etched Nitride(nm)	Etch Rate(nm/s)			
8	240	70	4.6	Nitride/Photoresist		
9	240	113	7.5	Wafer ID	Etch selectivity	
				Wafer 8	1.39	
wafer ID	Thickness(nm)	Etched Photoresist(nm)		Wafer 9	2.5	
8	750	50	3.3			
9	750	44	3			

Figure 15. Etch selectivity analysis

The etch selectivity data shows how with SF6 O2 combination the etch selectivity is close to one which is ideal for layer etching as the rate is the same.

4.5 ETCH MICRO-GRAPHS

The Nitride Etch micro-graphs show how the line/space etching and imaging are pretty anisotropic and clear all through the thin film especially at 1.0um features. It can is seen that the etch does some undercutting on the nitride layer when the photoresist is on top.

1.png

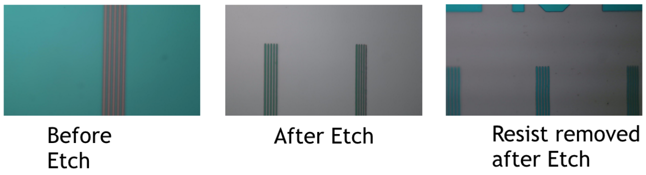


Figure 16. Nitride Etch Micro-graphs

The polysilicon wafer Micro-graphs show over etches in wafer 1 and 2 and 4 due to using the previously established recipe and over-etching to 5 min. wafer 3, 5 and 6 give us a etch rate data and the effect of different gas power and pressure combination.

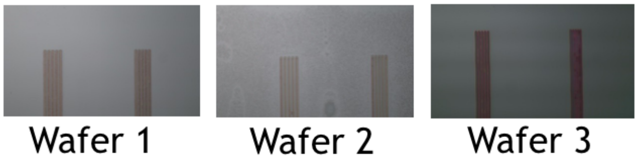


Figure 17. After etch image of 1.4 and 1.6 um L/S

Figure 18. After etch image of 1.4 and 1.6 um L/S

5. CONCLUSION AND FUTURE WORK

Through this research work, a greater understanding of the TRION III etcher was achieved, with this data new recipes can be made for better device fabrication which will yield in better yield.

It was observed that the methods differ profoundly compared to previous Drytek recipes and initial nitride data and Micrograph imaging promises desirable anisotropy which will be beneficial for smaller device fabrication.

The Nitride data showed a substantial effect on the combination of gas, O2 percentage plays an important on the Etch rate and pressure.

While in terms of Polysilicon rate, The power plays a big part in the etch recipe with similar effect due to combination of gases. Etch rates in both cases were faster compared to our previous established baseline recipe from the Drytek tool.

Future work on this characterization needs to take place where the Profile of the etched wafer needs to be checked using SEM and cross-sectional imaging.

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REFERENCES

1. https://people.rit.edu/lffeee/MCEE550.htm. *CMOS processing slide*. Lynn Fuller, RIT, Rochester, NY.
2. S.WOLF. *Microchip manufacturing* []. S.WOLFk, ISBN 0-9616721-8-8, 1995.
3. SMFL *LPCVD files* []. Recipes for LPCVD
4. Etching (microfabrication), wikipedia `https://en.wikipedia.org/wiki/Etching`$_{m}icrofabrication$

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