Fabrication of Photonic LPCVD Silicon-Nitride Waveguides

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Abstract — The purpose of this project was to develop a repeatable process flow for Silicon-Nitride optical waveguides at RIT. Previous projects have fabricated optical waveguides out of amorphous silicon and polymers but never out of Nitride. The grating coupler pitch was varied from 700nm to 1500nm and the length was varied from 100µm to 1000µm. A target Nitride deposition thicknesses of 250nm, 500nm, and 750nm were deposited through LPCVD methods and were measured to be 150nm, 450nm, and 770nm. The thicknesses were chosen to be half the waveguide width for optimal transmission. Fabrication was successful for all three waveguide widths on the 450nm and 770nm thick Nitride wafers for both the Loopback and Ring Resonator designs. The grating couplers were able to resolve with pitches of 900nm to 1500nm but the 800nm pitch and under were overexposed and did not develop.

Optical testing was unable to be performed due to test setup being broken at the end of fabrication. Instead simulations of the test setup were done to see the optimal transmission for the 450nm thick and 1000nm wide Nitride grating coupler and waveguide. The test setup can vary wavelength from 1500nm to 1600nm so optimal transmission should have been about 1550nm. The best transmission results came from the tester head at an angle of 24 degrees and the grating coupler pitch of 1300nm showing a peak at the 1500nm wavelength.

Keywords — Photonics, Silicon-Nitride, LPCVD, Waveguide, Integrated Photonics.

I. INTRODUCTION

As conventional electrical components are getting smaller, the electrical interconnects are nearing power consumption limits. Transistors have gotten to the point where they take up most of the room in a limited die area. There are many opportunities being explored for the next generation of electronics including FinFET fabrication, carbon nanotubes, III-V semiconductors, and photonics.

One of the possible areas of exploration is in photonics. Photonics is a study of optical physics focusing on the detection and transmission of light. Nothing moves faster than the speed of light, which makes photonics an ideal replacement for conventional electronics. Photonics, however, cannot replace traditional electronics completely due to how much space it takes up. Photonics and electronics can be incorporated together to get the best of both in the case of photonic integrated circuits. The RIT SMFL has shown the capability of being able to fabricate waveguides from amorphous silicon and polymer materials. Silicon-Nitride waveguides have only been fabricated one other time at RIT and were used for MEMS evaluations. These waveguides were not optimized, and the quality of the waveguide was not inspected for photonic use. Nitride is an ideal material for use in waveguides because it offers lower optical loss, better coupling, and better power handling capabilities over the previously mentioned materials.

II. THEORY

Waveguides function off the principle of total internal reflection. Total internal reflection is when a beam of light shone into a prism, in this case the waveguide, reflects off internal surfaces and allows very little light to escape.

Due to the total internal reflection, light follows the shape of the waveguides from the input grating coupler to the output grating coupler. This allows the test setup to measure the transmission and loss through the waveguide. A waveguide could be designed as a long, straight line but the curved shape takes up less room and can be measured with the test setup at RIT.

For this project there were two waveguide designs created. The loopback waveguide design can be seen in **figure 1** and the ring resonator waveguide can be seen in **figure 2**. The loopback waveguide is a basic waveguide that guides photons from one end to the other. The ring resonator design adds onto this design by the incorporation of the ring at the top of the curve. This allows for coupling to decrease the transmission through the main waveguide.



Figure 1. Shows Loopback Waveguide design for width of 500nm and grating coupler pitch of 700nm and 300nm taper.



Figure 2. Shows Resonator Waveguide design for width of 1500nm and grating coupler pitch of 1400nm and 200nm taper.

This project focuses on the fabrication of optimal LPCVD Silicon-Nitride waveguides with the tools available in the RIT SMFL cleanroom. This means there was not a lot of simulation work done to get the best results. Instead, a 20mm by 20mm mask was created with the two waveguide designs each with slightly different variations. The largest variation came from changes in the grating coupler where the pitch was changed from $0.7\mu m$ to $1.5\mu m$ and taper length was changed from $100\mu m$ to $1000\mu m$. The mask design can be seen in **figure 3**.



Figure 3. Shows mask design wave waveguide and grating coupler variations.

III. EXPERIMENT

The fabrication process for the LPCVD Nitride waveguides follows a similar flow to the amorphous silicon waveguides typically fabricated at RIT. The main modifications that needed to be made to this process was in the deposition step because LPCVD Silicon-Nitride was used instead of amorphous silicon and other minor steps based on the tools that were available at the time of fabrication. A detailed outline of each step can be found in the following subsections.

1. RCA Clean

The first step in the waveguide fabrication process was to obtain wafers. This were brand new blank wafers from the manufacturer. Typically, the type of wafer, n-type or p-type, should be considered but was not since this process does not involve any implant steps. These wafers were sitting around for an unknown amount of time and needed to go through the standard RCA clean. This clean was done to remove any organic or metal particulates that may be left on wafer surface and to remove any native oxide that formed while they were sitting around.

Si Substrate

Figure 4. Shows Cleaned Silicon-Substrate.

2. TEOS Oxide Deposition

The next step for processing that was performed was an oxide deposition. $2\mu m$ of TEOS Oxide was deposited on the silicon substrate to isolate the waveguides from the substrate as being too close to the substrate would result in high loss from the waveguides. The oxide was deposited on both sides of the wafer because it was also used to pad the Nitride and reduce the stress from lattice mismatch. A thick (> $2\mu m$) thermal oxide growth would be more optimal for uniformity reasons but due to diminishing marginal returns of the Bruce Tube Oxidation furnaces at RIT and the amount of time it would have taken, TEOS deposition was done in the ASM P5000 instead.



3. LPCVD Silicon-Nitride Deposition

Following the oxide deposition step, the LPCVD furnace was used to deposit Silicon-Nitride on both sides of the wafer. Nitride was deposited in three separate runs each with two wafers to get different thicknesses: $0.25\mu m$, $0.5\mu m$, and $0.75\mu m$. These different thicknesses were desired to be half of the waveguide line width.



Figure 6. Show wafer cross section following LPCVD Nitride Deposition.

The thinnest Nitride run's deposition time was incorrectly calculated and ended up only being 0.19μ m thick, the second run had a thickness of 0.45μ m, and the thickest Nitride tried to compensate for the deposition rate and ended up being 0.77μ m

thick. All the depositions were done using Dr. Lynn Fuller's Low-Pressure Nitride recipe. The details for each step in the recipe can be found in the back of the manual for the LPCVD tool.

4. Photoresist Coat

Prior to exposure on the ASML stepper, positive AZ MiR 701 photoresist was coated on the Silicon-Nitride. This photoresist was used to transfer the photomask image of the waveguide designs onto the wafer. The photoresist was coated using recipe one on the SVG 2 Track. This recipe coats a 0.925 μ m thick layer of photoresist and does an edge bead removal step. This thickness of photoresist was thick enough to block the waveguides from being etched in the sixth step.



Figure 7. Shows wafer cross section following Photoresist coat.

5. ASML Stepper Exposure

Most of the exposures done in the ASML stepper are done on materials such as Silicon-Dioxide or something with a similar refractive index. Silicon-Nitride has a much higher refractive index so the usual exposure dose of 275mJ/cm^2 was going to be too high to get the desired $0.5 \mu \text{m}$ or smaller resolution. To get an idea of the proper dose, a Focus-Exposure-Matrix was performed sweeping from a dose of 175mJ/cm^2 to 375mJ/cm^2 and a focus of $-1 \mu \text{m}$ to $+1 \mu \text{m}$. The best exposure dose was found to be 185mJ/cm^2 with a focus of $0 \mu \text{m}$.



Figure 8. Shows wafer cross section following AMSL exposure and develop.

Following develop on the SVG 2 Track, it was noticed that there was poor adhesion of the photoresist for the smaller features. This was thought the be a problem with the HMDS prime. Upon further inspection is was confirmed not to be a problem with the HMDS primer on the SVG Track but instead due to surface roughness of the Nitride. The photoresist was removed using the solvent strip bench and recoated on the SVG Track. The chemical removal of the photoresist was enough to make the surface less rough and promote adhesion of the photoresist during the second coat.

6. Silicon-Nitride Etch

There are plenty of tools in the lab capable of etching Nitride such as the LAM 490 that uses endpoint detection, the Trion Etcher, or the new Trion Phantom 3 Etcher. The Trion Phantom 3 Etcher was chosen to be used due to another student's project being on characterization of the etch, the ease of use for the tool, and that it was made by the same company that made the PECVD Nitride deposition tool that is being brought up and running. A standard Nitride etch recipe was used with the parameters as follows: Pressure = 150mT, RF Power = 125W, Process Time = Varies, CF4 Flow = 40sccm, SF₆ Flow = 0sccm, O₂ = 5sccm, and CHF₃ Flow = 0sccm.



Figure 9. Shows wafer cross section following Nitride etch.

7. Photoresist Strip

Typically, the GaSonics Asher is used to remove photoresist, however this tool was down due to an RF power problem. This means photoresist either needed to be removed using an O_2 plasma in another tool such as the Trion Phantom 3 or the LAM 490, or it could be removed chemically with acetone or other chemicals. Chemical removal of the photoresist was chosen based on it being a well-developed process in the lab. Specifically, the Solvent Strip bench that uses Baker PRS-2000 resist stripper was used to remove the photoresist.



8. TEOS Cladding Deposition

Due to the thermal budget, a thermal oxide could not be grown for this coating. Instead, TEOS deposition was performed again in the ASM P5000. There were two depositions done for this step. The first deposition was done to fill in the gap where Nitride was etched, the second deposition was another 2μ m oxide deposition. This resulted in a slightly higher Oxide thickness over the waveguides themselves, but this difference was not enough to make a significant impact on device performance. Once the cladding was deposited, the waveguides were ready for testing.



Figure 11. Shows wafer cross section following TEOS Cladding deposition.

IV. RESULTS AND DISCUSSION

The biggest challenges during fabrication were the need for an FEM to optimize exposure dose, a confirmation of the etch rate for the new Trion Phantom 3 tool, and fixing the resist adhesion problem following the first coat and exposure. Luckily these problems were not detrimental to the completion of this project.

A microscope capture of the FEM can be seen in **figure 12**. This FEM showed the best exposure dose for the film stack was with 185mJ/cm^2 and a focus offset of 0μ m. The resist problem was fixed after a surface preparation step was completed and the substrate was recoated. The adhesion problem can be seen in **figure 13**. Due to another student's project being on characterization of the etching tool, the etch rate was easily confirmed.



Figure 12. Shows Microscope capture of FEM to get correct exposure dose to resolve 0.5µm lines.



Figure 13. Shows photoresist adhesion problem with 0.5µm lines.

Following the photoresist adhesion problem, there were no major problems that were encountered. The etching step and the oxide deposition step were completed without a hitch. Upon visual inspection fabrication showed the 500nm wide loopback waveguides were easily resolved as seen in **figure 14**. Zooming in on the grating coupler showed consistent resolution for the 1000nm pitch coupler as seen in **figure 15**. Some smaller pitch couplers were also able to be resolved but it was hit-or-miss if the result was consistent.



Figure 14. Shows fabricated loopback design with $1.5\mu m$ wide waveguide and grating coupler pitch of $1\mu m$ and $400\mu m$ taper.



Figure 15. Shows microscope capture of grating coupler with 500nm lines and 500nm spaces.

Both waveguide designs were fabricated and showed good resolution. The ring resonator waveguide can be seen in **figure 16**. One of the reasons the ring resonator design was included in this project was to confirm the ability to resolve smaller features than 500nm. Inspection of the grating couplers showed there was inconsistency in the resolution of smaller lines. Inspection of the gap between the waveguide and the ring resonator showed spaces of less than 500nm could be resolved as seen in **figure 17**. Previous projects had trouble being able to resolve the 300nm gap that was chosen but the exposure dose, film stack, and etching chemistry chosen for this project was able to do so. Three factors were changed so it is unclear which of the three factors had the largest impact.



Figure 16. Shows fabricated ring resonator design with 0.5µm wide waveguide and grating coupler pitch of 1µm and 300µm taper.



Figure 17. Shows microscope capture of 300nm gap between ring resonator and waveguide.

Unfortunately, at the end of the waveguide fabrication, the test setup was broken so no physical testing of the waveguides could be done. Instead simulations using the actual fabricated numbers were performed. Two main simulations were run including: varying the angle of incidence of the test head and varying the grating coupler pitch.

Simulation of the angle of test head showed as angle increased, the transmission also increased but for a shorter wavelength as seen in **figure 18**. Since the tester can sweep from a wavelength of 1500nm to 1600nm the highest transmission in this range was chosen to be the ideal transmission. The simulation showed highest transmission came from a 23-degree angle for the wavelength of 1500nm. **Table 1** shows a summary of the varied angle simulations noting the maximum transmission, optimal wavelength, and transmission at the 1500nm wavelength.



Figure 18. Shows simulation results for transmission versus wavelength when varying test head angle.

	Max Transmission	Optimal Wavelength	Transmission at 1500nm
20 °	0.15	1530nm	0.13
21 °	0.17	1520nm	0.16
22°	0.19	1510nm	0.18
23°	0.20	1500nm	0.20
24 °	0.21	1490nm	0.20
25°	0.22	1480nm	0.20

Table 1. Summary of simulation results for angle variation.

Varying the grating coupler pitch provided the largest difference in results. Transmission was approximately the same for different pitches just centered at different wavelengths. Targeting the 1500nm wavelength showed highest transmission for the 1300nm pitch grating coupler. The simulation results can be seen in **figure 19**. **Table 2** shows a summary of the varied grating coupler pitch simulations noting the maximum transmission, optimal wavelength, and transmission at the 1500nm wavelength.





Table 2. Summary of	f simulation	results for	grating	coupler
	pitch variat	tion.		

	Max Transmission	Optimal Wavelength	Transmission at 1500nm
1.1µm Pitch	0.10	1400nm	0.04
1.2µm Pitch	0.20	1435nm	0.1
1.3µm Pitch	0.21	1500nm	0.21
1.4µm Pitch	0.14	1560nm	0.1
1.5µm Pitch	0.17	1660nm	0.05

After the grating coupler simulations were finished, one last simulation was run to see the transmission through the waveguide itself. An Eigenmode solution was generated to show that using Nitride as the waveguide material is truly a low loss material. The simulation as run using the 0.45μ m thick and 1μ m wide waveguide measurements from actual fabrication and an oxide cladding of 1.9μ m on both sides of the waveguide to get the result in **figure 20**. This figure shows most of the transmission is in the waveguide with only a bit of loss around the edges of the Nitride.



Figure 20. Shows simulated waveguide transmission.

V. CONCLUSIONS

A LPCVD Silicon-Nitride waveguide fabrication process has been successfully established for the tools available in the RIT SMFL cleanroom. Unfortunately, this project was unable to confirm if this process flow produces working waveguides due to the test setup not being available for optical testing.

Theoretically, the results from this project show when targeting the 1500nm wavelength, the best transmission will come from the loopback waveguide that is 1000nm wide, 500nm thick under the conditions where the tester head angle of 23-degrees and a grating coupler pitch of 1300nm

This project can be expanded on through simulations of all the waveguide designs to compare actual performance to theoretical performance. The waveguides can also be changed from a static waveguide to a dynamic waveguide through methods like the incorporation of a thermo-optic tuner.

ACKNOWLEDGMENTS

My advisors, Dr. Preble, Dr. Pearson, and Dr. Ewbank for guidance and help whenever a roadblock was encountered. Matt Van Niekerk for helping with simulations. Dr. Puchades for help with process development. Stephanie Bolster, Tim Blier, Ky-El Sanchez for teaching me about the tools. Patricia Meller, Sean O'Brien, and John Nash for helping me get certified on tools. The SMFL Staff for their tool knowledge and assistance. Dr. Pearson and Dr. Kurinec for starting wafer substrates. Dr. Fuller for his LPCVD Nitride Recipes and the other recipes developed over the years.

REFERENCES

- [1] P. Cadareanu, "Silicon Photonic Devices Manufactured Using Double Patterned i Line Lithography," rep.
- [2] Venkatesh Deenadayalan, Unpublished.