Enhanced Boron Activation in Xenon Flash Lamp Annealed Polysilicon Through Pre-Amorphization

Adam Rosenfeld, Glenn Packard, and Karl Hirschman

***Abstract*—Thin film transistors were fabricated to investigate the influence of the addition of a fluorine preamorphization implant on boron activation in the source/drain. The addition of the fluorine resulted in a higher drive current for high dose implants ($5x10^{15}$ cm^{-2}). The higher current as well as an increased calculated mobility supports the hypothesis that fluorine implant increases boron activation. Device performance was noticed to be dependent on its location on the wafer complicating experimental analysis. Additional system control would allow for more direct treatment comparisons.**

***Index Terms*—TFTs, FLAPS, Dopant Activation**

I. Introduction

THIN film transistors (TFTs) are an integral part of flat panel displays. They make up the backplane, which controls the switching of individual display pixels. The backplane applies a voltage to the liquid crystal for LCD displays or applies a current to the organic light emitting diode for OLED displays. Currently most TFTs are made from hydrogenated amorphous silicon (a-Si:H). These TFTs have an electron channel mobility of less than 1 $cm^2/(Vs)$ and are limited to NMOS only.

Amorphous silicon cannot meet the requirements for next generation displays. A higher mobility material is required for the increased pixel density and refresh rates demanded. Additionally, if the replacement material is CMOS compatible, external circuitry could be incorporated directly onto the backplane. One promising material is flash lamp annealed polysilicon (FLAPS). FLAPS TFTs have been shown to have high mobility and CMOS compatibility [1].

II. Theory

Flash lamp annealing polysilicon is a process to convert amorphous silicon on a glass substrate to polycrystalline material using a microsecond timescale pulse from a broad spectrum xenon flash bulb. The emission spectrum of the xenon flash bulb and the absorption spectrum of amorphous silicon are shown in Figure 1. The silicon film absorbs the light from the pulse, rapidly heating and melting, while the glass substrate minimally absorbs the pulse and stays below its thermal limit. The silicon rapidly cools and recrystallizes, forming polycrystalline material. An example of FLAPS is shown in Figure 2.

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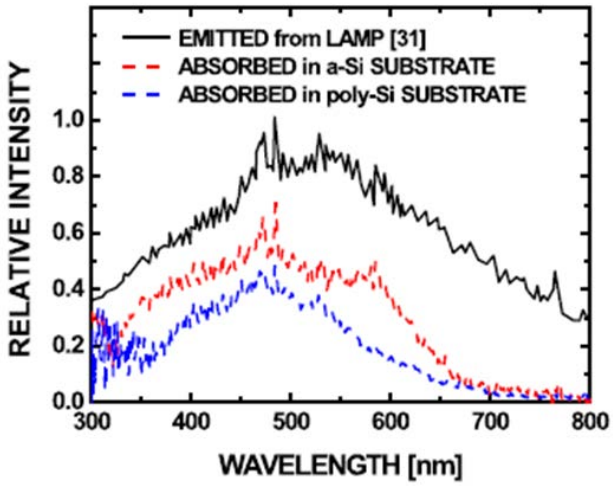

Fig. 1. Emission spectrum of xenon flashbulb and a-Si absorption spectrum [2]

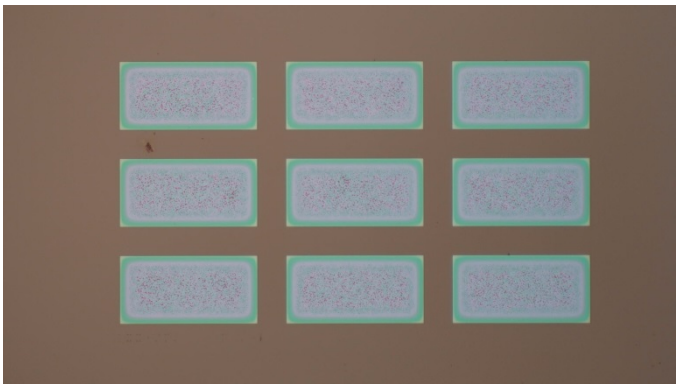

Fig. 2. FLAPS crystalized mesas

There are many different factors that determine the morphology of the polysilicon. These factors include mesa size, proximity between mesas, and degree of disorder of the starting silicon. Previous work has shown that there is maximum mesa size that can be crystallized uniformly. Additionally, the proximity of the mesa to neighboring mesa as well as position within larger arrays was noted to influence crystallization [3]. The degree of disorder also impacts the temperature at which the film melts, the more order in the film the higher the melting temperature [4]. Directionality of grain growth has been observed with the grains forming perpendicular to the edge of the mesa. The number and orientation of the grains in the

channel affect the device performance. The more grains in the channel, the lower the overall mobility of the device due to additional scattering at grain boundaries. Additionally, the melted silicon can de-wet from the barrier oxide below resulting in voids in the polycrystalline film.

Although dopant activation can occur during FLA it is not ideal for TFTs due to pronounced lateral dopant diffusion [1]. For self-aligned devices activation would be done in a subsequent furnace anneal after implant. Due to the thermal limitations of the glass, minimal boron activation occurs in the source and drain. During implantation the boron creates negligible displacements, due to its low mass. This results in few locations for the boron to activate in during the ensuing anneal. The low temperature requirement also doesn't provide enough energy for the silicon to leave the lattice allowing for boron to replace it. The addition of a fluorine implant has been shown to increase boron activation at low temperature [5]. This is thought to be due to the amorphization that the fluorine implant causes. With the additional displacements the boron is easier incorporated during the subsequent solid phase regrowth. Previous work on crystalline Si TFTs has shown this also works with thin films [6]. It was unknown if this benefit would be applicable for polycrystalline films.

III. Device Fabrication

TFTs were fabricated using a modified non-self-aligned process to allow for the extension to self-aligned transistors [1]. Starting substrates were 150 mm diameter Corning LOTUS NXT display glass wafers with 200 nm plasma enhanced chemical vapor deposition (PECVD) silane-based SiO_2 barrier layer. Hydrogenated amorphous silicon (a-Si:H) was deposited using PECVD resulting in a 60 nm film. The a-Si:H was deposited using SiH_4 and H_2 at 400 °C, 1 Torr, and RF power 100 mW/cm^2. Samples were dehydrogenated at 450°C for 2 hours in N_2 ambient to prevent hydrogen bubbles during the FLA step. Super-mesas were defined and etched into the a-Si using SF_6 in a reactive-ion etch (RIE). Samples were cleaned in heated piranha solution (H_2SO_4/H_2O_2) and HPM (HCl/ H_2O_2). A 100 nm PECVD TEOS-based SiO_2 (a.k.a oxide) capping and anti-reflective oxide layer was deposited. The samples were then ready for flash lamp annealing (FLA). The FLA was performed on a NovaCentrix PulseForge 3300. The samples were heated to 500 °C on enclosed hotplate. The samples were exposed to a single pulse with a lamp driver voltage of 505 V for 250 µsec. The resulting dose was measured by bolometer to be 5.1 J/cm^2.

After FLA the samples were cleaned and underwent a 12 hour destress anneal at 630 °C in N_2 ambient. The capping oxide was removed in buffered HF and the final mesa structure was patterned and etched. The samples were then cleaned and a 200 nm of PECVD oxide was deposited. This was patterned and etched to open the source/drain and form a blocking oxide over the channel region. An additional 100 nm PECVD oxide was deposited to thicken the blocking oxide and act a screening oxide. The source/drain received a fluorine preamorphization implant at 75 keV and varying doses, shown in Table 1, followed by a boron implant of 4x10^{15} cm^{-2} at 35 keV. The blocking oxide was then removed and 100 nm PECVD oxide was deposited for the gate dielectric. The samples then underwent an activation anneal at 630°C in N_2 ambient for 12 hours. This activates the dopant and densifies the PECVD gate dielectric. Contact holes were then patterned and etched. Aluminum was sputtered and etched for the source/drain contacts as well as the gate metal. The devices were sintered in a forming gas ambient (5%H_2 in N_2) for 30 min at 450°C. A finished device is shown in Figure 3.

Fig. 3. Completed FLAPS TFT

IV. Results and Discussion

A. Dopant Activation

Sheet resistance is inversely related to dopant activation and was used to compare the activation of different fluorine doses. Sheet resistance was measured using van der Pauw test structures. The sheet resistance increased as the fluorine dose increased. For FLAPS the sheet resistance of van der Pauw structures may not be an accurate measure for the activation process in the source/drain region of TFTs. This is due to the directionality and size dependence of FLAPS. The van der Pauw structures tested were much larger than the TFTs. Additionally, the van der Pauws encompassed an entire mesa resulting in it containing more grains than the TFTs.

B. TFT Results

Devices with varying fluorine doses are shown in Figure 4. The extracted parameters from these devices are shown in Table 1. Devices with 5x10^{15} cm^{-2} show an increase in maximum drain current. The channel mobility should not be dependent on the source/drain implant therefore the apparent mobility change is due to a decrease in series resistance. The mobility of the devices was extracted at max transconductance and neglected series resistance. Devices with fluorine implant showed DIBL-like behavior which is most likely caused by insufficient blocking oxide, allowing for fluorine to enter the channel. Degradation of subthreshold operation may be the result of associated interface traps.

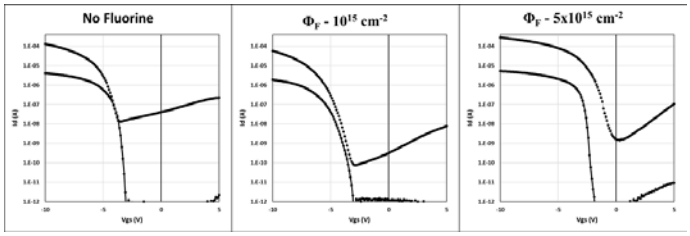

Fig. 4. Device transfer characteristics for varying F^+ dose L-12 µm W-24 µm

Table 1 TFT characteristics

Fluorine Dose	None	1^x10^{15} cm^{-2}	1^x10^{15} cm^{-2}
Linear V_T	-3.5 V	-4 V	-2.4 V
ΔV_T	0 V	0.3 V	2 V
μ_{lin}	24 cm^2/Vs	13 cm^2/Vs	28 cm^2/Vs
μ_{sat}	140 cm^2/Vs	70 cm^2/Vs	220 cm^2/Vs
I_{Dmax}	131 µA	58 µA	280 µA

C. *Location Dependence*

During device testing it was noticed that the device performance was a function of die position on the wafer. Figure 5 shows the peak drain current from a family of curves for the $1x10^{15}$ cm^{-2} fluorine dose section, all devices shown are length 12 µm & width 24 µm. The variation is most likely caused by a variation in crystallinity due to non-uniform exposure intensity. The variation of the devices based on position complicates analysis between the different treatments and overall statistical analysis. Improved system design and control is required to mitigate this issue.

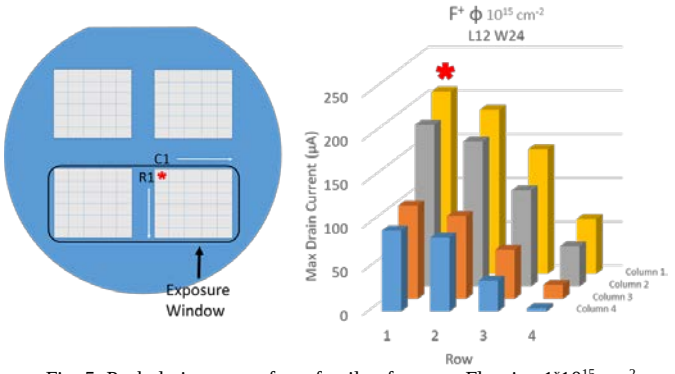

Fig. 5. Peak drain current from family of curves. Fluorine 1^x10^{15} cm^{-2}

V. Conclusion

Devices with high fluorine dose, $5x10^{15}$ cm^{-2}, showed increased drain current and larger extracted channel mobility, indicating lower series resistance from increased boron activation. High $^{19}F^+$ dose devices also had less off state gate control, high leakage, and a DIBL like behavior possibly due to interface traps caused by fluorine entering the channel due to insufficient blocking oxide. A quantitative comparison between the experimental treatments is compromised due to fluorine entering the channel and location dependence. Additional experiments are underway with a thicker blocking oxide to remove the influence of fluorine entering the channel and an investigation using silicon implant for amorphization.

Acknowledgment

The authors would like to recognize the technical support of Patricia Meller and the entire RIT SMFL staff, and Dr. Robert Manley from Corning Incorporated. This project is supported by Corning Incorporated and the NY State AMPrint Center at RIT.

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