Silicon Nanowire Solar Cells by Metal-Assisted Chemical Etching

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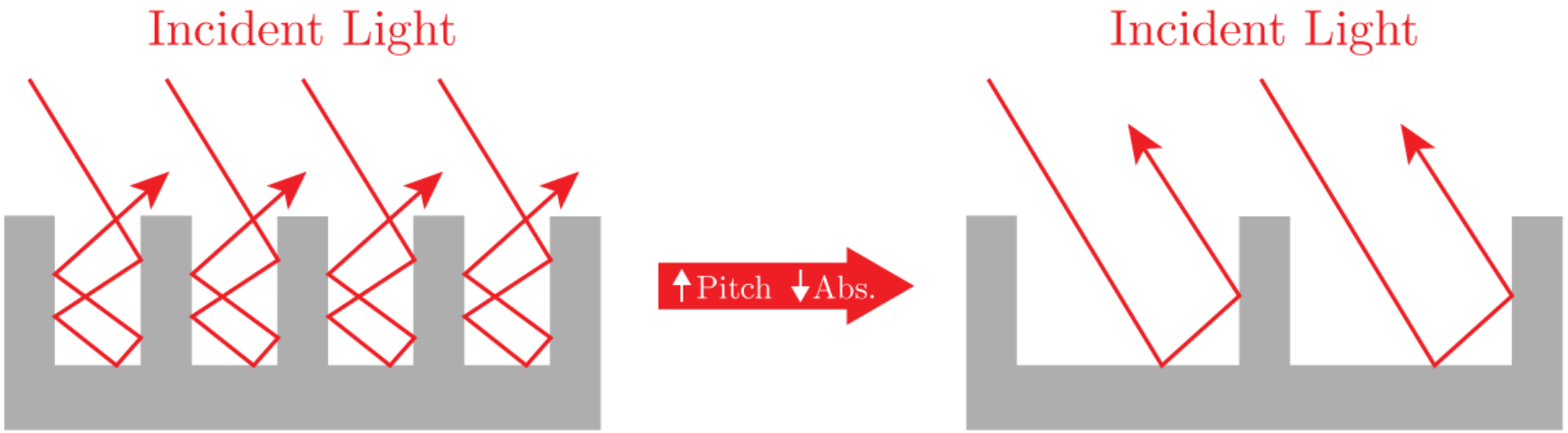
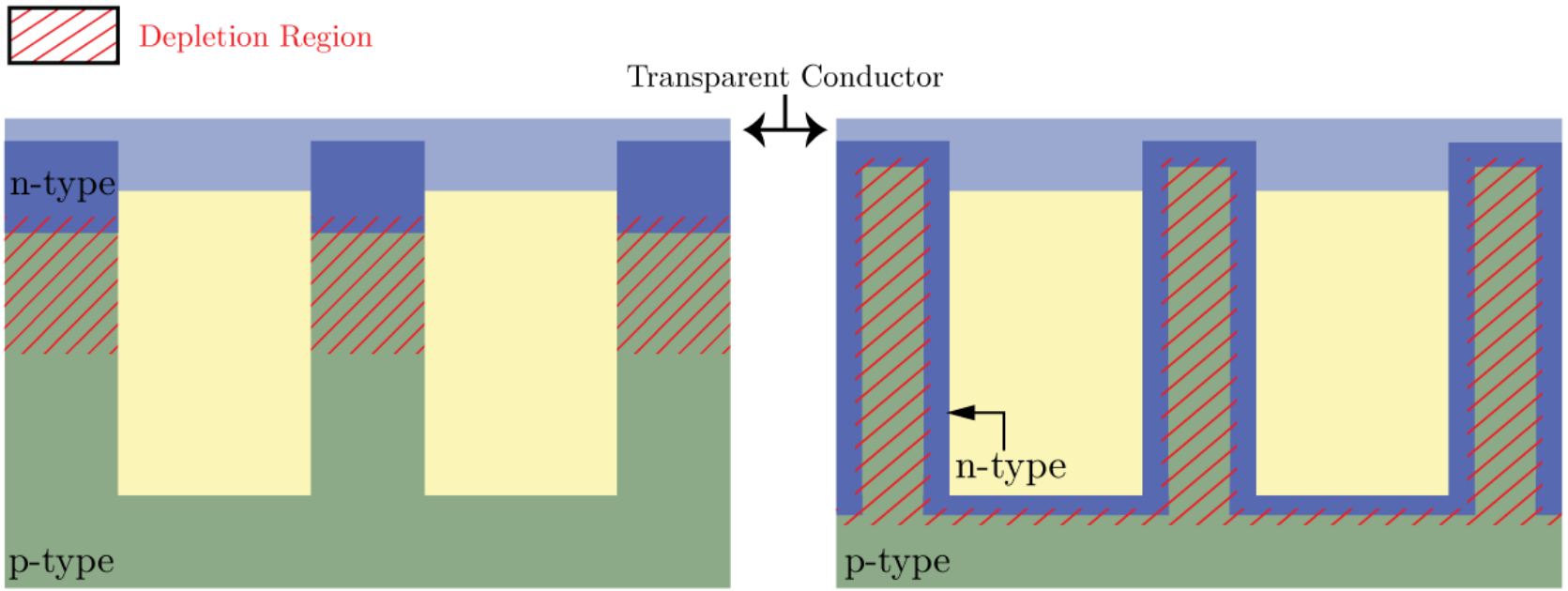
Silicon Nanowires

- Arrays of silicon nanowires (SiNWs) have been shown to have less than 1% reflectance over the peak solar radiation wavelength range by increasing the optical path length of light.
- The optical properties of SiNW arrays have been shown to be directly dependent on the diameter, pitch, and height of the wires.

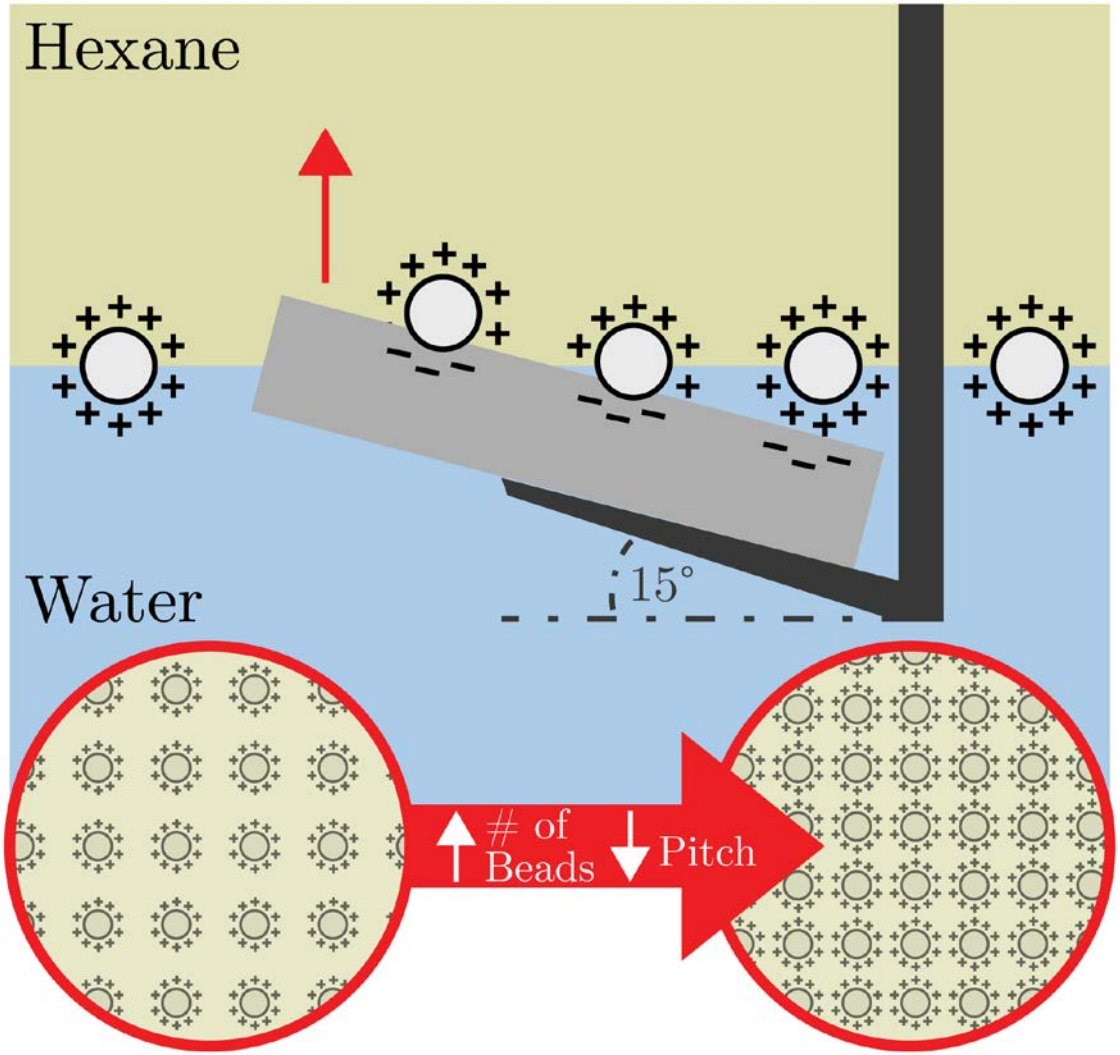


Silicon Nanowire Solar Cells

- The reduced reflection of SiNW arrays, along with light trapping, band gap tuning, charge separation, and carrier collection benefits makes them of interest to be used as the active region of a solar cell.



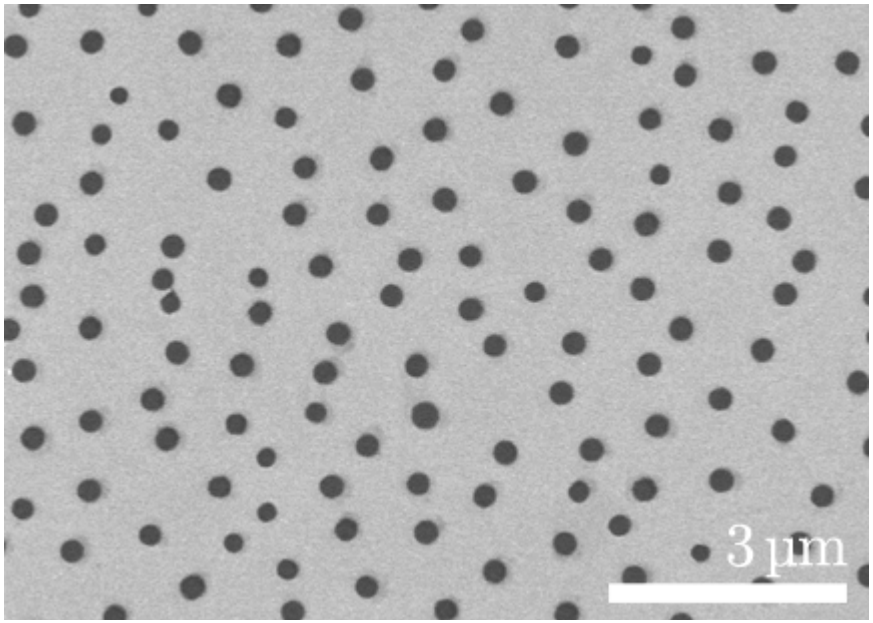
Nanosphere Lithography



- Charged polystyrene nanospheres are self assembled into a non-closed packed monolayer at the hexane-water interface.
- Different diameter NS can be injected at the interface at different densities to independently tune the arrangement.

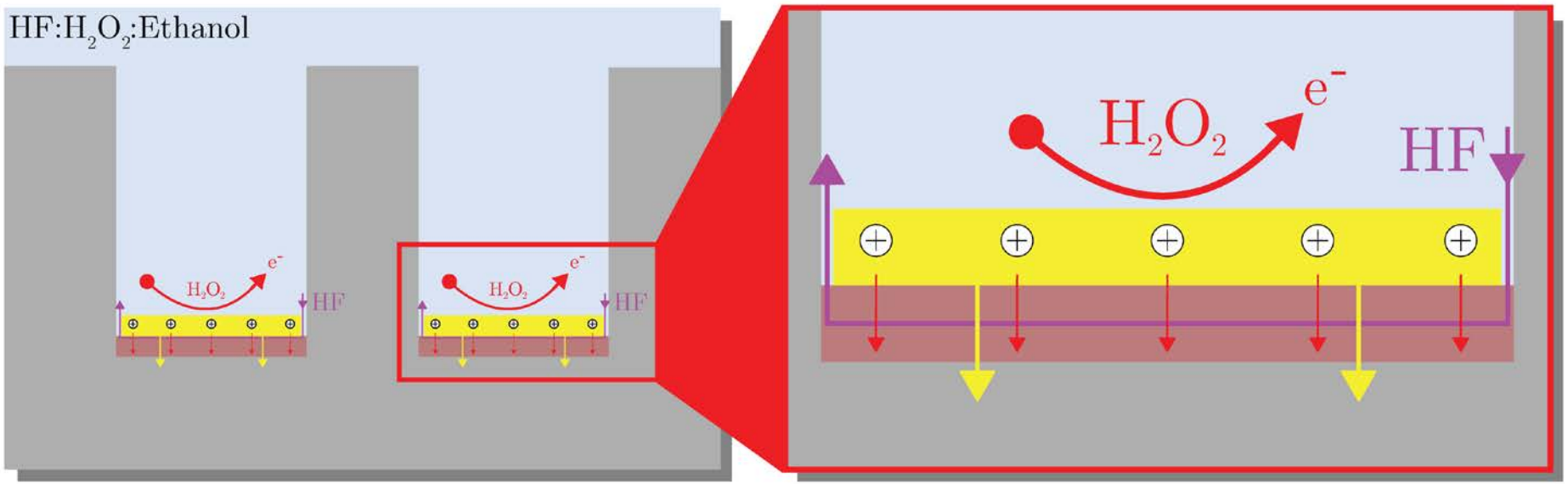
Pattern Transfer

- Gold is evaporated over the nanosphere array, then the nanospheres are removed, resulting in a nanoporous gold mask to be used in the following metal-assisted chemical etching step.

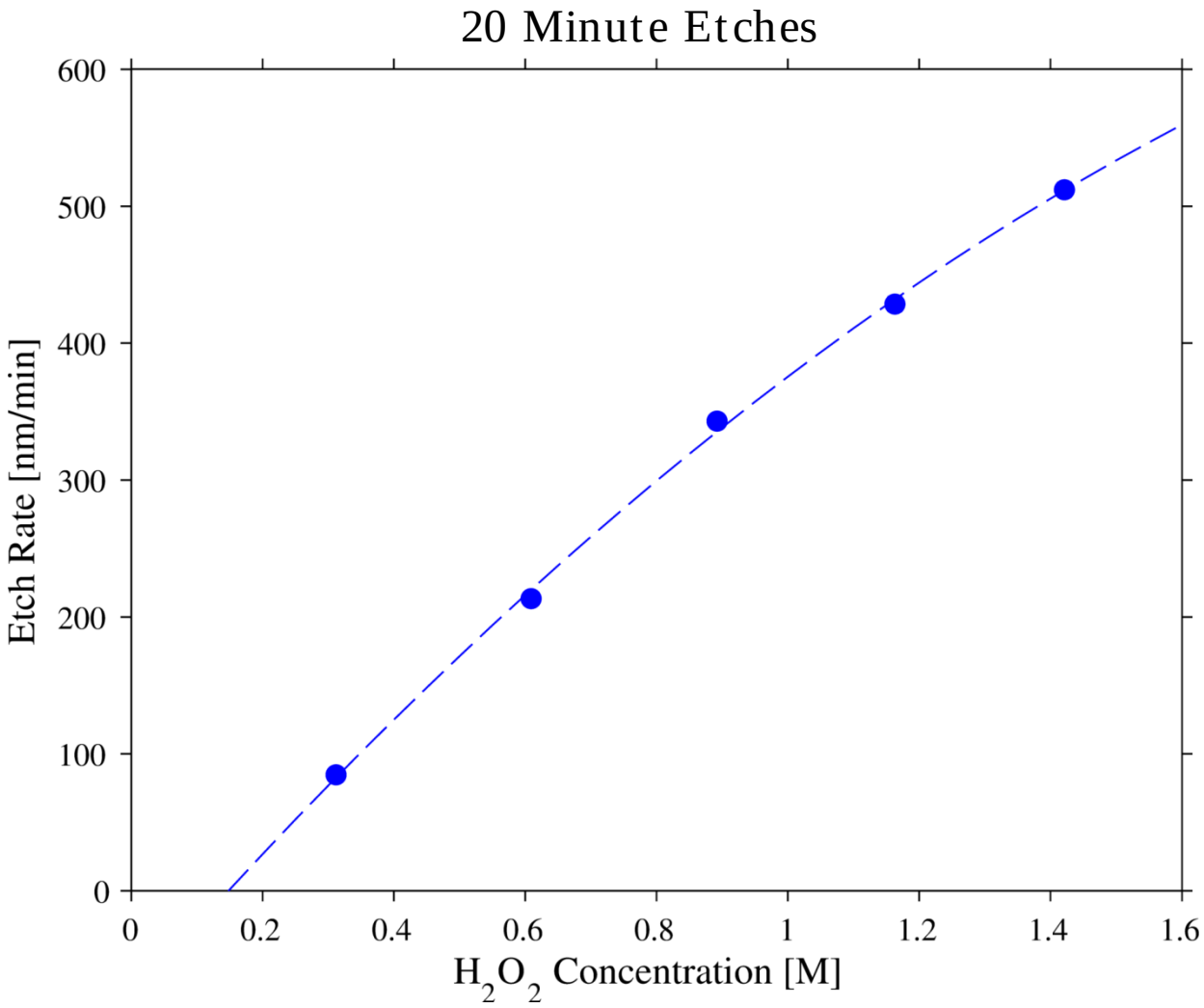


Metal-Assisted Chemical Etching

- Simple, low cost, top-down method of fabricating silicon nanostructures.
- H_2O_2 is reduced at the gold in a cathodic reaction, generated holes are injected through the gold, oxidizing the underlying silicon, which is dissolved by HF, causing the gold to sink into the substrate as etching proceeds.



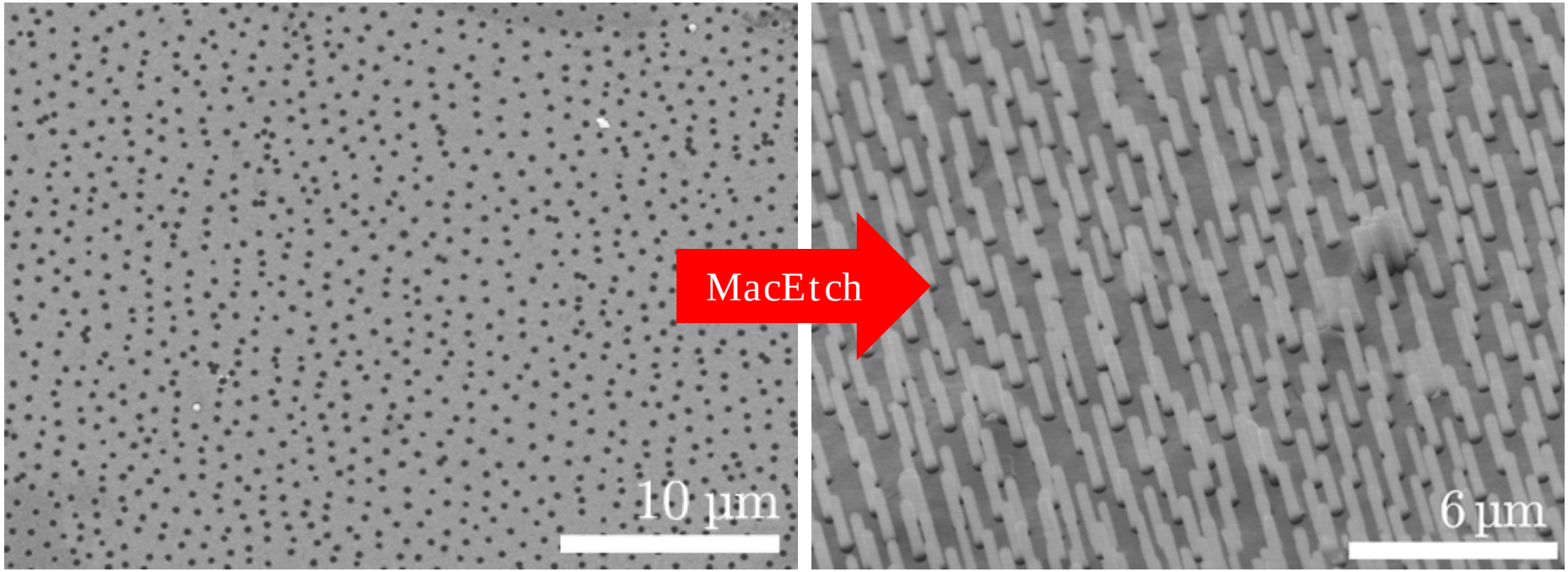
Metal-Assisted Chemical Etching



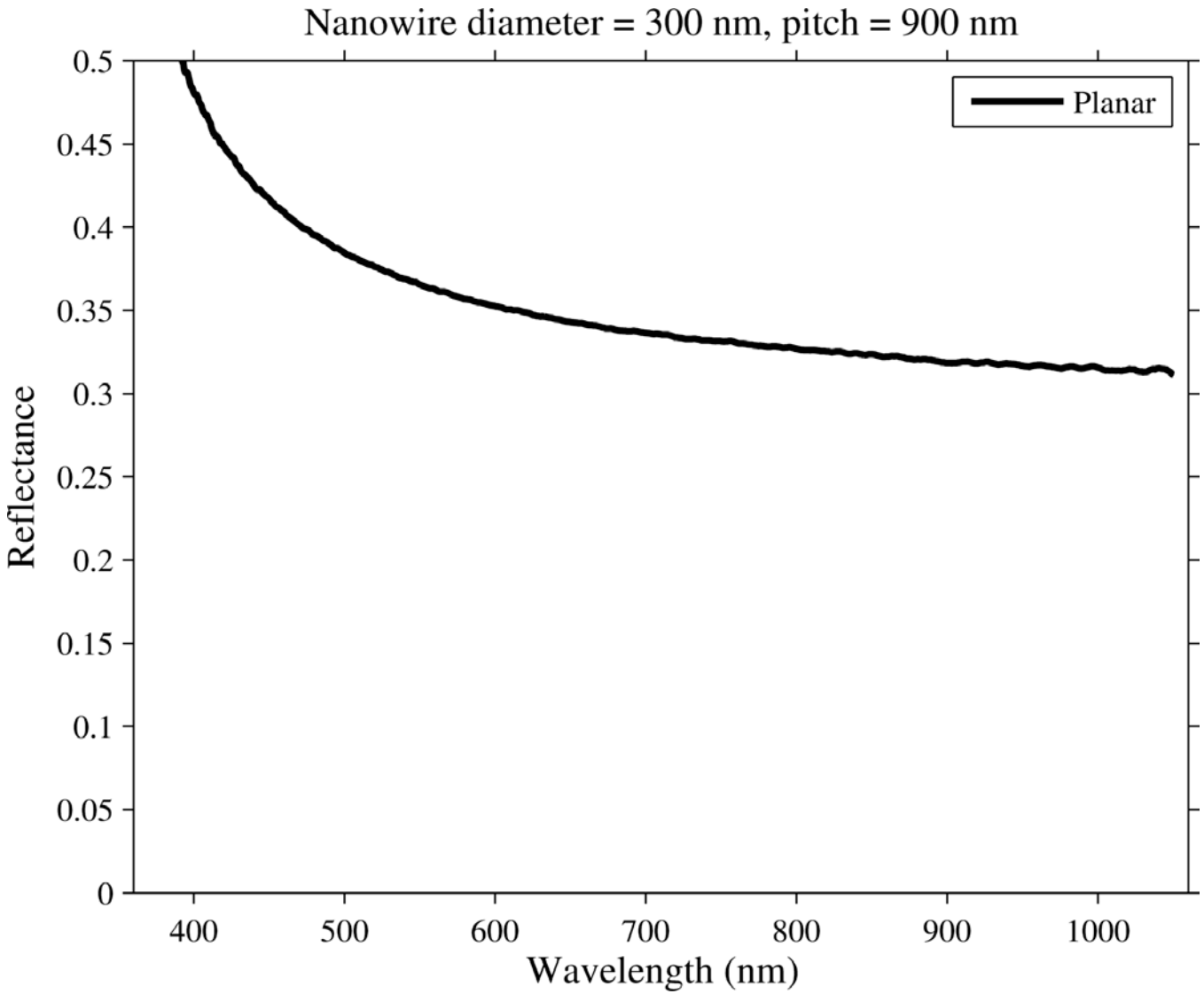
- Etch rate is limited by the concentration of peroxide in solution, which determines the rate of hole injection and the rate of oxidation of the silicon.

Nanowires

- Hydrogen peroxide concentration is varied to obtain a controlled etch rate of 150 $^{nm}/_{min}$.
- Optical reflectance of SiNW arrays studied as a function of nanowire diameter, pitch, and height in order to determine which arrangement should be chosen to fabricate solar cells.



NW Reflectance Measurements



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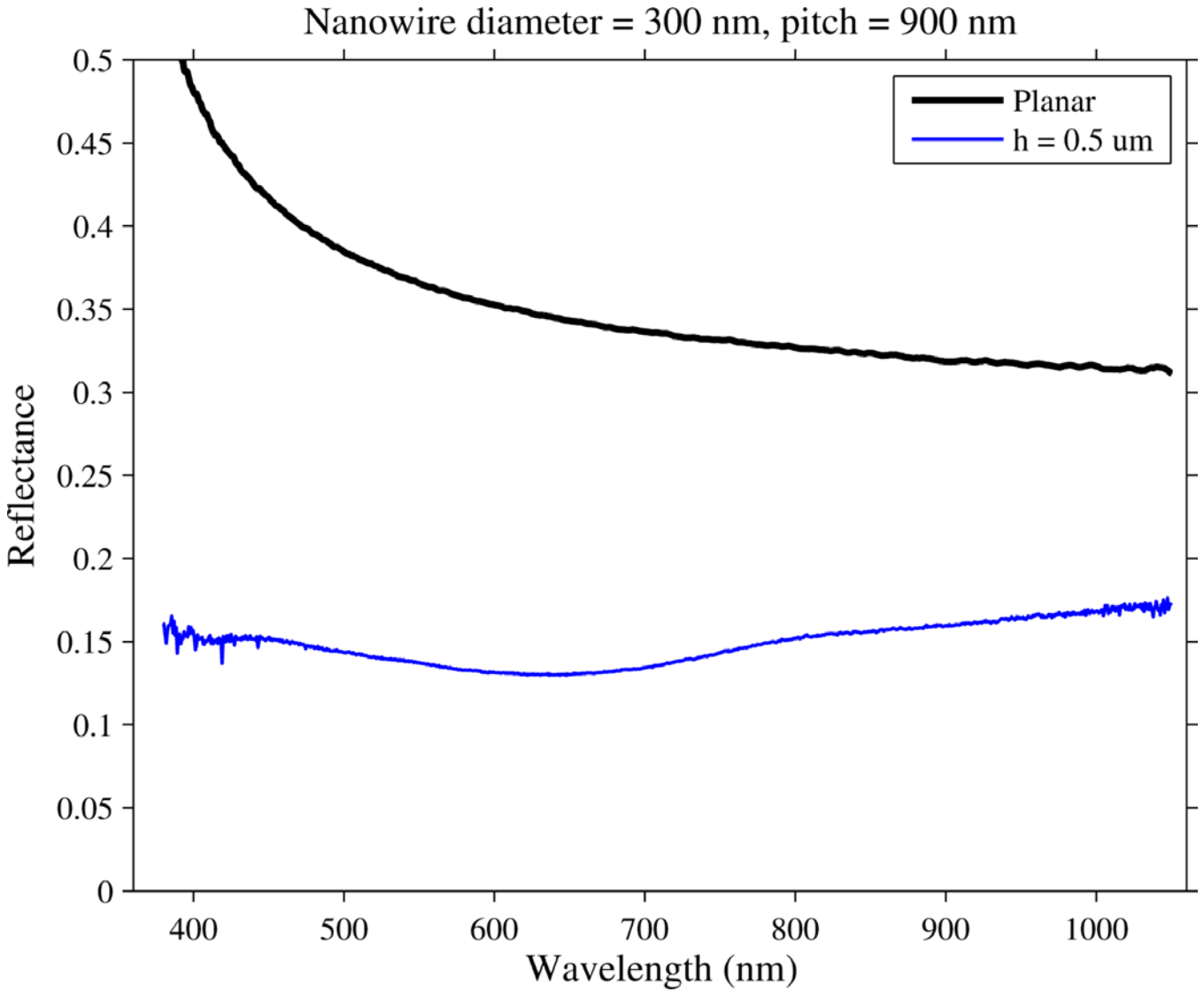

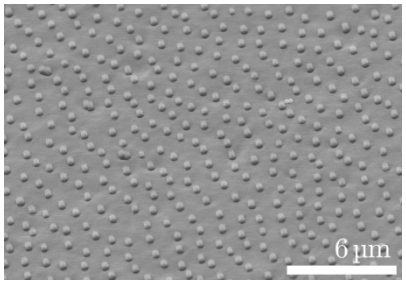

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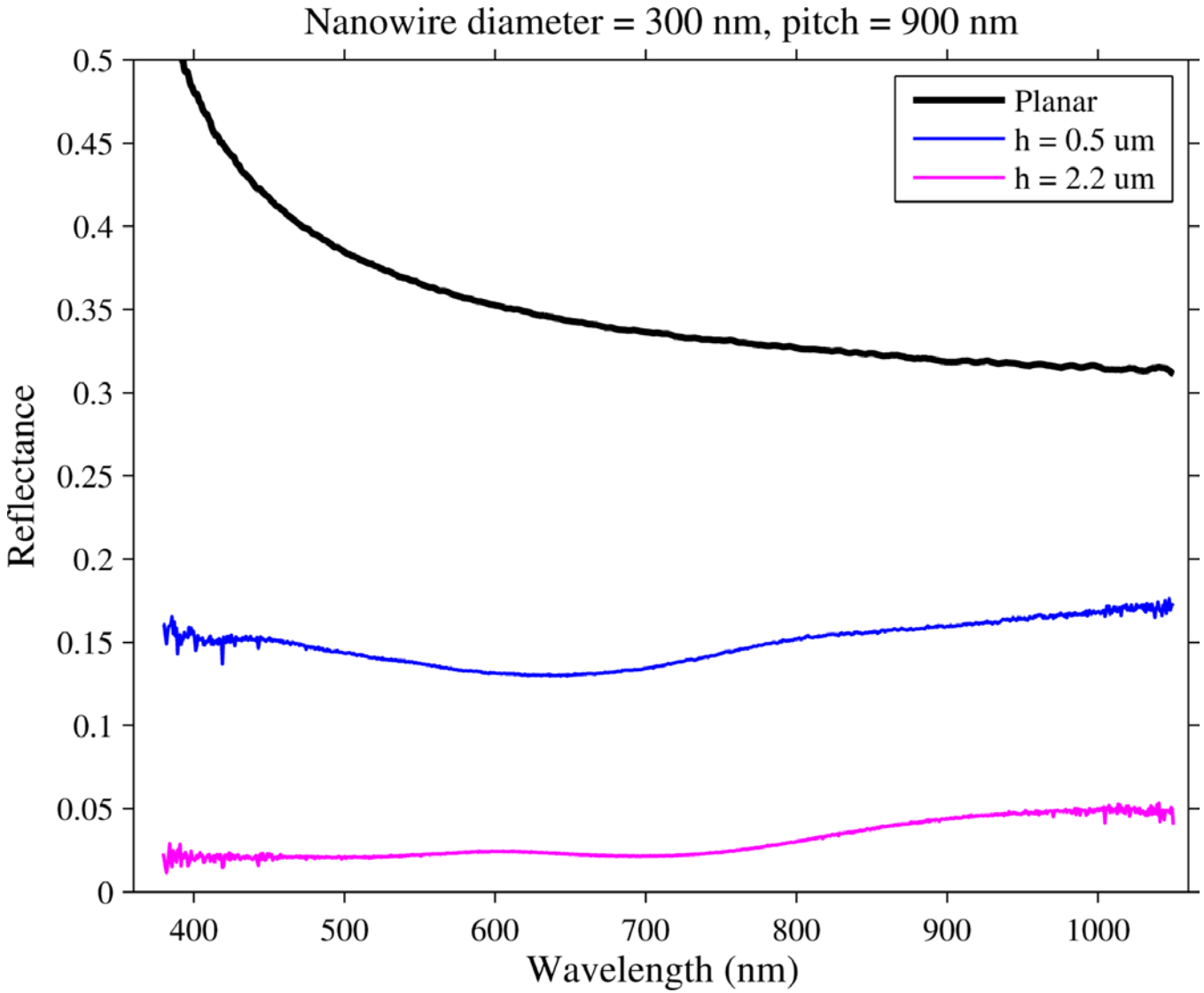

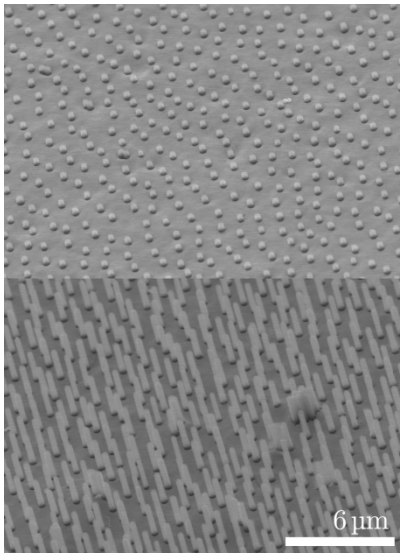

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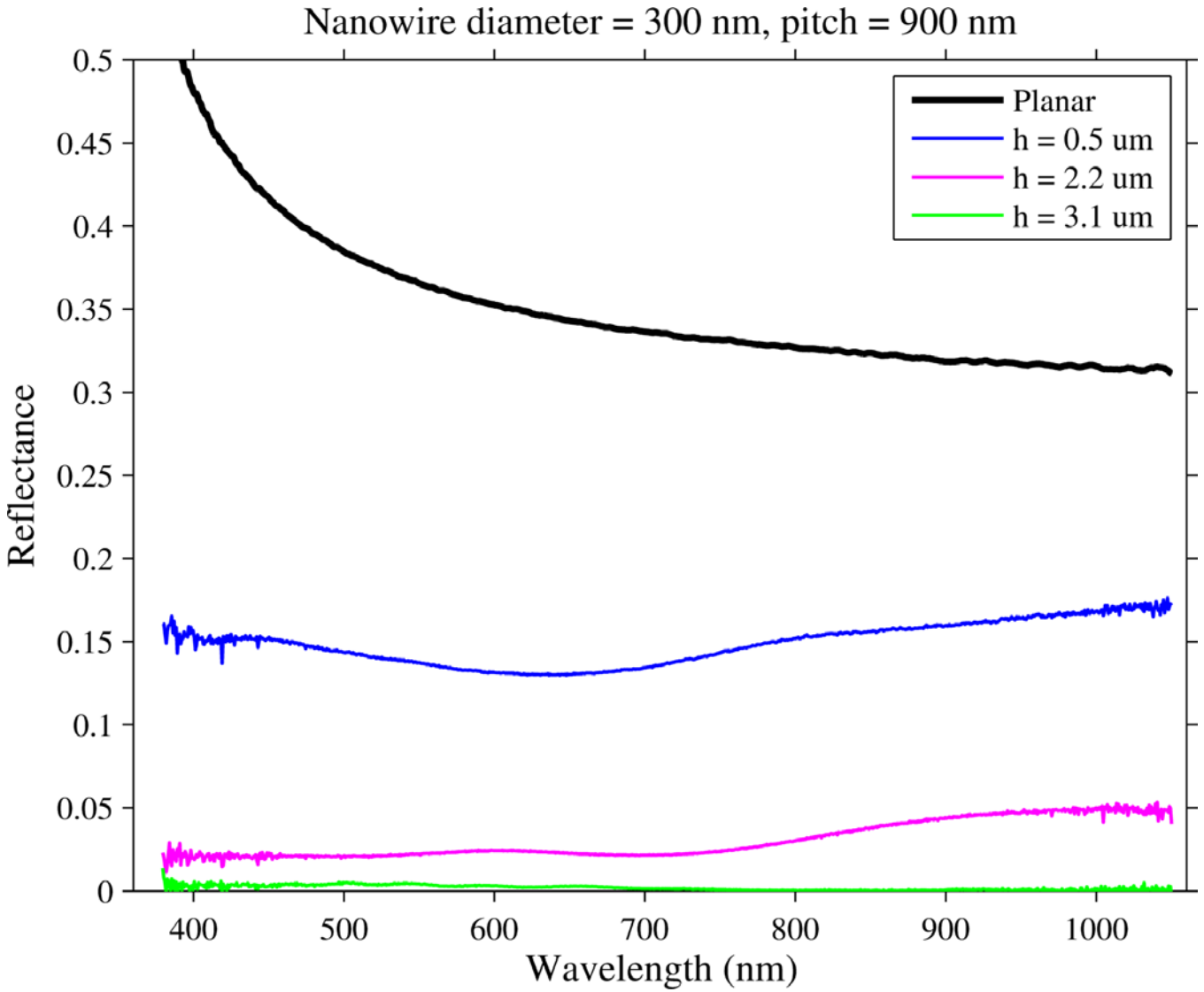

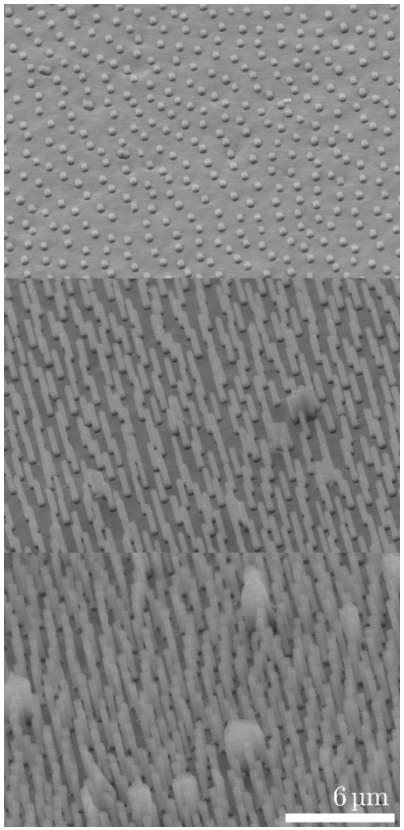

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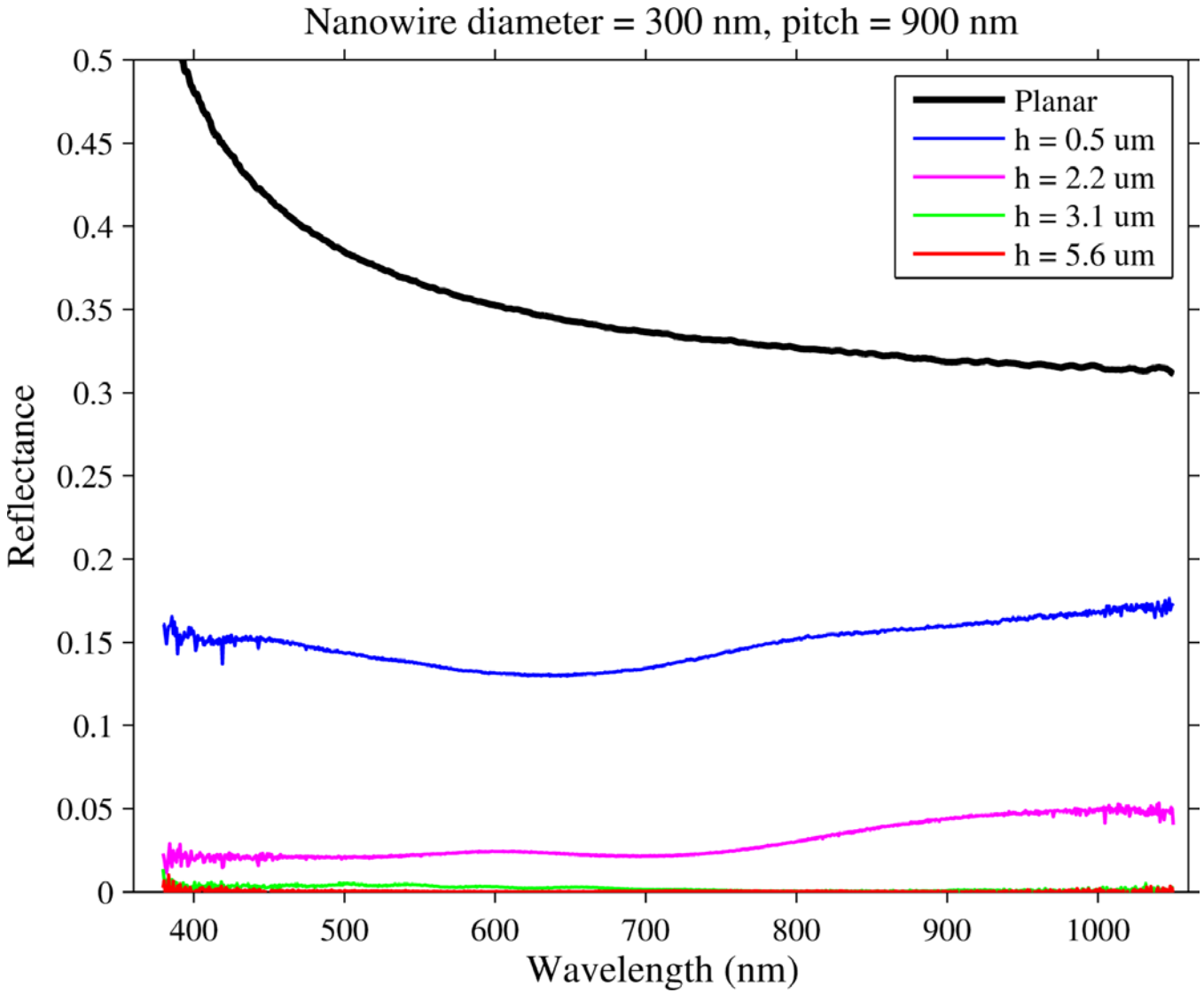
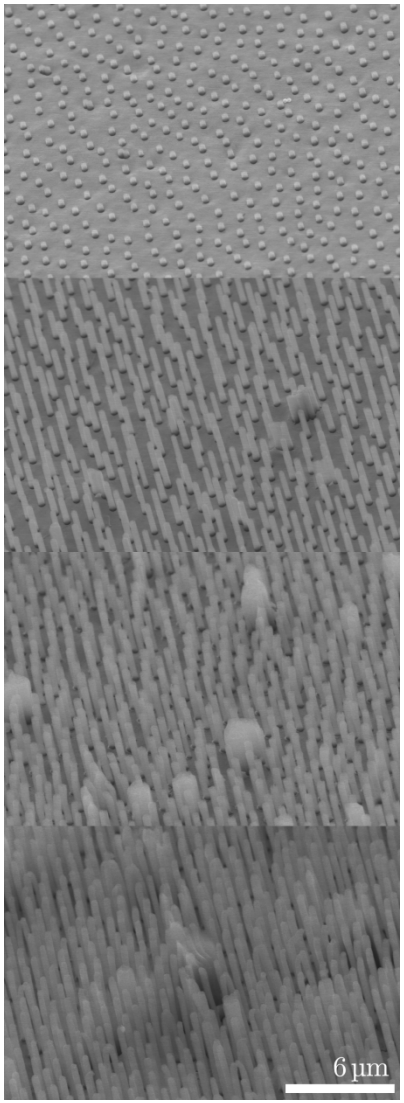
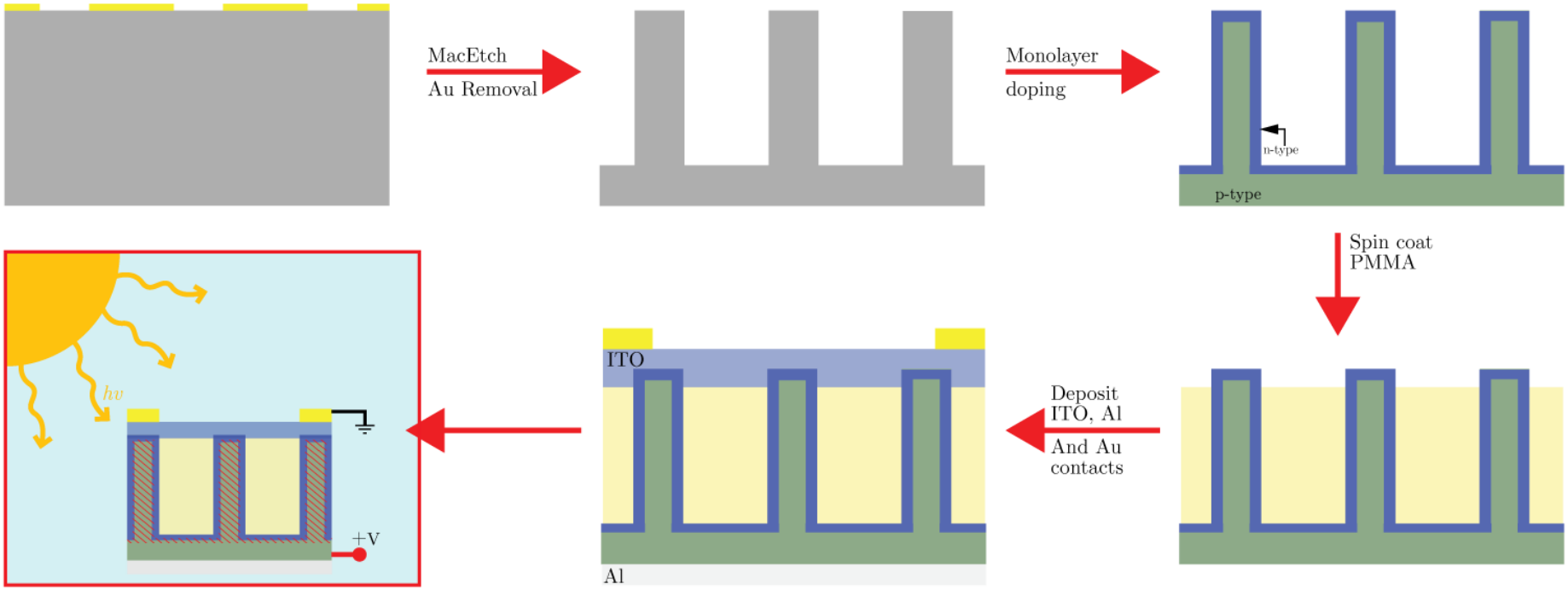




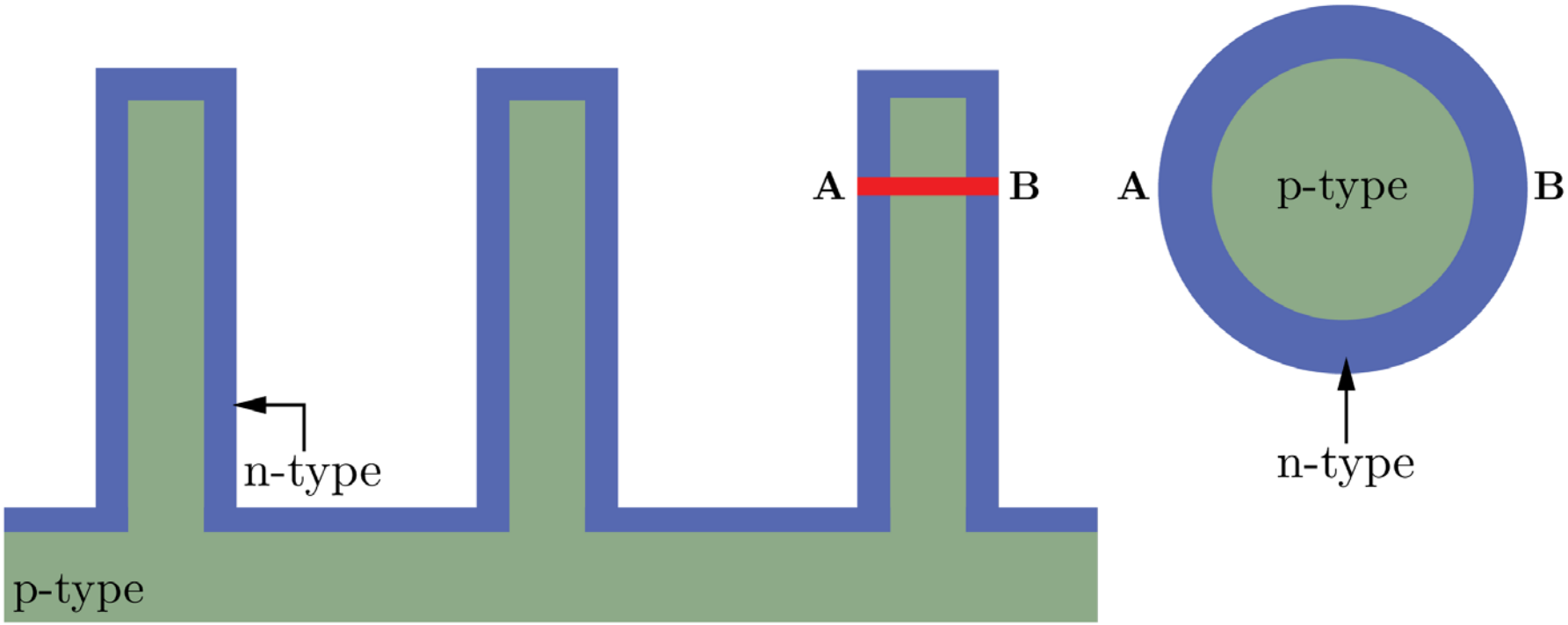
Remaining Process Flow

- After patterning the nanoporous gold mask with nanosphere lithography and etching the wires with metal-assisted chemical etching, the remaining process flow involves monolayer doping, wire encapsulation, and deposition of contacts.

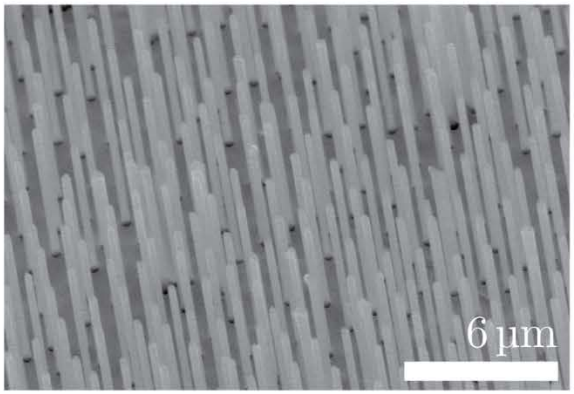


Monolayer Doping

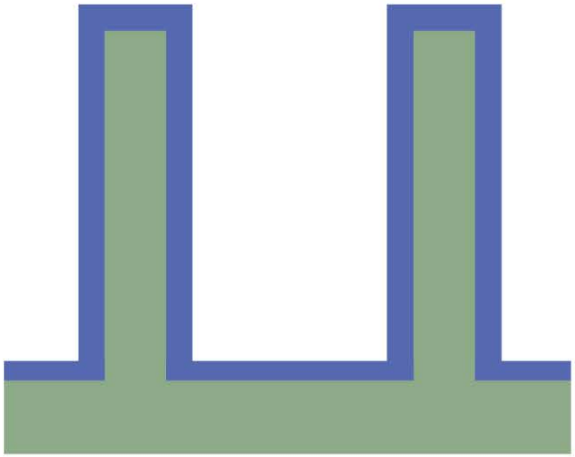
- Self assembly of phosphorus containing molecules allows for formation of ultra-shallow junctions.
- Expected 50 nm junction depth from Silvaco simulations.



PMMA Encapsulation



Nanowires



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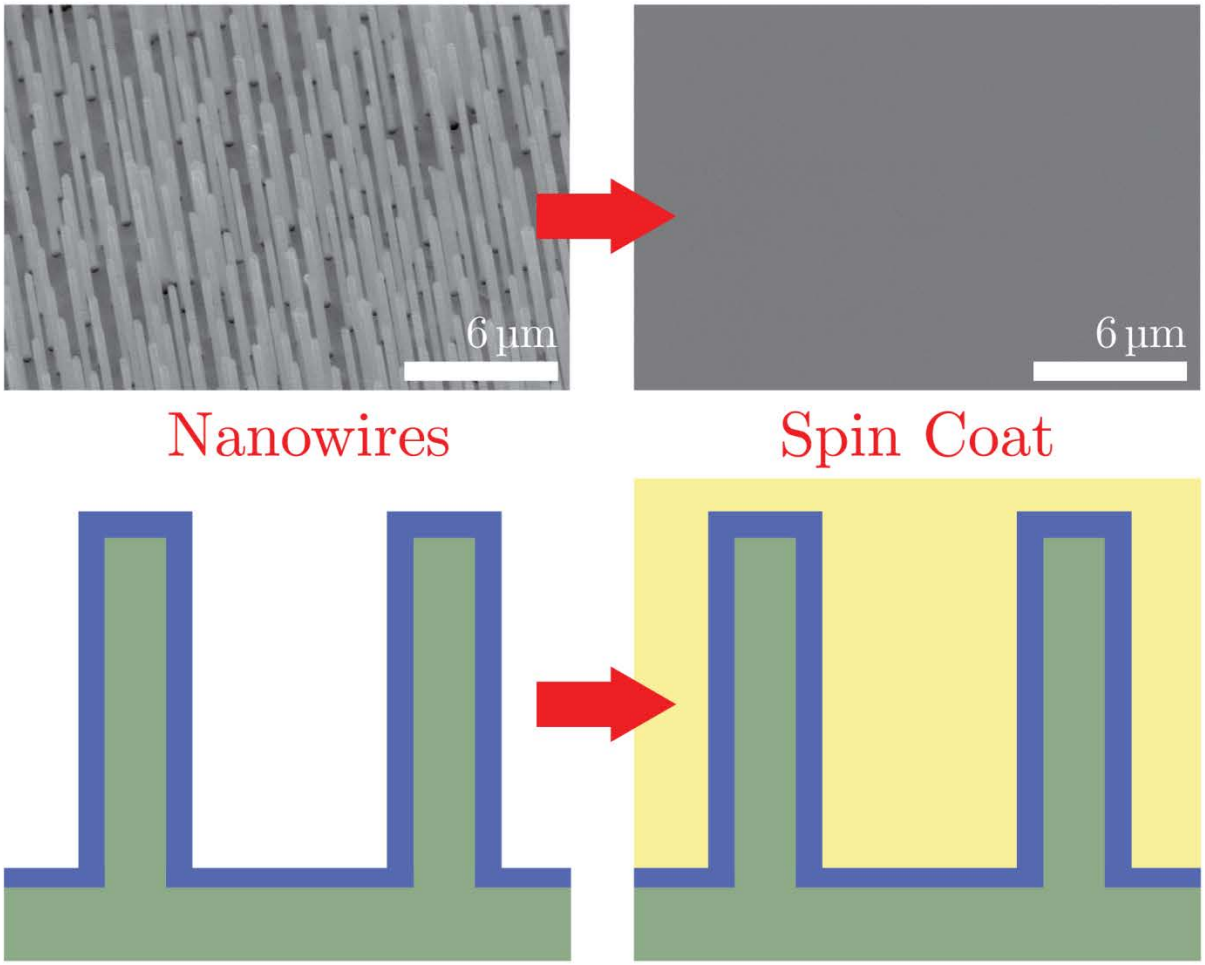
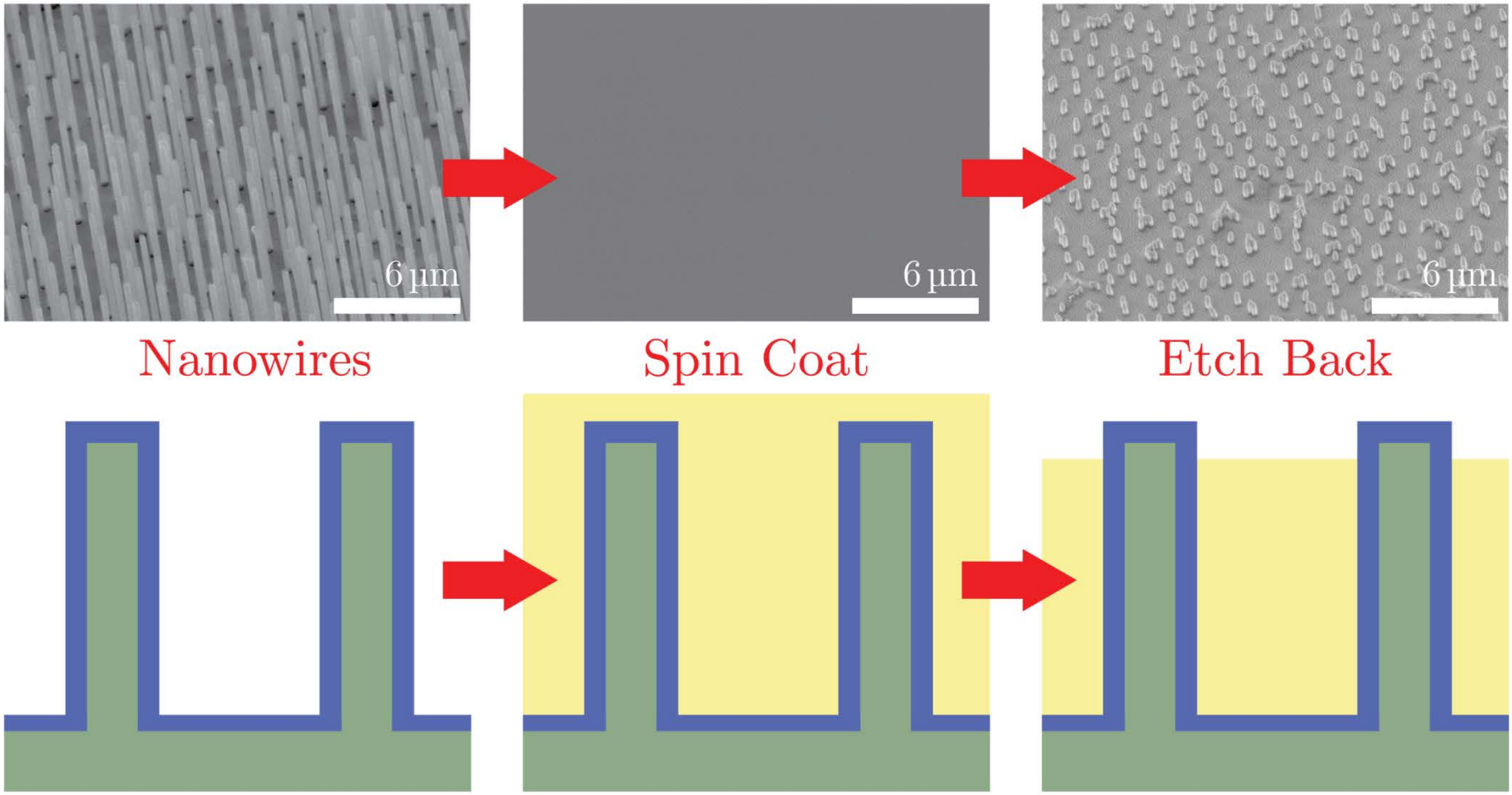
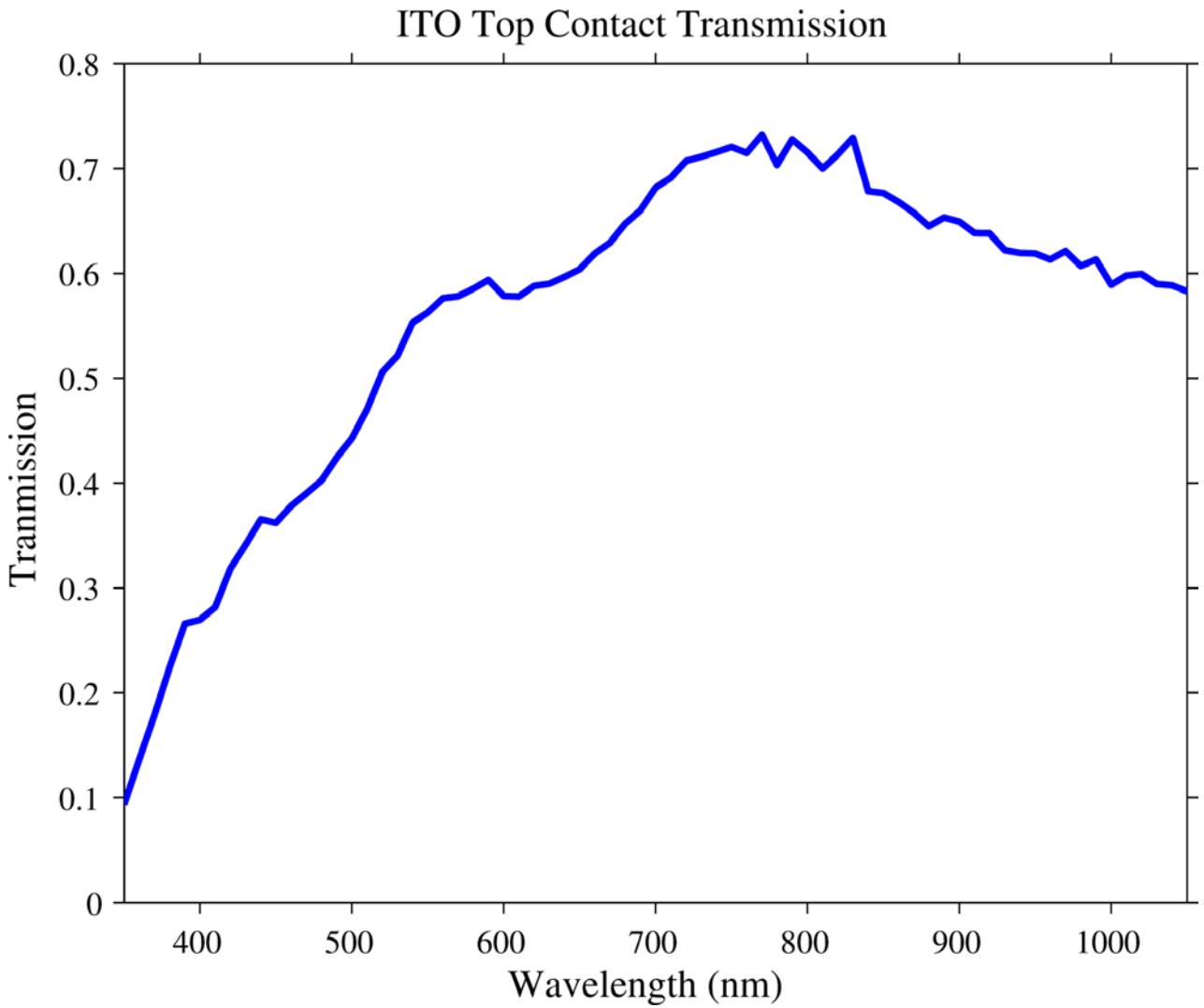


PMMA Encapsulation

- PMMA is etched in O_2 plasma at a rate of 300 $^{nm}/_{min}$

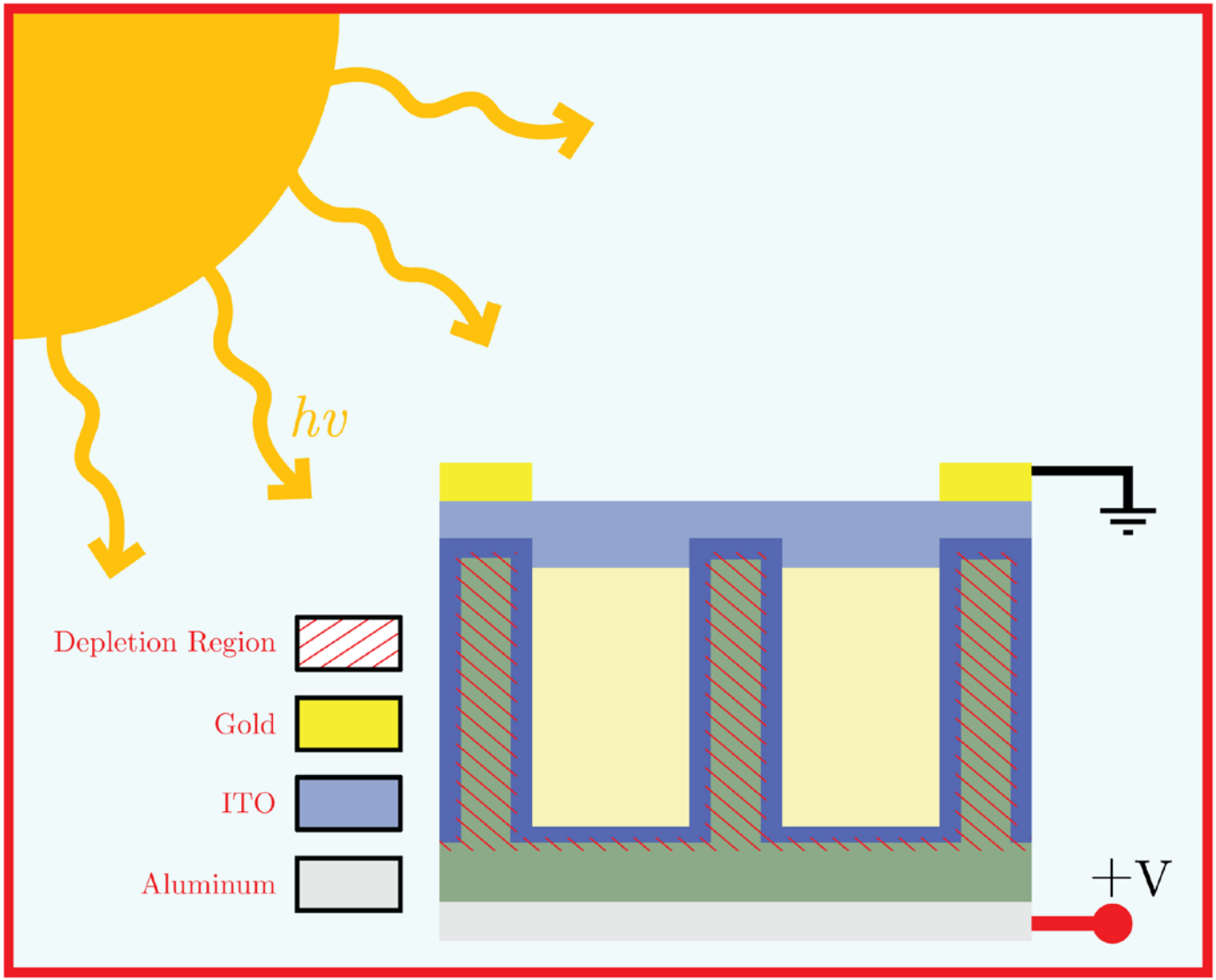


Deposition of Contacts

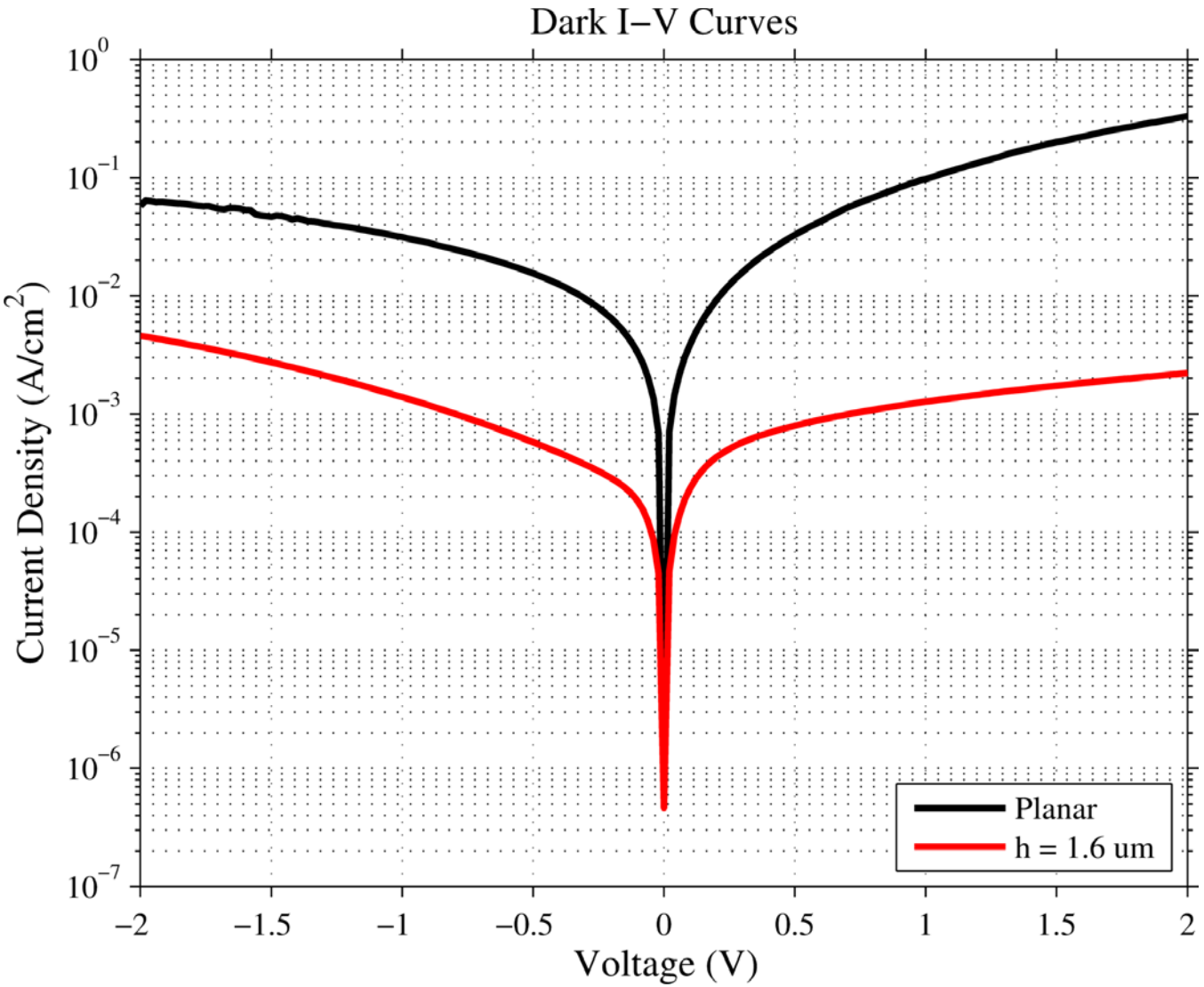


- ITO sputtered with pure Ar after an extended pre-sputter with Ar/O_2 to fully oxidize the target.
- SF_6/ Ar plasma etch on backside of device to etch through MLD junction, then aluminum evaporation for back contact.
- Gold sputtered on outside edge of top of device for top contact.

Solar Cell Structure

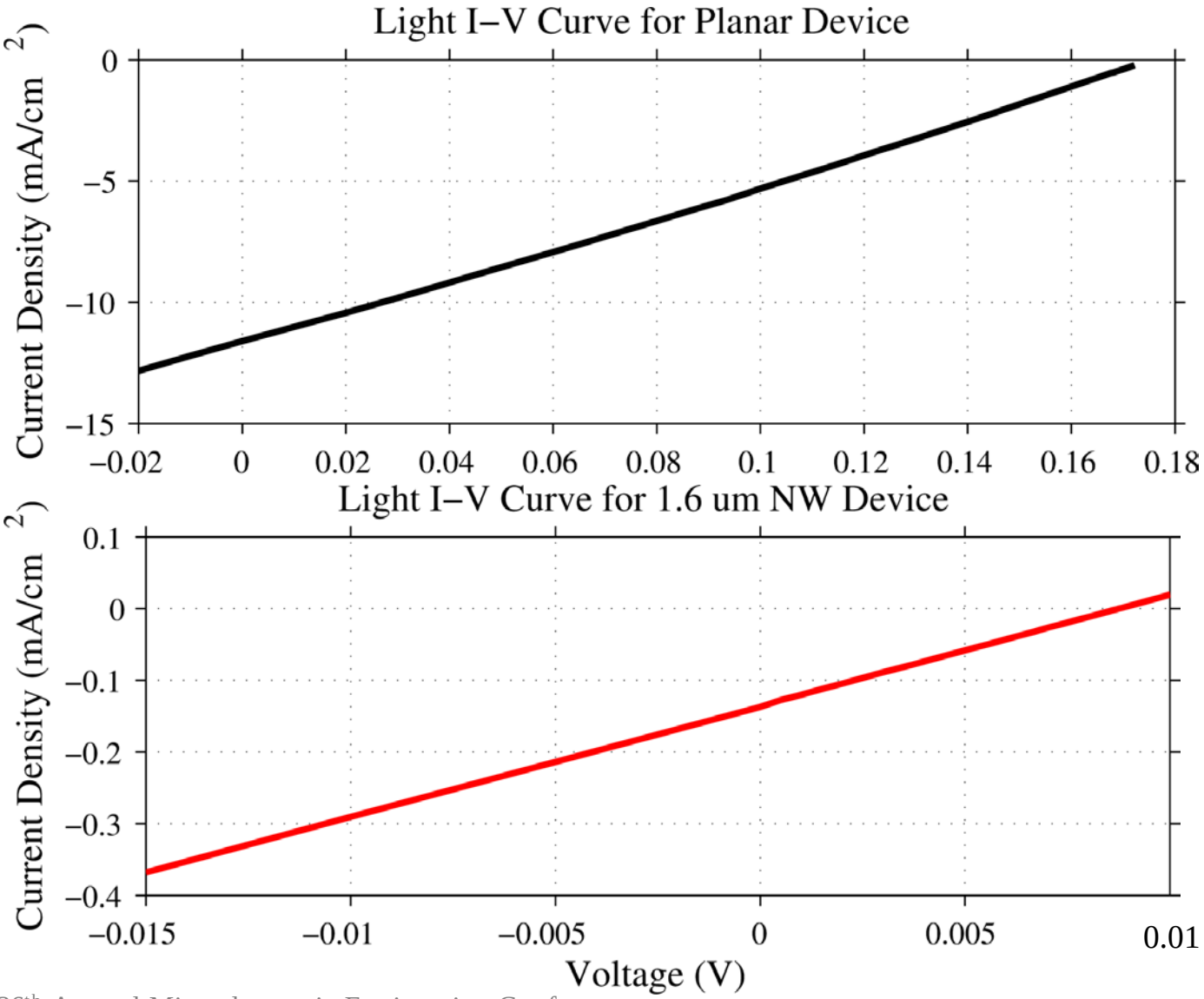


Solar Cell Test Results



- The short (1.6 µm) wire device showed slight rectification.

Solar Cell Test Results



- Short (1.6 µm) wire device showed slight light-generated current, although not as much as the planar device.
- With a V_{oc} of 10 mV and a J_{sc} of 0.36 mA/cm^2, the nanowire device performance is not great.

Possible Devices Issues

- Lack of surface passivation likely results in surface charge depletion along the nanowire sidewalls, leading to degraded device performance.
- For longer wires, increased surface area might have led to non-complete coverage of the dopant molecule in the MLD step, resulting in no junction formation.
- High contact resistance, unable to sinter backside contact with current process - the presence of PMMA restricts the processing temperature to < 250 ℃.

Conclusions

- Silicon nanowires were successfully fabricated with nanosphere lithography and metal-assisted chemical etching in a “new-to-RIT” process.
- Optical reflectance of different NW arrangements was studied as a function of NW height.
- Diode behavior was not observed with the NW devices as expected. There are a few things that could have happened, but more work is needed to determine which is the most likely.

Future Work

- Do an extended study with monolayer doping on the silicon nanowire arrays (or use ion implantation).
- Alter process so that backside aluminum contact can be sintered, this would significantly decrease the contact resistance.
- Try different surface passivation techniques, Al_2O_3, Si_3N_4, SiO_2, etc. to prevent the surface charge depletion along NW sidewalls that is degrading device performance.

Acknowledgements

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