Silicon Nanowire Solar Cells by Metal-Assisted Chemical Etching

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ABSTRACT

Silicon nanowire (SiNW) arrays were fabricated from a nanosphere lithography patterned gold mask by metal-assisted chemical etching. The optical reflectance of these SiNW arrays was studied as a function of nanowire diameter, pitch, and height. Less than 1% reflectance was achieved over the 300 to 1000 nm wavelength range for both 200 nm and 300 nm diameter wire arrays at different pitches and at as low as 3 m wire heights. With these SiNW arrays, a monolayer doping process was used to generate a radial p-n junction inside the nanowires, enabling the fabricated of silicon nanowire solar cells. Slight rectification and light-generated current was measured in short (1.6 µm) nanowire devices, however, the observed behavior was not what was expected of a typical p-n junction diode. It was hypothesized that lack of surface passivation led to surface charge depletion along the nanowire sidewalls, which ultimately led to poor device performance. This work presents the demonstration, characterization and implementation of a full device fabrication process for generating silicon nanowires via nanosphere lithography and metal-assisted chemical etching to pave the way for future work exploring silicon nanowire devices at RIT.

1. INTRODUCTION

To fuel the modern energy-centered lifestyle, fossil fuels such as petroleum, coal, and natural gas are burned to produce electricity. The combustion of fossil fuels releases large amounts of greenhouse gases into the atmosphere, leading to radiative forcing and accelerating the planet-warming greenhouse effect.[1] As this issue becomes more pressing, alternative sources of energy are being investigated to help reverse the negative environmental impacts of deriving our energy from fossil fuels, as well as to provide an affordable source of energy when fossil fuel resources inevitably become scare and expensive. Solar energy is one of the most promising alternative sources of energy. The energy from the sun is collected and converted to electricity by taking advantage of the photoelectric effect of semiconductor materials such as silicon. Due to the strong motivation behind this field of research, there has been significant progress made since the first reported single p-n junction silicon solar cell that had less than 1% energy conversion efficiency.[?] In contrast to the first published device, today's cutting-edge silicon solar cells have achieved conversion efficiencies that are approaching the theoretical efficiency limit of 29.43% for single junction silicon solar cells.[2,3]

To achieve high efficiency photovoltaic devices, the incoming light must be managed in such a way that the greatest amount of light is absorbed by the cell. Conventional anti-reflective (AR) coatings can provide relatively low reflectivity of incident light, however, they often require the deposition of foreign materials and have high associated costs. For alternative, silicon-based AR solutions, significant attention has been paid to the use of nanostructures such as pyramids, wires, and honeycombs to reduce the amount of incoming light reflected away from the solar cell.[4–6] Silicon nanowires (NWs), in particular, have been shown to have excellent optical absorption properties, making them ideal for use in solar cell applications.[7–11] By increasing the optical path length of incident light on a silicon solar cell, arrays of silicon NWs can achieve up to 96% peak absorption.[8] The optical properties of these periodic silicon NW arrays has been shown to be directly dependent on the diameter, spacing, height, and bending of the wires, showing the importance of having independent control over each of these parameters.[11,12]

Fabrication techniques for silicon-based nanostructures such as NWs can be put into two categories: bottom-up, or top-down. Bottom-up processes involve the growth of NWs from the substrate, the most common mechanism being vapor-liquid-solid (VLS) growth.[7,8,13] Top-down processes, on the other hand, involve etching into the silicon substrate to reveal the NWs, and include reactive ion etching (RIE) and metal-assisted chemical etching (MacEtch).[5,8,9,12,14–16] MacEtch is a simple and low-cost method for fabricating silicon nanostructures, where a mixture of HF and H_2O_2 are used to selectively etch the silicon underneath a noble metal layer, by the

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local oxidation of Si, and the etching of the oxidized interfacial layer by HF.

As a prerequisite for fabricating NWs, the areas where the NWs are ultimately desired must be lithographically defined. Traditional photolithography techniques, however, fail to provide the resolution needed for patterning truly nanoscale ($\lesssim$ 500 nm diameter) wires. Nanoscale wires can instead be achieved with next-generation photolithography techniques such as extreme ultraviolet and electron beam lithography, but, these technologies have a characteristically low throughput and high associated costs. For low cost nanoscale wires for photovoltaic applications, alternative patterning methods such as nanosphere lithography, nanoimprint lithography, and self-organizing polymers must be applied. Nanosphere lithography (NSL) is a widely employed patterning process that takes advantage of the self-assembly of small particles at the interface between two fluids to generate a colloidal crystal film with hexagonal symmetry in a close-packed or non-close-packed monolayer.[10,17,18] This self-assembled pattern is then transferred to the substrate, which is used to define the location of the NWs. With deposition of a noble metal, such as gold, over the nanospheres, the nanospheres can be removed, leaving a nanoporous metallic catalyst layer behind, which can then be used as-is for metal-assisted chemical etching.

In addition to their use as an anti-reflective layer, silicon NW arrays are also of interest to be used as the active region of a solar cell. In a silicon NW solar cell, the NWs are doped to form either an axial junction, or a radial (core/shell) junction. The theoretical efficiency of a radial p-n junction silicon NW solar cell has been shown to be as high as 30%, however, previously published work has presented devices that have achieved, at best, 17% efficiency.[16,19–22] A radial junction geometry is typically preferred because the carrier collection takes place in the radial direction, over a shorter distance, leading to a higher carrier collection efficiency.[23] Due to the preference of the radial geometry, axial p-n junction silicon NW solar cells have received significantly less attention in comparison. The most recent work concerning the axial junction geometry shows an efficiency of around 8%.[23] Aluminum oxide has been shown to be an effective surface passivation layer to improve silicon NW photovoltaic device performance.[5,24] Furthermore, these arrays of NW solar cells can be embedded in a polymeric matrix to realize a flexible NW solar cell that can be incorporated in a variety of real world applications.[25]

2. EXPERIMENTAL METHODS

Beginning with a bare p-type (100) silicon substrate, nanosphere lithography was used to provide the pattern for the nanowires that will be fabricated. Amidine functionalized polystyrene nanospheres are injected at the interface between hexane and water; they self-assemble into a non-closed packed monolayer at the interface, primarily due to long range electrostatic forces. The pitch of the nanosphere array can be independently tuned by injecting more or less nanospheres at the interface, and two different nanosphere diameters were used - 200 nm and 300 nm. To transfer the nanosphere pattern, the substrate is withdrawn through the interface, collecting the nanospheres, which are bound to the substrate due to their charged surface. The nanosphere lithography process is visualized in figure 3. With the nanospheres transferred to the substrate, 35 nm of gold was evaporated over the nanosphere array, and the nanospheres were then removed with sonication in toluene, leaving behind a nanoporous gold mask that will be used for metal-assisted chemical etching (MacEtch). The process flow following this step can be visualized in figure 1.

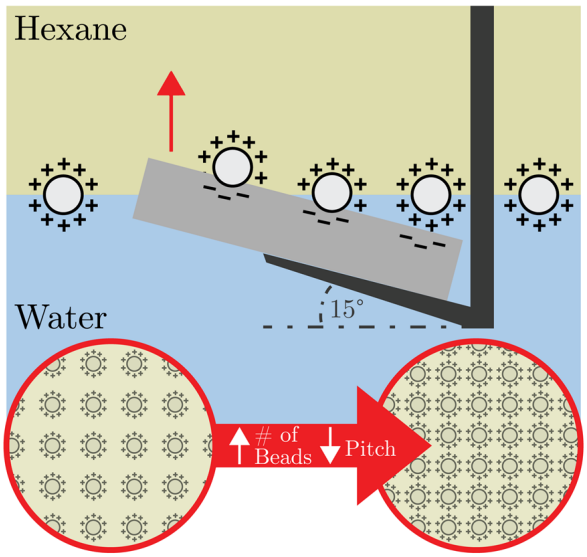

Figure 3. Visual representation of the nanosphere lithography process.

Hydrofluoric acid (HF), hydrogen peroxide (H_2O_2), and ethanol are mixed in various ratios to study the effect of the H_2O_2 concentration on the etch rate of the MacEtch process. The substrate with the nanoporous gold mask is immersed in a solution of hydrofluoric acid, hydrogen peroxide, and ethanol. The peroxide is reduced at the gold surface in a cathodic reaction, generating holes which are injected through the gold,

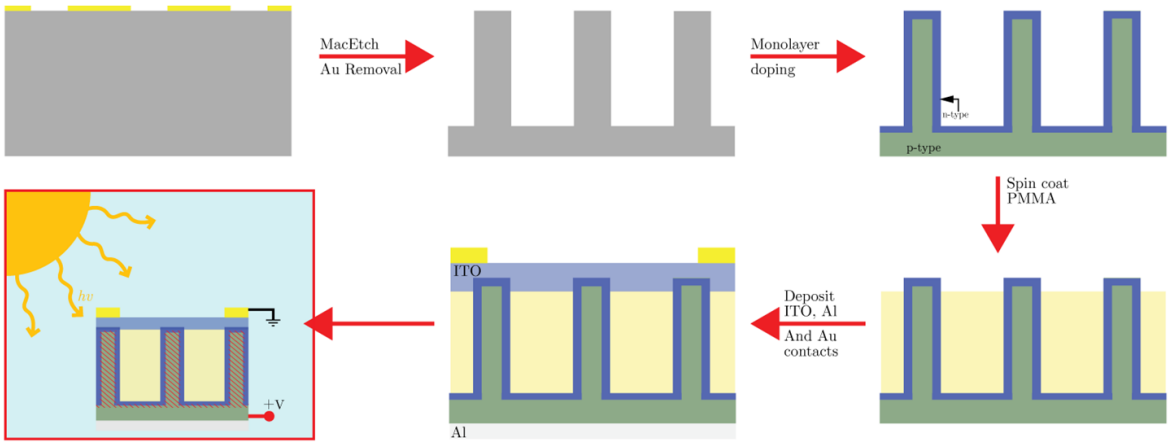

Figure 1. The process flow following the nanosphere lithography and metal-assisted chemical etching steps.

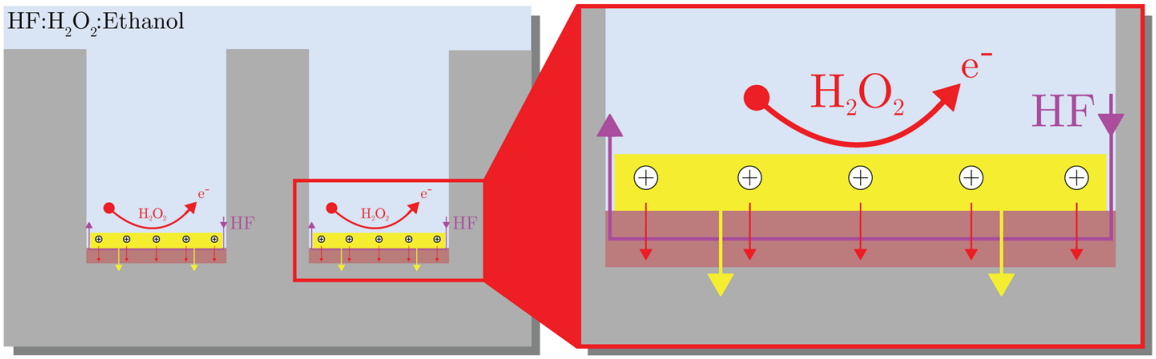

Figure 2. Visual representation of the MacEtch process.

causing the localized oxidation of the underlying silicon. The oxidized silicon is dissolved by the HF, causing the gold to sink into the substrate as etching proceeds. The MacEtch process is shown in figure 2, and the resulting generated nanowire array can be seen in 4. After etching, the gold mask is removed using a KI gold etchant from Transene. The optical reflectance of the nanowire array is then measured using a Filmetrics F20 tool.

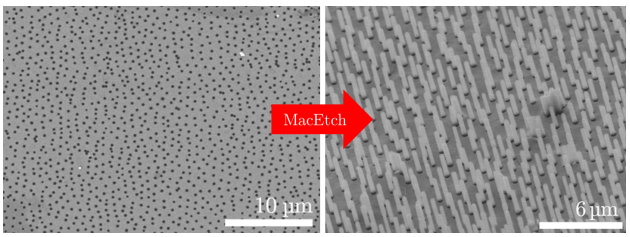

Figure 4. The nanoporous gold mask generated after nanosphere lithography in preparation for MacEtch, and the resulting NW array.

With the nanowire array generated, monolayer doping was done to form a radial p-n junction inside the nanowires. The monolayer doping solution was prepared in a glove bag under argon since diethyl vinylphosphonate (DVP) is sensitive to air and water vapors. DVP was combined with mesitylene in a 1:25 ratio by volume. After the solution was mixed, it was removed from the glove bag and sparged with argon for 15 minutes. While the solution was sparged, the MLD chamber is heated to 120 °C using a hotplate. Next, the chamber is backfilled with argon and the DVP/mesitylene solution is poured in. The samples were placed in the solution, and the chamber is closed. After two hours, the sample is removed and rinsed in toluene, acetone, methanol and DI water. The sample is then annealed with a rapid thermal anneal step at 1000 °C under N2 for 30 seconds to drive in the dopant molecules and burn off the excess organic molecules. A 30 second HF dip was done after the MLD process to ensure no leftover organic residue remained, and to remove any oxide that may have grown in the RTP step.

To encapsulate the nanowire array, PMMA was spin

coated at varying speeds with either PMMA A4 or A11 depending on nanowire height. The PMMA was hard baked at 180 °C for 15 minutes harden the material and to evaporate excess solvent. The PMMA was etched back using a pure oxygen plasma in a LAM 490 plasma etcher with a flow rate of 100 sccm O_2, at a gap of 1.65 cm, a power of 100 W, and a pressure of 120 mTorr to expose the tips of the nanowires. After the PMMA was etched back, the transparent conductor, indium tin oxide (ITO), was sputtered over the tips of the nanowires using a CVC 601 DC sputter system. The ITO is presputtered with 40 sccm Ar and 1 sccm O_2 at a DC power of 325 W, a base pressure of $\approx 6 \times 10^{-6}$ Torr and a sputter pressure of 5 mTorr. The transmission of the ITO layer was measured with a Woolam Varible Angle Spectroscopic Ellipsometer (VASE), while the resistivity of the film was measured with a CDE Resmap tool. Next, the backside of the of the substrate was etched in the Drytek Quad Reactive Ion Etcher with an SF_6/Ar plasma with 100 sccm SF_6 and 50 sccm Ar at a power of 200 W and a pressure of 120 mTorr. Approximately 500 nm of aluminum was evaporated as the back contact of the device with the CHA Flash Evaporator. The final step of the process flow includes depositing approximately 200 nm of gold by sputtering as the top contact of the device using a bench top sputter tool that was used as the top contact for probing in testing. The remaining process flow after nanosphere lithography and metal-assisted chemical etching can be seen in figure 1. An enclosed dark probe station was used to test the dark current-voltage characteristics of the solar cells, while a TS Space Systems two-zone close match solar simulator was used to match the AM1.5 solar spectrum to measure the illuminated current-voltage characteristics of the solar cells.

3. RESULTS

The dependence of the etch rate on H_2O_2 concentration in the MacEtch process was studied in order to determine which H_2O_2 concentration should be used for a moderate etch rate while minimizing the porosity of the silicon nanowires (this is a function of time and peroxide concentration). The concentration of the peroxide was varied, with a constant etch time of 20 minutes. The resulting etch rate was measured - the results from this study can be seen in figure 5.

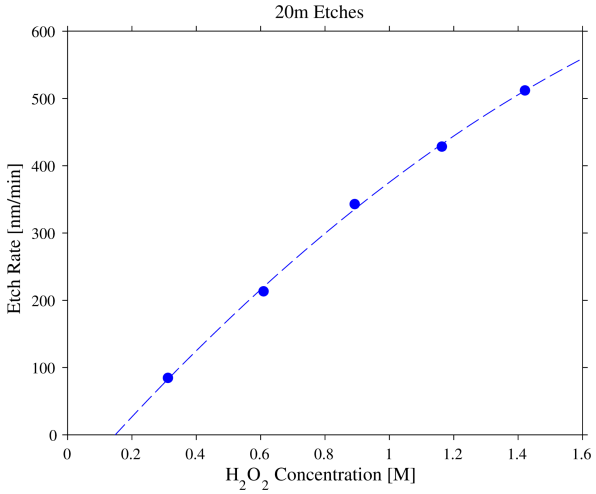

Figure 5. The dependence of the etch rate on the peroxide concentration in the MacEtch process.

Using the results from the previous experiment, a H_2O_2 concentration of ≈ 0.32 M was used for the remainder of the processing. The optical reflectance of various nanowire arrays was studied as a function of nanowire diameter, pitch, and height. Nanowire arrays were generated with 200 nm diameter wires at 600 nm and 800 nm pitch, and 300 nm diameter wires at 900 nm and 1200 nm pitch at varying heights. For reference, the optical reflectance of bare silicon is shown in figure 6. The optical reflectance curves for the generated nanowire arrays can be seen in figure 3.

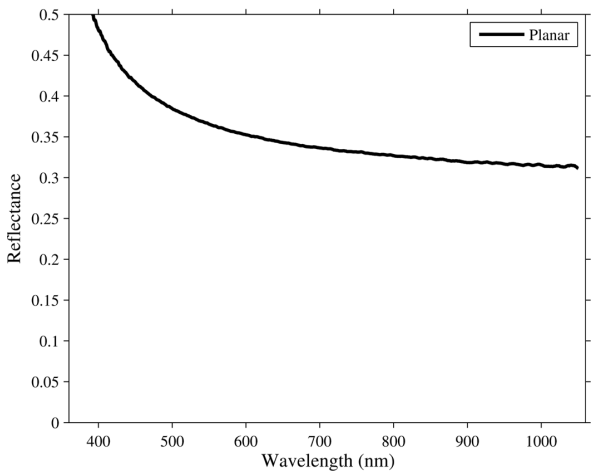

Figure 6. The reflectance of a bare silicon wafer.

From these optical reflectance results, it is determined that 300 nm diameter wires at 900 nm pitch will be the best candidate to fabricate solar cells with, due to their ability to reach sub 1% reflectance at a moderate 3 µm height, and their ability to absorb more light

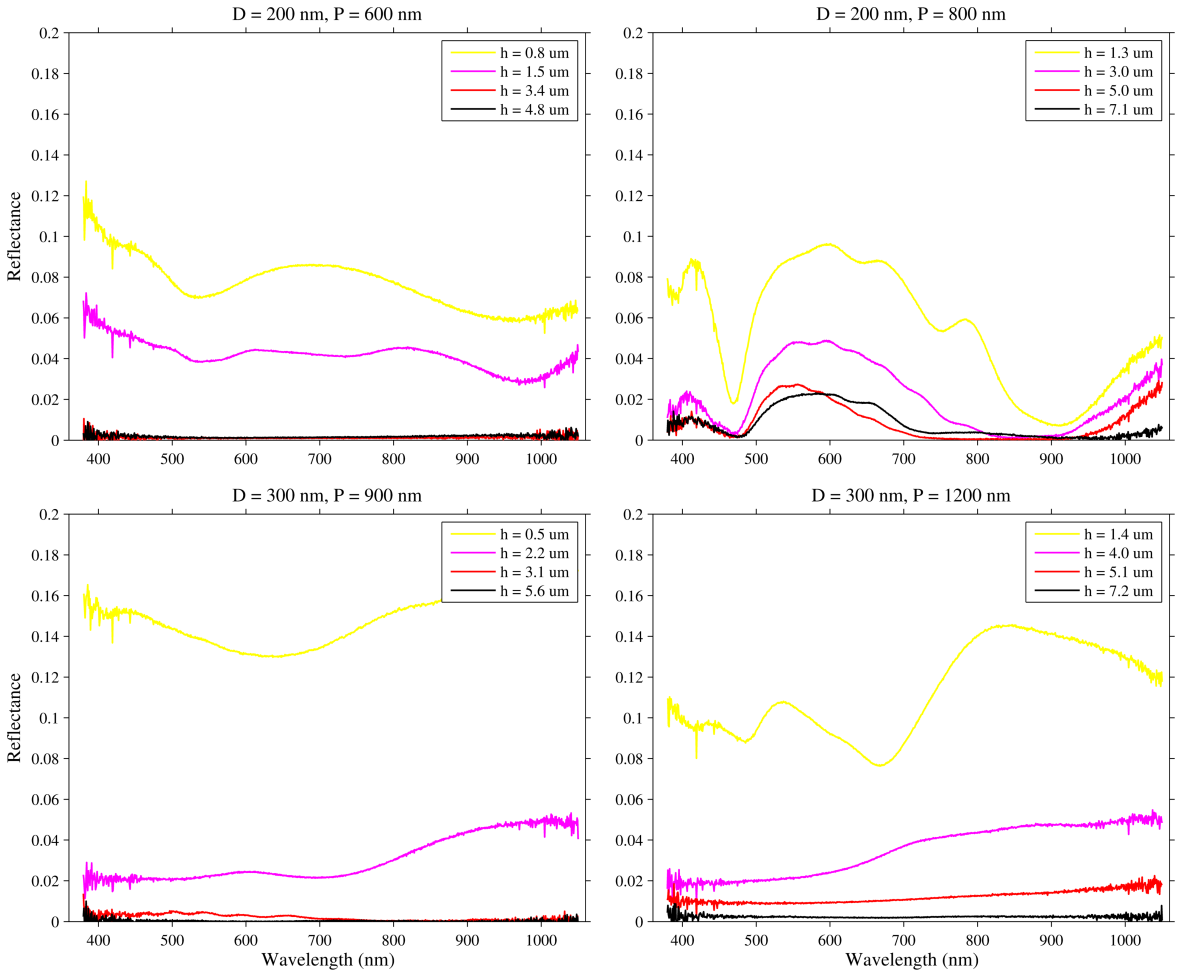

Figure 7. The optical reflectance of nanowire arrays with various diameters, pitches, and heights.

than the 200 nm wires. Multiple nanowire samples were generated with this nanowire arrangement and underwent the MLD process. A planar silicon sample was included in the MLD step, and was used to measure to sheet resistance change as a result of the process due to the inability to measure with the NW samples. Before the MLD step, the planar sample measured 8 Ω/□ p-type, and after the MLD step, it measured 16 Ω/□ n-type. The nanowire arrays were coated with PMMA according to their height, and etched back to reveal ≈ 200 nm of the wires for electrical contact. The etch rate of the PMMA was measured to be $200^{nm}/_{min}$ when deposited on a planar substrate, but the etch rate increased to $300^{nm}/_{min}$ when encapsulating the nanowire array. The PMMA encapsulation process can be seen in figure 8. After the etch back of the PMMA, the top conductor was deposited. The transmission and sheet resistance of this 200 nm thick ITO layer was measured in order to ensure that the transparent conductor was deposited transparent, and conductive, as intended. The sheet resistance measured was as low as 28 Ω/□, indicating a sufficiently conductive layer. The transmission was measured to be greater than 50% over most of the wavelength range of interest, as seen in figure 9, which matches closely with previous work.[26]

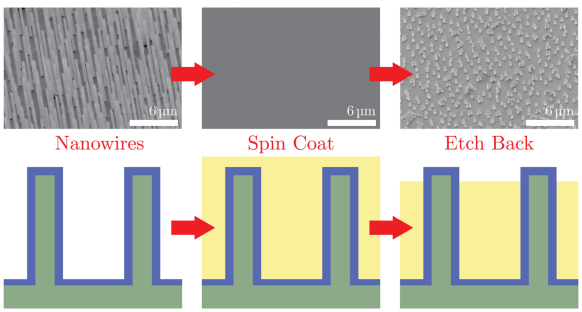

Figure 8. The PMMA spin coat and etch back process shown visually.

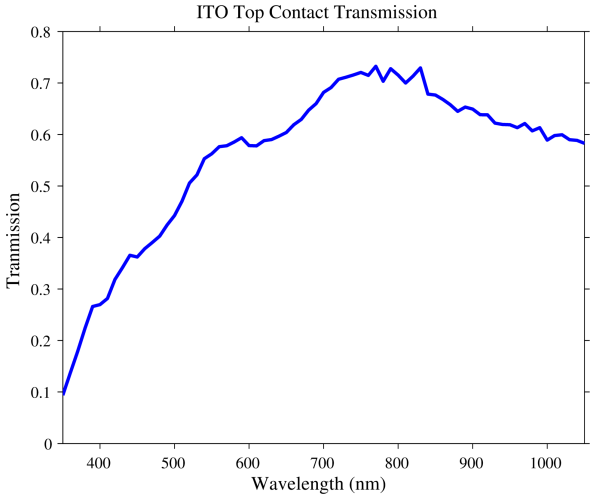

Figure 9. The transmission of the 200 nm ITO layer as deposited.

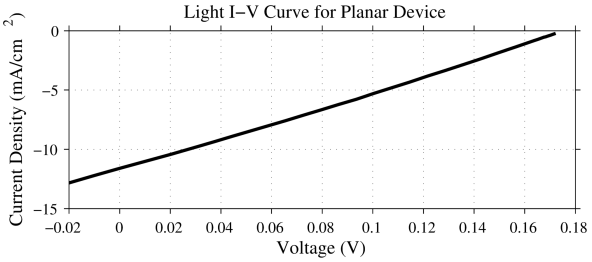

Figure 11. The illuminated IV curve of the planar device.

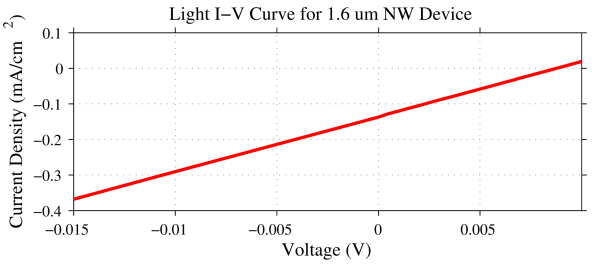

Figure 12. The illuminated IV curve of the short wire device.

The test results for the solar cell devices fabricated can be seen in figures 10, 11, and 12. A nanowire device with 1.6 µm wires at 300 nm diameter and 900 nm pitch was successfully fabricated and tested. Additionally, a planar device with the same MLD process and contact stack as the wire device was fabricated and tested as a reference. The nanowire device and the planar device active areas were around 0.5cm^2.

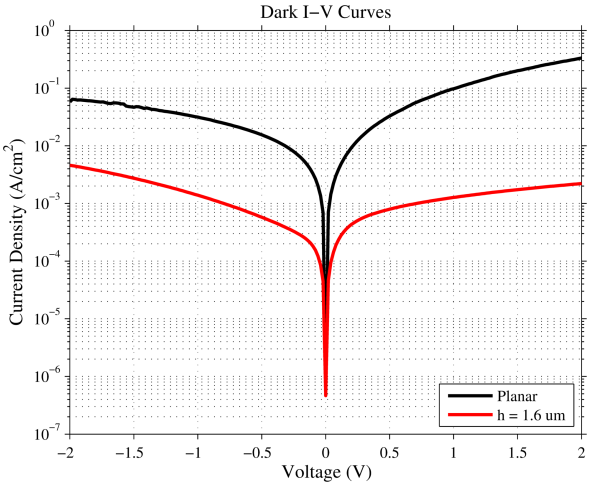

Figure 10. The dark IV curves of the two fabricated devices.

4. DISCUSSION

The etch rate of the metal-assisted chemical etching process used in conjunction with nanosphere lithography was successfully characterized as a function of peroxide concentration and time, leading to efficient generation of silicon nanowire arrays. The optical reflectance of these SiNW arrays was studied as a function of nanowire diameter, pitch, and height. Less than 1% reflectance was achieved over the 300 to 1000 nm wavelength range for both 200 nm and 300 nm diameter wire arrays at different pitches and at as low as 3 m wire heights. As expected, the smaller the pitch, the more effective the light trapping within the nanowire array, and the lower the reflectance. Similarly, taller wires corresponded to a decreased amount of reflected light. The 300 nm diameter, 900 nm pitch nanowire array was determine to be the most effective in terms of absorbing incoming light, and was chosen as the arrangement to fabricate solar cells. The planar device that was fabricated with the same contact stack as the nanowire device showed the expected rectification behavior, as seen in figure 10. The short wire device with 1.6 µm tall wires also showed slight rectification, as seen in figure 10, however, it is not the behavior expected from a typical p-n junction diode. The short wire device also showed some light-generated current, although much less than the planar device. With a very low open circuit voltage and short circuit current density, the NW device did not show significant light-generated current as would be expected with a true p-n junction. The long (7 µm) wire devices that were fabricated failed to

show any measurable light-generated current, and the dark current-voltage characteristics of those devices resembled that of resistors, showing no rectification.

There are a few things that could explain the poor nanowire device performance. There was a lack of surface passivation on the nanowires, which likely resulted in surface charge depletion along the nanowire sidewalls, ultimately leading to degraded device performance. This surface charge depletion behavior has been examined in previous work by Parsian K. Mohseni, et. al.[27] Upwards band bending near the nanowire sidewalls due to the un-passivated surface and build up of negative surface states generates a built-in electric field, causing electrons to be trapped in the inner part of the nanowire. In the case of the longer wire devices, the increased surface area of the wires may have led to incomplete coverage of the dopant molecule in the MLD step, resulting in no junction formation. Similarly, this could have been the case for the short-wire devices, as there was not significant rectification even in the planar device that is typically seen wih a p-n junction diode. However, if the nanowires were successfully doped, it is possible that the wires were fully depleted due to the high surface concentration and ultra-shallow junction generated by the MLD process. Additionally, there was high contact resistance, due to the inability to sinter the backside contacts, since having the PMMA present restricts processing temperatures to below around 250 °C. All of these effects contribute to the poor device performance observed in the nanowire device.

5. CONCLUSIONS

In conclusion, silicon nanowires were successfully fabricated with a combination of nanosphere lithography and metal-assisted chemical etching in a new-to-RIT process. The optical reflectance of different nanowire arrangements was studied as a function of nanowire height by changing the nanosphere lithography and MacEtch parameters. In the end, diode behavior was not observed with the nanowire devices as expected. There are a number of things that could have effected the nanowire device performance, such as the wires being doped but fully depleted, the surface charge depletion on the nanowire sidewalls hindering device performance, or that the p-n junction wasnt actually formed, meaning that the light-generated current was only from the ITO silicon junction. More work is needed to determine which of these things actually happened, however, it is safe to conclude that diode behavior was not observed as expected. Regardless, the fabrication process for generating silicon nanowires via NSL and MacEtching was demonstrated, characterized, and implemented in a full device process flow to allow for future work to build upon the work presented here.

6. FUTURE WORK

To address and prove that these issues are the reason for the poor device performance, future work could include an extended study with the MLD process on the silicon nanowire arrays to better characterize the effect of the geometry on the self-assembly and drive-in of the dopants. Additionally, for the entirety of this project, the ion implanter was out of service. Future work could use the ion implanter to form an axial junction at the beginning of the process instead of using the MLD method. The process could also be altered slightly to allow for sintering of the backside contact, to reduce the contact resistance in the device. Finally, different surface passivation techniques could be tested, such as alumina, silicon nitride, or silicon dioxide coatings on the wires to prevent the surface charge depletion along the nanowire sidewalls that may be degrading device performance.

7. ACKNOWLEDGMENTS

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