

ENHANCED BORON ACTIVATION IN XENON FLASH LAMP ANNEALED POLYSILICON THROUGH PRE-AMORPHIZATION

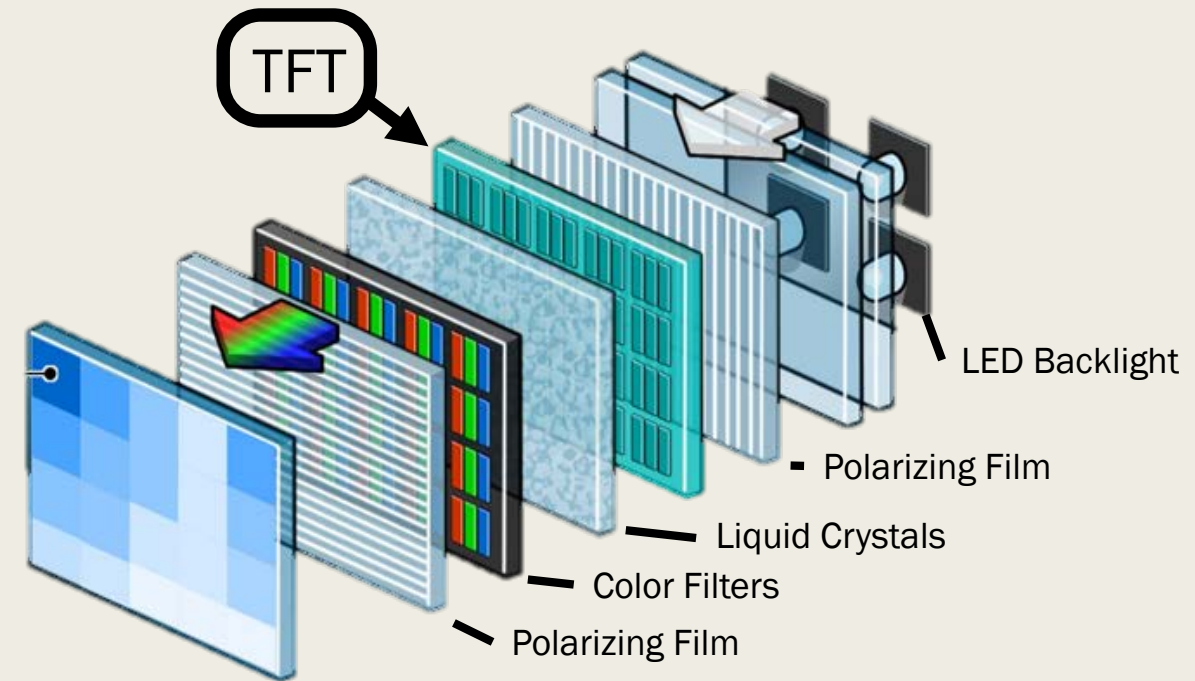
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Overview of Thin Film Transistors (TFTs)

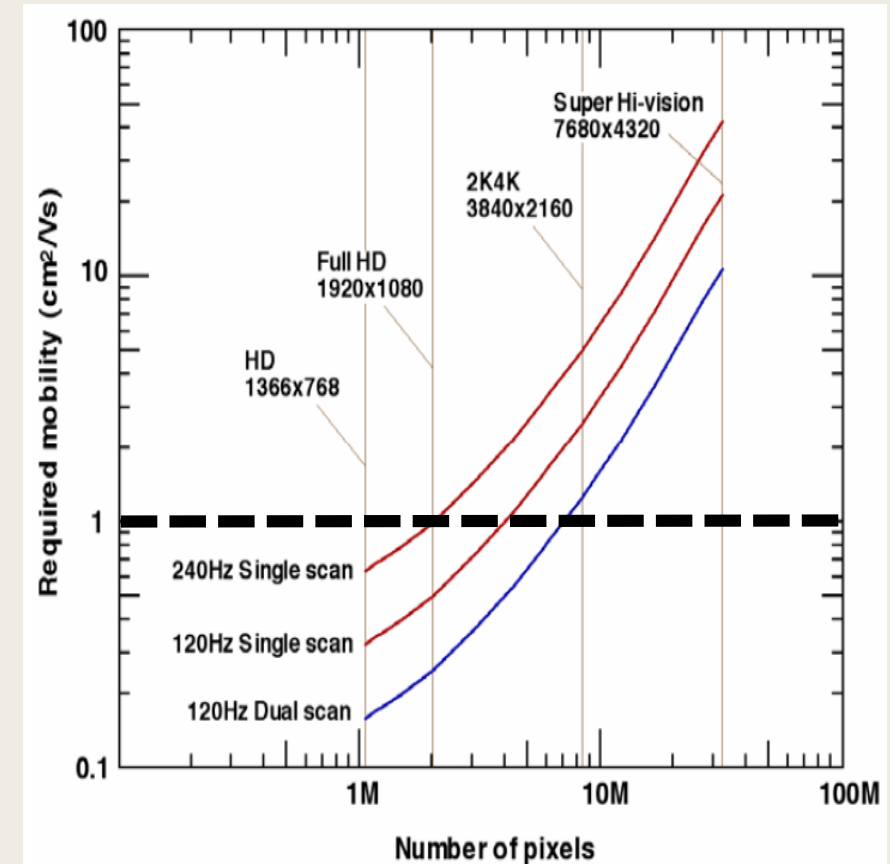
- Individual pixels of LCD and OLED displays are controlled by a TFT backplane
- Controls voltage applied to liquid crystal or current to OLED
- Majority of TFTs in production are made from amorphous silicon (aSi:H)
- Devices are limited to NMOS only and have electron mobility less than $1\text{cm}^2/\text{Vs}$



Expanded view of a LCD display[1]

TFT Overview Continued

- Next generation displays require TFTs made from higher mobility materials
- CMOS TFTs allow for incorporation of external control circuitry to be incorporated onto display
- Devices fabricated using flash lamp annealed polysilicon (FLAPS) have CMOS compatibility, high mobility, scalability, and are compatible with existing manufacturing



Carrier mobility requirements for different display configurations[2]

Overview of Flash Lamp Annealing (FLA)

- The sample, amorphous Si on glass, is heated and exposed to a pulse from broad-spectrum Xe flashbulbs
- Si film absorbs light, rapidly heating and melting
- Glass substrate doesn't absorb light, staying below the thermal limit
- Si recrystallizes resulting in a polycrystalline film
- Flash lamp system is scalable allowing larger displays to be fabricated

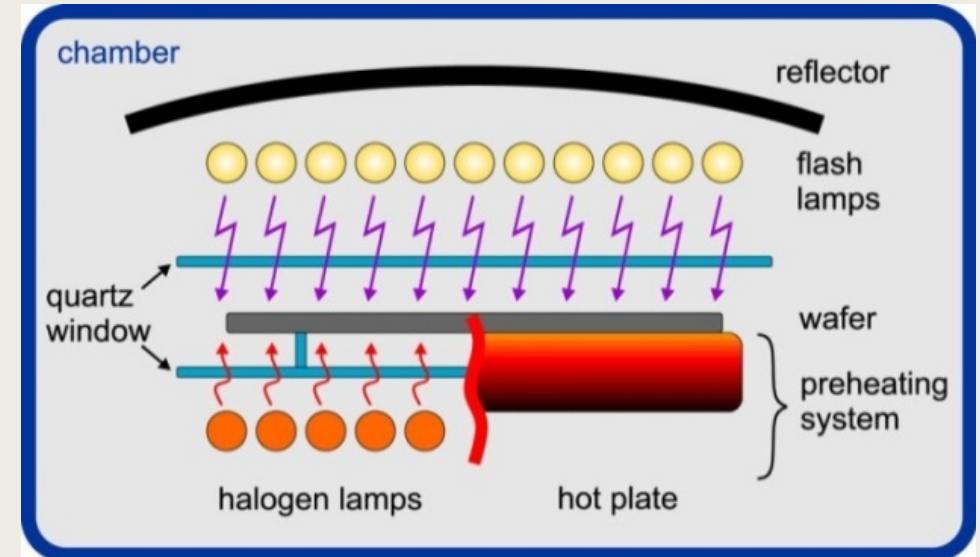
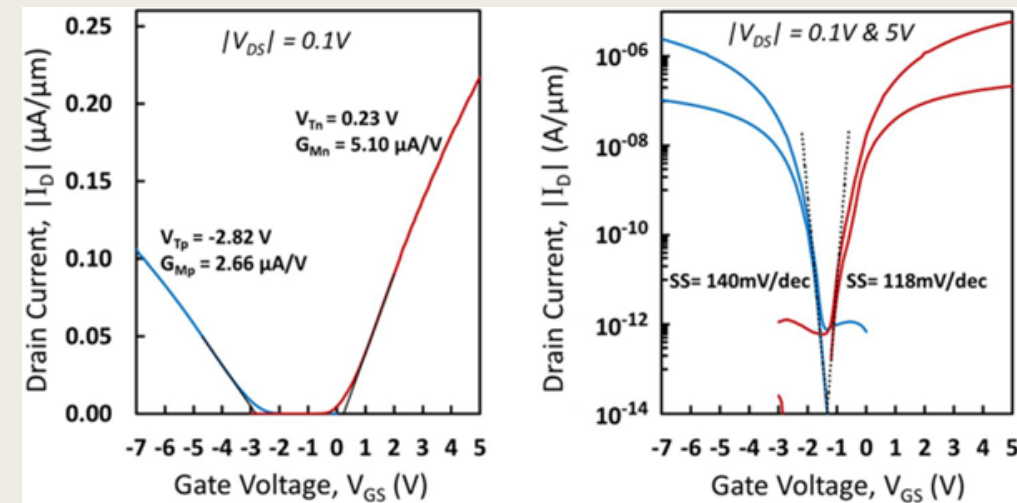


Illustration of FLA setup[3]

Previous Work at RIT

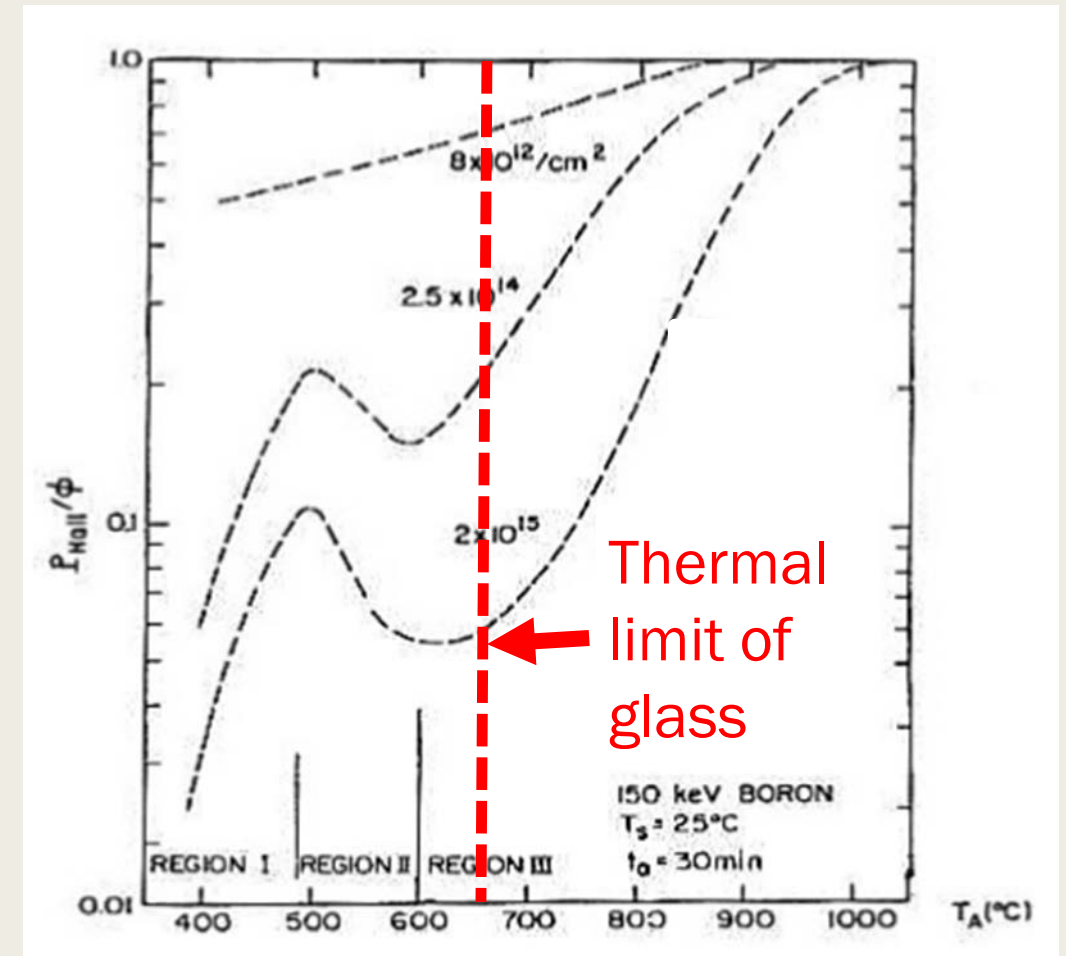
- FLAPS TFT have been fabricated with the source/drain implant prior to FLA, being activated during
 - Large devices worked but had significantly reduced effective channel length due to dopant diffusion during the Si melt
- Devices were subsequently fabricated with the implant occurring after FLA
 - Devices worked but the performance suffered due to low dopant activation in the source/drain
 - This was especially bad in PMOS devices



Best-case linear & log scale CMOS transfer characteristics from FLAPS TFTs with $L_{\text{mask}} = 32$ μm and $W = 100$ μm . [4]

Problem Statement

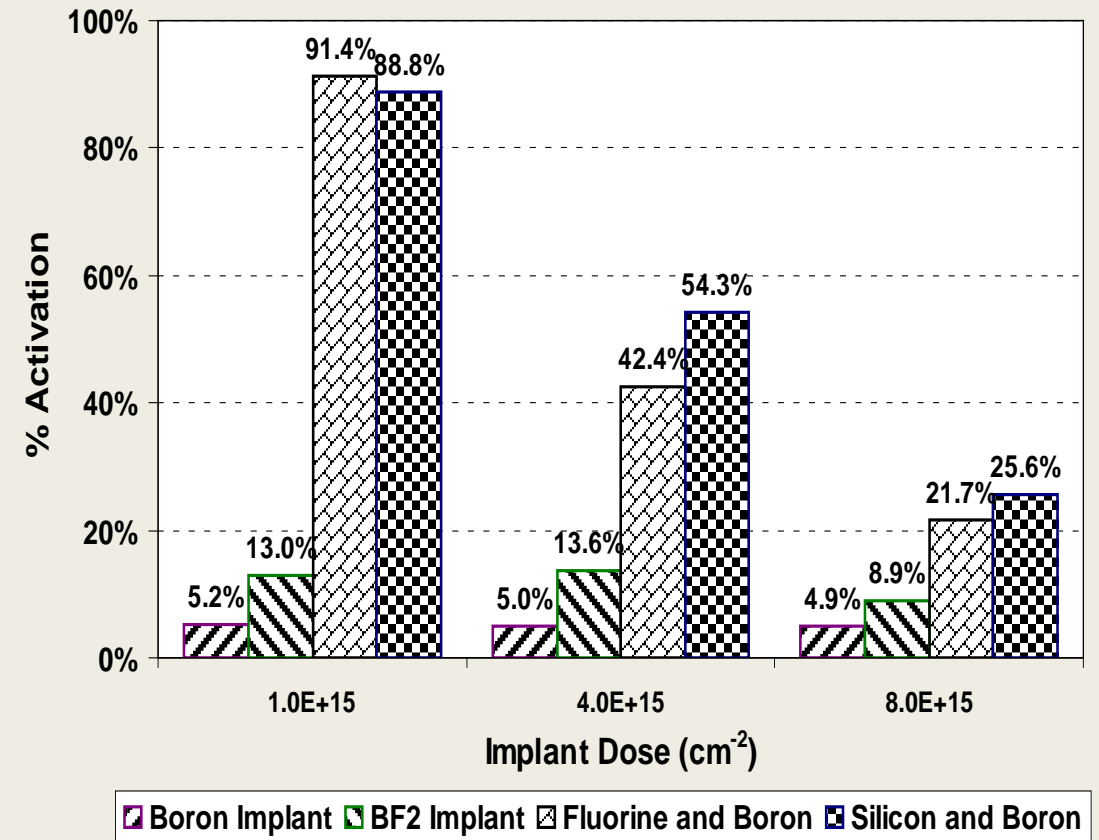
- Boron ions have difficulty creating Si displacements, which assist in activation, due to the small atomic mass and film limitations
- Diffusion processes are limited by the thermal limitation of the glass
 - This is why PMOS devices have activation problems



Boron activation vs temperature[5]

Activation Through Pre-Amorphisation

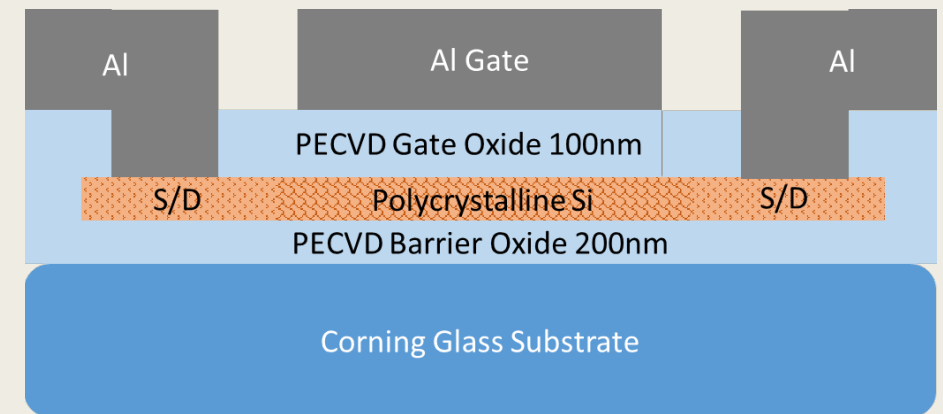
- Previous work with crystalline silicon shows that the addition of fluorine ions through implant increases the boron activation at low temperatures [6]
- Implant results translated well to thin film crystalline Si
- The fluorine ions are hypothesized to amorphize the Si resulting in higher activation during the anneal
- For this study fluorine implant doses of $1 \times 10^{15} \text{ cm}^{-2}$ and $5 \times 10^{15} \text{ cm}^{-2}$ at 75 keV were chosen



Addition of fluorine in crystalline Si [6]

Device Fabrication

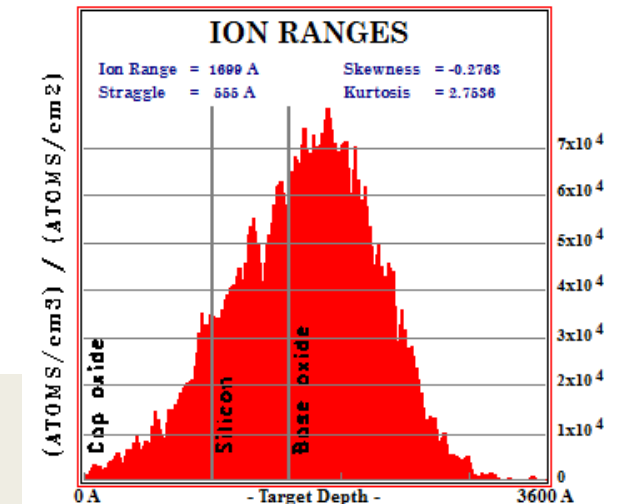
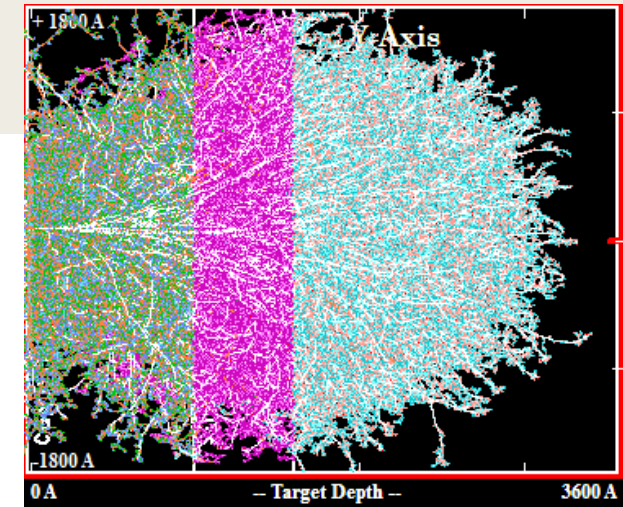
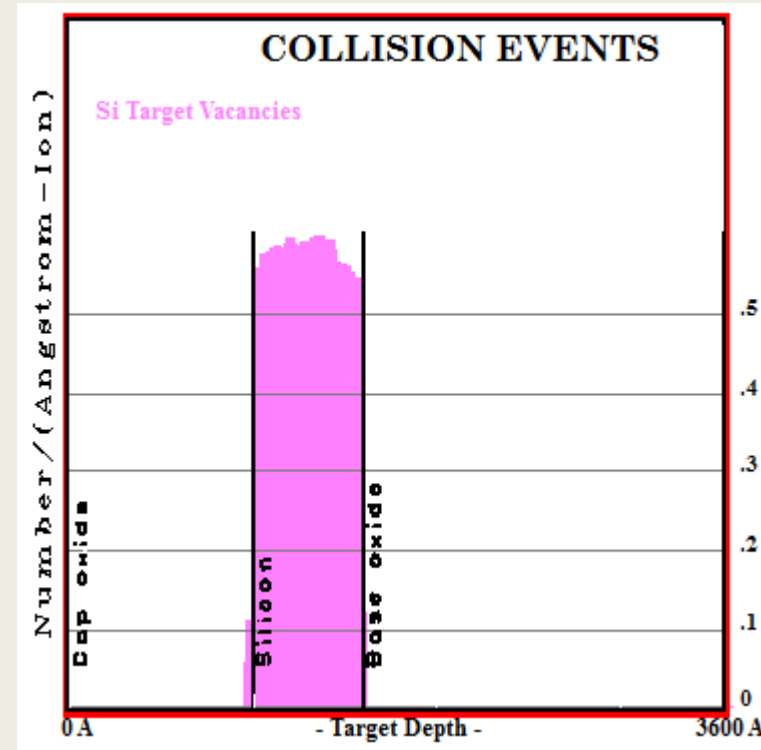
- Devices were fabricated using a previously developed FLAPS TFT process
 - Patterned a-Si mesas
 - 100nm SiO₂ capping layer
- Samples were preheated to 500 °C on an enclosed hotplate
- They were flashed at 505V for 250μs resulting in an exposure energy of 5.1 J/cm², measured by bolometer
- As part of the source/drain implant, fluorine was implanted before the boron



Device cross section

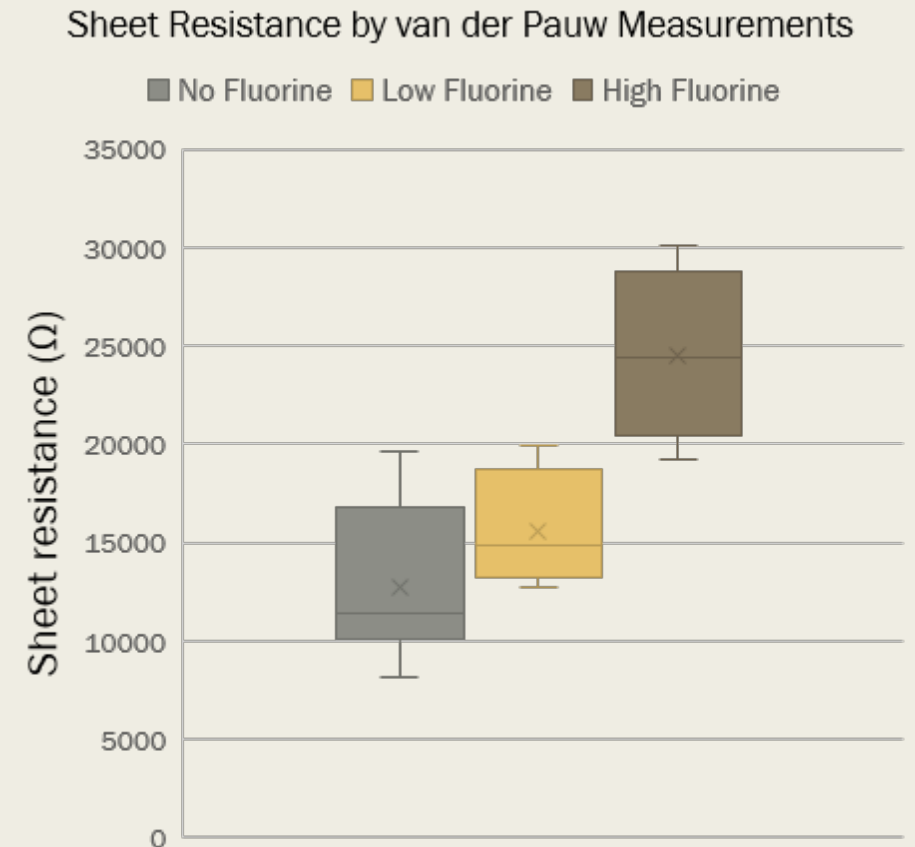
Fluorine Amorphization in Source/Drain

- SRIM simulation was performed to verify implantation settings
- Peak of the fluorine implant is below the silicon
- SRIM displacement profile suggests complete amorphization at fluorine dose 10^{15}cm^{-2}
- May offer boron activation enhancement as demonstrated in thin film crystalline Si

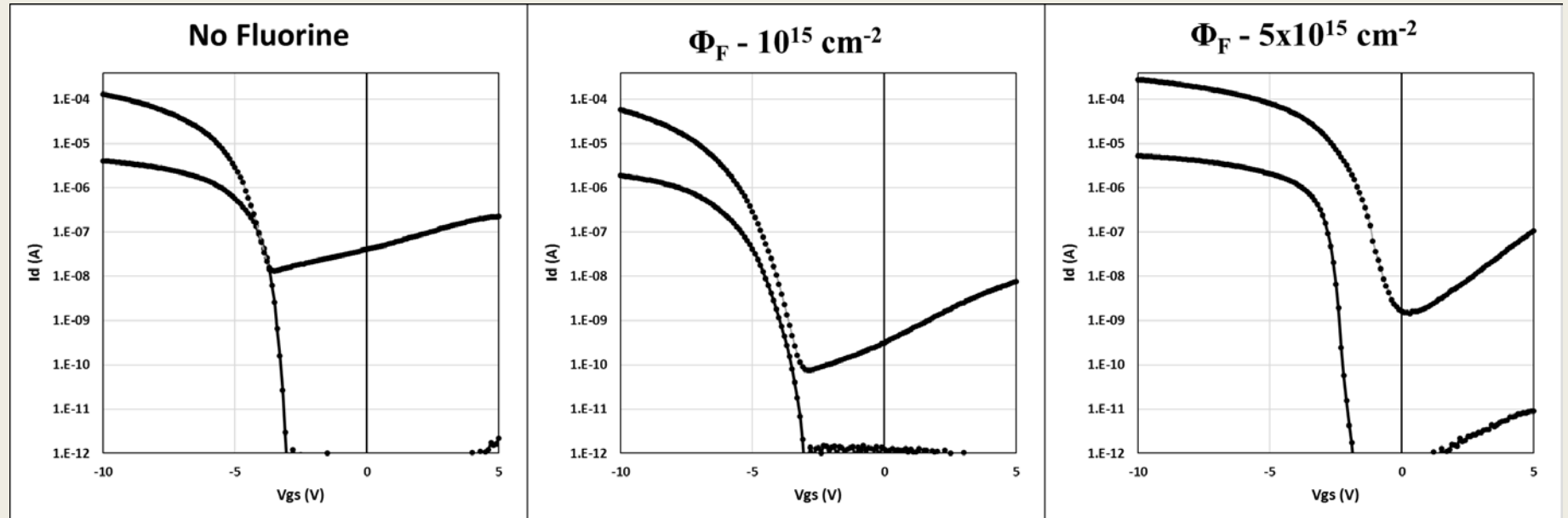


Impact of Fluorine on Sheet Resistance

- Sheet resistance was measured using van der Pauw test structures
- The sheet resistance increases as fluorine dose increases
- Source/drain mesa regions and van der Pauw structures are not perfectly analogous due to the directionality and area dependence of FLAPS
- What about TFTs?



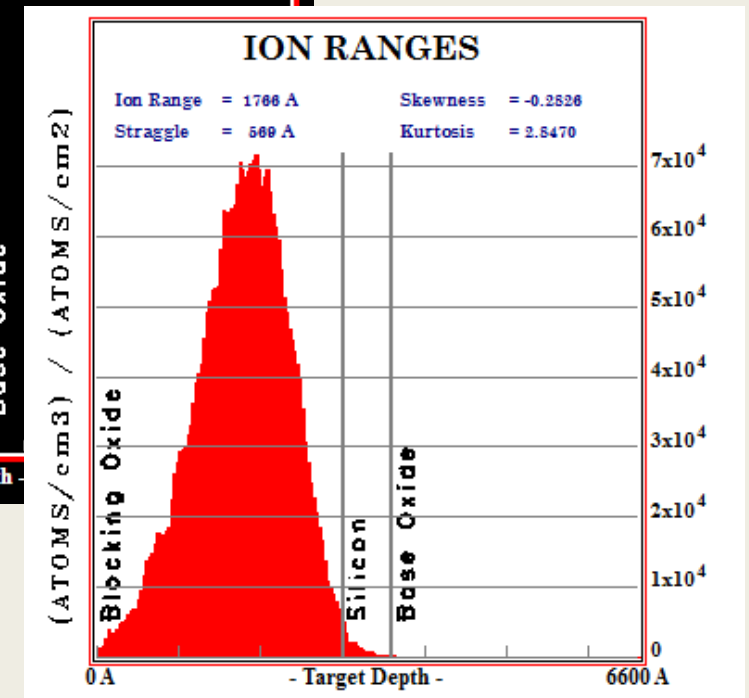
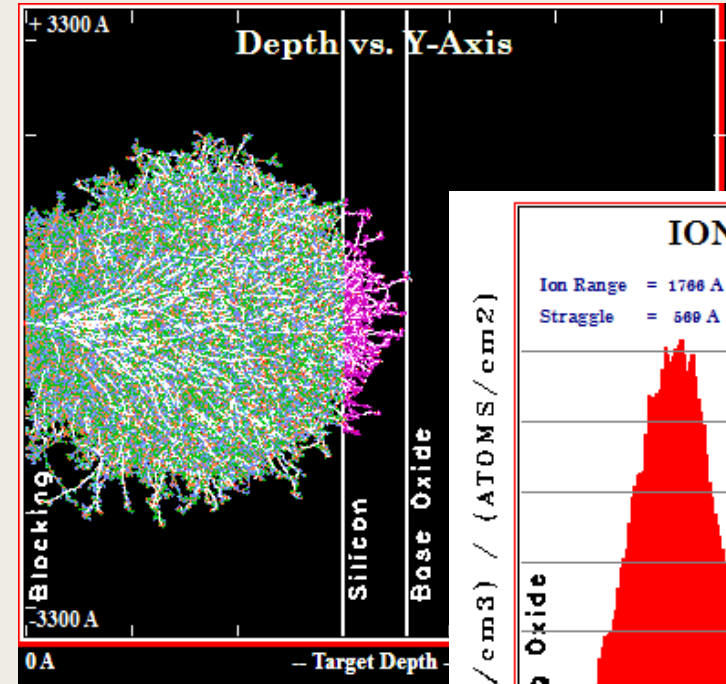
TFT Results



Linear V_T	-3.5 V	-4 V	-2.4 V
ΔV_T	0 V	0.3 V	2 V
μ_{lin}	24 cm ² /Vs	13 cm ² /Vs	28 cm ² /Vs
μ_{sat}	140 cm ² /Vs	70 cm ² /Vs	220 cm ² /Vs
I_{Dmax}	131 μ A	58 μ A	280 μ A

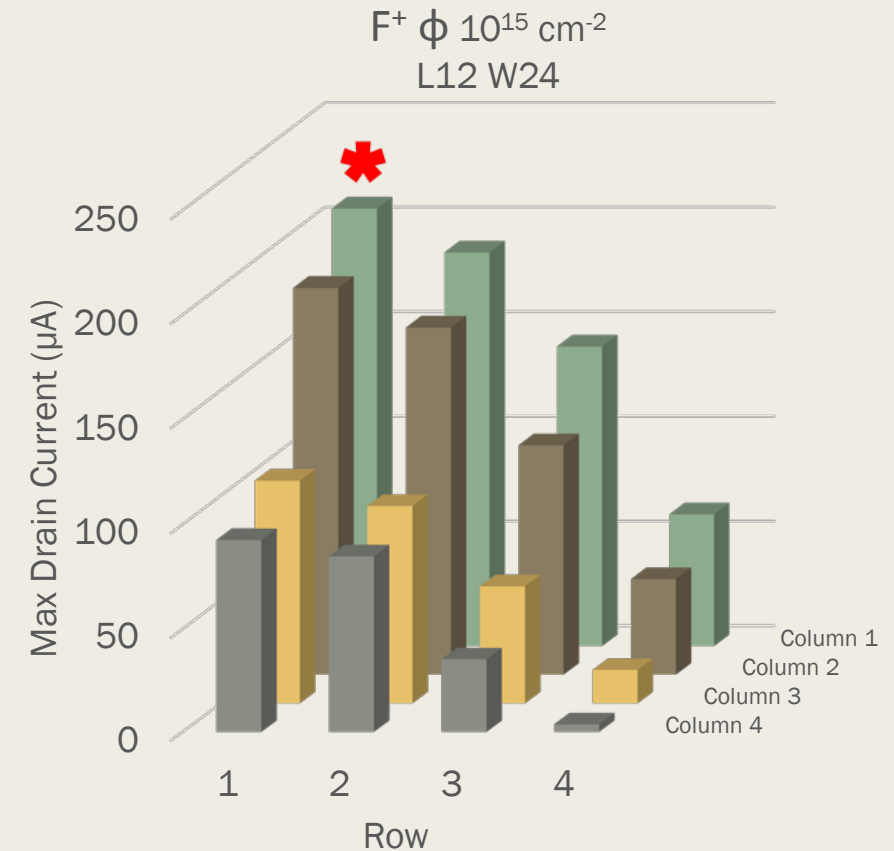
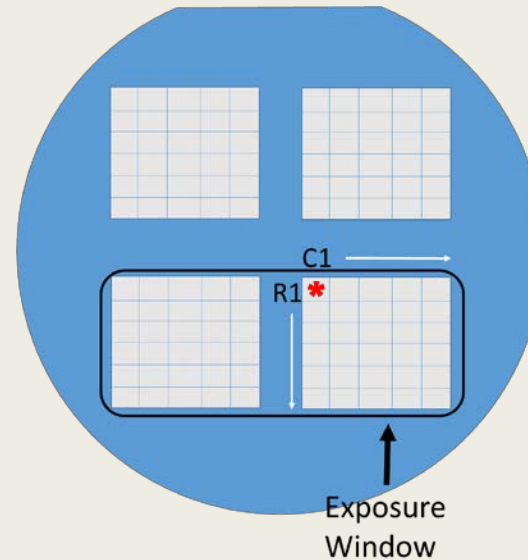
Fluorine related subthreshold degradation

- Presence of fluorine entering the channel may be the source of subthreshold degradation
- SRIM simulation confirms this possibility
 - Tail of fluorine implant made it through the blocking oxide



Location Dependence

- Device characteristics change consistently depending on location on wafer
- Most likely cause is variation in crystallinity due to non-uniform exposure condition
- Direct comparison between treatments difficult



Conclusion

- Increased current of devices with higher $^{19}\text{F}^+$ dose indicates lower series resistance
 - Formal separation of series and channel resistance is not possible due to inconsistencies in device operation
- High dose devices have less off-state gate control, high leakage and DIBL-like behavior
- Interpretation of the impact of fluorine on boron activation is compromised due to the likelihood of fluorine entering the channel
- Non-uniformity in the exposure window complicates direct device comparisons and statistical analysis
 - Improved system control needed to mitigate this issue
- Study is ongoing:
 - $^{19}\text{F}^+$ experiment replication with thicker blocking oxide
 - Additional investigation on $^{28}\text{Si}^+$ pre-amorphization

Acknowledgements

- Dr. Karl Hirschman
- Glenn Packard
- Corning Inc.
- Dr. Rob Manley
- Team FLAPS
- Patricia Meller
- SMFL Staff
- AM Print Center
- Dr. Rob Pearson
- Dr. Dale Ewbank

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