Vacuum Field Emission Devices with Integrated Carbon Nanotubes

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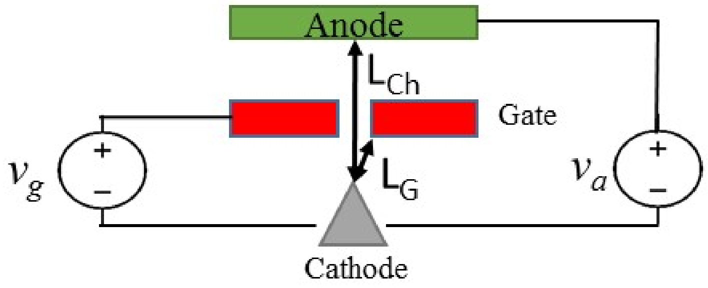
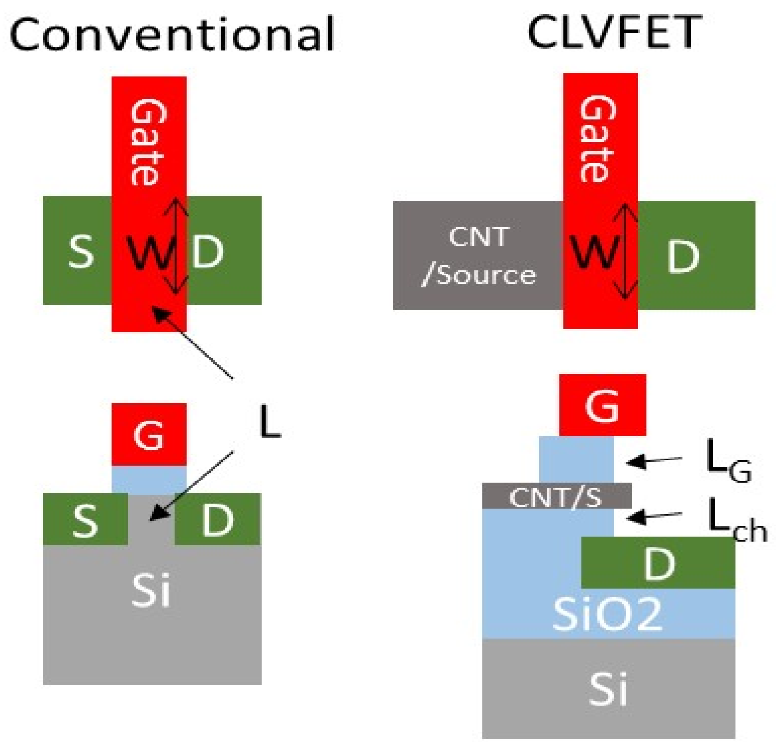
Introduction

- Investigate a vacuum field effect transistor device based on the electron emission of carbon nanotubes.
  - The proposed asymmetrical nanoscale vacuum FET will integrate carbon nanotube (CNT) emitters/cathodes in a lateral orientation and a vacuum channel in a vertical orientation (non-lithographically defined).
  - Create a two-electrode device (anode and cathode) as proof of concept and focus on material and process integration.





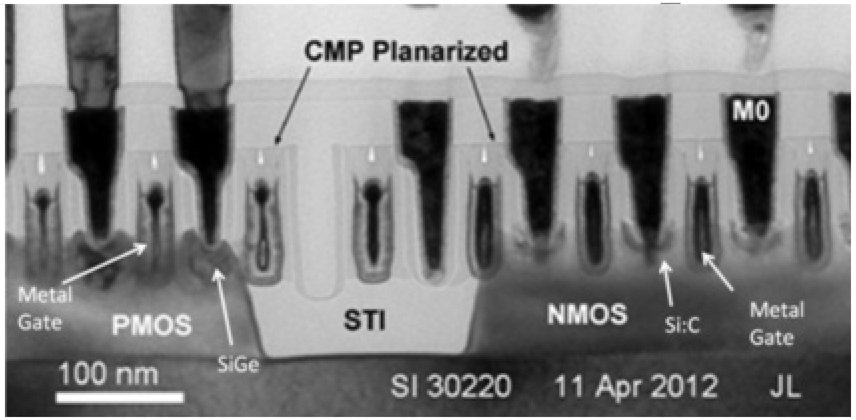
CNT-based Lateral Vacuum Field Effect Transistor

Design advantages over traditional and current Vacuum FETs

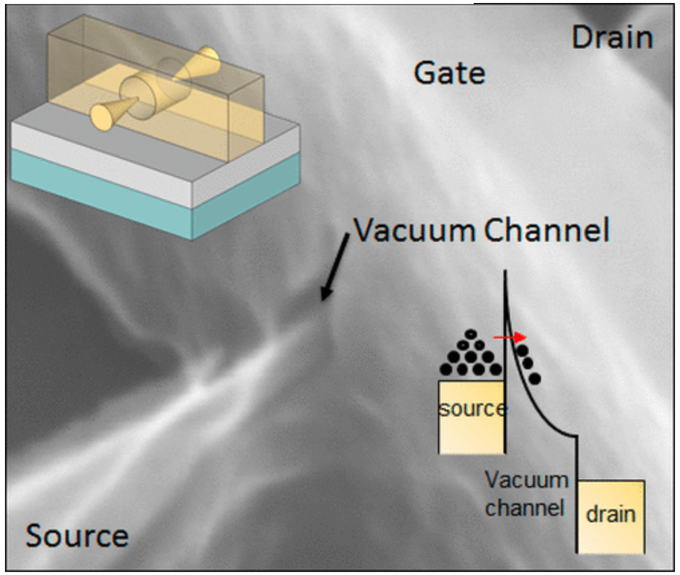
	SOA CMOS* 10 nm FinFET	Vacuum FETS** Silicon vacuum tube	Proposed CLVFET Lateral SWCNT emitter
Channel gate length	**10 nm** (immersion lithography))	**50 nm** (180nm-lithography and oxidation trimming)	**1 – 50 nm** (vertically defined by thin film deposition/ALD)
Source-to-gate distance	**0.8 nm** (high-k dielectric HfO_2 - equivalent oxide thick.)	**10 nm** (air gap)	**1 – 10 nm** (high-k dielectric equivalent thickness)
V_{DD}	**0.7 V**	**3 V**	**≤ 1.8 V**
I_{OFF}	**10 nA/µm** NMOS (VDS=0.7V)	**< nA** (~ nm tip) (VDS=2V)	**< nA/µm**
I_{ON}	**1.7 mA/µm** NMOS (VDS=0.7V)	**3 µA (~ nm tip)** (VG=3V)	**TBD/µm** or **/SWNCT**

*Etienne Sicard. Introducing 10-nm FinFET technology in Microwind. This paper describes the implementation of a high performance FinFET-based 10-nm CMOS Technology .. 2017.
**Jim-Woo Han, Dong-Il Moon, and M. Meyyappan, "Nanoscale Vacuum Channel Tansistor," Nano Lett. 2017, 17, 2146-2151

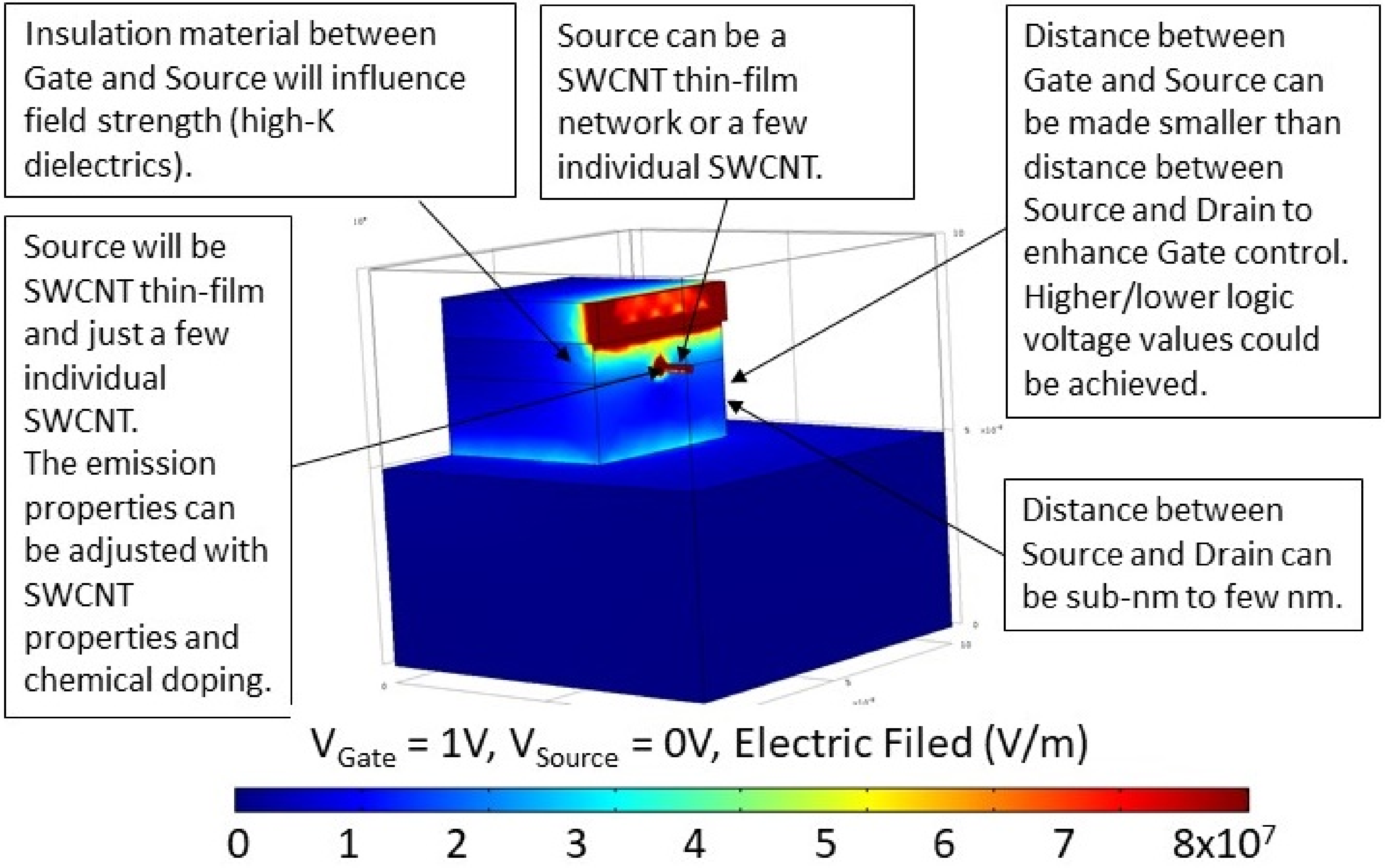
High complexity CMOS*



Si Vacuum FET**

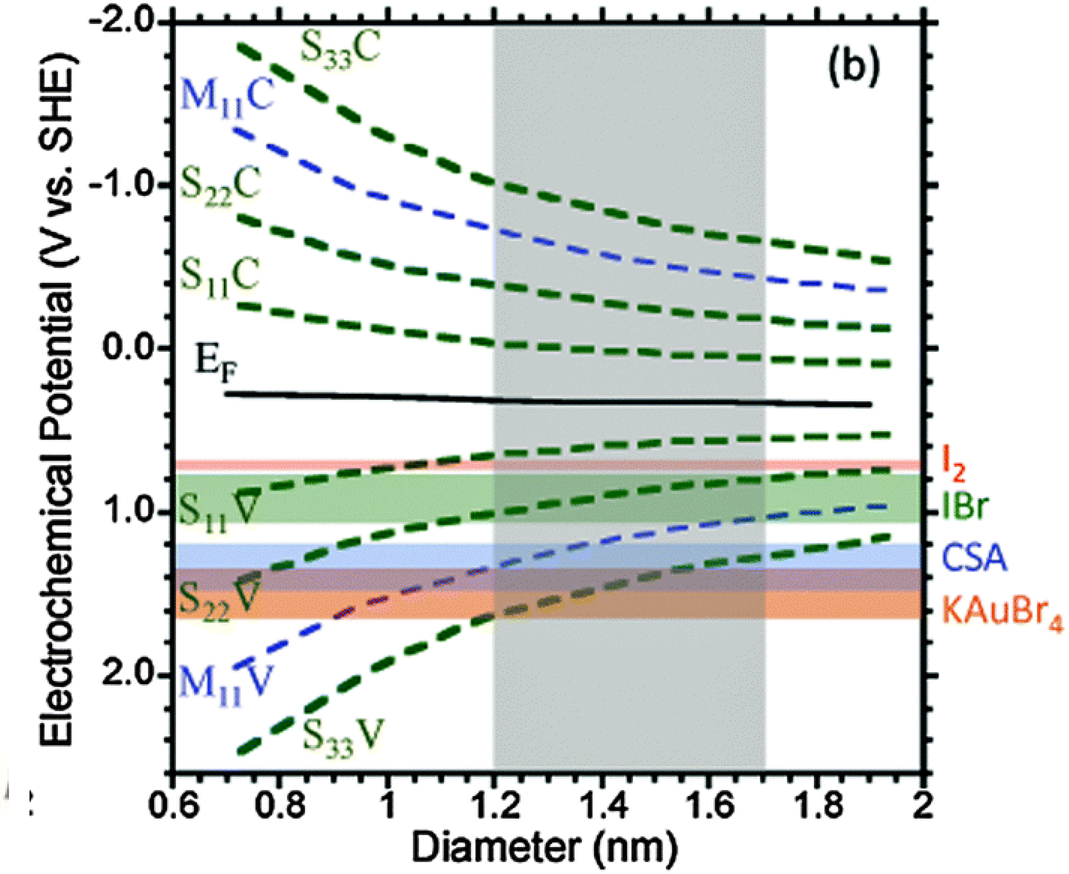


Design advantages over traditional and current Vacuum FETs



CNT (Carbon Nanotubes)

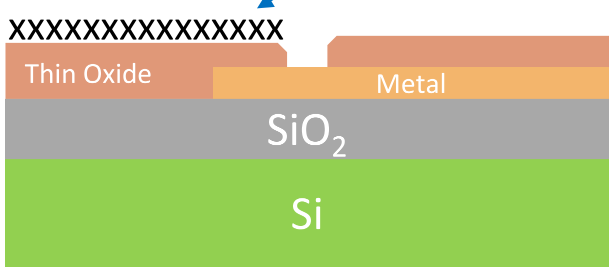
- Single-Wall Carbon Nanotubes (SWCNTs) could be the nanomaterial that replaces silicon in CMOS FETS (field-effect-transistors) and help us continue to follow Moore’s Law.
- SWCNTs posses remarkable properties such a high conductivity, radiation hardens (RADHARD) and **tunable** electron/hole emission properties.
- Currently BAE Systems and Nantero have already created a process of a hybrid CMOS-CNT device with RADHARD capabilities.

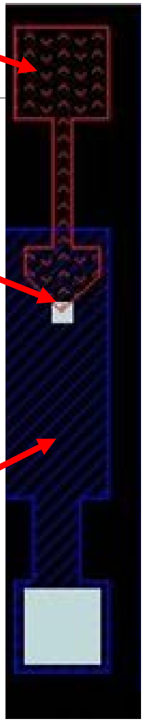


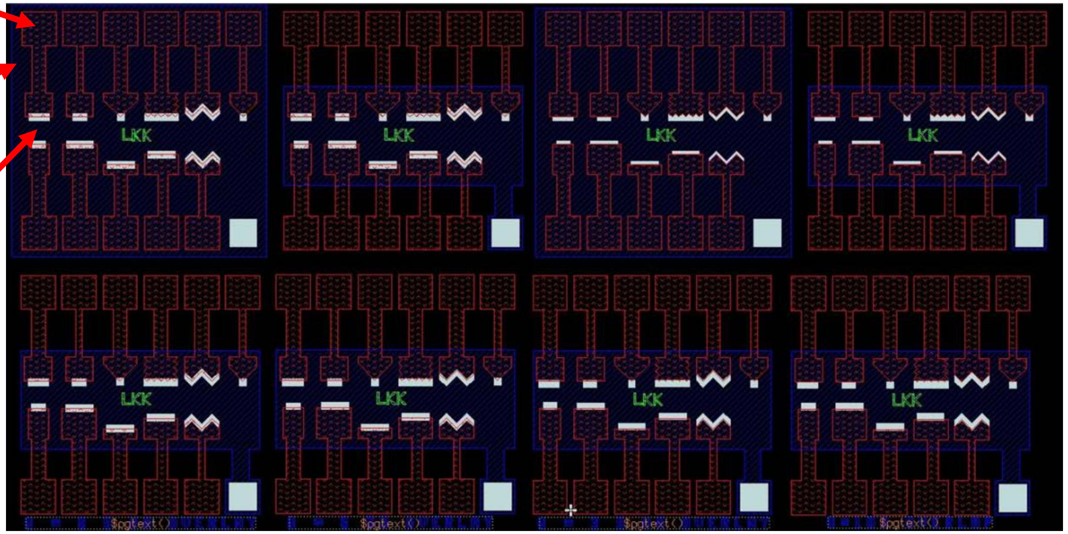
Puchades et al., *J. Mater. Chem. C*, 2015, **3**, 10256-10266

Design

- two-electrode device (anode and cathode) as proof of concept and focus on material and process integration.
  - A bottom layer of Aluminum to act as the anode
  - A middle layer of LTO to define a trench and localize the electron emission
  - A top layer of SWCNT to act as the cathode



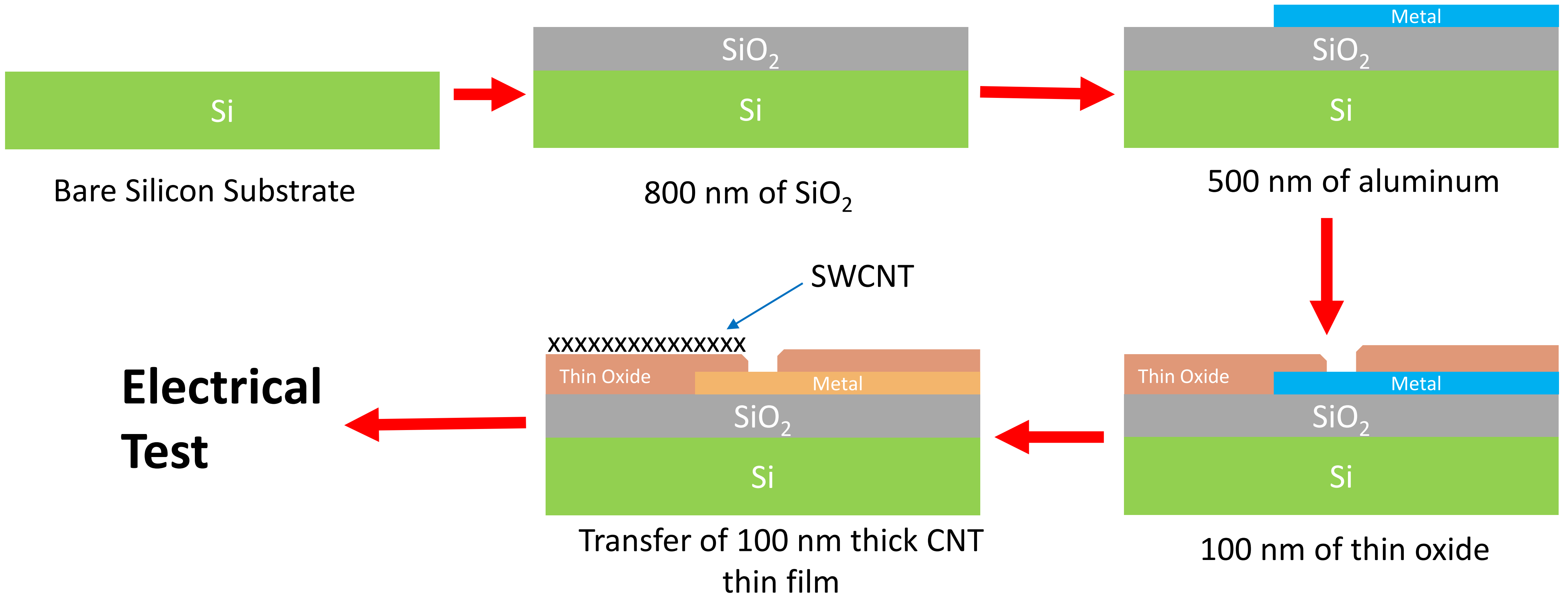




The designs varied based on several factors

- Size of anode layer and if it overlapped the pads and devices
- Size of devices
- Size of Trench and if it overlapped the devices or not

Fabrication Process

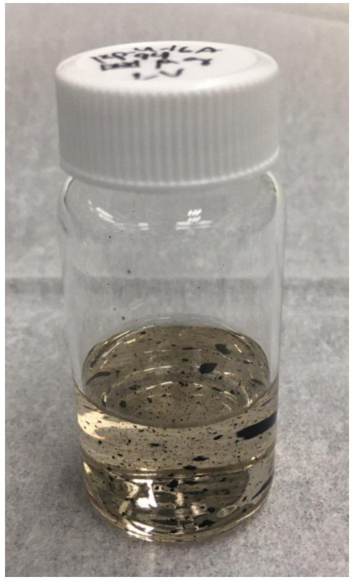


SWCNT Thin Film Process

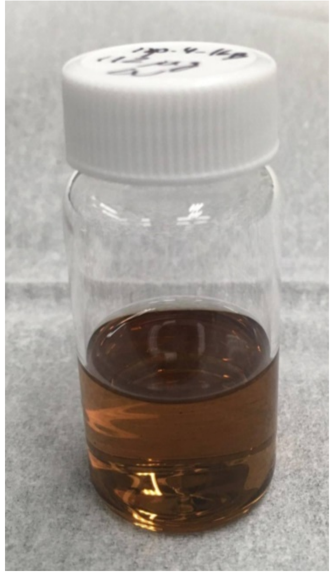
A **<u>thin film transfer process</u>** allows to select desired properties of SWCNTs.

High purity laser vaporized SWCNTs (mixed chirality, 1.2-1.7 nm diameter, electrochemical potential of **0.5-2.0 V vs. SHE**)   are dispersed in chlorosulfonic acid and further individualized with the aid of ultrasonic agitation.

Add Acid (CSA)



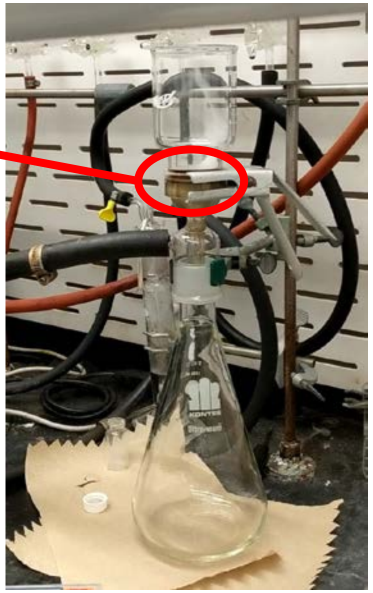
Shake for 1 hour



SWCNT Thin Film Creation

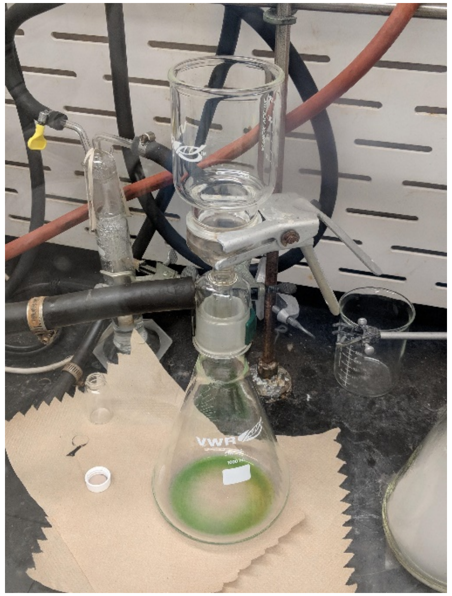
This dispersion of SWCNTs is then transferred onto a ceramic filter by vacuum filtration and the acid is rinsed with acetone. The film must dry for a minimum of 30 minutes with the vacuum on.

Ceramic Filter is clamped between Beaker and Flask



All components are clamped together and ready for Film Creation

Vacuum Filtration is turned on and acid is starting to be rinsed with acetone

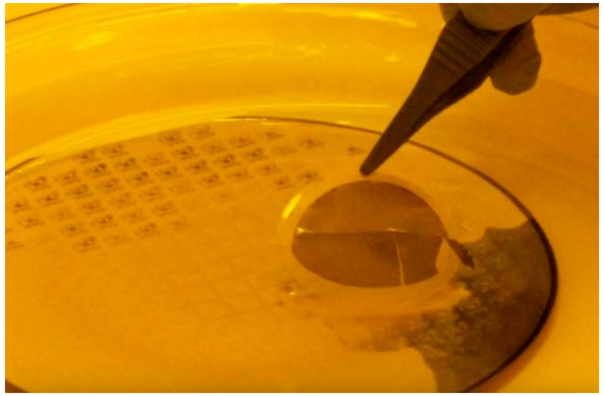


The thin film has been completely rinsed with acetone, and is ready to dry now

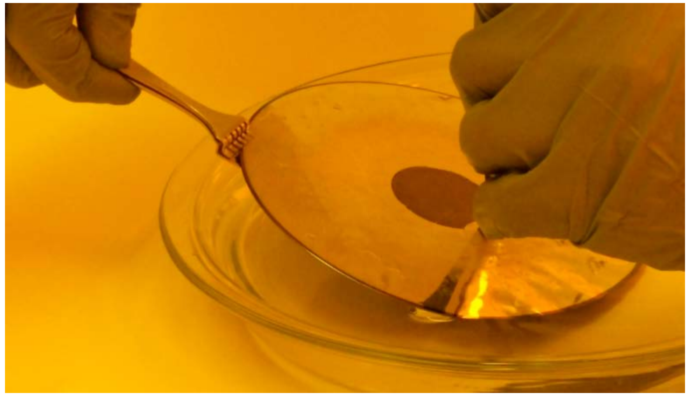
SWCNT Transfer

For SWCNT transfer to occur, the substrate with completed aluminum and LTO layers is dipped into DI water.

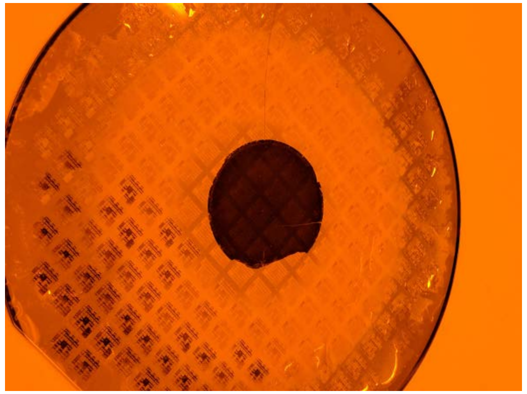
- The ceramic filter with the SWCNT thin film is slowly dispensed into the DI water where the film will slowly separate from the filter and float on the surface of the water.
- The substrate can then be slowly pulled out of the DI water where the SWCNT thin film will stick to the top of the substrate.
- The substrate is then left to dry overnight, and the wafer is ready to move on for patterning and etching of the SWCNT film.



SWCNT thin film is separating from ceramic filter



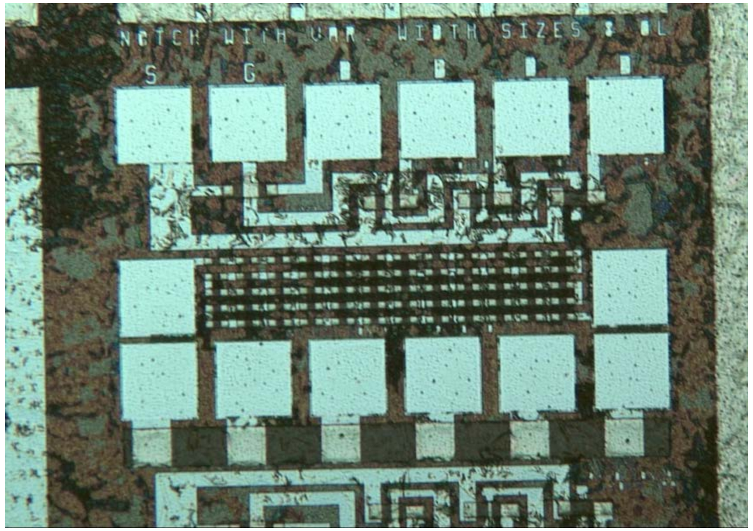
Substrate is being lifted out of the DI water with the SWCNT thin film



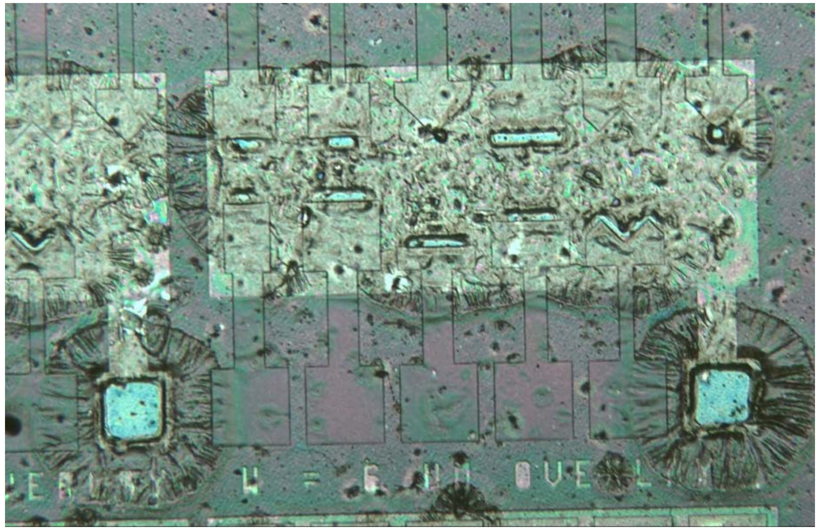
Wafer is being left to dry overnight

SWCNT Thin Film Transfer Microscope Images

After SWCNT Lithography

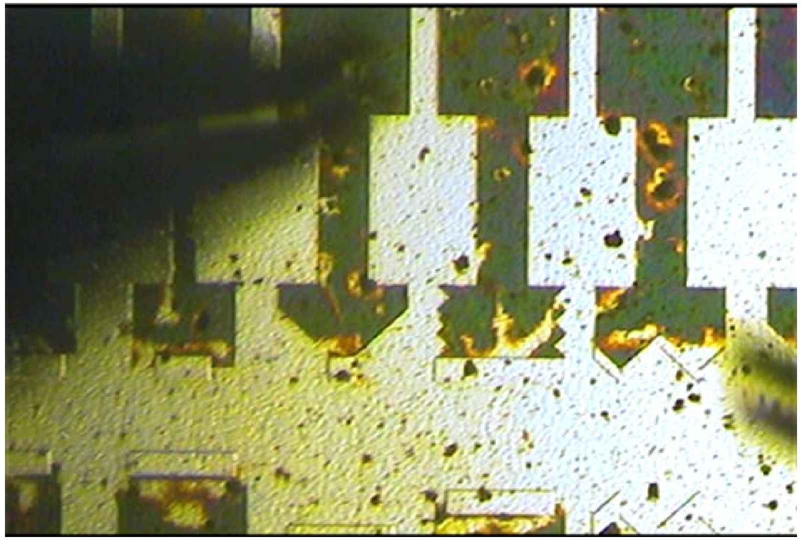


Residue of the transfer process result in visible defects.



Aluminum reflectivity and residue of the transfer process result in visible defects.

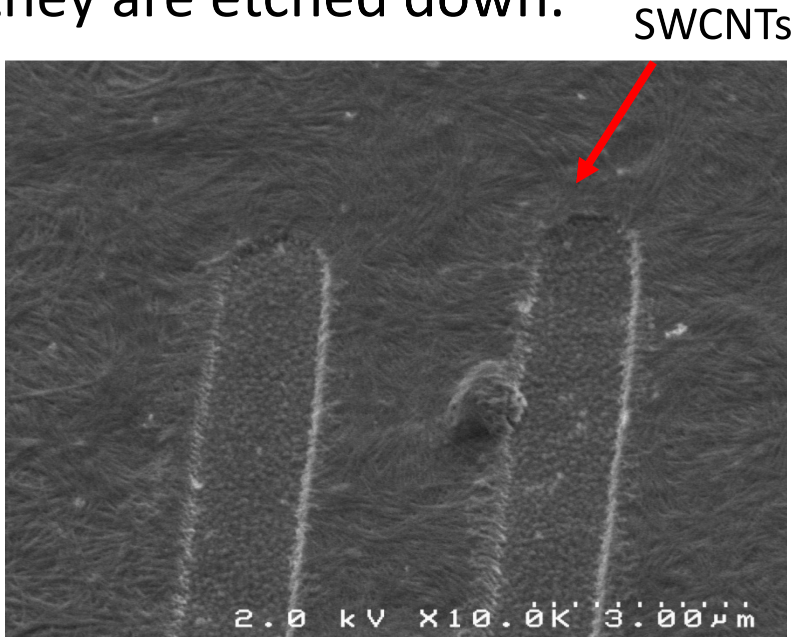
After SWCNT Etch



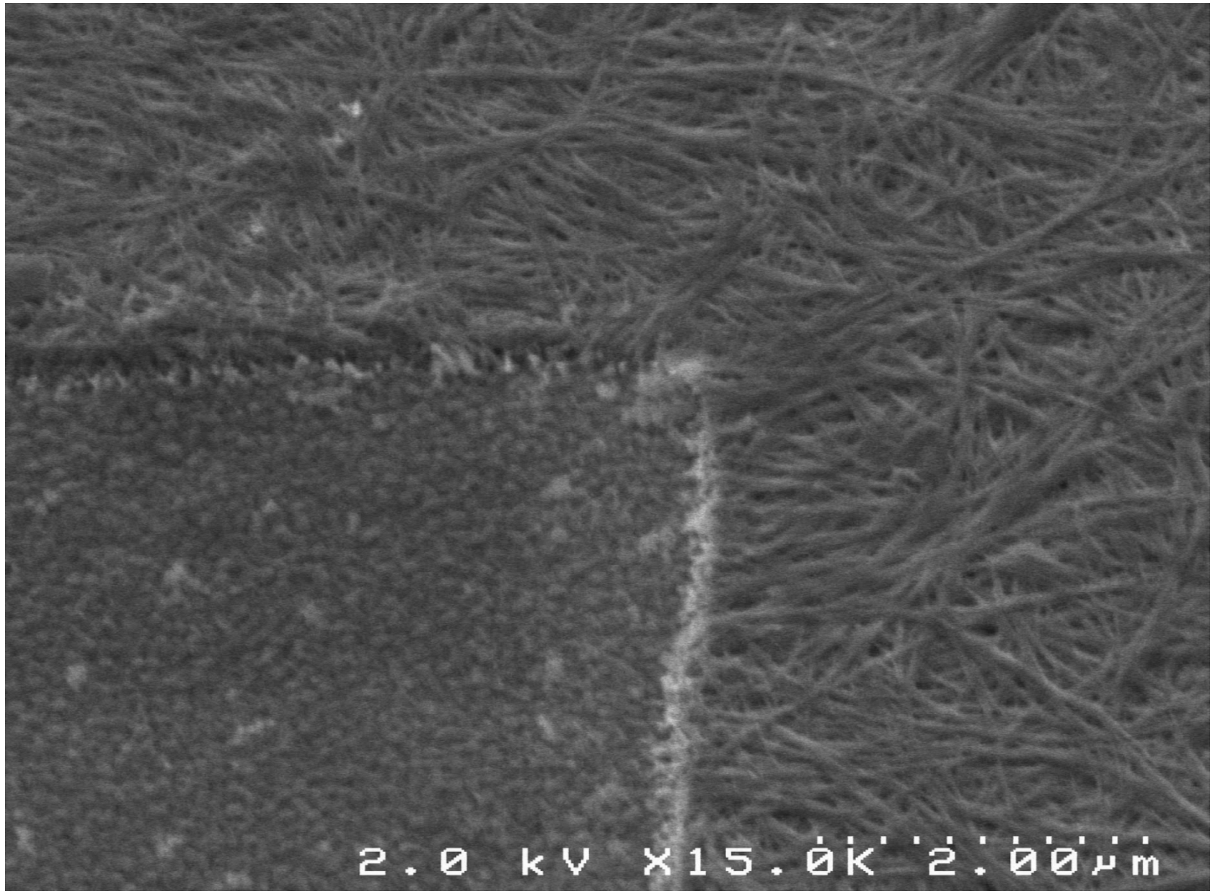
After etch the litho defects result in damaged SWCNT cathode structures.

SWCNT SEM Images After Etch

Scanning Electron Microscopy distinctly show where the SWCNTs exist and where they are etched down.



Contrast difference on SWCNT near the edge of pattern may indicate the etch resulted in damaged or modified nanotubes.

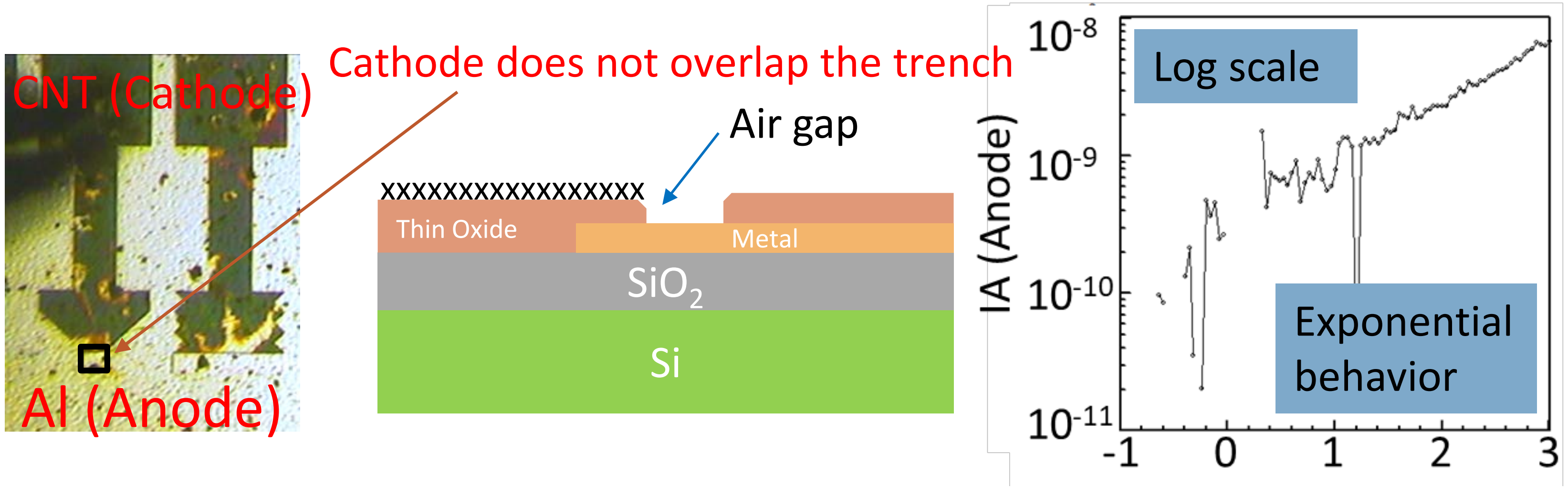


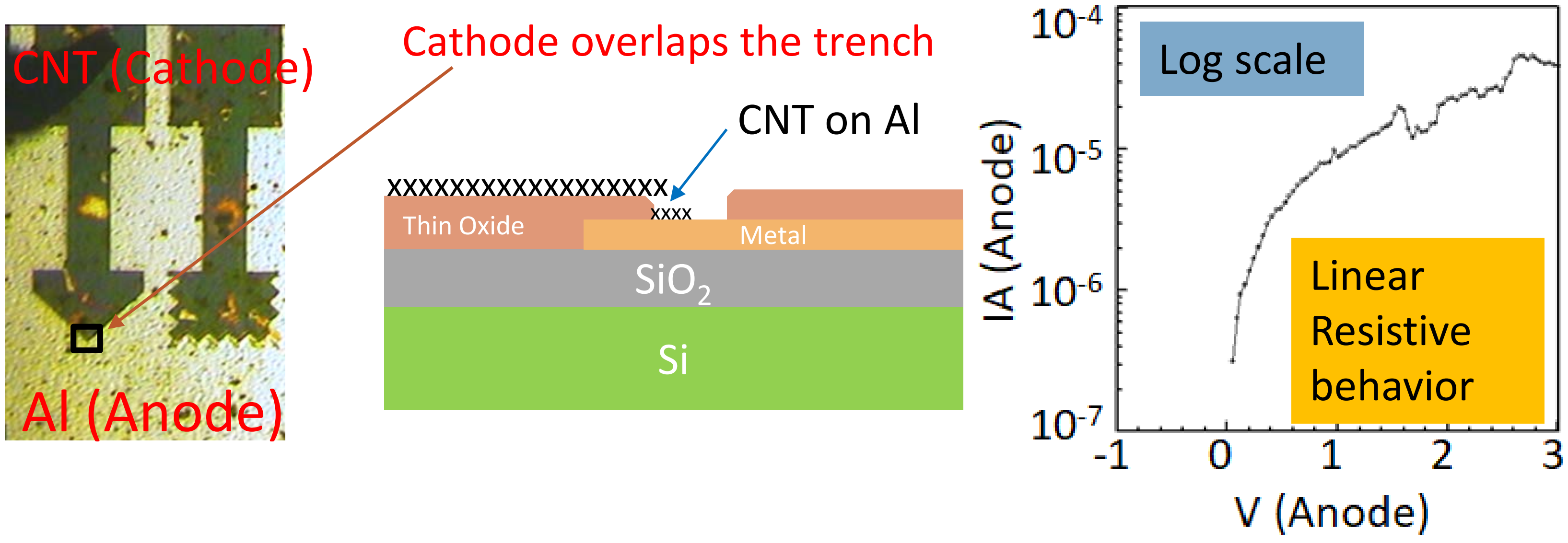
Electrical Test

Preliminary test data may indicate that Fowler-Northeim emission has been achieved under atmospheric conditions.

Top: No emitter overlap (I = 1 nA at 1 V)

Bottom: Emitter overlap results in resistive behavior (I = 10 µA at 1 V, R = 100 kOhm).





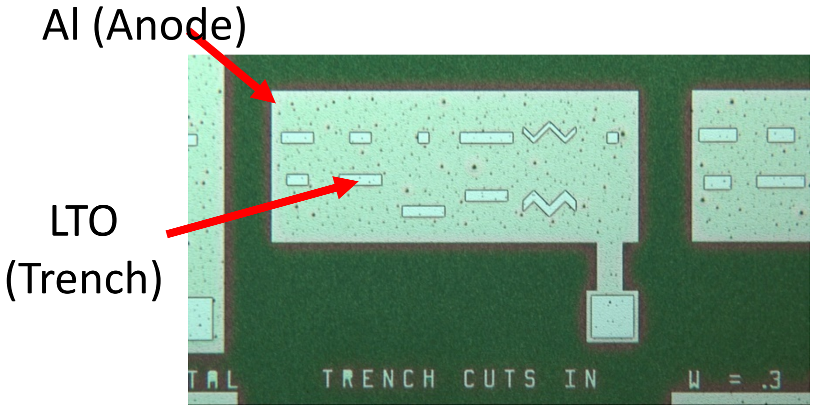
Conclusions

- Proof of concept of field emission device, based on carbon nanotube emitters, with an effective anode-to-cathode distance of 100 nm was designed, fabricated, and tested.
- SWCNT thin film transfer and patterning process needs improvement to reduce defects, protect SWCNTs and improve resolution.
- Fowler-Northeim emission under atmospheric conditions may have been observed.
- Although our devices were able to work, further analysis and characterization must be carried to confirm these results.

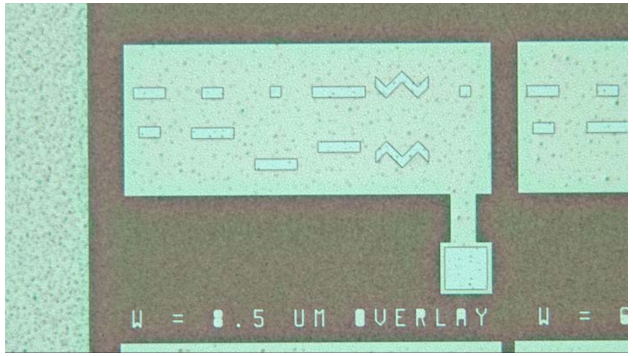
Thin Oxide Layer

After the Aluminum is complete, the next step is putting down a layer of LTO (LowThermal Oxide) to act as the trench of the design. This trench is equal to the cathode-to-anode distance that the electrons will be moving.

- The LTO layer was deposited using the ASM LPCVD in the SMFL where Silane and Oxygen are brought into a heated furnace tube at low pressures to react and grow a thin silicon dioxide film
- This film was grown to be 100 nm and then patterned and etched
- The following microscope images were captures after this process was complet
  - These images include the Aluminum Anode Plate and the LTO Trenches



Before Etch



After Etch